



**THE DATASHEET OF
ZL30162GDG2**



Features

- Fully compliant SEC (G.813) and EEC (G.8262) flexible rate conversion DPLL
- Four programmable digital PLLs/Numerically Controlled Oscillators (NCOs)
- Synchronize to any clock rate from 1 Hz to 750 MHz
- Four programmable synthesizers generate any clock rate from 1 Hz to 750 MHz with maximum jitter below 0.61ps RMS
- Flexible two-stage architecture translates between arbitrary data rates, line coding rates and FEC rates
- Digital PLLs filter jitter from 0.1 mHz up to 1 kHz
- Automatic hitless reference switching and digital holdover on reference fail
- Nine input references configurable as single ended or differential and two single ended input references
- Any input reference can be fed with sync (frame pulse) or clock

Ordering Information

ZL30162GDG2 144 Pin LBGAs Trays
 Pb Free Tin/Silver/Copper
-40°C to +85°C
 Package size: 13 x 13 mm

- Programmable DPLLs can synchronize to sync pulse and sync pulse/clock pair
- Eight LVPECL outputs and eight LVCMOS outputs
- Operates from a single crystal resonator or clock oscillator
- Field programmable via SPI/I²C interface

Applications

- SyncE/SONET/SDH Timing Cards
- Synchronous Ethernet, 10 GBASE-R and 10 GBASE-W
- SONET/SDH, Fibre Channel, XAUI

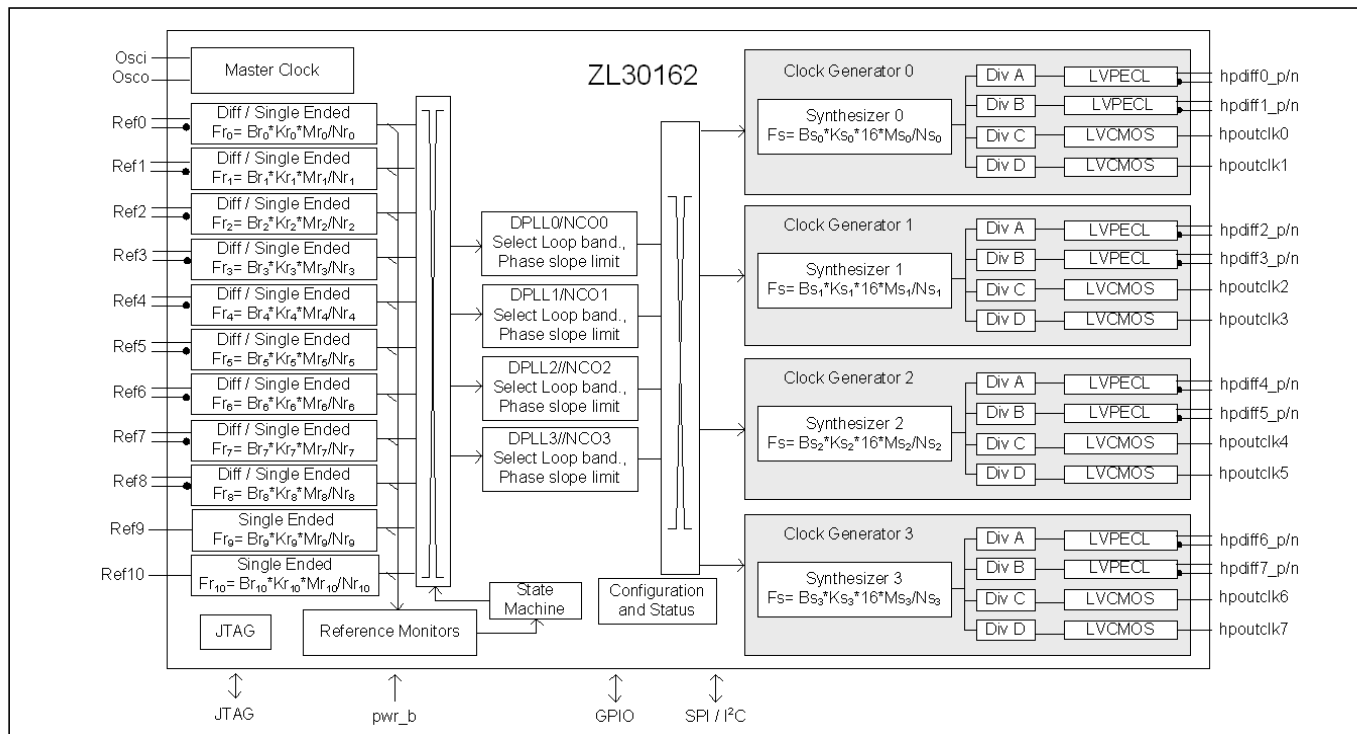


Figure 1 - Functional Block Diagram



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