THE DATASHEET OF

ZL30159GGG20037

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ZL30159
General Purpose Clock Rate Converter
Data Sheet

March 2015

Features

- Precision synthesizer generates any clock-rate from 1 Hz to 177.5 MHz with jitter below 1ps
- Programmable digital PLL synchronize to any clock rate from 1 Hz (1 pps) to 750 MHz
- Input reference configurable as single ended LVCMOS (up to 177.5 MHz) or differential LVPECL (up to 750 MHz)
- Flexible two-stage architecture translates between arbitrary data rates, line coding rates and FEC rates
- Programmable Digital PLL loop filter: 30 mHz, 14 Hz, 28 Hz, 56 Hz, 112 Hz, 224 Hz, 448 Hz or 896 Hz
- Two LVCMOS outputs —from 1 Hz (1 pps) to 177.5 MHz
- Operates from a single crystal resonator or clock oscillator

Ordering Information

ZL30159GGG2	64 Pin LBGA*	Trays

*Pb Free Tin/Silver/Copper

-40°C to +85°C

- Customer defined default device configuration, including input/output frequencies, is available via OTP(One Time Programmable) memory
- Dynamically configurable via SPI/I2C interface and volatile configuration registers

Applications

- General purpose clock rate translator
- GPS receiver clock synthesizer

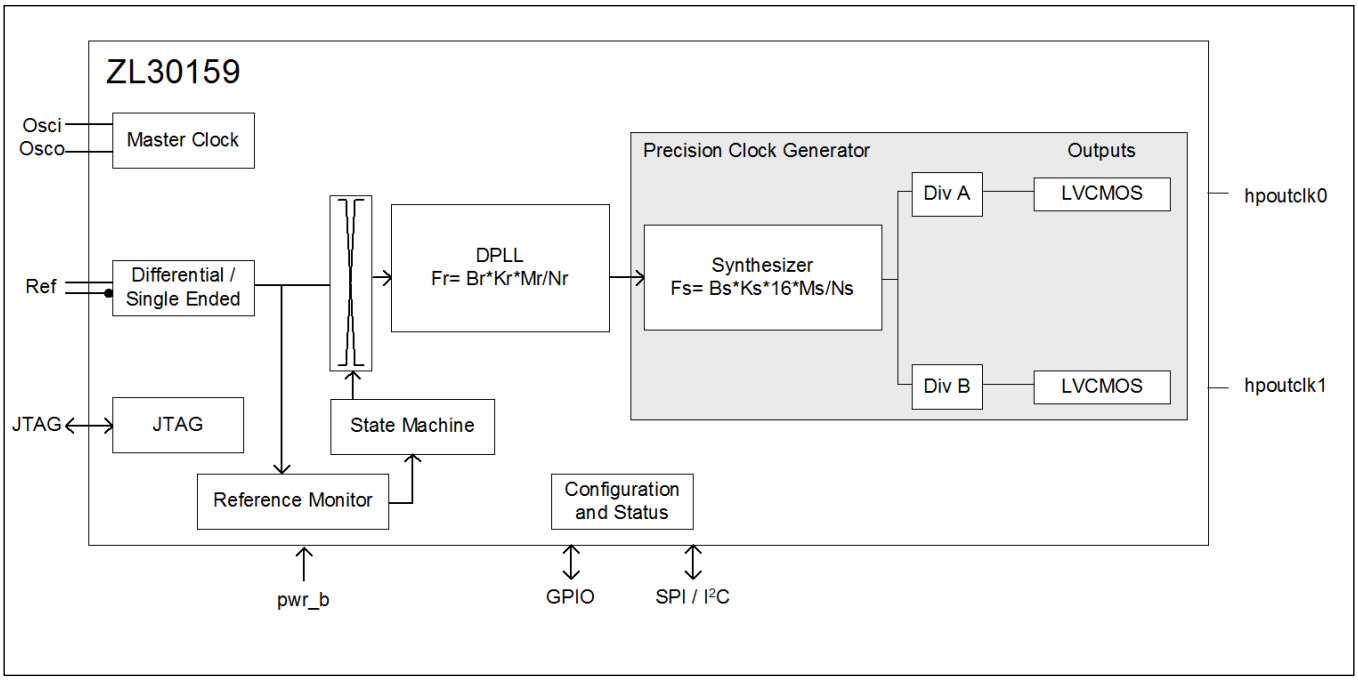

Figure 1 - Functional Block Diagram

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Change Summary

Below are the changes made May 2014 issue to March 2015 issue.

Page	Item	Change
1	Added Features bullet	Included availability of customer defined default configurations
12, 24, 24	Updated section 4.0, 5.0 and added 5.1	Updated to included the availability of Custom OTP configuration
83	12.0, “Package Markings“	Added section 12 for package markings

Below are the changes made from March 2013 issue to May 2014 issue.

Page	Item	Change
36 and 65	Register 0xC6: **chip_revision**	Updated chip revision regisetr to include revH id number
1, 11 ,14,15 ,46	30MHz loop filter	Numerous reference to 30MHz loop filter were corrected to read 30mHz
45	Register 0x30 : **dpll_ctrl**	Changed bits [1:0] to reserved bits with default = 0b00 (DPLL Pull-in and Hold-in range settings available at register 0xED)
57	Register 0x86:0x88: **synth_post_div_A**	Corrected description of bits 17:16
59	Register 0x89:0x8B: **synth_post_div_B**	Corrected description of bits 17:16
22	4.12, “Reset and Configuration Circuit“	Clarified power up conditions for gpio2 and gpio6
74	DC Electrical Characteristics* - High Performance Outputs	Corrected the Sym for line 2 in the table

Below are the changes made in March 2013 issue.

Page	Item	Change
Multiple	Zarlink logo and name reference	Updated to Microsemi® logo and name.
1	, “Ordering Information“	Removed GGG part number.

1.0 Pin Diagram

	1	2	3	4	5	6	7	8
A	NC	NC	NC	avss	filter	avss	osco	avss
B	NC	NC	NC	avdd	filter_ref	avdd	osci	avdd
C	NC	NC	avss	avcore	at	avss	avss	vss
D	avss	avdd	avdd	vss	vss	vss	vdd_io	pwr_b
E	hpoutclk1	hpoutclk0	gpio5	vcore	vss	gpio0	cs_b_asel0	sck_scl
F	avss	avdd	test_en	vcore	vcore	gpio3	gpio2	gpio1
G	gpio6	so_asel1	trst_b	avcore	avss	avdd	tms	tdi
H	gpio4	si_sda	tdo	ref_p	ref_n	NC	NC	tck

1 - A1 corner is identified by metallized markings.

2.0 Pin Description

All device inputs and output are LVCMOS unless it was specifically stated to be differential.

Ball #	Name	I/O	Description
Input Reference			
H4 H5	ref_p ref_n	I	**Input Reference.** Input reference used for synchronization. The positive and negative pair of this input accept a differential input signal. The ref_p input terminal accept a CMOS input reference. Maximum frequency limit on single ended input is 177.5 MHz, and 750 MHz on differential input.
Output Clocks			
E2 E1	hpoutclk0 hpoutclk1	O	**High Performance Output Clock 0 to 1.** This output can be configured to provide any one of the single ended high performance clock outputs. Maximum frequency limit on single ended LVCMOS outputs is 177.5 MHz
Control and Status			
D8	pwr_b	I	**Power-on Reset.** A logic low at this input resets the device. To ensure proper operation, the device must be reset after power-up. The pwr_b pin should be held low for at least 2 ms. This pin is internally pulled-up to V_{DD}. **User can access device registers either 55 ms after pwr_b goes high, or after bit 7 in register at address 0x00 goes high which can be determined by polling address 0x00.**

Table 1 - Pin Description

Ball #	Name	I/O	Description
E6 F8 F7 F6 H1 E3 G1	gpio0 gpio1 gpio2 gpio3 gpio4 gpio5 gpio6	I/O	**General Purpose Input and Output pins.** These are general purpose pins managed by the internal processor based on device configuration. Recommended usage of GPIO include: • DPLL lock indicators • DPLL holdover indicators • Reference fail indicators • Reference select control or monitor • High performance LVCMOS output enable • Host Interrupt Output: flags changes of device status prompting the processor to read the enabled interrupt service registers (ISR). • Microport interface protocol I2C or SPI • Master Clock frequency rate Pins gpio[5:0] are internally pulled down to GND and pin gpio6 is internally pulled up to V_{DD}. **After power on reset, device GPIO[0,1,3,4,5] configure some of device basic functions, GPIO[3] set I2C or SPI control mode, GPIO[1,0] set master clock rate selection. The GPIO[0,1,3] pins must be either pulled low or high with an external 1KΩ resistor as needed for their assigned functions at reset; or they must be driven low or high for 55 ms after reset, and released and used for normal GPIO functions.** **The GPIO[4,5] pins must be either pulled low with external 1KΩ resistors; or they must be driven low for 55 ms after reset, and then released and used for normal GPIO functions.**
Host Interface			
E8	sck_scl	I/O	**Clock for Serial Interface.** Provides clock for serial micro-port interface. This pin is also the serial clock line (SCL) when the host interface is configured for I2C mode. As an input this pin is internally pulled up to V_{DD}.
H2	si_sda	I/O	**Serial Interface Input.** Serial interface input stream. The serial data stream holds the access command, the address and the write data bits. This pin is also the serial data line (SDA) when host interface is configured for I2C mode. This pin is internally pulled up to V_{DD}.
G2	so_asel1	I/O	**Serial Interface Output.** Serial interface output stream. As an output the serial stream holds the read data bits. This pin is also the I2C address select when host interface is configured for I2C mode.
E7	cs_b_asel0	I	**Chip Select for Serial Interface.** Serial interface chip select, this is an active low signal. This pin is also the I2C address select when host interface is configured for I2C mode.This pin is internally pulled up to V_{DD}.
APLL Loop Filter			
A5	filter	A	**External Analog PLL Loop Filter terminal.**

Table 1 - Pin Description (continued)

Ball #	Name	I/O	Description
B5	filter_ref	A	**Analog PLL External Loop Filter Reference.**
JTAG (IEEE 1149.1) and Test			
F3	test_en	I	**Test Mode Enable.** A logic high at this pin enables device test modes. This pin is internally pulled down to GND. Connect this pin to GND.
C5	at	A-I/O	**Analog PLL Test.** Test pin for analog PLL. Leave unconnected.
H3	tdo	O	**Test Serial Data Out.** JTAG serial data is output on this pin on the falling edge of tck. This pin is held in high impedance state when JTAG scan is not enabled.
G8	tdi	I	**Test Serial Data In.** JTAG serial test instructions and data are shifted in on this pin. This pin is internally pulled up to V_{DD}. If this pin is not used then it should be left unconnected.
G3	trst_b	I	**Test Reset.** Asynchronously initializes the JTAG TAP controller by putting it in the Test-Logic-Reset state. This pin should be pulsed low on power-up to ensure that the device is in the normal functional state. This pin is internally pulled up to VDD. If this pin is not used then it should be connected to GND.
H8	tck	I	**Test Clock.** Provides the clock to the JTAG test logic. This pin is internally pulled up to V_{DD}. If this pin is not used then it should be connected to GND.
G7	tms	I	**Test Mode Select.** JTAG signal that controls the state transitions of the TAP controller. This pin is internally pulled up to V_{DD}. If this pin is not used then it should be left unconnected.
Master Clock			
A7	osco	A-O	**Oscillator Master Clock.** For crystal operation, a crystal is connected from this pin to osci. Not suitable for driving other devices. For clock oscillator operation, this pin is left unconnected.
B7	osci	I	**Oscillator Master Clock.** For crystal operation, a crystal is connected from this pin to osco. For clock oscillator operation, this pin is connected to a clock source.
Power and Ground			
D7	V_{DD-IO}		**Positive Supply Voltage IO.** $3.3V_{DC}$ nominal.
E4 F4 F5	V_{CORE}		**Positive Supply Voltage.** $+1.8V_{DC}$ nominal.
B4 B6 B8 D2 D3 F2 G6	AV_{DD}		**Positive Analog Supply Voltage.** $+3.3V_{DC}$ nominal.

Table 1 - Pin Description (continued)

Ball #	Name	I/O	Description
C4 G4	AV_{CORE}		**Positive Analog Supply Voltage.** +1.8V_{DC} nominal.
C8 D4 D5 D6 E5	V_{SS}		**Ground.** 0 Volts.
A4 A6 A8 C3 C6 C7 D1 F1 G5	AV_{SS}		**Analog Ground.** 0 Volts.
No Connect			
A1 A2 A3 B1 B2 B3 C1 C2 H6 H7	NC		**Not connected to the die.** Connect to the GND.

Table 1 - Pin Description (continued)

3.0 Application Example

The device integrates a digital PLL and a high-speed low-jitter clock synthesizer. The digital PLL locks to reference frequencies as low as 1 Hz while maintaining loop stability and while maintaining the device's low-jitter generation. The digital PLL ensures automatic stand-by mode on reference fail (holdover) preventing bit errors on the transmission links. The digital PLL implements loop filters with settings as low as 30 mHz to clean noisy references; or as high as 896 Hz to closely track less noisy references. The high-speed low-jitter clock synthesizer generates clocks with frequencies as high as 177.5 MHz with typical jitter performance below 1 ps RMS. The digital PLL plus high-speed synthesizer architecture allows the device to easily convert between SONET/SDH and Ethernet frequencies, with or without FEC scaling or line coding. Figure 2 shows an example application where ZL30159 is used to generate 25 MHz and 125 MHz (or any other two frequencies) from 1pps (1 Hz) input provided by GPS receiver. For applications where ZL30159 is synchronized to 1pps signal, ZL30159 loop bandwidth has to be 30 mHz.

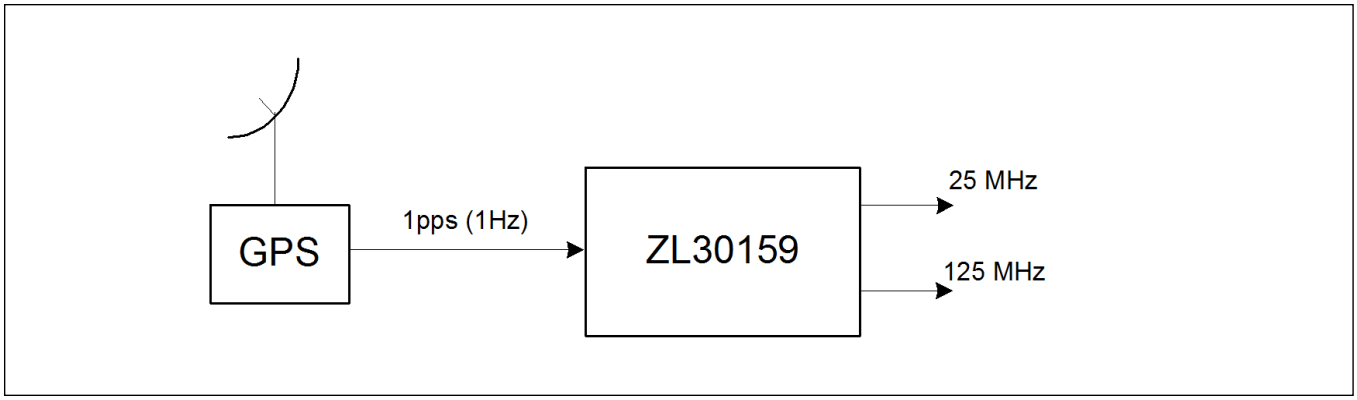


Figure 2 - Application Diagram

4.0 Functional Description

The functional block diagram of the device is shown in Figure 1. The ZL30159 is General Purpose Clock Rate Converter that can be configured by any of the following methods; power-up with its default configuration; power-up with a custom OTP (One Time Programmable) configuration; after power-up it can be dynamically configured via the SPI/I2C port. Configurations set via the SPI/I2C are volatile and will need to be rewritten if the device is reset or powered-down. The SPI/I2C port is also used to access the status registers. The ZL30159's detailed operation is described in the following sections.

4.1 Input Sources

The device has 2 input sources: one input reference (single ended or differential) and one oscillator clock source (oscillator or xtal).

The device master clock frequency is configured on reset via external voltage levels on GPIO[1:0] pins. The recommended frequency of the master clock is 24.576 MHz or 20 MHz.

The device synchronizes (locks) to any input reference which is a 1 Hz, 1 kHz multiple, or it synchronizes (locks) to any input reference which is an (M/N x 1 kHz) multiple (FEC rate converted) where M and N are 16 bits wide.

Input frequency is specified by programming four 16 bit registers: Base (B), Multiplier (K), M and N where input frequency is equal B * K * M/N. For example, to set the device to accept 1 Hz reference, the user will need to set B, K, M and N to 1. ZL30159 Evaluation Board GUI provides recommended B, K, M and N values for any required input reference frequency.

The device input reference frequency is programmed during initialization, change of input reference frequency can be supported if DPLL was forced in to Holdover mode before a frequency change.

The device accepts an input reference with maximum frequency of 177.5 MHz through single ended LVCMOS input (or 750 MHz frequency through differential inputs) and a minimum frequency of 1 Hz.

4.2 Input Reference Monitoring

The input reference is monitored by three reference monitor schemes. They indicate abnormal behavior of the reference signal, for example; drift from its nominal frequency or excessive jitter.

- **Loss of Signal Monitor (LOS)**: LOS is an external signal, fed to one of ZL30159 pins. LOS is typically generated by a PHY device whose recovered clock is fed to ZL30159 reference input. PHY device will generate LOS signal when it cannot reliably extract the clock from the line. User can set one of GPIO pins as LOS input by programming corresponding GPIO register.
- **Coarse Frequency Monitor (CFM)**: The CFM monitors input reference frequency for 1.25 ms so that it can quickly detect large changes in frequency. CFM limit for each input reference can be selected in corresponding scm_cfm_limit_ref registers with range from 0.1% to 50%. If the CFM limit is exceeded, then CFM failure is declared for corresponding reference.
- **Precise Frequency Monitor (PFM):** The PFM block measures the frequency accuracy of the reference over a 10 second interval. To ensure an accurate frequency measurement, the PFM measurement interval is re-initiated if phase or frequency irregularities are detected by the CFM. The PFM provides a level of hysteresis between the acceptance range and the rejection range to prevent a failure indication from toggling between valid and invalid for references that are on the edge of the acceptance range. PFM limit for each reference can be selected in pfm_range registers. When determining the frequency accuracy of the reference input, the PFM uses the external oscillator's output frequency (f_{ocsi}) as its point of reference. PFM limits can be set in pfm_range register at address 0xF7.
- **Single Cycle Monitor (SCM)**: This detector measures rising to rising edge and falling to falling edge periods. If either of them exceeds predefined SCM limit then SCM failure is declared. SCM limit for each

input reference can be selected in corresponding scm_cfm_limit_ref registers with range from 0.1% to 50%. The limits are input frequency dependent. Please refer to the description in scm_cfm_limit_ref registers

- **Guard Soak Timer (GST):** Timer associated with the CFM and SCM modules to disqualify the reference input signal (see Table 2)

The monitor failure indicator is flagged in the status register and have associated mask bit, as follows:

- Reference Fail Mask: RefFailMask<3:0> in register at address 0x09: these bits mask the LOS, SCM, CFM, GST failure indicators and Ref Fail PFM Mask in register at address 0xF5.
- Holdover Mask for the reference: HOMask<3:0> in register at address 0x34, these bits mask the he LOS, SCM, CFM, GST failure indicators and DPLL Holdover Mask on PFM in register at address 0xF4 that are used to put device into auto-holdover on reference failure.
- MSB bit for GST and LSB bit for LOS

The single cycle and coarse monitor failure flags feed a timer (Guard Soak Timer) that disqualifies the reference input signal when the failures are present for more than the period of time defined in Table 2.

Guard Soak Timer Control bits in control register	Time to disqualify a reference	Notes
00	minimum delay possible	
01	10 ms	
10	50 ms	default value
11	2.5 s	

Table 2 - Guard Soak Time To Disqualify A Reference

The Guard Soak Timer that is used for the CFM and SCM modules has a built-in decay time hysteresis according to Table 3 (Timer to Qualify a reference) to prevent flickering of status bits at the threshold boundaries.

The Timer to Qualify a reference is a multiple of the Guard Soak Timer. Table 3 shows the multiplication factor to multiply the Guard Soak Timer to calculate the time to qualify a reference.

Control bits to control the Timer to qualify a reference	Multiples of the Guard Soak Time to qualify a reference	Notes
00	2	
01	4	Default value
10	16	
11	32	

Table 3 - Guard Soak Time To Qualify A Reference

When a GPIO pin is used as a reference fail indicator, it indicates a valid reference if:

- The SCM does not detect phase hits, nor complete loss of clock or RefFailMask<1> is at logic “0”
- The CFM does not detect phase irregularity or RefFailMask<2> is at logic “0”
- The Guard Soak Time is triggered or RefFailMask<3> is at logic “0”

4.2.1 DPLL General Characteristics

Pull-in Hold-in range

The DPLL supports pull-in/hold-in of +/-52 ppm, +/-130 ppm or +/-400 ppm or +/-3900 ppm.

DPLL bandwidth (jitter/wander transfer)

The DPLL supports the following first order filtering cut-off frequencies (30 mHz, 14 Hz, 28 Hz, 56 Hz, 112 Hz, 224 Hz, 448 Hz and 896 Hz), DPLL bandwidth is determined during initialization. When changing any parameter such as loop bandwidth, phase slope limit, input/output frequency etc, user should first put the device into the holdover or free run mode, program required changes, and then put the device back to the normal mode. Same procedure should be followed during the initialization phase.

The DPLL locks to an input reference and provides stable low jitter output clock if the selected loop bandwidth is less than 1/30th the input reference frequency. As an example, a 19.44 MHz reference could deploy a bandwidth up to 896 Hz, and a 1 kHz input reference would deploy a loop bandwidth of 14 Hz. For 8 kHz reference we recommend a maximum loop bandwidth of 56 Hz. 1 Hz input reference, requires loop bandwidth of 30 mHz. Such narrow loop bandwidth (30 mHz) requires very stable master crystal oscillator (TCXO or OCXO)

On the power up when the device is fed with low frequency reference such as 1 Hz with 30mHz loop bandwidth, the frequency lock will be achieved relatively fast. However, the phase lock will take longer time because the device needs to pull the phase of the output clock for up to half a second before the input and output get aligned. To speed up the phase lock time user should cycle device between normal and holdover mode three times as described below:

- On the power up the device is fed with 1pps reference

- Initialise the device by programming it via SPI/I2C bus and set it to normal mode

- Loop three times:

    - Wait for 50 seconds

    - Set the device to the holdover mode

    - Wait for 5 milliseconds

    - Set the device to the normal mode

- End loop

Jitter/Wander Generation

Jitter generation performance (detailed in Table 9 -, “Jitter Generation Specifications - HPOUT Outputs“).

Wander generation of this device is applicable only when 30 mHz loop bandwidth is used. In this case wander generation is solely dependent on short term stability of master crystal oscillator. For wider loop bandwidths of 14 Hz or higher, wander generation of this device is negligible.

Phase Transients

The Microsemi device offers the following phase slope limiting options: 61 usec/sec, 7.5 usec/sec, 0.885 usec/sec or unlimited. If required phase slope limit is 0.885 usec/sec or 7.5 usec/sec, user should first set the device to unlimited phase slope and change it to required phase slope limit (0.885 usec/sec or 7.5 usec/sec) only after the device has achieved lock.

Holdover Stability

DPLL initial holdover accuracy is better than 50 ppb.

Input Tolerance Criteria

Input tolerance indicates that the device tolerates certain jitter, wander and phase transients at its input reference while maintaining outputs within an expected performance and without experiencing any alarms, or holdover conditions. Input tolerance is associated with input reference source characteristics and the standards associated with input reference type.

DPLL Monitoring

The DPLL provides lock and holdover indicators.

The lock time is dependent on employed loop bandwidth. The device has a lock time of less than 1 sec for all available DPLL loop bandwidth selections except 30 mHz.

The frequency lock time for 30 mHz loop bandwidth is up to 90 seconds. However, the phase lock is dependent on the input and output period—how far the output phase has to move to get phase aligned with the input phase. The slowest phase lock time will be for clock with maximum period (minimum frequency) which is 1 pps (1 Hz). For 1 pps, the phase lock time will be up to 20 minutes. To speed up the lock time for 1 pps clock, user should toggle the device though the holdover mode after 1 minute (normal mode - after 1 minute go to holdover mode and back to normal mode).

4.2.2 DPLL States

The device DPLL supports three states: Free-run, Normal (Locked) and Holdover. The Holdover and Free-run states are used to cope with reference impairments.

Each of these modes have a corresponding state in the internal State Machine described as follows:

Freerun State: the Freerun state is entered when synchronization to the reference is not required or is not possible. Typically this occurs immediately following system power-up. In the Freerun State, the device provides timing and synchronization signals which are based on the master clock frequency (supplied to osci pin) only, and are not synchronized to the reference input signals. The freerun accuracy of the output clock is equal to the accuracy of the master clock (osci). So if a ±20 ppm freerun output clock is required, the master clock must also be ±20 ppm.

Holdover State: the Holdover State is typically entered when input reference is temporarily disrupted. In the Holdover State, the device provides output clocks which are not locked to an external reference signal, but are based on storage techniques. The storage value is determined while the device is in Normal Mode and locked to an external reference signal. Initial holdover accuracy is a function of DPLL while holdover drift is reliant on the drift of the master clock (osci).

Normal State: the Normal State is entered when a valid reference clock is available for synchronization. In the Normal State the device provides output clocks which are synchronized to the input reference. From a reset condition - if a valid input reference is available - the device takes less than a second (lock time) to output signals which are synchronized (phase and frequency locked) to the reference input.

4.2.3 DPLL Rate Conversion Function and FEC Support

The DPLL supports rate conversion with a 16 bit forward divider and a 16 bit feedback divider.

The DPLL provides up scaling and down scaling functions.

The DPLL has the ability to switch from normal rate (before FEC is negotiated) to FEC rate and vice versa.

The DPLL supports simple rate conversion (i.e., take in 19.44 MHz and create 255/238 FEC SONET clock of 666.51 MHz), and supports double rate conversion (i.e., take in 19.44 MHz, create FEC 10 GbE clock of 644.5313, which is 66/64 rate converted 625 MHz, or create 690.5692 which is 255/238X66/64 rate converted 625 MHz)

The following is just an example of the frequencies that can be supported (many more frequencies can be supported):

- **GbE:**
  - 25 MHz
  - 125 MHz
- **XAUI (chip to chip interface, which is a common chassis to chassis interface)**:
  - 156.25 MHz or x2 or x4 version
- **OC-192/STM-64:**
  - 155.52 MHz or x2 or x4 version
  - 155.52 MHz x 255/237 (standard EFEC for long reach) or x2 or x4 version
  - 155.52 MHz x 255/238 (standard GFEC for long reach) or x2 or x4 version
- **10 GbE:**
  - 156.25 MHz which is 125 MHz x 10/8 or x2 or x4 version
  - 155.52 MHz x 66/64 or x2 or x4 version
  - Long reach 10GE might require the following frequencies with simple rate conversion: (156.25 MHz x 255/237) and (156.25 MHz x 255/238).
- The following frequencies with double rate conversion: (155.52 MHz x 66/64 x 255/237) or (155.52 MHz x 66/64 x 255/238) and (156.25 MHz x 66/64 x 255/238) or (156.25 MHz x 66/64 x 255/238). Also, user can use x2 or x4 version of the listed frequencies.
- Application Note ZLAN-267 explains how to generate the most common frequencies.

4.2.4 DPLL Input to Output And Output to Output Phase Alignment

Techniques offered for Phase Alignment

When the output clock is locked to a jitter free and wander free input clock, input to output latency is expected to have a typical error of 0 nsec.

The coarse and fine phase adjustments allow for input to output and output to output latency corrections to compensate for PCB load delay, as detailed in 4.6, “Output Drivers“.

4.3 Frequency Synthesis Engine

The device frequency synthesis engine is comprised of a hardware DCO and an analog jitter filtering APLL with built-in digital jitter attenuation scheme. The ultra low jitter frequency synthesis engine can generate output clocks which meet the jitter generation requirements detailed in Table 9 -, “Jitter Generation Specifications - HPOUT Outputs“.

The frequency synthesis engine’s APLL requires an external RC loop filter as described in section 4.13

The frequency synthesis engines can generate any clock which is (M/N X 1 kHz) multiple (FEC rate converted clock). The M and N are 16 bits wide.

When the DPLL is locked to the input reference, the DCO external control can be used. The DCO external control allows for the calibration of the DCO center frequency to adjust for external system oscillator center frequency.

4.4 Dividers and Skew Management

The device has 2 independent dividers associated with frequency synthesis engine.

The divider engines can generate output clocks between 1 Hz and 177.5 MHz with 50% duty cycle.

The divider modules generating the single ended output clocks provides the ability to manage the phase skew of the output clock by a coarse step equal to the internal high speed clock period.

The single ended generated output clocks can be stopped either on rising or falling edge (programmed through serial interface or GPIO).

4.5 Output Multiplexer

Figure 3 shows the multiplexing configuration that is supported.

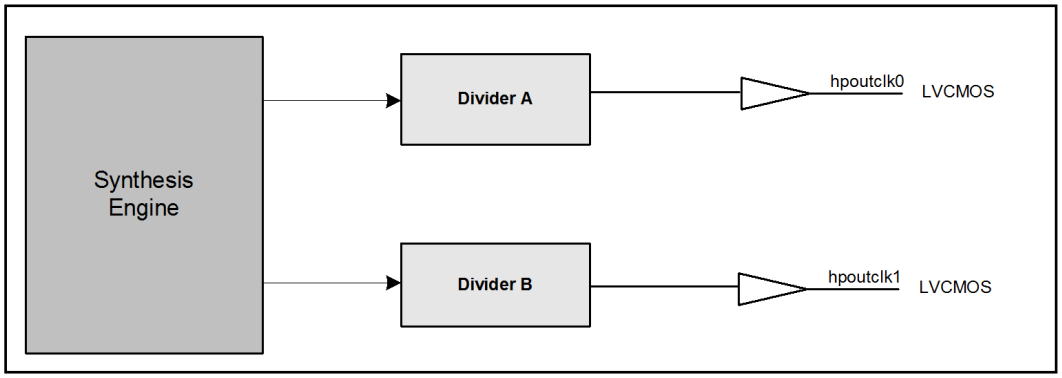


Figure 3 - Output Clocks Muxing Configuration

4.6 Output Drivers

The device has 2 high performance (HP) single ended (LVCMOS) outputs.

High Performance (HP) single ended driver (LVCMOS) supports the jitter specification detailed in Table 9 -, “Jitter Generation Specifications - HPOUT Outputs“ and a maximum speed of 177.5 MHz.

High performance LVCMOS outputs (hpoutclkx) should be terminated at the source with 22 Ω resistor as shown in Figure 4.

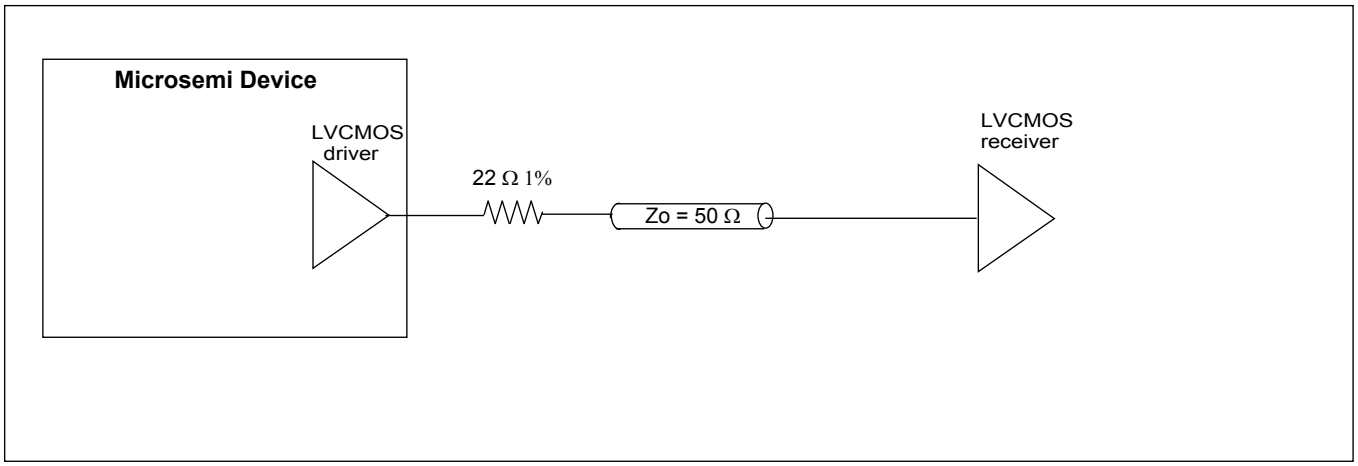


Figure 4 - Terminating HP LVCMOS Outputs

4.7 Input Buffers

ZL30159 has one reference input ref_p/ref_n that can work as either single ended or differential. By default ref is single ended. This can be changed by programming ref_config register at address 0x0A.

Input frequency range for differential input is: 1 kHz to 750 MHz; for single ended input is: 1 kHz to 177.5 MHz.

Differential reference input need to be properly terminated and biased as shown in Figure 5 and Figure 6 for LVPECL and Figure 7 and Figure 8 for LVDS drivers. When terminating LVPECL signal, it is necessary either to adjust termination resistors for DC coupling or to AC couple the LVPECL driver because ZL30159 differential input have different common mode (bias) voltage than LVPECL receivers. Thevenin termination (182 Ω and 68 Ω resistors) provide 50 ohm equivalent termination as well as biasing of the input buffer for DC coupled line. For AC

coupled line, Thevenin termination with 127 Ω and 82 Ω resistors should be used as shown in Figure 6. The value of the AC coupling capacitors will depend on the minimum reference clock frequency. The value of 10 nF is good for input clock frequencies above 100 MHz. For lower clock frequencies capacitor values will have to be increased.

Terminations for DC and AC coupled LVDS line are shown in Figure 7 and Figure 8 respectively. Differential input biasing is provided by LVDS driver in case of DC coupling (Figure 7), whereas for AC coupling (Figure 8) biasing is generated by 12 kΩ and 8.2 kΩ resistors. In both cases, the line is terminated with 100Ω.resistor.

For single ended CMOS input, ref_n input needs to be connected to the ground as shown in Figure 9. The value of series termination resistor will depend on CMOS output driver but the most common values are 33 Ω and 22 Ω.

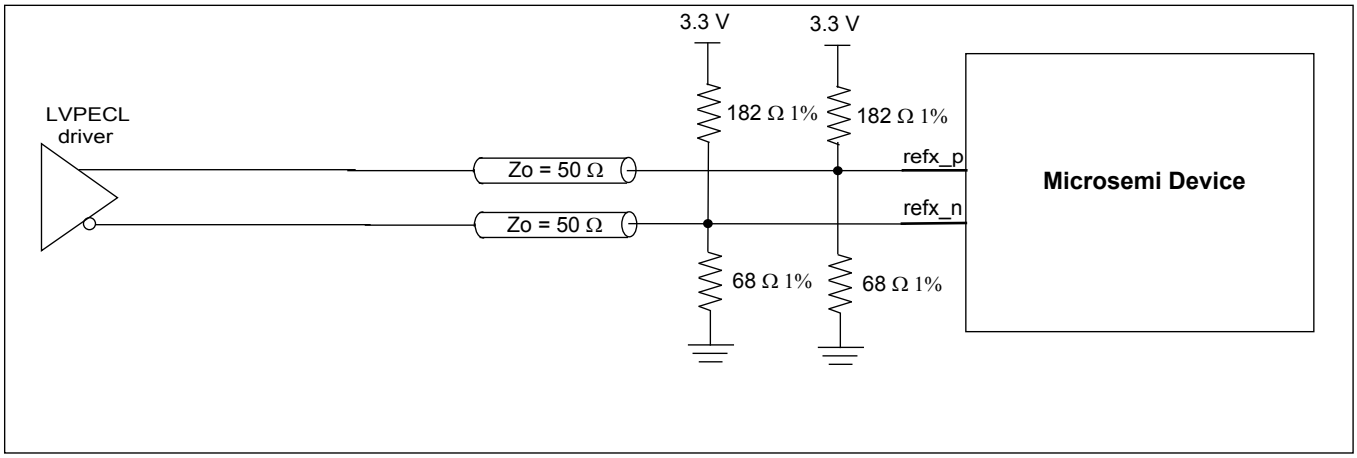


Figure 5 - Differential DC Coupled LVPECL Termination

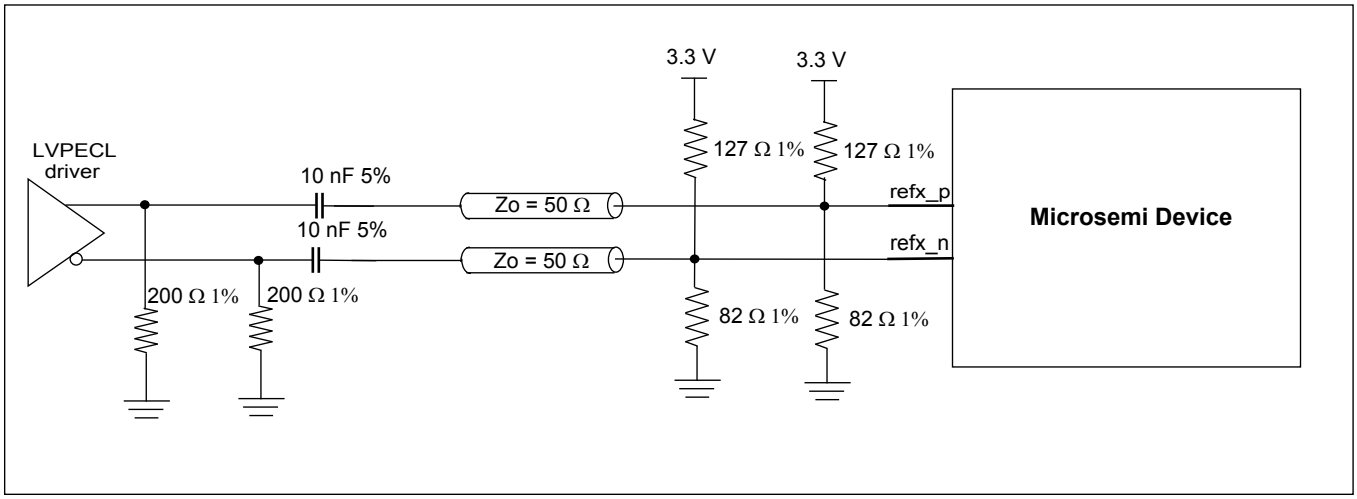


Figure 6 - Differential AC Coupled LVPECL Termination

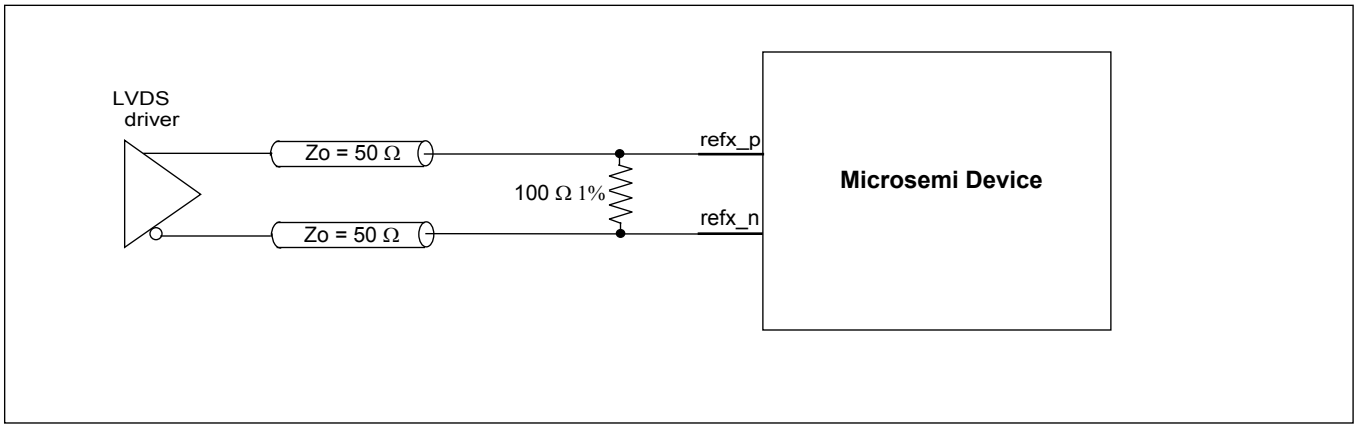


Figure 7 - Differential DC Coupled LVDS Termination

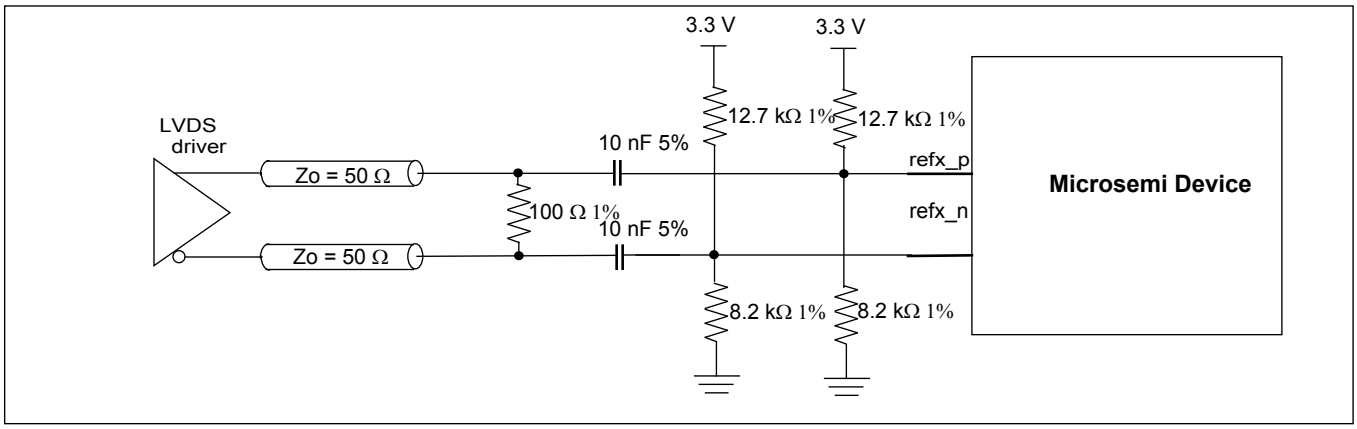


Figure 8 - Differential AC Coupled LVDS Termination

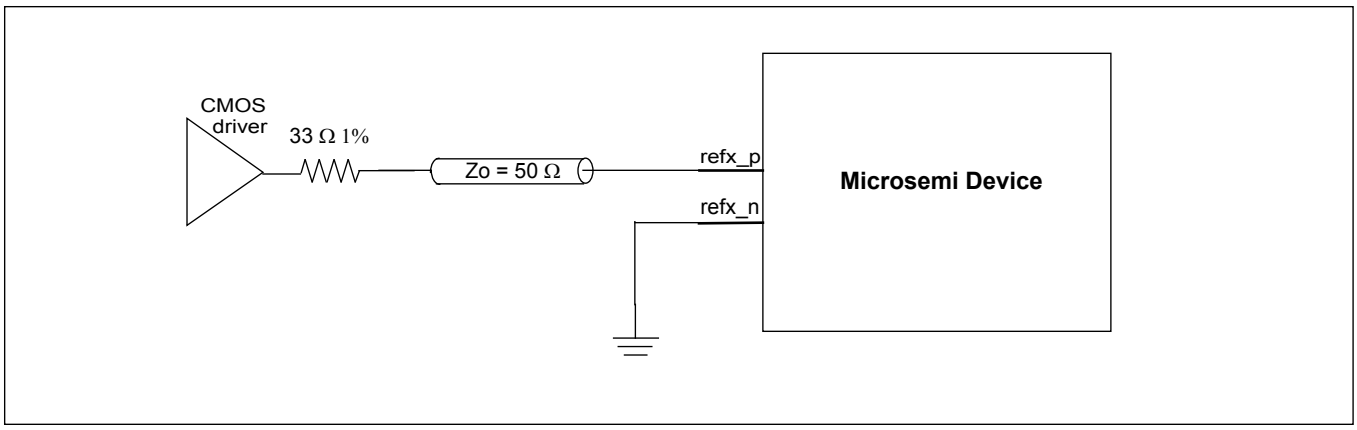


Figure 9 - Single Ended CMOS Termination

4.8 Master Clock Interface

The master oscillator determines the DPLL's free-run frequency accuracy and holdover stability. The reference monitor circuitry also uses this frequency as its point of reference (0 ppm) when making frequency measurements. The master clock interface was designed to accept either a free-running clock oscillator (XO) or a crystal (XTAL). Refer to application note ZLAN-68 for a list of recommended clock oscillators.

4.9 Clock Oscillator

When using a clock oscillator as the master timing source, connect the oscillator's output clock to the **osci** pin as shown in Figure 10. The connection to osci should be direct and not AC coupled. The **osco** pin must be left unconnected.

When using crystal resonator as the master timing source, connect crystal between **osci** and **osco** pins as shown in Figure 10. Crystal should have bias resistor of 1 MΩ and load capacitances C1 and C2. Value of load capacitances is dependent on crystal and should be as per crystal datasheet. Crystal should be a fundamental mode type -- not an overtone. See ZLAN-68 for crystal recommendation.

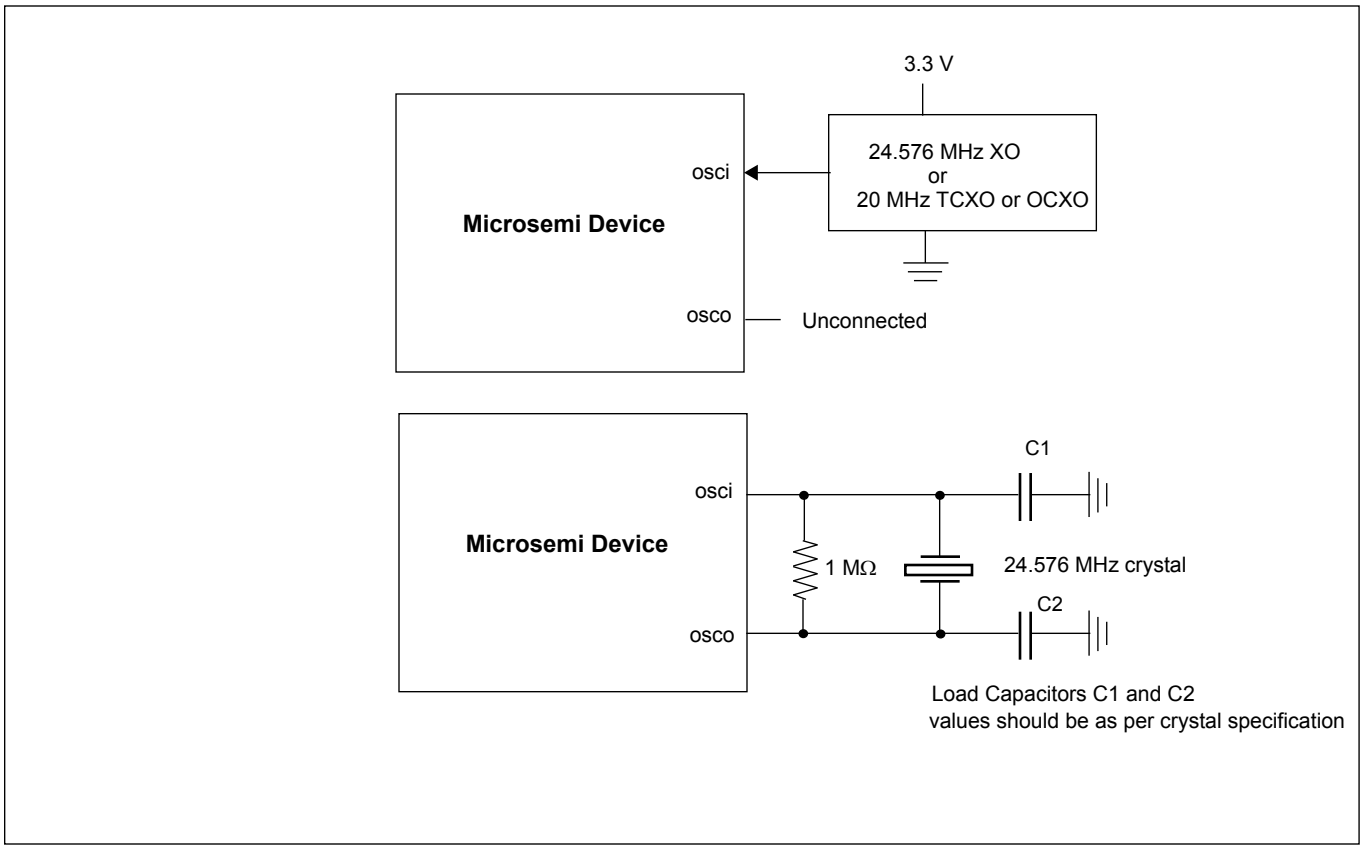


Figure 10 - Clock Oscillator Circuit

The device internal system clocks are generated off the device master clock input (Oscillator or a crystal employing an on-chip buffer/driver). The master clock selection is done at start-up using the available GPIO pins, right after pwr_b get de-asserted. GPIO[0,1] pins need to be held high for 55 ms after the de-assertion of pwr_b, after which time they can be released and used as any other GPIO. Alternatively, these pins can be pulled high with 1KΩ resistors.

GPIO [1:0]	Master Clock Frequency
00	reserved
01	reserved
10	20 MHz
11	24.576 MHz

Table 4 - Master Clock Frequency Selection

4.10 Power Up/Down Sequence

The 3.3 V power rail should be powered before or simultaneously with the 1.8 V power rail to prevent the risk of latch-up (latch-up occur when the 1.8 V supply exceeds the 3.3 V rail by more than 1.8 V).

The power-down sequence is less critical, however it should be performed in the reverse order to reduce transient currents that consume power.

4.11 Power Supply Filtering

Jitter levels on the output clocks may increase if the device is exposed to excessive noise on its power pins. For optimal jitter performance, the device should be isolated from noise on power planes connected to its 3.3 V and 1.8 V supply pins. For recommended common layout practices, refer to Microsemi Application Note ZLAN-230.

4.12 Reset and Configuration Circuit

To ensure proper operation, the device must be reset by holding the pwr_b pin low for at least 2 ms after power-up when 3.3V and 1.8V supplies are stable. Following reset, the device will operate under specified default settings.

The reset pin can be controlled with on-board system reset circuitry or by using a stand-alone power-up reset circuit as shown in Figure 11. This circuit provides approximately 2 ms of reset low time. The pwr_b input has Schmidt trigger properties to prevent level bouncing.

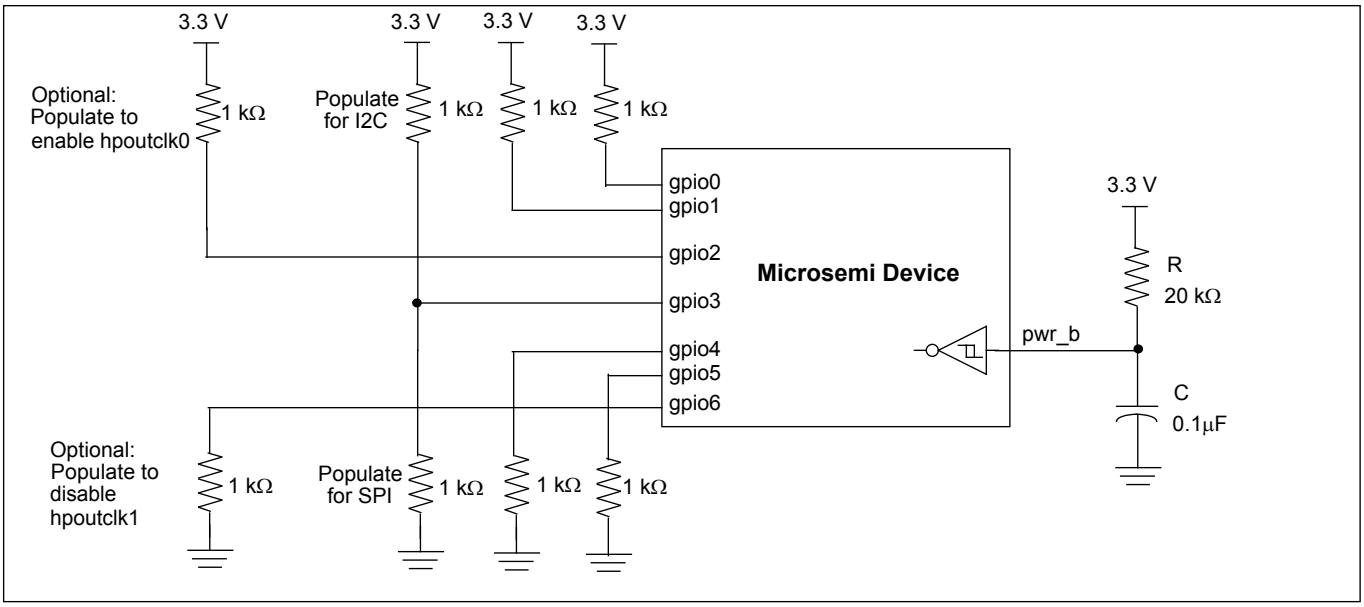


Figure 11 - Typical Power-Up Reset and Configuration Circuit with 24.576 MHz XO

General purpose pins gpio[0,1,3,4,5] are used to configure device on the power up. They have to be pulled up/down with 1 KΩ resistors as shown in Figure 11 or they can be pulsed low/high during the pwr_b low pulse and kept at the same level for at least 55 ms after pwr_b goes high. After 55 ms they can be released and used as general purpose I/O.

By default hpoutclk0 is disabled (gpio2 internal pull-down) and hpoutclk1 is enabled (gpio6 internal pull-up). During the prototype phase, a hardware designer can verify if the device is working properly even before the software driver is implemented just by pulling up gpio2 or gpio6 pin which enables hpoutclk0 output (generates 25 MHz by default) or hpclkout1 output (generates 125 MHz by default) respectively. This feature can also be used for systems where ZL30159 drives a master clock of an ethernet switch with embedded micro processor which needs 25 MHz (and/or 125 MHz) clock on the power up before it can initialize the other components on the board including ZL30159. The hpoutclk1 can be disabled at powerup by pulling down gpio6.

4.13 Ultra Low Jitter Synthesizer Filter Components and Recommended Layout

The APLL for the ultra low jitter synthesizer in the Microsemi device uses external components to help optimize its loop bandwidth. For optimal jitter performance, the following component values are recommended:

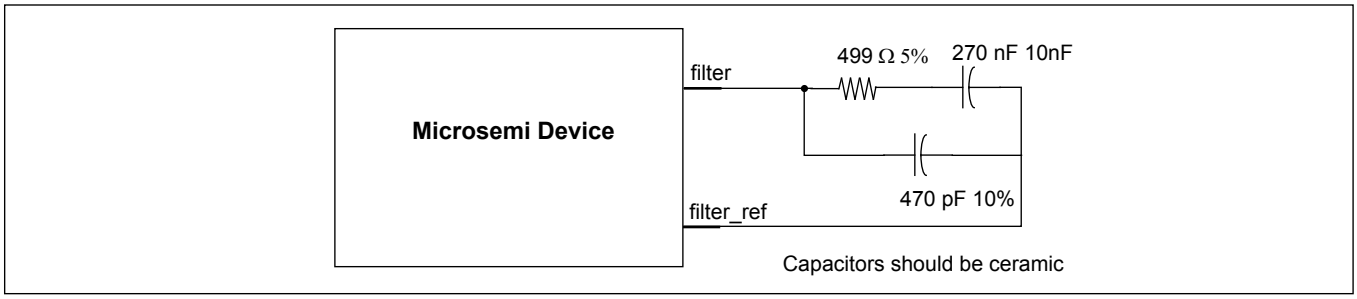


Figure 12 - APLL Filter Component Values

Recommended layout for loop filters is shown in Figure 13:

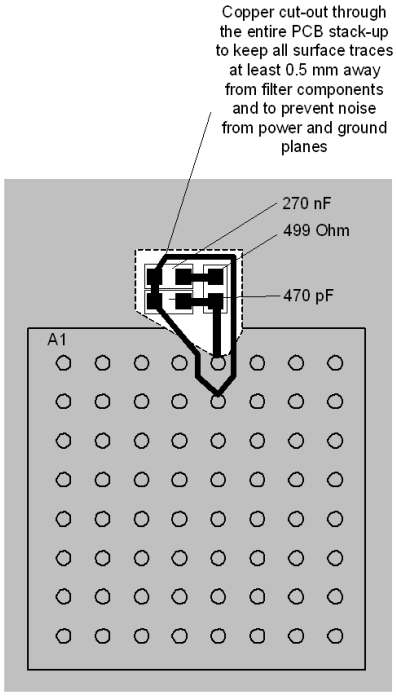


Figure 13 - Recommended Layout for Loop Filters

5.0 Configuration and Control

The ZL30159 configuration is composed of 253 x 8 bits. The configuration registers are assigned their values by any of the following three methods:

1) Default configuration
2) Custom OTP (One Time Programmable) configuration
3) SPI/I2C configuration

The SPI/I2C host interface allows field programmability of the device configuration registers. As an example, user might start the device at nominal SONET rate, then switch to an FEC rate once the link FEC rate is negotiated.

5.1 Custom OTP Configuration

At power-up the device sets its configuration registers to the user defined custom configuration values stored in it's OTP (One Time Programmable). Custom configurations can be generated using Microsemi's Clockcenter GUI software (ZLS30CLKCTR). For custom configured devices contact your local Microsemi Field Applications Engineer or Sales Manager.

5.2 GPIO Configuration and Programmability

The device GPIO is mapped by the SPI/I2C programmability. The following is an example of control and status signals that can be supported:

- DPLL lock indicators
- DPLL holdover indicators
- Reference fail indicators
- Reference control or monitor
- Output clock enable (per output)
- Host Interrupt Output: flags changes of device status prompting the processor to read the enabled interrupt service registers (ISR).
- Output clock stop/start

The following table defines the function of the GPIO pin when configured as a control pin. Configuring the value in bit 7:0 in GPIO configuration registers enables the stated function.

Value	Name	Description
Default		
0x00	default	GPIO pin defined as an input. No function assigned.
Input References		
0x10	Ref external LOS signal	Ref external Loss Of Signal (LOS) - indicator to DPLLs that Ref has failed. Internally in the DPLL this signal is used for reference monitor indicator, or holdover entering and for ISR generation.
DPLL		
0x20	DPLL Time Interval Error (TIE) clear enable	This signal is OR-ed with the 'DPLL TIE clear enable' bit of the 'DPLL control' register. Functionality of this signal is explained in the 'DPLL control' register.

Value	Name	Description
Synthesizer Post Divider		
0x44	Stop output clock from Synthesizer Post Divider A bit1	This signal is OR-ed with the 'Synthesizer Post Divider A stop clock' bit1 in the 'Synthesizer Post Divider stop clock' register. Functionality of this signal is explained in above mentioned register.
0x45	Stop output clock from Synthesizer Post Divider A bit0	Same description as above.
0x46	Stop output clock from Synthesizer Post Divider B bit1	Same description as above.
0x47	Stop output clock from Synthesizer Post Divider B bit0	Same description as above.
High Performance CMOS Outputs		
0x70	Enable HPOUTCLK0	This signal is OR-ed with the 'Enable HPOUTCLK0' bit in the 'High performance CMOS output enable' register. Functionality of this signal is explained in above mentioned register.
0x72	Enable HPOUTCLK1	Same description as Enable HPOUTCLK0

The following table defines the function of the GPIO pin when configured as a status pin. Configuring the value in bit 7:0 in GPIO configuration registers enables the stated function.

Value	Name	Description
Interrupt		
0x80	Interrupt output signal	This bit will be high if the interrupt has been asserted.
Input References		
0x88	Ref - Signal not present in last second	This bit will be high if Ref signal was not toggling in the last second.
0x89	Ref Single Cycle Measurement (SCM) failure	This bit will be set if Ref SCM indicator is active (see 'Ref SCM and CFM limits' register for SCM limits).
0x8A	Ref Coarse Frequency Measurement (CFM) failure	This bit will be set if Ref CFM indicator is active (see 'Ref SCM and CFM limits' register for CFM limits).
0x8B	Ref Guard Soak Timer (GST) indicator	Ref Guard Soak Timer (GST) indicator
0x8C	Ref failure indicator	This bit will be set if either Ref external LOS signal is high, or Ref SCM, CFM or GST indicator is high, and appropriate mask bit in the 'Ref failure mask' register is set to 1 (not masked).
DPLL Filters		
0xA8	DPLL Normal mode indicator	This bit will be set when the DPLL is in normal locking mode (not holdover, not freerun)
0xA9	DPLL holdover mode indicator	This bit will be set when the DPLL is in holdover mode
0xAD	DPLL out of pull-in/hold-in range indication	This bit will be set when DPLL frequency is beyond pull-in/hold-in range limit, specified in the 'DPLL control' register
0xAF	DPLL Lock Indication 0	This bit will be set when DPLL phase error is less then 36us during 10s period.

Value	Name	Description
0xB0	DPLL Lock Indication 1	This bit will be set when DPLL phase error is less then 1us during 1s period.
0xB1	DPLL Lock Indication 2	This bit will be set when DPLL phase error is less then 10us during 1s period.
0xB2	DPLL Lock Indication 3	This bit will be set when DPLL phase error is less then 10us during 10s period.

5.3 Configuration Registers

This section refers to configuration registers that are set by the user to define device operation.

5.3.1 Input Reference Configuration and Programmability

The following is the set of parameters that are configurable:

- Input reference frequency as multiple of 1 kHz, and M/N ratio of the 1 kHz multiple or 1 Hz
- Input reference type: single ended or differential
- Holdover mode based on input reference single cycle monitor or coarse frequency monitor or guard soak timer

5.3.2 DPLL Configuration and Programmability

The following is the set of parameters that are configurable:

- DPLL input reference
- DPLL loop bandwidth

5.3.3 Synthesis Macro Configuration and Programmability

The following is the set of parameters that are configurable:

- Synthesis Macro locked to DPLL freerun or disabled
- Synthesis Macro mode M/N ratio or 1 kHz multiple
- Synthesis Macro high speed output clock, defined as a 1 kHz multiple and 1 kHz multiple with M/N ratio

5.3.4 Output Dividers and Skew Management Configuration and Programmability

The following is the set of parameters that are configurable:

- Post divider enable/disable
- Divider ratio
- Output delay value

5.3.5 Output Drivers configuration and Programmability

The following is the set of parameters that are configurable:

- Output driver Enable/Disable

5.4 State Control

The device has two main control modes of operation: un-managed mode and managed mode.

In un-managed mode of operation, the DPLL state (normal, freerun and holdover) is automatically set by the device internal state machine. It is based on availability of a valid reference.

In managed mode of operation, the DPLL state (normal, freerun and holdover) is manually set by the user.

The device allows for smooth transition from in and out of the two modes of operation. Hence if the DPLL was in managed mode and locked to the input reference and it was switched to un-managed mode of operation, then the state machine continues managing the device starting from being locked to the input reference and it will not force the device into holdover mode unless a change in conditions required such transition.

To facilitate monitoring and managing the device during managed mode of operation, and to facilitate monitoring the device during the un-managed mode, some control and status bits can be muxed into the GPIO pins. The following is a list for such control and monitor bits:

- DPLL state (2 control bits), Normal, holdover and freerun

- Reference monitoring (3 status bits)
- DPLL holdover indication (1 status bit)
- DPLL lock indication (1 status bit)

5.4.1 Un-managed Mode

In this mode, transitioning from one mode to the other is controlled by the device internal state machine.

The on-chip state machine monitors the device status bits, and based on the status information the state machine makes a decision to force holdover.

In the un-managed mode of operation, the device internal state machine manages the device operating states. The switch to holdover is based on the internal clock monitoring.

In un-managed mode of operation, the state machine only reacts to failure indicators and goes into auto-holdover under one of the following conditions if they are not masked with their corresponding mask bits:

- LOS detected a failure and HOMask<0> is at logic “1”
- SCM detected a failure and HOMask<1> is at logic “1”
- CFM detected a failure and HOMask<2> is at logic “1”
- The Guard Soak Time is triggered and HOMask<3> is at logic “1”
- PFM detected a failure and PFM_HOMask is set at logic "1"

The default conditions is HOMask<3:0> is “0111”.

The default conditions for HOMask<3:0> (Register at address 0x34) is “0111” and for PFM_HOMask (register at address 0xF4) is "1".

In un-managed mode of operation, the state machine automatically recovers from auto-holdover when the conditions to enter auto-holdover are not present.

5.4.2 Managed Mode

The managed mode combines the functionality of the Holdover, Freerun and Normal states with automatic Holdover. In this mode, transitioning from one state to the other is controlled by an external controller.

The external controller monitors the device status bits. Based on the status information, the external controller makes a decision to force holdover. If the external controller sets the device to lock to a failed reference, the device stays in auto-holdover and only locks to that reference if it becomes valid.

The state machine only reacts to failure indicators and goes into auto-holdover under one of the following conditions if they are not masked with their corresponding mask bits:

- LOS detected a failure and HOMask<0> is at logic “1”
- SCM detected a failure and HOMask<1> is at logic “1”
- CFM detected a failure and HOMask<2> is at logic “1”
- The Guard Soak Time is triggered and HOMask<3> is at logic “1”
- PFM detected a failure and PFM_HOMask is set at logic "1"

The default conditions HOMask<3:0> (Register at address 0x34) is “0111” and for PFM_HOMask (register at address 0xF4) is "1".

The state machine automatically recovers from auto-holdover when the conditions to enter auto-holdover are not present.

Time critical state transitions for entry into auto-holdover and exit from auto-holdover are managed by the internal state machine.

6.0 Host Interface

A host processor controls and receives status from the Microsemi device using either a SPI or an I^2C interface. The type of interface is selected using the startup state of the GPIO pins.

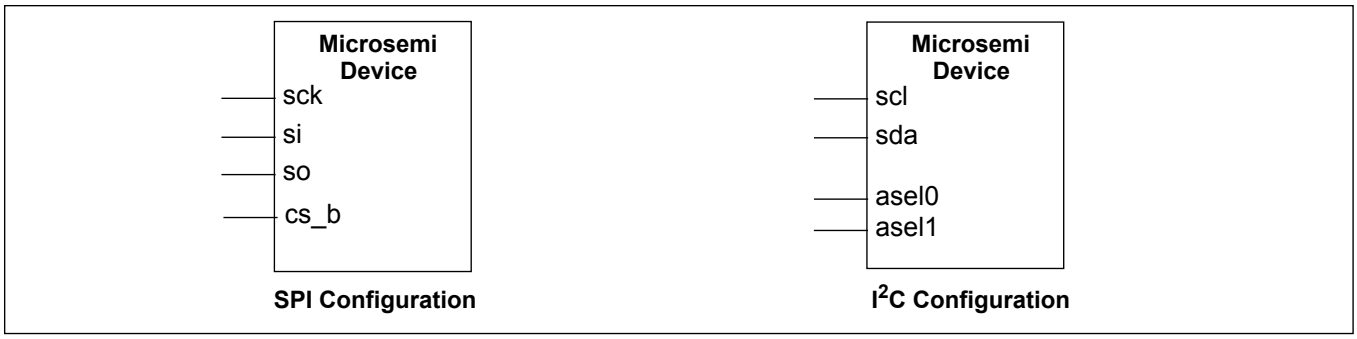


Figure 14 - Serial Interface Configuration

The selection between I2C and SPI interfaces is performed at start-up using GPIO[3] pin, right after pwr_b gets de-asserted. The GPIO pin need to be held at their appropriate value for 55 ms after the de-assertion of pwr_b, after which time they can be released and used as any other GPIO.

Both interfaces use seven bit address field and the device has eight bit address space. Hence, memory is divided in two pages. Page 0 with addresses 0x00 to 0x7E and Page 1 with addresses 0x80 to 0xFF. Writing 0x01 to Page Register at address 0x7F, toggles SPI/I2C accesses between Page 0 and Page 1.

GPIO[3]	Serial Interface
0	SPI
1	I2C

Table 5 - Serial Interface Selection

6.1 Serial Peripheral Interface

The serial peripheral interface (SPI) allows read/write access to the registers that are used to configure, read status, and allow manual control of the device.

This interface supports two modes of access: Most Significant Bit (MSB) first transmission or Least Significant Bit (LSB) first transmission. The mode is automatically selected based on the state of **sck**_scl pin when the **cs_b**_asel0 pin is active. If the **sck**_scl pin is low during **cs_b**_asel0 activation, then MSB first timing is selected. If the **sck**_scl pin is high during **cs_b**_asel0 activation, then LSB first timing is assumed.

The SPI port expects 7-bit addressing and 8-bit data transmission, and is reset when the chip select pin **cs_b**_asel0 is high. During SPI access, the **cs_b**_asel0 pin must be held low until the operation is complete. The first bit transmitted during the address phase of a transfer indicates whether a read (1) or a write (0) is being performed. Burst read/write mode is also supported by leaving the chip select signal **cs_b**_asel0 is low after a read or a write. The address will be automatically incremented after each data byte is read or written.

The serial peripheral interface supports half-duplex processor mode which means that during a write cycle to the device, output data from the **so**_asel1 pin must be ignored. Similarly, the input data on the **si**_sda pin is ignored by the device during a read cycle.

Functional waveforms for the LSB and MSB first mode, and burst mode are shown in Figure 15, Figure 16 and Figure 17. Timing characteristics are shown in Table 7, Figure 27, and Figure 28.

6.1.1 Least Significant Bit (LSB) First Transmission Mode

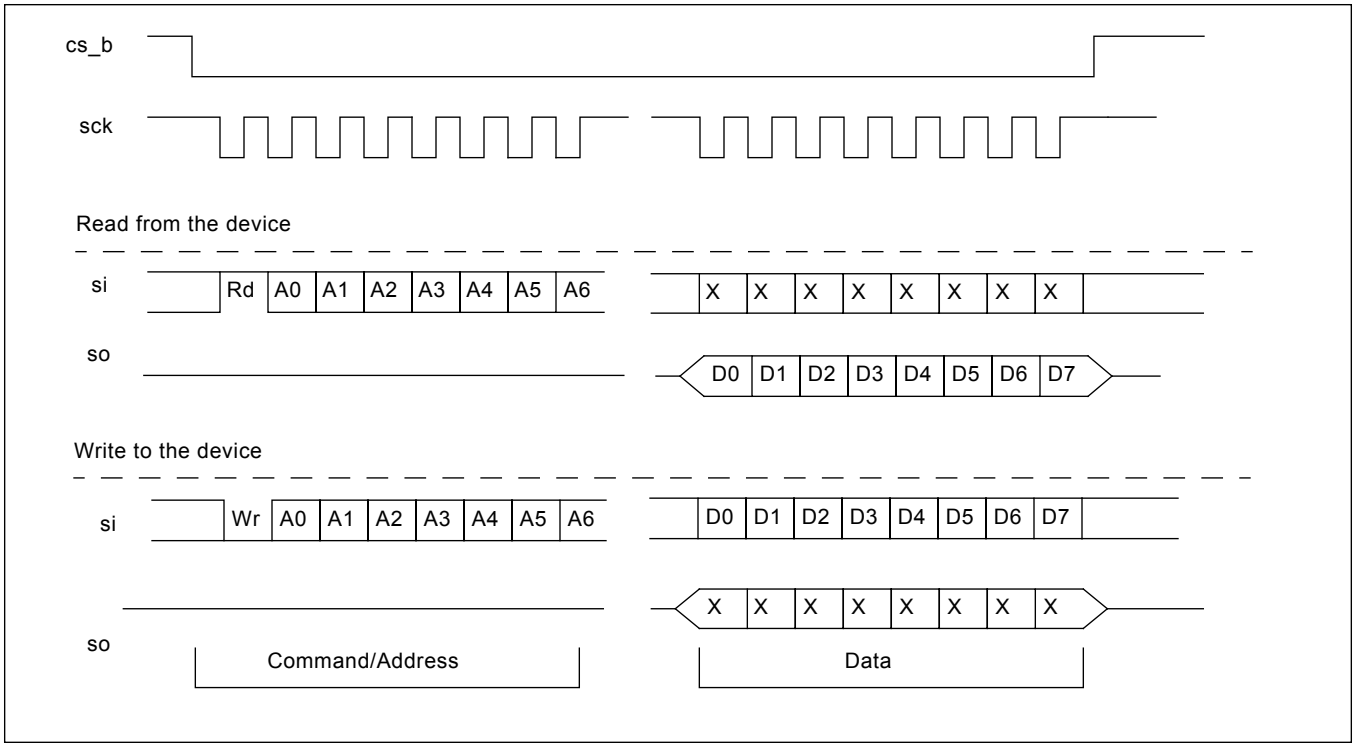


Figure 15 - Serial Peripheral Interface Functional Waveforms - LSB First Mode

6.1.2 Most Significant Bit (MSB) First Transmission Mode

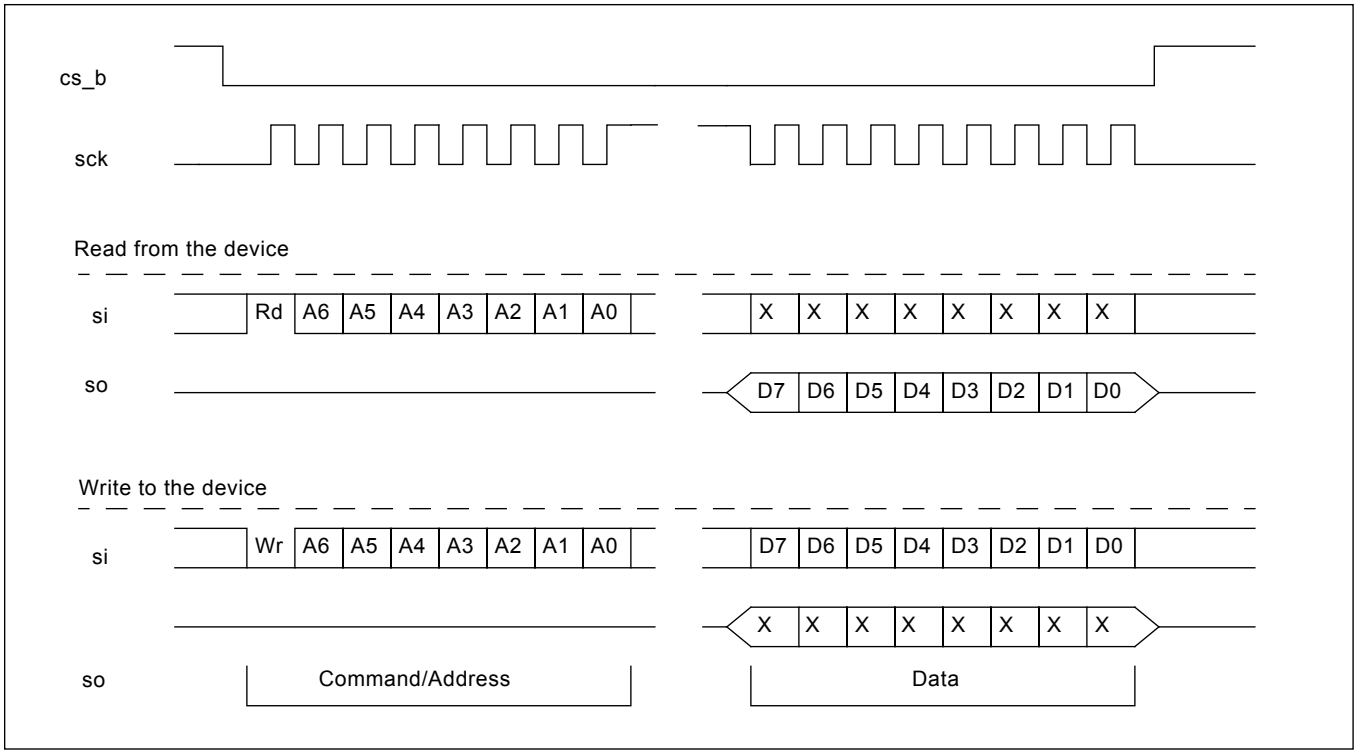


Figure 16 - Serial Peripheral Interface Functional Waveforms - MSB First Mode

6.1.3 SPI Burst Mode Operation

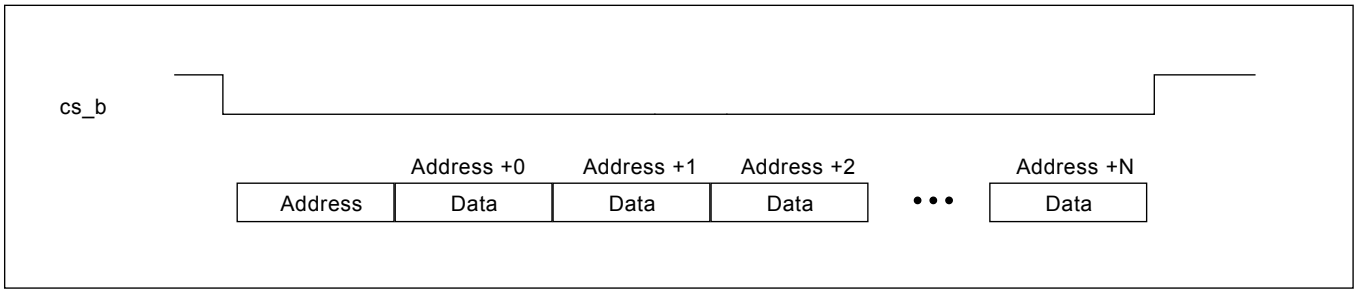


Figure 17 - Example of a Burst Mode Operation

6.1.4 I²C Interface

The I²C controller supports version 2.1 (January 2000) of the Philips I²C bus specification. The port operates in slave mode with 7-bit addressing, and can operate in Standard (100 kbits/s) and Fast (400 kbits/s) mode. Burst mode is supported in both standard and fast modes.

Data is transferred MSB first and occurs in 1 byte blocks. As shown in Figure 18, a **write** command consists of a 7-bit device (slave) address, a 7-bit register address (0x00 - 0x7F), and 8-bits of data.

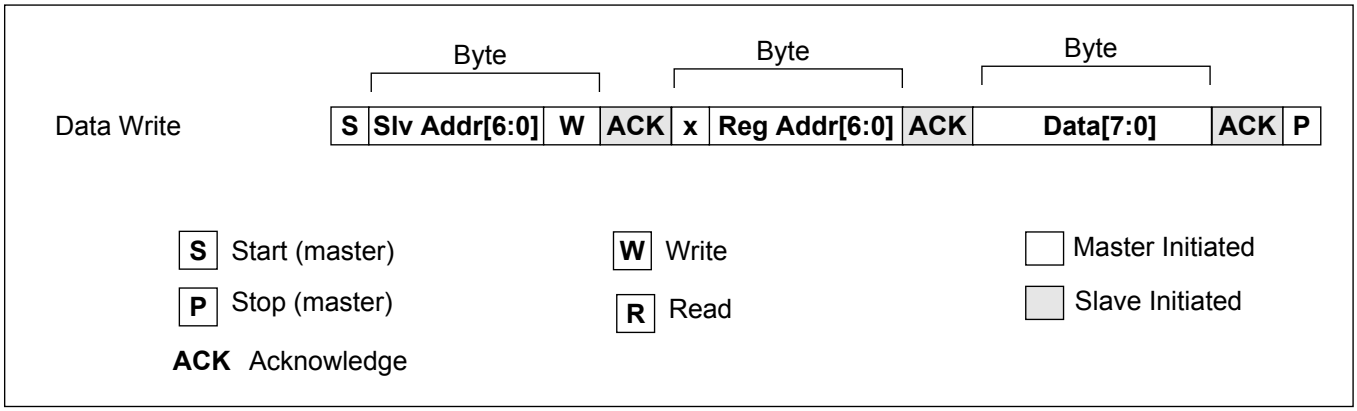


Figure 18 - I²C Data Write Protocol

A **read** is performed in two stages. A data write is used to set the register address, then a data read is performed to retrieve the data from the set address. This is shown in Figure 19.

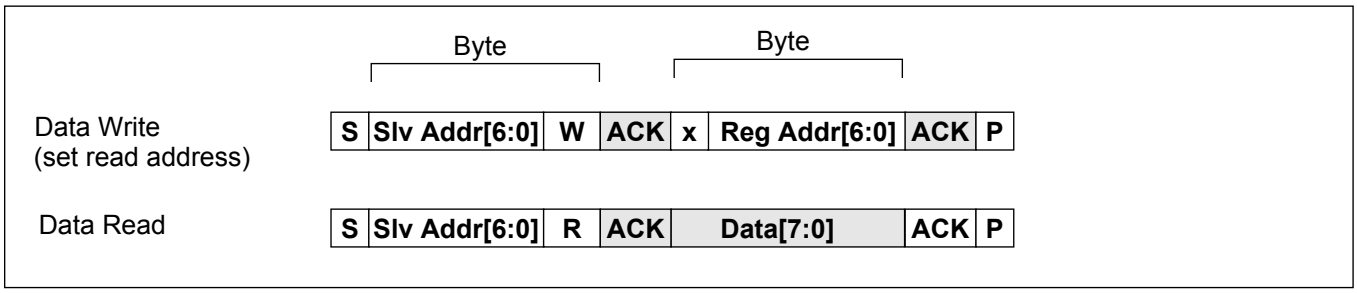


Figure 19 - I²C Data Read Protocol

The **7-bit device (slave) address** contains a 5-bit fixed address plus variable bits which are set with the **asel0,** and **asel1** pins. This allows multiple ZL30159s to share the same I^{2}C bus. The address configuration is shown in Figure 20.

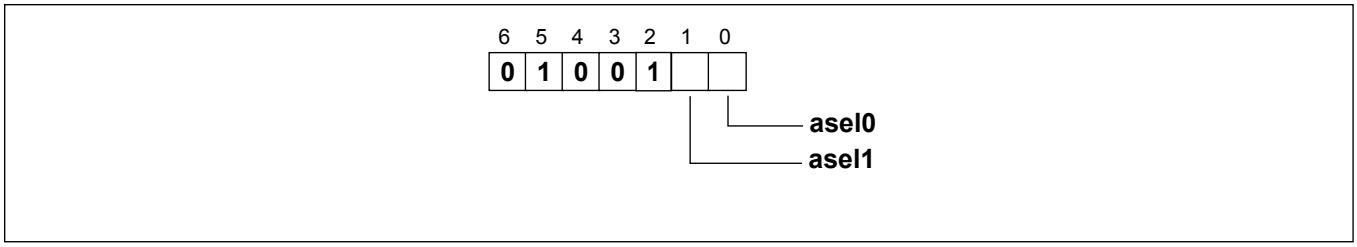


Figure 20 - I^{2}C 7-bit Slave Address

The device also supports burst mode which allows multiple data write or read operations with a single specified address. This is shown in Figure 21 (write) and Figure 22 (read). The first data byte is written/read from the specified address, and subsequent data bytes are written/read using an automatically increment address. The maximum auto increment address of a burst operation is 0x7F. Any operations beyond this limit will be ignored. In other words, the auto increment address does not wrap around to 0x00 after reaching 0x7F.

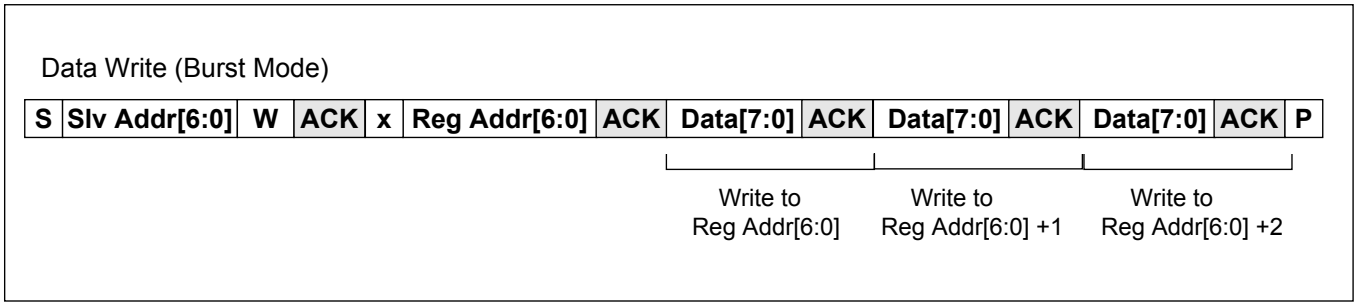


Figure 21 - I^{2}C Data Write Burst Mode

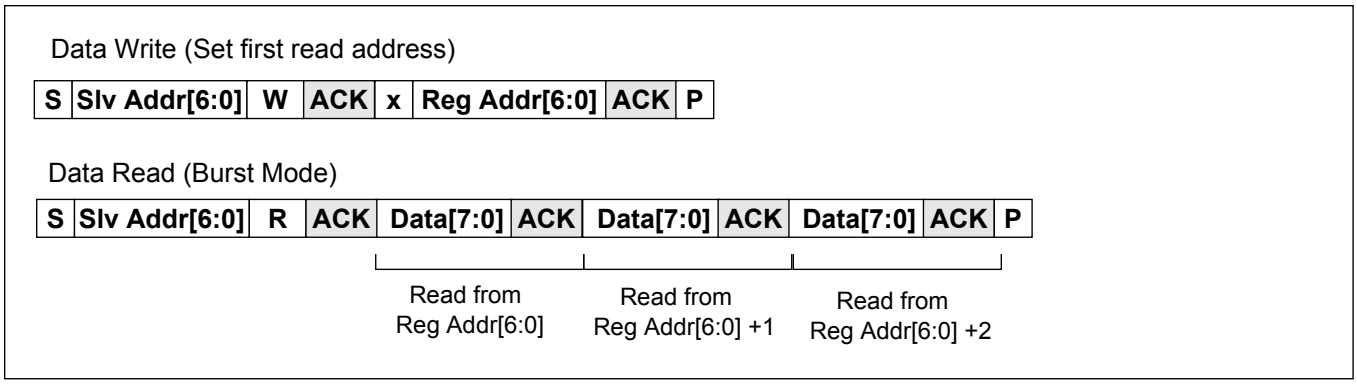


Figure 22 - I^{2}C Data Read Burst Mode

7.0 Register Map

The device is mainly controlled by accessing software registers through the serial interface (SPI or I^2C). The device can be configured to operate in a highly automated manner which minimizes its interaction with the system's processor, or it can operate in a manual mode where the system processor controls most of the operation of the device.

The simplest way to generate appropriate configuration for the device is to use the evaluation board GUI which can operate standalone (without the board). With GUI user can quickly set all required parameters and save the configuration to a text file.

Multi-byte Register Values

The device register map is based on 8-bit register access, so register values that require more than 8 bits must be spread out over multiple registers and accessed in 8-bit segments. When accessing multi-byte register values, it is important that the registers are accessed in the proper order—they must follow big endian addressing scheme. The 8-bit register containing the most significant byte (MSB) must be accessed first, and the register containing the least significant byte (LSB) must be accessed last. An example of a multi-byte register is shown in Figure 23. When writing a multi-byte value, the value is latched when the LSB is written.

Example:
The programmable input reference M and N 16 bit values defining the M/N ratio is programmed using a 32-bit value which is spread over four 8-bit registers. The MSB is contained in address 0x14 and the LSB in 0x17. When reading or writing this multi-byte value, the MSB must be accessed first, followed by the middle bytes, and the LSB last.

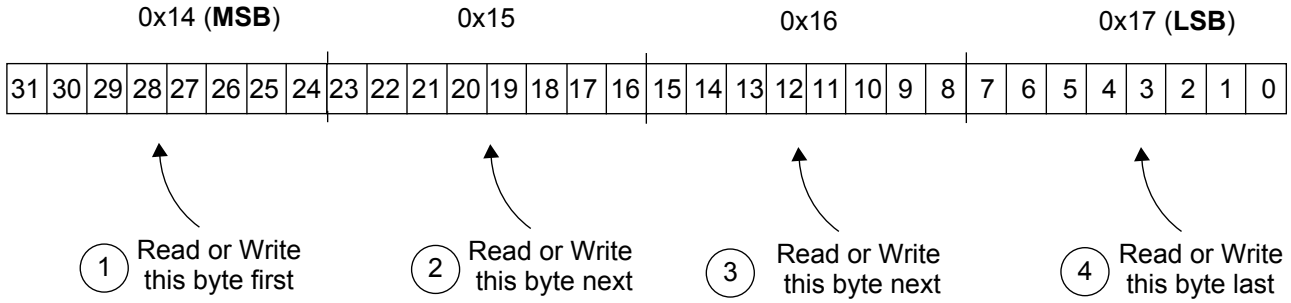


Figure 23 - Accessing Multi-byte Register Values

To assist in device setup, a configuration GUI is provided. The configuration GUI can directly configure the device evaluation board, but it also functions as a tool to provide details on how to configure different device registers.

Writing to registers

Writes to registers should follow following procedure:

-write 0x01 to Sticky R Lock Register at address 0x0D

- write to one or multiple register(s)

-write 0x00 to Sticky R Lock Register at address 0x0D

Time between two write accesses to the same register

User should wait at least 5 ms between two write accesses to the same register. This applies to all registers except Sticky R Lock Register at address 0x0D and page register at address 0x7F which can be accessed immediately.

Reading from Sticky Read (StickyR) Registers

Access to some status registers is defined as Sticky Read (StickyR). Procedure for accessing these registers is:

-clear status register(s) by writing 0x00 to it (please follow Writing to registers procedure shown above)

-wait for 5 ms

-read the status register(s)

The following table provides a summary of the registers available for status updates and configuration of the device.Devices with a custom OTP configuration will power-up with the custom configuration values instead of the default values.

Reg_Addr (Hex)	Register Name	Default Value (Hex)	Description	Type
Miscellaneous Registers				
0x00	id_reg	0x09	Chip ID and version identification. User should not write to this register. If this register is written to, the default value will be temporarily overwritten until the next reset. The temporary change of the default value will not affect the performance of the device.	R/W
Interrupts and Reference Monitor				
0x02	ref_fail_isr_status	0x00	Reference failure status register	StickyR
0x03	dpll_isr_status	0x00	DPLL status register	StickyR
0x04	ref_fail_isr_mask	0x00	Reference failure interrupt service register mask	R/W
0x05	dpll_isr_mask	0x00	DPLL interrupt service register mask	R/W
0x07	ref_mon_fail	0x00	Ref failure indications	StickyR
0x09	ref_mon_fail_mask	0x66	Control register to mask failure indicator for Ref	R/W
0x0A	ref_config	0x00	Configures input reference to be differential or single-ended	R/W
0x0B	gst_disqualif_time	0xAA	Control register for the guard soak timer disqualification time for the reference	R/W
0x0C	gst_qualif_time	0x55	Control register for the guard soak timer qualification time for the reference	R/W

Table 6 - Register Map

Reg_Addr (Hex)	Register Name	Default Value (Hex)	Description	Type
0x0D	sticky_r_lock	0x00	Used to lock StickyR Status Registers from being updated by internal device logic	R/W
Input Frequency Configuration				
0x10:0x11	ref_base_freq	0x61A8	Ref base frequency in Hz (16 bits, unsigned integer)	R/W
0x12: 0x13	ref_freq_multiple	0x03E8	Ref frequency as a multiple of the base frequency (16 bits, unsigned integer)	R/W
0x14:0x17	ref_ratio_M_N	0x00010001	Ref Mr and Nr values, used for multiplication ratio Mr/Nr (2 x 16 bits unsigned integers)	R/W
DPLL Configuration, State Machine Control and Monitor				
0x30	dpll_ctrl	0x0C	DPLL control register	R/W
0x33	dpll_mode_refsel	0x03	DPLL reference selection control or reference selection status	R/W
0x34	dpll_ref_fail_mask	0x87	Control register to mask each failure indicator (SCM, CFM and GST) used for automatic holdover	R/W
0x44	dpll_hold_lock_fail	0x00	DPLL lock and holdover status	StickyR
Input Reference Monitoring Registers				
0x47	phase_mem_limit_ref	0x0A	Reference phase memory limit	R/W
0x4B	scm_cfm_limit_ref	0x55	Reference single cycle monitor (SCM) and coarse frequency monitor (CFM) limits	R/W
0x4F	dpll_config	0x31	Enables DPLL	R/W
Output Synthesizer Configuration Registers				
0x50:0x51	synth_base_freq	0x61A8	Synthesizer base frequency	R/W
0x52:0x53	synth_freq_multiple	0x0EA6	Synthesizer base frequency multiplication number	R/W
0x54:0x57	synth_ratio_M_N	0x00010001	Specifies numerator Ms and denominator Ns for synthesizer multiplication ratio Ms/Ns	R/W
0x71	output_synthesizer_en	0x01	Output synthesizer enable	R/W
0x72	dpll_lock_selection	0xAA	DPLL lock selection	R/W

Table 6 - Register Map (continued)

Reg_Addr (Hex)	Register Name	Default Value (Hex)	Description	Type
0x73:0x76	central_freq_offset	0x046AAAAB	Central frequency offset to compensate for oscillator inaccuracy	R/W
0x77	synth_filter_sel	0x00	Synthesizer selection between internal and external filter	R/W
0x78	synth_fine_phase_shift	0x00	Synthesizer fine phase shift	R/W
0x7F	page_register	0x00	Selects between pages 0 and 1	R/W
0x86:0x88	synth_post_div_A	0x00003C	Synthesizer post divider A	R/W
0x89:0x8B	synth_post_div_B	0x00000C	Synthesizer post divider B	R/W
Output Reference Selection and Output Driver Control				
0xB1	hp_cmos_en	0x00	Enables High Performance CMOS outputs hpoutclk[1:0]	R/W
0xB8	synth_stop_clk	0x00	Stops output clocks at either high or low logical level for post dividers A and/or B	R/W
0xB9	sync_fail_flag_status	0x00	Indicates Synthesizers loss of lock	StickyR
0xBA	clear_sync_fail_flag	0x00	Clears Synthesizers fail flag in register 0xB9	R/W
0xBF:0xC0	phase_shift_s_postdiv_A	0x0000	hpoutclk0 output coarse phase shift in granularity of 45 degrees and one high frequency synthesizer clock period.	R/W
0xC1:0xC2	phase_shift_s_postdiv_B	0x0000	hpoutclk1 output coarse phase shift in granularity of 45 degrees and one high frequency synthesizer clock period.	R/W
0xC3	xo_or_crystal_sel	0x00	Disables OSCo driver.	R/W
0xC6	chip_revision	0x03	Chip revision number	R/W
0xE0	gpio_function_pin0	0x00	GPIO0 control or status select	R/W
0xE1	gpio_function_pin1	0x00	GPIO1 control or status select	R/W
0xE2	gpio_function_pin2	0x70	GPIO2 control or status select	R/W
0xE3	gpio_function_pin3	0x00	GPIO3control or status select	R/W
0xE4	gpio_function_pin4	0x00	GPIO4 control or status select	R/W
0xE5	gpio_function_pin5	0x00	GPIO5 control or status select	R/W
0xE6	gpio_function_pin6	0x72	GPIO6 control or status select	R/W

Table 6 - Register Map (continued)

Reg_Addr (Hex)	Register Name	Default Value (Hex)	Description	Type
0xEC	dpll_ctrl2	0x00	DPLL Control Register 2	R/W
0xED	dpll_holdpull	0x07	Pull-in/hold-in range setting	R/W
0xF4	pfm_mask_ho	0xF0	Control register to mask PFM failure indicator used for automatic holdover.	R/W
0xF5	pfm_mask_ref_fail	0x00	Control register to mask PFM failure indication for the input reference.	R/W
0xF7	pfm_range_ref	0x33	Precise Frequency Monitoring for the input reference	R/W

Table 6 - Register Map (continued)

8.0 Detailed Register Map

Register_Address: **0x00** Register Name: **id_reg** Default Value: **0x09** Type: R/W		
Bit Field	**Function Name**	**Description**
4:0	chip_id	Chip Identification = 0b01001
6:5	chip_revision	Chip revision number 0b11: RevE 0b00: Chip revision specified in register 0xC6
7	ready_indication	After reset this bit will be undefined for up to 45 ms. After 45 ms this bit will go low indicating that the device is finalizing self-initialization. Finally, this bit will go high indicating that the device is ready to be programmed by the user. It can take up to 55 ms for this bit to go high after the reset.

Register_Address: **0x02** Register Name: **ref_fail_isr_status** Default Value: **0x00** Type: StickyR		
Bit Field	**Function Name**	**Description**
0	ref_fail	This bit is set to 1 when ref has a failure. The device will set this bit to high when ref_fail_mask bit of the ref_fail_isr_mask register at address 0x04 is high and conditions for ref failure are satisfied. When this bit is set to high, it also sets IRQ line to high.
7:1	reserved	Leave as default

Register_Address: **0x03** Register Name: **dpll_isr_status** Default Value: **0x00** Type: StickyR		
Bit Field	**Function Name**	**Description**
0	dpll_holdover	The device will set this bit to high when dpll_holdover_mask bit of the dpll_interrupt_mask register at address 0x05 is high and DPLL went into holdover mode. When this bit is set to high, it also sets IRQ line to high.
1	dpll_loss_of_lock	The device will set this bit to high when 'dpll_loss_of_lock_mask bit of the dpll_interrupt_mask register at address 0x05 is high and DPLL has lost lock. When this bit is set to high, it also sets IRQ line to high.
7:2	reserved	Leave as default

Register_Address: **0x04** Register Name: **ref_fail_isr_mask** Default Value: **0x00** Type: R/W		
Bit Field	**Function Name**	**Description**
0	ref_fail_isr_mask	Reference failure interrupt generation mask. When set to zero disables interrupt generation and appearance in the Reference Status ISR register.
7:1	reserved	Leave as default

Register_Address: **0x05** Register Name: **dpll_isr_mask** Default Value: **0x00** Type: R/W		
Bit Field	**Function Name**	**Description**
0	dpll_holdover_mask	DPLL holdover indication mask. When set to zero disables interrupt generation and appearance in the DPLL Status ISR register.

Register_Address: **0x05** Register Name: **dpll_isr_mask** Default Value: **0x00** Type: R/W		
Bit Field	**Function Name**	**Description**
1	dpll_loss_of_lock_mask	DPLL loss of lock indication mask. When set to zero disables interrupt generation and appearance in the DPLL Status ISR register.
7:2	reserved	Leave as default.

Register_Address: **0x07** Register Name: **ref_mon_fail** Default Value: **0x00** Type: SticlyR		
Bit Field	**Function Name**	**Description**
0	ref_fail_los	Reference Loss Of Signal (LOS) indicator. The device will set this bit to high when external Ref 0 LOS signal (typically from PHY device), applied to selected GPIO, goes high. The Ref LOS signal indicator can be associated with any of available GPIOs pins through the 'GPIO function' registers. **Note:** this bit is not maskable.
1	ref_fail_scm	Reference Single Cycle Monitor (SCM) indicator. This bit is set high whenever Single Cycle Failure on Reference occurs. **Note:** this bit is not maskable.
2	ref_fail_cfm	Reference coarse frequency monitoring (CFM) indicator. This bit is set high whenever coarse frequency monitoring failure on Reference occurs. **Note:** this bit is not maskable.
3	ref_fail_gst	Guard Soak Timer (GST) failure indicator on Reference. This bit is set high whenever Reference guard soak timer expires. **Note:** this bit is not maskable.
7:4	reserved	Leave as default

Register_Address: **0x09** Register Name: **ref_mon_fail_mask** Default Value: **0x66** Type: R/W		
Bit Field	**Function Name**	**Description**
3:0	ref_fail_mask	Masks failure indicators (LOS,SCM, CFM, and GST) for input reference. bit 0: LOS (Loss of Clock) bit 1: SCM (Single Cycle Monitor) bit 2: CFM (Coarse Frequency Monitor) bit 3: GST (Guard Soak Timer) 0: failure bit is masked (disabled) 1: failure bit is un-masked (enabled) Note: When set low these bits will mask corresponding Reference failure indicators in Reference Failure Interrupt Status Register at address 0x02. They will not affect bits in Reference Monitoring Failure Mask Register at address 0x07 because bits in Reference Monitoring Failure Mask Register are not maskable.
7:4	reserved	Leave as default

Register_Address: **0x0A** Register Name: **ref_config** Default Value: **0x00** Type: R/W		
Bit Field	**Function Name**	**Description**
0	ref_pre-divider_enable	When set high, the Reference input clock will be divided by 2 prior to being fed to DPLL. All registers, which depend on the frequency of the input reference will have to be programmed with half of the reference frequency. When set low, the Reference is fed directly to DPLL.
3:1	reserved	Leave as default
4	ref_diff_input_enable	When set high, the device expects differential clock at Ref input pins (Ref_p and Ref_n). When set low, the device expects single-ended clock at Ref_p input pin, and Ref_n input should be connected to ground.
7:5	reserved	Leave as default

Register_Address: **0x0B** Register Name: **gst_disqualif_time** Default Value: **0xAA** Type: R/W		
Bit Field	**Function Name**	**Description**
1:0	ref_gst_disqualif_timer	Selects time to disqualify input reference after detection of either the Ref CFM or Ref SCM indicators. 00: minimum delay 01: 10 ms 10: 50 ms (default) 11: 2.5 s
7:2	reserved	Leave as default

Register_Address: **0x0C** Register Name: **gst_qualif_time** Default Value: **0x55** Type: R/W		
Bit Field	**Function Name**	**Description**
1:0	ref_gst_qualif_timer	Selects time to qualify input reference after deassertion of both the Ref CFM and Ref SCM indicators. 00: 2 x selected Ref GST disqualify time 01: 4 x selected Ref GST disqualify time (default) 10: 6 x selected Ref GST disqualify time 11: 8 x selected Ref GST disqualify time
7:2	reserved	Leave as default

Register_Address: **0x0D** Register Name: **sticky_r_lock** Default Value: **0x00** Type: R/W		
Bit Field	**Function Name**	**Description**
7:0	sticky_r_lock	This register is used when accessing StickyR status registers. Writing 0x01 to this register locks the status register from being updated by internal logic. Writing 0x00 to this register enables internal updates of StickyR status registers Please refer to **Reading from Sticky Read (StickyR) registers and Writing to registers** procedure at the beginning of 7.0, “Register Map“ section.

Register_Address: **0x10:0x11** Register Name: **ref_base_freq** Default Value: **0x61A8** Type: R/W		
Bit Field	**Function Name**	**Description**
15:0	ref_base_freq	Unsigned binary value of these bits represents Ref base frequency Br in Hz. Values for Br that can be programmed: 0x03E8 for 1 kHz, 0x07D0 for 2 kHz, 0x1388 for 5 kHz, 0x186A for 6.25 kHz, 0x1F40 for 8 kHz, 0x2710 for 10 kHz, 0x30D4 for 12.5 kHz, 0x61A8 for 25 kHz, 0x9C40 for 40 kHz. **Note 1:** Other Br rates can be supported, please contact Microsemi application support team if another specific Br rate is required **Note 2:** in order to write 16 bit value to this register (and any other register that is bigger than 8 bits), the most significant byte has to be written to the lower address and least significant byte has to be written to the higher address. Hence, memory mapping follows big endian.

Register_Address: **0x12:0x13**
Register Name: **ref_freq_multiple**
Default Value: **0x03E8**
Type: R/W

Bit Field	Function Name	Description
15:0	ref_freq_multiple	Unsigned binary value of these bits represents Ref base frequency multiplication factor Kr. For regular (non-FEC) reference frequencies, the 'Base frequency' number Br multiplied by the 'Base frequency multiple' number Kr has to equal the reference frequency in Hz. Examples of some references frequencies and appropriate values that can be programmed for Br and Kr to match that reference frequency: Reference frequency / Base frequency Br / Base frequency multiple Kr 2.048 MHz / 8 kHz (0x1F40) / 256 (0x0100) 1.544 MHz / 8 kHz (0x1F40) / 193 (0x00C1) 19.44 MHz / 40 kHz (0x9C40) / 486 (0x01E6) 177.5.MHz / 25 kHz (0x61A8) / 7100 (0x1BBC) 125 MHz / 40 kHz (0x9C40) / 18752 (0x4940) 156.25.MHz / 25 kHz (0x61A8) / 6250 (0x186A) 155.52 MHz / 40 kHz (0x9C40) / 3888 (0x0F30) 8 kHz / 1 kHz (0x03E8) / 8 (0x0008)

Register_Address: **0x14:0x17**
Register Name: **ref_ratio_M_N**
Default Value: **0x00010001**
Type: R/W

Bit Field	Function Name	Description
15:0	ref_FEC_denom_Nr	Unsigned binary value of Mr bits, in combination with unsigned binary value of Nr bits represents Ref FEC multiplication ratio. For FEC reference frequencies, the 'Base frequency' number Br multiplied by the 'Base frequency multiple' number Kr, multiplied by Mr and divided by Nr has to equal the reference frequency in Hz; Ref_freq [Hz] = Br x Kr x Mr / Nr For regular (non-FEC) reference frequencies, Mr and Nr should be programmed to 0x0001 (default values) Examples of some FEC references frequencies and appropriate values that can be programmed for the Br, Kr, Mr and Nr register to match that FEC reference frequency: **a) OC-192 mode, standard EFEC for long reach:** Reference frequency: 155.52 MHz x 255 / 237 Base frequency Br: 40 kHz (0x9C40) Base frequency multiple Kr : 3888 (0x0F30) FEC ratio Numerator Mr: 255 (0x00FF) FEC ratio denominator Nr: 237 (0x00ED) **b) Long reach 10GE mode, double rate conversion:** Reference frequency: 156.25 MHz x 66/64 x 255/238 Base frequency Br: 25 kHz (0x61A8) Base frequency multiple Kr : 6250 (0x186A) FEC ratio Numerator Mr: 66x255 (0x41BE) FEC ratio denominator Nr: 64x238 (0x3B80))
31:16	ref_FEC_numer_Mr	

Register_Address: **0x30**
Register Name: **dpll_ctrl**
Default Value: **0x0C**
Type: R/W

Bit Field	Function Name	Description
1:0	Reserved	Leave as Default

Register_Address: **0x30** Register Name: **dpll_ctrl** Default Value: **0x0C** Type: R/W		
Bit Field	**Function Name**	**Description**
3:2	dpll_phase_slope_limit	Selects phase slope limit for DPLL 00: 61 usec/sec 01: 7.5 usec/sec 10: 0.885 usec/sec 11: unlimited
4	dpll_tie_clear_enable	Set high to align phase of the DPLL output clock with the phase of input reference.
7:5	dpll_loop_bandwidth	Selects loop bandwidth of DPLL: 000: 14 Hz 001: 28 Hz 010: 56 Hz 011: 112 Hz 100: 224 Hz 101: 448 Hz 110: 896 Hz 111: 30 mHz

Register_Address: **0x33** Register Name: **dpll_mode_refsel** Default Value: **0x03** Type: R/W		
Bit Field	**Function Name**	**Description**
1:0	dpll_mode	Selects DPLL mode of operation. 00: freerun mode 01: forced holdover mode 10: reserved 11: automatic mode In 'automatic mode', locking is based on the input reference availability. In this mode, DPLL will go to holdover only if the input reference is not available. When the 'forced holdover mode' is programmed, the input reference is ignored and DPLL has to go to holdover. When the 'freerun mode' is selected, the DPLL has to generate all its output clocks based only on the oscillator OSCI input.
7:2	reserved	Leave as default

Register_Address: **0x34** Register Name: **dpll_ref_fail_mask** Default Value: **0x87** Type: R/W		
Bit Field	**Function Name**	**Description**
3:0	dpll_holdover_mask	When set low these bits prevent DPLL from going to holdover mode when corresponding reference failure mechanism occur. xxx0: mask holdover on LOS xx0x: mask holdover on SCM x0xx: mask holdover on CFM 0xxx: mask holdover on GST **Note:** GST bit should never be programmed to 1 if neither CFM nor SCM bits are programmed to 1 (e.g. bits 3:1 should never be programmed to '100').
7:4	reserved	Leave as default

Register_Address: **0x44** Register Name: **dpll_hold_lock_fail** Default Value: **0x00** Type:**Sticky R**		
Bit Field	**Function Name**	**Description**
0	dpll_holdover_status	The device will set this bit high when DPLL is in holdover mode. **Note:** This bit is not maskable.
1	dpll_lock_status	The device will set this bit high when DPLL is locked to an input reference. **Note:** This bit is not maskable.
7:2	reserved	Leave as default

Register_Address: **0x47** Register Name: **phasememlimit_ref** Default Value: **0x0A** Type: R/W		
Bit Field	**Function Name**	**Description**
7:0	ref_phasemem_limit	Unsigned binary value of these bits are used to calculate Ref. phase memory limit. Value that needs to be written to this register is calculated as: Value = round(32 * log(PhaseMemLimit * 10^5)) Phase memory limit should be at least one half period of the clock fed the reference. Typical phase memory limits are: Phase memory limit Value Input reference frequency 10 us 0x00 higher than 200 kHz 100 us 0x20 8 kHz 1 ms 0x40 1 kHz 930 ms 0x9F 1 Hz

Register_Address: **0x4B** Register Name: **scm_cfm_limit_ref** Default Value: **0x55** Type: R/W		
Bit Field	**Function Name**	**Description**
2:0	ref_cfm_limit	These bits represent the input reference Coarse Frequency Monitor (CFM) limit selection. When the input reference fails criteria specified by these bits, the CFM failure indicator will go high (can be read in the 'Ref failure indicator' register). Selection: 000 = +/- 0.1% (in Ref frequency units) 001 = +/- 0.5% 010 = +/- 1% 011 = +/- 2% 100 = +/- 5% 101 = +/- 10% 110 = +/- 20% 111 = +/- 50%
3	reserved	Leave as default.
6:4	ref_scm_limit	These bits represent the input reference Single Cycle Monitor (SCM) limit selection. When the input reference fails criteria specified by these bits, the SCM failure indicator will go high. Selection: 000 = +/- 0.1% (in Ref frequency units) 001 = +/- 0.5% 010 = +/- 1% 011 = +/- 2% 100 = +/- 5% 101 = +/- 10% 110 = +/- 20% 111 = +/- 50% Note that the input reference clock is sampled by 800 MHz clock, so the measurement granularity is 1.25 ns. This imposes limitation to SCM limits that can be programmed depending on Ref clock frequencies: +/- 0.1% : can be programmed for frequencies below 800 kHz +/- 0.5% : below 4 MHz +/- 1% : below 8 MHz +/- 2% : below 16 MHz +/- 5% : below 40 MHz +/- 10% : below 80 MHz +/- 20% : below 160 MHz +/- 50% : below 400 MHz **Note:** SCM indicator should not be used (should be masked) for input references frequencies above 400 MHz.

Register_Address: **0x4B** Register Name: **scm_cfm_limit_ref** Default Value: **0x55** Type: R/W		
Bit Field	**Function Name**	**Description**
7	reserved	Leave as default.

Register_Address: **0x4F** Register Name: **dpll_config** Default Value: **0x31** Type:**R/W**		
Bit Field	**Function Name**	**Description**
0	dpll_config	Enables DPLL 0: DPLL disabled 1: DPLL enabled
3:1	reserved	Leave as default.
4	phase_acquisiton_enable	When set high enables phase acquisition module. When set low powers down the phase acquisition module. 1: enables phase acquisition module
7:5	reserved	Leave as default

Register_Address: **0x50:0x51** Register Name: **synth_base_freq** Default Value: **0x61A8** Type:**R/W**		
Bit Field	**Function Name**	**Description**
15:0	synth_base_freq_Bs	Unsigned binary value of these bits represents Synthesizer base frequency Bs in Hz. Values for Bs that can be programmed: 0x1388 for 5 kHz, 0x186A for 6.25 kHz, 0x1F40 for 8 kHz, 0x2710 for 10 kHz, 0x30D4 for 12.5 kHz, 0x61A8 for 25 kHz, 0x9C40 for 40 kHz. **Note:** Other Bs rates can be supported, please contact Microsemi application support team if another specific Bs rate is required

Register_Address: **0x52:0x53** Register Name: **synth_freq_multiple** Default Value: **0x0EA6** Type:**R/W**		
Bit Field	**Function Name**	**Description**
15:0	synth_base_freq_mult_Ks	Unsigned binary value of these bits represents Synthesizer base frequency multiplication number. For regular (non-FEC) synthesizer frequency, the 'Base frequency' number Bs multiplied by the 'Base frequency multiple' number Ks, and multiplied by 16 has to equal the synthesizer frequency in Hz. **Note 1:** synthesizer frequency has to be between 1 GHz and 1.5 GHz, so: Bs x Ks x 16 x Ms / Ns has to be between 1 000 000 000 and 1 500 000 000. Examples of some synthesizer frequencies and appropriate values that can be programmed for Bs and Ks to get desired synthesizer frequency: Synthesizer frequency — Base frequency Bs — Base frequency multiple Ks 1.048576 GHz — 8 kHz (0x1F40) — 8192 (0x2000) 1.24416 GHz — 40 kHz (0x9C40) — 1944 (0x0798) 1.25 GHz — 25 kHz (0x61A8) — 3125 (0x0C35) 1.50 GHz — 25 kHz (0x61A8) — 3750 (0x0EA6)

Register_Address: **0x54:0x57**
Register Name: **synth_ratio_M_N**
Default Value: **0x00010001**
Type:**R/W**

Bit Field	Function Name	Description
15:0	synth_ratio_denom_Ns	Unsigned binary value of Ms bits, in combination with unsigned binary value of Ns bits represents Synthesizer FEC multiplication ratio. Synthesizer FEC frequencies are calculated using the following formula: Synth_freq [Hz] = Bs x Ks x 16 x Ms / Ns
31:16	synth_ratio_numer_Ms	For regular (non-FEC) synthesizer frequencies, Ms and Ns should be programmed to 0x0001 (default values) Examples of some synthesizer FEC frequencies and appropriate values that can be programmed for the Bs, Ks, Ms and Ns registers to get those FEC frequencies: **a) OC-192 mode, standard EFEC for long reach:** Desired frequency: 155.52 MHz x 255 / 237 Synth frequency: 1.24416 GHz x 255/237 Base frequency Bs: 40 kHz (0x9C40) Base freq. multiplier Ks: 1944 (0x0798) FEC ratio numerator Ms: 255 (0x00FF) FEC ratio denominator Ns: 237 (0x00ED) Post div PA: 8 **b) Long reach 10GE mode, double rate conversion:** Desired frequency: 156.25 MHz x 66/64 x 255/238 Synth frequency: 1.25 GHz x 66/64 x 255/238 Base frequency Bs: 25 kHz (0x061A8) Base freq. multiplier Ks: 3125 (0x0C35) FEC ratio numerator Ms: 66x255 (0x41BE) FEC ratio denominator Ns: 64x238 (0x3B80) Post div PA: 8

Register_Address: **0x71** Register Name: **output_synth_en** Default Value: **0x01** Type:**R/W**		
Bit Field	**Function Name**	**Description**
0	synth_en	Enables output Synthesizer 0: disables synth output 1: enables synth output
7:1	reserved	Leave as default

Register_Address: **0x72** Register Name: **dpll_lock_selection** Default Value: **0xAA** Type:**R/W**		
Bit Field	**Function Name**	**Description**
1:0	dpll_lock_selection	Selects DPLL lock indicator status condition (appearing in the 'DPLL lock fail' register). 00: phase error is smaller than 36 us during 10 s 01: phase error is smaller than 1 us during 1 s 10: phase error is smaller than 10 us during 1 s 11: phase error is smaller than 10 us during 10 s
7:2	reserved	Leave as default

Register_Address: **0x73:0x76**
Register Name: **central_freq_offset**
Default Value: **0x046AAAAB**
Type:**R/W**

Bit Field	Function Name	Description
31:0	central_freq_offset	2's complement binary value of these bits represent central frequency offset for the device. This value should be used to compensate for oscillator inaccuracy, or make the device look like Numerically Controlled Oscillator (NCO). This register controls central frequency of all 4 Synthesizers. Expressed in steps of +/- 2^-32 of nominal setting. When oscillator inaccuracy is known: inacc_osc = (f_osc - f_nom)/f_nom (usually specified in ppm), value to be programmed in this register is calculated as per the following formula: X = (1/(1 + inacc_osc) - 1)*2^32, when f_osc < f_nom X = (1/(1 + inacc_osc))*2^32, when f_osc > f_nom, where inacc_osc - represents oscillator frequency inaccuracy, f_osc - represents oscillator frequency, and f_nom - represents oscillator nominal frequency (i.e., 25 MHz, 20 MHz) Generally, when the oscillator frequency is lower than the nominal, frequency offset has to be programmed to compensate it in opposite direction, i.e. frequency offset has to be positive, and vice versa. Example 1): if oscillator inaccuracy is -2% (f_osc = 24.5 MHz; inacc_osc = (f_osc - 25 MHz)/25MHz = -0.02), X= (1/(1+(-0.02)) - 1)*2^32 = (1/0.98 - 1)*2^32 = 87652394 = 0x0539782A Example 2): if oscillator inaccuracy is +2% (f_osc = 25.5 MHz; inacc_osc = (f_osc - 25 MHz)/25MHz = 0.02), X= (1/(1+ 0.02))*2^32 = (1/1.02)*2^32 = 4210752251 = 0xFAFAFAFB When NCO behavior is desired, the output frequency should be calculated as per formula: fout = (1 + X/2^32)*finit where X -represent 2's complement number specified in this register finit - initial frequency set by Bs, Ks, Ms, Ns and postdivider number for particular VCO fout - output frequency **Note 1:**The default value is based on 24.576 MHz oscillator. The default value should be changed to 0x00000000 for 20 MHz oscillator. **Note 2:** Central Frequency Offset should not exceed +/-5% off nominal.

Register_Address: **0x77** Register Name: **synth_filter_sel** Default Value: **0x00** Type:**R/W**		
Bit Field	**Function Name**	**Description**
0	synth_filter_select	Selects filter used by Synthesizer 0: external filter 1: internal filter
7:1	reserved	reserved

Register_Address: **0x78** Register Name: **synth_fine_phase_shift** Default Value: **0x00** Type:**R/W**		
Bit Field	**Function Name**	**Description**
7:0	syn_fine_phase_shift	Unsigned binary value of these bits represent Synth fine phase shift (advancement) in steps of Synth_period / 256. **Note 1:** This register controls fine phase shift for all clocks coming out of the Synthesizer (including both postdividers)

Register_Address: **0x7F** Register Name: **page_register** Default Value: **0x00** Type:**R/W**		
Bit Field	**Function Name**	**Description**
0	page_select	This register is used to toggle memory access between page 0 (addresses 0x00 to 0x7E) and page 1 (addresses 0x80 to 0xFF). This is required because SPI and I2C ports have only seven address bits and the device memory space is eight bit wide. 0: selects addresses 0x00 to 0x7E 1: selects addresses 0x80 to 0xFB
7:1	reserved	reserved

Reg_Address: **0x86:0x88** Register Name: **synth_post_div_A** Default Value: **0x00003C** Type:**R/W**		
Bit Field	**Function Name**	**Description**
15:0	frm_pulse_rate_or_div	Function of these bits depends on the value in bits[23:20]. Whenever bits[23:20] are equal to'1111' and bits[17:16] are different from '00' these bits represent number of periods of the selected clock (bits[17:16]) in between two frame pulses. Whenever bits[23:20] are equal to '1111' and bits[17:16] are equal to '00' these bits selects division factor of the low frequency output clock. The output is low frequency is equal to 2 x Synthesizer base frequency divided by the value stored in these bits. Whenever bits[23:20] are different from '1111' the value is these bits is part of output divider (bits[23:0]). The output frequency is then equal to Synthesizer output frequency divided by the value stored in bits[23:0]. **Note:** The output clock duty-cycle may not be within specified 45% to 55% when post divider value PA is an odd number and where frequency of the output clock is close to the maximum output frequency supported by hpoutclk. The worst case duty-cycle is 30% is when synthesizer frequency is set to 1 GHz and the PA is set to 7. If duty-cycle of 45% to 55% is required, user can set synthesizer to run at 1GHz * 8/7 and P0C to 8 which will still generate the same frequency but within 45% to 55% duty-cycle. For odd PA values greater than or equal to 41 (43, 45...) the duty-cycle will be within 45% to 55%. For even PA values duty-cycle is always within 45% to 55%
17:16	frm_pulse_source_or_div	Function of these bits depends on value in bits[23:20]. Whenever these bits are '11' and bits[23:20] are equal to'1111' these bits select related clock (postdivider) within the Synthesizer (frame pulse width is equal to the related clock period) Otherwise they are used to select low frequency clock ([17:16] == 10 and [23:20] == 1111) or they are used as part of divider ratio (bits[23:0]) when bits[23:20] != 1111. 00 and 01: reserved 10: low frequency clock 11: clock 1 (Synth postdivider B)

Reg_Address: **0x86:0x88** Register Name: **synth_post_div_A** Default Value: **0x00003C** Type:**R/W**		
Bit Field	**Function Name**	**Description**
18	frm_pulse_polrty_or_div	Function of this bit depends on the value in bits[23:20]. Whenever bits[23:20] are equal to ’1111’ this bit is used to select between positive and negative frame pulse. Otherwise it is used as part of divider ratio (bits[23:0]) 0: positive frame pulse 1: negative frame pulse
19	frm_pulse_type_or_div	Function of this bit depends on the value in bits[23:20]. Whenever bits[23:20] are equal to ’1111’ this bit is used to select between ST-Bus and GCI frame pulse. Otherwise it is used as part of divider ratio (bits[23:0]) 0: ST-Bus frame pulse (frame boundary in the middle of the frame pulse) 1: GCI frame pulse (frame boundary defined by first edge of the frame pulse
23:20	frm_or_low_freq_or_div	These bits select if the output is frame pulse, low frequency clock (1Hz) or regular clock (1 kHz or higher) 1111 and bits[17:16] == 00 : output is low frequency clock with 50% duty cycle with frequency equal to 2 x Synthesizer base frequency divided by the value in bits[15:0] 1111 and bits[17:16] != 00 : output is frame pulse whose width is equal to period of the clock driven from the output selected by bits[17:16] if these bits are different from ’1111’ then the output is clock with 50% duty cycle with frequency equal to the Synthesizer frequency divided by the value in bits [23:0]

Reg_Address: **0x89:0x8B** Register Name: **synth_post_div_B** Default Value: **0x00000C** Type:**R/W**		
Bit Field	**Function Name**	**Description**
15:0	frm_pulse_rate_or_div	Function of these bits depends on the value in bits[23:20]. Whenever bits[23:20] are equal to'1111' and bits[17:16] are different from '01' these bits represent number of periods of the selected clock (bits[17:16]) in between two frame pulses. Whenever bits[23:20] are equal to '1111' and bits[17:16] are equal to '01' these bits selects division factor of the low frequency output clock. The output is low frequency is equal to 2 x Synthesizer base frequency divided by the value stored in these bits. Whenever bits[23:20] are different from '1111' the value is these bits is part of output divider (bits[23:0]). The output frequency is then equal to Synthesizer output frequency divided by the value stored in bits[23:0]. **Note:** The output clock duty-cycle may not be within specified 45% to 55% when post divider value PB is an odd number and where frequency of the output clock is close to the maximum output frequency supported by hpoutclk. The worst case duty-cycle is 30% is when synthesizer frequency is set to 1 GHz and the PB is set to 7. If duty-cycle of 45% to 55% is required, user can set synthesizer to run at 1 GHz * 8/7 and PB to 8 which will still generate the same frequency but within 45% to 55% duty-cycle. For odd PB values greater than or equal to 41 (43, 45...) the duty-cycle will be within 45% to 55%. For even PB values duty-cycle is always within 45% to 55%
17:16	frm_pulse_source_or_div	Function of these bits depends on value in bits[23:20]. Whenever these bits are '10' and bits[23:20] are equal to '1111' these bits select related clock (postdivider) within the Synthesizer (frame pulse width is equal to the related clock period) Otherwise they are used to select low frequency clock ([17:16] == 11 and [23:20] == 1111) or they are used as part of divider ratio (bits[23:0]) when bits[23:20] != 1111. 00 and 01: reserved 10: clock 2 (Synth 0 postdivider A) 11: low frequency clock

Reg_Address: **0x89:0x8B** Register Name: **synth_post_div_B** Default Value: **0x00000C** Type:**R/W**		
Bit Field	**Function Name**	**Description**
18	frm_pulse_polrty_or_div	Function of this bit depends on the value in bits[23:20]. Whenever bits[23:20] are equal to ’1111’ this bit is used to select between positive and negative frame pulse. Otherwise it is used as part of divider ratio (bits[23:0]) 0: positive frame pulse 1: negative frame pulse
19	frm_pulse_type_or_div	Function of this bit depends on the value in bits[23:20]. Whenever bits[23:20] are equal to ’1111’ this bit is used to select between ST-Bus and GCI frame pulse. Otherwise it is used as part of divider ratio (bits[23:0]) 0: ST-Bus frame pulse (frame boundary in the middle of the frame pulse) 1: GCI frame pulse (frame boundary defined by first edge of the frame pulse
23:20	frm_or_low_freq_or_div	These bits select if the output is frame pulse, low frequency clock (1Hz) or regular clock (1KHz or higher) 1111 and bits[17:16] == 01 : output is low frequency clock with 50% duty cycle with frequency equal to 2 x Synthesizer base frequency divided by the value in bits[15:0] 1111 and bits[17:16] != 01 : output is frame pulse whose width is equal to period of the clock driven from the output selected by bits[17:16] if these bits are different from ’1111’ then the output is clock with 50% duty cycle with frequency equal to the Synthesizer frequency divided by the value in bits [23:0]

Register_Address: **0xB1** Register Name: **hp_cmos_en** Default Value: **0x00** Type:**R/W**		
Bit Field	**Function Name**	**Description**
1:0	hp_cmos_en	Set high to enable corresponding high performance output. Set low to tristate the corresponding output. x1: enables hpout0 1x: enables hpout1
7:2	reserved	Leave as default.

Register_Address: **0xB8** Register Name: **synth_stop_clock** Default Value: **0x00** Type:**R/W**		
Bit Field	**Function Name**	**Description**
1:0	synth_post_div_A_stop	Appropriate setting of these bits will cause Synthesizer Post Divider A to stop clock at either rising or falling edge. Selection: 00 - 01: continuous run (stop clock function is disabled) 10: stop hpoutclk0 at falling edge (output stays low) 11: stop hpoutclk0 at rising edge (output stays high)
3:2	synth_post_div_B_stop	Appropriate setting of these bits will cause Synthesizer Post Divider B to stop clock at either rising or falling edge. Selection: 00 - 01: continuous run (stop clock function is disabled) 10: stop hpoutclk1 at falling edge (output stays low) 11: stop hpoutclk1 at rising edge (output stays high)
7:4	reserved	Leave as default

Register_Address: **0xB9** Register Name:**sync_fail_flag_status** Default Value: **0x00** Type:**StickyR**		
Bit Field	**Function Name**	**Description**
0	Synth_syncFail_flag	When high, this bit indicates that Synthesizer has lost lock. If this status bit appears set after clearing Synth_ClearSyncFail_flag (register at address 0xBA), it is indication that Synthesizer has lost lock, therefore generating wrong output frequency. **Note:** This bit will be set upon power up or device reset.
7:1	reserved	Leave as default.

Register_Address: **0xBA** Register Name:**clear_sync_fail_flag** Default Value: **0x00** Type:**R/W**		
Bit Field	**Function Name**	**Description**
0	Synth_clearSyncFail_flag	When high, this bit clears sticky Synth_syncFail_flag. **Note:** after clearing Synth_syncFail_flag, this bit must be set low for normal device operation
7:1	reserved	Leave as default.

Register_Address: **0xBF:0xC0** Register Name:**phase_shift_s_postdiv_a** Default Value: **0x0000** Type:**R/W**		
Bit Field	**Function Name**	**Description**
12:0	phase_shift_s_postdiv_a	2's complement binary value of these bits represent phase shift in steps of one period of Synthesizer frequency for all clocks coming from Synthesizer Post Divider A (0:no shift, -1: delay output clock for 1 period, 1: advance output clock for 1 period, and so on)
15:13	quad_shift_s_postdiv_a	These bits select quadrature phase shift (in 45 degrees step, from -135 to +135 degrees) for all clocks coming from Synthesizer Post Divider A. 000: 0 degrees (no shift) 001: -45 degrees 010: -90 degrees 011: -135 degrees 100: -180 (or 180) degrees 101: 135 degrees 110: 90 degrees 111: 45 degrees

Register_Address: **0xC1:0xC2** Register Name:**phase_shift_s_postdiv_b** Default Value: **0x0000** Type:**R/W**		
Bit Field	**Function Name**	**Description**
12:0	phase_shift_s_postdiv_b	2's complement binary value of these bits represent phase shift in steps of one period of Synthesizer frequency for all clocks coming from Synthesizer Post Divider B (0: no shift, -1: delay output clock for 1 period, 1: advance output clock for 1 period, and so on)

Register_Address: **0xC1:0xC2** Register Name:**phase_shift_s_postdiv_b** Default Value: **0x0000** Type:**R/W**		
Bit Field	**Function Name**	**Description**
15:13	quad_shift_s_postdiv_b	These bits select quadrature phase shift (in 45 degrees step, from -135 to +135 degrees) for all clocks coming from Synthesizer Post Divider B. 000: 0 degrees (no shift) 001: -45 degrees 010: -90 degrees 011: -135 degrees 100: -180 (or 180) degrees 101: 135 degrees 110: 90 degrees 111: 45 degrees

Register_Address: **0xC3** Register Name:**xo_or_crystal_sel** Default Value: **0x00** Type:**R/W**		
Bit Field	**Function Name**	**Description**
0	xo_or_crystal_sel	0: enables OSCo driver 1: disables OSCo driver Set to 1 when xo is used as master clock. Set to 0 when crystal is used as master clock.
7:1	Reserved	Leave as default

Register_Address: **0xC6** Register Name:**chip_revison** Default Value: **0x03** Type:**R/W**		
Bit Field	**Function Name**	**Description**
7:0	chip_revision	When the Chip Revision bits in the ID register at address 0x00 are set to '00', value of chip_revision register represents chip revision number: 0x00: Whenever Chip Revision bits in ID register at address 0x00 are different from 0b00 0x01: RevF 0x03: RevH

Register_Address: **0xE0** Register Name:**gpio_function_pin0** Default Value: **0x00** Type:**R/W**		
Bit Field	**Function Name**	**Description**
6:0	gpio_pin0_table_address	Unsigned binary value of these bits represents bit address in the control or status table, depending on 'GPIO0 control or status select' bit. The control and status table consist of 128 bits each. Default: GPIO pin unused.
7	gpio_pin0_con_or_stat_sel	Selects whether GPIO0 is input (control) pin or output (status) pin. Selection: 0 = control 1 = status

Register_Address: **0xE1** Register Name:**gpio_function_pin1** Default Value: **0x00** Type:**R/W**		
Bit Field	**Function Name**	**Description**
6:0	gpio_pin1_table_address	Unsigned binary value of these bits represents bit address in the control or status table, depending on 'GPIO1 control or status select' bit. The control and status table consist of 128 bits each. Default: GPIO pin unused.
7	gpio_pin1_con_or_stat_sel	Selects whether GPIO1 is input (control) pin or output (status) pin. Selection: 0 = control 1 = status

Register_Address: **0xE2** Register Name:**gpio_function_pin2** Default Value: **0x70** Type:**R/W**		
Bit Field	**Function Name**	**Description**
6:0	gpio_pin2_table_address	Unsigned binary value of these bits represents bit address in the control or status table, depending on 'GPIO2 control or status select' bit. The control and status table consist of 128 bits each. Default: hpdiff0 enable.
7	gpio_pin2_con_or_stat_sel	Selects whether GPIO2 is input (control) pin or output (status) pin. Selection: 0 = control 1 = status

Register_Address: **0xE3** Register Name:**gpio_function_pin3** Default Value: **0x00** Type:**R/W**		
Bit Field	**Function Name**	**Description**
6:0	gpio_pin3_table_address	Unsigned binary value of these bits represents bit address in the control or status table, depending on 'GPIO3 control or status select' bit. The control and status table consist of 128 bits each. Default: GPIO pin unused.
7	gpio_pin3_con_or_stat_sel	Selects whether GPIO3 is input (control) pin or output (status) pin. Selection: 0 = control 1 = status

Register_Address: **0xE4** Register Name:**gpio_function_pin4** Default Value: **0x00** Type:**R/W**		
Bit Field	**Function Name**	**Description**
6:0	gpio_pin4_table_address	Unsigned binary value of these bits represents bit address in the control or status table, depending on 'GPIO4 control or status select' bit. The control and status table consist of 128 bits each. Default: GPIO pin unused.
7	gpio_pin4_con_or_stat_sel	Selects whether GPIO4 is input (control) pin or output (status) pin. Selection: 0 = control 1 = status

Register_Address: **0xE5** Register Name:**gpio_function_pin5** Default Value: **0x00** Type:**R/W**		
Bit Field	**Function Name**	**Description**
6:0	gpio_pin5_table_address	Unsigned binary value of these bits represents bit address in the control or status table, depending on 'GPIO5 control or status select' bit. The control and status table consist of 128 bits each. Default: GPIO pin unused..
7	gpio_pin5_con_or_stat_sel	Selects whether GPIO5 is input (control) pin or output (status) pin. Selection: 0 = control 1 = status

Register_Address: **0xE6** Register Name:**gpio_function_pin6** Default Value: **0x72** Type:**R/W**		
Bit Field	**Function Name**	**Description**
6:0	gpio_pin6_table_address	Unsigned binary value of these bits represents bit address in the control or status table, depending on 'GPIO6 control or status select' bit. The control and status table consist of 128 bits each. Default:Enable hpoutclk1.
7	gpio_pin6_con_or_stat_sel	Selects whether GPIO6 is input (control) pin or output (status) pin. Selection: 0 = control 1 = status

Register_Address: **0xEC** Register Name:**dpll_ctrl2** Default Value: **0x00** Type: **R/W**		
Bit Field	**Function Name**	**Description**
4:0	Holdover Storage delay	The storage delay is set using the formula Value = round(8 * log(StorageDelay/10) Note: StorageDelay is in ms. Example values: 0x00: 10 ms 0x08: 100 ms 0x10: 1 s 0x1D: 42.2 s
5	Reserved	Leave as default
7:6	Input edge sensitivity	Select the inout sign of the signal Note: The pulse options select the middle between the edges Selection: 00: positive (rising) edge 01: negative (falling) edge 10: low pulse 11: high pulse

Register_Address: **0xED** Register Name:**dpll_holdpull** Default Value: **0x07** Type:**R/W**		
Bit Field	**Function Name**	**Description**
2:0	Hold-in/pull-in range	Selects the hold-in/pull-in range for the DPLL Selection: 000:12 ppm 001: 52 ppm 010: 83 ppm 011: 130 ppm 100: 400 ppm 101: reserved 110: reserved 111: unlimited
7:3	Reserved	

Register_Address: **0xF4** Register Name:**pfm_mask_ho** Default Value: **0xF0** Type:**R/W**		
Bit Field	**Function Name**	**Description**
3:0	Reserved	Leave as default
4	DPLL holdover mask on PFM alarm	Set to 0 to mask DPLL holdover on PFM alarm
7:5	Reserved	Leave as default

Register_Address: **0xF5** Register Name:**pfm_mask_reffail** Default Value: **0x00** Type:**R/W**		
Bit Field	**Function Name**	**Description**
0	Ref Fail PFM Mask	Set to 0 to mask PFM alarm indication for the input reference
7:1	Reserved	Leave as default

Register_Address: **0xF7** Register Name:**pfm_range** Default Value: **0x33** Type:**R/W**		
Bit Field	**Function Name**	**Description**
2:0	pfm_range	This values controls the acceptance and rejection ranges for the frequency monitor for the input reference. Frequencies within the lower range will always be accepted and frequencies outside of the high range will always be rejected. The state remains unchanged for frequencies between the two ranges. Selection Acceptance Range (ppm), Rejection Range (ppm) 000: 9.2, 12 001: 40, 52 010: 64, 83 011: 100, 130 100: 13.8, 18 101: 24.6, 32 110: 33.6, 47.5 111: 52, 67.5
7:3	Reserved	Leave as default

9.0 AC and DC Electrical Characteristics

Absolute Maximum Ratings*

	Parameter	Symbol	Min.	Max.	Units
1	Supply voltage	V_{DD_R}	-0.5	4.6	V
2	Core supply voltage	V_{CORE_R}	-0.5	2.5	V
3	Voltage on any digital pin	V_{PIN}	-0.5	6	V
4	Voltage on osci and osco pin	V_{OSC}	-0.3	V_{DD} + 0.3	V
5	Storage temperature	T_{ST}	-55	125	°C

* Exceeding these values may cause permanent damage. Functional operation under these conditions is not implied.
* Voltages are with respect to ground (GND) unless otherwise stated

Recommended Operating Conditions*

	Characteristics	Sym	Min.	Typ.	Max.	Units
1	Supply voltage	V_{DD-IO} AV_{DD}	3.135	3.30	3.465	V
2	Core supply voltage	V_{CORE} AV_{CORE}	1.71	1.80	1.89	V
3	Operating temperature	T_A	-40	25	85	°C

* Voltages are with respect to ground (GND) unless otherwise stated

DC Electrical Characteristics* - Power - Core

	Characteristics	Sym	Typ.	Max.	Units	Notes
1	Core supply current (Vcore)	I_{CORE} (Vdd 3.3V)	46	48	mA	
		I_{CORE} (Vdd 1.8V)	102	109	mA	
2	Current for HP Synthesis Engine	I_{SYN} (Vdd 3.3V)	57	73	mA	
		I_{SYN}(Vdd 1.8V)	0.2	1	mA	

DC Electrical Characteristics* - Inputs

	Characteristics	Sym.	Min.	Typ.	Max.	Units	Notes
1	CMOS high-level input voltage	V_{CIH}	$0.7 \cdot V_{DD-IO}$			V	
2	CMOS low-level input voltage	V_{CIL}			$0.3 \cdot V_{DD-IO}$	V	
3	CMOS Input leakage current	I_{IL}	-10		10	µA	$V_I = V_{DD}$ or 0 V
4	Differential input common mode voltage	V_{CM}	1.1		2.0	V	
5	Differential input voltage difference	V_{ID}	0.25		1.0	V	

AC/DC Electrical Characteristics* - OSCi Input

	Characteristics	Sym.	Min.	Typ.	Max.	Units	Notes
1	CMOS high-level input voltage	V_{CIH}	2.0			V	
2	CMOS low-level input voltage	V_{CIL}			0.8	V	
3	Input leakage current	I_{IL}	-10		10	µA	$V_I = V_{DD}$ or 0 V
4	Duty Cycle		40		60	%	

DC Electrical Characteristics* - High Performance Outputs

	Characteristics	Sym.	Min.	Typ.	Max.	Units	Notes
1	HPCMOS High-level output voltage	V_{OH}	$0.8 \cdot AV_{DD}$			V	I_{OH} = 2mA C_L = 5pF
2	HPCMOS Low-level output voltage	V_{OL}			$0.2 \cdot AV_{DD}$	V	I_{OL} = 2mA C_L = 5pF

AC Electrical Characteristics† - Output Timing Parameters Measurement Voltage Levels (see Figure 24)

	Characteristics	Sym.	CMOS	Units
1	Threshold Voltage	$V_{T\text{-}CMOS}$	$0.5V_{DD}$	V
2	Rise and Fall Threshold Voltage High	V_{HM}	$0.8V_{DD}$	V
3	Rise and Fall Threshold Voltage Low	V_{LM}	$0.2V_{DD}$	V

* Supply voltage and operating temperature are as per Recommended Operating Conditions.
* Voltages are with respect to ground (GND) unless otherwise stated

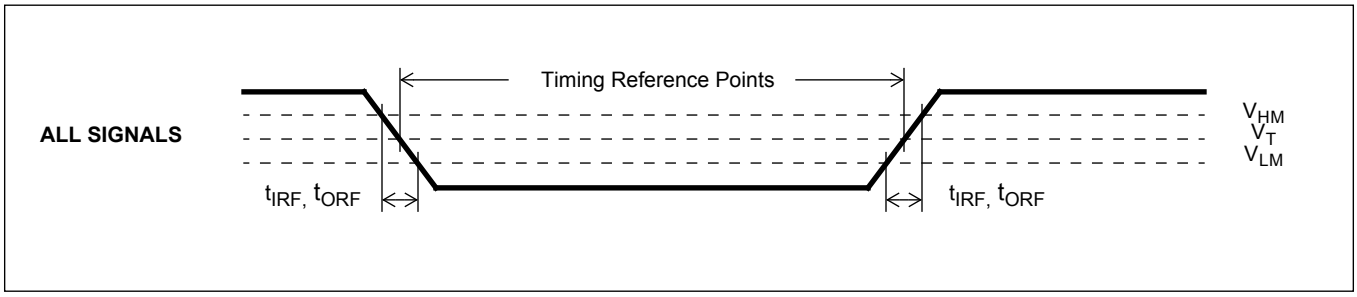


Figure 24 - Timing Parameter Measurement Voltage Levels

AC Electrical Characteristics* - Inputs (see Figure 25).

	Characteristics	Symbol	Min.	Typ.	Max.	Units
1	Input reference Frequency (CMOS Inputs)	$1/t_{REFP}$			177.5	MHz
2	Input reference Frequency (LVPECL Inputs)	$1/t_{REFP}$			750	MHz
3	Input reference pulse width high or low	t_{REFW}	0.55			ns

* Supply voltage and operating temperature are as per Recommended Operating Conditions

AC Electrical Characteristics* - Input To Output Timing (see Figure 25)

	Characteristics	Symbol	Min.	Typ.	Max.	Units
1	Input reference to hpoutclk0 output clock (with same frequency) delay	t_{HP_REFD}		0		ns

* Supply voltage and operating temperature are as per Recommended Operating Conditions.

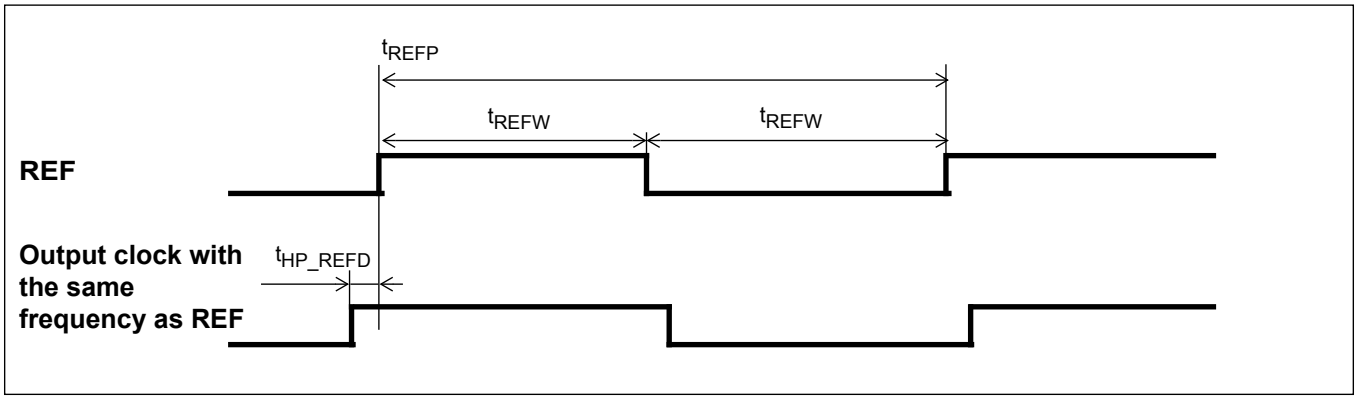


Figure 25 - Input To Output Timing for hpoutclk0

AC Electrical Characteristics* - Outputs (see Figure 26).

	Characteristics	Sym.	Min.	Typ.	Max.	Units	Notes
1	Clock skew between outputs	$t_{OUT2OUTD}$		0		ns	
2	Output clock Duty Cycle	t_{PWH}, t_{PWL}	45%	50%	55%	Duty Cycle	
3	LVCMOS output clock rise and fall time	t_r / t_f	620	950	1490	ps	10pF load
4	Output Clock Frequency (hpoutclk)	F_{hpout}			177.5	MHz	

* Supply voltage and operating temperature are as per Recommended Operating Conditions

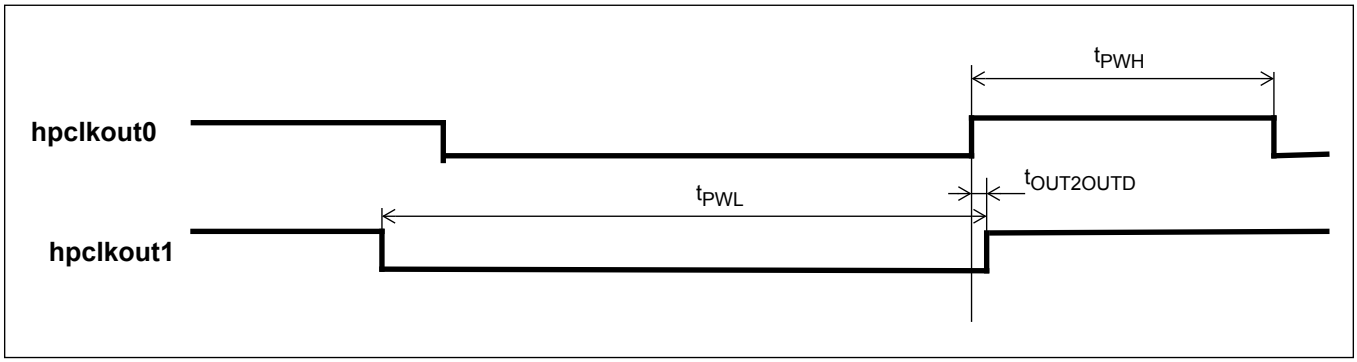


Figure 26 - Output Timing Referenced To hpclkout0

Functional waveforms and timing characteristics for the LSB first mode are shown in Figure 27, and Figure 28 describe the MSB first mode. Table 7 shows the timing specifications.

Specification	Name	Min.	Max.	Units
sck period	tcyc	124		ns
sck pulse width low	tclkl	62		ns
sck pulse width high	tclkh	62		ns
si setup (write) from sck rising	trxs	10		ns
si hold (write) from sck rising	trxh	10		ns
so delay (read) from sck falling	txd		25	ns
cs_b setup from sck falling (LSB first)	tcssi	20		ns
cs_b setup from sck rising (MSB first)	tcssm	20		ns
cs_b hold from sck falling (MSB first)	tcshm	10		ns
cs_b hold from sck rising (LSB first)	tcshi	10		ns
cs_b to output high impedance	tohz		60	ns

Table 7 - Serial Peripheral Interface Timing

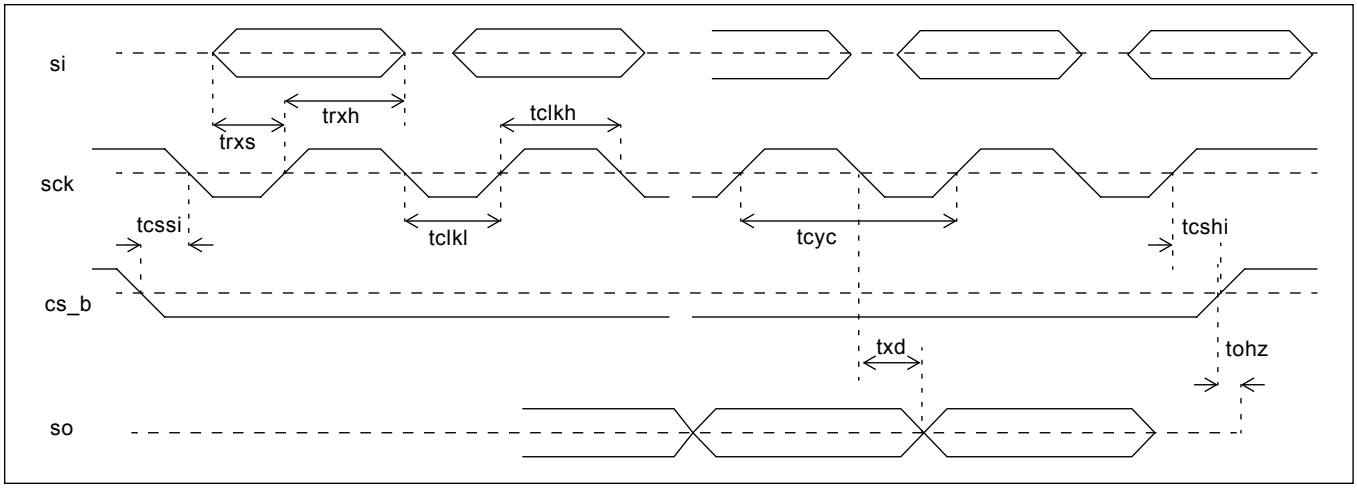


Figure 27 - Serial Peripheral Interface Timing - LSB First Mode

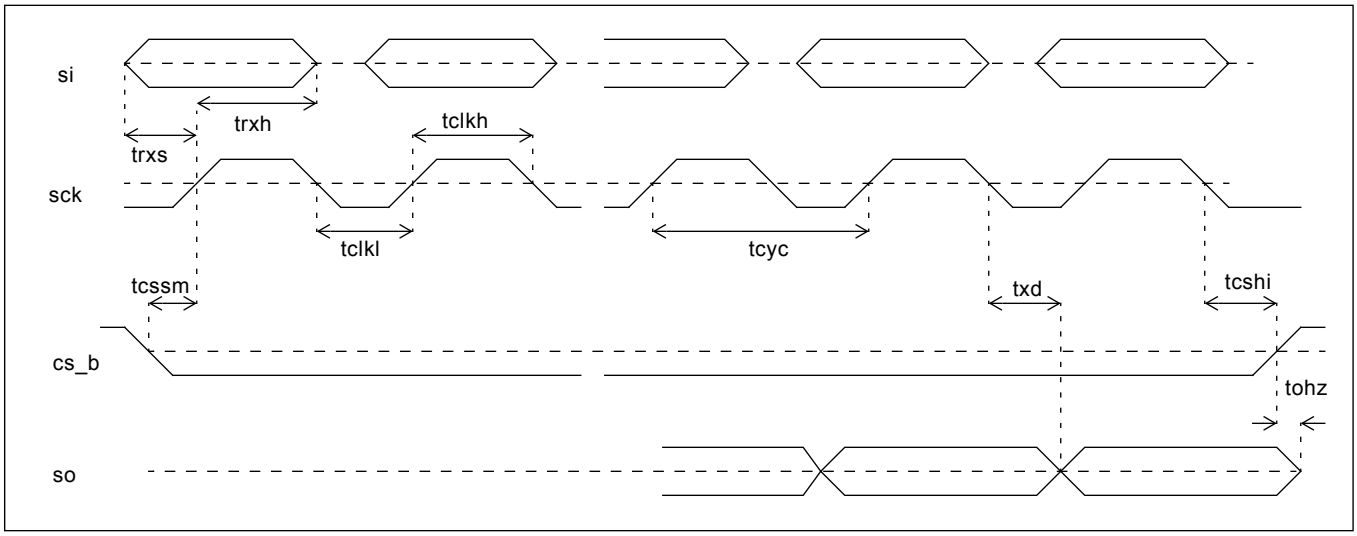


Figure 28 - Serial Peripheral Interface Timing - MSB First Mode

The timing specification for the I^{2}C interface is shown in Figure 29 and Table 8.

Specification	Name	Min.	Typ.	Max.	Units	Note
SCL clock frequency	f_{SCL}	0		400	kHz	
Hold time START condition	$t_{HD:STA}$	0.6			us	
Low period SCL	t_{LOW}	1.3			us	
Hi period SCL	t_{HIGH}	0.6			us	
Setup time START condition	$t_{SU:STA}$	0.6			us	
Data hold time	$t_{HD:DAT}$	0		0.9	us	
Data setup time	$t_{SU:DAT}$	100			ns	
Rise time	t_r				ns	Determined by choice of pull-up resistor
Fall time	t_f	20 + 0.1C_b		250	ns	
Setup time STOP condition	$t_{SU:STO}$	0.6			us	
Bus free time between STOP/START	t_{BUF}	1.3			us	
Pulse width of spikes which must be suppressed by the input filter	t_{SP}	0		50	ns	
Max capacitance for each I/O pin				10	pF	

Table 8 - I^{2}C Serial Microport Timing

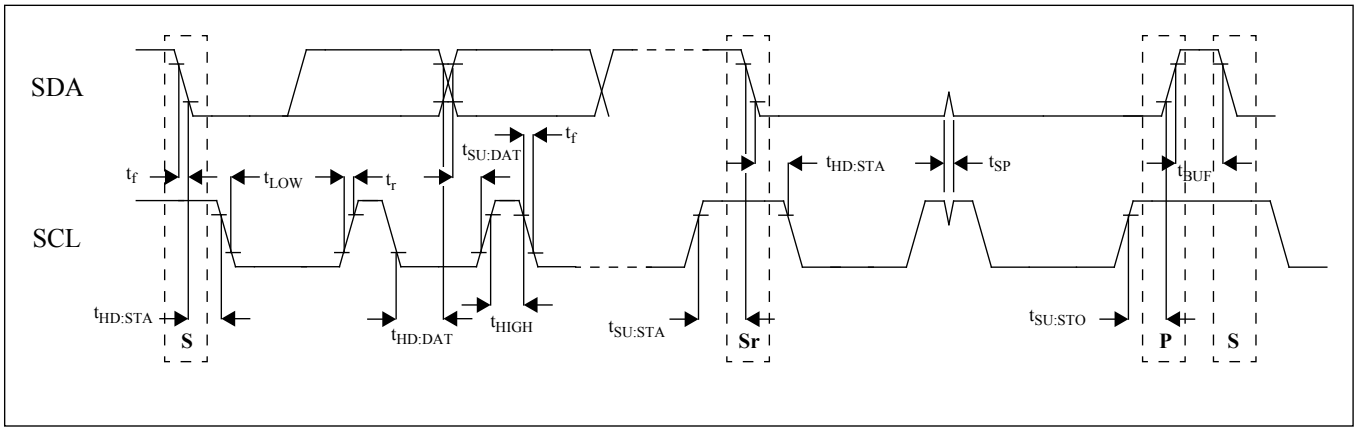


Figure 29 - I²C Serial Microport Timing

10.0 Performance Characterization

10.1 Output Clocks Jitter Generation

Output Frequency	Jitter Measurement Filter	Max.	Units	Notes
25 MHz	12 kHz - 5 MHz	0.81	ps_{rms}	
77.76 MHz	12 kHz - 20 MHz	1.25	ps_{rms}	
125 MHz	12 kHz - 20 MHz	1.01	ps_{rms}	
156.25 MHz	12 kHz - 20 MHz	1.03	ps_{rms}	

Table 9 - Jitter Generation Specifications - HPOUT Outputs

10.2 DPLL Performance Characteristics

	Characteristics	Min.	Typ.	Max.	Units	Notes
1	Pull-in/Hold-in Range	+/-52		+/-3900	ppm	user selectable
2	Frequency Lock Time			1	sec	loop bandwidth larger or equal than 14 Hz and unlimited phase slope
				90	sec	loop bandwidth 30mHz
3	Entry into Holdover MTIE			5	nsec	
4	Exit from Holdover MTIE			5	nsec	
5	Holdover Accuracy			50	ppb	
6	Phase gain in the passband			0.1	dB	

Note) Lock time of 1 sec is achieved when pulling a 9.2ppm reference for any selected bandwidth except 30 mHz and when phase slope limit is larger than 7.5usec.

Table 10 - DPLL Characteristics

11.0 Thermal Characteristics

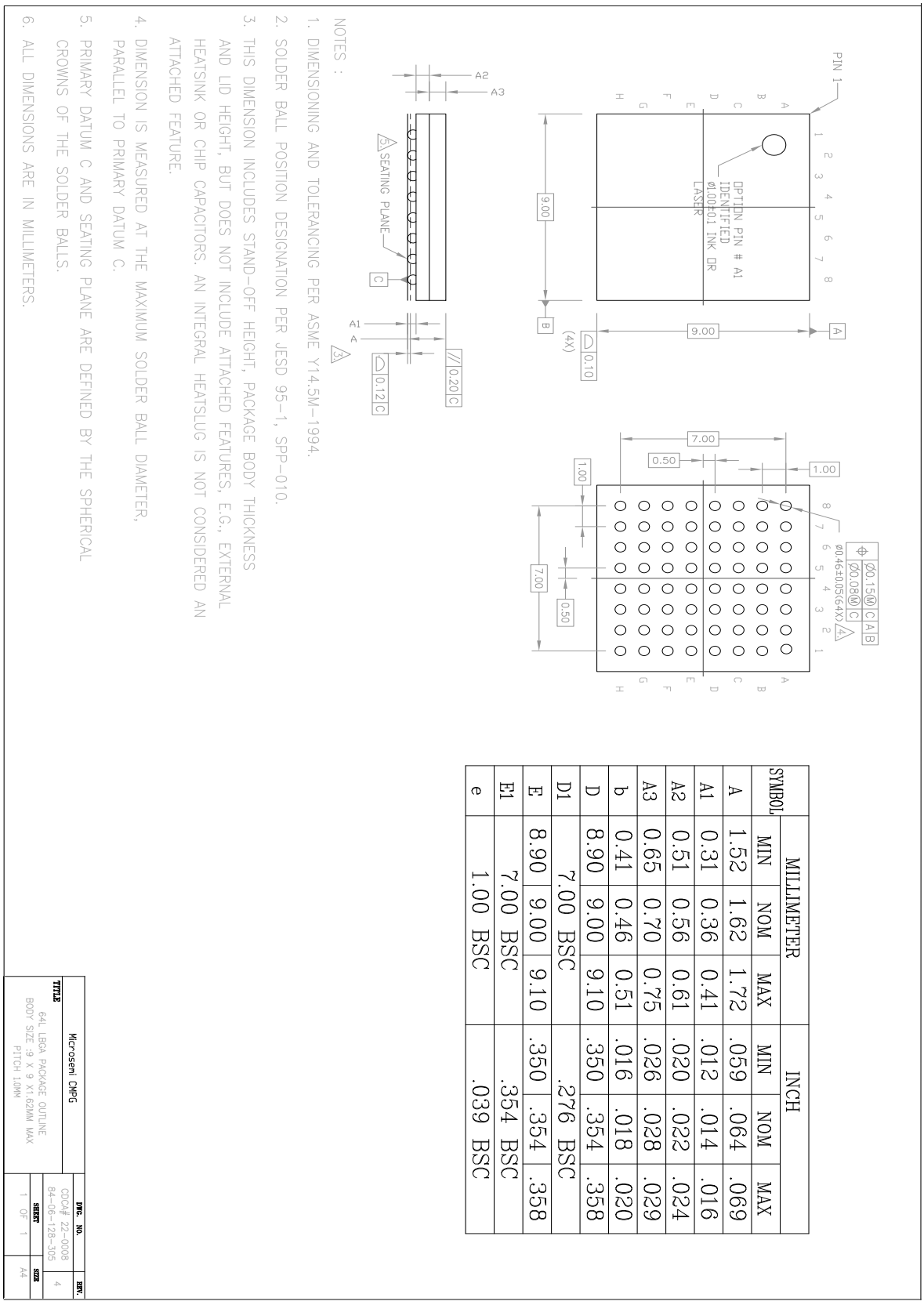
y

Parameter	Symbol	Test Condition	Value	Unit
Junction to Ambient Thermal Resistance	θ_{ja}	Still Air 1 m/s 2 m/s	35.5 31.9 30.6	^{o}C/W
Junction to Case Thermal Resistance	θ_{jc}		8.3	^{o}C/W
Maximum Junction Temperature note	T_{jmax}		125	^{o}C
Maximum Ambient Temperature	T_A		85	^{o}C

Note) Proper thermal management must be practiced to ensure that T_{jmax} is not exceeded.

Table 11 - Thermal Data

Mechanical Drawing



SYMBOL	MILLIMETER			INCH		
	MIN	NOM	MAX	MIN	NOM	MAX
A	1.52	1.62	1.72	.059	.064	.069
A1	0.31	0.36	0.41	.012	.014	.016
A2	0.51	0.56	0.61	.020	.022	.024
A3	0.65	0.70	0.75	.026	.028	.029
b	0.41	0.46	0.51	.016	.018	.020
D	8.90	9.00	9.10	.350	.354	.358
D1	7.00 BSC			.276 BSC		
E	8.90	9.00	9.10	.350	.354	.358
E1	7.00 BSC			.354 BSC		
e	1.00 BSC			.039 BSC		

NOTES :

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M-1994.
2. SOLDER BALL POSITION DESIGNATION PER JESD 95-1, SPP-010.
3. THIS DIMENSION INCLUDES STAND-OFF HEIGHT, PACKAGE BODY THICKNESS AND LID HEIGHT, BUT DOES NOT INCLUDE ATTACHED FEATURES, E.G., EXTERNAL HEATSINK OR CHIP CAPACITORS. AN INTEGRAL HEATSLUG IS NOT CONSIDERED AN ATTACHED FEATURE.
4. DIMENSION IS MEASURED AT THE MAXIMUM SOLDER BALL DIAMETER, PARALLEL TO PRIMARY DATUM C.
5. PRIMARY DATUM C AND SEATING PLANE ARE DEFINED BY THE SPHERICAL CROWNS OF THE SOLDER BALLS.
6. ALL DIMENSIONS ARE IN MILLIMETERS.

Microsemi CMPG	DWG. NO. CDCA# 22-0008 84-06-128-305	REV. 4
TITLE 64L LBGA PACKAGE OUTLINE BODY SIZE :9 X 9 X1.62MM MAX PITCH 1.0MM	SHEET 1 OF 1	SIZE A4

12.0 Package Markings

12.1 64-pin BGA. Package Top Mark Format

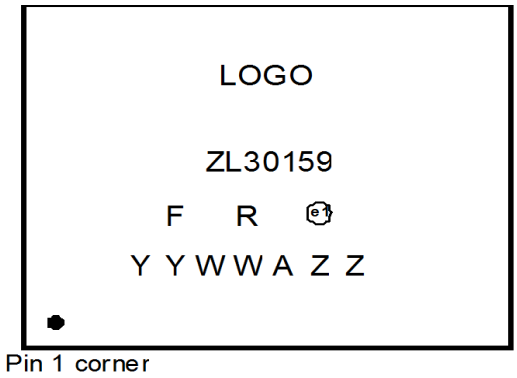


Figure 30 - Non-customized Device Top Mark

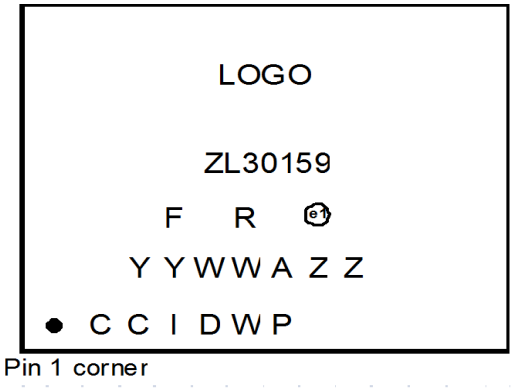


Figure 31 - Custom Factory Programmed Device Top Mark

Line	Characters	Description
1	ZL30159	Part Number
2	F	Fab Code
2	R	Product Revision Code
2	e1	Denotes Pb-Free Package
3	YY	Last Two Digits of the Year of Encapsulation
3	WW	Work Week of Assembly
3	A	Assembly Location Code
3	ZZ	Assembly Lot Sequence
4	CCID	Custom Programming Identification Code
4	WP	Work Week of Programming

Table 12 - Package Marking Legend

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