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Z80230/Z85230/L

Enhanced Serial
Communications Controller

Product Specification

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Revision History

Each instance in Revision History reflects a change to this document from its previous revision. For more details, refer to the corresponding pages and appropriate links in the table below.

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May 2009	06	system update change only - no technical content revised	n/a
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Pin Descriptions

The Enhanced Serial Communication Controller (ESCC) pins are divided into seven functional groups:

1. Address/Data
2. Bus Timing and Reset
3. Device Control
4. Interrupt
5. Serial Data (both channels)
6. Peripheral Control (both channels)
7. Clocks (both channels)

Figure 1 on page 2 and Figure 2 on page 2 display the pins in each functional group for both the Z80230 and Z85230/L. The pin functions are unique to each bus interface version in the Address/Data group, Bus Timing and Reset group, and Device Control group.

The Address/Data group consists of the bidirectional lines used to transfer data between the CPU and the ESCC (addresses in the Z80230 are latched by $\overline{AS}$). The direction of these lines depends on whether the operation is a Read or a Write operation.

The Timing and Control groups designate the type of transaction to occur and the timing of the occurrence. The interrupt group provides inputs and outputs for handling and prioritizing interrupts. The remaining groups are divided into Channel A and Channel B groups for:

- Serial Data (Transmit or Receive)
- Peripheral Control (such as DMA or modem)
- Input and Output Line for the Receive and Transmit Clocks

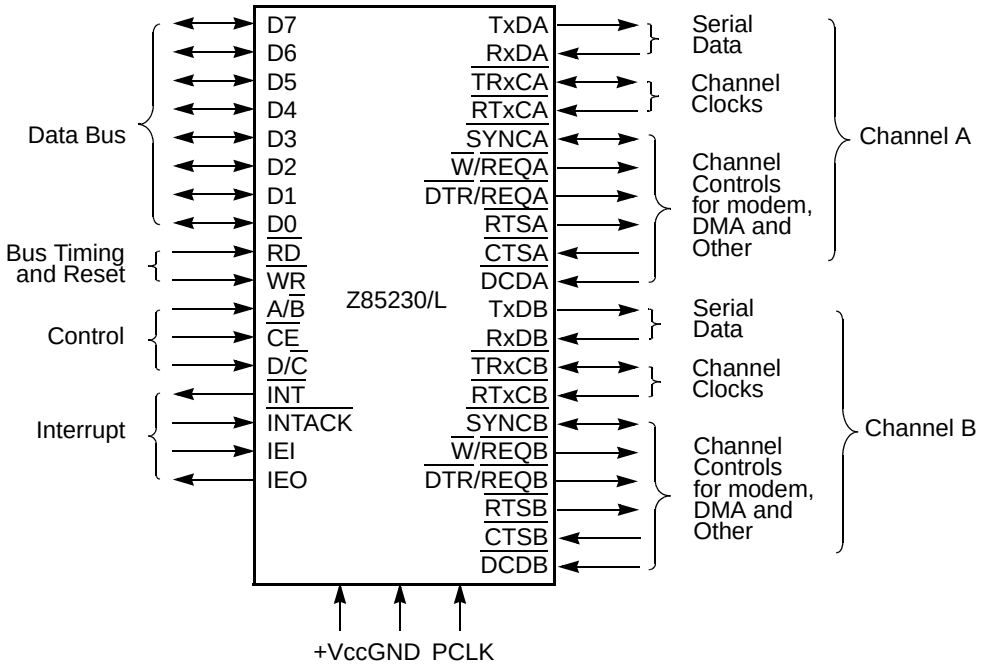


Figure 1. Z85230/L Pin Functions

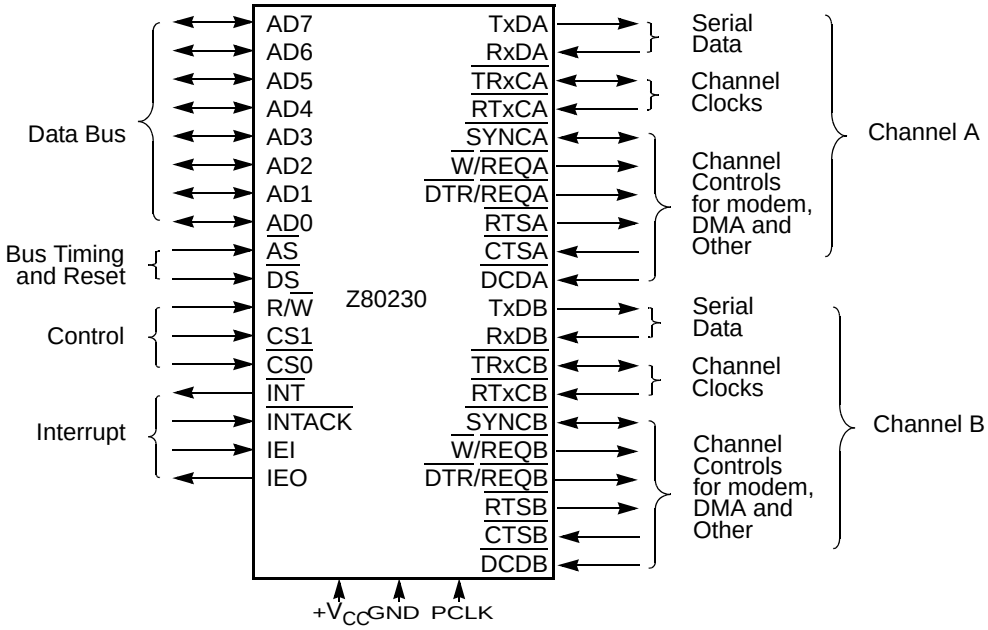


Figure 2. Z80230 Pin Functions

Figure 3 displays the Z85230/L DIP and PLCC pin assignments, respectively. Figure 4 displays the Z80230 DIP and PLCC pin assignments.

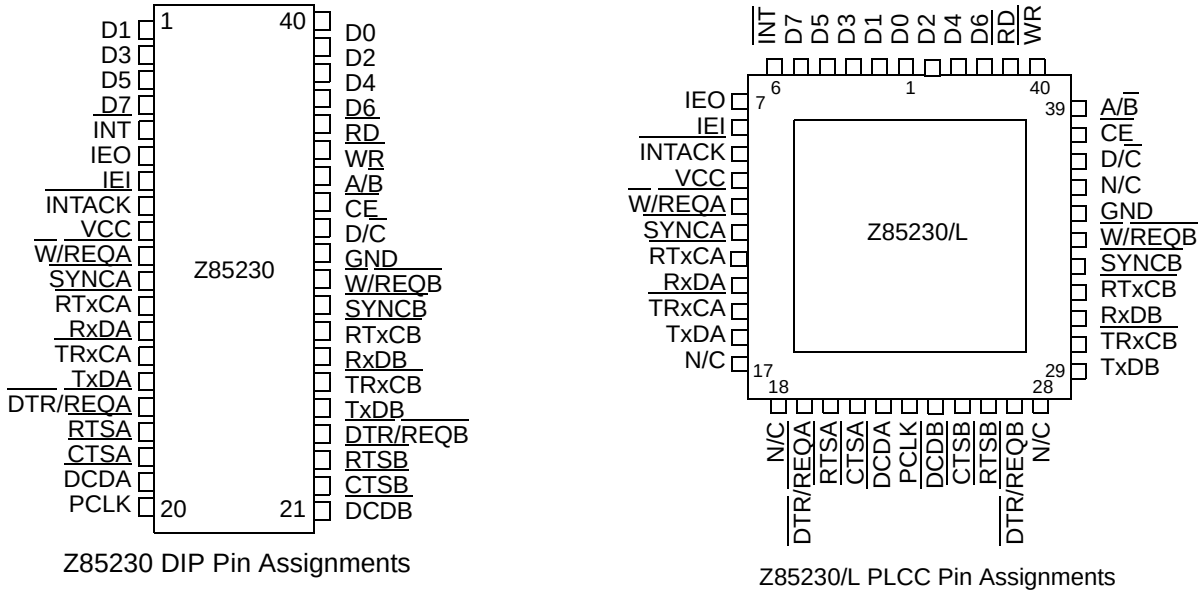


Figure 3. Z85230/L Pin Assignments

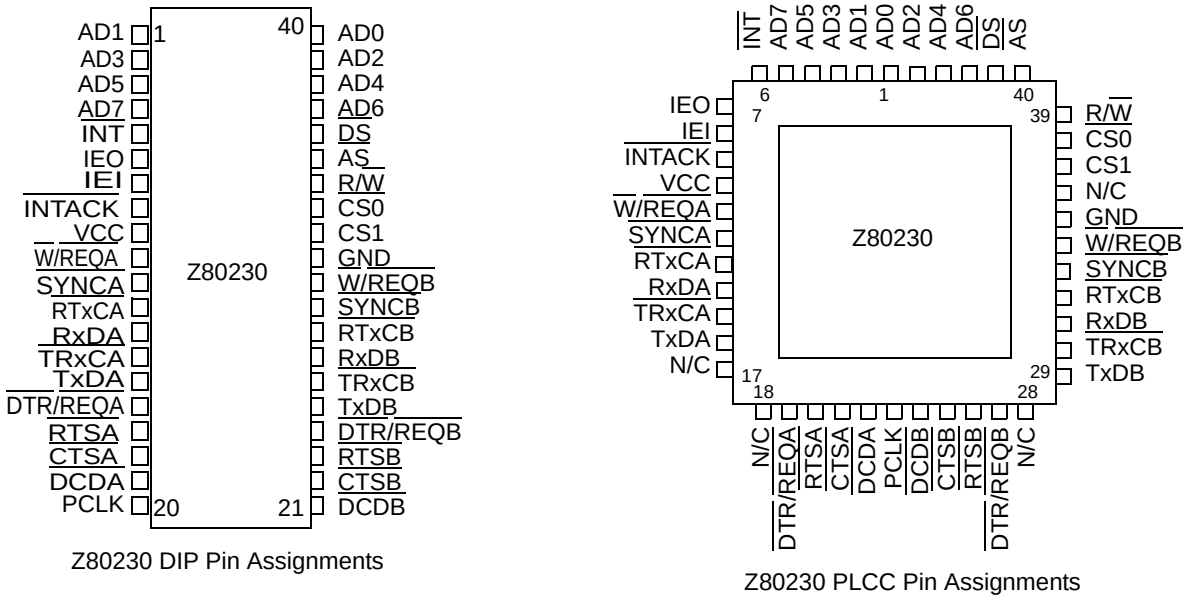


Figure 4. Z80230 Pin Assignments

Pins Common to Both Z85230/L and Z80230

The pin descriptions for pins common to both Z85230/L and Z80230 are provided below:

$\overline{\text{CTSA}}$, $\overline{\text{CTSB}}$ (Clear To Send (Inputs, Active Low))—These pins function as transmitter enables if they are programmed for AUTO ENABLE (WR3 bit 5 is 1), in which case a Low on each input enables the respective transmitter. If not programmed as AUTO ENABLE, the pins may be used as general-purpose inputs. These pins are Schmitt-trigger buffered to accommodate slow rise-time inputs. The ESCC detects pulses on these pins and may interrupt the CPU on both logic level transitions.

$\overline{\text{DCDA}}$, $\overline{\text{DCDB}}$ (Data Carrier Detect (Inputs, Active Low))—These pins function as receiver enables if they are programmed for AUTO ENABLE (WR3 bit 5 is 1); otherwise, they are used as general-purpose input pins. The pins are Schmitt-trigger buffered to accommodate slow rise-time signals. The ESCC detects pulses on these pins and may interrupt the CPU on both logic level transitions.

$\overline{\text{RTSA}}$, $\overline{\text{RTSB}}$ (Request To Send (Outputs, Active Low))—The $\overline{\text{RTS}}$ pins can be used as general-purpose outputs or with the AUTO ENABLE feature. When AUTO-ENABLE is off, these pins follow the inverse state of WR5 bit 1. When used with the AUTO-ENABLE feature in ASYNCHRONOUS mode, this pin immediately goes Low when WR5 bit 1 is 1. When WR5 bit 0 is 0, this pin remains Low until the transmitter is empty.

In Synchronous Data Link Control (SDLC) mode, the $\overline{\text{RTS}}$ pins can be programmed to be deasserted when the closing flag of the message clears the TxD pin, if WR7' bit 2 is 1, WR10 bit 2 is 0, and WR5 bit 1 is 0.

$\overline{\text{SYNCA}}$, $\overline{\text{SYNCB}}$ (Synchronization (Inputs Or Outputs, Active Low))—These pins can act either as inputs, outputs, or as part of the crystal oscillator circuit. In the ASYNCHRONOUS RECEIVE mode (crystal oscillator option not selected), these pins are inputs similar to $\overline{\text{CTS}}$ and $\overline{\text{DCD}}$. In this mode, transition on these lines affect the state of the SYNC/HUNT status bits in Read Register 0 but have no other function.

In EXTERNAL SYNCHRONIZATION mode, with the crystal oscillator not selected, these lines also act as inputs. In this mode, $\overline{\text{SYNC}}$ is driven Low, two Rx clock cycles after the last bit of the $\overline{\text{SYNC}}$ character is received. Character assembly begins on the rising edge of the receive clock immediately preceding the activation of $\overline{\text{SYNC}}$.

In the INTERNAL SYNCHRONIZATION mode (MONOSYNC and BISYNC) with the crystal oscillator not selected, these pins act as outputs. These outputs go Low each time a SYNC pattern is recognized, regardless of character boundaries. In SDLC mode, pins switch from input to output when MONOSYNC, BISYNC, or SDLC is programmed in WR4 and SYNC modes are enabled.

$\overline{\text{DTR}}/\overline{\text{REQA}}$, $\overline{\text{DTR}}/\overline{\text{REQB}}$ (Data Terminal Ready/Request (Output, Active Low))—

These pins can be programmed (WR14 bit 2) to serve either as general-purpose outputs or as DMA Request lines. When programmed for DTR function (WR14 bit 2 is 0), these outputs follow the inverse of the DTR bit of Write Register 5 (WR5 bit 7). When programmed for REQUEST mode these pins serve as DMA Requests for the transmitter.

When used as DMA Request line (WR14 bit 2 is 1), the timing for the deactivation request can be programmed in Write Register 7′ (WR7') bit 4. If this bit is 1, the $\overline{DTR}/\overline{REQ}$ pin is deactivated with the same timing as the $\overline{W}/\overline{REQ}$ pin. If 0, the deactivation timing of $\overline{DTR}/\overline{REQ}$ pin is four clock cycles, the same as in the Z80C30/Z85C30.

$\overline{W}/\overline{REQA}$, $\overline{W}/\overline{REQB}$ (Wait/request (Output, Open-drain When Programmed For $\overline{WAIT}$ Function, Driven High And Low When Programmed For Request Function))—These dual-purpose outputs may be programmed as REQUEST lines for a DMA controller or as WAIT lines to synchronize the CPU to the ESCC data rate. The reset state is WAIT.

RxDA, RxDB (Receive Data (inputs, active High))—These inputs receive serial data at standard Transistor-Transistor Logic (TTL) levels.

$\overline{RTxCA}$, $\overline{RTxCB}$ (Receive/Transmit Clocks (Input, Active Low))—These pins can be programmed to several modes of operation. In each channel, RTxC may supply the following:

- Receive clock and/or the transmit clock
- Clock for the baud rate generator (BRG)
- Clock for the Digital Phase-Locked Loop

These pins can also be programmed for use with the respective $\overline{SYNC}$ pins as a crystal oscillator. The receive clock may be 1, 16, 32, or 64 times the data rate in ASYNCHRONOUS modes.

TxDA, TxDB (Transmit Data (Output, Active High))—These output transmit serial data at standard TTL levels.

$\overline{TRxCA}$, $\overline{TRxCB}$ (Transmit/Receive Clocks (Input or Output, Active Low))—These pins can be programmed in several different modes. When configured as an input, the TRxC may supply the receive clock and/or the transmit clock. When configured as an output, TRxC can echo the clock output of the Digital Phase-Locked Loop, the crystal oscillator, the BRG or the transmit clock.

PCLK (Clock (Input))—This clock is the master ESCC clock used to synchronize internal signals. PCLK is a TTL level signal. PCLK is not required to have any phase relationship with the master system clock.

IEI (Interrupt Enable In (Input, Active High))—IEI is used with IEO to form an interrupt daisy chain when there is more than one interrupt-driven device. A High IEI indicates that no higher priority device has an Interrupt Under Service (IUS) or is requesting an interrupt.

IEO (Interrupt Enable Out (Output, Active High))—IEO is High only if IEI is High and the CPU is not servicing an ESCC interrupt. During an Interrupt Acknowledge Cycle, IEO is also driven Low if the ESCC is requesting an interrupt. IEO can be connected to the next lower priority device's IEI input, and in this case inhibits interrupts from lower priority devices.

INT (Interrupt (Output, Open-Drain, Active Low))—This pin activates when the ESCC requests an interrupt. The $\overline{INT}$ is an open-drain output.

$\overline{INTACK}$ (Interrupt Acknowledge (Input, Active Low))—This pin is a strobe which indicates that an Interrupt Acknowledge Cycle is in progress. During this cycle, the ESCC interrupt daisy chain is resolved. The device can return an interrupt vector that may be encoded with the type of interrupt pending. During the acknowledge cycle, if IEI is High, the ESCC places the interrupt vector on the data bus when $\overline{RD}$ goes active for the Z85230/L, or when $\overline{DS}$ goes active for the Z80230. $\overline{INTACK}$ is latched by the rising edge of PCLK.

Pin Descriptions Exclusive to the Z85230/L

The pin description for pins exclusive to Z85230/L is provided below:

Pins D7–D0 (Data Bus (Bidirectional, tristate))—These pins carry data and commands to and from the Z85230/L.

$\overline{CE}$ (Chip Enable (Input, Active Low))—This pin selects the Z85230/L for a Read or Write operation.

$\overline{RD}$ ((Read (input, Active Low))—This pin indicates a Read operation and, when the Z85230/L is selected, enables the Z85230/L's bus drivers. During the Interrupt Acknowledge cycle, $\overline{RD}$ gates the interrupt vector onto the bus if the Z85230/L is the highest priority device requesting an interrupt.

$\overline{WR}$ (Write (Input, Active Low))—When the Z85230/L is selected, this pin denotes a Write operation, which indicates that the CPU writes command bytes or data to the Z85230/L write registers.

Note: $\overline{WR}$ *and* $\overline{RD}$ *going Low simultaneously is interpreted as a Reset.*

A/$\overline{B}$ (Channel A/Channel B (Input))—This pin selects the channel in which the Read or Write operation occurs. A High selects Channel A and a Low selects Channel B.

D/$\overline{C}$ (Data/Control Select (Input))—This signal defines the type of information transferred to or from the Z85230/L. A High indicates data transfer and a Low indicates a command transfer.

Pin Descriptions Exclusive to the Z80230

The pin description for pins exclusive to Z80230 is provided below:

AD7–AD0 (Address/Data Bus (Bidirectional, Active High, tristate))—These multiplexed lines carry register addresses to the Z80230 as well as data or control information to and from the Z80230.

R/$\overline{W}$ (Read/Write (Input, Read Active High))—This pin specifies if the operation to be performed is a Read or Write operation.

$\overline{\text{CS0}}$ (Chip Select 0 (Input, Active Low))—This pin is latched concurrently with the addresses on A7-A0 and must be Low for the intended bus transaction to occur.

CS1 (Chip Select 1 (Input, Active High))—This second chip select pin must be High before and during the intended bus transaction.

DS (Data Strobe (Input, Active Low))—This pin provides timing for the transfer of data into and out of the Z80230. If $\overline{\text{AS}}$ and $\overline{\text{DS}}$ are both Low, this condition is interpreted as a RESET.

$\overline{\text{AS}}$ (Address Strobe (Input, Active Low))—Addresses on A7-A0 are latched by the rising edge of this signal.

Functional Description

The architecture of the ESCC is described based on its functionality as a:

- Data communications device, which transmits and receives data in a wide variety of protocols
- Microprocessor peripheral, in which the ESCC offers valuable features such as vectored interrupts and DMA support

The details of the communication between the receive and transmit logic of the system bus are displayed in Figure 5 and Figure 6 on page 9. The features and data path for each of the ESCC A and B channels are identical. For more information on SCC/ESCC and ISCC Family of Products, refer to the respective User Manuals available for download from www.zilog.com.

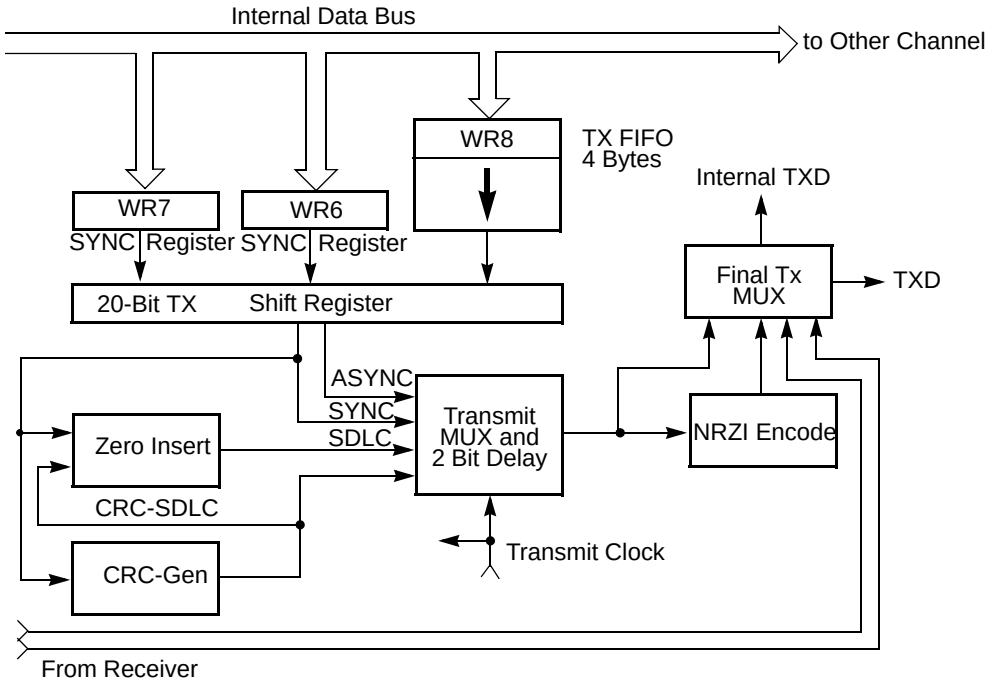


Figure 5. ESCC Transmit Data Path

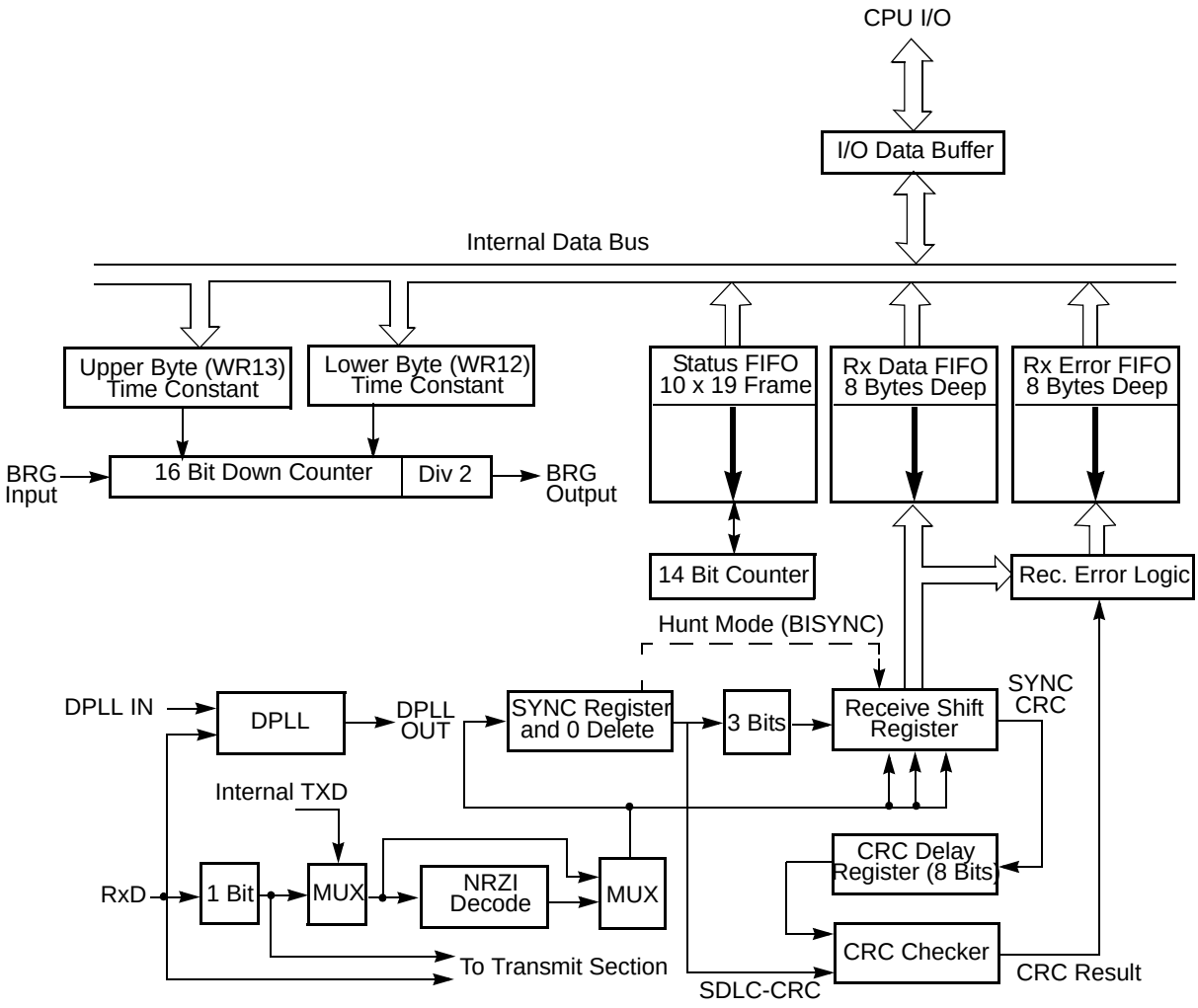


Figure 6. ESCC Receive Data Path

Input/Output Capabilities

System communication to and from the ESCC is accomplished using the ESCC register set. There are 17 Write registers and 16 Read registers. Many of the features on the ESCC are enabled through a new register in the ESCC: Write Register 7 Prime (WR7'). This new register can be accessed if bit 0 or WR15 is set to 1. Table 1 on page 10 lists the Write registers and a brief description of their functions. Table 2 on page 11 lists the Read Registers.

Note: *Throughout this document the Write and Read registers are referenced with the notations WR for Write Register and RR for Read Register. For example:*

WR4A – Write Register 4 for Channel A

RR3 – Read Register 3 for either or both channels

Table 1. ESCC Write Registers

Write Register	Functions
WR0	Command Register; Select Shift Left/Right Mode, Cyclic Redundancy Check (CRC) Initialization, and Resets for Various Modes
WR1	Interrupt Conditions, Wait/DMA Request Control
WR2	Interrupt Vector, Accessed Through Either Channel
WR3	Receive and Miscellaneous Control Parameters
WR4	Transmit and Receive Parameters and Modes
WR5	Transmit Parameters and Controls
WR6	SYNC Character or SDLC Address Field
WR7	SYNC Character or SDLC Flag
WR7’	SDLC Enhancements Enable, Accessible if WR15 bit D0 is 1
WR8	Transmit FIFO, 4-Bytes Deep
WR9	Reset Commands and Master INT Enable, Accessible Through Either Channel
WR10	Miscellaneous Transmit and Receive Controls
WR11	Clock Mode Control
WR12	Lower Byte of BRG Time Constant
WR13	Upper Byte of BRG Time Constant
WR14	Miscellaneous Controls and Digital Phase-Locked Loop (DPLL) Commands
WR15	External Interrupt Control

Table 2. ESCC Read Registers

Register Name	Functions
RR0	Transmit, Receive, and External Status
RR1	Special Receive Condition Status Bits
RR2A	Unmodified Interrupt Vector
RR2B	Modified Interrupt Vector
RR3A	Interrupt Pending Bits
RR4	WR4 Mirror, if WR7' bit D6 equals 1
RR5	WR5 Mirror, if WR7' bit D6 equals 1
RR6	SDLC Frame LSB Byte Count, if WR15 bit D2 equals 1
RR7	SDLC Frame 10 X 19 FIFO Status and MSB Byte Count, if WR15 bit DS equals 1
RR8	Receive Data FIFO, 8 Bits Deep
RR9	WR9 Mirror, if WR7' bit D6 Equals 1
RR10	Miscellaneous Status Bits
RR11	WR11 Mirror, if WR7' bit D6 Equals 1
RR12	Lower Byte of BRG Time Constant
RR13	Upper Byte of BRG Time Constant
RR14	WR14 Mirror, if WR7' bit D6 Equals 1
RR15	WR 15 Mirror, if WR7' bit D6 Equals 1

There are three modes used to move data into and out of the ESCC:

1. POLLING
2. INTERRUPT (vectored and non-vectored)
3. BLOCK TRANSFER

The BLOCK TRANSFER mode can be implemented under CPU or DMA control.

POLLING

When POLLING, data interrupts are disabled, three registers in the ESCC are automatically updated whenever any function is performed. For example, end-of-frame (EOF) in SDLC mode sets a bit in one of these status registers. The purpose of POLLING is for the CPU to periodically read a status register until the register contents indicate the need that data requires transfer. RR0 is the only register that must be read to determine if data needs to be transferred. An alternative to polling RR0 for each channel is to poll the Interrupt

Pending register. Status information for both channels resides in one register. Only one register may be read. Depending on its contents, the CPU performs one of the three operations listed below:

1. Write data
2. Read data
3. Continues processing

Two bits in the register indicate the requirement for data transfer.

INTERRUPT

The ESCC INTERRUPT mode supports vectored and nested interrupts. The fill levels at which the transmit and receive FIFOs interrupt the CPU are programmable, allowing the ESCC requests for data transfer to be tuned to the system interrupt response time.

Nested interrupts are supported with the interrupt acknowledge ($\overline{\text{INTACK}}$) feature of the ESCC. It allows the CPU to acknowledge the occurrence of an interrupt, and re-enable higher priority interrupts. Since an $\overline{\text{INTACK}}$ cycle releases the $\overline{\text{INT}}$ pin from the active state, a higher priority ESCC interrupt or another higher priority device can interrupt the CPU. When an ESCC responds to $\overline{\text{INTACK}}$ signal from the CPU, it can place an interrupt vector on the data bus. This vector is written in WR2 and may be read in RR2. To increase the interrupt response time, the ESCC can modify 3 bits in this vector to indicate status. If the vector is read in Channel A, status is not included. If it is read in Channel B, status is included.

Each of the six sources of interrupts in the ESCC (Transmit, Receive, and External/Status interrupts in both channels) has 3 bits associated with the interrupt source as listed below:

1. Interrupt Pending (IP)
2. Interrupt Under Service (IUS)
3. Interrupt Enable (IE)

If the IE bit is set for a given interrupt source, then that source can request interrupts. However, when the Master Interrupt Enable (MIE) bit in WR9 is reset, no interrupts can be requested. The IE bits are write-only. The other two bits are related to the interrupt priority chain (see Figure 7 on page 13). The ESCC can request an interrupt only when no higher priority device is requesting an interrupt (that is, when IEI is High). If the device in question requests an interrupt, it pulls down $\overline{\text{INT}}$. The CPU then responds with $\overline{\text{INTACK}}$, and the interrupting device places a vector on the data bus.

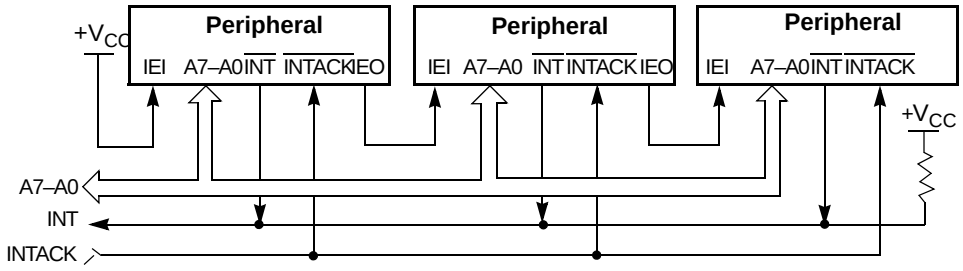


Figure 7. ESCC Interrupt Priority Schedule

The ESCC can also execute an Interrupt Acknowledge cycle using software. Sometimes it is difficult to create the $\overline{\text{INTACK}}$ signal with the necessary timing to acknowledge interrupts and allow the nesting of interrupts. In such cases, interrupts can be acknowledged with a software command to the ESCC. For more information, Z80230/Z85230/L Enhancements on page 22

Interrupt Pending (IP) bits signal a need for interrupt servicing. When an IP bit is 1 and the IEI input is High, the $\overline{\text{INT}}$ output is pulled Low, requesting an interrupt. In the ESCC, if an IE bit is not set, then the IP for that source is never set. The IP bits are read in RR3A.

The Interrupt Under Service (IUS) bits signal that an interrupt request is serviced. If IUS is set to 1, all interrupt sources of low priority in the ESCC and external to the ESCC are prevented from requesting interrupts. The internal interrupt sources are inhibited by the state of the internal daisy chain, while lower priority devices are inhibited by setting IEO Low for subsequent peripherals. An IUS bit is set during an Interrupt Acknowledge cycle if there are no higher priority devices requesting interrupt.

There are three type of interrupts as listed below:

1. Transmit
2. Receive
3. External/Status

Each interrupt type is enabled under program control with Channel A having higher priority than Channel B, and with Transmit, Receive, and External/Status interrupts prioritized in that order within each channel. When the Transmit interrupt is enabled (WR1 bit 1 is 1), the occurrence of the interrupt depends on the state of WR7’ bit 5. If WR7’ bit 5 is 0, the CPU is interrupted when the top byte of the transmit First In First Out (FIFO) becomes empty. If WR7’ bit 5 is 1, the CPU is interrupted when the transmit FIFO becomes completely empty. The transmit interrupt occurs when the data in the exit location of the Transmit FIFO loads into the Transmit Shift Register and the Transmit FIFO becomes completely empty. This condition means that there must be at least one character written to the Tx FIFO for it to become empty.

When the receiver is enabled, the CPU is interrupted in one of the following three methods:

1. Interrupt on First Receive Character or Special Receive Condition
2. Interrupt on All Receive Characters or Special Receive Conditions
3. Interrupt on Special Receive Conditions Only

If WR7' bit 3 is 1, and the Special Receive Condition is selected, the Receive character occurs when there are four bytes available in the Receive FIFO. This is most useful in synchronous applications as the data is in consecutive bytes. Interrupt on First Character or Special Condition and Interrupt on Special Condition Only are typically used with the BLOCK TRANSFER mode. A special Receive Condition consists of one of the following:

- Receiver Overrun
- Framing error in ASYNCHRONOUS mode
- EOF in SDLC mode
- Parity error (optional)

The Special Receive Condition interrupt is different from an ordinary receive character available interrupt only by the status placed in the vector during the Interrupt Acknowledge cycle. In Receive Interrupt on First Character or Special Condition mode, an interrupt occurs from Special Receive Conditions any time after the first receive character interrupt.

The primary function of the External/Status interrupt is to monitor the signal transitions of the $\overline{\text{CTS}}$, $\overline{\text{DCD}}$, and $\overline{\text{SYNC}}$ pins. However, an External/Status interrupt is also caused by any of the following:

- A Transmit Underrun condition
- A zero count in the BRG
- A detection of a Break (ASYNCHRONOUS mode)
- An ABORT (SDLC mode)
- An End Of Poll (EOP) sequence in the data stream (SDLC LOOP mode)

The interrupt caused by the ABORT or EOP sequence has a special feature that allows the ESCC to interrupt when the ABORT or EOP sequence is detected or terminated. This feature facilitates the proper termination of the current message, correct initialization of the next message, and the accurate timing of the ABORT condition by external logic in SDLC mode. SDLC LOOP mode allows secondary stations to recognize the primary station and regain control of the loop during a poll sequence.

CPU/DMA BLOCK TRANSFER

The ESCC provides a BLOCK TRANSFER mode to accommodate CPU/DMA controller. The BLOCK TRANSFER mode uses the $\overline{\text{WAIT}}/\overline{\text{REQUEST}}$ output in conjunction with the $\overline{\text{WAIT}}/\overline{\text{REQUEST}}$ bits in WR1. The $\overline{\text{WAIT}}/\overline{\text{REQUEST}}$ output can be defined as a $\overline{\text{WAIT}}$ line in the CPU BLOCK TRANSFER mode or as a $\overline{\text{REQUEST}}$ line in the DMA BLOCK TRANSFER mode.

To a DMA controller, the ESCC $\overline{\text{REQUEST}}$ output indicates that the ESCC is ready to transfer data to or from memory.

To the CPU, the $\overline{\text{WAIT}}$ line indicates that the ESCC is not ready to transfer data, thereby requesting the CPU to extend the I/O cycle.

The $\overline{\text{DTR}}/\overline{\text{REQUEST}}$ line allows full-duplex operation under DMA control. The ESCC can be programmed to deassert the $\overline{\text{DTR}}/\overline{\text{REQUEST}}$ pin with the same timing as the $\overline{\text{WAIT}}/\overline{\text{REQUEST}}$ pin if WR7' bit 4 is 1.

ESCC Data Communications Capabilities

The ESCC provides two independent full-duplex programmable channels for use in any common ASYNCHRONOUS or SYNCHRONOUS data communication protocols (see Figure 8). The channels have identical features and capabilities.

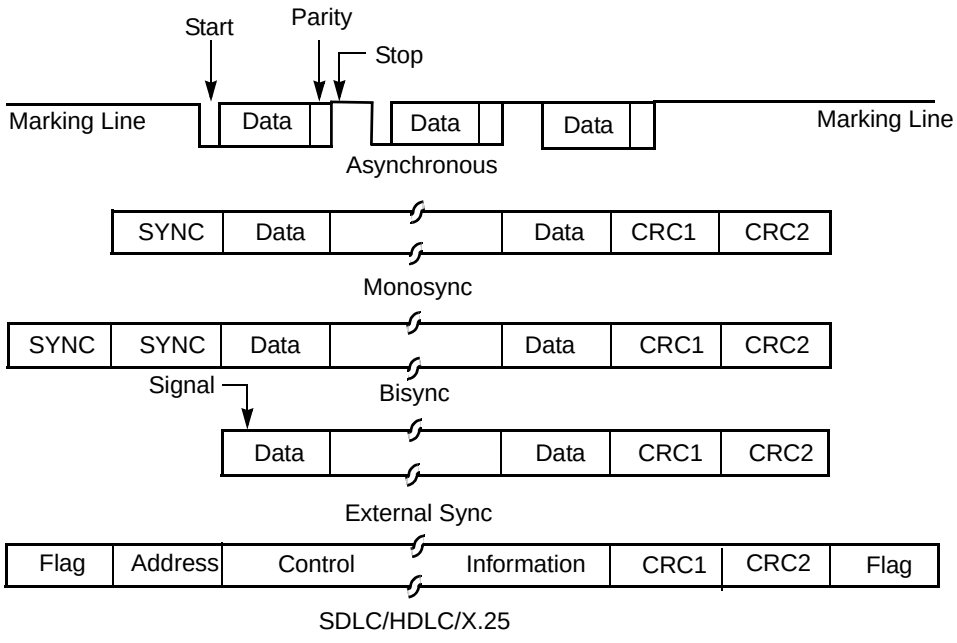


Figure 8. Various ESCC Protocols

ASYNCHRONOUS Mode

The ESCC has significant improvements over the standard Serial Communications Controller (SCC). The addition of the deeper data FIFOs provide greater protection against underruns and overruns as well as more efficient use of bus bandwidth. The deeper data FIFOs are accessible regardless of the protocol used and they need not be enabled. For information on these improvements, see Z80230/Z85230/L Enhancements on page 22

Send and Receive allow 5 to 8 bits per character, plus optional Even or Odd parity. The transmitters can supply 1, 1.5, or 2 stop bits per character and can provide break indication. The receiver break-detection logic interrupts the CPU both at the start and at the end of a received break. Reception is protected from spikes by start-bit validation that delays the signal for a length of time equal to one half the time period required to process 1 bit of data after a Low level is detected on the receive data input (RxDA or RxDB pins). If the Low level does not persist (that is, a transient), the character assembly process does not start.

Framing errors and overrun errors are detected and buffered together with the character at which they occur. Vectored interrupts allow fast servicing of error conditions. Furthermore, a built-in checking process avoids the interpretation of a framing error as a new start bit. A framing error results in the addition of a delay of one half the amount of time required to process 1 bit of data at the point at which the search for the next start bit begins. Transmit and Receive clock can be selected from any of the several sources. In ASYNCHRONOUS mode, the $\overline{\text{SYNC}}$ pin may be programmed as an input with interrupt capability.

SYNCHRONOUS Mode

The ESCC supports both byte-oriented and bit-oriented SYNCHRONOUS communication. SYNCHRONOUS byte-oriented protocols are handled in several modes. They enable character synchronization with a 6- or 8-bit SYNC character (MONOSYNC) or a 12-bit or 16-bit synchronization pattern (BISYNC), or with an external sync signal. Leading sync characters are removed without interrupting the CPU.

5- or 7-bit sync characters are detected from 8- or 16-bit patterns in the ESCC by overlapping the larger pattern across multiple incoming sync characters as displayed in Figure 9.

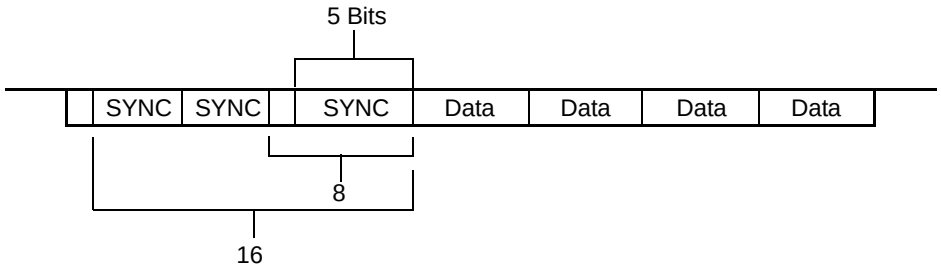


Figure 9. Detecting 5- or 7-Bit Synchronous Characters

CRC checking for SYNCHRONOUS BYTE-ORIENTED mode is delayed by one character time so that the CPU may disable CRC checking on specific characters. This action permits the implementation of protocols such as IBM BISYNC.

Both CRC-16 ($X^{16} + X^{15} + X^2 + 1$) and CRC-CCITT ($X^{16} + X^{12} + X^5 + 1$) error checking polynomials are supported. Either polynomial may be selected in all synchronous modes. You can preset the CRC generator and checker to all 1s or all 0s. The ESCC also provides a feature that automatically transmits CRC data when no other data is available for transmission. This feature enables high-speed transmissions under DMA control, with no need for CPU intervention at the end of a message. When there is no data or CRC to send in the SYNCHRONOUS mode, the transmitter inserts 6-, 8-, 12-, or 16-bit SYNC characters, regardless of the programmed character length.

SDLC Mode

The ESCC supports SYNCHRONOUS bit-oriented protocols, such as SDLC and High-Level Data Link Control (HDLC), by performing automatic flag sending, zero insertion, and CRC generation.

A special command is used to abort a frame which is in transmission. At the end of a message, the ESCC automatically transmits the CRC and trailing flag when the transmitter underruns. The transmitter may also be programmed to send an idle line consisting of continuous flag characters or a steady marking condition.

If a transmit underrun occurs in the middle of a message, an External/Status interrupt warns the CPU of this status change so that an `Abort` command can be issued. The ESCC may also be programmed to send an `Abort` command by itself, in the event of an underrun, relieving the CPU of the task. The last character of a frame may consist of 1- to 8-bits, allowing reception of frames of any length.

The receiver automatically synchronizes on the leading flag of a frame in SDLC or HDLC and provides a synchronization signal on the $\overline{\text{SYNC}}$ pin (an interrupt may also be programmed). The receiver may search for frames addressed by 1-byte or 4-bits within a byte of a user-specified address or for a global broadcast address. Frames not matching either the user-selected address or broadcast address are ignored.

The number of address bytes are extended under software control. To receive data, an interrupt can be selected on the first received character, or on every character, or On Special Condition Only (EOF). The receiver automatically deletes all zeros inserted by the transmitter during character assembly. CRC is also calculated and is automatically checked to validate frame transmission. At the end of transmission, the status of a received frame is available in the status registers. In SDLC mode, the ESCC must be programmed to use the CRC-CCITT polynomial, but the generator and checker may be pre-set to all 1s or all 0s. The CRC data is inverted before transmission and the receiver checks against the bit pattern `0001110100001111`.

NRZ, NRZI, or FM coding may be used in any 1X mode. The parity options available in ASYNCHRONOUS mode are also available in SYNCHRONOUS mode. However, parity checking is not normally used for SDLC because CRC checking is more robust.

SDLC LOOP Mode

The ESCC supports SDLC LOOP mode as well as normal SDLC. In SDLC LOOP mode, a primary controller station manages the message traffic flow on the loop and any number of secondary stations. In SDLC LOOP mode, the ESCC performs the functions of a secondary station. An ESCC operation in regular SDLC mode may act as a controller (see Figure 10). SDLC LOOP mode is selected by setting WR10 bit 1 to 1.

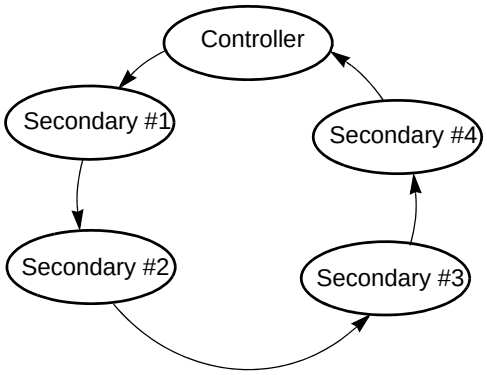


Figure 10. SDLC LOOP mode

A secondary station in an SDLC LOOP mode always monitors the messages sent around the loop and passes these messages to the rest of the loop, retransmitting them with a one-bit time delay. The secondary station places its own message in the loop only at specific times. The controller indicates that the secondary stations can transmit messages by sending a special character, called EOP, around the loop. The EOP character has a bit pattern `11111110`, the same pattern as an `Abort` character in normal HDLC. This bit pattern is unique and easily recognized, because of the zero insertion in the message.

When a secondary station has a message to transmit and recognizes an EOP on the line, it changes the last binary 1 of the EOP to a 0 before transmission. This action changes the EOP into a flag sequence. The secondary station now places its message on the loop and terminates the message with an EOP. Any secondary stations further down the loop with messages to transmit appends their messages to the message of the first secondary station using the same process. Secondary stations without any messages to transmit merely echo the incoming message. All secondary stations are prohibited from placing messages on the loop except upon recognizing an EOP. In SDLC LOOP mode, NRZ, NRZI or FM coding can be used.

SDLC Status FIFO

The ESCC's ability to receive high speed back-to-back SDLC frames is maximized by a 10-bit deep by 19-bit wide status FIFO buffer. When enabled (through WR15 bit 2 is 1), the storage area enables DMA to continue data transfer into the memory, so that the CPU examines the message later. For each SDLC frame, 14 counter bits and 5 Status/Error bits are stored. The byte count and status bits are accessed through Read Registers, RR6, and RR7. RR6 and RR7 are only used when the SDLC FIFO buffer is enabled. The 10 x 19 status FIFO buffer is separate from the 8-byte receive data FIFO buffer.

Baud Rate Generator

Each channel in the ESCC contains a programmable BRG. Each generator consists of two 8-bit registers that form a 16-bit time constant, a 16-bit down counter, and a flip-flop on the output, producing a square wave. At start-up, the flip-flop at the output is set High, the value in the time constant register is loaded into the counter, and the count down begins. When the BRG reaches zero, the output toggles, the counter is reloaded with the time constant, and the process repeats. The time constant can be changed at any time, but the new value does not take effect until the counter is loaded again.

The output of the BRG may be used as the Transmit clock, the Receive clock, or both. The output can also drive the DPLL. For more information, see Digital Phase-Locked Loop.

If the receive clock or the transmit clock is not programmed to come from the TRxC pin, the output of the BRG may be echoed out by the TRxC pin.

The following formula relates the time constant to the baud rate. PCLK or $\overline{\text{RTxC}}$ is the clock input to the BRG. The clock mode is 1, 16, 32, or 64, as selected in WR 4 bits 6 and 7.

$$\text{Time Constant} = \frac{\text{PCLK or RTxC Frequency}}{2(\text{Baud Rate})(\text{Clock Mode})} - 2$$

Digital Phase-Locked Loop

The ESCC contains a DPLL to recover clock information from a data stream with NRZI or FM encoding. The DPLL is driven by a clock that is nominally 32 (NRZI) or 16 (FM) times the data rate. The DPLL uses this clock, along with the data stream, to construct a clock for the data. This clock is then used as the ESCC receive clock, the transmit clock, or both. When the DPLL is selected as the transmit clock source, it provides a jitter-free clock output. The clock output is the DPLL input frequency divided by the appropriate divisor for the selected encoding technique.

For NRZI encoding, the DPLL counts the 32x clock to create nominal bit times. As the 32x clock is counted, the DPLL searches the incoming data stream for edges (either 1 to 0 or 0 to 1). When a transition is detected the DPLL makes a count adjustment (during the next counting cycle), producing a terminal count closer to the center of the bit cell.

For FM encoding, the DPLL counts from 0 to 32, but with a cycle corresponding to two bit times. When the DPLL is locked, the clock edges in the data stream occurs between counts 15 and 16 and between counts 31 and 0. The DPLL looks for edges only during a time centered on the 15 to 16 counting transition.

The 32x clock for the DPLL can be programmed to come from either the RTxC input or the output of the BRG. The DPLL output is programmed to be echoed out the ESCC by the TRxC pin (if this pin is not being used as an input).

Data Encoding

Data encoding allows the transmission of clock and data information over the same medium. This capability saves the need to transmit clock and data over separate medium as is normally required tor synchronous data. The ESCC provides four different data encoding methods, selected by bits 6 and 5 in WR10. Examples of these 4 encoding methods is displayed in Figure 11. Any encoding method is used in any X1 mode in the ESCC, ASYNCHRONOUS or SYNCHRONOUS. The data encoding selected is active even if the transmitter or receiver is idling or disabled.

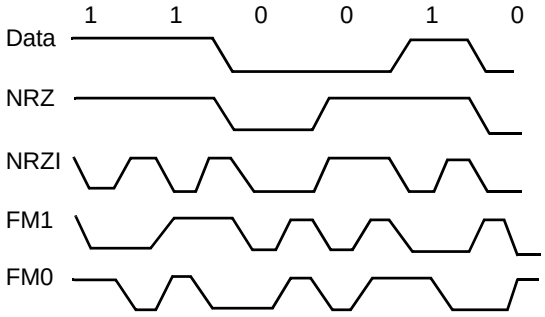


Figure 11. Data Encoding Methods

Table 3 lists the four encoding methods, their levels, and values.

Table 3. Data Encoding Descriptions

Code Type	Level	Value
NRZ	High Low	1 0
NRZI	No Change Change	1 0

Table 3. Data Encoding Descriptions (Continued)

Code Type	Level	Value
FM1 (biphase mark)	Additional Transition at the Center of the Bit Cell No Additional Transition at the Center of the Bit Cell	1 0
FM0 (biphase space)	A transition occurs at the beginning of every bit call. A 0 is represented by an additional transition at the center of the bit cell. A 1 is represented by no additional transition at the center of the bit cell.	0 1

In addition to the four methods, ESCC can be used to decode Manchester (biphase level) data using DPLL in the FM mode and programming the receiver for NRZ data. Manchester encoding always produces a transition at the center of the bit cell. If the transition is 0 to 1, the bit is a 0. If the transition is 1 to 0, the bit is a 1.

Auto Echo and Local Loopback

The ESCC is capable of automatically echoing everything it receives. This feature is useful mainly in ASYNCHRONOUS modes, but works in SYNCHRONOUS and SDLC modes as well. AUTO ECHO mode (TxD is RxD) is used with NRZI or FM encoding with an additional delay because the data stream is not decoded before retransmission. In AUTO ECHO mode, the $\overline{\text{CTS}}$ input is ignored as a transmitter enable, (although transitions for this input can cause interrupts if programmed to do so). In this mode, the transmitter is actually bypassed and the programmer is responsible for disabling transmitter interrupts and $\overline{\text{Wait}}/\overline{\text{Request}}$ on transmit.

The ESCC is also capable of LOCAL LOOPBACK. In this mode the internal transmit data is tied to the internal receive data and RxD is ignored. The $\overline{\text{CTS}}$ and $\overline{\text{DCD}}$ inputs are also ignored as transmit and receive enables. However, transitions on these inputs can cause interrupts. LOCAL LOOPBACK works in ASYNCHRONOUS, SYNCHRONOUS, and SDLC modes with NRZ, NRZI, or FM coding of the data stream.

Z80230/Z85230/L Enhancements

A detailed description of the enhancements to the Z80230/Z85230/L ESCC that differentiate it from the standard SCC is provided below:

4-Byte Transmit FIFO Buffer

The ESCC has a 4-byte transmit buffer with programmable interrupt and DMA request levels. It is not necessary to enable the FIFO buffer as it is always available. You can set the Transmit Buffer Empty (TBE) interrupt and DMA Request on Transmit command to be generated either when the top byte of transmit FIFO is empty or only when the FIFO is completely empty. A hardware or channel reset clears the transmit shift register, flushes the transmit FIFO, and sets WR7' bit 5 to 1.

If the transmitter generates the interrupt or DMA request for data when the top byte of the FIFO is empty (WR7' bit 5 is 0), the system allows for a long response time to the data request without underflowing. The interrupt service routine (ISR) writes 1byte and then tests RR0 bit 2. The DMA Request on Transmit in this mode is set to 0 after each data Write (that is, TBE), RR0 bit 2, is set to 1 when the top byte of the FIFO is empty. WR7' bit 5 resets to 1.

In applications for which the interrupt frequency is important, the transmit ISR can be optimized by programming the ESCC to generate the TBE interrupt only when the FIFO is completely empty (WR7' bit 5 is 1) and, writing 4 bytes to fill the FIFO. When WR7' bit 5 is 1, only one DMA request is generated, filling the bottom of the FIFO. However, this may be advantageous for applications where the possible reassertion of the DMA request is not required. The TBE status bit, RR0 bit 2, is set to 1 when the top byte of the FIFO is empty. WR7' bit 5 is set to1 after a hardware or channel reset.

8-Byte Receive FIFO

The ESCC has an 8-byte receive FIFO with programmable interrupt levels. It is not necessary to enable the 8-byte FIFO as it is always available. A hardware or channel reset clears the Receive Shift register and flushes the Receive FIFO. The Receive Character Available interrupt is generated as selected by WR7' bit 3. The Receive Character Available bit, RR0 bit 0 is set to 1 when at least one byte is available at the top of the FIFO (independent of WR7' bit 3).

A DMA Request on Receive, if enabled, is generated whenever 1 byte is available in the receive FIFO independent of WR7' bit 3. If more than 1 byte is available in the FIFO, the $\overline{\text{Wait}}/\overline{\text{Request}}$ pin becomes inactive and becomes active when the FIFO is emptied.

By resetting WR7' bit 3 to 0, applications which have a long latency to interrupts can generate the request to read data from the FIFO when one byte is available. The application can then test the Receive Character Available bit to determine if more data is available.

By setting WR7' bit 3 to 0, the ESCC can issue an interrupt when the receive FIFO is half full (4 bytes available), allowing the frequency of interrupts to be reduced. If WR7' bit 3 is 1, the Receive Character Available interrupt is generated when there are 4 bytes available. If the ISR reads 4 bytes during each routine, the frequency of interrupts is reduced.

If WR7' bit 3 is 1 and Receive Interrupt on All Characters and Special Conditions is enabled, the receive character available interrupt is generated when four characters are available. However, when a character is detected to have a special condition, an interrupt is generated when the character is loaded into the top four bytes of the FIFO. Therefore, the Special Condition ISR must be RR1 before reading the data to determine which byte has the special condition.

Write Register 7 PRIME (WR7')

A new register, WR7', has been added to the ESCC to enable the programming of six new features. The format of this register is listed in Table 4.

Table 4. Write Register 7 Prime (WR7')

Bit	7	6	5	4	3	2	1	0
R/W	W	W	W	/W	W	W	W	W
Reset	0	0	0	0	0	0	0	0

Note: R = Read W = Write X = Indeterminate

Bit Position	R/W	Value	Description
7	W	0	Reserved, must be 0
6	W		Extended Read Enable
5	W		Transmit FIFO Int Level
4	W		$\overline{\text{DTR}}/\overline{\text{REQ}}$ Timing Mode
3	W		Receive FIFO Int Level
2	W		Auto RTS Deactivation
1	W		Auto EOM Reset
0	W		Auto Transmit Flag

WR7' is written by first setting Bit 0 of Write Register 15 (WR15 bit 0) to 1 and then accessing WR7. All write commands to register 7 are to WR7' while WR15 bit 0 is set to

1. WR15 bit 0 must be reset to 0 to address the SYNC character in register WR7. If bit 6 of WR7' is set to 1, then WR7' can be read by performing a read cycle to RR14. The WR7' features remain enabled until specifically disabled or by a hardware or software reset. Bit 5 is set to 1 and all other bits are reset to 0 after a reset.

For applications which use either the Zilog Z8X30SCC or Z80230, these two device types can be identified in software with the following test:

1. Write `01H` to Write Register 15
2. Read Register 15

If bit 0 is set to 0, the device is Z8X30SCC. If bit 0 is set to 1, it is a Z80C30. If the device is Z8XC30, a write to WR15 is required before proceeding. If the device is Z80230, all writes to address 7 are to WR7' until WR15 is set to 0.

The WR7 register bits are described below:

Bit 7 (Not used)

This bit must always be 0.

Bit 6 (Extended Read Enable)

Setting this bit to 1 enables WR3, WR4, WR5, WR7' and WR10 to be read by issuing a READ command for RR9 (WR3) RR4, RR5, RR14 (WR7') and RR11 (WR10), respectively.

Bit 5 (Transmit FIFO Interrupt Level)

If this bit is set to 1, the TBE interrupt is generated when the transmit FIFO is completely empty. If this bit is set to 0, the TBE interrupt is generated when the top byte of the transmit FIFO is empty. This bit is set following a hardware or channel reset.

In DMA REQUEST ON TRANSMIT mode, when using either the $\overline{W}/\overline{REQ}$ or $\overline{DTR}/\overline{REQ}$ pins, the request is asserted when the Tx FIFO is completely empty if WR7' bit 5 is set to 1. The request is asserted when the top byte of the FIFO is empty if bit 5 is reset.

Bit 4 ($\overline{DTR}/\overline{REQ}$ Timing)

If this bit is set to 1 and the $\overline{DTR}/\overline{REQ}$ pin is used for REQUEST mode (WR14 bit 2 is 1), the deactivation of the $\overline{DTR}/\overline{REQ}$ pin is identical to the $\overline{W}/\overline{REQ}$ pin as displayed in Figure 12 on page 25. If this bit is reset, the deactivation time is 4TcPc.

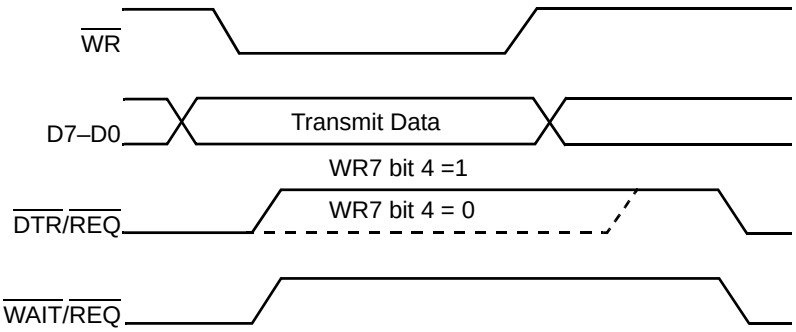


Figure 12. DMA Request on Transmit Deactivation Timing

Bit 3 (Receive FIFO Interrupt Level)

This bit sets the interrupt level of the receive FIFO. If this bit is set to 1, the receive data available bit is asserted when the receive FIFO is half full (4 bytes available). If this bit is reset to 0, the Receive Data Available interrupt is requested when all bytes are set. For more information, see 8-Byte Receive FIFO on page 22.

Bit 2 (Automatic $\overline{\text{RTS}}$ Pin Deassertion)

This bit controls the timing of the deassertion of the $\overline{\text{RTS}}$ pin in SDLC mode. If this bit is 1 and WR5 bit 1 is set to 0 during the transmission of an SDLC frame, the deassertion of the $\overline{\text{RTS}}$ pin is delayed until the last bit of the closing flag clears the TxD pin. The $\overline{\text{RTS}}$ pin is pulled High after the rising edge of the transmit clock cycle from the last bit of the closing flag. This action implies that the ESCC must be programmed for Flag on Underrun (WR10 bit 2 is 0) for the $\overline{\text{RTS}}$ pin to deassert at the end of the frame. This feature works independently of the programmed Transmitter Idle state. In SYNCHRONOUS mode other than SDLC, the $\overline{\text{RTS}}$ pin immediately follows the state programmed into WR5 bit 1. When WR7' bit 2 is set to 0, the $\overline{\text{RTS}}$ follows the state of WR5 bit 1.

Bit 1 (Automatic EOM Reset)

If this bit is 1, the ESCC automatically resets the Tx Underrun/EOM latch and presets the transmit CRC generator to its programmed preset state (per values set in WR5 bit 2 and WR10 bit 7). Therefore, it is not necessary to issue the Reset Tx Underrun/EOM Latch command when this feature is enabled.

Bit 0 (Automatic Tx SDLC Flag)

If this bit is 1, the ESCC automatically transmits an SDLC flag before transmitting data. This action removes the requirement to reset the Mark Idle bit (WR10 bit 3) before writing data to the transmitter.

Historically, the SCC latched the databus on the falling edge of $\overline{WR}$. However, as many CPUs do not guarantee that the databus is valid when the $\overline{WR}$ pin goes Low, Zilog modified the databus timing to allow a maximum delay of 20 nS from the $\overline{WR}$ signal going active Low to the latching of the databus.

CRC Reception in SDLC Mode

In SDLC mode, the entire CRC is clocked into the receive FIFO. The ESCC completes clocking in the CRC to allow it to be retransmitted or manipulated software. In the SCC, when the closing flag is recognized, the contents of the receive shift register are immediately transferred to the receive FIFO, resulting in the loss of the last two bits of the CRC. In the ESCC, it is not necessary to program this feature. When the closing flag is detected, the last 2 bits of the CRC are transferred into the receive FIFO. In all other SYNCHRONOUS mode, the ESCC does not clock in the last 2 CRC bits (same as the SCC).

TxD Forced High in SDLC with NRZI Encoding When Marking Idle

When the ESCC is programmed for SDLC mode with NRZI data encoding and Mark Idle (WR10 bit 6 is 0, bit 5 is 1, bit 3 is 1), the TxD pin is automatically forced High when the transmitter enters the Mark Idle state. There are several different ways for the transmitter to enter the Idle state. In each of the following cases the TxD pin is forced High when the Mark Idle condition is reached:

- Data, CRC, flag, and Idle
- Data, flag, and Idle
- Data, abort (on underrun), and Idle
- Data, abort (command), and Idle
- Idle flag and command to Idle Mark

The Force High feature is disabled when the Mark Idle bit is set to 0.

This feature is used in combination with the automatic SDLC opening flag transmission feature, WR7’ bit 0 is 1, to assure that data packets are formatted correctly. In this case, the CPU is not required to issue any commands. If WR7’ bit 0 is 0, as on the SCC, the Mark Idle bit (WR10 bit 3), is set to 1, to enable flag transmission before an SDLC packet transmits.

Improved Transmit Interrupt Handling

The ESCC latches the TBE interrupt because the CRC is loaded into the Transmit Shift register even if the TBE interrupt, due at the last data byte, has not been reset. The end of a

synchronous frame is guaranteed to generate two TBE interrupts even if a Reset Transmit Buffer Interrupt command for the data created interrupt is issued after the CRC interrupt occurs (Time A in Figure 13). Two `Reset TBE` commands are required. The TxIP latches if the EOM latch resets before the end of the frame.

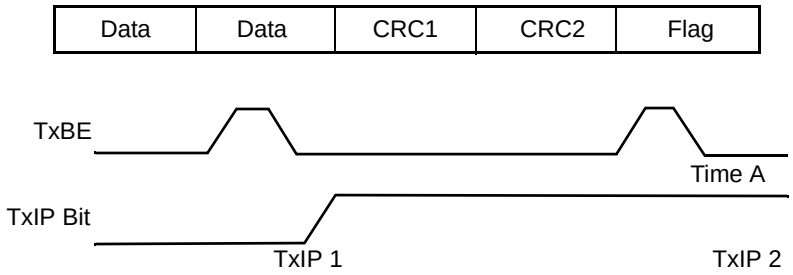


Figure 13. TxIP Latching

DPLL Counter Tx Clock Source

When the DPLL is selected as the transmit clock source, the DPLL counter output is the DPLL source clock divided by the appropriate divisor for the programmed data encoding format. In FM mode (FM0 or FM1), the DPLL counter output signal is the input frequency divided by 16.

In NRZI mode, the DPLL counter output signal is the input clock cycle divided by 32. This feature provides a jitter-free output signal that replaces the DPLL transmit clock output as the transmit clock source. This action has no effect on the use of the DPLL as the receive clock source (see Figure 14).

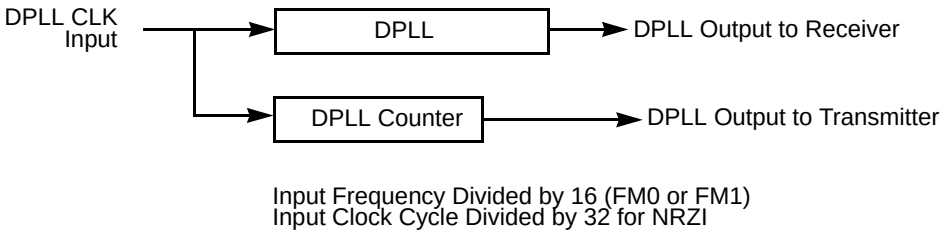


Figure 14. DPLL Outputs

Read Register 0 Status Latched During Read Cycle

The contents of Read Register 0, RR0 is latched during a Read operation. The ESCC prevents the contents of RR0 from changing during a Read operation. But, the SCC allows the status of RR0 to change while reading the register and may require reading RR0 twice. The contents of RR0 is updated after the rising edge of $\overline{RD}$ signal.

Software Interrupt Acknowledge

The Z80230/Z85230/L interrupt acknowledge cycle can be initiated using software. If Write Register 9 (WR9 bit 5 is 1), Read Register 2 (RR2) results in an interrupt $\overline{\text{INTACK}}$ cycle, a software acknowledgment causes the $\overline{\text{INT}}$ pin to go High. The IEO pin goes Low. The Interrupt Under Service (IUS) latch is set to the highest priority pending interrupt.

When a hardware $\overline{\text{INTACK}}$ signal is desired, a software acknowledge cycle requires that a Reset Highest IUS command be issued in the ISR. If RR2 is read from Channel A, the unmodified vector is returned. If RR2 is read from Channel B, then the vector is modified to indicate the source of the interrupt. The Vector Includes Status (VIS) and No Vector (NV) bits in WR9 are ignored when WR9 bit 5 is set to 1.

If the $\overline{\text{INTACK}}$ and IEI pins are not used, they are pulled up to V_{CC} through a resistor (2.2 k?, typical).

Fast SDLC Transmit Data Interrupt Response

To facilitate the transmission of back-to-back SDLC frames with a single shared flag between frames, the ESCC allows data for a second frame to be written to the transmit FIFO after the Tx Underrun/EOM interrupt occurs. This feature allows application software more time to write the data to the transmitter while allowing the current frame to conclude with CRC and flag. The SCC required that data not be written to the transmitter until a TBE interrupt is generated after the CRC completed transmission.

If data is written to the transmit FIFO after the Transmit Underrun/EOM interrupt is issued but before the TBE interrupt is issued, the Automatic EOM Reset function is enabled (WR7’ bit 1 is 1). Consequently, the commands Reset Tx/Underrun EOM Latch and Reset Tx CRC Generator must never be used.

SDLC FIFO Frame Status Enhancement

When used with a DMA controller, the ESCC SDLC Frame Status FIFO enhancement maximizes the ESCC’s ability to receive high-speed, back-to-back SDLC messages. It minimizes frame overruns due to CPU latencies in responding to interrupts. The feature (displayed in Figure 15 on page 29) includes:

- 10-bit deep by 19-bit wide status FIFO
- 14-bit receive byte counter
- Control logic

The 10 x 19 bits status FIFO is separate from the 8-byte receive data FIFO.

When the enhancement is enabled, the status in Read Register 1 (RR1) and byte count for the SDLC frame are stored in the 10- x 19-bit status FIFO. This action allows the DMA

controller to transfer the next frame into memory while the CPU verifies the previously received frame.

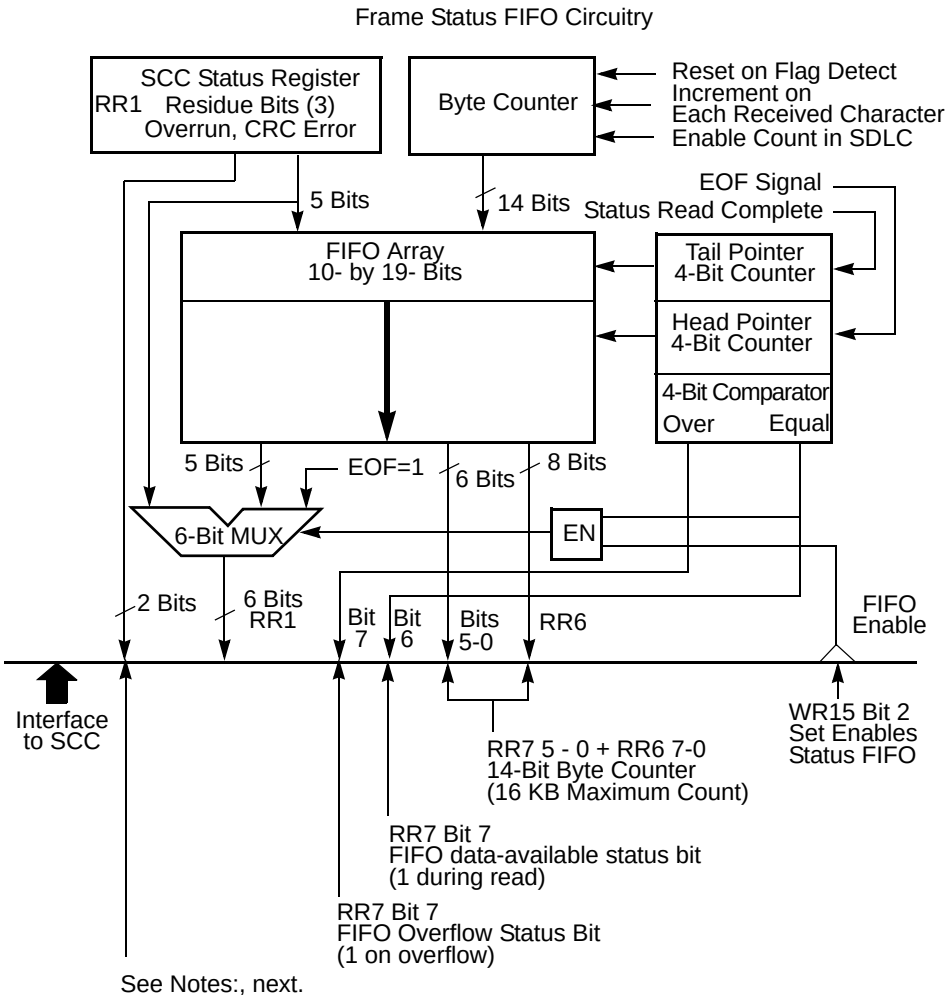


Figure 15. SDLC Frame Status FIFO

Notes:

1. *All Sent bypasses MUX and equals contents of SCC Status Register.*
2. *Parity bits bypass MUX and equals contents of SCC Status Register.*
3. *EOF is set to 1 whenever reading from the FIFO.*

Summarizing the operation: Data is received, assembled, and loaded into the 8-byte FIFO before transferring to memory by the DMA controller.

When a flag is received at the end of an SDLC frame, the frame byte count from the 14-bit counter and 5 status bits are loaded into the status FIFO for verification by the CPU. The CRC checker is automatically reset in preparation for the next frame, which starts immediately.

Because the byte count and status are saved for each frame, the message integrity can be verified at a later time. Status information for up to ten frames is stored before a status FIFO overrun occurs.

If a frame is terminated with an `Abort` command, the byte count and status is loaded to the status FIFO and the counter is reset for the next frame.

FIFO Enable/Disable

This FIFO buffer is enabled when WR15 bit 2 is 1 and the ESCC is in the SDLC/HDLC mode. Otherwise, the status register contents bypass the FIFO and transfer directly to the bus interface (the FIFO pointer logic is reset either when disabled or by a channel or power-on reset). When the FIFO mode is disabled, the ESCC is downward-compatible with the NMOS Z8030/Z8530. The FIFO mode is disabled on power-up (WR15 bit 2 set to 0 on reset). The effects of backward compatibility on the register set are that RR4 is an image of RR0, RR5 is an image of RR1, RR6 is an image of RR2, and RR7 is an image of RR3. For information on the added registers, see Read Registers on page 53. The status of the FIFO Enable signal is read at RR15 bit 2. If the FIFO is enabled, the bit is set to 1; otherwise it is reset to 0.

FIFO Read Operation

When WR15 bit 2 is 1 and the FIFO is not empty, the next read status register RR1 or the additional registers RR7 and RR6, reads the FIFO. Reading status register RR1 causes one location of the FIFO to empty, so status is read after reading the byte count; otherwise the count is incorrect. Before the FIFO underflows, it is disabled. In this case, the multiplexer is switched to allow status to read directly from the status register. In this state, reads from RR7 and RR6 are undefined bit 6 of RR7 (FIFO data available) status data is coming from the FIFO or directly from the status register, because it is set to 1 whenever the FIFO is not empty.

Since all status bits are not stored in the FIFO, the All Sent, Parity, and EOF bits bypass the FIFO. The status bits sent through the FIFO are the three Residue Bits, Overrun, and CRC Error.

The correct sequence for polling the byte count and FIFO logic is RR7, RR6, then RR1 (reading RR6 is optional). Additional logic prevents the FIFO from emptying by multiple reads from RR1. The read from RR7 latches the FIFO empty/full status bit (bit 6) and steers the status multiplexer to read the ESCC megacell instead of the status FIFO

(because the status FIFO is empty). The read from RR1 allows an entry to be read from the FIFO (if the FIFO is empty, the logic prevents a FIFO underflow condition).

FIFO Write Operation

When the end of an SDLC frame is received and the Status FIFO is enabled, the contents of the status and byte-count registers load into the FIFO. The EOF signal increments the FIFO. If the FIFO overflows, the RR7 bit 7 (FIFO overflow) is set, indicating the overflow. This bit and the FIFO control logic is reset by disabling and re-enabling the FIFO control bit (WR15 bit 2). For details about FIFO control timing during an SDLC frame, see Figure 16.

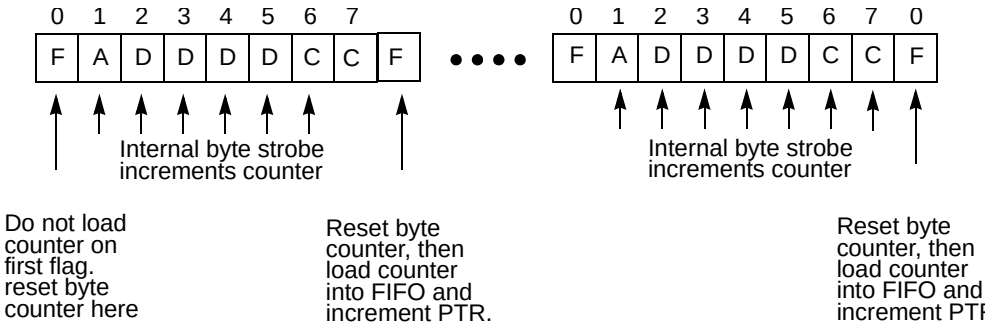


Figure 16. SDLC Byte Counting Detail

SDLC Status FIFO Anti-Lock Feature

When the Frame Status FIFO is enabled and the ESCC is programmed for Special Receive Condition Only (WR1 bit 4 = bit 3=1), the data FIFO is not locked when a character with EOF status is read.When EOF status is at the top of the FIFO, an interrupt with a vector for receive data is generated. The command `Reset Highest IUS` must be issued at the end of the ISR regardless of whether an Interrupt Acknowledge cycle was executed (hardware or software).

This action allows the DMA to complete the transfer of the received frame to memory, then interrupt the CPU that a frame was completed, without locking the FIFO. Because in the RECEIVE INTERRUPT ON SPECIAL CONDITION ONLY mode the interrupt vector for receive data is not used, it indicates that the last byte of a frame has been read from the receive FIFO. Reading the frame status (CRC, byte count and other status stored in the status FIFO) determines that EOF is not required.

When a character with a special receive condition other than EOF is received (receiver overrun or parity), a special receive condition interrupt is generated after the character is read from the FIFO and the receive FIFO is locked until the `Error Reset` command is issued.

Programming

The ESCC contains write registers in each channel that are programmed by the system separately to configure the function of each channel.

In the Z85230/L ESCC, the data FIFOs are directly accessible by selecting a High on the D/$\overline{C}$ pin. Except WR0 and RR0, programming the write registers requires two write operations and reading a read register requires a write and a read operation. The first Write is to WR0 which contains bits that point to the selected register. If the next operation is a Write the selected write register is written. If the next operation is a read, the selected read register is read. The pointer bits are automatically cleared after the second operation so the next read or write comes from RR0 or goes to WR0. It is not necessary to write 00 to WR0 to access WR0 or RR0.

For the Z80230 ESCC, the registers are directly addressable. A command issued to WR0B determines how the ESCC decodes the address placed on the address/data bus at the beginning of a Read or Write cycle. In Shift Right mode the channel select A/$\overline{B}$ is taken from AD0 and the state of AD5 is ignored. In Shift Left mode, the channel select A/$\overline{B}$ is taken from AD5 and the state of AD0 is ignored. AD7 and AD6 are always ignored as address bits and the register address itself occupies AD4–AD1.

Initializing

The software first issues a series of commands to initialize the basic mode of operation. These commands are followed by other commands to qualify conditions within the selected mode. For example, in the ASYNCHRONOUS mode, character length, clock rate, number of stop bits, and even and odd parity is set first. Next, the INTERRUPT mode is set. Finally, the receiver and transmitter are enabled.

Write Registers

The ESCC contains 16 write registers (17 counting the transmit buffer) in each channel. These write registers are programmed to configure the function of the channel. There are two registers (WR2 and WR9) shared by the two channels, which can be accessed through either of them. WR2 contains the interrupt vector for both channels. WR9 contains the interrupt control bits and reset commands. Register WR7’ can be written to if WR15 bit 0 is 1.

Z80X20 Register Access

The Z80230 registers are addressed using the address on AD7–AD0 which are latched by the rising edge of $\overline{AS}$. The Shift Right/Shift Left bit in the Channel B WR0 controls which

bits are decoded to form the register address. This bit is placed in this register to simplify programming when the current state of the Shift right/Shift Left bit is not known.

A hardware reset forces SHIFT LEFT mode where the address is decoded from AD5–AD0. In SHIFT RIGHT mode, the address is decoded from AD4–AD0. The Shift Right/Shift Left bit is written using a command to make the software writing to WR0 independent of the state of the Shift Right/Shift Left bit.

While in the SHIFT LEFT mode, the register address is placed on AD4–AD0 and the Channel Select bit A/$\overline{B}$, is decoded from AD5. In SHIFT RIGHT mode, the register address is again placed on AD4–AD1 but the Channel Select A/$\overline{B}$ is decoded from AD0.

Since Z80230 does not contain 16 read registers, the decoding of the read registers is not complete; this state is listed in Table 4 on page 23 and Table 5 by parentheses around the register name. These addresses may also be used to access the read registers. The Z80230 contains only one WR2 and WR9; these registers may be written from either channel.

SHIFT LEFT mode is used when Channel A and B are programmed differently. Using SHIFT LEFT mode allows the software to sequence through the registers of one channel at a time. The SHIFT RIGHT mode is used when the channels are programmed the same. By incrementing the address, you can program the same data value into both Channel A and Channel B registers.

Table 5 lists details of the Z80X30 Register Map in SHIFT LEFT Mode.

Table 5. Z80230 Register Map (Shift Left Mode)

AD5	AD4	AD3	AD2	AD1	Write	80230 WR15 D2=0	80230 WR15 D2=1	80230 WR15 D2=1 WR7' D6=1
0	0	0	0	0	WR08	RR0B	RR0B	RR08
0	0	0	0	1	WR1B	RR1B	RR1B	RR1B
0	0	0	1	0	WR2	RR2B	RR2B	RR2B
0	0	0	1	1	WR3B	RR3B	RR3B	RR3B
0	0	1	0	0	WR4B	(RR0B)	(RR0B)	(WR4B)
0	0	1	0	1	WR5B	(RR1B)	(RR1B)	(WR5B)
0	0	1	1	0	WR6B	RR6B	(RR2B)	RR6B
0	0	1	1	1	WR7B	RR7B	(RR3B)	RR7B
0	1	0	0	0	WR8B	RR8B	RR8B	RR8B
0	1	0	0	1	WR9	(RR13B)	(RR13B)	(WR3B)
0	1	0	1	0	WR10B	RR10B	RR10B	RR10B
0	1	0	1	1	WR11B	(RR15B)	(RR15B)	(WR10B)

Table 5. Z80230 Register Map (Shift Left Mode) (Continued)

AD5	AD4	AD3	AD2	AD1	Write	80230 WR15 D2=0	80230 WR15 D2=1	80230 WR15 D2=1 WR7' D6=1
0	1	1	0	0	WR12B	RR12B	RR12B	RR12B
0	1	1	0	1	WR13B	RR13B	RR13B	RR13B
0	1	1	1	0	WR14B	RR14B	RR14B	(WR7'B)
0	1	1	1	1	WR15B	RR15B	RR15B	RR15B
1	0	0	0	0	WR0A	RR0A	RR0A	RR0A
1	0	0	0	1	WR1A	RR1A	RR1A	RR1A
1	0	0	1	0	WR2	RR2A	RR2A	RR2A
1	0	0	1	1	WR3A	RR3A	RR3A	RR3A
1	0	1	0	0	WR4A	(RR0A)	(RR0A)	(WR4A)
1	0	1	0	1	WR5A	(RR1A)	(RR1A)	(WR5A)
1	0	1	1	0	WR6A	(RR2A)	RR6A	RR6A
1	0	1	1	1	WR7A	(RR3A)	RR7A	RR7A
1	1	0	0	0	WR8A	RR8A	RR8A	RR8A
1	1	0	0	1	WR9	(RR13A)	(RR13A)	(WR3A)
1	1	0	1	0	WR10A	RR10A	RR10A	RR10A
1	1	0	1	1	WR11A	(RR15A)	(RR15A)	(WR10A)
1	1	1	0	0	WR12A	RR12A	RR12A	RR12A
1	1	1	0	1	WR13A	RR13A	RR13A	RR13A
1	1	1	1	0	WR14A	RR14A	RR14A	(WR7'A)
1	1	1	1	1	WR15A	RR15A	RR15A	RR15A

Notes:
1. The register names in ( ) are the values read out from that register location.
2. WR15 bit D2 enables status FIFO function (not available on NMOS).
3. WR7' bit D6 enables extend read function (only on ESCC).

Table 6 lists details of the Z80X30 Register Map in SHIFT RIGHT mode.

Table 6. Z80X30 Register Map (Shift Right Mode)

AD4	AD3	AD2	AD1	AD0	Write	80230 WR15 D2=0	80230 WR15 D2=1	80230 WR15 D2=1 WR7' D6=1
0	0	0	0	0	WR08	RR0B	RR0B	RR0B
0	0	0	0	1	WR0A	RR0A	RR0A	RR0A
0	0	0	1	0	WR1B	RR1B	RR1B	RR1B
0	0	0	1	1	WR1A	RR1A	RR1A	RR1A
0	0	1	0	0	WR2	RR2B	RR2B	RR2B
0	0	1	0	1	WR2	RR2A	RR2A	RR2A
0	0	1	1	0	WR3B	RR3B	RR3B	RR3B
0	0	1	1	1	WR3A	RR3A	RR3A	RR3A
0	1	0	0	0	WR4B	(RR0B)	(RR0B)	(WR4B)
0	1	0	0	1	WR4A	(RR0A)	(RR0A)	(WR4A)
0	1	0	1	0	WR5B	(RR1B)	(RR1B)	(WR5B)
0	1	0	1	1	WR5A	(RR1A)	(RR1A))	(WR5A)
0	1	1	0	0	WR6B	(RR2B)	RR12B	RR12B
0	1	1	0	1	WR6A	(RR2A)	RR13B	RR13B
0	1	1	1	0	WR7B	(RR3B)	RR14B	(WR7'B)
0	1	1	1	1	WR7A	(RR3A)	RR15B	RR15B
1	0	0	0	0	WR8B	RR8B	RR8B	RR8B
1	0	0	0	1	WR8A	RR8A	RR8A	RR8A
1	0	0	1	0	WR9	(RR13B)	(RR13B)	(WR3B)
1	0	0	1	1	WR9	(RR13A)	(RR13A)	(WR3A)
1	0	1	0	0	WR10B	RR10B	RR10B	RR10B
1	0	1	0	1	WR10A	RR10A	RR10A	RR10A
1	0	1	1	0	WR11B	(RR15B)	(RR15B)	(WR10B)
1	0	1	1	1	WR11A	(RR15A)	(RR15A)	(WR10A)
1	1	0	0	0	WR12B	RR12B	RR12B	RR12B
1	1	0	0	1	WR12A	RR12B	RR12B	RR12B
1	1	0	1	0	WR13B	RR13B	RR13B	RR13B
1	1	0	1	1	WR13A	RR13A	RR13A	RR13A
1	1	1	0	0	WR14B	RR12B	RR12B	(WR7'B)
1	1	1	0	1	WR14A	RR12B	RR12B	(WR7'B)
1	1	1	1	0	WR15B	RR13B	RR13B	RR13B
1	1	1	1	1	WR15A	RR13A	RR13A	RR13A

Notes:
1. The register names in ( ) are the values read out from that register location.
2. WR15 bit D2 enables status FIFO function (not available on NMOS).
3. WR7' bit D6 enables extend read function (only on ESCC).

Bits 2–0 of WR0 select registers 0–7. With the Point High command, Registers 8–15 are selected. Table 7 lists details of the Z85230/L Register Map.

Table 7. Z85230/L Register Map

A/$\overline{B}$	PNT2	PNT1	PNT0	Write	Read 85C30/230 WR15 D2=0	Read 85C30/230 WR15 D2=1	Read WR15 D2=1 WR7' D6=1
0	0	0	0	WR0B	RR0B	RR0B	RR0B
0	0	0	1	WR1B	RR1B	RR1B	RR1B
0	0	1	0	WR2	RR2B	RR2B	RR2B
0	0	1	1	WR3B	RR3B	RR3B	RR3B
0	1	0	0	WR4B	(RR0B)	(RR0B)	(WR4B)
0	1	0	1	WR5B	(RR1B)	(RR1B)	(WR5B)
0	1	1	0	WR6B	(RR2B)	RR6B	RR6B
0	1	1	1	WR7B	(RR3B)	RR7B	RR7B
1	0	0	0	WR0A	RR0A	RR0A	RR0A
1	0	0	1	WR1A	RR1A	RR1A	RR1A
1	0	1	0	WR2	RR2A	RR2A	RR2A
1	0	1	1	WR3A	RR3A	RR3A	RR3A
1	1	0	0	WR4A	(RR0A)	(RR0A)	(WR4A)
1	1	0	1	WR5A	(RR1A)	(RR1A)	(WR5A)
1	1	1	0	WR6A	(RR2A)	RR6A	RR6A
1	1	1	1	WR7A	(RR3A)	RR7A	RR7A
With Point High Command							
0	0	0	0	WR8B	RR8B	RR8B	RR8B
0	0	0	1	WR9	(RR13B)	(RR13B)	(WR3B)
0	0	1	0	WR10B	RR10B	RR10B	RR10B
0	0	1	1	WR11B	(RR15B)	(RR15B)	(WR10B)
0	1	0	0	WR12B	RR12B	RR12B	RR12B
0	1	0	1	WR13B	RR13B	RR13B	RR13B
0	1	1	0	WR14B	RR14B	RR14B	(WR7'B)
0	1	1	1	WR15B	RR15B	RR15B	RR15B
1	0	0	0	WR8A	RR8A	RR8A	RR8A
1	0	0	1	WR9	(RR13A)	(RR13A)	(WR3A)
1	0	1	0	WR10A	RR10A	RR10A	RR10A
1	0	1	1	WR11A	(RR15A)	(RR15A)	(WR10A)
1	1	0	0	WR12A	RR12A	RR12A	RR12A
1	1	0	1	WR13A	RR13A	RR13A	RR13A
1	1	1	0	WR14A	RR14A	RR14A	(WR7'A)
1	1	1	1	WR15A	RR15A	RR15A	RR15A

Notes:
1. WR15 bit D2 enables status FIFO function (not available on NMOS).
2. WR7' bit D6 enables extend read function (only on ESCC and 85C30).

Table 8 through Table 24 on page 53 list the format of each write register.

Table 8. Write Register 0

Bit	7	6	5	4	3	2	1	0
R/W	W							
Reset	0	0	0	0	0	0	0	0
R = Read W = Write X = Indeterminate								

Bit Position	R/W	Value	Description
7, 6	W	00 01 10 11	Null Code Reset Tx CRC Checker Reset Tx CRC Generator Reset Tx Underrun/EOM Latch
5, 4, 3		000 001 010 011 100 101 110 111	Null Code Point High Reset Ext/Status Interrupts Send Abort (SDLC) Enable Int on Next Rx Character Reset Tx Int Pending Error Reset Reset Highest IUS
2, 1, 0		000 001 010 011 100 101 110 111 000 001 010 011 100 101 110 111	Register 0 Register 1 Register 2 Register 3 Register 4 Register 5 Register 6 Register 7 Register 8 (with Point High) Register 9 (with Point High) Register 10 (with Point High) Register 11 (with Point High) Register 12 (with Point High) Register 13 (with Point High) Register 14 (with Point High) Register 15 (with Point High)
For the 80230, bits 1 and 0 are accessible only through Channel B.			

Table 9. Write Register 1

Bit	7	6	5	4	3	2	1	0
R/W	W							
Reset	0	0	X	0	0	X	0	0
R = Read W = Write X = Indeterminate								

Bit Position	R/W	Value	Description
7		0 1	WAIT/DMA Request Enable Disabled Enabled
6		0 1	WAIT/DMA Request Function Wait Request
5		0 1	WAIT/DMA Request on Receive/Transmit Transmit Receive
4, 3		00 01 10 11	Receive Interrupt Disable Rec Int on First Character or Special Condition Int on all Rx Characters or Special Condition Rx Int on Special Condition Only
2			Parity is Special condition
1			Tx Int Enable
0			Ext Int Enable

Table 10. Write Register 2

Bit	7	6	5	4	3	2	1	0
R/W	W							
Reset	X	X	X	X	X	X	X	X
R = Read W = Write X = Indeterminate								

Bit Position	R/W	Value	Description
7			V7–Interrupt Vector
6			V6–Interrupt Vector
5			V5–Interrupt Vector
4			V4–Interrupt Vector
3			V3–Interrupt Vector
2			V2–Interrupt Vector
1			V1–Interrupt Vector
0			V0–Interrupt Vector

Table 11. Write Register 3

Bit	7	6	5	4	3	2	1	0
R/W	W							
Reset	X	X	X	X	X	X	X	0
R = Read W = Write X = Indeterminate								

Bit Position	R/W	Value	Description
7, 6		00 01 10 11	Rx 5 Bits/Character Rx 7 Bits/Character Rx 6 Bits/Character Rx 8 bits/Character
5			Auto Enable
4			Enter HUNT Mode
3			Rx CRC Enable
2			Address Search Mode (SDLC)
1			Sync Character Load Inhibit
0			Rx Enable

Table 12. Write Register 4

Bit	7	6	5	4	3	2	1	0
R/W	W							
Reset	X	X	X	X	X	1	X	0
R = Read W = Write X = Indeterminate								

Bit Position	R/W	Value	Description
7, 6		00 01 10 11	X1 Clock Mode X16 Clock Mode Z32 Clock Mode X64 Clock Mode
5, 4		00 01 10 11	8-Bit Sync Character 16-Bit Sync Character SDLC Mode (01111110 Flag) External Sync Mode
3, 2		00 01 10 11	Sync Modes Enable 1 Stop Bit/Character 1.5 Stop Bits/Character 2 Stop Bits/Character
1		 0 1	Parity EVEN/$\overline{\text{ODD}}$ Odd Even
0			Parity Enable

Table 13. Write Register 5

Bit	7	6	5	4	3	2	1	0
R/W	W							
Reset	0	X	X	0	0	0	0	X
R = Read W = Write X = Indeterminate								

Bit Position	R/W	Value	Description
7			DTR
6, 5		00 01 10 11	Tx 5 Bits (or less)/Character Tx 7 Bits/Character Tx 6 Bits/Character Tx 8 Bits/Character
4			Send Break
3			Tx Enable
2		 0 1	CRC-16/$\overline{\text{CRC-CCITT}}$ $\overline{\text{CRC-CCITT}}$ CRC-16
1			$\overline{\text{RTS}}$
0			Tx CRC Enable

Table 14. Write Register 6

Bit	7	6	5	4	3	2	1	0
R/W	W							
Reset	X	X	X	X	X	X	X	X
R = Read W = Write X = Indeterminate								

Bit Position	R/W	Value	Description					
			Monosync 8 Bits	Monosync 6 Bits	Bisync 16 Bits	Bisync 12 Bits	SDLC	SDLC (Address Range)
7			Sync7	Sync1	Sync7	Sync3	ADR7	ADR7
6			Sync6	Sync0	Sync6	Sync2	ADR6	ADR6
5			Sync5	Sync5	Sync5	Sync1	ADR5	ADR5
4			Sync4	Sync4	Sync4	Sync0	ADR4	ADR4
3			Sync3	Sync3	Sync3	1	ADR3	X
2			Sync2	Sync2	Sync2	1	ADR2	X
1			Sync1	Sync1	Sync1	1	ADR1	X
0			Sync0	Sync0	Sync0	1	ADR0	X

Table 15. Write Register 7

Bit	7	6	5	4	3	2	1	0
R/W	W							
Reset	X	X	X	X	X	X	X	X
R = Read W = Write X = Indeterminate								

Bit Position	R/W	Value	Description					
			This column contains no data	**Monosync 8 Bits**	**Monosync 6 Bits**	**Bisync 16 Bits**	**Bisync 12 Bits**	**SDLC**
7				Sync7	Sync5	Sync15	Sync11	0
6				Sync6	Sync4	Sync14	Sync10	1
5				Sync5	Sync3	Sync13	Sync9	1
4				Sync4	Sync2	Sync12	Sync8	1
3				Sync3	Sync1	Sync11	Sync7	1
2				Sync2	Sync0	Sync10	Sync6	1
1				Sync1	X	Sync9	Sync5	1
0				Sync0	X	Sync8	Sync4	0

Table 16. Write Register 7'

Bit	7	6	5	4	3	2	1	0
R/W	W							
Reset	0	0	1	0	0	0	0	0
R = Read W = Write X = Indeterminate								

Bit Position	R/W	Value	Description
7		0	Not Used. Must be 0.
6			Extended Read Enable
5			Tx FIFO Int Level
4			$\overline{DTR}/\overline{REQ}$ Timing Mode
3			Rx FIFO Int Level
2			Auto RTS Deactivation
1			Auto EOM Reset
0			Auto Tx Flag

Table 17. Write Register 8

Bit	7	6	5	4	3	2	1	0
R/W	W							
Reset	0	0	1	0	0	0	0	0
R = Read W = Write X = Indeterminate								

Bit Position	R/W	Value	Description
7			D7
6			D6
5			D5
4			D4
3			D3
2			D2
1			D1
0			D0

Table 18. Write Register 9

Bit	7	6	5	4	3	2	1	0
R/W	W							
Hardware Reset	1	1	0	0	0	0	X	X
Channel Reset	X	X	0	X	X	X	X	X
R = Read W = Write X = Indeterminate								

Bit Position	R/W	Value	Description
7, 6		00 01 10 11	No Reset Channel Reset B Channel Reset A Force Hardware Reset
5			Software $\overline{\text{INTACK}}$ Enable
4		 0 1	Status High/ Status Low Low High
3			Master Interrupt Enable
2			Disable Lower Chain
1			No Vector
0			Vector Includes Status

Table 19. Write Register 10

Bit	7	6	5	4	3	2	1	0
R/W	W							
Hardware Reset	0	0	0	0	0	0	0	0
Channel Reset	0	X	X	0	0	0	0	0
R = Read W = Write X = Indeterminate								

Bit Position	R/W	Value	Description
7			CRC Preset I/O
6, 5		00 01 10 11	NRZ NRZI FM 1 (Transition = 1) FM 0 (Transition = 0)
4			Go Active on Poll
3		 0 1	Mark/Flag Idle Flag Idle Mark Idle
2		 0 1	Abort/Flag on Underrun Flag Abort
1			Loop Mode
0		 0 1	6-Bit/8-Bit sync 8-Bit 6-bit

Table 20. Write Register 11

Bit	7	6	5	4	3	2	1	0
R/W	W							
Hardware Reset	0	0	0	0	1	0	0	0
Channel Reset	X	X	X	X	X	X	X	X

R = Read W = Write X = Indeterminate

Bit Position	R/W	Value	Description
7			$\overline{\text{RTxC}}$ Xtal/No Xtal
		0	No Xtal
		1	$\overline{\text{RTxC}}$ Xtal
6, 5		00	Receive Clock = $\overline{\text{RTxC}}$ Pin
		01	Receive Clock = $\overline{\text{TRxC}}$ Pin
		10	Receive Clock = BRG Output
		11	Receive Clock = DPLL Output
4, 3		00	Transmit Clock = $\overline{\text{RTxC}}$ Pin
		01	Transmit Clock = $\overline{\text{TRxC}}$ Pin
		10	Transmit Clock = BRG Output
		11	Transmit Clock = DPLL Output
2			TRxC Input/Output
		0	Output
		1	Input
1		00	$\overline{\text{TRxC}}$ Out = Xtal Output
		01	$\overline{\text{TRxC}}$ Out = Transmit Clock
		10	$\overline{\text{TRxC}}$ Out = BRG Output
		11	$\overline{\text{TRxC}}$ Out = DPLL Output

Table 21. Write Register 12

Bit	7	6	5	4	3	2	1	0
R/W	W							
Reset	X	X	X	X	X	X	X	X
R = Read W = Write X = Indeterminate								

Bit Position	R/W	Value	Description (Lower Byte of Time Constant)
7			TC7
6			TC6
5			TC5
4			TC4
3			TC3
2			TC2
1			TC1
0			TC0

Table 22. Write Register 13

Bit	7	6	5	4	3	2	1	0
R/W	W							
Reset	X	X	X	X	X	X	X	X
R = Read W = Write X = Indeterminate								

Bit Position	R/W	Value	Description (Upper Byte of Time Constant)
7			TC15
6			TC14
5			TC13
4			TC12
3			TC11
2			TC10
1			TC9
0			TC8

Table 23. Write Register 14

Bit	7	6	5	4	3	2	1	0
R/W	W							
Reset	X	X	X	X	X	X	X	X
R = Read W = Write X = Indeterminate								

Bit Position	R/W	Value	Description (Upper Byte of Time Constant)
7, 6, 5		000 001 010 011 100 101 110 111	Null Command Enter Search Mode Reset Missing Clock Disable DPLL Set source - $\overline{\text{BRG}}$ Set Source = $\overline{\text{RTxC}}$ Set FM Mode Set NRZI Mode
4			Local Loopback
3			Auto Echo
2			DTR/Request Generator Source
1			$\overline{\text{BRG}}$ Source
0			$\overline{\text{BRG}}$ Enable

Table 24. Write Register 15

Bit	7	6	5	4	3	2	1	0
R/W	W							
Reset	1	1	1	1	0	0	0	0
R = Read W = Write X = Indeterminate								

Bit Position	R/W	Value	Description
7			Break/Abort Interrupt Enable
6			Tx Underrun/EOM Interrupt Enable
5			$\overline{\text{CTS}}$ Interrupt Enable
4			$\overline{\text{Sync}}$/Hunt
3			$\overline{\text{DCD}}$ Interrupt Enable
2			SDLC FIFO Enable
1			Zero Count Interrupt Enable
0			WR7' SDLC Feature Enable

Read Registers

The ESCC contains ten read registers (eleven, counting the receive buffer RR8) in each channel. Four of these may be read to obtain status information (RR0, RR1, RR10, and RR15).

Two registers, RR12 and RR13, are read to learn the BRG time constant. RR2 contains either the unmodified interrupt vector, Channel A, or the vector modified by status information, Channel B.

RR3 contains the Interrupt Pending (IP) bits for Channel A.

RR6 and RR7 contain the information in the SDLC Frame Status FIFO, but is only read when WR15 bit 2 is 1. If WR7' bit 6 is 1, Write Registers WR3, WR4, WR5, and WR10 can be read as RR9, RR4, RR5, and RR14, respectively. Table 25 on page 54 through Table 40 on page 69 list the format of the read registers.

Table 25. Read Register 0

Bit	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
R/W	R							
Reset	X	1	X	X	X	1	0	0
R = Read W = Write X = Indeterminate								

Bit Position	**R/W**	**Value**	**Description**
7			Break/Abort
6			Tx Underrun/EOM
5			$\overline{\text{CTS}}$
4			$\overline{\text{Sync}}$/Hunt
3			$\overline{\text{DCD}}$ Interrupt Enable
2			Tx Buffer Empty
1			Zero Count
0			Rx Character Available

Table 26. Read Register 1

Bit	7	6	5	4	3	2	1	0
R/W	R							
Reset	0	0	0	0	0	1	1	X
R = Read W = Write X = Indeterminate								

Bit Position	R/W	Value	Description
7			EOF (SDLC)
6			CRC/Framing Error
5			Rx Overrun Error
4			Parity Error
3			Residue Code 0
2			Residue Code 1
1			Residue Code 2
0			All Sent

Table 27. Read Register 2

Bit	7	6	5	4	3	2	1	0
R/W	R							
Reset	X	X	X	X	X	X	X	X
R = Read W = Write X = Indeterminate								

Bit Position	R/W	Value	Description (Interrupt Vector)
7			V7
6			V6
5			V5
4			V4
3			V3
2			V2
1			V1
0			V0
These bits include status information when read from Channel B.			

Table 28. Read Register 3

Bit	7	6	5	4	3	2	1	0
R/W	R							
Reset	X	X	X	X	X	X	X	X
R = Read W = Write X = Indeterminate								

Bit Position	R/W	Value	Description
7			0
6			0
5			Channel A Rx IP
4			Channel A Tx IP
3			Channel A Ext/Status IP
2			Channel B Rx IP
1			Channel B Tx IP
0			Channel B Ext/Status IP
Bits 5, 4, 3, 2, 1 and 0 are always 0 when read from Channel B.			

Table 29. Read Register 4

Bit	7	6	5	4	3	2	1	0
R/W	R							
Reset	X	X	X	X	X	X	X	X
R = Read W = Write X = Indeterminate								

Bit Position	R/W	Value	Description
7, 6		00 01 10 11	X1 Clock Mode X16 Clock Mode Z32 Clock Mode X64 Clock Mode
5, 4		00 01 10 11	8-Bit Sync Character 16-Bit Sync Character SDLC Mode (01111110 Flag) External Sync Mode
3, 2		00 01 10 11	Sync Modes Enable 1 Stop Bit/Character 1.5 Stop Bits/Character 2 Stop Bits/Character
1		 0 1	Parity EVEN/$\overline{\text{ODD}}$ Odd Even
0			Parity Enable
This register reflects the contents of RR0 if WR7' bit 6 is enabled.			

Table 30. Read Register 5

Bit	7	6	5	4	3	2	1	0
R/W	R							
Reset	X	X	X	X	X	X	X	X
R = Read W = Write X = Indeterminate								

Bit Position	R/W	Value	Description
7			$\overline{\text{DTR}}$
6, 5		00 01 10 11	Tx 5 Bits (or less)/Character Tx 7 Bits/Character Tx 6 Bits/Character Tx 8 Bits/Character
4			Send Break
3			Tx Enable
2		 0 1	CRC-16/$\overline{\text{CRC-CCITT}}$ $\overline{\text{CRC-CCITT}}$ CRC-16
1			$\overline{\text{RTS}}$
0			Tx CRC Enable
This register reflects the contents of RR1 if WR7' bit 6 is enabled.			

Table 31. Read Register 6

Bit	7	6	5	4	3	2	1	0
R/W	R							
Reset	X	X	X	X	X	X	X	X
R = Read W = Write X = Indeterminate								

Bit Position	R/W	Value	Description
7			BC7
6			BC6
5			BC5
4			BC4
3			BC3
2			BC2
1			BC1
0			BC0
This register can be accessed only if WR15 bit 2 is 1. If this bit is not enabled this register reflects RR2.			

Table 32. Read Register 7

Bit	7	6	5	4	3	2	1	0
R/W	R							
Reset	X	X	X	X	X	X	X	X
R = Read W = Write X = Indeterminate								

Bit Position	R/W	Value	Description
7		0 1	FOS: FIFO Status Overflow FIFO Overflowed Normal
6		0 1	FDA: FIFO Data Available Status Reads from FIFO Status Reads from ESCC
5			BC13
4			BC12
3			BC11
2			BC10
1			BC9
0			BC8
This register can be accessed only if WR15 bit 2 is 1. If this bit is not enabled this register reflects RR3.			

Table 33. Read Register 8

Bit	7	6	5	4	3	2	1	0
R/W	R							
Reset	0	0	1	0	0	0	0	0
R = Read W = Write X = Indeterminate								

Bit Position	R/W	Value	Description
7			D7
6			D6
5			D5
4			D4
3			D3
2			D2
1			D1
0			D0

Table 34. Read Register 9

Bit	7	6	5	4	3	2	1	0
R/W	R							
Hardware Reset	1	1	0	0	0	0	X	X
Channel Reset	X	X	0	X	X	X	X	X
R = Read W = Write X = Indeterminate								

Bit Position	R/W	Value	Description
7, 6		00 01 10 11	No Reset Channel Reset B Channel Reset A Force Hardware Reset
5			Software INTACK Enable
4		 0 1	Status High/Status Low Low High
3			Master Interrupt Enable
2			Disable Lower Chain
1			No Vector
0			Vector Includes Status
To access this register WR7’ bit 6 must be enabled.			

Table 35. Read Register 10

Bit	7	6	5	4	3	2	1	0
R/W	R							
Reset	0	0	1	0	0	0	0	0
R = Read W = Write X = Indeterminate								

Bit Position	R/W	Value	Description
7			One Clock Missing
6			Two Clocks Missing
5			0
4			Loop Sending
3			0
2			0
1			On Loop
0			0

Table 36. Read Register 11

Bit	7	6	5	4	3	2	1	0
R/W	R							
Hardware Reset	0	0	0	0	0	0	0	0
Channel Reset	X	X	X	X	X	X	X	X
R = Read W = Write X = Indeterminate								

Bit Position	R/W	Value	Description
7			CRC Preset I/O
6, 5		00 01 10 11	NRZ NRZI FM1 (Transition = 1) FM0 (Transition = 0)
4			Go Active on Poll
3		 0 1	Mark/Flag Idle Flag Idle Mark Idle
2		 0 1	Abort Flag on Underrun Flag Abort
1			Loop Mode
0		 0 1	6-Bit/8-Bit Sync 8-Bit Sync 6-Bit Sync
To access this register WR7' bit 6 must be enabled. If this bit is not enabled, this register reflects RR15.			

Table 37. Read Register 12

Bit	7	6	5	4	3	2	1	0
R/W	R							
Reset	X	X	X	X	X	X	X	X
R = Read W = Write X = Indeterminate								

Bit Position	R/W	Value	Description (Lower Byte of Time Constant)
7			TC7
6			TC6
5			TC5
4			TC4
3			TC3
2			TC2
1			TC1
0			TC0

Table 38. Read Register 13

Bit	7	6	5	4	3	2	1	0
R/W	R							
Reset	X	X	X	X	X	X	X	X
R = Read W = Write X = Indeterminate								

Bit Position	R/W	Value	Description (Upper Byte of Time Constant)
7			TC15
6			TC14
5			TC13
4			TC12
3			TC11
2			TC10
1			TC9
0			TC8

Table 39. Read Register 14

Bit	7	6	5	4	3	2	1	0
R/W	R							
Reset	0	0	1	0	0	0	0	0
R = Read W = Write X = Indeterminate								

Bit Position	R/W	Value	Description
7		0	Not Used. Must be 0.
6			Extended Read Enable
5			Tx FIFO Int Level
4			$\overline{DTR}/\overline{REQ}$ Timing Mode
3			Rx FIFO Int Level
2			Auto RTS Deactivation
1			Auto EOM Reset
0			Auto Tx Flag
To access this register WR7' bit 6 must be enabled. If this bit is not enabled this register reflects RR10.			

Table 40. Read Register 15

Bit	7	6	5	4	3	2	1	0
R/W	R							
Reset	X	X	X	X	X	X	X	X
R = Read W = Write X = Indeterminate								

Bit Position	R/W	Value	Description
7			Break/Abort Interrupt Enable
6			Tx Underrun/EOM Interrupt Enable
5			$\overline{\text{CTS}}$ Interrupt Enable
4			$\overline{\text{Sync}}$/Hunt
3			$\overline{\text{DCD}}$ Interrupt Enable
2			SDLC FIFO Enable
1			Zero Count Interrupt Enable
0			WR7’ SDLC Feature Enable

Z80230 Interface Timing

Z80230 Write Cycle Timing

The Z-Bus compatible ESCC is suited for system applications with multiplexed address/data buses.

Two control signals, $\overline{AS}$ and $\overline{DS}$, are used by the Z80230 to control bus transactions. Additionally, four other control signals ($\overline{CS0}$, CS1, $\overline{RW}$, and $\overline{INTACK}$) control the type of bus transaction that occurs. A bus transaction is initiated by $\overline{AS}$. The rising edge latches the register address on the Address/Data bus and the state of $\overline{INTACK}$ and $\overline{CS0}$.

In addition to bus transactions, the interrupt section uses the $\overline{AS}$ to set Interrupt Pending (IP) bits. Therefore, $\overline{AS}$ must be kept cycling for the interrupt section to function.

The Z80230 generates internal control signals in response to a register access. Because $\overline{AS}$ and $\overline{DS}$ have no defined phase relationship with PCLK, the circuitry generating these internal control signals provide time for metastable conditions to disappear. This action results in a recovery time related to PCLK.

This recovery time applies only to transactions involving the Z80230, and any intervening transactions are ignored. This recovery time is four PCLK cycles, measured from the falling edge of $\overline{DS}$ for one access to the ESCC, to the falling edge of $\overline{DS}$ for a subsequent access. Figure 17 displays the Write cycle timing.

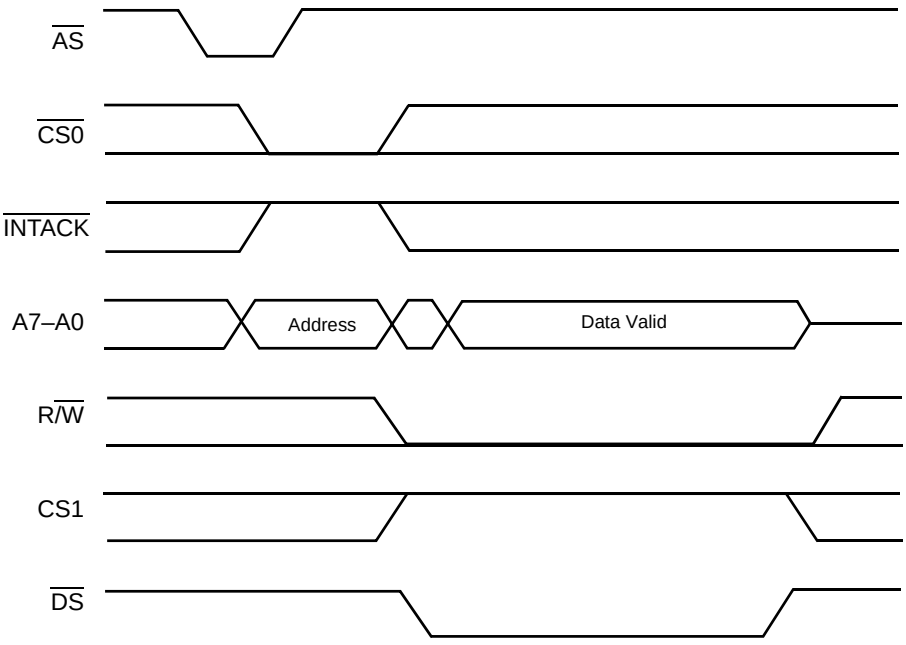


Figure 17. Z80230 Write Cycle Timing

Z80230 Read Cycle Timing

The Read Cycle Timing for the Z80230 is displayed in Figure 18. The register address on A7-A0, as well as the state of $\overline{CS0}$ and $\overline{INTACK}$, are latched by the rising edge of $\overline{AS}$. R/$\overline{W}$ must be High before $\overline{DS}$ falls to indicate a Read cycle. The Z80230 data bus drivers are enabled while CS1 is High and $\overline{DS}$ is Low.

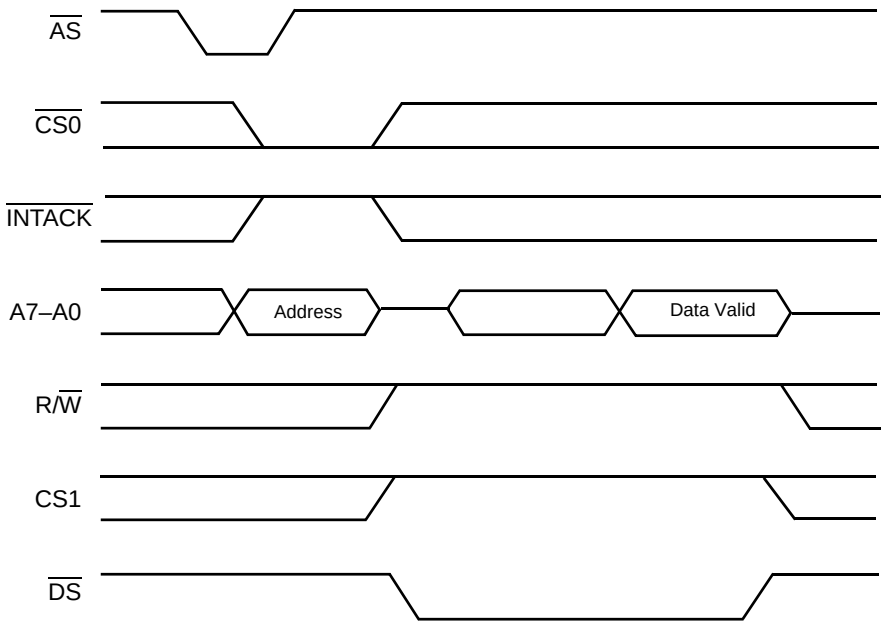


Figure 18. Z80230 Read Cycle Timing

Z80230 Interrupt Acknowledge Cycle Timing

The Interrupt Acknowledge cycle timing for the Z80230 is displayed in Figure 19 on page 72. The address on A7-A0 and the state of $\overline{CS0}$ and $\overline{INTACK}$ are latched by the rising - edge of $\overline{AS}$. However, if $\overline{INTACK}$ is Low. The address on A7-A0, $\overline{CS0}$, CS1, and R/$\overline{W}$ are ignored for the duration of the interrupt acknowledge cycle.

The Z80230 samples the state of $\overline{INTACK}$ on the rising edge of $\overline{AS}$, and AC parameters. Parameters 7 and 8 of Table 45 on page 83, specify the setup and hold time requirements. Between the rising edge of $\overline{AS}$ and the falling edge of $\overline{DS}$, the internal and external daisy chains settle, as specified in parameter 29. A system with no external daisy chain provides the time priority internal to the ESCC. Systems using an external daisy chain must refer to Note 5 of Table 45, for the time required to settle the daisy chain.

If there is an interrupt pending in the ESCC, and IEI is High when $\overline{DS}$ falls, the acknowledge cycle is intended for the ESCC. Consequently, the Z80230 sets the Interrupt Under Service (IUS) latch for the highest priority pending interrupt, and places an interrupt vec-

tor on A7-A0. WR9 bit 1 is set to 1 to disable the placing of a vector on a bus. The $\overline{INT}$ pin also goes inactive in response to the falling edge of $\overline{DS}$. There is only one $\overline{DS}$ per interrupt acknowledge cycle.

IP bits in the Z80230 are updated by $\overline{AS}$, which can delay interrupt requests if the processor does not supply $\overline{AS}$ strobes during the time in between accesses of the Z80230.

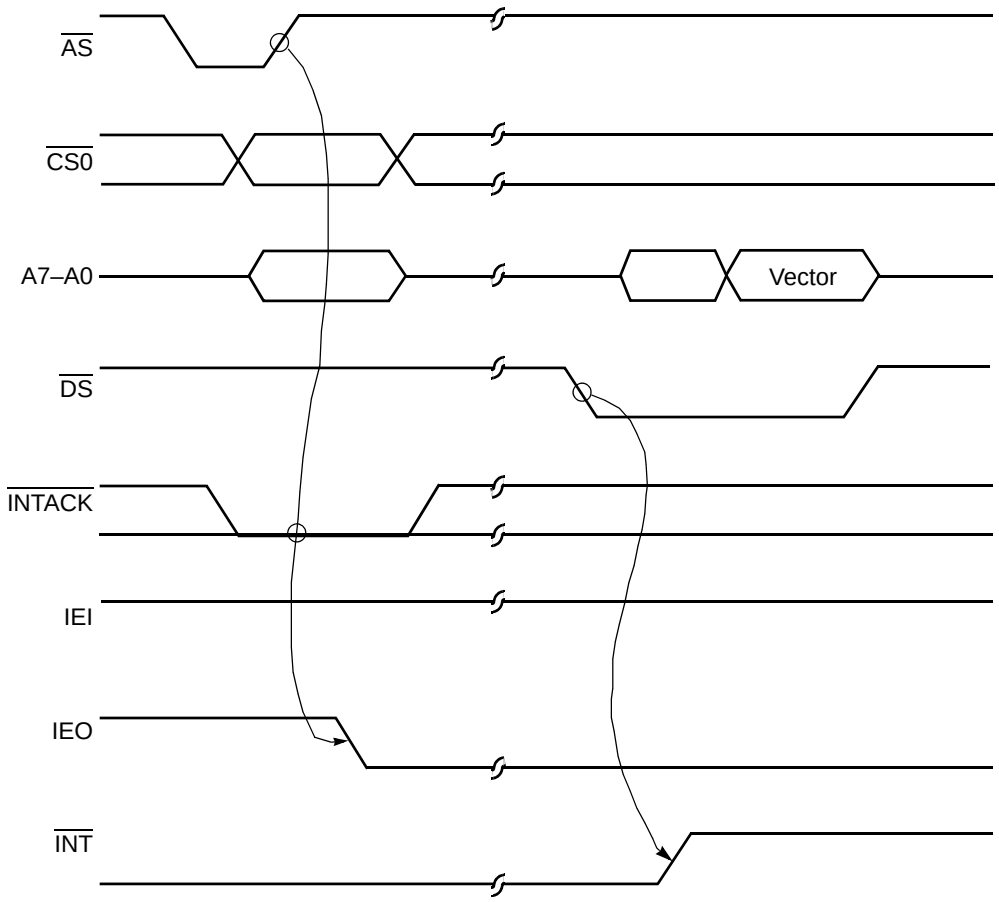


Figure 19. Z80230 Interrupt Acknowledge Cycle Timing

Z85230/L Timing

The ESCC generates internal control signals from $\overline{WR}$ and $\overline{RD}$ that relate to PCLK. Because PCLK had no defined phase relationship with $\overline{WR}$ and $\overline{RD}$, the circuitry generating the internal control signals provides time for metastable conditions to disappear. This causes a recovery time related to PCLK. The recovery time applies only to bus transactions involving the ESCC. The recovery time required for proper operation is specified

from the falling edge of $\overline{WR}$ or $\overline{RD}$ in the first transaction involving the ESCC, to the falling edge of $\overline{WR}$ or $\overline{RD}$ in the second transaction. This time must be at least four PCLKs regardless of which register or channel is accessed.

Z85230/L Read Cycle Timing

Figure 20 displays Read Cycle timing. Addresses on A/$\overline{B}$ and D/$\overline{C}$ and the status on $\overline{INTACK}$ must remain stable throughout the cycle. The effective $\overline{RD}$ time reduces if $\overline{CE}$ falls after $\overline{RD}$ falls, or if it rises before $\overline{RD}$ rises.

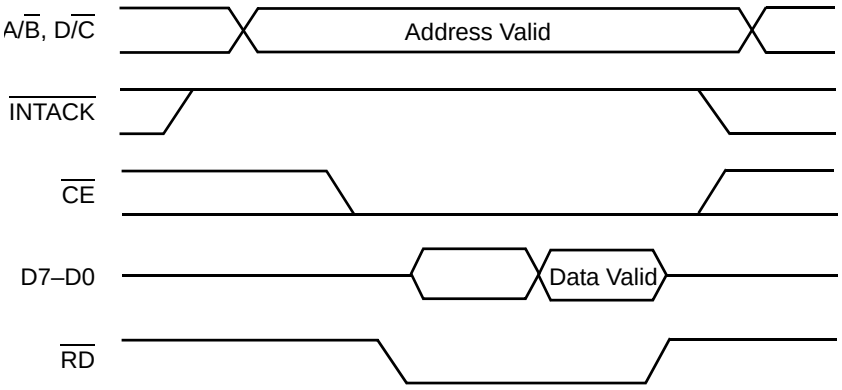


Figure 20. Read Cycle Timing (Z85230/L)

Z85230/L Write Cycle Timing

Figure 21 on page 74 displays Write Cycle timing. Addresses on A/$\overline{B}$ and D/$\overline{C}$ and the status on $\overline{INTACK}$ must remain stable throughout the cycle. The effective $\overline{WR}$ time reduces if $\overline{CE}$ falls after $\overline{WR}$ falls, or if it rises before $\overline{WR}$ rises. In Write Cycle timing, the $\overline{WR}$ signal returns a High slightly before the Address goes invalid.

Because many popular CPUs do not guarantee that the databus is valid when $\overline{WR}$ is Low, the ESCC no longer requires a valid databus when the $\overline{WR}$ pin is Low. For more information, see AC characteristics parameter 29 available in Table 47 on page 90.

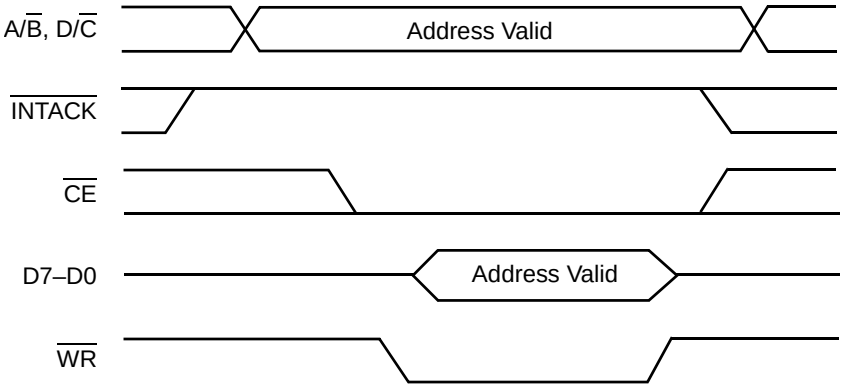


Figure 21. Write Cycle Timing (Z85230/L)

Z85230/L Interrupt Acknowledge Cycle Timing

Figure 22 displays Interrupt Acknowledge Cycle timing. Between the time INTACK goes Low and the falling edge of RD, the internal and external IEI/IEO daisy chains settle. If there is an interrupt pending in the ESCC and IEI is High when RD falls, the Acknowledge cycle is intended for the ESCC. In this case, the ESCC may be programmed to respond to RD Low by placing its interrupt vector on D7–D0. It then sets the appropriate IUS latch internally. If the external daisy chain is not used, then AC Parameter 38 is required to settle the interrupt priority daisy chain internal to the ESCC. If the external daisy chain is used, follow the equation in AC Characteristics Note 5 (Table 47 on page 90) to calculate the required daisy chain settle time.

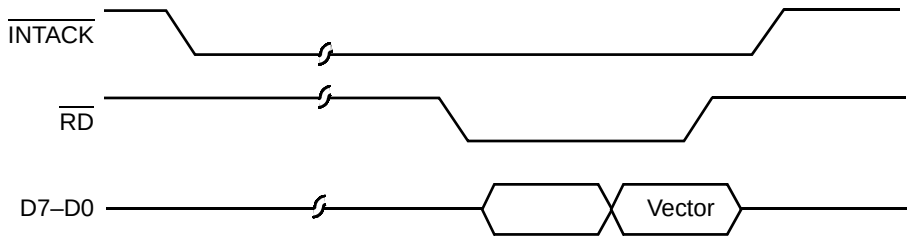


Figure 22. Interrupt Acknowledge Cycle Timing (Z85230/L)

Electrical Characteristics

Absolute Maximum Ratings

Stresses greater than those listed in this section can cause permanent damage to the device. These ratings are stress ratings only. Operation of the device at any condition above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods can affect reliability.

V_{CC} Supply Voltage Range	–0.3 V to +7.0 V
Voltages on All Pins with Respect to GND	–0.3 V to V_{CC} +0.3 V
Operating Ambient Temperature	See Ordering Information on page 107
Storage Temperatures	–65º C to +150º C

Standard Test Conditions

The DC Characteristics and capacitance sections apply for the following standard test conditions, unless otherwise noted. All voltages reference GND. Positive current flows into the referenced pin. Standard conditions are as follows:

- GND = 0 V
- T_A as specified in Ordering Information
- +4.5V ≤ V_{CC} ≤ +5.5V" or +3.0 V ≤ V_{CC} ≤ +3.6V (Z8523L only)

Figure 23 displays typical test load configurations.

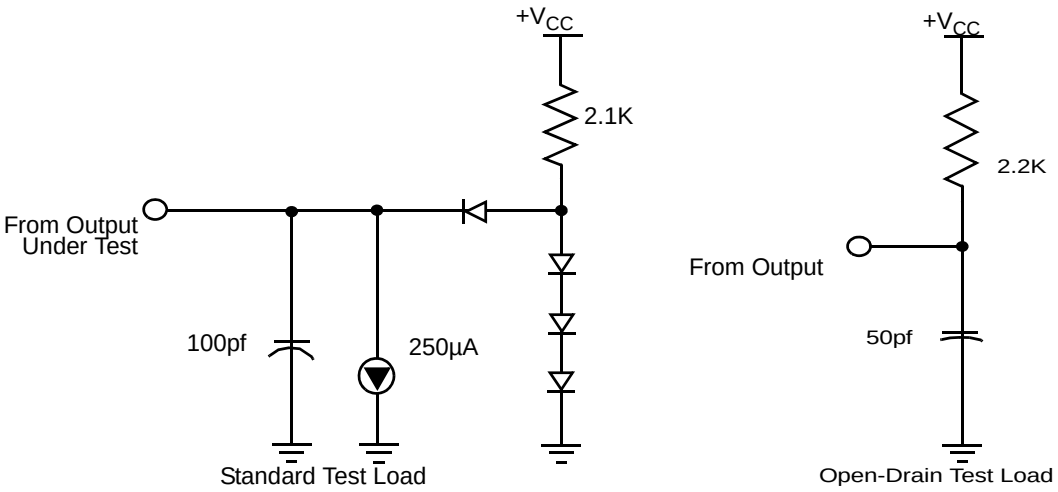


Figure 23. Standard and Open-Drain Test Loads

Capacitance

Table 41 lists the capacitance parameters and contains the symbols and test conditions for each.

Table 41. Capacitance Parameters

Symbol	Parameter	Min	Max	Unit	Test Condition
C_{IN}	Input Capacitance		10	pF	Unmeasured Pins Returned to Ground
C_{OUT}	Output Capacitance		15	pF	
$C_{I/O}$	Bidirectional Capacitance		20	pF	

Note: f = 1 MHz, over specified temperature range.

Miscellaneous

Gate count—11,000 for both Z80230 and Z85230/L.

DC Characteristics

Table 42 lists the DC characteristics for the Z80230/Z85230 device.

Table 42. Z80230/Z85230 DC Characteristics

Symbol	Parameter	Min.	Typ.	Max.	Unit	Condition
V_{IH}	Input High Voltage	2.2		V_{CC} + 0.3	V	
V_{IL}	Input Low Voltage	– 0.3		0.8	V	
V_{OH1}	Output High Voltage	2.4			V	IOH = – 1.6 mA
V_{OH2}	Output High Voltage	V_{CC} – 0.8			V	IOH = – 250 µA
V_{OL}	Output Low Voltage			0.4	V	IOL = +2.0 mA
I_{IL}	Input Leakage			± 10.0	µA	0.4 <V_{IN}<+2.4 V
I_{OL}	Output Leakage			± 10.0	µA	0.4 <V_{OUT}<+2.4 V
I_{CC1}	V_{CC} Supply Current		4 5 7 9	10 (8.5 MHz) 12 (10 MHz) 15 (16 MHz) 20 (20 MHz)	mA mA mA mA	V_{CC}=5 V,V_{IH}=4.8, V_{IL}=0.2 V Crystal oscillators off
$I_{CC(OSC)}$	Crystal OSC Current		6		mA	Current for each oscillator in addition to I_{CC1}

Notes:
1. Vcc=5 V ± 10% unless otherwise specified, over specified temperature range.
2. Typical Icc was measured with oscillator off.
3. No Icc(osc) max is specified because of dependency on the external circuit.

Table 43 lists the DC characteristics for the Z8523L device.

Table 43. Z8523L DC Characteristics

Symbol	Parameter	Min.	Typ.	Max.	Unit	Condition
V_{IH}	Input High Voltage	2.2		V_{CC} + 0.3	V	
V_{IL}	Input Low Voltage	– 0.3		0.2*V_{CC}	V	
V_{OH1}	Output High Voltage	2.4			V	IOH = – 1.6 mA
V_{OH2}	Output High Voltage	V_{CC} – 0.4			V	IOH = – 250 µA
V_{OL}	Output Low Voltage			0.2	V	IOL = +2.0 mA
I_{IL}	Input Leakage			± 10.0	µA	0.4 <V_{IN}<+2.4 V
I_{OL}	Output Leakage			± 10.0	µA	0.4 <V_{OUT}<+2.4 V
I_{CC1}	V_{CC} Supply Current		2 2.5 4	3 (8.5 MHz) 4 (10 MHz) 6 (16 MHz)	mA mA mA	V_{CC}=3.3 V,V_{IH}=3.1, V_{IL}=0.2 V Crystal oscillators off
$I_{CC(OSC)}$	Crystal OSC Current		6		mA	Current for each oscillator in addition to I_{CC1}

Notes:
1. Vcc=3.3 V ± 10% unless otherwise specified, over specified temperature range.
2. Typical Icc was measured with oscillator off.
3. No Icc(osc) max is specified because of dependency on the external circuit.
4. **I/O pins are NOT 5V tolerant**

AC Characteristics

Figure 24 on page 79 displays the Z80230 Read/Write timing diagram.

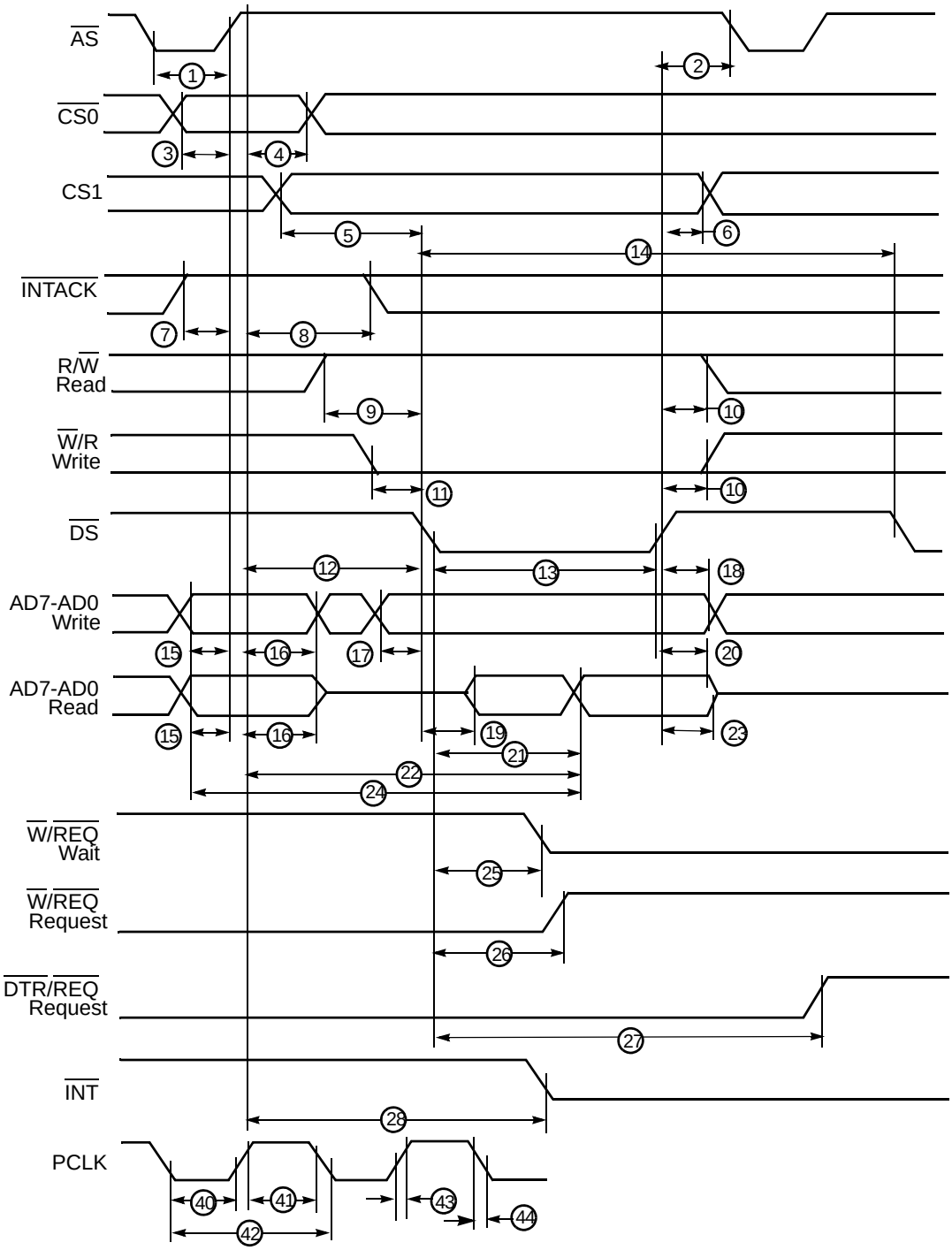


Figure 24. Z80230 Read/Write Timing Diagram

Figure 25 displays the Z80230 Interrupt Acknowledge timing diagram

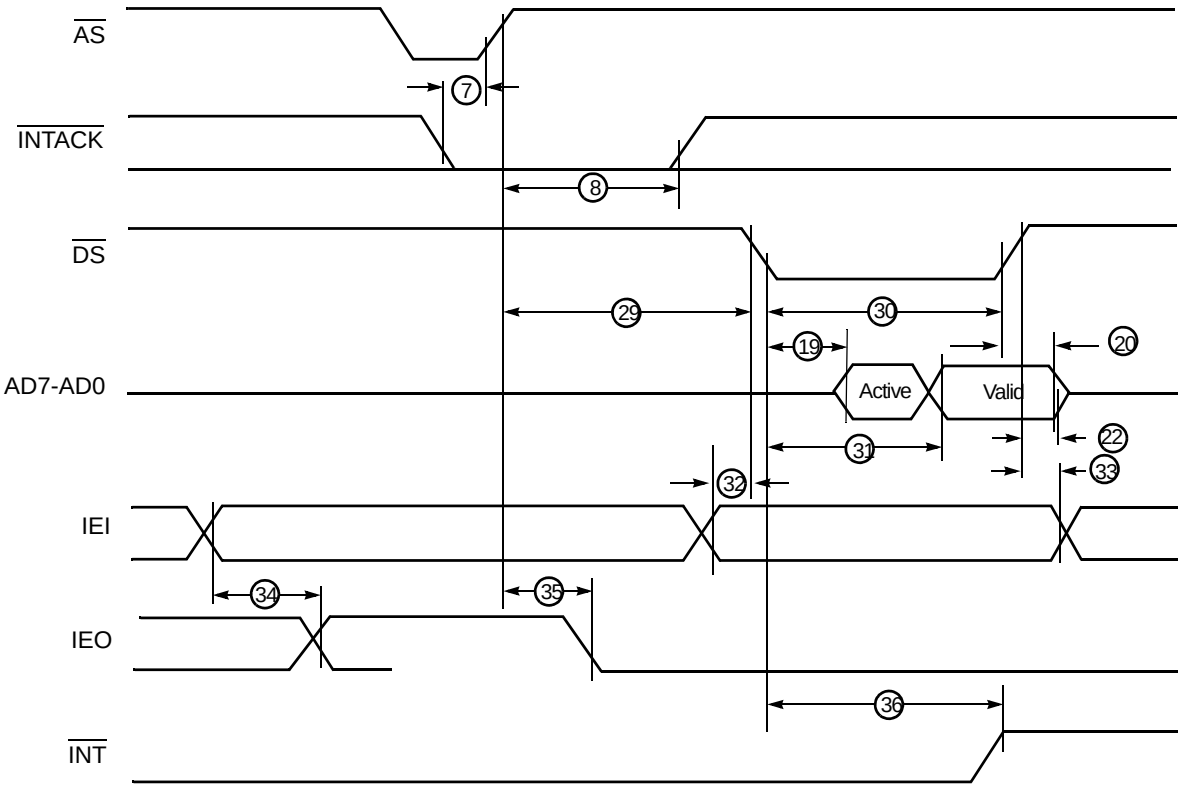


Figure 25. Z80230 Interrupt Acknowledge Timing Diagram

Figure 26 displays the Z80230 Reset timing diagram

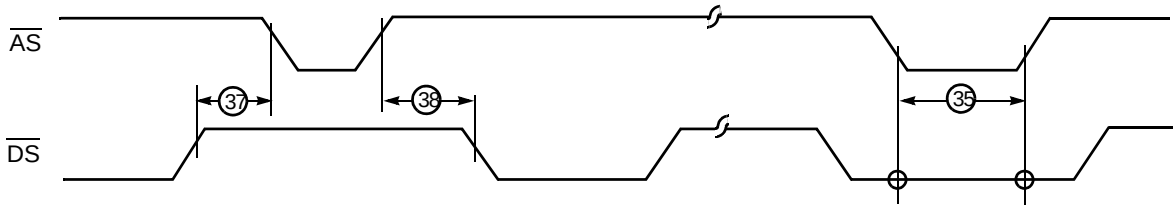


Figure 26. Z80230 Reset Timing Diagram

Table 45 lists the AC characteristics of the Z80230 and Table 47 lists the AC characteristics of Z85230/L.

Figure 27 displays the Z80230 general timing diagram.

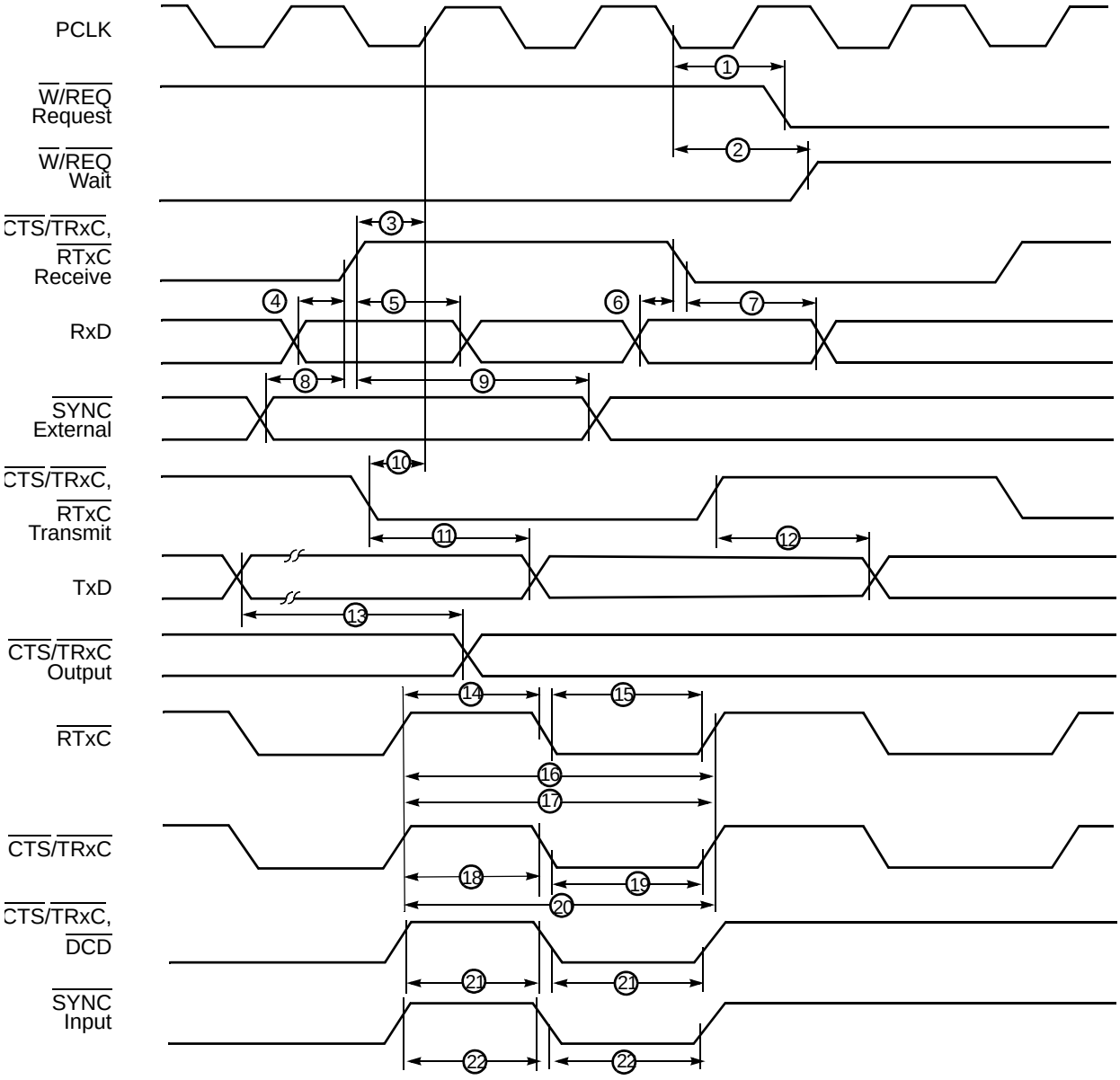


Figure 27. Z80230 General Timing Diagram

Table 44 lists the Z80230 general timing characteristics details.

Table 44. Z80230 General Timing Characteristics

			10 MHz		16 MHz		
No.	**Symbol**	**Parameter**	**Min.**	**Max.**	**Min.**	**Max.**	**Notes**
1	TdPC (REQ)	PCLK Low to $\overline{W}$/$\overline{REQ}$ Valid		200		110	9
2	TsPC (W)	PCLK Low to Wait Inactive		300		180	9
3	TsRXC (PC)	RxC High to PCLK High Setup Time	NA		NA		1, 4, 9
4	TsRXD (RXCr)	RxD to RxC High Setup Time	0		0		1,9
5	ThRXD (RxCr)	RxD to RxC High Hold Time	125		60		1,9
6	TsRXD (RXCf)	RxD to RxC Low Setup Time	0		0		1, 5, 9
7	ThRXD (RXCf)	RxD to RxC Low Hold Time	125		60		1, 5, 9
8	TsSY (RXC)	$\overline{SYNC}$ to RxC High Setup Time	-150		-100		1, 9
9	ThSY (RXC)	$\overline{SYNC}$ to RxC High Hold Time	5		5		1, 10
10	TsTXC (PC)	TxC Low to PCLK High Setup Time	NA		NA		2, 4, 9
11	TdTXCf (TXD)	TxC Low to TxD Delay		150		85	2, 9
12	TdTxCr (TXD)	TxC High to TxD Delay		150		85	2, 5, 9
13	TdTXD (TRX)	TxD to $\overline{TRxC}$ Delay		140		80	9
14	TwRTXh	$\overline{RTxC}$ High Width	120		80		6, 9
15	TwRTXl	$\overline{TRxC}$ Low Width	120		80		6, 9
16a	TcRTX	$\overline{RTxC}$ Cycle Time	400		244		6, 7, 9
16b	TxRX (DPLL)	DPLL Cycle Time Minimum	50		31		7, 8, 9
17	TcRTXX	Crystal Oscillator Period	100	1000	100	1000	3, 9
18	TwTRXh	$\overline{TRxC}$ High Width	120		80		6, 9
19	TwTRXl	$\overline{TRxC}$ Low Width	120		80		6, 9
20	TcTRX	$\overline{TRxC}$ Cycle Time	400		244		6, 7, 9
21	TwEXT	$\overline{DCD}$ or $\overline{CTS}$ Pulse Width	120		70		9
22	TwSY	$\overline{SYNC}$ Pulse Width	120		70		9

Table 44. Z80230 General Timing Characteristics (Continued)

No.	Symbol	Parameter	10 MHz Min.	10 MHz Max.	16 MHz Min.	16 MHz Max.	Notes

Notes:
1. RxC is $\overline{\text{RTxC}}$ or $\overline{\text{TRxC}}$, whichever is supplying the receive clock.
2. TxC is $\overline{\text{TRxC}}$ or $\overline{\text{RTxC}}$, whichever is supplying the transmit clock.
3. Both RTxC and $\overline{\text{SYNC}}$ have 30 pf capacitors to ground connected to them.
4. Synchronization of RxC to PCLK is eliminated in divide by four operation.
5. Parameter applies only to FM encoding/decoding.
6. Parameter applies only for transmitter and receiver; DPLL and BRG timing requirements are identical to PCLK requirements.
7. The maximum transmit or receive data rate is 1/4 PCLK.
8. Applies to the DPLL clock source only. Maximum data rate of 1/4 PCLK still applies. DPLL clock must have a 50% duty cycle.
9. Units in ns.
10. Units in TcPc.

Table 45 lists the Z80230 Read and Write AC characteristics.

Table 45. Z80230 AC Characteristics

No	Symbol	Parameter	10 MHz Min.	10 MHz Max.	16 MHz Min.	16 MHz Max	Notes
1	TwAS	$\overline{\text{AS}}$ Low Width	30		20		8
2	TdDS (AS)	$\overline{\text{DS}}$ Rise to $\overline{\text{AS}}$ Fall Delay	10		10		1, 8
3	TsCS0 (AS)	$\overline{\text{CS0}}$ to $\overline{\text{AS}}$ Rise Setup Time	0		0		1, 8
4	ThCS0 (AS)	$\overline{\text{CS0}}$ to $\overline{\text{AS}}$ Rise Hold Time	20		15		1, 8
5	TsCS1 (DS)	CS1 to $\overline{\text{DS}}$ Fall Setup Time	50		35		1, 8
6	ThCS1 (DS)	CS1 to $\overline{\text{DS}}$ Rise Hold Time	20		10		1, 8
7	TsIA (AS)	$\overline{\text{INTACK}}$ to $\overline{\text{AS}}$ Rise Setup Time	10		10		8
8	ThIA (AS)	$\overline{\text{INTACK}}$ to $\overline{\text{AS}}$ Rise Hold Time	125		100		8
9	TsRWR (DS)	R/$\overline{\text{W}}$ (Read) to $\overline{\text{DS}}$ Fall Setup Time	50		35		8
10	ThRW (DS)	R/$\overline{\text{W}}$ to $\overline{\text{DS}}$ Rise Hold Time	0		0		8
11	TsRWW (DS)	R/$\overline{\text{W}}$ (Write) to $\overline{\text{DS}}$ Fall Setup Time	0		0		8
12	TdAS (DS)	$\overline{\text{AS}}$ Rise to $\overline{\text{DS}}$ Fall Delay	20		15		8

Table 45. Z80230 AC Characteristics (Continued)

			10 MHz		16 MHz		
No	**Symbol**	**Parameter**	**Min.**	**Max.**	**Min.**	**Max**	**Notes**
13	TwDSI	$\overline{DS}$ Low Width	125		80		8
14	TrC	Valid Access Recovery Time	4		4		2, 9
15	TsA (AS)	Address to $\overline{AS}$ Rise Setup Time	10		10		1, 8
16	ThA (AS)	Address to $\overline{AS}$ Rise Hold Time	20		10		1, 8
17	TsDW (DS)	Write Data to $\overline{DS}$ Fall Setup Time	10		10		8
18	ThDW (DS)	Write Data to $\overline{DS}$ Rise Hold Time	0		0		8
19	TdDS (DA)	$\overline{DS}$ Fall to Data Active Delay	0		0		8
20	TdDSr (DR)	$\overline{DS}$ Rise to Read Data Not Valid Delay	0		0		8
21	TdDSf (DR)	DS Fall to Data Active Delay		120		70	8
22	TdAS (DR)	$\overline{AS}$ Rise to Read Data Valid Delay		190		110	8
23	TdDS (DRz)	$\overline{DS}$ Rise to Read Data Float Delay		35		20	3, 8
24	TdA (DR)	Address Required Valid to Read Data Valid Delay		210		100	
25	TdDS (W)	$\overline{DS}$ Fall to Wait Valid Delay		160		60	4, 8
26	TdDSf (REQ)	$\overline{DS}$ Fall to $\overline{W}/\overline{REQ}$ Not Valid Delay		160		60	8
27	TdDSr (REQ)	$\overline{DS}$ Fall to $\overline{DTR}/\overline{REQ}$ Not Valid Delay		4		4	9
28	TdAS (INT)	$\overline{AS}$ Rise to $\overline{INT}$ Valid Delay		500		175	
29	TdAS (DSA)	$\overline{AS}$ Rise to $\overline{DS}$ Fall (Acknowledge) Hold Time	225		50		5
30	TsDSA	$\overline{DS}$ (Acknowledge) Low Width	125		75		8
31	TdDSA (DR)	$\overline{DS}$ Fall (Acknowledge) to Read Data Valid Delay	120		70		8
32	TsIEI (DSA)	IEI to $\overline{DS}$ Fall (Acknowledge) Setup time	80		50		8
33	ThIEI (DSA)	IEI to $\overline{DS}$ Rise (Acknowledge) Hold Time	0		0		8

Table 45. Z80230 AC Characteristics (Continued)

			10 MHz		16 MHz		
No	**Symbol**	**Parameter**	**Min.**	**Max.**	**Min.**	**Max**	**Notes**
34	TdIEI (IEO)	IEI to IEO Delay		90		45	8
35	TdAS (IEO)	$\overline{AS}$ Rise to IEO Delay		175		80	6
36	TdDSA (INT)	$\overline{DS}$ Fall (Acknowledge) to $\overline{INT}$ Inactive Delay		450		200	4, 8
37	TdDS (ASQ)	$\overline{DS}$ Rise to $\overline{AS}$ Fall Delay for No Reset	15		10		8
38	TdASQ (DS)	$\overline{AS}$ Rise to $\overline{DS}$ Fall Delay for No Reset	15		10		8
39	TwRES	AS and DS Coincident Low for Reset7	100		75		8
40	TwPCl	PCLK Low Width	40	100	26	1000	8
41	TwPCh	PCLK High Width	40	1000	26	1000	8
42	TcPc	PCLK Cycle Time	100	2000	61	2000	8
43	TrPC	PCLK Rise Time		10		5	8
44	TfPC	PCLK Fall Time		10		5	8

Notes:

1. Parameter does not apply to Interrupt Acknowledge transactions.
2. Parameter applies only between transactions involving the ESCC.
3. Float delay is defined as the time required for a ±0.5 V change in the output with a maximum DC load and a minimum AC load.
4. Open-drain output, measured with open-drain test load.
5. Parameter is system-dependent. For any Zilog ESCC in the daisy chain. TdAS (DSA) must be greater than the sum of TdAS (IEO) for the highest priority device in the daisy chain. TsIEI (DSA) for the Zilog ESCC, and TdIEI (IEO) for each device separating them in the daisy chain.
6. Parameter applies only to a Zilog ESCC pulling INT Low at the beginning of the Interrupt Acknowledge transaction.
7. Internal circuitry allows for the reset provided by the Z8® to be recognized as a reset by the Z-ESCC. All timing references assume 2.0 V for a 1 and 0.8 V for a logic 0.
8. Units in ns.
9. Units inTcPc

Figure 28 displays the Z80230 system timing diagram.

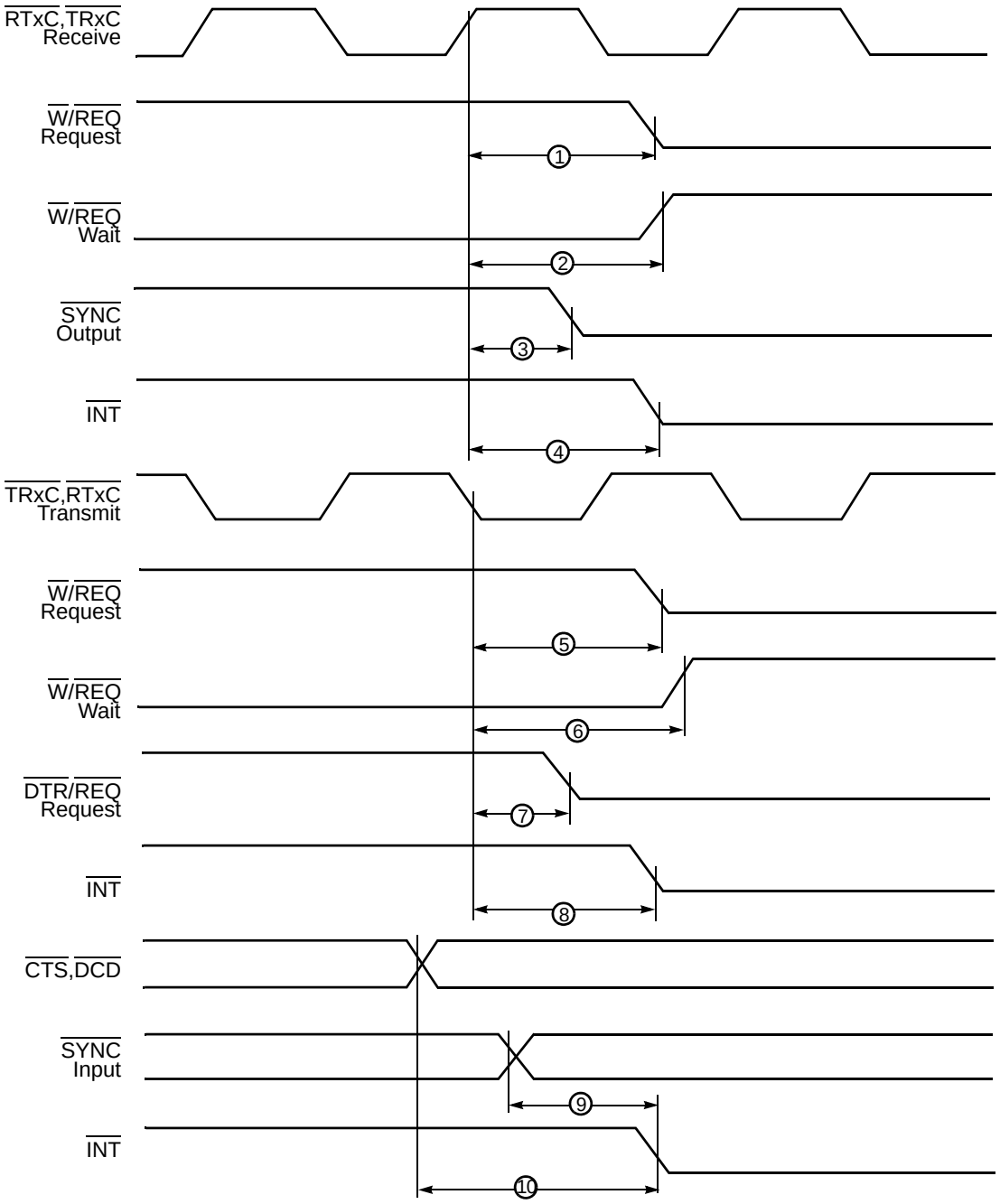


Figure 28. Z80230 System Timing Diagram

Table 46 lists the Z80230 system timing parameter details.

Table 46. Z80230 System Timing Table

No.	Symbol	Parameter	10 MHz		16 MHz		Notes
			Min.	Max.	Min.	Max.	
1	TdRXC (REQ)	RxC High to W/REQ Valid	13	17	13	17	2, 5
2	TdRXC (W)	RxC High to Wait Inactive	13	19	13	19	1, 2, 5
3	TdRXC (SY)	RxC High to SYNC Valid	9	12	9	12	2, 5
4	TdRXC (INT), Z80230	RxC High to INT Valid	13 2	17 3	13 2	17 3	1, 2, 4
5	TdTXC (REQ)	TxC Low to W/REQ Valid	11	14	11	14	3, 5
6	TdTXC (W)	TxC Low to Wait Inactive	8	14	8	14	1, 3, 5
7	TdTXC (DRQ)	TxC Low to DTR/REQ Valid					3, 5
8	TdTXC (INT), Z80230	TxC Low to INT Valid	7 2	9 3	7 2	9 3	1, 3, 4
9	TdSY (INT)	SYNC to INT Valid	2 +2	6 +3	2 +2	6 +3	1, 5
10	TdEXT (INT), Z80230	DCD or CTS to INT Valid	2	3	3	8	1, 4

Notes:
1. Open-drain output, measured with open-drain test load.
2. RxC is RTxC or TRxC, whichever is supplying the receive clock.
3. TxC is TRxC or RTxC, whichever is supplying the transmit clock.
4. Units equal to AS.
5. Units equal to TcPc.

Z85230/L AC Characteristics

Figure 29 on page 88 displays the Z85230/L Read and Write Timing Diagram. Figure 30 on page 89 displays the Z85230/L Reset Timing Diagram. Figure 31 on page 89 displays the Z85230/L Interrupt Acknowledge Timing Diagram. Figure 32 on page 89 displays the Z85230/L Cycle Timing Diagram.

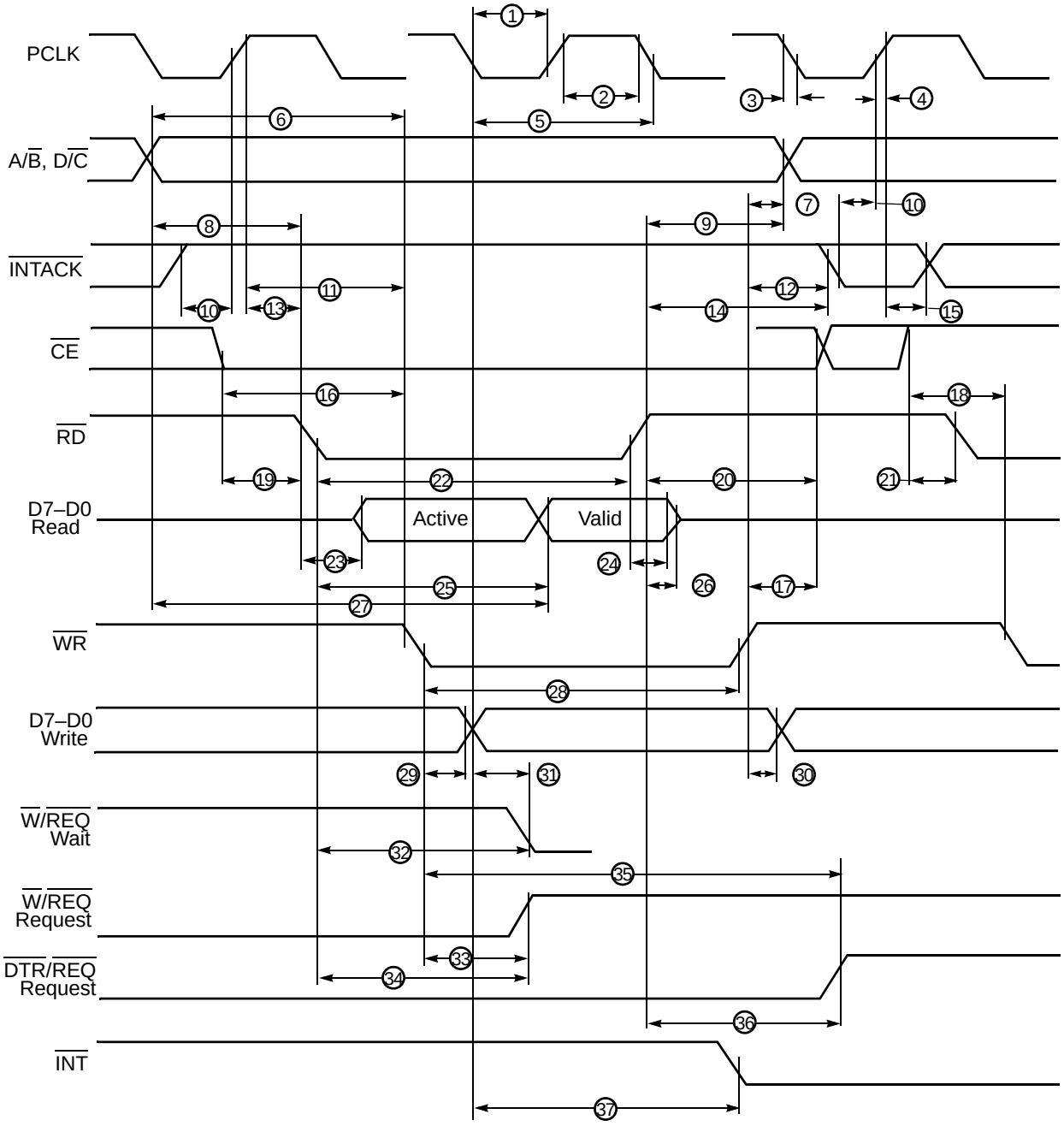


Figure 29. Z85230/L Read/Write Timing Diagram

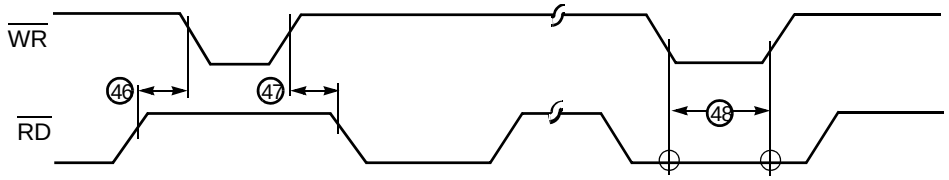


Figure 30. Z85230/L Reset Timing Diagram

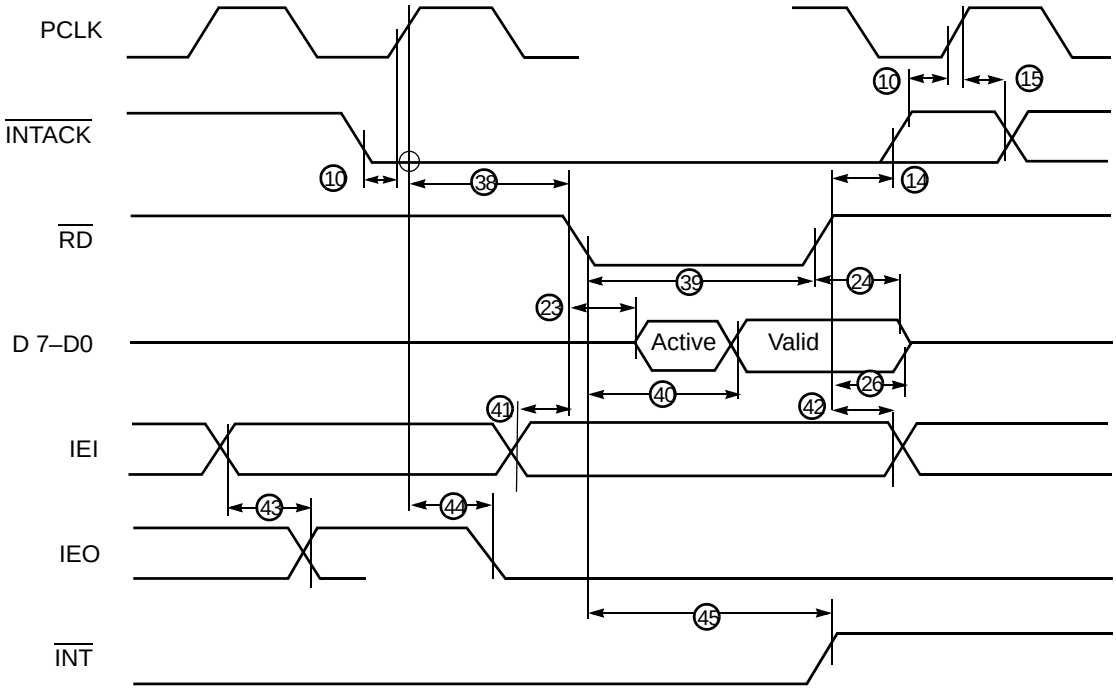


Figure 31. Z85230/L Interrupt Acknowledge Timing Diagram

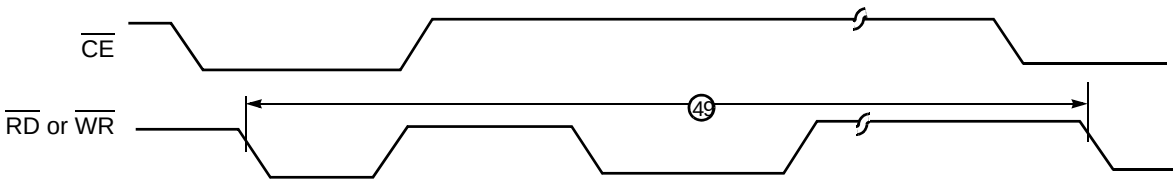


Figure 32. Z85230/L Cycle Timing Diagram

Table 47 lists the Z85230/L Read and Write AC characteristics details.

Table 47. Z85230/L AC Characteristics (20MHz applies only to Z85230)

No	Symbol	Parameter	8.5 MHz		10 MHz		16 MHz		20 MHz		Notes
			Min	Max	Min	Max	Min	Max	Min	Max	
1	TwPCl	PCLK Low Width	45	1000	40	1000	26	1000	22	1000	6
2	TxPCh	PCLK High Width	45	1000	40	1000	26	1000	22	1000	6
3	TfPC	PCLK Fall Time		10		10		5		5	6
4	TrPC	PCLK Rise Time		10		10		5		5	6
5	TcPc	PCLK Cycle Time	118	2000	100	2000	61	2000	50	2000	6
6	TsA	Address to $\overline{WR}$ fall Setup Time	66		50		35		30		6
7	ThA (WR)	Address to $\overline{WR}$ Rise Hold Time	0		0		0		0		6
8	TsA (RD)	Address to $\overline{RD}$ Fall Setup Time	66		50		35		30		6
9	ThA (RD)	Address to $\overline{RD}$ Rise Hold Time	0		0		0		0		6
10	TsIA (PC)	$\overline{INTACK}$ to PCLK Rise Setup Time	20		20		15		15		6
11	TsIAi (WR)	$\overline{INTACK}$ to $\overline{WR}$ Fall Setup Time	140		130		70		65		1, 6
12	ThIA (WR)	$\overline{INTACK}$ to $\overline{WR}$ Rise Hold Time	0		0		0		0		6
13	TsIAi (RD)	$\overline{INTACK}$ to $\overline{RD}$ Fall Setup Time	140		130		70		65		1, 6
14	ThIA (RD)	$\overline{INTACK}$ to $\overline{RD}$ Rise Hold Time	0		0		0		0		6
15	ThIA (PC)	$\overline{INTACK}$ to PCLK Rise Hold Time	38		30		15		15		6
16	TsCEI (WR)	$\overline{CE}$ Low to $\overline{WR}$ Fall Setup Time	0		0		0		0		6
17	ThCE (WR)	$\overline{CE}$ to $\overline{WR}$ Rise Hold Time	0		0		0		0		6

Table 47. Z85230/L AC Characteristics (20MHz applies only to Z85230) (Continued)

No	Symbol	Parameter	8.5 MHz		10 MHz		16 MHz		20 MHz		Notes
			Min	Max	Min	Max	Min	Max	Min	Max	
18	TsCEh (WR)	$\overline{CE}$ High to $\overline{WR}$ Fall Setup Time	58		58		38		25		6
19	TsCEl (RD)	$\overline{CE}$ Low to $\overline{RD}$ Fall Setup Time	0		0		0		0		1, 6
20	ThCE ((RD)	$\overline{CE}$ to $\overline{RD}$ Rise Hold Time	0		0		0		0		1, 6
21	TsCEh (RD)	$\overline{CE}$ High to $\overline{RD}$ Fall Setup Time	58		50		30		25		1, 6
22	TwRDl	$\overline{RD}$ Low Width	145		125		70		65		1, 6
23	TdRD (DRA)	$\overline{RD}$ Fall to Read Data Active Delay	0		0		0		0		6
24	TdRDr (DR)	$\overline{RD}$ Rise to Data Not Valid Delay	0		0		0		0		6
25	TdRDl	$\overline{RD}$ Fall to Read Data Valid Delay		135		120		70		65	6
26	TdRD (DRz)	$\overline{RD}$ Rise to Read Data Float Delay		38		35		30		30	6
27	TdA (DR)	Addr to Read Data Valid Delay		210		180		100		90	6
28	TwWRl	$\overline{WR}$ Low Width	145		125		75		65		6
29	TdWR (DW)	$\overline{WR}$ Fall to Write Data Valid Delay		20		20		20		20	6
30	ThDW (WR)	Write Data to $\overline{WR}$ Rise Hold Time	0		0		0		0		6
31	TdWR (W)	$\overline{WR}$ Fall to $\overline{Wait}$ Valid Delay		168		100		50		50	3, 6
32	TdRD (W)	$\overline{RD}$ Fall to Wait Valid Delay		168		100		50		50	3, 6
33	TdWRf (REQ)	$\overline{WR}$ Fall to $\overline{W}$/$\overline{REQ}$ not Valid Delay		168		100		50 60		50	6 8
34	TdRDf (REQ)	$\overline{RD}$ Fall to $\overline{WR}$/ $\overline{REQ}$ Not Valid Delay		168		100		50 60		50	5,6 8

Table 47. Z85230/L AC Characteristics (20MHz applies only to Z85230) (Continued)

No	Symbol	Parameter	8.5 MHz		10 MHz		16 MHz		20 MHz		Notes
			Min	Max	Min	Max	Min	Max	Min	Max	
35a	TdWRr (REQ)	$\overline{WR}$ Fall to $\overline{DTR}$/ $\overline{REQ}$ Not Valid		4		4		4		4	7
35b	TdWRr (REQ)	$\overline{WR}$ Fall to $\overline{DTR}$/ $\overline{REQ}$ Not Valid		168		100		50 60		50	5, 6 8
36	TdRDr (REQ)	$\overline{RD}$ Rise to $\overline{DTR}$/ $\overline{REQ}$ Not Valid Delay		NA		NA		NA		NA	6
37	TdPC (INT)	PCLK Fall to $\overline{INT}$ Valid Delay		500		320		175		160	6
38	TdIAi (RD)	$\overline{INTACK}$ to $\overline{RD}$ Fall (ACK) Delay	145		90		50		45		4, 6
39	TwRDA	$\overline{RD}$ (Acknowledge) Width	145		125		75		65		6
40	TdRDA (DR)	$\overline{RD}$ Fall (ACK) to Read Data Valid Delay	135		120		70		60		6
41	TsIEI (RDA)	IEI to $\overline{RD}$ Fall (ACK) Setup Time	95		95		50 60		45		6 8
42	ThIEI (RDA)	IEI to $\overline{RD}$ Rise (Ack) Hold Time	0		0		0		0		6
43	TdIEI (IEO)	IEI to IEO Delay Time		95		90		45		40	6
44	TdPC (IEO)	PCLK Rise to IEO Delay		195		175		80		80	6
45	TdRDA (INT)	$\overline{RD}$ Fall to $\overline{INT}$ Inactive Delay		480		320		200		180	3, 6
46	TdRD (WRQ)	$\overline{RD}$ Rise to $\overline{WR}$ Fall Delay for No Reset	15		15		10		10		6
47	TdWRQ (RD)	$\overline{WR}$ Rise to $\overline{RD}$ Fall Delay for No Reset[6]	15		15		10		10		6
48	TwRES	$\overline{WR}$ and $\overline{RD}$ Low for Reset	145		100		75		65		6

Table 47. Z85230/L AC Characteristics (20MHz applies only to Z85230) (Continued)

No	Symbol	Parameter	8.5 MHz		10 MHz		16 MHz		20 MHz		Notes
			Min	Max	Min	Max	Min	Max	Min	Max	
49	Trc	Valid Access Recovery Time	4		4		4		4		2, 7

Notes:
1. Parameter does not apply to Interrupt Acknowledge transactions.
2. Parameter applies only between transactions involving the ESCC.
3. Open-drain output, measured with open-drain test load.
4. Parameter is system-dependent. For any ESCC in the daisy chain, TdIAi (RD) must be greater than the sum of TdPC (IEO) for the highest priority device in the daisy chain. TsIEI (RDA) for the ESCC and TdIEI (IEO) for each device separating them in the daisy chain.
5. Parameter applies to enhanced Request mode only (WR7' bit 4=1)
6. Units in ns.
7. Units in TcPc.
8. Applies to 8523L (3V version) only

Figure 33 displays the Z85230/L General Timing Diagram

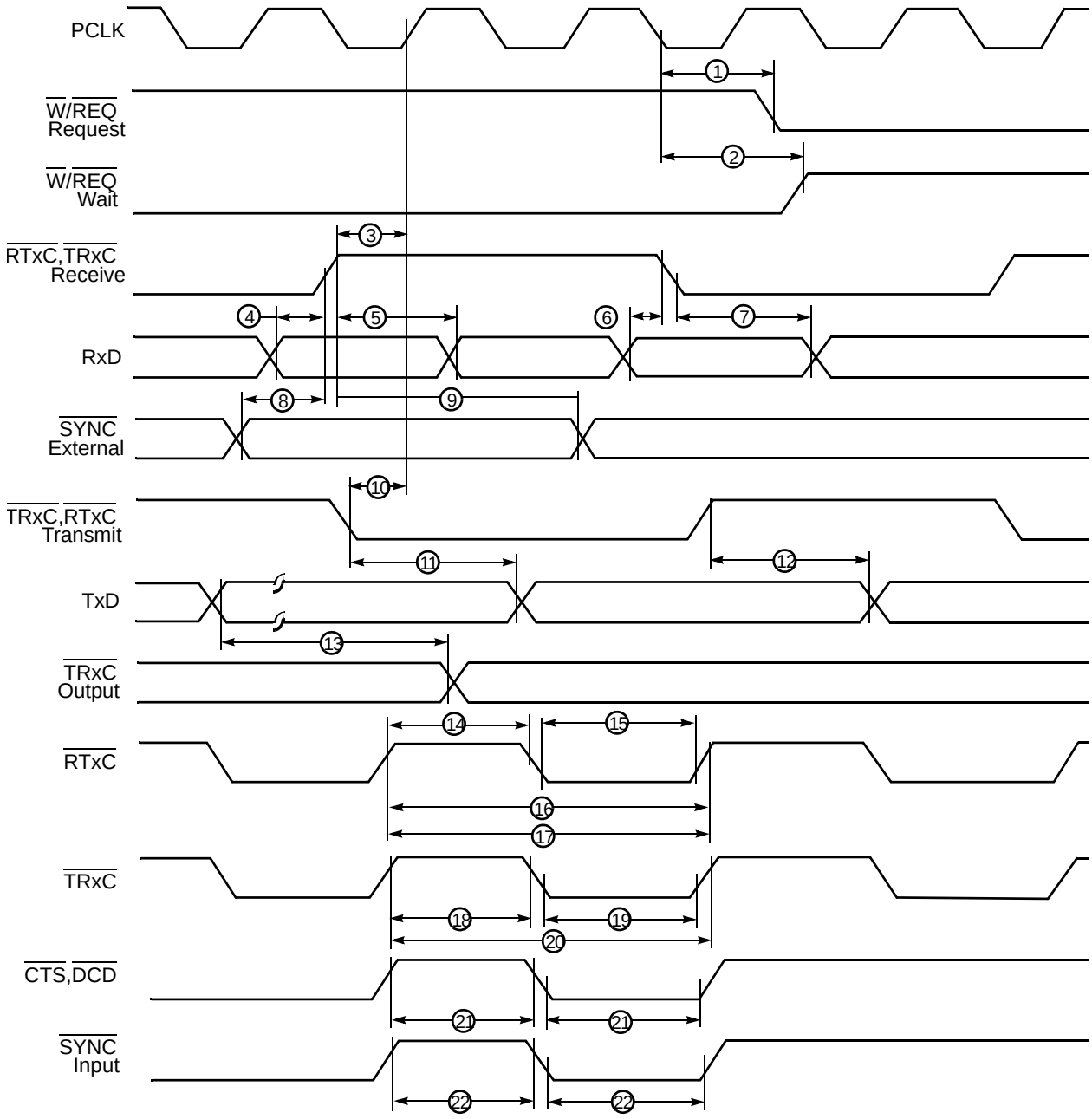


Figure 33. Z85230/L General Timing Diagram

Table 48 lists the Z85230/L general timing characteristics details. Table 49 on page 98 lists the Z85230/L Read/Write Timing characteristics details.

Table 48. Z85230/L General Timing Table (20MHz applies only to Z85230)

No	Symbol	Parameter	8.5 MHz		10 MHz		16 MHz		20 MHz		
			Min	Max	Min	Max	Min	Max	Min	Max	Notes
1	TdPC (REQ)	PCLK to $\overline{W}/\overline{REQ}$ Valid		250		200		80		70	9
2	TdPC (W)	PCLK to Wait Inactive		350		300		180		170	9
3	TsRXC (PC)	RxC to PCLK Setup Time	NA		NA		NA		NA		1, 4, 9
4	TsRXD (RXCr)	RxD to RXC Setup Time		0		0		0		0	1, 9
5	ThRXD (RxCr)	RxD to RXC Hold Time	150		125		50		45		1, 9
6	TsRXD (RXCf)	RxD to RXC Setup Time	0		0		0		0		1, 5, 9
7	ThRXD (RXCf)	RXD to RXC Hold Time	150		125		50		45		1, 5, 9
8	TsSY (RXC)	$\overline{SYNC}$ to RXC Setup Time	–200		–150		–100		–90		1, 9
9	ThSY (RXC)	$\overline{SYNC}$ to RXC Hold Time	5		5		5		5		1, 10
10	TsTXC (PC)	TxC to PCLK Setup Time[2,4]	NA		NA		NA		NA		
11	TdTXCf (TXD)	TxC to TxD Delay		190		150		80		70	2, 9
12	TdTxCr (TXD)	TxC to TxD Delay		190		150		80		70	2, 5, 9
13	TdTXD (TRX)	TxD to $\overline{TRxC}$ Delay		200		140		80		70	9
14	TwRTXh	$\overline{RTxC}$ High Width	130		120		80		70		6, 9
15	TwRTXl	$\overline{RTxC}$ Low Width	130		120		80		70		6, 9

Table 48. Z85230/L General Timing Table (20MHz applies only to Z85230) (Continued)

No	Symbol	Parameter	8.5 MHz		10 MHz		16 MHz		20 MHz		
			Min	Max	Min	Max	Min	Max	Min	Max	Notes
16a	TcRTX	$\overline{\text{RTxC}}$ Cycle Time	472		400		244		200		6, 7, 9
16b	TxRX (DPLL)	DPLL Cycle Time Min.	50		50		31		31		7, 8, 9
17	TcRTXX	Crystal Osc. Period	125	1000	100	1000	61	1000	61	1000	3, 9
18	TwRTXh	$\overline{\text{TRxC}}$ High Width	130		120		80		70		5, 9
19	TwTRXI	$\overline{\text{TRxC}}$ Low Width	130		120		80		70		6, 9
20	TcTRX	$\overline{\text{TRxC}}$ Cycle Time	472		400		244		200		6, 7, 9
21	TwEXT	$\overline{\text{DCD}}$ or $\overline{\text{CTS}}$ Pulse Width	200		120		70		60		9
22	TwSY	$\overline{\text{SYNC}}$ Pulse Width	200		120		70		60		9

Notes:
1. RxC is RTxC or TRxC, whichever is supplying the receive clock.
2. TxC is TRxC or RTxC, whichever is supplying the transmit clock.
3. Both RTxC and SYNC have 30 pF capacitors to ground connected to them.
4. Synchronization of RxC to PCLK is eliminated in divide by four operation.
5. Parameter applies only to FM encoding/decoding.
6. Parameter applies only for transmitter and receiver; DPLL and BRG timing requirements are identical to case PCLK requirements.
7. The maximum receive or transmit data rate is 1/4 PCLK.
8. Applies to the DPLL clock source only. Maximum data rate of 1/4 PCLK still applies. DPLL clock must have a 50% duty cycle.
9. Units in ns.
10. Units in TcPc.

Figure 34 displays the Z85230/L System Timing Diagram. Table 49 on page 98 lists the Z85230/L System Timing Characteristics.

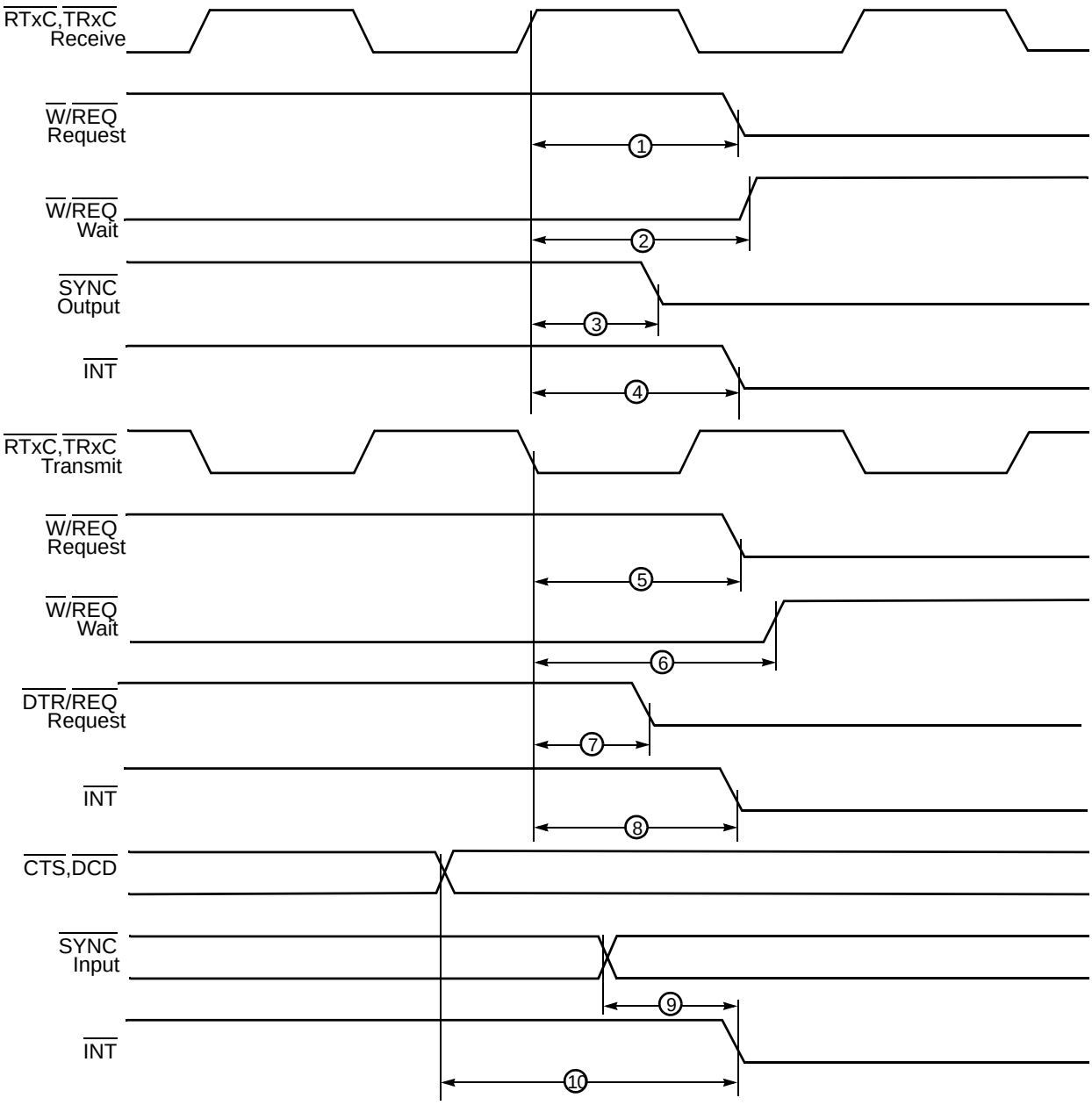


Figure 34. Z85230/L System Timing Diagram

Table 49. Z85230/L System Timing Characteristics (20MHz applies only to Z85230)

No	Symbol	Parameter	8.5 MHz		10 MHz		16 MHz		20 MHZ		
			Min	Max	Min	Max	Min	Max	Min	Max	Notes
1	TdRXC (REQ)	RxC to $\overline{W}/\overline{REQ}$ Valid	13	17	13	17	13	17	13	18	2, 4
2	TdRXC (W)	RxC to $\overline{Wait}$ Inactive	13	17	13	17	13	17	13	18	1, 2, 4
3	TdRXC (SY)	RxC to $\overline{SYNC}$ Valid[2]	4	7	4	7	4	7	4	8	2, 4
4	TdRXC (INT)	RxC to $\overline{INT}$ Valid	15	21	15	21	15	21	15	22	1, 2, 4
5	TdTXC (REQ)	TxC to $\overline{W}/\overline{REQ}$ Valid	8	13	8	13	8	13	8	12	3, 4
6	TdTXC (W)	TxC to $\overline{Wait}$ Inactive	8	14	8	14	8	14	8	15	1, 3, 4
7	TdTXC (DRQ)	TxC to $\overline{DTR}/\overline{REQ}$ Valid	7	10	7	10	7	10	7	11	3, 4
8	TdTXC (INT)	TxC to $\overline{INT}$ Valid	7	13	7	13	7	13	7	14	1, 3, 4
9	TsSY (INT)	$\overline{SYNC}$ to $\overline{INT}$ Valid	2	7	2	7	2	7	2	7	1, 4
10	TdEXT (INT)	$\overline{DCD}$ or $\overline{CTS}$ to $\overline{INT}$ Valid	3	8	3	8	3	8	3	9	1, 4

Notes:
1. Open-drain output, measured with open-drain test load.
2. $\overline{RxC}$ is $\overline{RTxC}$ or $\overline{TRxC}$, whichever is supplying the receive clock.
3. $\overline{TxC}$ is TRxC or RTxC, whichever is supplying the transmit clock.
4. Units in TcPc.

Z80230/Z85230/L Errata

The current revision of Zilog's ESCC has six known bugs. This section identifies these bugs and provides workarounds.

IUS Problem Description

The IUS problem occurs under the following conditions:

- SDLC 10x19 Status FIFO is enabled
- Interrupts on Receive Special Conditions only

This mode is intended for an application where received characters are read by a DMA controller. EOF is treated differently from other special conditions (for example, parity error, overrun error, and CRC error).

When EOF is detected, the following conditions occur:

- A Receive Character Available (RCA) interrupt is generated, rather than the Special Conditions interrupt, as in other operating modes.
- The data FIFO is not locked, as in other operating modes, and is known as the Anti-Lock feature.

This feature allows the processor to service the EOF interrupt with more latency. Immediate attention from the processor is not necessary because the data FIFO is not locked. Incoming data can still be delivered to the Receive FIFO and not get lost. It also allows for operation with no servicing of the interrupt.

When the EOF interrupt (RCA interrupt) is serviced, the processor must use the `Reset Highest IUS` command to clear the EOF.

If an EOF interrupt occurs when another lower priority interrupt is enabled (for example, Ext/Status interrupt is serviced) the `Reset Highest IUS` command issued by the lower priority ISR (to clear out the pending interrupt) can accidentally clear the pending EOF interrupt.

The `Reset Highest IUS` command clears the IP bit related to the EOF (in this mode, the RCA IP bit) regardless of the priorities of the pending interrupts. This action causes errors under the following circumstances:

- Another ESCC interrupt is being serviced (for example, an Ext/Status interrupt for Transmitter Underrun in Full Duplex operation)
- The DMA reads a byte marked with EOF. The corresponding IP bit is set to 1 and the $\overline{\text{INT}}$ line goes Low (highest priority interrupt in the daisy chain).

- The processor does not acknowledge this interrupt because it is servicing another interrupt.
- The processor finishes servicing the other interrupt and uses the `Reset Highest IUS` command.
- The IP bit reset corresponding to the EOF, and the EOF interrupt is lost.

IUS Problem Solutions

The following methods can be used to work around the previously described problems.

- Alternate Operating Mode–A similar operating mode can be used to achieve the same functionality with minimum code modifications. The ESCC must operate in Receive Interrupts on First Character and Special Condition, instead of Receive Interrupt on Special Condition Only.

  In this mode, the Anti-Lock feature is not enabled. The FIFO is locked after the last character of a frame has been transferred, and the interrupt condition does not disappear until after an `Error Reset` command is issued to the ESCC. No `Reset Highest IUS` command can clear any IP bit.

- Daisy Chain– This workaround uses the following two conditions:
  - The EOF interrupt is the highest priority interrupt if only one channel is used.
  - Channel A is the only channel issuing interrupts.

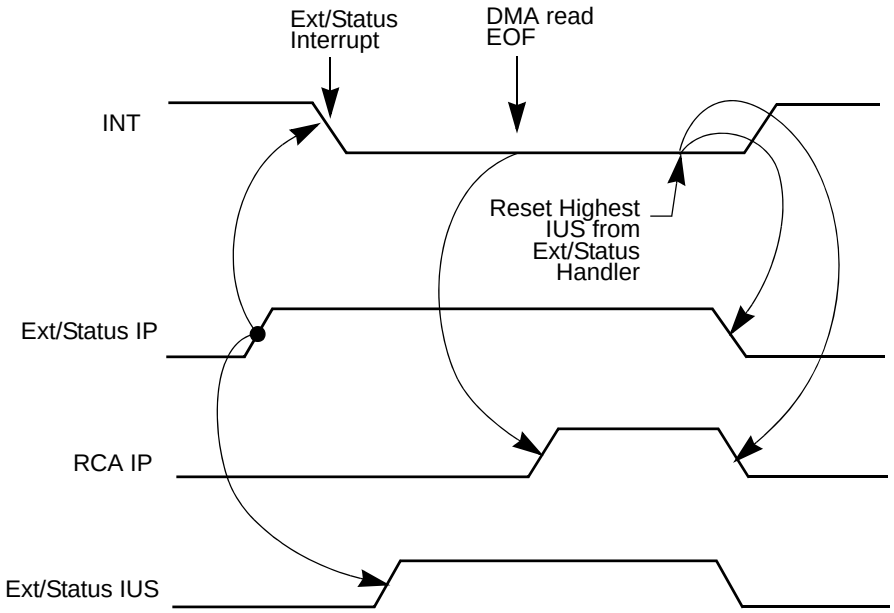
  If both conditions are satisfied, allowing nested interrupts can solve the problem.

  The processor servicing an interrupt on the daisy chain must be interruptible again from another interrupt of higher priority on that same daisy chain.

- RR7 Register–This workaround is applicable if the EOF interrupt is used only to notify another part of the software that there has been another frame received:
  - Read RR7 after issuing the `Reset IUS` command.
  - Check bit 6 of RR7. This bit, when set, indicates that the SDLC frame FIFO contains a valid frame. Although one interrupt might have been lost (IP reset) by the `Reset IUS` command, bit 6 of RR7 always indicates that at least one frame is available in the frame FIFO. If bit 6 of RR7 is 1, notify the concerned part of the software that at least one frame is available in the frame FIFO.

When the SDLC FIFO is enabled and Receive Interrupts on Special Conditions Only is selected, software checks that there is a Receive Character Available interrupt, which is generated by DMA reading an EOF character, and before issuing the `Reset Highest IUS` command. Otherwise, the EOF interrupt conditions are cleared by that command.

Figure 35 displays the procedure for resetting highest IUS.



Resetting highest IUS from lower priority interrupt clears the EOF (RCA) interrupt.

Figure 35. Resetting Highest IUS from Lower Priority

$\overline{\text{RTS}}$ Problem Description

The ESCC (Z80230/Z85230/L) contains a functional problem in Automatic $\overline{\text{RTS}}$ Deactivation (see Figure 36 on page 102).

This mode is intended for SDLC applications where the $\overline{\text{RTS}}$ signal from the ESCC is used to enable a line driver in multi-drop line communications.

Before the frame transmission, $\overline{\text{RTS}}$ is asserted by an `Activate RTS` command (ER5 bit1 equals 0).

After the last data bit of a frame is sent, a Transmit Underrun interrupt is requested. A `Deactivate RTS` command is issued (WR5 bit 1 equals 1) to deactivate the $\overline{\text{RTS}}$ signal to turn off the line driver after the multiple-frame packet is sent.

On the SCC, the processor must monitor the data line to ensure that the frame has been sent before it issues the `Deactivate RTS` command.

On the ESCC, $\overline{\text{RTS}}$ can be programmed to deactivate automatically after the frame is sent. If the following sequence is performed, additional monitoring is not required:

1. Enable Automatic $\overline{\text{RTS}}$ Deactivation (WR7' bit 2 equals 1).

2. Enable the CRC/Flag on Underrun (WR10 bit 2 equals 0).
3. Issue a `Deactivate RTS` command in the Transmit Underrun ISR. The $\overline{RTS}$ signal deactivates automatically after the closing flag disappears.

The `Automatic RTS Deactivation` command works for a single frame and for two consecutive frames back-to-back. This command does not work with more than two back-to-back frames.

In the latter condition, if the `Deactivate RTS` command is issued at the beginning of the `Transmit Underrun` ISR. $\overline{RTS}$ is deactivated after the CRC is gone, but before the closing flag is sent. The final frame is not concluded, and is corrupted.

$\overline{RTS}$ Problem Solutions

A workaround for the $\overline{RTS}$ problem is not to send back-to-back frames. Idle time is inserted between frames.

There is, however, a limitation to this workaround in that the system throughput is reduced by the idle time inserted between the frames.

Figure 36 displays Automatic $\overline{RTS}$ Deactivation.

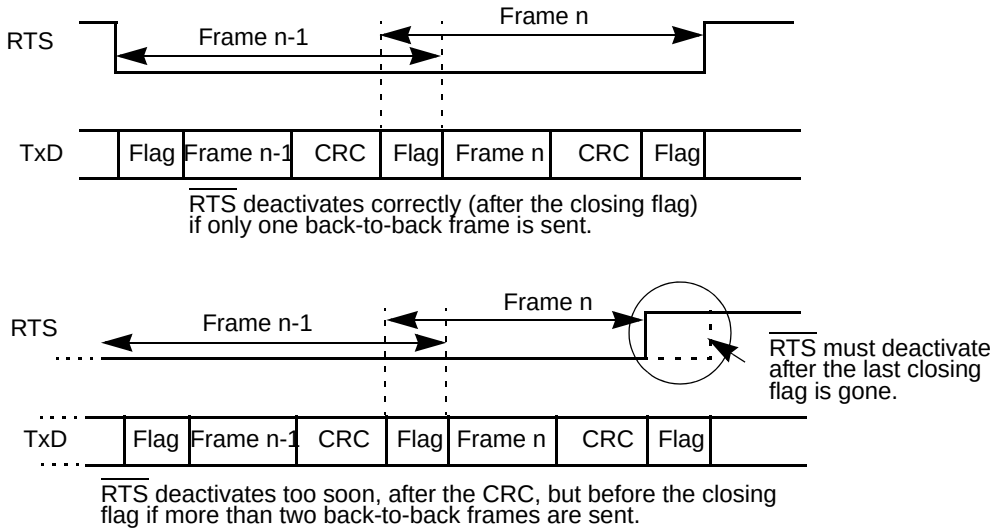


Figure 36. Automatic $\overline{RTS}$ Deactivation

Automatic TxD Forced High Problem Description

If WR10 is programmed with bits 6 and 5 equal to 01 (NRZI), bit 3 equals 1 (Mark Idle) and WR4 bits 5 and 4 equal 10 (SDLC), the TxD pin is forced High after detecting the last bit of the closing flag at the falling edge of TxC. This feature does not work if back-to-

back frames are sent. The TxD output is automatically forced High for eight bit-times and the first byte of the second frame is corrupted. In a multiple-frame transmission, a zero (0) bit is inserted before the opening flag of the second frame.

Automatic TxD Forced High Problem Solutions

Send back-to-back frames in FLAG IDLE mode, because the Automatic TxD Forced High feature creates problems only if all the following conditions are true:

- Back-to-back frame transmission
- NRZI
- Mark Idle

Setting the system in Flag Idle mode (WR10 bit 3 equals 0) in frame transmission allows back-to-back frames to be sent without any data corruption.

SDLC FIFO Overflow Problem Description

In SDLC mode, bit 7 of RR7 (FIFO Overflow status bit) is set if an 11th frame ends while the FIFO is full (that is, ten frames have accumulated in the Status FIFO and have not yet been read by the processor). Under this circumstance, the status FIFO is locked and no data can be written to the Status FIFO until bit 7 of RR7 is reset.

If the ESCC is set up in ANTI-LOCK mode (that is, the SDKC FIFO is used when Receive Interrupts on Special Condition Only is enabled), the only method of resetting bit 7 of RR7(the FIFO Overflow bit) is to reset and set WR15 bit 2 (SDLC FIFO Enable Bit). This action causes the SDLC FIFO to reset and all the SDLC frame information is lost.

With no Anti-Lock feature, the FIFO Overflow status bit is reset if the SDLC FIFO is read.

If the ESCC is in NRZI and Mark Idle in back-to-back frame transmission, (one the FIFO Overflow bit RR7 bit 7) is set, the only method of resetting the status is to reset and set WR15 bit 2. This action causes the SDLC FIFO to reset and the unprocessed frame information stored in the SDLC FIFO is lost.

SDLC FIFO Overflow Problem Solution

Do not use Receive Interrupts on Special Conditions Only and Mark Idle if there is a possibility of Status FIFO Overflow.

Default RR0 Value Problem Description

RR7 bit 7, the Break/Abort status bit, does not always clear after reset.

Default RR0 Value Problem Solution

Ignore the first bit 7 value read from RR0 after reset.

Default RR10 Value Problem Description

RR10 bit 6, the 2 clock missing bit, is sometimes erroneously set to indicate that the DPLL detects a clock edge in two successive tries after hardware reset.

Default RR10 Value Problem Solution

Ignore the first bit 7 value Read from RR10 after reset.

CRC Problem Description

The CRC cannot be interpreted from the Receive FIFO when one or two residue bits are sent. The CRC value is received and checked correctly but is not loaded to the Receive FIFO. The two types of CRC problems are described below:

- Two Residue bits (Residue code is 000)

The last three bytes of the Receive FIFO read:

D7	D6	D5	D4	D3	D2	D1	D0
C5	C4	C3	C2	C1	C0	D9	D8
C15	C14	C13	C12	C11	C10	C9	C8

Bits 6 and 7 of the CRC are lost.

- One Residue Bit (Residue code is 111)

The last three bytes of the Receive FIFO read:

D7	D6	D5	D4	D3	D2	D1	D0
C6	C5	C4	C3	C2	C1	C0	D8
C15	C14	C13	C12	C11	C10	C9	C8

Bit 7 of the CRC is lost.

The CRC is received and loaded into the Receive FIFO in other situations (that is, the 0, 3, 4, 5, 6, and 7 residue bits).

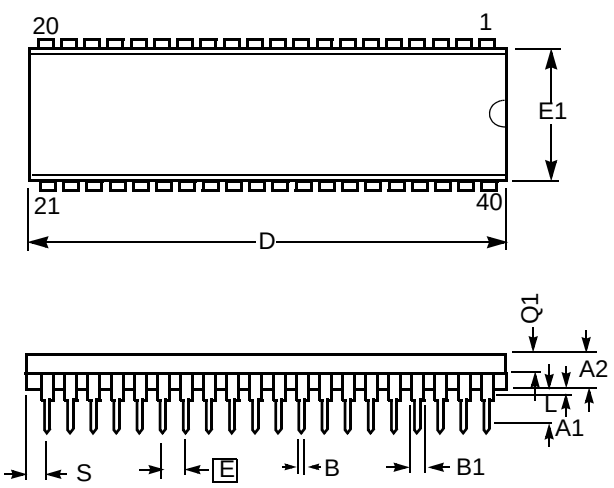
The Residue code, RR1 bits 3, 2, and 1, is reported independently of the number of residue bits sent.

CRC Problem Solution

Ignore the CRC value read from the Receive FIFO if one or two residue bits are sent.

Package Information

Figure 37 displays the 40-pin Dual-Inline Package (DIP).

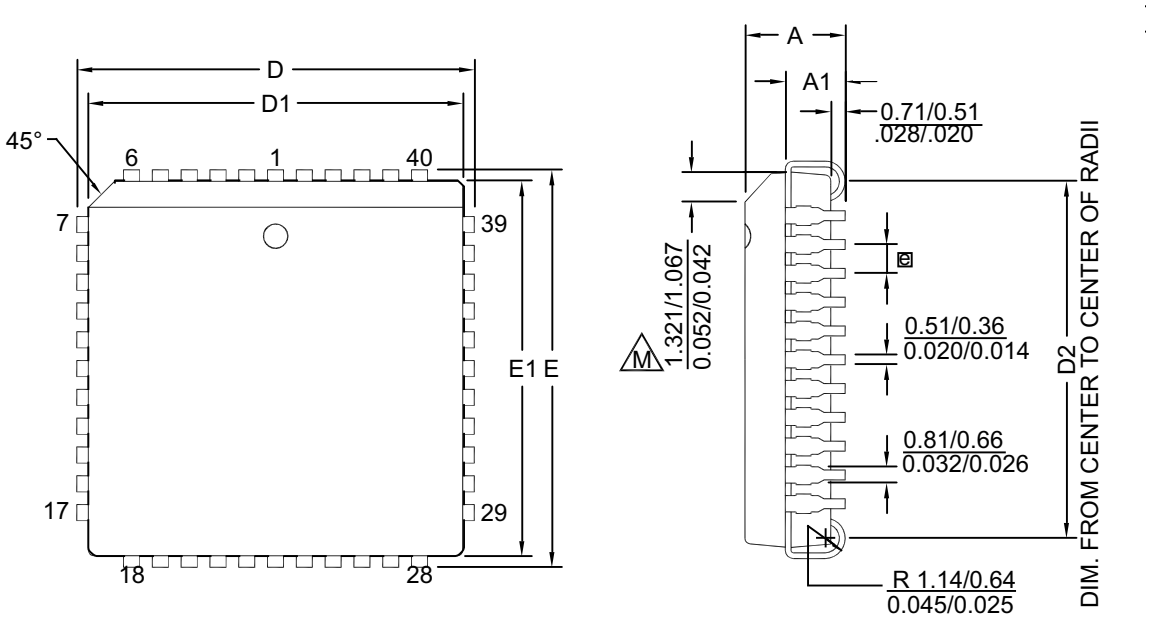


SYMBOL	MILLIMETER		INCH	
	MIN	MAX	MIN	MAX
A1	0.51	0.81	.020	.032
A2	3.25	3.43	.128	.135
B	0.38	0.53	.015	.021
B1	1.02	1.52	.040	.060
C	0.23	0.38	.009	.015
D	52.07	52.58	2.050	2.070
E	15.24	15.75	.600	.620
E1	13.59	14.22	.535	.560
[E]	2.54 TYP		.100 TYP	
eA	15.49	16.51	.610	.650
L	3.18	3.81	.125	.150
Q1	1.52	1.91	.060	.075
S	1.52	2.29	.060	.090

Controlling Dimensions: Inch

Figure 37. 40-Pin DIP Package Diagram

Figure 38 displays the 44-pin Plastic Leaded Chip Carrier (PLCC) package.



SYMBOL	MILLIMETER		INCH	
	MIN	MAX	MIN	MAX
A	4.27	4.57	0.168	0.180
A1	2.41	2.92	0.095	0.115
D/E	17.40	17.65	0.685	0.695
D1/E1	16.51	16.66	0.650	0.656
D2	15.24	16.00	0.600	0.630
e	1.27 BSC		0.050 BSC	

NOTES:
1. CONTROLLING DIMENSION : INCH
2. LEADS ARE COPLANAR WITHIN 0.004".
3. DIMENSION : MM / INCH

Figure 38. 44-Pin PLCC Package Diagram

Ordering Information

Order the required ESCC from Zilog using the following part details. For more information on ordering, consult your local Zilog sales offices. The Zilog website (www.zilog.com) lists all the regional offices and provides additional product information.

Z8523L (3.3V)

Z8523L Available Packages

8 MHz Z8523L	Z8523L08VSG Z8523L08VEG
10 MHz Z8523L	Z8523L10VSG Z8523L10VEG
16 MHz Z8523L	Z8523L16VSG Z8523L16VEG

Z85230 (5V)

Z85230 Available Packages

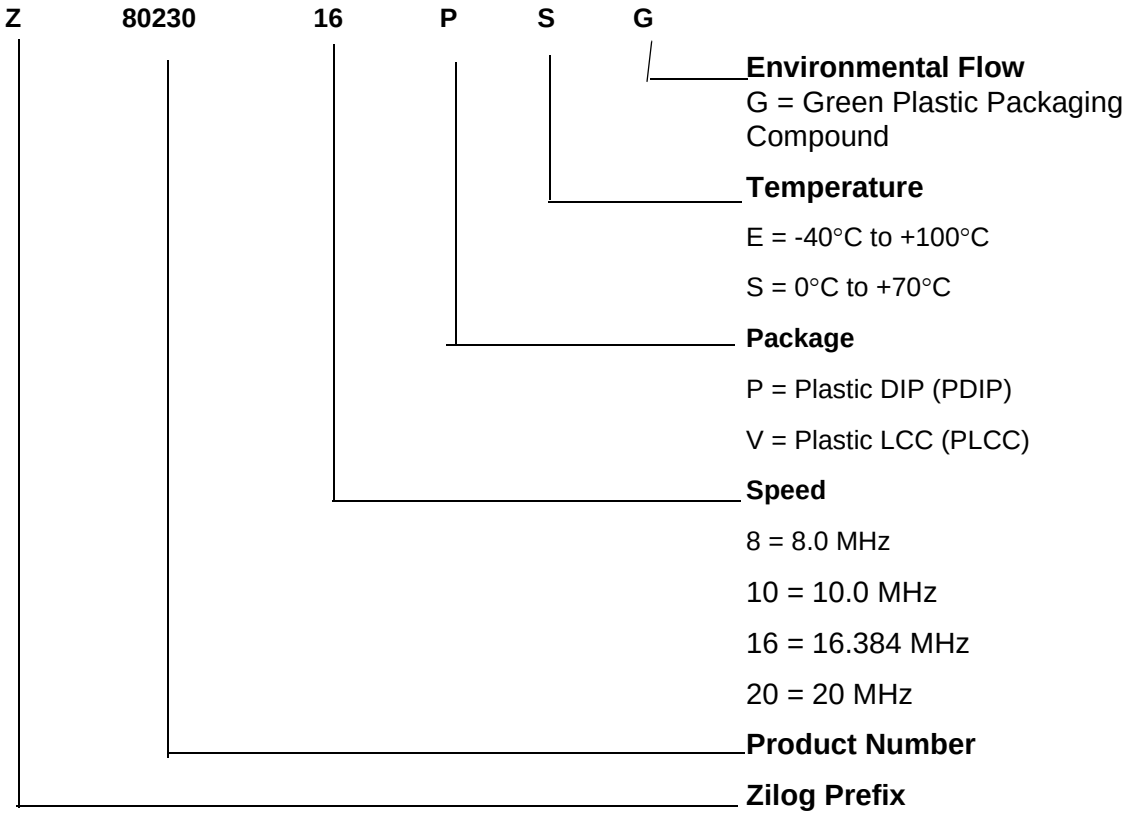
8 MHz Z85230	Z8523008PSG Z8523008VSG Z8523008PEG Z8523008VEG
10 MHz Z85230	Z8523010PSG Z8523010VSG Z8523010PEG Z8523010VEG
16 MHz Z85230	Z8523016PSG Z8523016VSG Z8523016PEG Z8523016VEG
20 MHz Z85230	Z8523020PSG Z8523020VSG

Z80230

Z80230 Available Packages

10 MHz Z80230	Z8023010PSG Z8023010VSG
16 MHz Z80230	Z8023016PSG Z8023016VSG

Part Number Suffix Designation



Customer Support

For answers to technical questions about the product, documentation, or any other issues with Zilog's offerings, please visit Zilog's Knowledge Base at http://www.zilog.com/kb.

For any comments, detail technical questions, or reporting problems, please visit Zilog's Technical Support at http://support.zilog.com.

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