

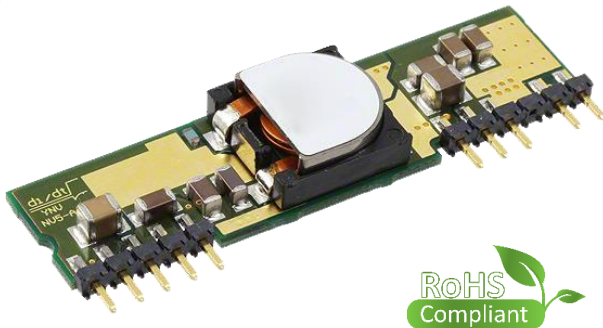


**THE DATASHEET OF  
YNV05T10033-D**



# YNV05T100xy DC-DC Converter

3.0 - 5.5 VDC Input; 0.9 - 3.3 VDC  
Programmable @ 10 A



## Key Features

- RoHS lead-free solder and lead-solder-exempted products are available
- No derating up to 85 °C
- Industry-standard footprint and pinout
- Single-in-Line Package (SIP): 2.0" x 0.575" x 0.28" (50.8 x 14.59 x 7.11 mm)
- Weight: 0.26 oz [7.28 g]
- Synchronous Buck Converter topology
- Start-up into pre-biased output
- No minimum load required
- Output voltage trim +/-10% of Vout (-5% to +10% for 0.9 V output)
- Operating ambient temperature: -40 °C to 85 °C
- Remote output sense
- Remote ON/OFF (Positive or Negative)
- Fixed-frequency operation
- Auto-reset output overcurrent protection
- Auto-reset overtemperature protection
- High reliability, MTBF = TBD million hours
- All materials meet UL94, V-0 flammability rating
- Safety approved to UL/CSA 62368-1 and EN/IEC 62368-1

Bel Power Solutions point-of-load converters are recommended for use with regulated bus converters in an Intermediate Bus Architecture (IBA). The Y-Series YNV05T100XY non-isolated DC-DC converters deliver up to 10 A of output current in an industry-standard through hole single in-line package (SIP). Operating from a 3.0 – 5.5V input, these converters are ideal choices for Intermediate Bus Architectures where point-of-load power delivery is generally a requirement.

The YNV05T100XY converters are available in individual output voltage versions, allowing coverage of the output voltage range from 0.9V to 3.3V. Each version is capable of providing an extremely tight, highly regulated and trimmable output.

The YNV05T100XY converters provide exceptional thermal performance, even in high temperature environments with minimal airflow. No derating is needed up to 85 °C under natural convection conditions. This is accomplished through the use of circuitry, packaging, and processing techniques to achieve ultra-high efficiency and excellent thermal management along with a very sleek body profile.

The sleek body profile and the preclusion of heat sinks minimize impedance to system airflow, thus enhancing cooling for both upstream and downstream devices. The use of 100% automation for assembly, coupled with advanced power electronics and thermal design, results in a product with extremely high reliability.

## Applications

- Intermediate Bus Architectures
- Telecommunications
- Data Communications
- Distributed Power Architectures
- Servers, Workstations

## Benefits

- High efficiency – no heat sink required
- Reduces Total Solution Board Area

## ELECTRICAL SPECIFICATIONS

Conditions:  $T_A = 25\text{ }^\circ\text{C}$ , Airflow = 200 LFM (1 m/s),  $V_{in} = 5\text{ VDC}$ ,  $V_{out} = 0.9 - 3.3\text{ V}$ , unless otherwise specified.

PARAMETER	NOTES	MIN	TYP	MAX	UNITS
<b>ABSOLUTE MAXIMUM RATINGS</b>					
Input Voltage	Continuous	-0.3		6	VDC
Operating Ambient Temperature		-40		85	$^\circ\text{C}$
Storage Temperature		-55		125	$^\circ\text{C}$
<b>FEATURE CHARACTERISTICS</b>					
Switching Frequency			300		kHz
Output Voltage Trim Range	See Trim Equations on page 6 & 7	-10		+10	%
	$V_{OUT} = 0.9\text{ VDC}$	-5		+10	%
Remote Sense Compensation				0.5	VDC
Turn-On Delay Time <sup>1</sup>	Full resistive load				
With $V_{in} = (\text{Converter Enabled, then } V_{in} \text{ applied})$	From $V_{in} = V_{in}(\text{min})$ to $V_o = 0.1 * V_o(\text{nom})$		3.5		ms
With Enable ( $V_{in} = V_{in}(\text{nom})$ applied, then enabled)	From enable to $V_o = 0.1 * V_o(\text{nom})$		3.5		ms
Rise time <sup>1</sup> (Full resistive load)	From $0.1 * V_o(\text{nom})$ to $0.9 * V_o(\text{nom})$		3.5		ms
ON/OFF Control (Positive Logic) <sup>2</sup>	Converter Off	-5		0.8	VDC
	Converter On	2.4		5.5	VDC
ON/OFF Control (Negative Logic) <sup>2</sup>	Converter Off	2.4		5.5	VDC
	Converter On	-5		0.8	VDC
<b>INPUT CHARACTERISTICS</b>					
Operating Input Voltage Range	For $V_{out} > 2.5\text{ V}$	4.5	5.0	5.5	VDC
	For $V_{out} \leq 2.5\text{ V}$	3.0	5.0	5.5	VDC
Input Under Voltage Lockout	Turn-on Threshold		2.05	2.15	VDC
	Turn-off Threshold	1.75	1.9		VDC
Maximum Input Current					
$V_{in} = 4.5\text{V}$ , $I_{out} = 10\text{A}$	$V_{OUT} = 3.3\text{ VDC}$			7.8	ADC
$V_{in} = 3.0\text{V}$ , $I_{out} = 10\text{A}$	$V_{OUT} = 2.5\text{ VDC}$			9	ADC
$V_{in} = 3.0\text{V}$ , $I_{out} = 10\text{A}$	$V_{OUT} = 2.0\text{ VDC}$			7.3	ADC
$V_{in} = 3.0\text{V}$ , $I_{out} = 10\text{A}$	$V_{OUT} = 1.8\text{ VDC}$			6.7	ADC
$V_{in} = 3.0\text{V}$ , $I_{out} = 10\text{A}$	$V_{OUT} = 1.5\text{ VDC}$			5.7	ADC
$V_{in} = 3.0\text{V}$ , $I_{out} = 10\text{A}$	$V_{OUT} = 1.2\text{ VDC}$			4.7	ADC
$V_{in} = 3.0\text{V}$ , $I_{out} = 10\text{A}$	$V_{OUT} = 1.0\text{ VDC}$			4.0	ADC
$V_{in} = 3.0\text{V}$ , $I_{out} = 10\text{A}$	$V_{OUT} = 0.9\text{ VDC}$			3.6	ADC
Input Stand-by Current (Converter disabled)	$V_{in} = 5.0\text{ VDC}$		10		mA
Input No Load Current (Converter enabled)	$V_{in} = 5.5\text{ VDC}$				
	$V_{OUT} = 3.3\text{ VDC}$		90		mA
	$V_{OUT} = 2.5\text{ VDC}$		85		mA
	$V_{OUT} = 2.0\text{ VDC}$		80		mA
	$V_{OUT} = 1.8\text{ VDC}$		75		mA
	$V_{OUT} = 1.5\text{ VDC}$		70		mA
	$V_{OUT} = 1.2\text{ VDC}$		65		mA
	$V_{OUT} = 1.0\text{ VDC}$		60		mA
	$V_{OUT} = 0.9\text{ VDC}$		60		mA
Input Reflected-Ripple Current - $i_s$	See Fig. H for setup. (BW = 20 MHz)		15		$\text{mA}_{P-P}$

OUTPUT CHARACTERISTICS				
Output Voltage Set Point (no load)		-1.5	Vout	+1.5 %Vout
Output Regulation <sup>3</sup>				
Over Line	Vin = 3.0V – 5.5V, Full resistive load		0.2	%Vout
Over Load	From no load to full load		0.4	%Vout
Output Voltage Tolerance	(Overall operating input voltage, resistive load and temperature conditions until end of life )	-3		+3 %Vout
Output Ripple and Noise - 20MHz bandwidth (Fig. H) Over line, load and temperature				
Peak-to-Peak	Vout = 3.3V Full load		40	70 mV <sub>P-P</sub>
Peak-to-Peak	Vout = 0.9V Full load		20	40 mV <sub>P-P</sub>
External Load Capacitance Plus full load (resistive)				
Min ESR > 1mΩ				1,000 μF
Min ESR > 10 mΩ				5,000 μF
Output Current Range		0		10 A
Output Current Limit Inception (I <sub>OUT</sub> )			15	18.5 A
Output Short- Circuit Current (Hiccup mode)	Short=10 mΩ, continuous		3	Arms
DYNAMIC RESPONSE				
Load current change from 5A – 10A, di/dt = 5 A/μS	Co = 100 μF ceramic + 1 μF ceramic		120 <sup>4</sup>	mV
Settling Time (V <sub>OUT</sub> < 10% peak deviation)			40	μs
Unloading current change 10A – 5A, di/dt = -5 A/μS	Co = 100 μF ceramic + 1 μF ceramic		125 <sup>4</sup>	mV
Settling Time (V <sub>OUT</sub> < 10% peak deviation)			40	μs
EFFICIENCY				
Full load (5A)				
	V <sub>OUT</sub> = 3.3 VDC		95.5	%
	V <sub>OUT</sub> = 2.5 VDC		93.5	%
	V <sub>OUT</sub> = 2.0 VDC		92.0	%
	V <sub>OUT</sub> = 1.8 VDC		91.5	%
	V <sub>OUT</sub> = 1.5 VDC		90.0	%
	V <sub>OUT</sub> = 1.2 VDC		88.5	%
	V <sub>OUT</sub> = 1.0 VDC		86.5	%
	V <sub>OUT</sub> = 0.9 VDC		85.0	%

Notes:

- <sup>1</sup> Note that start-up time is the sum of turn-on delay time and rise time.
- <sup>2</sup> The converter is on if ON/OFF pin is left open.
- <sup>3</sup> Trim resistor connected across the GND (pin 5) and TRIM pins of the converter.
- <sup>4</sup> See waveforms for dynamic response and settling time for different output voltages.

## OPERATIONS

### Input and Output Impedance

YNV05T100XY converters should be connected via a low impedance to the DC power source. In many applications, the inductance associated with the distribution from the power source to the input of the converter can affect the stability of the converter. It is recommended to use decoupling capacitors (minimum 47 $\mu$ F) placed as close as possible to the converter input pins in order to ensure stability of the converter and reduce input ripple voltage. Internally, the converter has 52 $\mu$ F (low ESR ceramics) of input capacitance.

In a typical application, low - ESR tantalum or POS capacitors will be sufficient to provide adequate ripple voltage filtering at the input of the converter. However, very low ESR ceramic capacitors 47 $\mu$ F-100 $\mu$ F are recommended at the input of the converter in order to minimize the input ripple voltage. They should be placed as close as possible to the input pins of the converter.

The YNV05T100xy has been designed for stable operation with or without external output capacitance. Low ESR ceramic capacitors placed as close as possible to the load (Min 47 $\mu$ F) are recommended for improved transient performance and lower output voltage ripple.

It is important to keep low resistance and low inductance PCB traces when the connecting load to the output pins of the converter in order to maintain good load regulation.

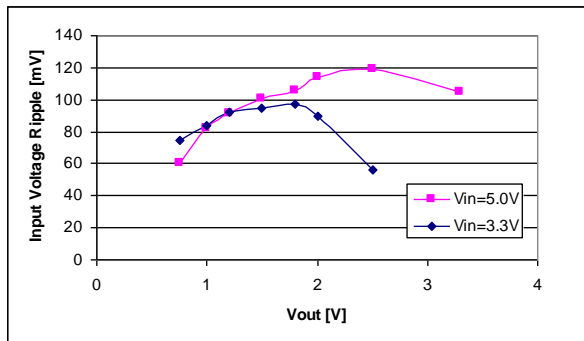


Fig. A: Input Voltage Ripple,  $C_{IN} = 4 \times 47 \mu F$  ceramic.

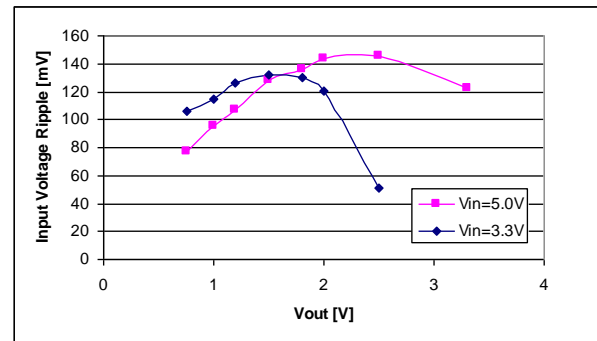


Fig. B: Input Voltage Ripple,  $C_{IN} = 470 \mu F$  polymer +  $2 \times 47 \mu F$  ceramic

Fig. A shows input voltage ripple for various output voltages using four 47 $\mu$ F input ceramic capacitors. The same plot is shown in Fig. B with one 470 $\mu$ F polymer capacitor (6TPB470M from Sanyo) in parallel with two 47 $\mu$ F ceramic capacitors at full load.

### ON/OFF (Pin 10)

The ON/OFF pin is used to turn the converter on or off remotely via a system signal. There are two remote control options available, positive logic (standard option) and negative logic, and both are referenced to GND. Typical connections are shown in Fig. C.

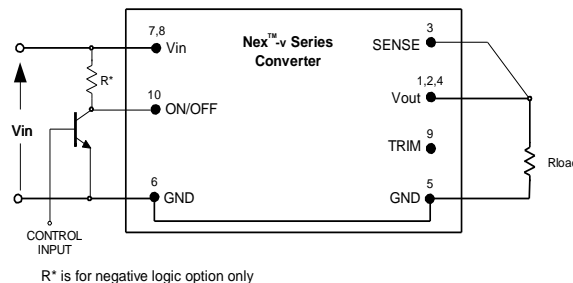


Fig. C: Circuit configuration for ON/OFF function.

The positive logic version turns the converter on when the ON/OFF pin is at a logic high or left open, and turns converter off when at a logic low or shorted to GND.

The negative logic version turns the converter on when the ON/OFF pin is at a logic low or left open, and turns the converter off when the ON/OFF pin is at a logic high or connected to Vin.

ON/OFF pin is internally pulled-up to  $V_{in}$  for a positive logic version and pulled-down for a negative logic version. A TTL or CMOS logic gate, open collector (open drain) transistor can be used to drive ON/OFF pin. When using open collector (open drain) transistor with a negative logic option, add a pull-up resistor ( $R^*$ ) of 10K to  $V_{in}$  as shown in Fig. C. External pull-up resistor ( $R^*$ ) can be increased to 20K if minimum input voltage is more than 4.5V. This device must be capable of:

- sinking up to 0.6 mA at a low level voltage of  $\leq 0.8$  V
- sourcing up to 0.25 mA at a high logic level of 2.3V – 5.5V

### Remote Sense (Pin 3)

The remote sense feature of the converter compensates for voltage drops occurring only between  $V_{out}$  of the converter and the load. The SENSE (Pin 3) pin should be connected at the load or at the point where regulation is required (see Fig. D). There is no sense feature on the output GND return pin, where a solid ground plane is recommended to provide a low voltage drop.

If remote sensing is not required, the SENSE pin must be connected to the  $V_{out}$  to ensure the converter will regulate at the specified output voltage. If these connections are not made, the converter will deliver an output voltage that is slightly higher than the specified value.

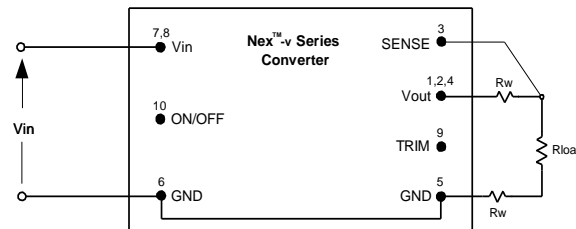


Fig. D: Remote sense circuit configuration.

Because the sense lead carries minimal current, large trace on the end-user board is not required. However, the sense trace should be located close to a ground plane to minimize system noise and insure optimum performance.

When utilizing the remote sense feature, care must be taken not to exceed the maximum allowable output power capability of the converter, equal to the product of the nominal output voltage and the allowable output current for the given conditions.

When using remote sense, the output voltage of the converter can be increased up to 0.5 V above the sense point voltage in order to maintain the required voltage across the load. Therefore, the designer must, decrease the maximum current (originally obtained from the derating curves) by the same percentage to ensure the converter's actual output power remains at or below the maximum allowable output power.

### Output Voltage Adjust / TRIM (Pin 9)

The converter's output voltage can be adjusted up 10% or down 10% for  $V_{out} \geq 1.0$  V, and +10%/-5% for  $V_{out} = 0.9$  V relative to the rated output voltage by the addition of an externally connected resistor.

The TRIM pin should be left open if trimming is not being used. To minimize noise pickup, a 0.1 uF capacitor is connected internally between the TRIM and Ground.

To trim up the output voltage, refer to Fig. E. A trim resistor ( $R_{T-INCR}$ ) should be connected between the TRIM pin (Pin 9) and output GND pin (Pin 5), with a value of:

For  $V_{O-NOM} \geq 1.2V$ ,

$$R_{T-INCR} = \frac{24.08}{(V_{O-REQ} - V_{O-NOM})} - R_{INT} \quad [k\Omega]$$

For  $V_{O-NOM} = 1.0V, 0.9V$ ,

$$R_{T-INCR} = \frac{21.07}{(V_{O-REQ} - V_{O-NOM})} - R_{INT} \quad [k\Omega]$$

where,

$R_{T-INC}$  = Required value of trim-up resistor [k $\Omega$ ]

$V_{O-REQ}$  = Desired (trimmed) output voltage [V]

$V_{O-NOM}$  = Nominal output voltage [V]

$R_{INT}$  = Internal series resistor according to Table A below [k $\Omega$ ]

Table A: Internal series Resistor R <sub>INT</sub>								
<b>V<sub>O-NOM</sub> [V]</b>	3.3	2.5	2.0	1.8	1.5	1.2	1.0	0.9
<b>R<sub>INT</sub> [k<math>\Omega</math>]</b>	59	78.7	100	100	100	59	30.1	5.11

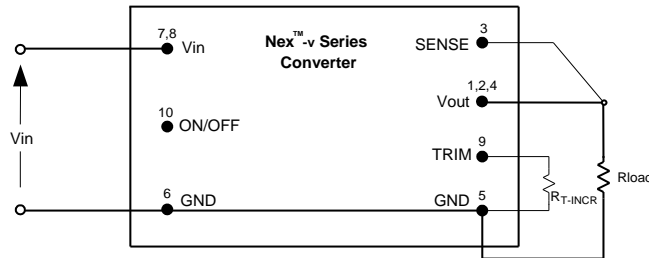


Fig. E: Configuration for increasing output voltage.

To trim down the output voltage (Fig. F), a trim resistor ( $R_{T-DECR}$ ) should be connected between the TRIM pin (Pin 9) and SENSE pin (Pin 3), with a value of:

For  $V_{O-NOM} \geq 1.2V$ ,

$$R_{T-DECR} = \frac{(V_{O-REQ} - 0.8) * 30.1}{(V_{O-NOM} - V_{O-REQ})} - R_{INT} \quad [k\Omega]$$

For  $V_{O-NOM} = 1.0V, 0.9V$ ,

$$R_{T-DECR} = \frac{(V_{O-REQ} - 0.7) * 30.1}{(V_{O-NOM} - V_{O-REQ})} - R_{INT} \quad [k\Omega]$$

where,  $R_{T-DECR}$  = Required value of trim-down resistor [k $\Omega$ ]

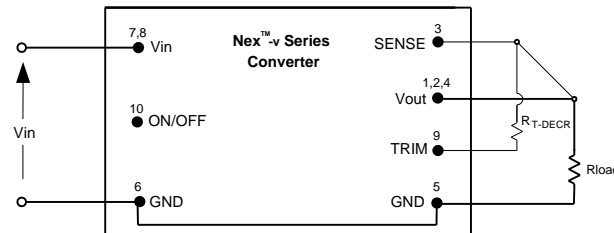


Fig. F: Configuration for decreasing output voltage.

Standard 1% and 5% resistors can be used for trimming. Ground pin of the trim resistor should be connected directly to the converter GND pin (Pin 5) with no voltage drop in between.

The output voltage can also be trimmed up or down using an external voltage source:

For  $V_{O-NOM} \geq 1.2V$ ,

$$V_{TRIM} = 0.8 - \frac{(V_{O-REQ} - V_{O-NOM}) * R_{INT}}{30.1} \quad [V]$$

For  $V_{O-NOM} = 1.0V, 0.9V$ ,

$$V_{TRIM} = 0.7 - \frac{(V_{O-REQ} - V_{O-NOM}) * R_{INT}}{30.1} \quad [V]$$

where,  $V_{TRIM}$  = Output voltage applied to TRIM pin (referenced to GND) [V]

The trim equations for the converters with  $V_{O-NOM} \geq 1.2V$  are industry standard; thus allowing easy second sourcing.

## PROTECTION FEATURES

### Input Undervoltage Lockout

Input undervoltage lockout is standard with this converter. The converter will shut down when the input voltage drops below a pre-determined voltage; it will start automatically when  $V_{in}$  returns to a specified range.

The input voltage must be typically 2.05V for the converter to turn on. Once the converter has been turned on, it will shut off when the input voltage drops below typically 1.9V.

### Output Overcurrent Protection (OCP)

The converter is protected against overcurrent and short circuit conditions. Upon sensing an over-current condition, the converter will enter hiccup mode. Once the overload or short-circuit condition is removed,  $V_{out}$  will return to nominal value.

### Overtemperature Protection (OTP)

The converter will shut down under an over-temperature condition to protect itself from overheating caused by operation outside the thermal derating curves, or operation in abnormal conditions such as system fan failure. After the converter has cooled to a safe operating temperature, it will automatically restart.

### Safety Requirements

Approved to the latest edition and amendment of ITE Safety standards, UL/CSA 62368-1 and IEC/EN 62368-1.

The maximum DC voltage between any two pins is  $V_{in}$  under all operating conditions. Therefore, the unit has ELV (extra low voltage) output; it meets ES1 requirements under the condition that all input voltages are ELV.

The converter is not internally fused. To comply with safety agencies requirements, a recognized fuse with a maximum rating of 20 Amps must be used in series with the input line.

## CHARACTERIZATION

### General Information

The converter has been characterized for many operational aspects, to include thermal derating (maximum load current as a function of ambient temperature and airflow) for vertical and horizontal mounting, efficiency, start-up parameters, output ripple and noise, and transient response to load step-change.

The figures are numbered as Fig. x.y, where x indicates the different output voltages, and y associates with specific plots ( $y = 1$  for the vertical thermal derating, ...). For example, Fig. x.1 will refer to the vertical thermal derating for all the output voltages in general.

The following pages contain specific plots or waveforms associated with the converter. Additional comments for specific data are provided below.

### Test Conditions

All thermal and efficiency data presented were taken with the converter soldered to a test board, specifically a 0.060" thick printed wiring board (PWB) with four layers. The top and bottom layers were not metalized. The two inner layers, comprising two-ounce copper, were used to provide traces for connectivity to the converter.

The lack of metalization on the outer layers as well as the limited thermal connection ensured that heat transfer from the converter to the PWB was minimized. This provides a worst-case but consistent scenario for thermal derating purposes.

All measurements requiring airflow were made in vertical and horizontal wind tunnel facilities using Infrared (IR) thermography and thermocouples for thermometry.

Ensuring components on the converter do not exceed their ratings is important to maintaining high reliability. If one anticipates operating the converter at or close to the maximum loads specified in the derating curves, it is prudent to check actual operating temperatures in the application. Thermographic imaging is preferable; if this capability is not available, then thermocouples may be used. Bel Power Solutions recommends the use of AWG #40 gauge thermocouples to ensure measurement accuracy. Careful routing of the thermocouple leads will further minimize measurement error. Refer to Fig. G for optimum measuring thermocouple location.



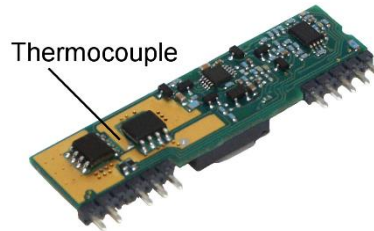


Fig. G: Location of the thermocouple for thermal testing.

### Thermal Derating

Load current vs. ambient temperature and airflow rates are given in Figs. x.1 to x.2 for maximum temperature of 120°C. Ambient temperature was varied between 25 °C and 85 °C, with airflow rates from 30 to 500 LFM (0.15 m/s to 2.5 m/s), and vertical and horizontal converter mounting. The airflow during the testing is parallel to the long axis of the converter, going from ON/OFF pin to output pins.

For each set of conditions, the maximum load current was defined as the lowest of:

- (i) The output current at which any MOSFET temperature does not exceed a maximum specified temperature (120 °C) as indicated by the thermographic image, or
- (ii) The maximum current rating of the converter (10 A)

During normal operation, derating curves with maximum FET temperature less than or equal to 120 °C should not be exceeded. Temperature on the PCB at the thermocouple locations shown in Fig. G should not exceed 120 °C in order to operate inside the derating curves.

### Efficiency

Fig. x.3 show the efficiency vs. load current plot for ambient temperature of 25 °C, airflow rate of 200 LFM (1 m/s) and input voltages of 4.5 V, 5.0 V, and 5.5 V.

Fig. x.4 show the efficiency vs. load current plot for ambient temperature of 25 °C, airflow rate of 200 LFM (1 m/s) and input voltages of 3.0 V, 3.3 V, and 3.6 V for output voltages 2.5 V.

### Power Dissipation

Fig. 3.3V.4 shows the power dissipation vs. load current plot for  $T_a = 25$  °C, airflow rate of 200 LFM (1 m/s) with vertical mounting and input voltages of 4.5 V, 5.0 V, and 5.5 V for 3.3 V output voltage.

### Start-up

Output voltage waveforms, during the turn-on transient with application of  $V_{in}$  at full rated load current (resistive load) are shown with 47  $\mu$ F external load capacitance at  $V_{in} = 5$  V in Fig. x.5.

### Ripple and Noise

The output voltage ripple waveform is measured at full rated load current. Note that all output voltage waveforms are measured across a 1  $\mu$ F ceramic capacitor. The output voltage ripple and input reflected ripple current waveforms are obtained using the test setup shown in Fig. H.

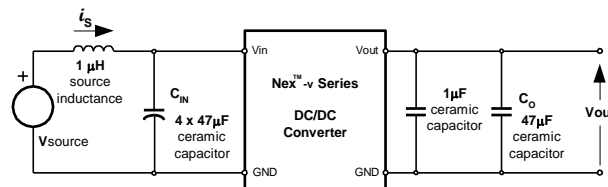


Fig. H: Test setup for measuring input reflected ripple currents,  $i_s$  and output voltage ripple.

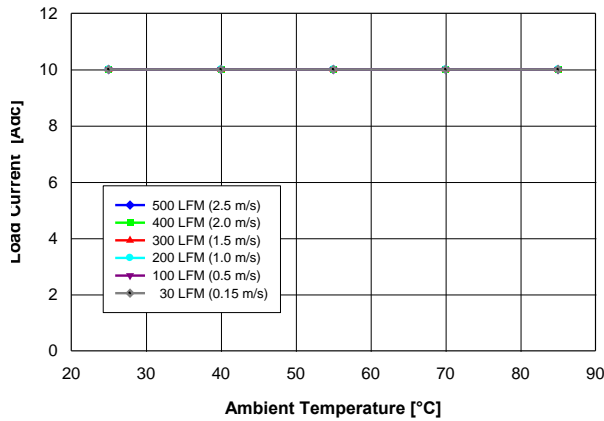


Fig. 3.3V.1: Available load current vs. ambient temperature and airflow rates for YNV05T10033 converter mounted vertically with  $V_{in} = 5V$ , air flowing from pin 10 to pin 1, and maximum MOSFET temperature  $\leq 120^{\circ}C$ .

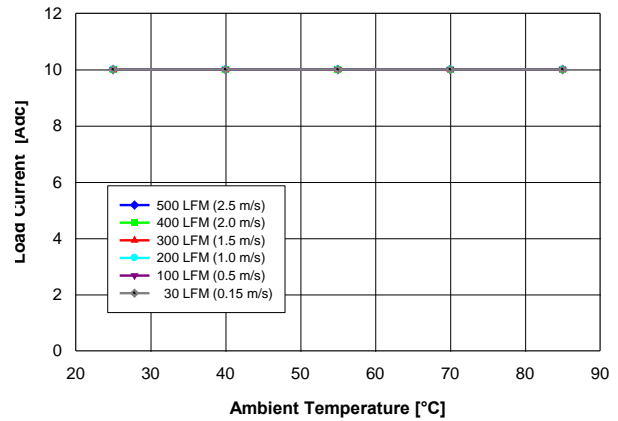


Fig. 3.3V.2: Available load current vs. ambient temperature and airflow rates for YNV05T10033 converter mounted horizontally with  $V_{in} = 5V$ , air flowing from pin 10 to pin 1, and maximum MOSFET temperature  $\leq 120^{\circ}C$ .

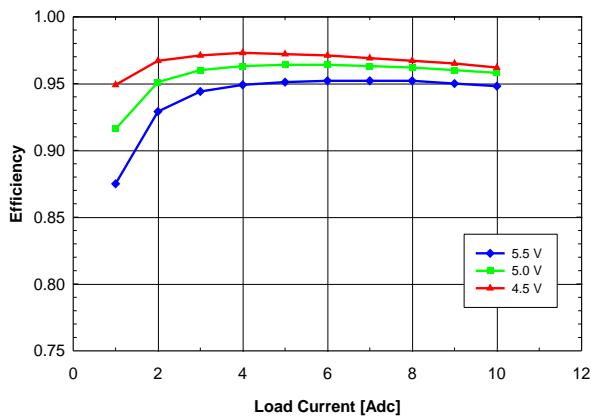


Fig. 3.3V.3: Efficiency vs. load current and input voltage for YNV05T10033 converter mounted vertically with air flowing from pin 10 to pin 1 at a rate of 200 LFM (1m/s) and  $T_a = 25^{\circ}C$ .

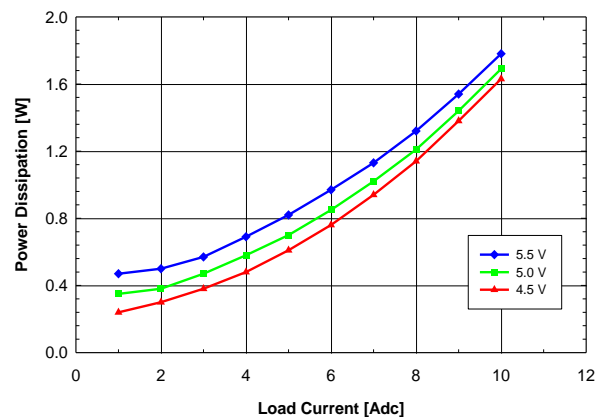


Fig. 3.3V.4: Power loss vs. load current and input voltage for YNV05T10033 converter mounted vertically with air flowing from pin 10 to pin 1 at a rate of 200 LFM (1m/s) and  $T_a = 25^{\circ}C$ .

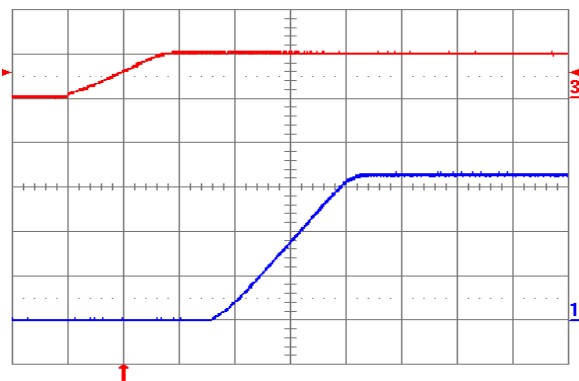


Fig. 3.3V.5: Turn-on transient (YNV05T10033) with application of  $V_{in}$  at full rated load current (resistive) and  $47\mu F$  external capacitance at  $V_{in} = 5V$ . Top trace:  $V_{in}$  (5V/div.); Bottom trace: output voltage (1V/div.); Time scale: 2ms/div.

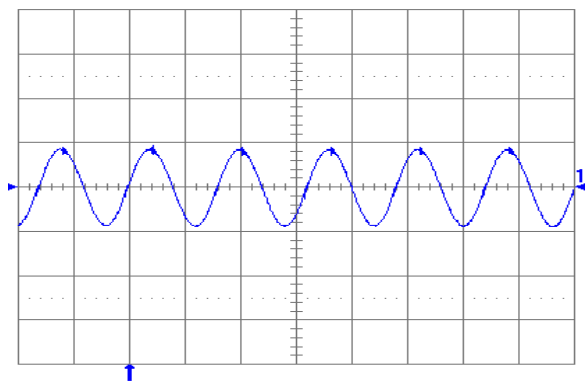


Fig. 3.3V.6: Output voltage ripple (20mV/div.) at full rated load current into a resistive load with external capacitance  $47\mu F$  ceramic +  $1\mu F$  ceramic and  $V_{in} = 5V$  (YNV05T10033). Time scale:  $2\mu s$ /div.

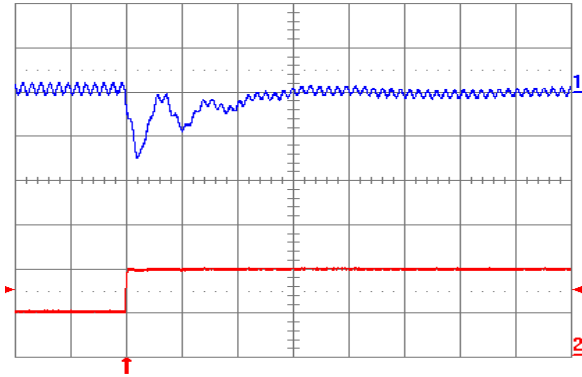


Fig. 3.3V.7: Output voltage response (YNV05T10033) to positive load current step change from 2.5A to 5A with slew rate of 5A/µs at Vin = 5V. Top trace: output voltage (100mV/div.); Bottom trace: load current (5A/div.). Co = 100µF ceramic + 1µF ceramic. Time scale: 20µs/div.

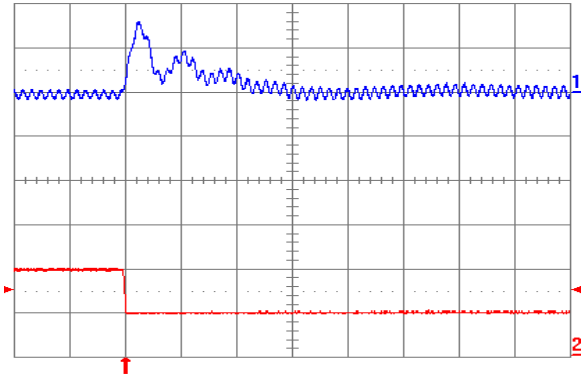


Fig. 3.3V.8: Output voltage response (YNV05T10033) to negative load current step change from 5A to 2.5A with slew rate of -5A/µs at Vin = 5V. Top trace: output voltage (100mV/div.); Bottom trace: load current (5A/div.). Co = 100µF ceramic + 1µF ceramic. Time scale: 20µs/div.

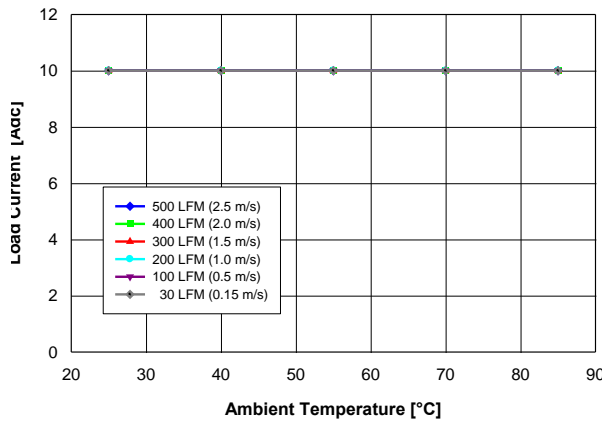


Fig. 2.5V.1: Available load current vs. ambient temperature and airflow rates for YNV05T10025 converter mounted vertically with air flowing from pin 10 to pin 1, and maximum MOSFET temperature ≤ 120°C.

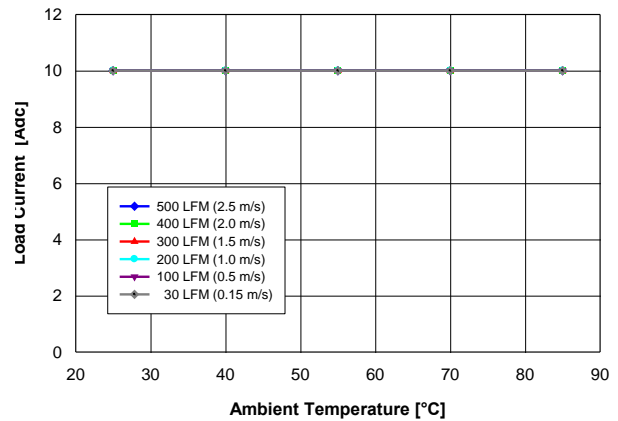


Fig. 2.5V.2: Available load current vs. ambient temperature and airflow rates for YNV05T10025 converter mounted horizontally with air flowing from pin 10 to pin 1, and maximum MOSFET temperature ≤ 120°C.

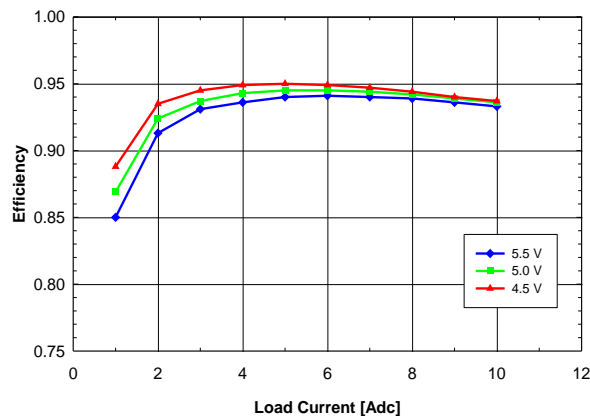


Fig. 2.5V.3: Efficiency vs. load current and input voltage for YNV05T10025 converter mounted vertically with air flowing from pin 10 to pin 1 at a rate of 200 LFM (1m/s) and Ta = 25°C.

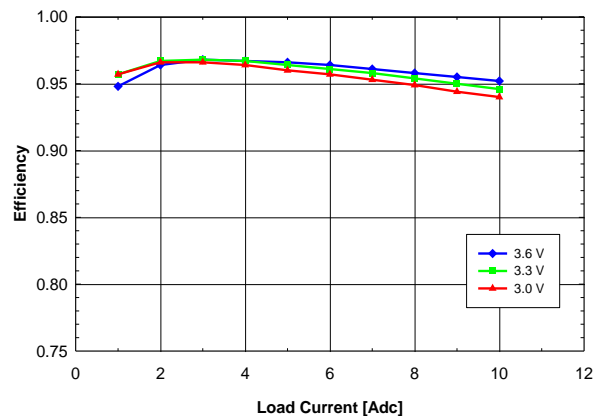


Fig. 2.5V.4: Efficiency vs. load current and input voltage for YNV05T10025 converter mounted vertically with air flowing from pin 10 to pin 1 at a rate of 200 LFM (1m/s) and Ta = 25°C.

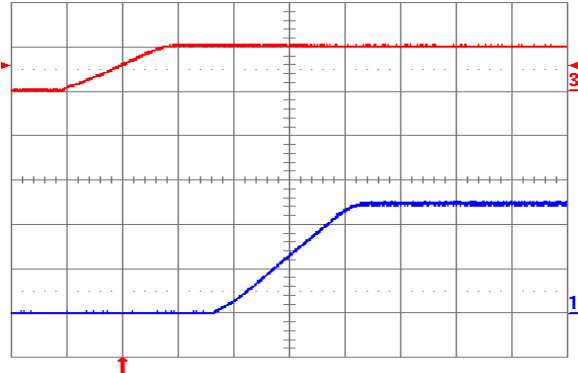


Fig. 2.5V.5: Turn-on transient (YNV05T10025) with application of  $V_{in}$  at full rated load current (resistive) and  $47\mu F$  external capacitance at  $V_{in} = 5V$ . Top trace:  $V_{in}$  (5V/div.); Bottom trace: output voltage (1V/div.); Time scale: 2ms/div.

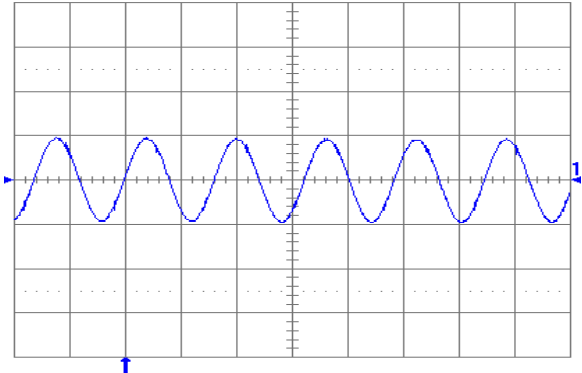


Fig. 2.5V.6: Output voltage ripple (20mV/div.) at full rated load current into a resistive load with external capacitance  $47\mu F$  ceramic +  $1\mu F$  ceramic and  $V_{in} = 5V$  (YNV05T10025). Time scale: 2 $\mu s$ /div.

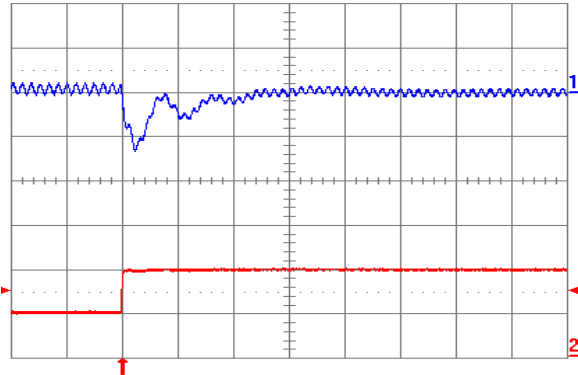


Fig. 2.5V.7: Output voltage response (YNV05T10025) to positive load current step change from 2.5A to 5A with slew rate of  $5A/\mu s$  at  $V_{in} = 5V$ . Top trace: output voltage (100mV/div.); Bottom trace: load current (5A/div.).  $C_o = 100\mu F$  ceramic +  $1\mu F$  ceramic. Time scale: 20 $\mu s$ /div.

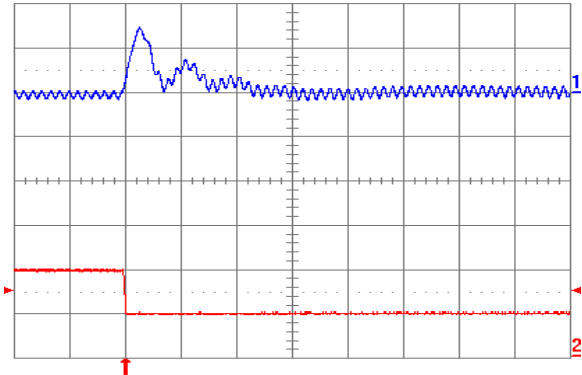


Fig. 2.5V.8: Output voltage response (YNV05T10025) to negative load current step change from 5A to 2.5A with slew rate of  $-5A/\mu s$  at  $V_{in} = 5V$ . Top trace: output voltage (100mV/div.); Bottom trace: load current (5A/div.).  $C_o = 100\mu F$  ceramic +  $1\mu F$  ceramic. Time scale: 20 $\mu s$ /div.

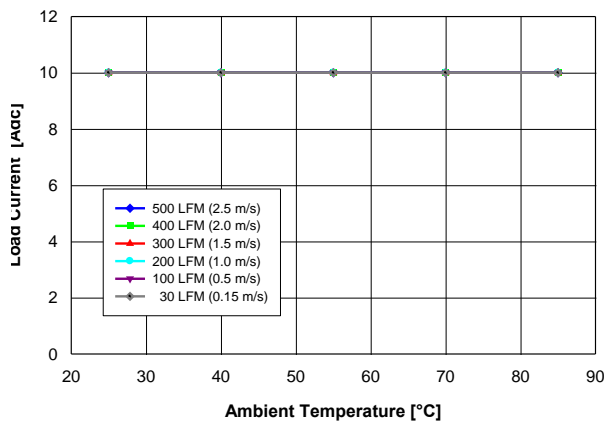


Fig. 2.0V.1: Available load current vs. ambient temperature and airflow rates for YNV05T10020 converter mounted vertically with air flowing from pin 10 to pin 1, and maximum MOSFET temperature  $\leq 120^\circ C$ .

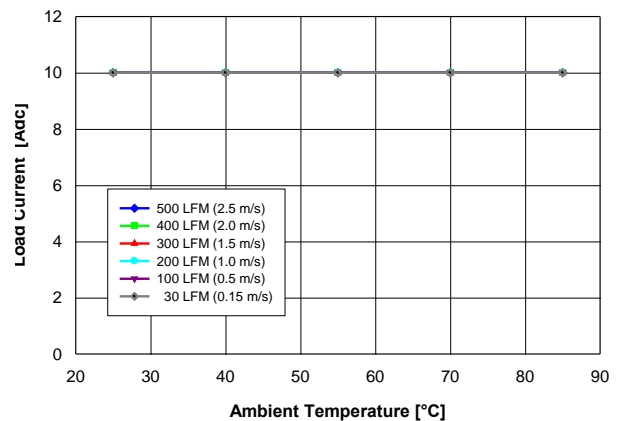


Fig. 2.0V.2: Available load current vs. ambient temperature and airflow rates for YNV05T10020 converter mounted horizontally with air flowing from pin 10 to pin 1, and maximum MOSFET temperature  $\leq 120^\circ C$ .

# YNV05T100xy DC-DC Converter

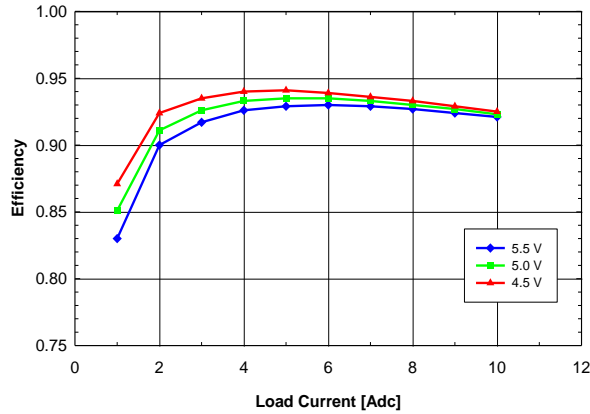


Fig. 2.0V.3: Efficiency vs. load current and input voltage for YNV05T10020 converter mounted vertically with air flowing from pin 10 to pin 1 at a rate of 200 LFM (1m/s) and  $T_a = 25^\circ\text{C}$ .

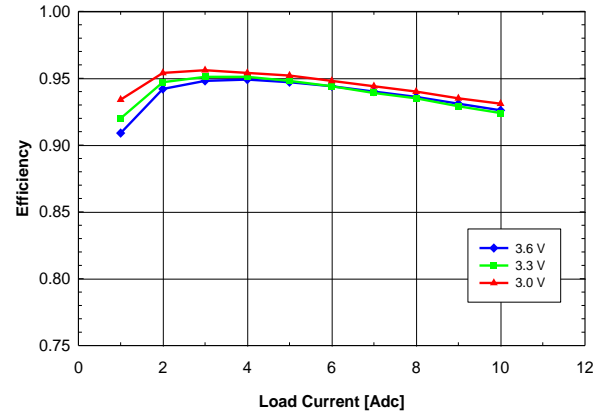


Fig. 2.0V.4: Efficiency vs. load current and input voltage for YNV05T10020 converter mounted vertically with air flowing from pin 10 to pin 1 at a rate of 200 LFM (1m/s) and  $T_a = 25^\circ\text{C}$ .

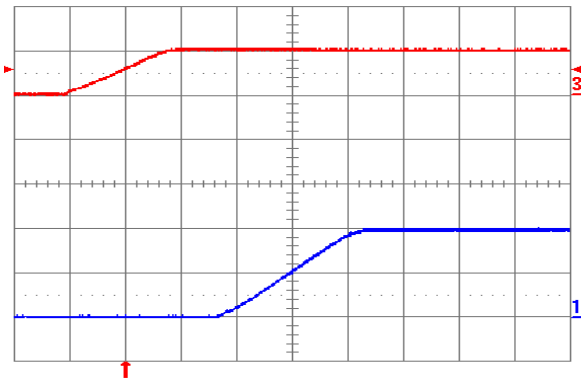


Fig. 2.0V.5: Turn-on transient (YNV05T10020) with application of  $V_{in}$  at full rated load current (resistive) and  $47\mu\text{F}$  external capacitance at  $V_{in} = 5\text{V}$ . Top trace:  $V_{in}$  (5V/div.); Bottom trace: output voltage (1V/div.); Time scale: 2ms/div.

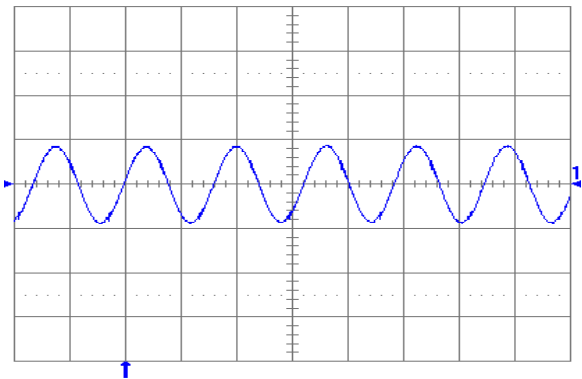


Fig. 2.0V.6: Output voltage ripple (20mV/div.) at full rated load current into a resistive load with external capacitance  $47\mu\text{F}$  ceramic +  $1\mu\text{F}$  ceramic and  $V_{in} = 5\text{V}$  (YNV05T10020). Time scale: 2μs/div.

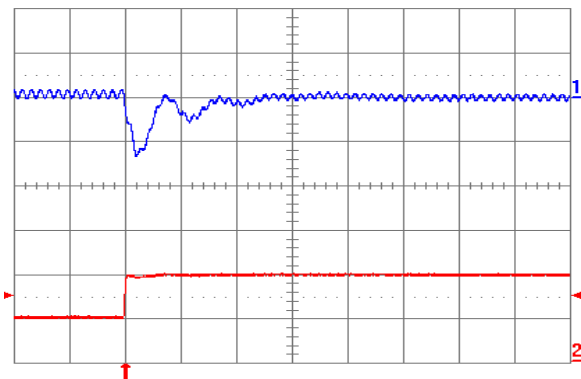


Fig. 2.0V.7: Output voltage response (YNV05T10020) to positive load current step change from 2.5A to 5A with slew rate of  $5\text{A}/\mu\text{s}$  at  $V_{in} = 5\text{V}$ . Top trace: output voltage (100mV/div.); Bottom trace: load current (5A/div.).  $C_o = 100\mu\text{F}$  ceramic +  $1\mu\text{F}$  ceramic. Time scale: 20μs/div.

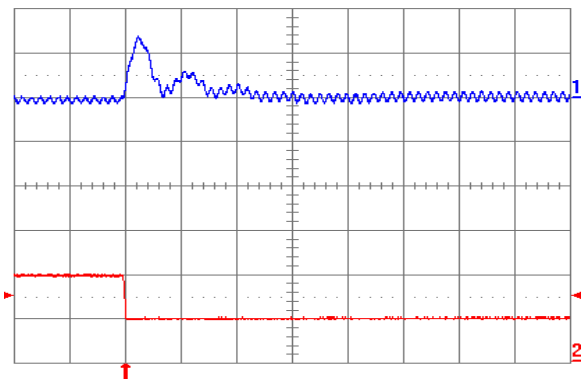


Fig. 2.0V.8: Output voltage response (YNV05T10020) to negative load current step change from 5A to 2.5A with slew rate of  $-5\text{A}/\mu\text{s}$  at  $V_{in} = 5\text{V}$ . Top trace: output voltage (100mV/div.); Bottom trace: load current (5A/div.).  $C_o = 100\mu\text{F}$  ceramic +  $1\mu\text{F}$  ceramic. Time scale: 20μs/div.

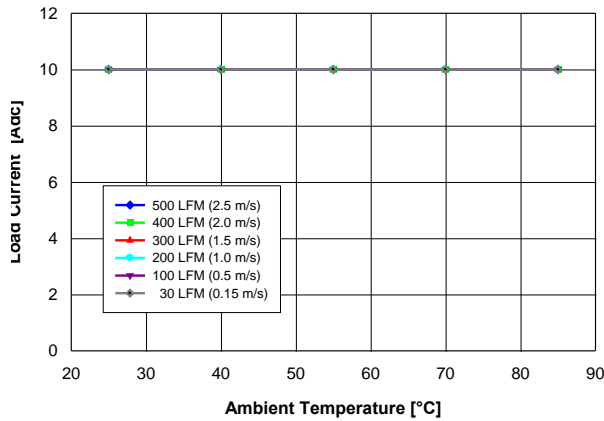


Fig. 1.8V.1: Available load current vs. ambient temperature and airflow rates for YNV05T10018 converter mounted vertically with air flowing from pin 10 to pin 1, and maximum MOSFET temperature  $\leq 120^{\circ}\text{C}$ .

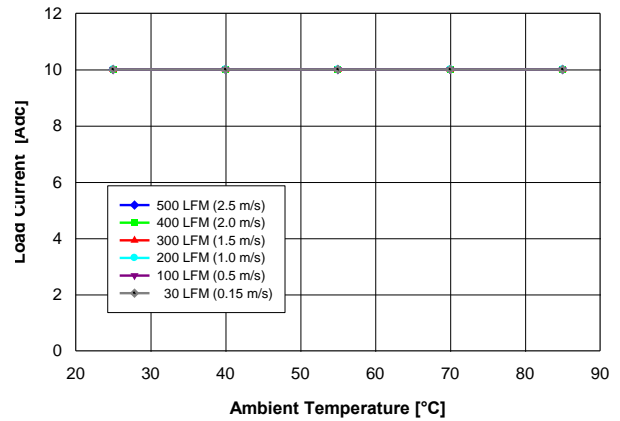


Fig. 1.8V.2: Available load current vs. ambient temperature and airflow rates for YNV05T10018 converter mounted horizontally with air flowing from pin 10 to pin 1, and maximum MOSFET temperature  $\leq 120^{\circ}\text{C}$ .

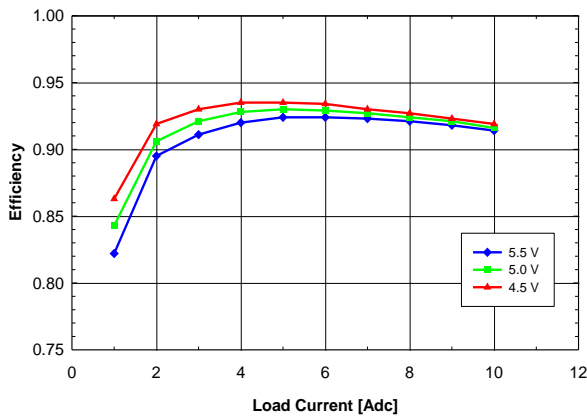


Fig. 1.8V.3: Efficiency vs. load current and input voltage for YNV05T10018 converter mounted vertically with air flowing from pin 10 to pin 1 at a rate of 200 LFM (1m/s) and  $T_a = 25^{\circ}\text{C}$ .

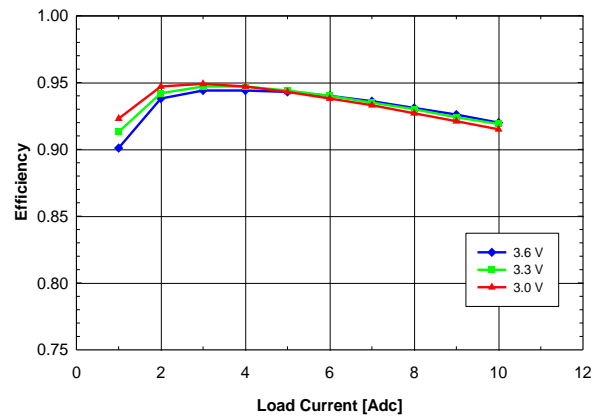


Fig. 1.8V.4: Efficiency vs. load current and input voltage for YNV05T10018 converter mounted vertically with air flowing from pin 10 to pin 1 at a rate of 200 LFM (1m/s) and  $T_a = 25^{\circ}\text{C}$ .

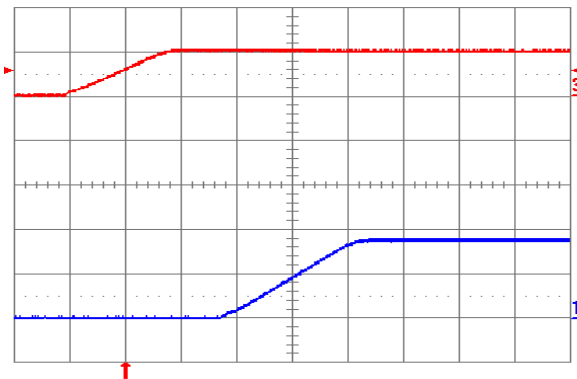


Fig. 1.8V.5: Turn-on transient (YNV05T10018) with application of  $V_{in}$  at full rated load current (resistive) and  $47\mu\text{F}$  external capacitance at  $V_{in} = 5\text{V}$ . Top trace:  $V_{in}$  (5V/div.); Bottom trace: output voltage (1V/div.); Time scale: 2ms/div.

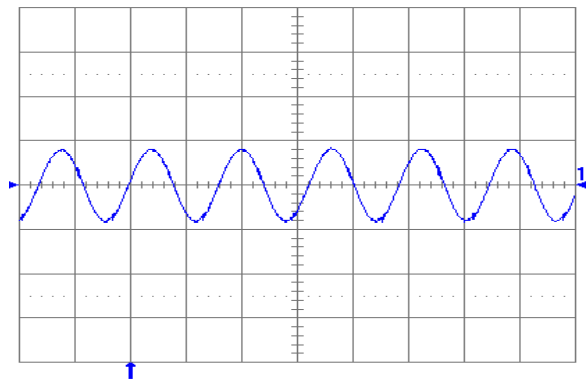


Fig. 1.8V.6: Output voltage ripple (20mV/div.) at full rated load current into a resistive load with external capacitance  $47\mu\text{F}$  ceramic +  $1\mu\text{F}$  ceramic and  $V_{in} = 5\text{V}$  (YNV05T10018). Time scale: 2 $\mu\text{s}$ /div.

# YNV05T100xy DC-DC Converter

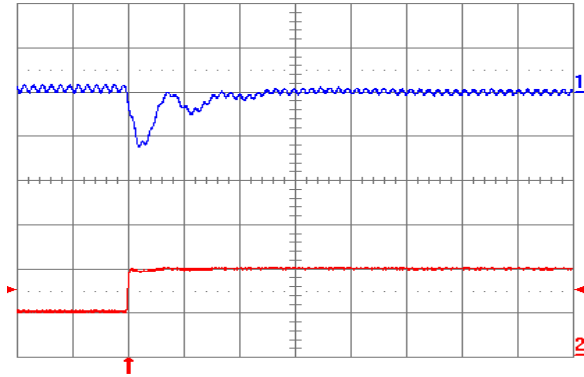


Fig. 1.8V.7: Output voltage response (YNV05T10018) to positive load current step change from 2.5A to 5A with slew rate of 5A/µs at Vin = 5V. Top trace: output voltage (100mV/div.); Bottom trace: load current (5A/div.). Co = 100µF ceramic + 1µF ceramic. Time scale: 20µs/div.

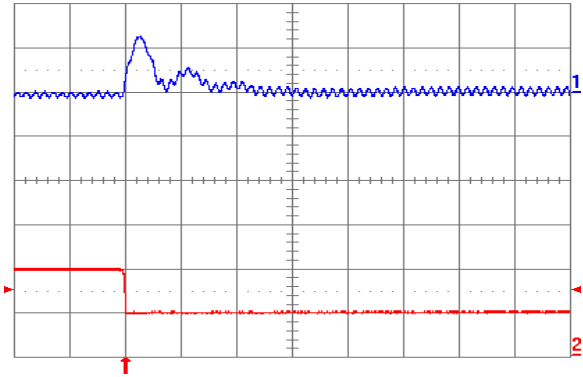


Fig. 1.8V.8: Output voltage response (YNV05T10018) to negative load current step change from 5A to 2.5A with slew rate of -5A/µs at Vin = 5V. Top trace: output voltage (100mV/div.); Bottom trace: load current (5A/div.). Co = 100µF ceramic + 1µF ceramic. Time scale: 20µs/div.

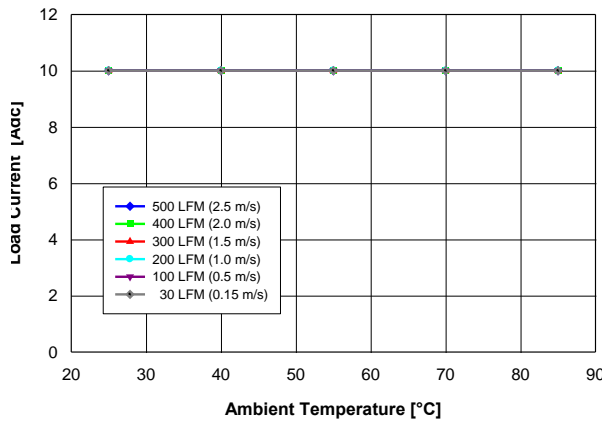


Fig. 1.5V.1: Available load current vs. ambient temperature and airflow rates for YNV05T10015 converter mounted vertically with air flowing from pin 10 to pin 1, and maximum MOSFET temperature ≤ 120°C.

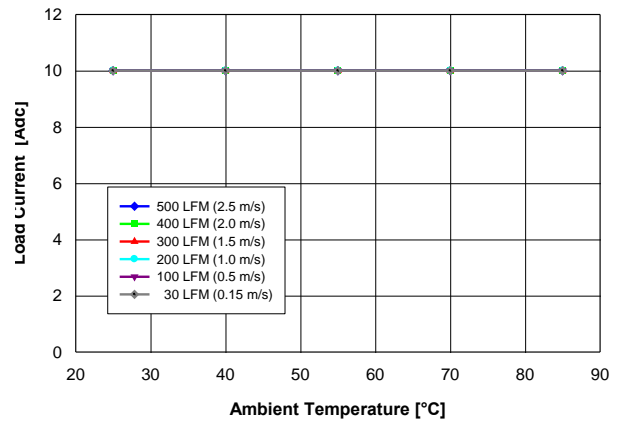


Fig. 1.5V.2: Available load current vs. ambient temperature and airflow rates for YNV05T10015 converter mounted horizontally with air flowing from pin 10 to pin 1, and maximum MOSFET temperature ≤ 120°C.

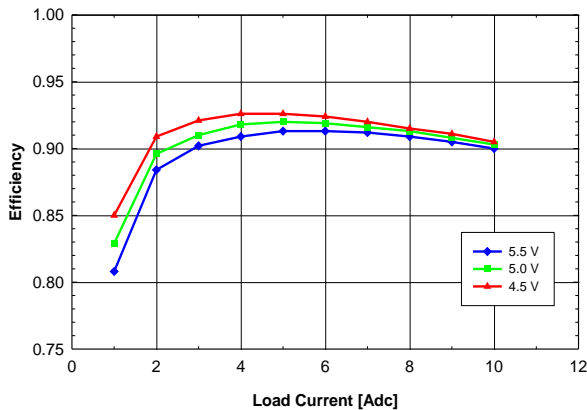


Fig. 1.5V.3: Efficiency vs. load current and input voltage for YNV05T10015 converter mounted vertically with air flowing from pin 10 to pin 1 at a rate of 200 LFM (1m/s) and Ta = 25°C.

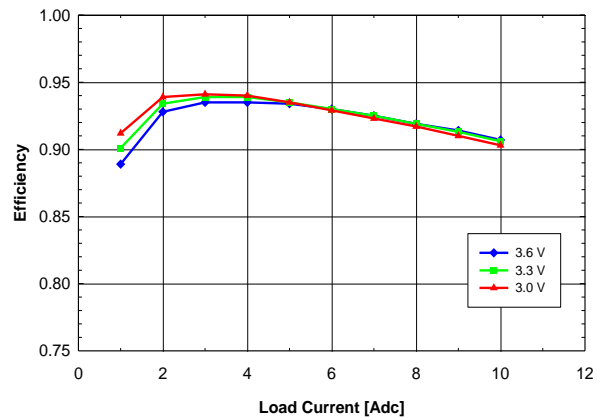


Fig. 1.5V.4: Efficiency vs. load current and input voltage for YNV05T10015 converter mounted vertically with air flowing from pin 10 to pin 1 at a rate of 200 LFM (1m/s) and Ta = 25°C.

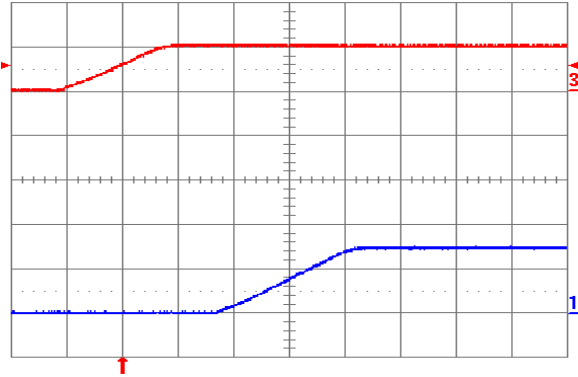


Fig. 1.5V.5: Turn-on transient (YNV05T10015) with application of  $V_{in}$  at full rated load current (resistive) and  $47\mu\text{F}$  external capacitance at  $V_{in} = 5\text{V}$ . Top trace:  $V_{in}$  (5V/div.); Bottom trace: output voltage (1V/div.); Time scale: 2ms/div.

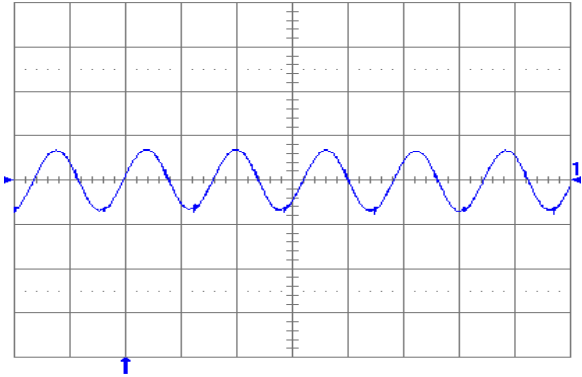


Fig. 1.5V.6: Output voltage ripple (20mV/div.) at full rated load current into a resistive load with external capacitance  $47\mu\text{F}$  ceramic +  $1\mu\text{F}$  ceramic and  $V_{in} = 5\text{V}$  (YNV05T10015). Time scale: 2μs/div.

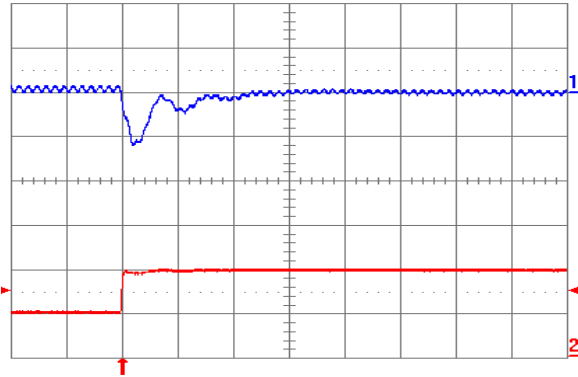


Fig. 1.5V.7: Output voltage response (YNV05T10015) to positive load current step change from 2.5A to 5A with slew rate of  $5\text{A}/\mu\text{s}$  at  $V_{in} = 5\text{V}$ . Top trace: output voltage (100mV/div.); Bottom trace: load current (5A/div.).  $C_o = 100\mu\text{F}$  ceramic +  $1\mu\text{F}$  ceramic. Time scale: 20μs/div.

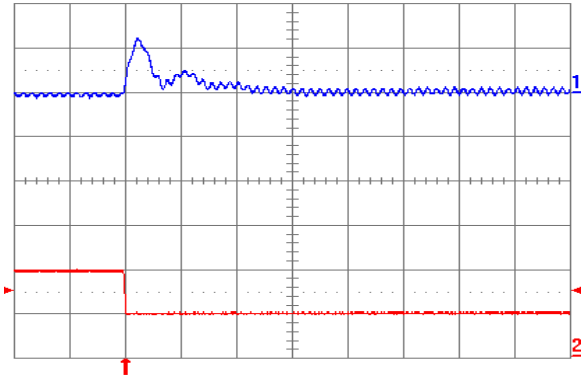


Fig. 1.5V.8: Output voltage response (YNV05T10015) to negative load current step change from 5A to 2.5A with slew rate of  $-5\text{A}/\mu\text{s}$  at  $V_{in} = 5\text{V}$ . Top trace: output voltage (100mV/div.); Bottom trace: load current (5A/div.).  $C_o = 100\mu\text{F}$  ceramic +  $1\mu\text{F}$  ceramic. Time scale: 20μs/div.

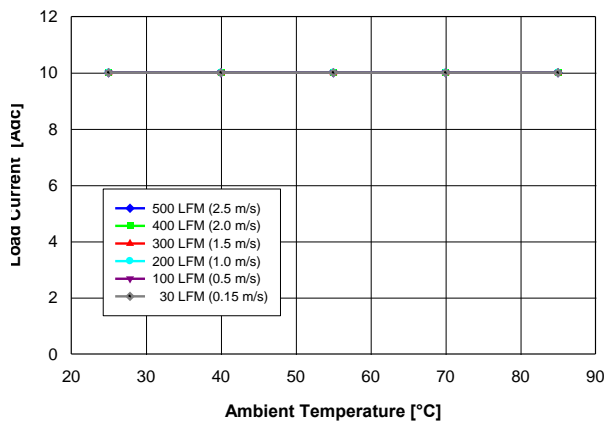


Fig. 1.2V.1: Available load current vs. ambient temperature and airflow rates for YNV05T10012 converter mounted vertically with air flowing from pin 10 to pin 1, and maximum MOSFET temperature  $\leq 120^\circ\text{C}$ .

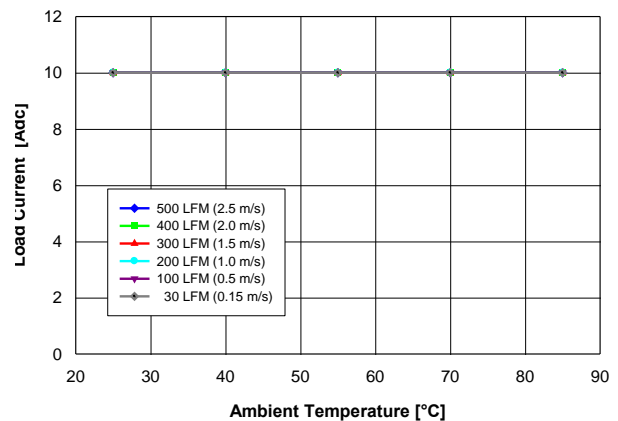


Fig. 1.2V.2: Available load current vs. ambient temperature and airflow rates for YNV05T10012 converter mounted horizontally with air flowing from pin 10 to pin 1, and maximum MOSFET temperature  $\leq 120^\circ\text{C}$ .

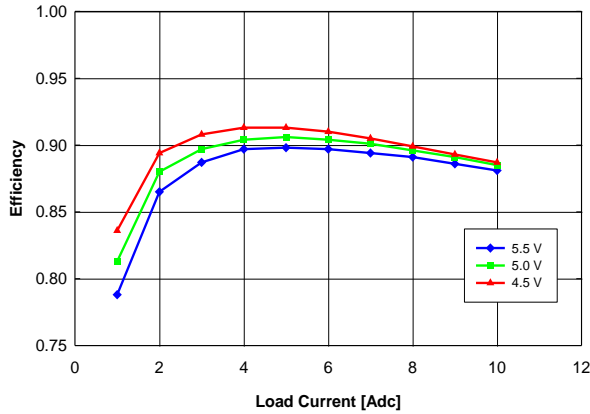


Fig. 1.2V.3: Efficiency vs. load current and input voltage for YNV05T10012 converter mounted vertically with air flowing from pin 10 to pin 1 at a rate of 200 LFM (1m/s) and  $T_a = 25^\circ\text{C}$ .

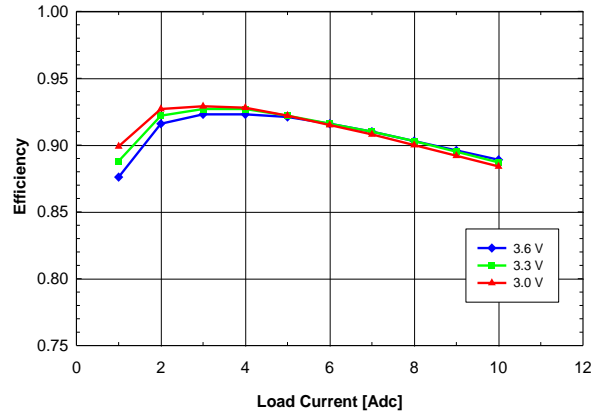


Fig. 1.2V.4: Efficiency vs. load current and input voltage for YNV05T10012 converter mounted vertically with air flowing from pin 10 to pin 1 at a rate of 200 LFM (1m/s) and  $T_a = 25^\circ\text{C}$ .

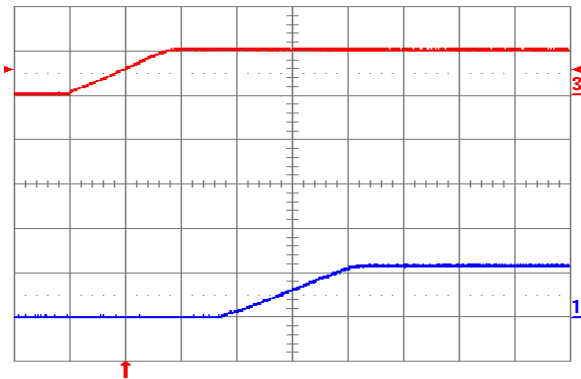


Fig. 1.2V.5: Turn-on transient (YNV05T10012) with application of  $V_{in}$  at full rated load current (resistive) and  $47\mu\text{F}$  external capacitance at  $V_{in} = 5\text{V}$ . Top trace:  $V_{in}$  (5V/div.); Bottom trace: output voltage (1V/div.); Time scale: 2ms/div.

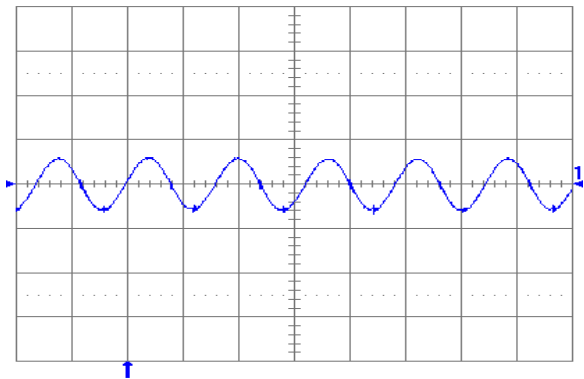


Fig. 1.2V.6: Output voltage ripple (20mV/div.) at full rated load current into a resistive load with external capacitance  $47\mu\text{F}$  ceramic +  $1\mu\text{F}$  ceramic and  $V_{in} = 5\text{V}$  (YNV05T10012). Time scale: 2μs/div.

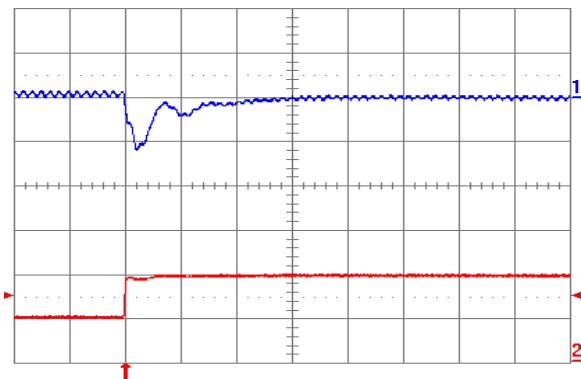


Fig. 1.2V.7: Output voltage response (YNV05T10012) to positive load current step change from 2.5A to 5A with slew rate of  $5\text{A}/\mu\text{s}$  at  $V_{in} = 5\text{V}$ . Top trace: output voltage (100mV/div.); Bottom trace: load current (5A/div.).  $C_o = 100\mu\text{F}$  ceramic +  $1\mu\text{F}$  ceramic. Time scale: 20μs/div.

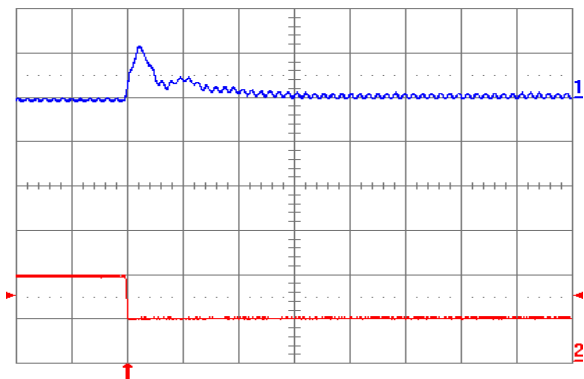


Fig. 1.2V.8: Output voltage response (YNV05T10012) to negative load current step change from 5A to 2.5A with slew rate of  $-5\text{A}/\mu\text{s}$  at  $V_{in} = 5\text{V}$ . Top trace: output voltage (100mV/div.); Bottom trace: load current (5A/div.).  $C_o = 100\mu\text{F}$  ceramic +  $1\mu\text{F}$  ceramic. Time scale: 20μs/div.

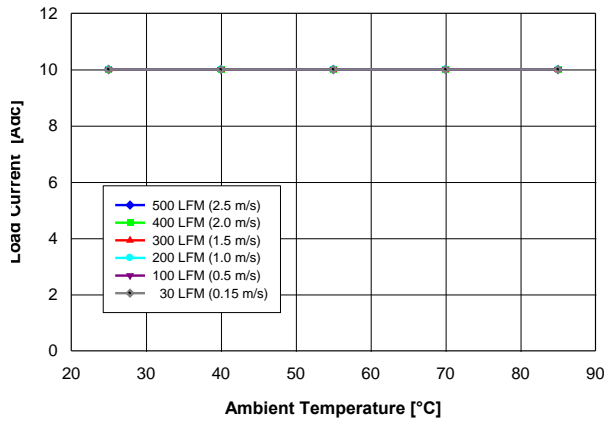


Fig. 1.0V.1: Available load current vs. ambient temperature and airflow rates for YNV05T10010 converter mounted vertically with air flowing from pin 10 to pin 1, and maximum MOSFET temperature  $\leq 120^{\circ}\text{C}$ .

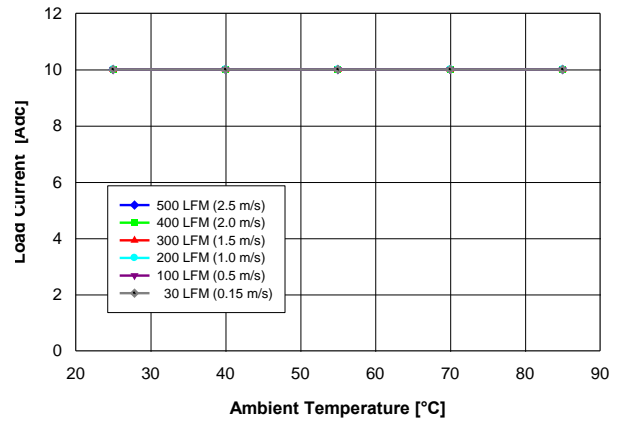


Fig. 1.0V.2: Available load current vs. ambient temperature and airflow rates for YNV05T10010 converter mounted horizontally with air flowing from pin 10 to pin 1, and maximum MOSFET temperature  $\leq 120^{\circ}\text{C}$ .

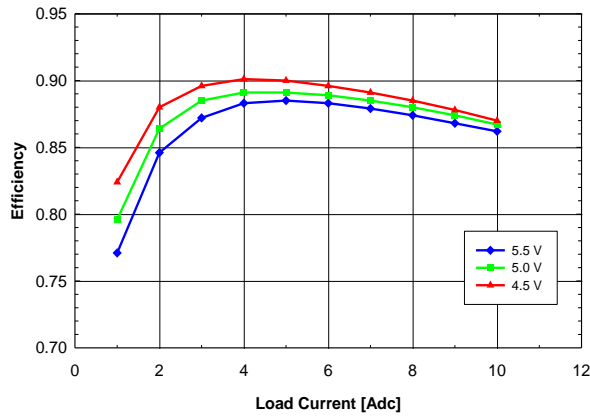


Fig. 1.0V.3: Efficiency vs. load current and input voltage for YNV05T10010 converter mounted vertically with air flowing from pin 10 to pin 1 at a rate of 200 LFM (1m/s) and  $T_a = 25^{\circ}\text{C}$ .

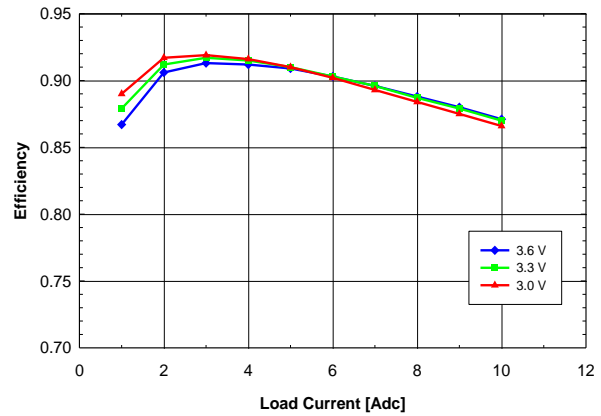


Fig. 1.0V.4: Efficiency vs. load current and input voltage for YNV05T10010 converter mounted vertically with air flowing from pin 10 to pin 1 at a rate of 200 LFM (1m/s) and  $T_a = 25^{\circ}\text{C}$ .

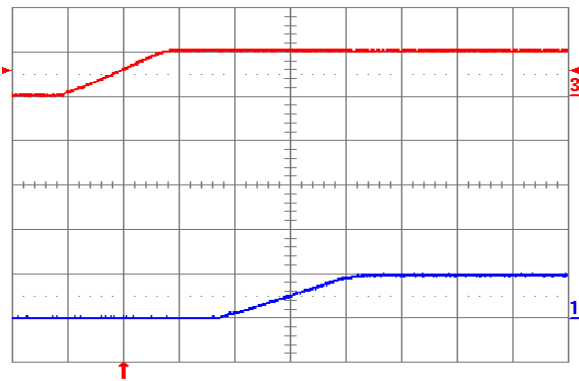


Fig. 1.0V.5: Turn-on transient (YNV05T10010) with application of  $V_{in}$  at full rated load current (resistive) and  $47\mu\text{F}$  external capacitance at  $V_{in} = 5\text{V}$ . Top trace:  $V_{in}$  (5V/div.); Bottom trace: output voltage (1V/div.); Time scale: 2ms/div.

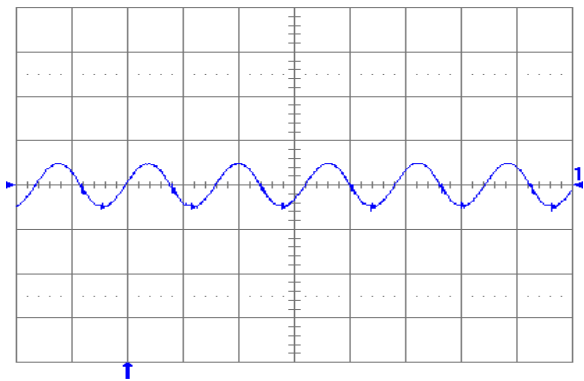


Fig. 1.0V.6: Output voltage ripple (20mV/div.) at full rated load current into a resistive load with external capacitance  $47\mu\text{F}$  ceramic +  $1\mu\text{F}$  ceramic and  $V_{in} = 5\text{V}$  (YNV05T10010). Time scale:  $2\mu\text{s}/\text{div}$ .

# YNV05T100xy DC-DC Converter

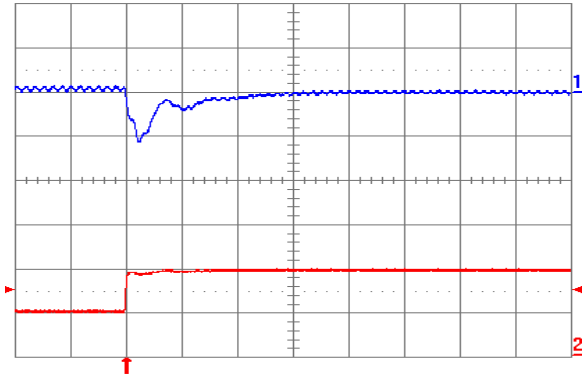


Fig. 1.0V.7: Output voltage response (YNV05T10010) to positive load current step change from 2.5A to 5A with slew rate of 5A/μs at Vin = 5V. Top trace: output voltage (100mV/div.); Bottom trace: load current (5A/div.). Co = 100μF ceramic + 1μF ceramic. Time scale: 20μs/div.

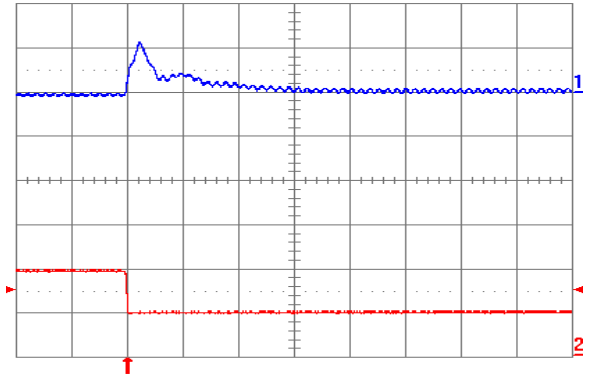


Fig. 1.0V.8: Output voltage response (YNV05T10010) to negative load current step change from 5A to 2.5A with slew rate of -5A/μs at Vin = 5V. Top trace: output voltage (100mV/div.); Bottom trace: load current (5A/div.). Co = 100μF ceramic + 1μF ceramic. Time scale: 20μs/div.

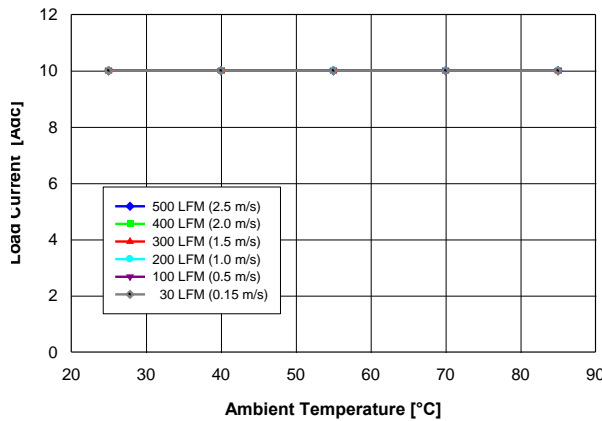


Fig. 0.9V.1: Available load current vs. ambient temperature and airflow rates for YNV05T10009 converter mounted vertically with air flowing from pin 10 to pin 1, and maximum MOSFET temperature ≤ 120°C.

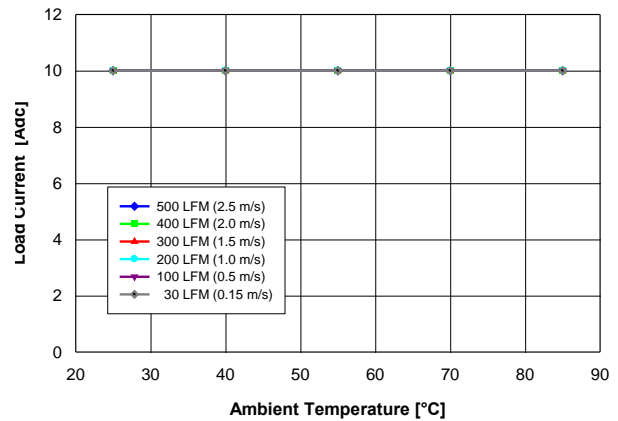


Fig. 0.9V.2: Available load current vs. ambient temperature and airflow rates for YNV05T10009 converter mounted horizontally with air flowing from pin 10 to pin 1, and maximum MOSFET temperature ≤ 120°C.

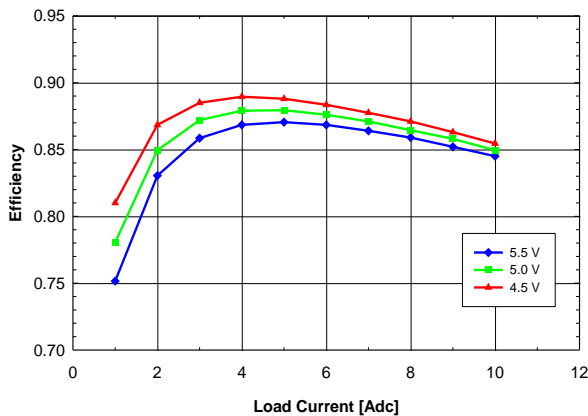


Fig. 0.9V.3: Efficiency vs. load current and input voltage for YNV05T10009 converter mounted vertically with air flowing from pin 10 to pin 1 at a rate of 200 LFM (1m/s) and Ta = 25°C.

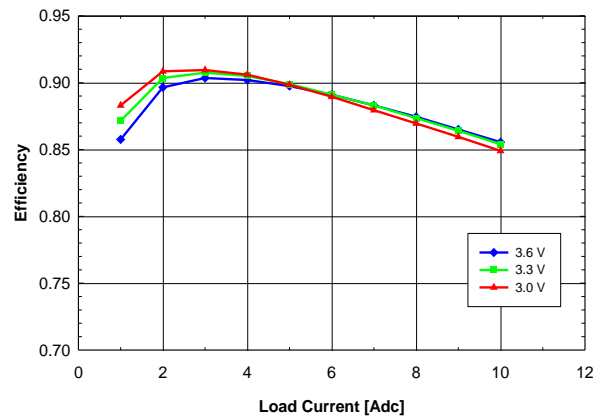


Fig. 0.9V.4: Efficiency vs. load current and input voltage for YNV05T10009 converter mounted horizontally with air flowing from pin 10 to pin 1 at a rate of 200 LFM (1m/s) and Ta = 25°C.

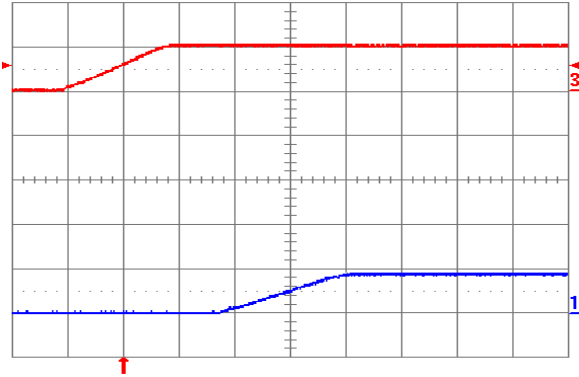


Fig. 0.9V.5: Turn-on transient (YNV05T10009) with application of  $V_{in}$  at full rated load current (resistive) and  $47\mu\text{F}$  external capacitance at  $V_{in} = 5\text{V}$ . Top trace:  $V_{in}$  (5V/div.); Bottom trace: output voltage (1V/div.); Time scale: 2ms/div.

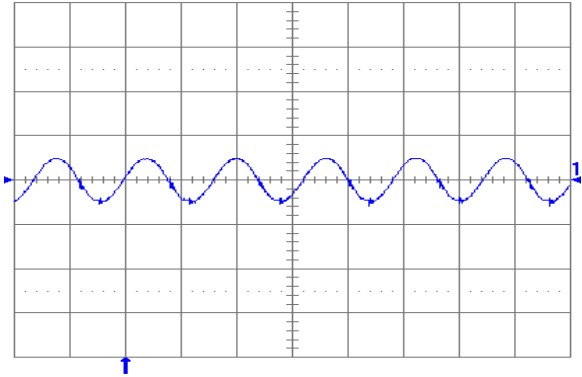


Fig. 0.9V.6: Output voltage ripple (20mV/div.) at full rated load current into a resistive load with external capacitance  $47\mu\text{F}$  ceramic +  $1\mu\text{F}$  ceramic and  $V_{in} = 5\text{V}$  (YNV05T10009). Time scale: 2 $\mu\text{s}$ /div.

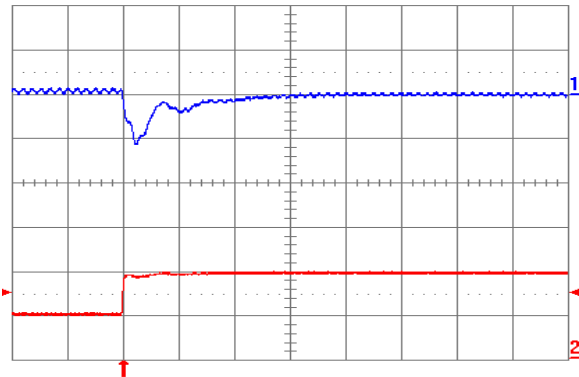


Fig. 0.9V.7: Output voltage response (YNV05T10009) to positive load current step change from 2.5A to 5A with slew rate of  $5\text{A}/\mu\text{s}$  at  $V_{in} = 5\text{V}$ . Top trace: output voltage (100mV/div.); Bottom trace: load current (5A/div.).  $C_o = 100\mu\text{F}$  ceramic +  $1\mu\text{F}$  ceramic. Time scale: 20 $\mu\text{s}$ /div.

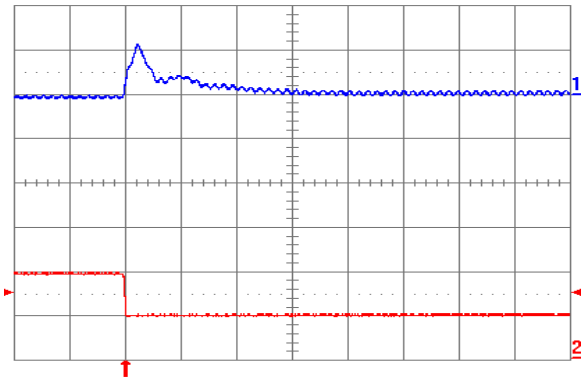
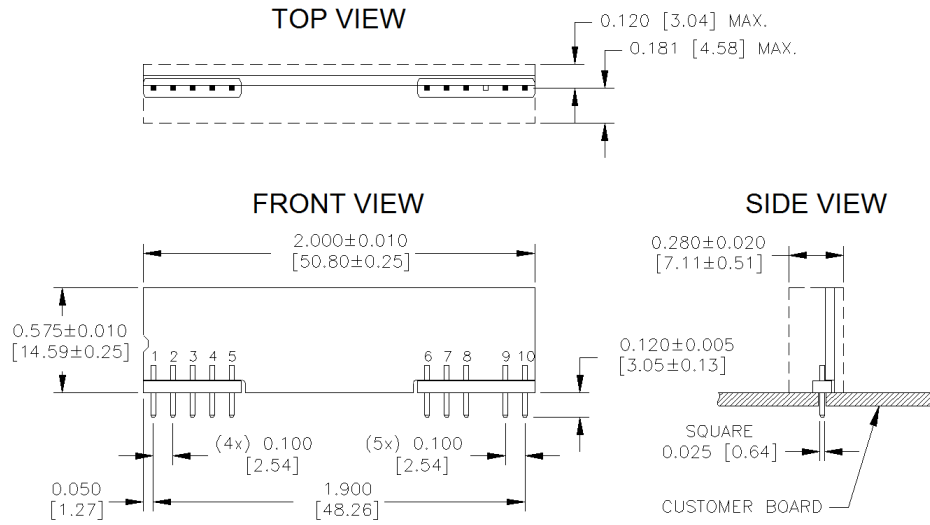


Fig. 0.9V.8: Output voltage response (YNV05T10009) to negative load current step change from 5A to 2.5A with slew rate of  $-5\text{A}/\mu\text{s}$  at  $V_{in} = 5\text{V}$ . Top trace: output voltage (100mV/div.); Bottom trace: load current (5A/div.).  $C_o = 100\mu\text{F}$  ceramic +  $1\mu\text{F}$  ceramic. Time scale: 20 $\mu\text{s}$ /div.

## PHYSICAL INFORMATION



PAD/PIN CONNECTIONS	
Pad/Pin #	Function
1	Vout
2	Vout
3	Vout SENSE
4	Vout
5	GND
6	GND
7	Vin
8	Vin
9	TRIM
10	ON/OFF

**YNV05T100xy Pinout (Through-Hole - SIP)**

### YNV05T100xy Platform Notes

- All dimensions are in inches [mm]
- Connector Material: Phosphor Bronze/ Brass Alloy 360
- Connector Finish: Tin over Nickel
- Converter Weight: 0.26 oz [7.28 g]
- Converter Height: 0.585" Max.
- Recommended Through Hole Via/Pad: Min. 0.043" X 0.064" [1.09 x 1.63 mm]

## ORDERING INFORMATION

Product Series	Input Voltage	Mounting Scheme	Rated Load Current	Output Voltage	Enable Logic	RoHS
YNV	05	T	10	018	0	
Y-Series	3.0 – 5.5 V	T ⇒ Through-Hole (SIP)	10 A (0.9 to 3.3 VDC)	009 ⇒ 0.9 V 010 ⇒ 1.0 V 012 ⇒ 1.2 V 015 ⇒ 1.5 V 018 ⇒ 1.8 V 020 ⇒ 2.0 V 025 ⇒ 2.5 V 033 ⇒ 3.3 V	0 ⇒ Standard (Positive Logic) D ⇒ Opposite of Standard (Negative Logic)	No Suffix ⇒ RoHS lead solder exemption compliant G ⇒ RoHS compliant for all six substances

The example above describes P/N YNV05T10018-0: 3.0V – 5.5V input, thru-hole (SIP), 10A at 1.8V output, standard enable logic, and RoHS lead solder exemption. Please consult factory regarding availability of a specific version.

Model numbers highlighted in yellow or shaded are not recommended for new designs.



**For more information on these products consult: [tech.support@psbel.com](mailto:tech.support@psbel.com)**

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**TECHNICAL REVISIONS** - The appearance of products, including safety agency certifications pictured on labels, may change depending on the date manufactured. Specifications are subject to change without notice.

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