



**THE DATASHEET OF  
XRD9824ACD-F**





# XRD9824

## 14-Bit Linear CIS/CCD Sensor Signal Processor with Serial Control

May 2000-3

### FEATURES

- 14-Bit Resolution, No Missing Codes
- One-channel 6MSPS Pixel Rate
- Triple-channel 2MSPS Pixel Rate
- 6-Bit Programmable Gain Amplifier
- 8-Bit Programmable Offset Adjustment
- CIS or CCD Compatibility
- Internal Clamp for CIS or CCD AC Coupled Configurations
- 5V Operation
- Serial Load Control Registers
- Low Power CMOS: 200mW-typ
- Low Cost 20-Lead Packages
- USB Compliant

### APPLICATIONS

- Color and Grayscale Flatbed Scanners
- Color and Grayscale Sheetfed Scanners
- Multifunction Peripherals
- Digital Color Copiers
- General Purpose CIS or CCD Imaging
- Low Cost Data Acquisition
- Simple and Direct Interface to Canon 600 DPI Sensors

### GENERAL DESCRIPTION

The XRD9824 is a complete linear CIS or CCD sensor signal processor on a single monolithic chip. The XRD9824 includes a high speed 14-bit resolution ADC, a 6-bit Programmable Gain Amplifier with gain adjustment of 1 to 10, and 8-bit programmable input referred offset calibration range of 800mV.

In the CCD configuration the input signal is AC coupled with an external capacitor. An internal clamp sets the black level. In the CIS configuration, the clamp switch can be disabled and the CIS output signal is DC coupled from the CIS sensor to the XRD9824. The CIS signal is level shifted to VRB in

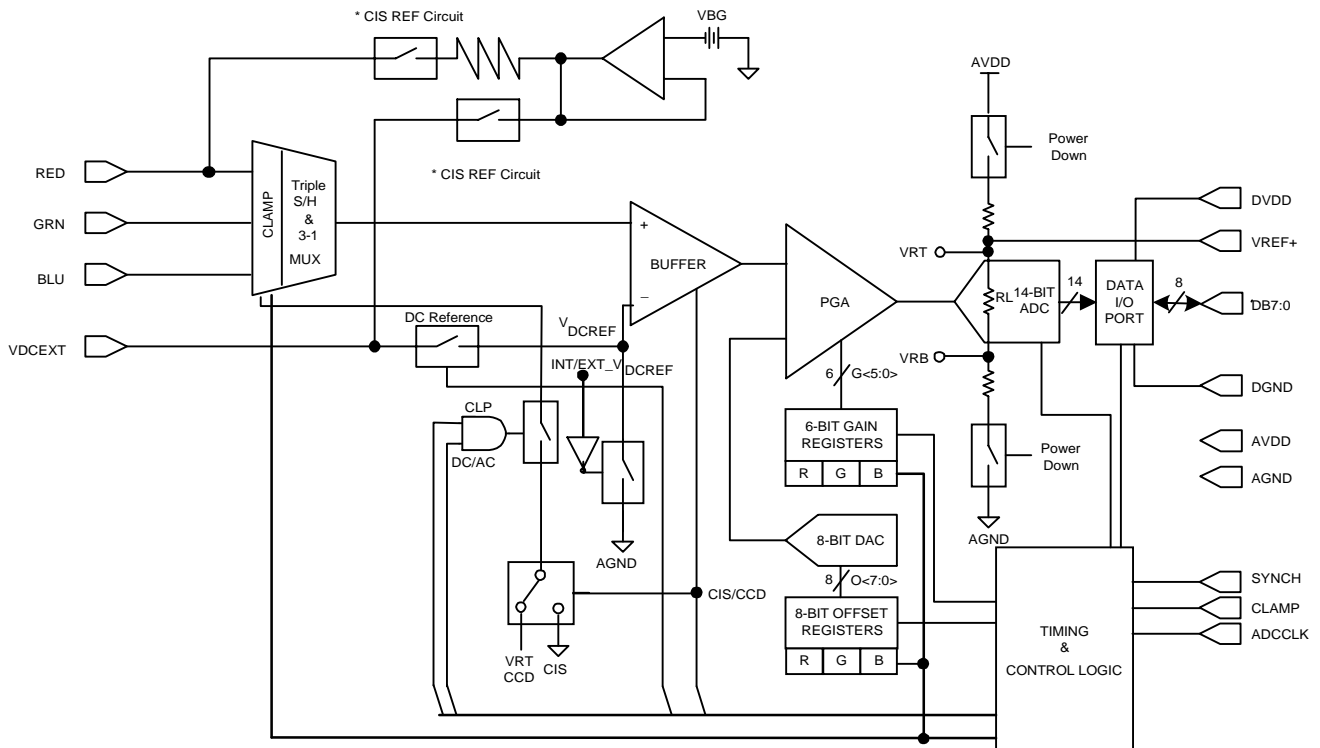
order to use the full range of the ADC. In the CIS configuration the input can also be AC coupled similar to the CCD configuration. This enables CIS signals with large black levels to be internally clamped to a DC reference equal to the black level. The DC reference is internally subtracted from the input signal.

The CIS configuration can also be used in other applications that do not require CDS function, such as low cost data acquisition.

### ORDERING INFORMATION

| Package Type | Temperature Range | Part Number |
|--------------|-------------------|-------------|
| 20-Lead SOIC | 0°C to +70°C      | XRD9824ACD  |
| 20-Lead SSOP | 0°C to +70°C      | XRD9824ACU  |

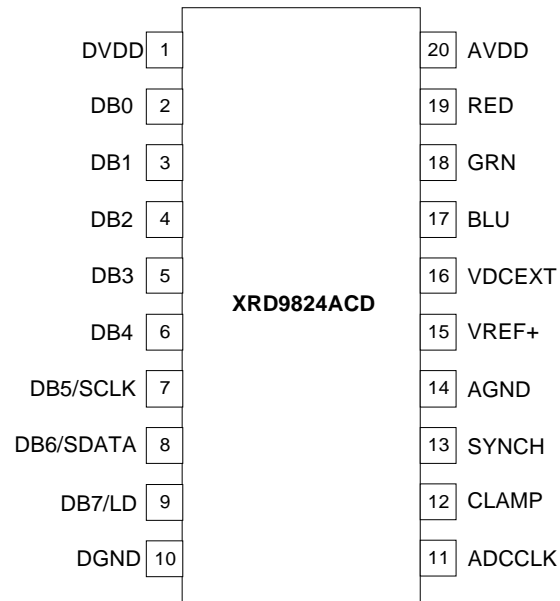
Rev. 2.00



**Note:** \* For Canon CIS Sensor

**Figure 1. Functional Block Diagram**

## PIN CONFIGURATION



### 20-Lead SOIC

## PIN DESCRIPTION

| Pin # | Symbol    | Description                                     |
|-------|-----------|---|
| 1     | DVDD      | Digital VDD (for Output Drivers)                |
| 2     | DB0       | Data Output Bit 0                               |
| 3     | DB1       | Data Output Bit 1                               |
| 4     | DB2       | Data Output Bit 2                               |
| 5     | DB3       | Data Output Bit 3                               |
| 6     | DB4       | Data Output Bit 4                               |
| 7     | DB5/SCLK  | Data Output Bit 5 & Data Input SCLK             |
| 8     | DB6/SDATA | Data Output Bit 6 & Data Input SDATA            |
| 9     | DB7/LD    | Data Output Bit 7 & LD                          |
| 10    | DGND      | Digital Ground (for Output Drivers)             |
| 11    | ADCCLK    | A/D Converter Clock                             |
| 12    | CLAMP     | Clamp and Video Sample Clock                    |
| 13    | SYNCH     | Start of New Line and Serial Data Input Control |
| 14    | AGND      | Analog Ground                                   |
| 15    | VREF+     | A/D Positive Reference for Decoupling Cap       |
| 16    | VDCEXT    | External DC Reference                           |
| 17    | BLU       | Blue Input                                      |
| 18    | GRN       | Green Input                                     |
| 19    | RED       | Red Input                                       |
| 20    | AVDD      | Analog Power Supply                             |

## ELECTRICAL CHARACTERISTICS

Test Conditions:  $AV_{DD}=DV_{DD}=5V$ ,  $ADCCLK=6MHz$ , 50% Duty Cycle,  $T_A=25^{\circ}C$  unless otherwise specified.

| Symbol                                     | Parameter   | Min.  | Typ.          | Max.  | Unit     | Conditions              |
|--|---|-------|---------------|-------|----------|-------------------------|
| <b>Power Supplies</b>                      |   |       |               |       |          |                         |
| $AV_{DD}$                                  | Analog Power Supply                                     | 3.0   | 3.3           | 5.5   | V        | (Note 2)                |
| $DV_{DD}$                                  | Digital I/O Power Supply                                | 3.0   | 3.3           | 5.5   | V        | $DV_{DD} \leq AV_{DD}$  |
| $I_{DD}$                                   | Supply Current  |       | 40            | 55    | mA       | $V_{DD}=5V$             |
| $IDD_{PD}$                                 | Power Down Power Supply Current                         |       |               | 50    | $\mu A$  | $V_{DD}=5V$             |
| <b>ADC Specifications</b>                  |   |       |               |       |          |                         |
| RES  | Resolution  | 14    |               |       | Bits     |                         |
| $F_s$                                      | Maximum Sampling Rate                                   | 12    |               |       | MSPS     |                         |
| DNL  | Differential Non-Linearity                              | -3.0  | $\pm 1.5$     | 3.0   | LSB      |                         |
| $V_{RT}$                                   | Top Reference Voltage                                   | 3.50  | $AV_{DD}/1.3$ | 3.90  | V        |                         |
| $V_{RB}$                                   | Bottom Reference Voltage                                |       | $AV_{DD}/10$  |       | V        |                         |
| $DV_{REF}$                                 | Differential Reference Voltage<br>( $V_{RT} - V_{RB}$ ) | 0.3   | $0.67AV_{DD}$ |       | V        |                         |
| $R_L$                                      | Ladder Resistance                                       | 300   | 600           | 780   | $\Omega$ |                         |
| <b>PGA &amp; Offset DAC Specifications</b> |   |       |               |       |          |                         |
| PGARES                                     | PGA Resolution  | 6     |               |       | Bits     |                         |
| $PGAG_{MIN}$                               | Minimum Gain  | 0.950 | 1.0           | 1.050 | V/V      |                         |
| $PGAG_{MAX}$                               | Maximum Gain  | 9.5   | 10.0          | 10.50 | V/V      |                         |
| PGAGD                                      | Gain Adjustment Step Size                               |       | 0.14          |       | V/V      |                         |
| $V_{BLACK}$                                | Black Level Input Range                                 | -100  |               | 500   | mV       | DC Configuration        |
| DACRES                                     | Offset DAC Resolution                                   | 8     |               |       | Bits     |                         |
| $OFF_{MIN}$                                | Minimum Offset Adjustment                               | -250  | -200          | -150  | mV       | Mode 111, D5=0 (Note 1) |
| $OFF_{MAX}$                                | Maximum Offset Adjustment                               | +500  | +600          | +700  | mV       | Mode 111, D5=0          |
| $OFF_{MIN}$                                | Minimum Offset Adjustment                               | -450  | -400          | -350  | mV       | Mode 111, D5=1 (Note 1) |
| $OFF_{MAX}$                                | Maximum Offset Adjustment                               | +350  | +400          | +450  | mV       | Mode 111, D5=1          |
| $OFF_{\Delta}$                             | Offset Adjustment Step Size                             |       | 3.14          |       | mV       |                         |

**Note 1:** The additional  $\pm 100$  mV of adjustment with respect to the black level input range is needed to compensate for any additional offset introduced by the XRD9824 Buffer/PGA internally.

**Note 2:** It is not recommended to operate the part between 3.6V and 4.4V.

## ELECTRICAL CHARACTERISTICS (CONT'D)

Test Conditions:  $AV_{DD}=DV_{DD}=5V$ ,  $ADCCLK=6MHz$ , 50% Duty Cycle,  $T_A=25^\circ C$  unless otherwise specified.

| Symbol                               | Parameter                      | Min.            | Typ.     | Max.                       | Unit       | Conditions   |
|--------------------------------------|--------------------------------|-----------------|----------|----------------------------|------------|--|
| <b>Buffer Specifications</b>         |                                |                 |          |                            |            |  |
| $I_{IL}$                             | Input Leakage Current          |                 |          | 100                        | nA         |  |
| $C_{IN}$                             | Input Capacitance              |                 | 10       |                            | pF         |  |
| $V_{IN_{PP}}$                        | AC Input Voltage Range         | 0               |          | $AV_{DD}-1.4$              | V          | CIS AC; INT $V_{DCREF}$<br>Config Reg<br>=> XXX010XX<br>Gain=1 (Note 1)                                      |
|                                      | AC Input Voltage Range         | 0               |          | $DV_{REF}$                 | V          | CCD AC; INT $V_{DCREF}$<br>Config Reg<br>=> XXX011XX<br>Gain=1 (Note 1)                                      |
| $V_{IN}$                             | DC Input Voltage Range         | -0.1            |          | $AV_{DD}-1.4$              | V          | CIS DC; INT $V_{DCREF}$<br>Config Reg<br>=> XXX000XX<br>Gain=1 (Note 2)                                      |
|                                      | DC Input Voltage Range         | $V_{DCEXT}-0.1$ |          | $V_{DCEXT}+$<br>$DV_{REF}$ | V          | CIS DC; EXT $V_{DCREF}$<br>Config Reg<br>=> XXX100XX<br>Gain=1 (Note 3)<br>$V_{DCEXT}+DV_{REF} \leq AV_{DD}$ |
| $V_{DCEXT}$<br>Pin 16=Input          | External DC Reference          | 0.3             |          | $AV_{DD}/2$                | V          | CIS DC; EXT $V_{DCREF}$<br>Config Reg Mode 110<br>=> XXX100XX  |
| $V_{DCEXT}$<br>Pin 16=Output         | Internal DC Reference          | 1.17            |          | 1.34                       | V          | Internal CIS Reference<br>Circuit<br>Config Reg Mode 111<br>=> XXX1XXXX                                      |
| $V_{IN_{BW}}$                        | Input Bandwidth (Small Signal) |                 | 10       |                            | MHz        |  |
| $V_{IN_{CT}}$                        | Channel to Channel Crosstalk   |                 | -60      | -50                        | dB         | $f_{in}=3MHz$  |
| <b>Internal Clamp Specifications</b> |                                |                 |          |                            |            |  |
| $V_{CLAMP}$                          | Clamp Voltage                  |                 | AGND     | 50                         | mV         | CIS (AC) Config  |
|                                      |                                | 3.5             | $V_{RT}$ |                            | V          | CCD (AC) Config  |
| $R_{INT}$                            | Clamp Switch On Resistance     |                 | 100      | 150                        | $\Omega$   |  |
| $R_{OFF}$                            | Clamp Switch Off Resistance    | 10              |          |                            | M $\Omega$ |  |

**Note 1:**  $V_{IN_{PP}}$  is the signal swing before the external capacitor tied to the MUX inputs.

**Note 2:** The -0.1V minimum is specified in order to accommodate black level signals lower than the external DC reference (clamp) voltage.

**Note 3:** The  $V_{DCEXT}-0.1V$  minimum is specified in order to accommodate black level signals lower than the external DC reference voltage.

## ELECTRICAL CHARACTERISTICS (CONT'D)

Test Conditions:  $AV_{DD}=DV_{DD}=5V$ ,  $ADCCLK=6MHz$ , 50% Duty Cycle,  $T_A=25^\circ C$  unless otherwise specified.

| Symbol  | Parameter                        | Min.                  | Typ. | Max. | Unit              | Conditions   |
|---|----------------------------------|-----------------------|------|------|-------------------|--|
| <b>System Specifications (MUX + Buffer + PGA + ADC)</b> |                                  |                       |      |      |                   | <b>Note 1</b>  |
| SYS <sub>DNL</sub>                                      | System DNL                       | -1.0                  | ±0.5 | +2.3 | LSB               | Gain=1<br>Gain=10  |
| SYS <sub>LIN</sub>                                      | System Linearity                 |                       | ±6.0 |      | LSB               |  |
| SYS <sub>GE</sub>                                       | System Gain Error                | -5.0                  |      | +5.0 | %                 |  |
| IRN   | Input Referred Noise             |                       | 1.5  |      | mV <sub>rms</sub> |  |
|   | Input Referred Noise             |                       | 0.5  |      | mV <sub>rms</sub> |  |
| <b>System Timing Specifications</b>                     |                                  |                       |      |      |                   |  |
| tcklw   | ADCCLK Low Pulse Width           | 50                    | 83   |      | ns                | SYNCH must rise equal to<br>or after ADCCLK, See Figure 18<br>Note 2 |
| tckhw   | ADCCLK High Pulse Width          | 70                    | 83   |      | ns                |  |
| tckpd   | ADCCLK Period                    | 120                   | 166  |      | ns                |  |
| tsypw   | SYNCH Pulse Width                | 30                    |      |      | ns                |  |
| trars   | Rising ADCCLK to rising<br>SYNCH | 0                     |      |      |                   |  |
| tclpw   | CLAMP Pulse Width                | 30                    |      |      | ns                |  |
|   |                                  |                       |      |      |                   |  |
| <b>Write Timing Specifications</b>                      |                                  |                       |      |      |                   |  |
| tsclkw  | SCLK Pulse Width                 | 40                    |      |      | ns                |  |
| tdz   | LD Low to SCLK High              | 20                    |      |      | ns                |  |
| tds   | Input Data Set-up Time           | 20                    |      |      | ns                |  |
| tdh   | Input Data Hold Time             | 0                     |      |      | ns                |  |
| tdl   | SCLK High to LD High             | 50                    |      |      | ns                |  |
|   |                                  |                       |      |      |                   |  |
| <b>ADC Digital Output Specifications</b>                |                                  |                       |      |      |                   |  |
| tap   | Aperture Delay                   |                       | 10   |      | ns                | 3ch Pixel Md<br>Config 00, 11<br>Config 01, 10                       |
| tdv   | Output Data Valid                | 40                    |      |      | ns                |  |
| t <sub>sa</sub>   | SYNCH to ADCCLK                  | 15                    |      |      | ns                |  |
| tlat  | Latency                          |                       | 8    |      | cycles            |  |
| tlat  | Latency                          |                       | 6    |      | pixels            |  |
|   |                                  |                       |      |      |                   |  |
| <b>Digital Input Specifications</b>                     |                                  |                       |      |      |                   |  |
| V <sub>IH</sub>   | Input High Voltage               | AV <sub>DD</sub> -2.5 |      |      | V                 |  |
| V <sub>IL</sub>   | Input Low Voltage                |                       |      | 1    | V                 |  |
| I <sub>IH</sub>   | High Voltage Input Current       |                       | 5    |      | µA                |  |
| I <sub>IL</sub>   | Low Voltage Input Current        |                       | 5    |      | µA                |  |
| C <sub>IN</sub>   | Input Capacitance                |                       | 10   |      | pF                |  |
|   |                                  |                       |      |      |                   |  |

**Note 1:** System performance is specified for typical digital system timing specifications.

**Note 2:** The actual minimum 'tclpw' is dependent on the external capacitor value, the CIS output impedance. During 'clamp' operation, sufficient time needs to be allowed for the external capacitor to charge up to the correct operating level. Refer to the description in Theory of Operation, CIS Config.

## ELECTRICAL CHARACTERISTICS (CONT'D)

Test Conditions:  $AV_{DD}=DV_{DD}=5V$ ,  $ADCCLK=6MHz$ , 50% Duty Cycle,  $T_A=25^{\circ}C$  unless otherwise specified.

| Symbol                               | Parameter                         | Min. | Typ. | Max. | Unit    | Conditions                  |
|--------------------------------------|-----------------------------------|------|------|------|---------|-----------------------------|
| <b>Digital Output Specifications</b> |                                   |      |      |      |         |                             |
| $V_{OH}$                             | Output High Voltage               | 80   |      |      | (%)     |                             |
| $DV_{DD}$                            | $I_L=1mA$                         |      |      |      |         |                             |
| $V_{OL}$                             | Output Low Voltage                |      |      | 20   | (%)     |                             |
| $DV_{DD}$                            | $I_L=-1mA$                        |      |      |      |         |                             |
| $I_{OZ}$                             | Output High-Z Leakage Current     | -10  |      | 10   | $\mu A$ |                             |
| $C_{OUT}$                            | Output Capacitance                |      | 10   |      | pF      |                             |
| SR                                   | Slew Rate (10% to 90% $DV_{DD}$ ) | 2    |      | 15   | ns      | $C_L=10pF$ , $DV_{DD}=3.3V$ |

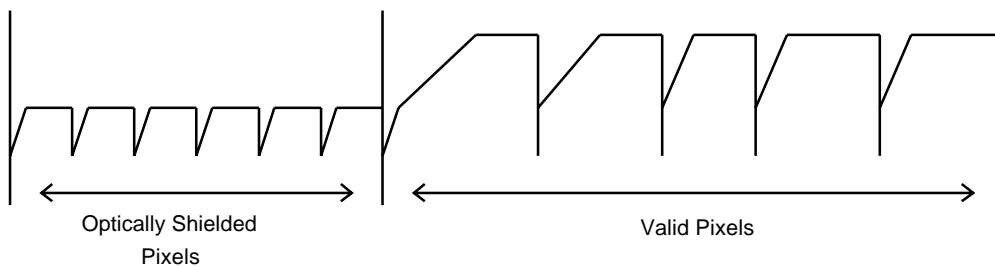
## THEORY OF OPERATION

### CIS Configuration (Contact Image Sensor)

The XRD9824 has two configurations for CIS applications. Each configuration is set by the control registers accessed through the serial port.

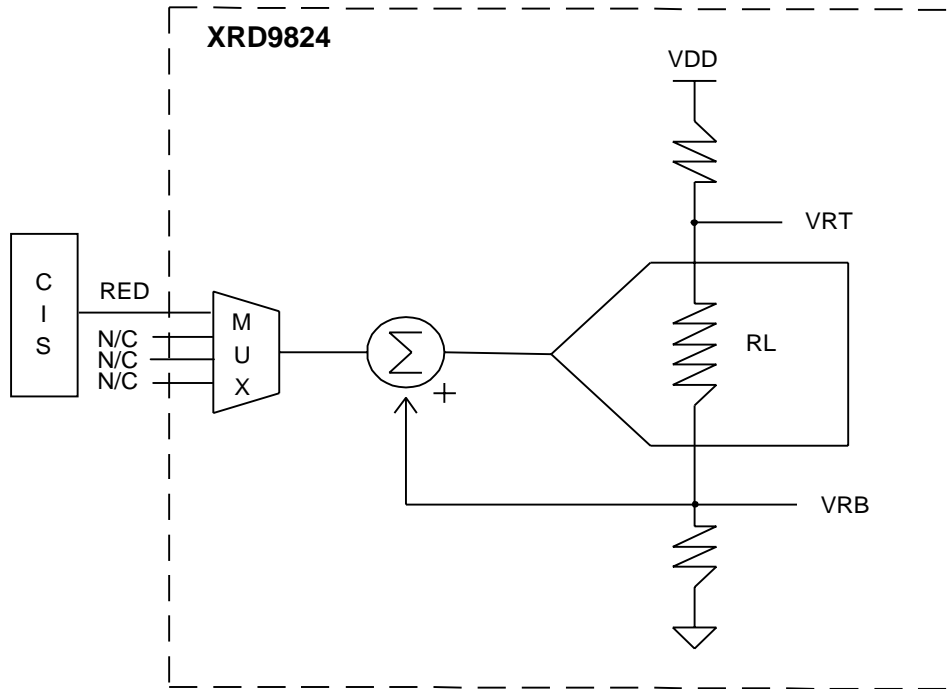
#### Mode 1. DC Coupled

If the CIS does not have leading or trailing black pixels as shown in Figure 2, then DC couple the CIS output to the XRD9824 input.



**Figure 2. Typical Output CIS Mode**

Adjust the offset of the CIS (-100 mV to 500 mV) by setting the internal registers of the XRD9824 to set the black pixel value when the LEDs of the CIS are off. When the LEDs are on, use the XRD9824 Programmable Gain to maximize the ADCs dynamic range. Figure 3 shows a typical application for a CIS with an offset of -100mV to 500mV.

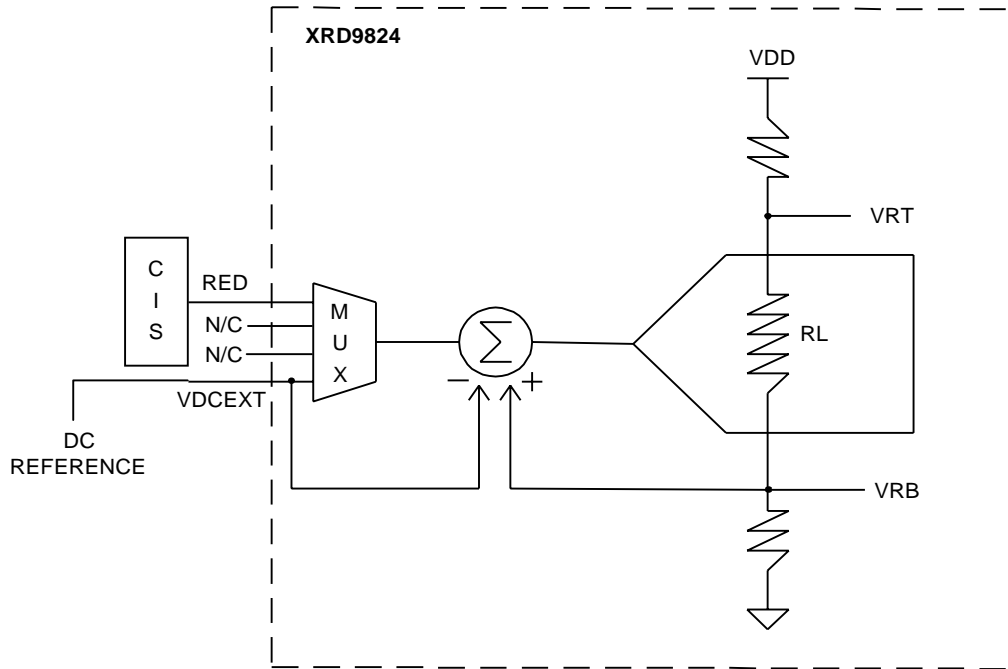


**Figure 3. Application with Offset in the Range (-100mv to 500mv)**

The input is added to VRT before the signal passes through the ADC. If the CIS output is zero, then the output of the ADC will be zero code. This enables the CIS to be referenced to the bottom ladder reference voltage to use the full range of the ADC.

Some CIS sensors have an output with an offset voltage of greater than 500mV. If the CIS output is

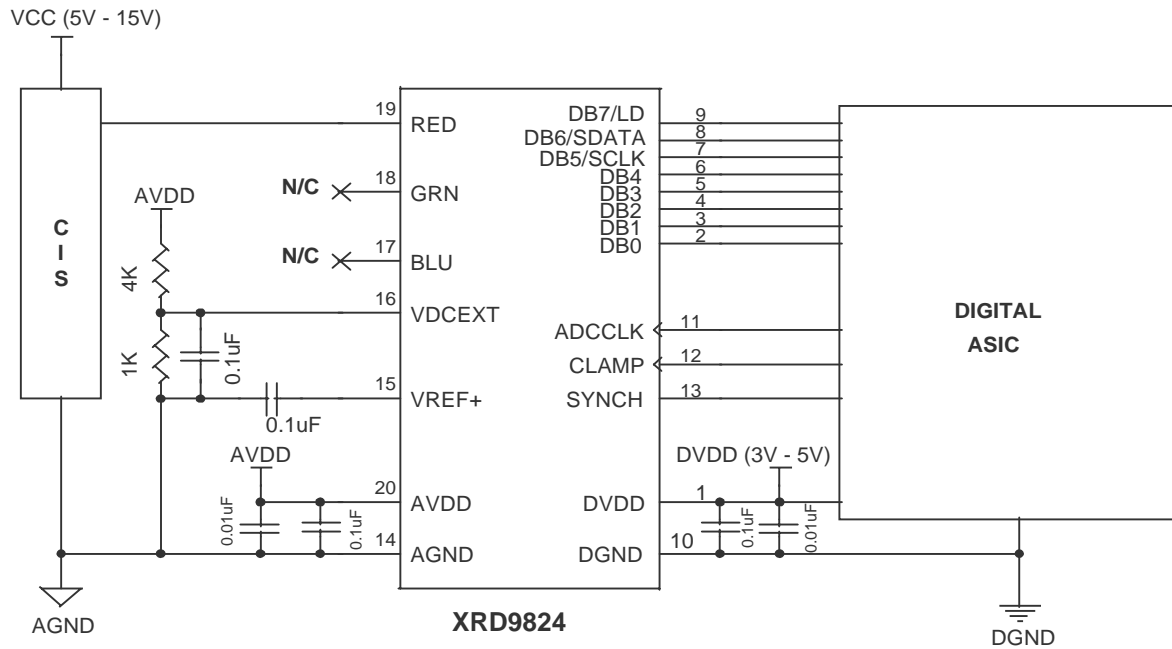
beyond the offset range of the XRD9824 (see Offset Control DAC, Pg. 28) set the internal mode registers to external reference. An external reference voltage equal to the value of the CIS offset voltage can be applied to VDCEXT (Figure 4) in order to meet the dynamic range of the XRD9824. Figure 4 is a diagram of the XRD9824 in the external reference mode for CIS, DC coupled applications.



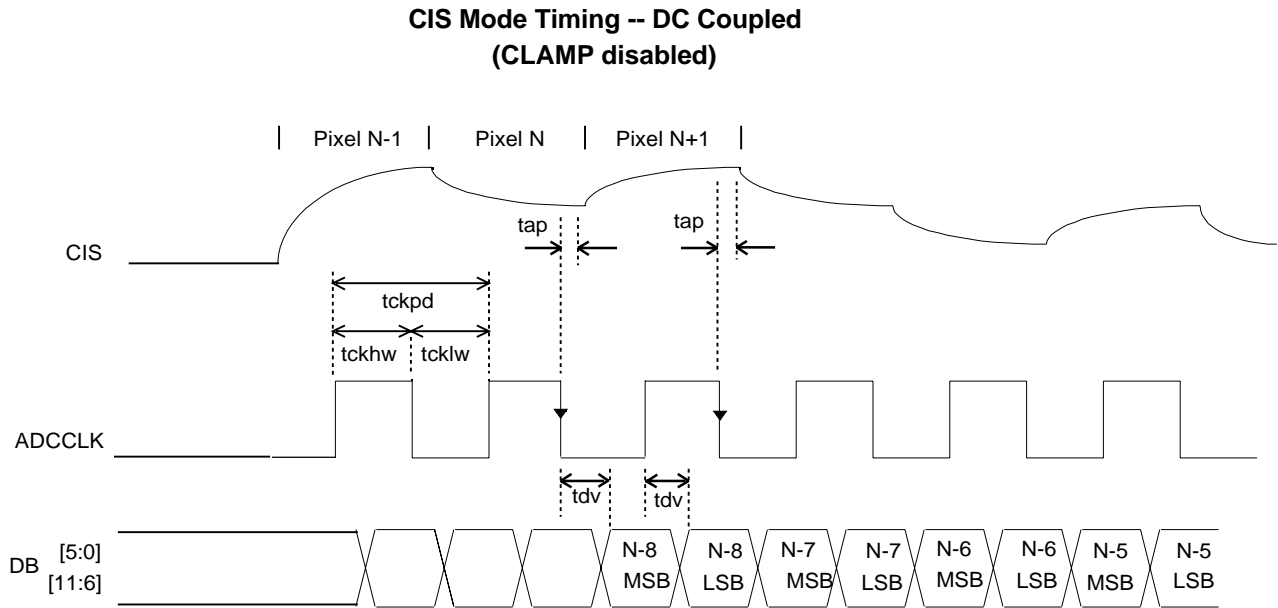
**Figure 4. Application with Offset Greater Than (-100mv to 500mv)**

The DC reference voltage applied to VDCEXT does not have to be accurate. The internal offset DAC voltage is still used in this mode for fine adjustment.

VDCEXT cannot be used as an input from the CIS. Any signal applied to VDCEXT will be subtracted from the output signal of the multiplexer.



**Figure 5. Typical Application Circuitry CIS DC Coupled Non-Inverted Mode**



**Figure 6. Timing Diagram for Figure 5**

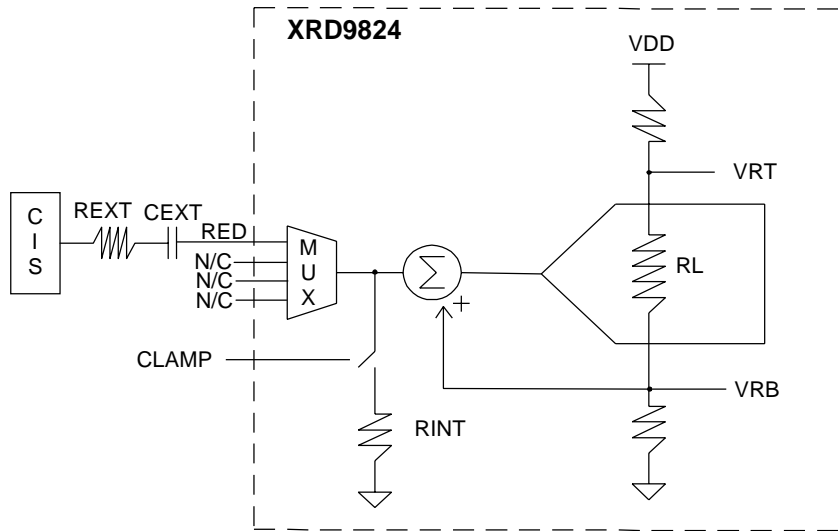
| ADCCLK | Events   |
|--------|--|
| ↓      | ADC Sample & PGA Start Tracking next Pixel<br>MSB Data Out |
| ↑      | LSB Data Out   |
| HI     | ADC Track PGA Output                                       |
| LO     | ADC Hold/Convert   |

**Table 1.**

## Mode 2. AC Coupled

If the CIS signal has a black reference for the video signal, an external capacitor  $C_{EXT}$  is used. When CLAMP (clamp) pin is set high an internal switch allows

one side of the external capacitor to be set to ground. It then is level shifted to correspond to the bottom ladder reference voltage of the ADC (Figure 7).



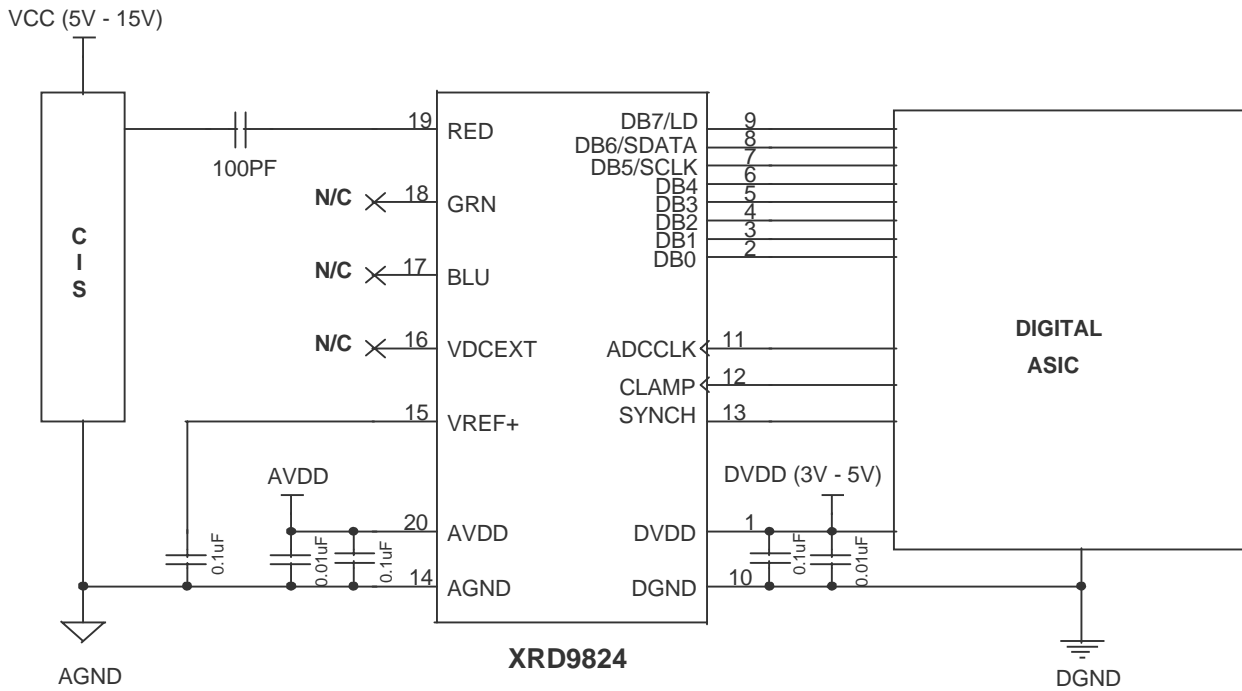
**Figure 7. CIS AC Coupled Application**

This value corresponds to the black reference of the image sensor. When the CLAMP pin is set back to low, the ADC samples the video signal with respect to the black reference. The typical value for the external capacitor is 100pF. This value should be adjusted according to the time constant (Tc) needed in a particular application. The CLAMP pin has an internal 150 ohm impedance ( $R_{INT}$ ) which is in series with the external capacitor ( $C_{EXT}$ ).

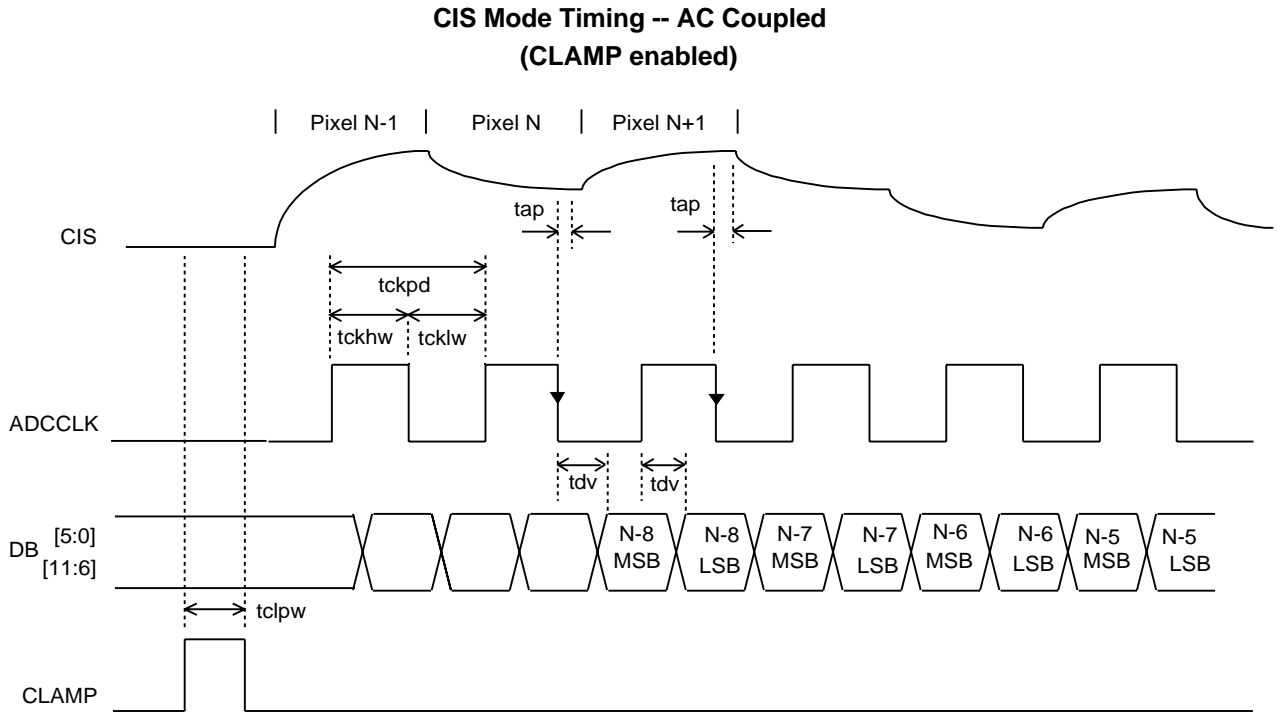
$$\text{Therefore, } T_c = 1/R_{INT} C_{EXT}$$

If the input to the external capacitor has a source impedance ( $R_{EXT}$ ), then:

$$T_c = 1/(R_{INT} + R_{EXT}) C_{EXT}$$



**Figure 8. Typical Application Circuitry CIS AC Coupled Non-Inverted**



**Figure 9. Timing Diagram for Figure 8**

| ADCCLK | Events   |
|--------|--|
| ↓      | ADC Sample & PGA Start Track of next Pixel<br>MSB Data Out |
| ↑      | LSB Data Out   |
| HI     | ADC Track PGA Output                                       |
| LO     | ADC Hold/Convert   |

**Table 3.**

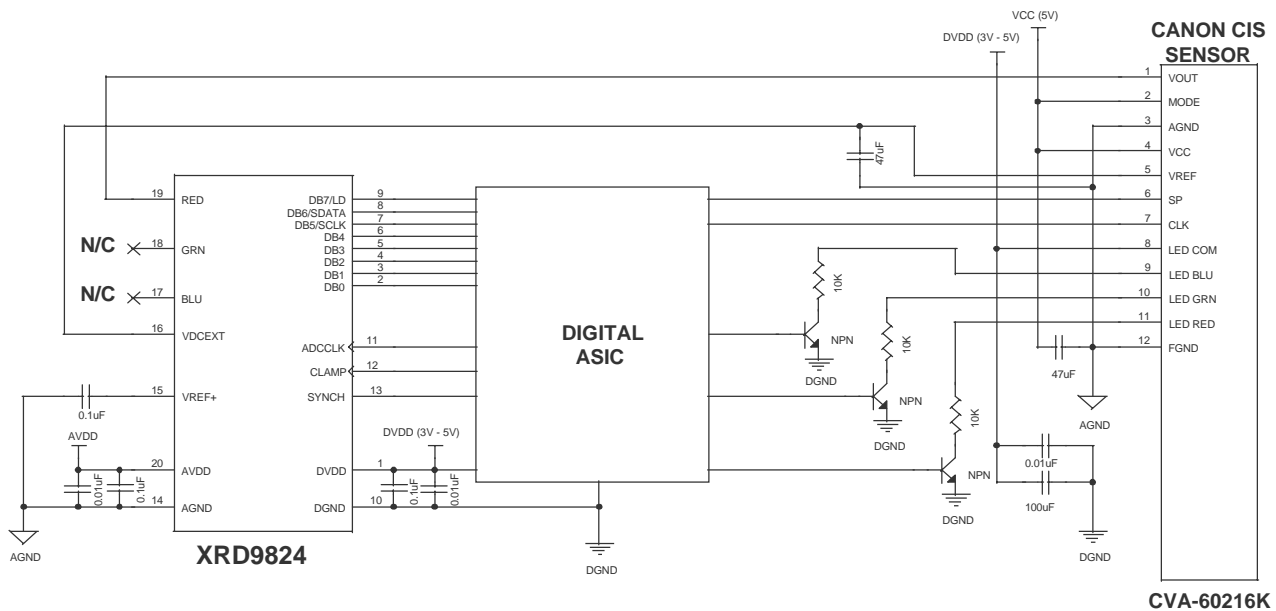
| CLAMP | Events  |
|-------|---|
| HI    | PGA Tracks $V_{CLAMP}$ & $C_{EXT}$ is Charged to                                    |
| LO    | $V_{BLACK} - V_{CLAMP}$ , which is equal to $V_{BLACK}$<br>PGA Tracks $V_{IN_{PP}}$ |

**Table 4.**

## Internal CIS Reference Circuit (DB 4 = 1)

The XRD9824 has an internal register reserved for interfacing to the Canon CIS model number CVA-60216K. When this register is selected, the VDCEXT (Pin 16) becomes an output voltage of 1.24 volts. This voltage can be directly connected to the VREF (Pin 15) of the Canon sensor. This reduces the amount of

components needed for biasing the Canon CIS sensor (the external diodes and resistors typically used in this application have been included inside the XRD9824 for this mode of operation). Below is a typical application circuit using the XRD9824 and the Canon CVA-60216K CIS sensor.

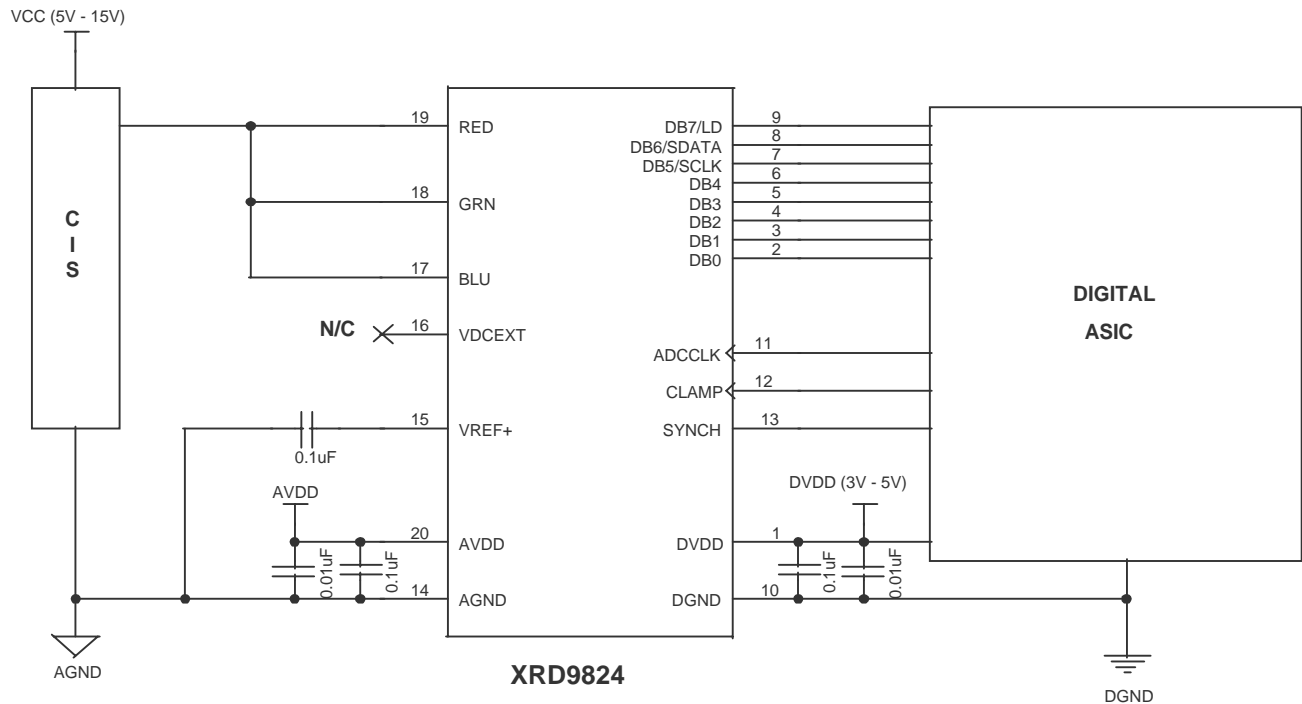


**Figure 10. Typical Application Circuitry Internal CIS Reference Circuit Mode  
CANON CIS Sensor, Model #CVA=60216k**

**CIS Line-By-Line Rotating Gain and Offset  
(Configuration DB1 = 1, DB0 = 1)**

Line-by-line rotating gain and offset minimizes the amount of write cycles per scan. Pre-loaded values of gain and offset can be loaded for each color before the first line is scanned. Each gain and offset is cycled

through line-by-line so that the gain and offset do not have to be loaded in between lines. Below is the typical application circuit and timing for this configuration.



**Figure 11. Typical Application Circuitry Internal CIS Rotating Gain and Offset Line-By-Line**

## CIS Rotating Gain and Offset Line-By-Line (Md 11)

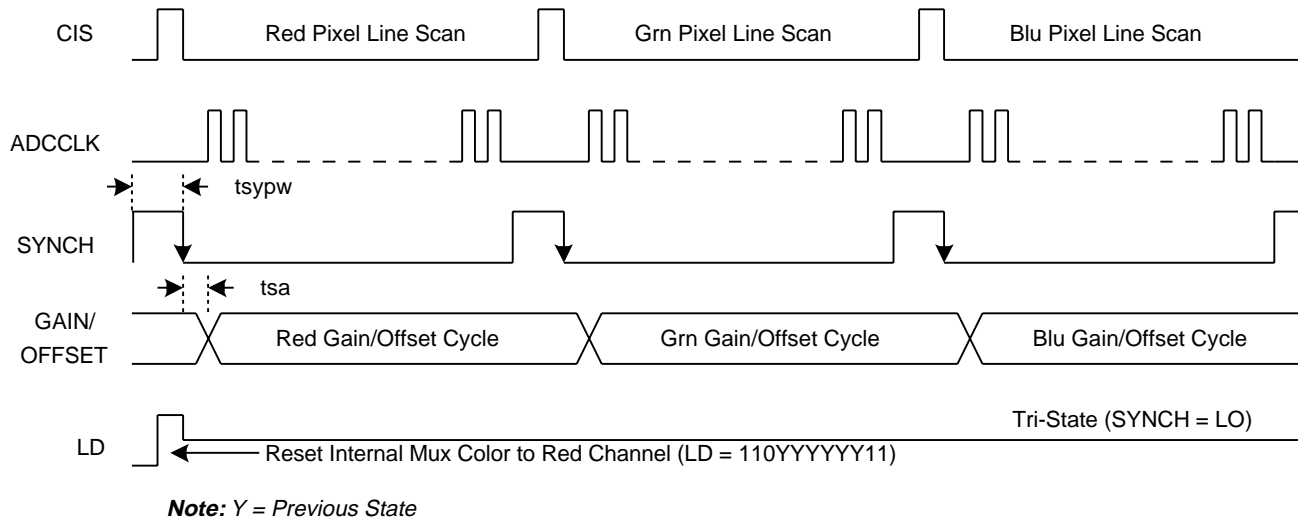


Figure 12. Timing Diagram for Figure 11

### CCD Configuration (Charge Coupled Device)

#### Mode 1. AC Coupled

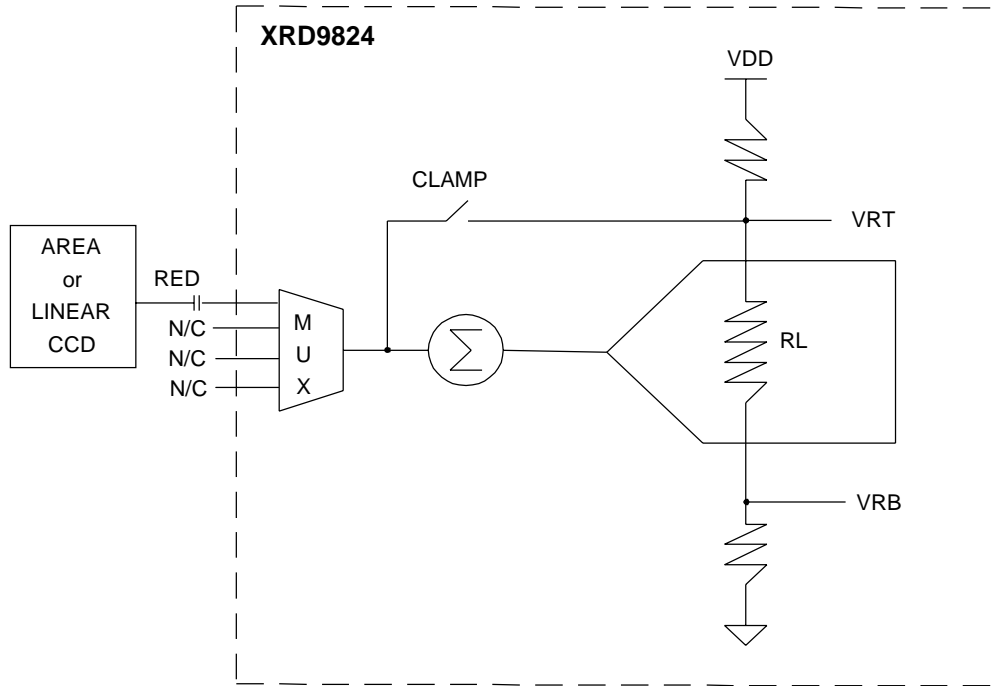
In the CCD configuration of operation, an external capacitor needs to be chosen according to the equations below. The typical value for the external capacitor is 100pF. This value should be adjusted according to the time constant ( $T_c$ ) needed in a particular application. The CLAMP pin has an internal 150 ohm impedance ( $R_{INT}$ ) which is in series with the external capacitor ( $C_{EXT}$ ).

$$\text{Therefore, } T_c = 1 / (R_{INT} \cdot C_{EXT})$$

If the input to the external capacitor has a load impedance ( $R_{EXT}$ ), then

$$T_c = 1 / (R_{INT} + R_{EXT}) \cdot C_{EXT}$$

When CLAMP (clamp) pin is set high an internal switch allows one side of the external capacitor to be set to VRT (Figure 13). This value corresponds to the black reference of the CCD. When the CLAMP pin is set back to low, the ADC samples the video signal with respect to the black reference. The difference between the black reference and the video signal is the actual pixel value of the video content. Since this value is referenced to the top ladder reference voltage of the ADC a zero input signal would yield a full scale output code. Therefore, the output of the conversion is inverted (internally) to correspond to zero scale output code.

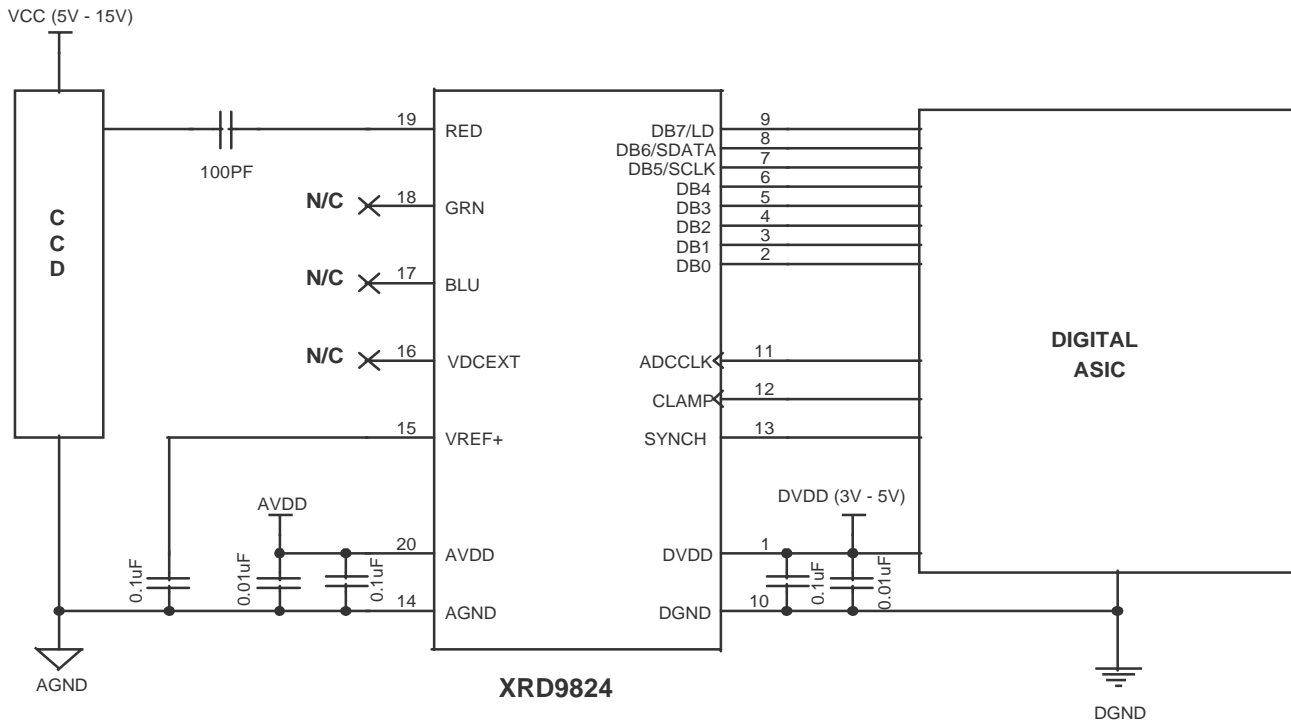


**Figure 13. CCD AC Coupled Application**

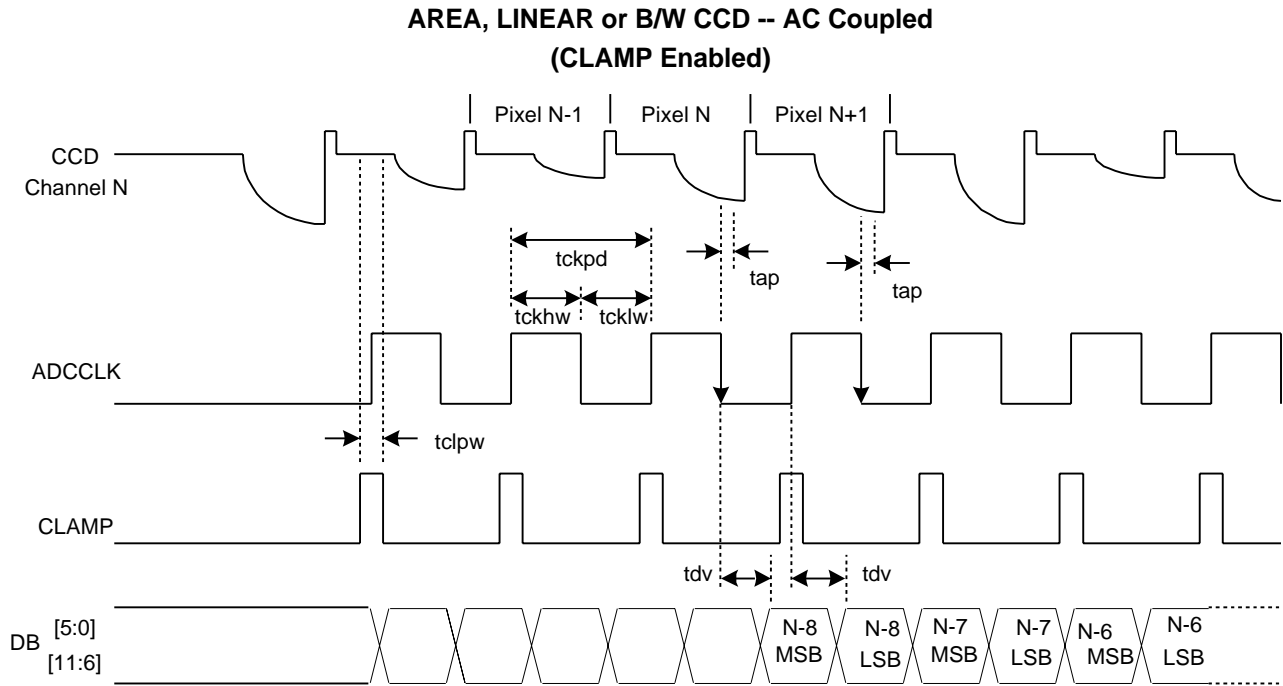
**Area or Linear CCD Applications**

Figure 13 is a block diagram for applications with Area or Linear CCDs (The timing for Area CCDs and B/W CCDs is the same). For Area or Linear CCD applications, a global offset is loaded into the serial port at the beginning of a line. The gain is set to adjust for the highest color intensity of the CCD output. Once the

pixel values have been sampled, the gain and offset are adjusted at the beginning of the next line. For example, if there is a line-to-line variation between the black reference pixels, the offset is adjusted. The gain is always adjusted for the highest color intensity.



**Figure 14. Typical Application Circuitry Single Channel CCD AC Coupled Inverted Mode**



**Figure 15. Timing Diagram for Figure 14**

**Triple Channel CCD Application**

Figure 16, is a block diagram for pixel-by-pixel applications with triple channel CCDs. During the optically shielded section of a pixel, CLAMP must go high to store the black reference on each capacitor to the

input. The gain and offset is automatically rotated to adjust for each channel input. The MSBs are available on the output bus on the falling edge of ADCCLK. The LSBs are available on the rising edge of ADCCLK.

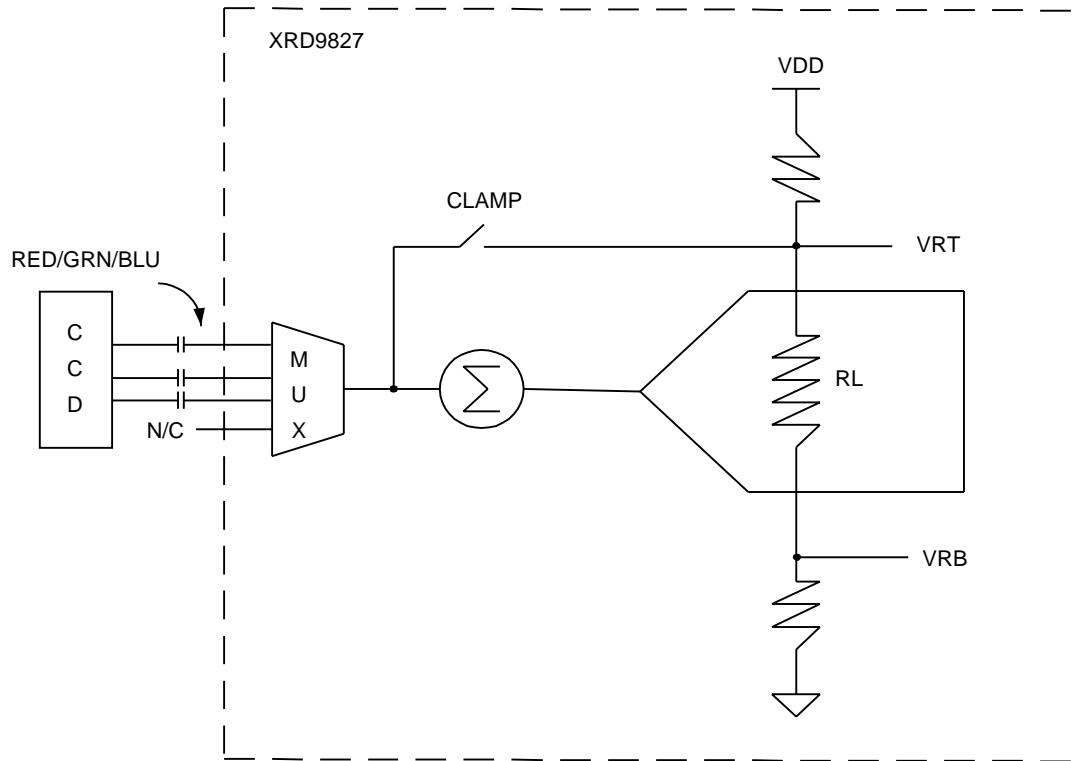
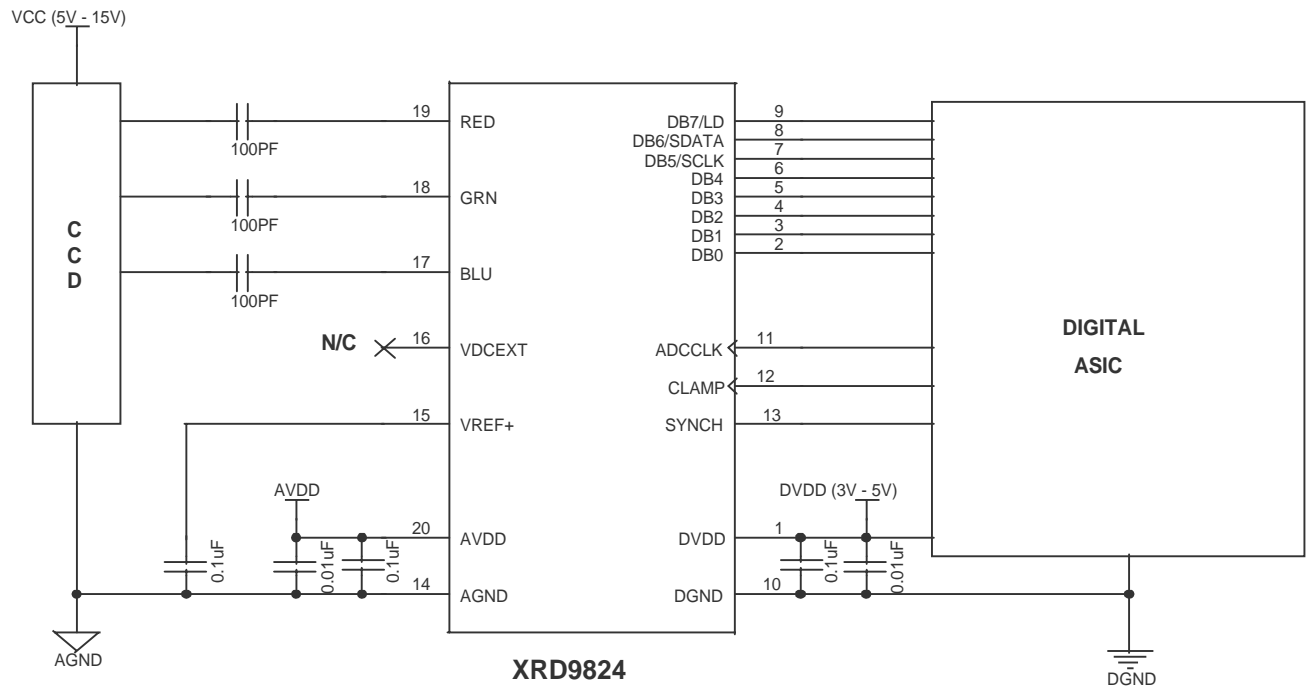
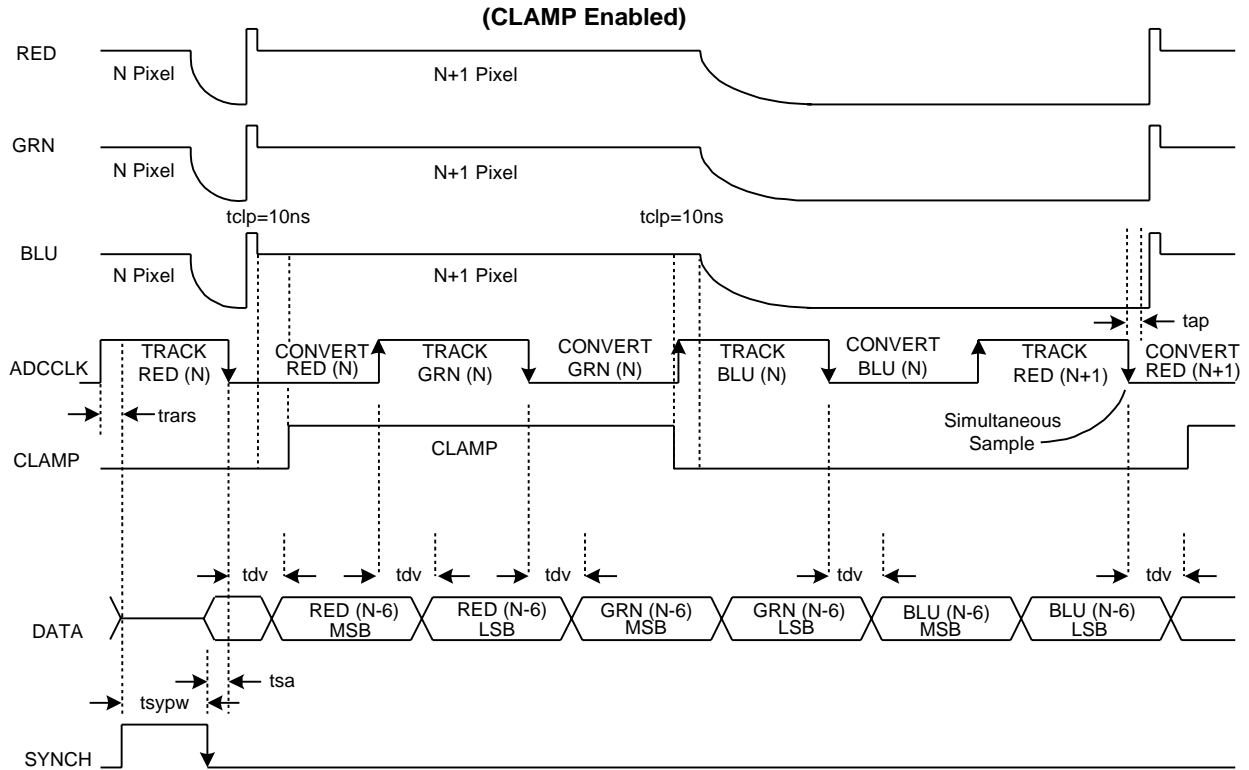


Figure 16. CCD AC Coupled Application



**Figure 17. Typical Application Circuitry Triple Channel CCD  
AC Coupled Inverted Mode**

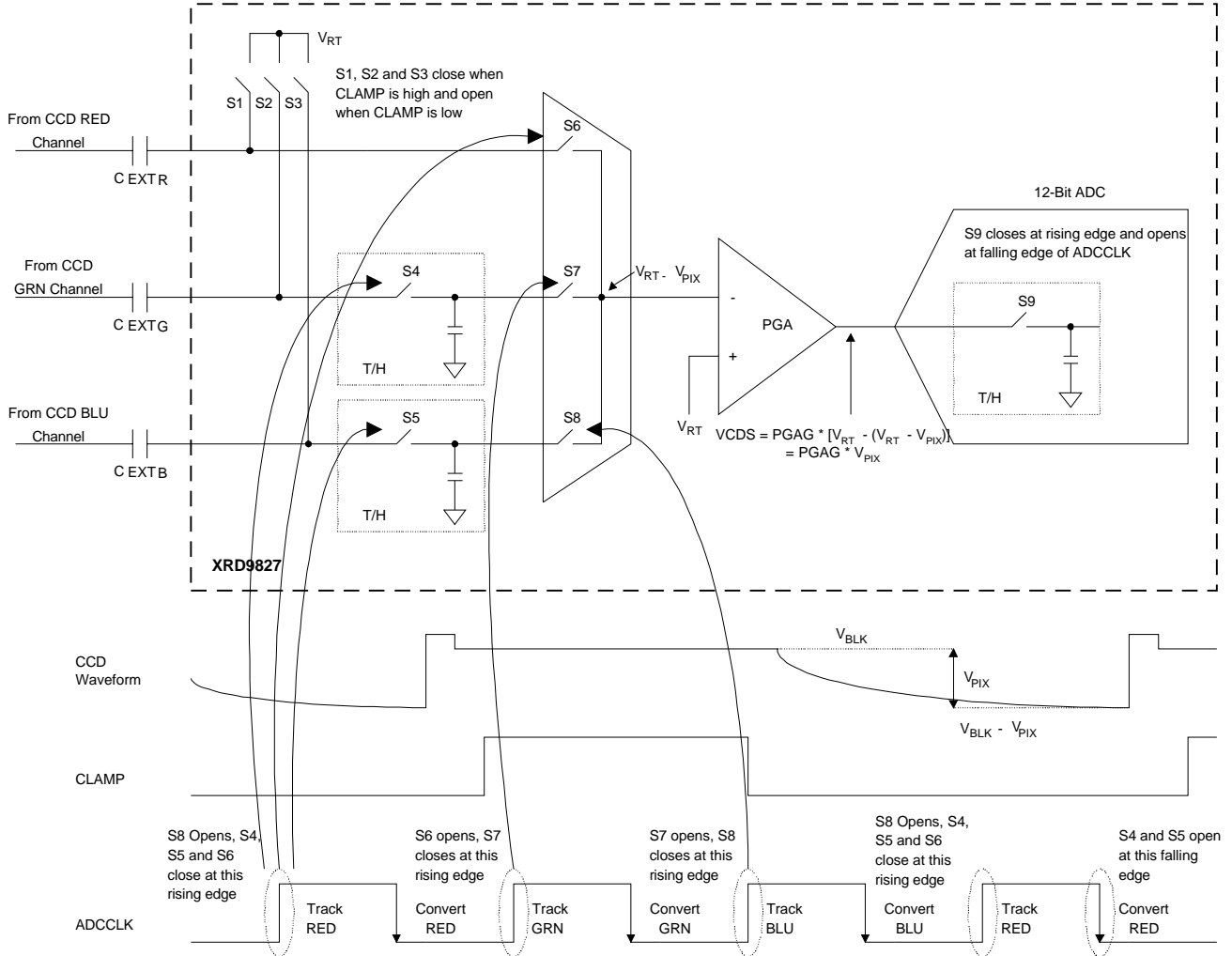
## PIXEL-BY-PIXEL 3 CHANNEL CCD -- AC Coupled



**Figure 18. Timing Diagram for Figure 17**

| ADCCLK | Events   |
|--------|--|
| 3rd ↓  | Simultaneous RED/GRN/BLU Sample Every 3rd CLK.<br>Convert RED, S/H GRN, S/H BLU. |
| All ↓  | MSB Data Out   |
| ↑      | LSB Data Out   |
| HI     | ADC Track PGA Output   |
| LO     | ADC Hold/Convert   |
| CLAMP  | Events   |
| HI     | Internal Clamp Enabled   |
| LO     | Internal RED/GRN/BLU Tracking Enabled  |
| SYNCH  | Events   |
| HI     | Reset Internal Mux to Red, Output Bus is Tri-stated                              |
| LO     | Increment Mux Color on Falling Edge of ADCCLK                                    |

**Table 5.**



**Figure 19. CDS Timing (Triple Channel)  
Mode: 110 00001110**

## Mode 2. DC Coupled

Typical CCDs have outputs with black references. Therefore, DC Coupled is not recommended for CCD applications.

### Offset Control DAC

The offset DAC is controlled by 8 bits. The offset range is 800 mV ranging from -200 mV to +600 mV (when DB5 is set to 0) and -400 mV to +400 mV (when DB5 is set to 1). Therefore, the resolution of the 8-Bit offset DAC is 3.14 mV. However, the XRD9824 has +/- 100 mV reserved for internal offsets. Therefore, the effective range for adjusting for CIS offsets or black reference is 600 mV. The offset adjustment is used primarily to correct for the difference between the black level of the image sensor and the bottom ladder reference voltage (VRB) of the ADC. By adjusting the black level to correspond to VRB, the entire range of the ADC can be used.

If the offset of the CIS output is greater than 500 mV an external reference can be applied to VDCEXT. The external reference can be used to adjust for large offsets only when the internal mode is configured through the serial port.

Since the offset DAC adjustment is done before the gain stage, it is gain-dependent. For example, if the gain needs to be changed between lines (red to blue, etc.), the offset is calibrated before the signal passes through the PGA.

### PGA (Programmable Gain Amplifier) DAC

The gain of the input waveform is controlled by a 6-Bit PGA. The PGA is used along with the offset DAC for the purpose of using the entire range of the ADC. The PGA has a linear gain from 1 to 10. Figure 19 is a plot of the transfer curve for the PGA gain.

PGA GAIN TRANSFER CURVE  
GAIN 1 - 10

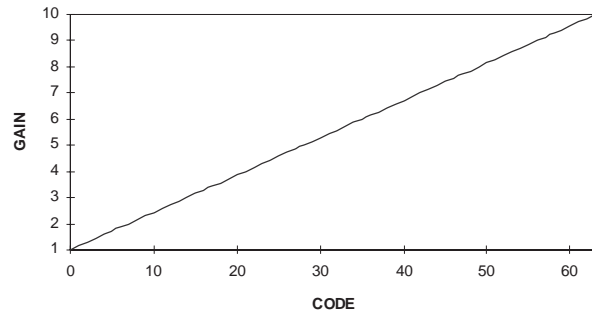


Figure 20. Transfer Curve for the 6-Bit PGA

After the signal is level shifted to correspond with the bottom ladder reference voltage, the system can be calibrated such that a white video pixel can represent the top ladder reference voltage to the ADC. This allows for a full scale conversion maximizing the resolution of the ADC.

### Analog to Digital Converter

The ADC is a 14-bit, 10 MSPS analog-to-digital converter for high speed and high accuracy. The ADC uses a subranging architecture to maintain low power consumption at high conversion rates. The output of the ADC is on 8-bit databus. The 8-bit databus supports 8x6 output data. ADCCLK samples the input on its falling edge. After the input is sampled, the MSB is latched to the output drivers. On the rising edge of the ADCCLK, the LSB is latched to the output drivers. The output needs to be demultiplexed with external circuitry or a digital ASIC. There is an 8 clock cycle latency (Config 00, 11) or 6 pixel count latency (Config 01, 10) for the analog-to-digital converter.

The  $V_{RT}$  and  $V_{RB}$  reference voltages for the ADC are generated internally, unless the external  $V_{RT}$  is selected. In the external  $V_{RT}$  mode, the  $V_{RT}$  voltage is set through the VREF+ pin. This allows the user to select the dynamic range of the ADC.

## Serial Load Control Registers

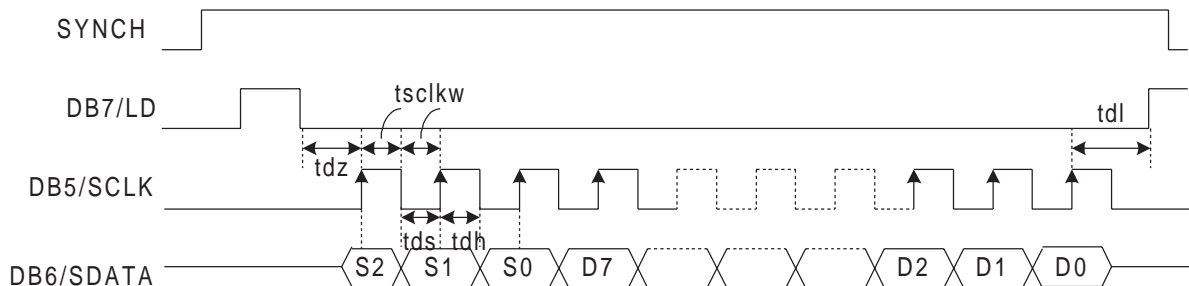
The serial load registers are controlled by a three wire serial interface through the bi-directional parallel port to reduce the pin count of this device. When SYNCH is set to high, the output bus is tri-stated and the serial interface is activated. DB7/LD, DB5/SCLK and DB6/SDATA are the three input signals that control this process. The DB7/LD signal is set low to initiate the loading of the internal registers.

There are internal registers that are accessed via an 11-bit data string. Data is shifted in on the rising edge of SCLK and loaded to the registers on the rising edge of LD. The data on pin DB6/SDATA is latched automatically after eleven DB5/SCLKs have been counted. If eleven clocks are not present on DB5/SCLK before the DB7/LD signal returns high, no data will be loaded into the internal registers. If more than 11 clocks are present on DB5/SCLK, the additional clocks will be ignored. The data corresponding to the first eleven DB5/SCLKs will be loaded only.

The first three MSBs choose which internal register will be selected. The remaining 8 LSBs contain the data needed for programming the internal register for a particular configuration.

## Power-Up State of the Internal Registers

The control register settings upon initial power-up are for CIS, DC Coupled configuration (VRT is set to internal, Input DC Reference=AGND and the input to the ADC is selected through the RED channel). Gain is unity and Offset is set to zero. The test modes are disabled in the power-up state.



**Figure 21. Write Timing**

## Output Bus Format

ADC Output → DO13(MSB):DO0(LSB)

|     | DB7  | DB6  | DB5  | DB4  | DB3 | DB2 | DB1 | DB0 |
|-----|------|------|------|------|-----|-----|-----|-----|
| MSB | DO13 | DO12 | DO11 | DO10 | DO9 | DO8 | DO7 | DO6 |
| LSB | DO5  | DO4  | DO3  | DO2  | DO1 | DO0 | X   | X   |

**Table 9. 8 MSB + 6 LSB Output Bus Format**

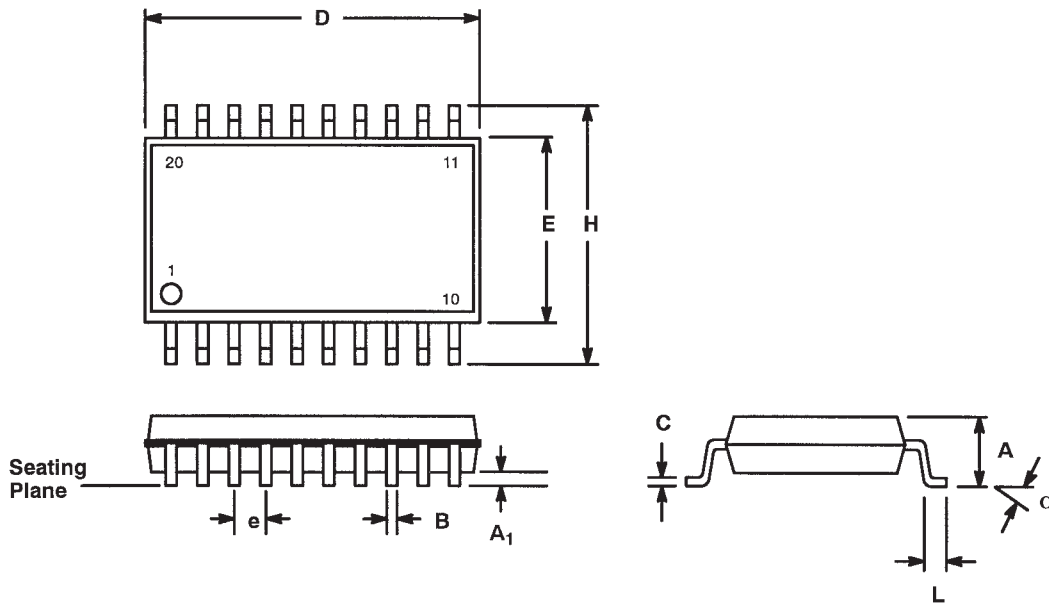
**Note :** *These are the control register settings upon initial power-up. The previous register settings are retained following a logic power-down initiated by the power down bit except the signal configuration. When de-selecting the power down bit (D7 = 0, Normal), the signal configuration (D5 and D0) has to be reprogrammed.*

## Control Registers

| Function (Register S2/S1/S0) | D7   | D6  | D5   | D4  | D3  | D2  | D1  | D0   | Power-up State (Note 1) |
|------------------------------|--|---|--|---|---|---|---|--|-------------------------|
| <b>Red Gain (000)</b>        | G5 (MSB)   | G4  | G3   | G2  | G1  | G0 (LSB)  | X   | X  | 000000XX                |
| <b>Red Offset (001)</b>      | O7 (MSB)   | O6  | O5   | O4  | O3  | O2  | O1  | O0 (LSB)                                       | 01000000                |
| <b>Grn Gain (010)</b>        | G5 (MSB)   | G4  | G3   | G2  | G1  | G0 (LSB)  | X   | X  | 000000XX                |
| <b>Grn Offset (011)</b>      | O7 (MSB)   | O6  | O5   | O4  | O3  | O2  | O1  | O0 (LSB)                                       | 01000000                |
| <b>Blu Gain (100)</b>        | G5 (MSB)   | G4  | G3   | G2  | G1  | G0 (LSB)  | X   | X  | 000000XX                |
| <b>Blu Offset (101)</b>      | O7 (MSB)   | O6  | O5   | O4  | O3  | O2  | O1  | O0 (LSB)                                       | 01000000                |
| <b>Mode (110)</b>            | POWER DOWN<br><br>0: NORMAL<br><br>1: POWER DOWN | DIGITAL RESET<br><br>0: NO RESET<br><br>1: RESET (REGISTERS ARE RESET TO POWER-UP STATES) | $V_{RT}$<br><br>0: INTERNAL<br><br>1: EXTERNAL                         | INPUT DC REFERENCE ( $V_{DCREF}$ )<br><br>0: INTERNAL ( $V_{DCREF}=AGND$ )<br>1: EXTERNAL ( $V_{DCREF}=V_{DCEXT}$ ) | DC/AC<br><br>0: DC<br><br>1: AC                                       | SIGNAL POLARITY<br><br>0: Non-Inverted (CIS)<br>1: Inverted (CCD/CIS) | SIGNAL CONFIGURATION<br><br>00: Single-Channel RED input/gain/offset<br><br>01: Single-Channel RED input RED/GRN/BLU gain/offset cycle pixel-by-pixel<br><br>10: Triple-Channel RED/GRN/BLU input/gain/offset cycle pixel-by-pixel<br><br>11: Triple-Channel RED/GRN/BLU input/gain/offset cycle line-by-line |  | 00000000                |
| <b>Mode &amp; Test (111)</b> | TEST5<br><br>0: NORMAL<br><br>1: NOT USED        | OUTPUT DISABLE<br><br>0: OUTPUTS ENABLED<br><br>1: OUTPUTS DISABLED                       | OFFSET DAC RANGE<br><br>0: -200mV to +600mV<br><br>1: -400mV to +400mV | INTERNAL CIS REFERENCE CIRCUIT<br><br>0: NORMAL<br><br>1: REFERENCE CIRCUIT ENABLED                                 | TEST4<br><br>0: TEST4 DISABLED<br><br>1: OUTPUT OF BUFFER TIED TO BLU | TEST3<br><br>0: TEST3 DISABLED<br><br>1: OUTPUT OF PGA TIED TO VDCEXT | TEST2<br><br>0: TEST2 DISABLED<br><br>1: INPUT OF ADC TIED TO GRN   | TEST1<br><br>0: NORMAL<br><br>1: TEST1 ENABLED | 00000000                |

## 20 LEAD SMALL OUTLINE (300 MIL JEDEC SOIC)

Rev. 1.00

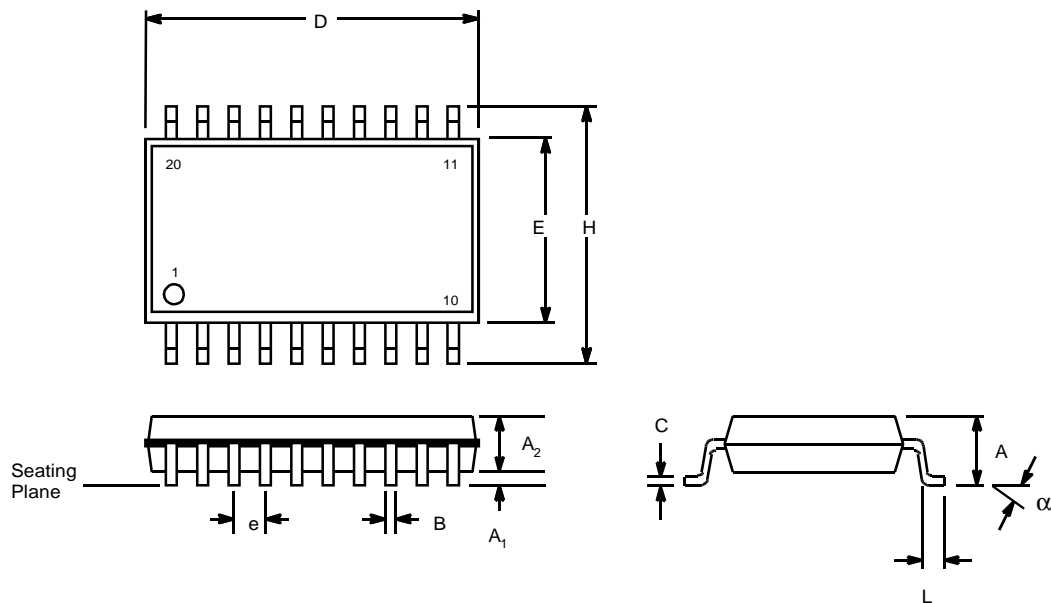


| SYMBOL         | INCHES    |       | MILLIMETERS |       |
|----------------|-----------|-------|-------------|-------|
|                | MIN       | MAX   | MIN         | MAX   |
| A              | 0.093     | 0.104 | 2.35        | 2.65  |
| A <sub>1</sub> | 0.004     | 0.012 | 0.10        | 0.30  |
| B              | 0.013     | 0.020 | 0.33        | 0.51  |
| C              | 0.009     | 0.013 | 0.23        | 0.32  |
| D              | 0.496     | 0.512 | 12.60       | 13.00 |
| E              | 0.291     | 0.299 | 7.40        | 7.60  |
| e              | 0.050 BSC |       | 1.27 BSC    |       |
| H              | 0.394     | 0.419 | 10.00       | 10.65 |
| L              | 0.016     | 0.050 | 0.40        | 1.27  |
| α              | 0°        | 8°    | 0°          | 8°    |

Note: The control dimension is the millimeter column

## 20 LEAD SHRINK SMALL OUTLINE PACKAGE (5.3 mm SSOP)

Rev. 2.00



| SYMBOL   | INCHES     |       | MILLIMETERS |      |
|----------|------------|-------|-------------|------|
|          | MIN        | MAX   | MIN         | MAX  |
| A        | 0.067      | 0.079 | 1.70        | 2.00 |
| A1       | 0.002      | 0.006 | 0.05        | 0.15 |
| A2       | 0.065      | 0.073 | 1.65        | 1.85 |
| B        | 0.009      | 0.015 | 0.22        | 0.38 |
| C        | 0.004      | 0.010 | 0.09        | 0.25 |
| D        | 0.272      | 0.296 | 6.90        | 7.50 |
| E        | 0.197      | 0.221 | 5.00        | 5.60 |
| e        | 0.0256 BSC |       | 0.65 BSC    |      |
| H        | 0.292      | 0.323 | 7.40        | 8.20 |
| L        | 0.022      | 0.037 | 0.55        | 0.95 |
| $\alpha$ | 0°         | 8°    | 0°          | 8°   |

Note: The control dimension is the inch column

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