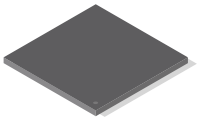
THE DATASHEET OF

VSP2254GSJR



36-MHz SAMPLE TWO CHANNEL CCD SIGNAL PROCESSOR

FEATURES

- **TWO CHANNEL CCD SIGNAL PROCESSING:**
  - **Correlated Double Sampling**
- **75-dB SNR**
- **14-BIT A/D CONVERSION:**
  - **No Missing Codes**
- **PORTABLE OPERATION:**
  - **Low Voltage: 2.7 V to 3.6 V**
  - **Low Power: 210 mW (typ) at 2.7 V**
  - **Power-Down Mode: 14 mW**

APPLICATIONS

- **Digital Video Camera (DVC)**
- **Digital Still Camera (DSC)**
- **Front End for Dual Channel CCD**

DESCRIPTION

The VSP2254 is a high-speed and high-resolution mixed-signal processing IC for CCD signal processing, which integrates two channels of correlated double sampling (CDS) and a 14-bit analog-to-digital converter. The VSP2254 also provides black level clamping for an accurate black level reference, input signal clamping, and offset correction of the CDS. The VSP2254 operates from 2.7 V to 3.6 V of single supply.

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

ORDERING INFORMATION

PRODUCT	PACKAGE	PACKAGE CODE	OPERATION TEMPERATURE RANGE	PACKAGE MARKING	ORDERING NUMBER(1)	TRANSPORT MEDIA
VSP2254GSJ	BGA 96	GSJ	–25°C to 85°C	VSP2254	VSP2254GSJ	Tray
					VSP2254GSJR	Tape and reel

(1) For the most current specification and package information, refer to our web site at www.ti.com.

ABSOLUTE MAXIMUM RATINGS

over operating free-air temperature range unless otherwise noted(1)

	UNITS
Supply voltage, V_{CC}, V_{DD}	4 V
Supply voltage differences, among V_{CC} terminals	±0.1 V
Ground voltage differences, AGND, DGND	±0.1 V
Digital input voltage	–0.3 V to (V_{DD} + 0.3 V)
Analog input voltage	–0.3 V to (V_{CC} + 0.3 V)
Input current (any pins except supplies)	±10 mA
Ambient temperature under bias	–40°C to 125°C
Storage temperature, T_{stg}	–55°C to 150°C
Junction temperature T_J	150°C
Lead temperature (soldering)	260°C, 5 s
Package temperature (IR reflow, peak)	260°C

(1) Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

all specifications at T_A = 25°C, all power supply voltages = 3 V, and conversion rate = 27 MHz, unless otherwise noted(1)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
	Resolution			14		Bits
	Channel			2		
	Maximum conversion rate		36			MHz
DIGITAL INPUTS						
	Logic family			CMOS		
V_{IT+}	Positive-going input threshold voltage			1.7		V
$V_{IT–}$	Negative-going input threshold voltage			1		V
I_{IH}	Input current	Logic high, V_{IN} = 3 V			±20	µA
I_{IL}		Logic low, V_{IN} = 0 V			±20	µA
	ADC clock duty cycle			50%		
	Input capacitance			5		pF
DIGITAL OUTPUT (Channel A/B)						
	Logic family			CMOS		
	Logic coding			Straight Binary		
V_{OH}	Output voltage	Logic high, I_{OH} = –2 mA	2.4			V
V_{OL}		Logic low, I_{OL} = 2 mA			0.4	V

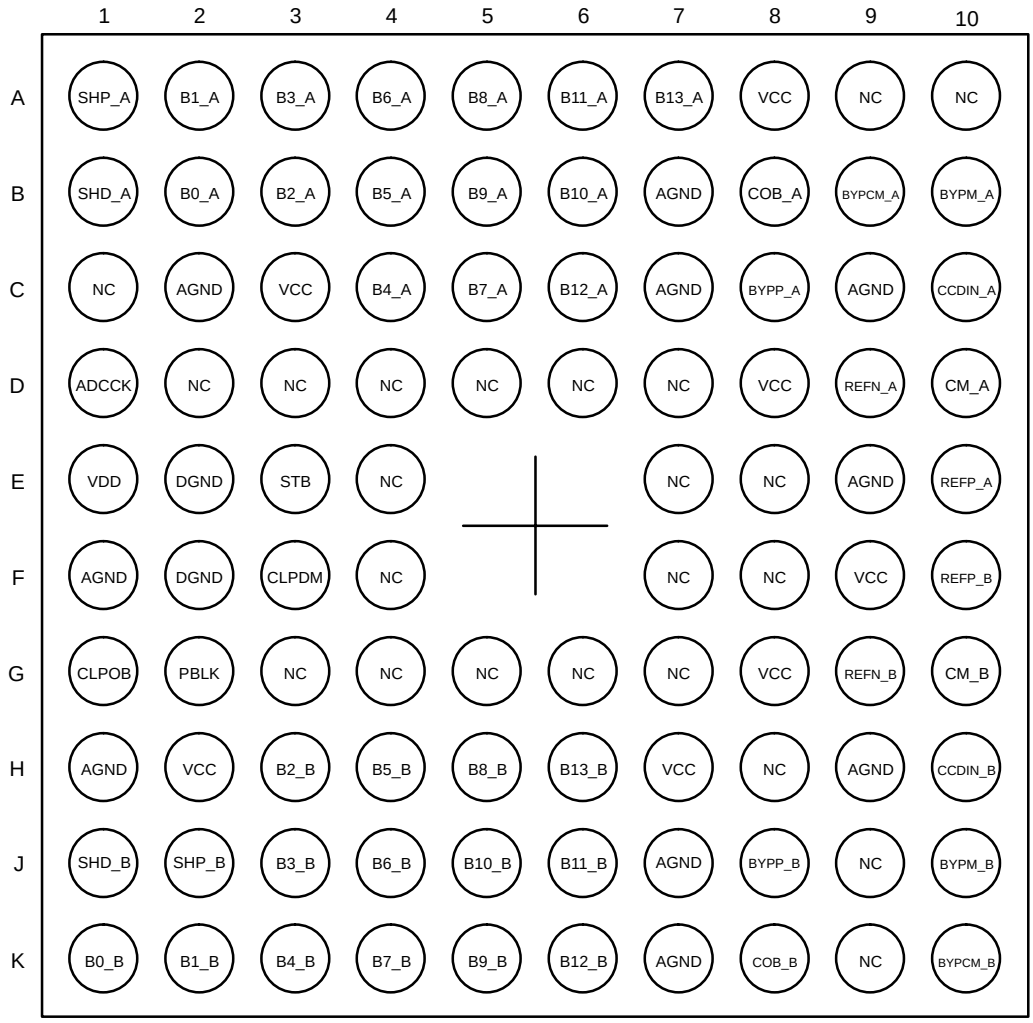
ELECTRICAL CHARACTERISTICS (continued)

all specifications at T_A = 25°C, all power supply voltages = 3 V, and conversion rate = 27 MHz, unless otherwise noted(1)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
ANALOG INPUT (Channel A/B)						
	Input signal level for FS out		900		1100	mV
	Input capacitance			10		pF
	Input limit		–0.3		3.3	V
TRANSFER CHARACTERISTICS (Channel A/B)						
	Differential nonlinearity			±2		LSB
	Integral nonlinearity			±8		LSB
	No missing codes			Assured		
	Step response settling time	Full-scale step input		1		pixels
	Overload recovery time	Step input from 1.8 V to 0 V		2		pixels
	Data latency			8 (fixed)		clocks
	Signal-to-noise ratio(1)	Grounded input cap		75		dB
	Channel separation			80		dB
	CCD offset correction range		–180		200	mV
	Optical black clamp level			512		LSB
CDS (Channel A/B)						
	Reference sample settling time	Within 1 LSB, driver impedance = 50 Ω		6.9		ns
	Data sample settling time	Within 1 LSB, driver impedance = 50 Ω		6.9		ns
INPUT CLAMP (Channel A/B)						
	Clamp-on resistance			400		Ω
	Clamp level			1.5		V
OBCLP LOOP						
	DAC resolution			10		bits
	Minimum DAC output current			±0.15		µA
	Maximum DAC output current			±153		µA
	Loop time constant	Time constant for ADCOUT code from 0 LSB to 1543 LSB (14 bit), C_{COB} = 0.1 µF		40.7		µs
	Slew rate	ADCOUT CODE above 1543 LSB (14 bit), C_{COB} = 0.1 µF		1530		V/s
REFERENCE (Channel A/B)						
	Positive reference voltage			1.75		V
	Negative reference voltage			1.25		V
POWER SUPPLY						
V_{CC}, V_{DD}	Supply voltage		2.7	3	3.6	V
P_D	Power dissipation	At V_{CC} = 3 V, f_{CLK} = 36 MHz		210		mW
		Power-down mode (f_{CLK} = 0 MHz)		14		mW
TEMPERATURE RANGE						
	Operation temperature		–25		85	°C
θ_{JA}	Thermal resistance			55		°C/W

(1) SNR = 20 log (full-scale voltage/rms noise)

PIN ASSIGNMENTS



NOTE: The corner of the A1 position is indicated on the device top by a dot.

Terminal Functions

TERMINAL NAME	TERMINAL NO.	TYPE(1)	DESCRIPTION
ADCCK	D1	DI	Clock for ADC output
AGND	B7, C2, C7, C9, E9, F1, H1, H9, J7, K7	P	Analog ground
B0_A	B2	DO	A-channel ADC output bit 0
B0_B	K1	DO	B-channel ADC output bit 0 (LSB)
B1_A	A2	DO	A-channel ADC output bit 1
B1_B	K2	DO	B-channel ADC output bit 1
B10_A	B6	DO	A-channel ADC output bit 10
B10_B	J5	DO	B-channel ADC output bit 10
B11_A	A6	DO	A-channel ADC output bit 11
B11_B	J6	DO	B-channel ADC output bit 11
B12_A	C6	DO	A-channel ADC output bit 12
B12_B	K6	DO	B-channel ADC output bit 12
B13_A	A7	DO	A-channel ADC output bit 13 (MSB)
B13_B	H6	DO	B-channel ADC output bit 13 (MSB)
B2_A	B3	DO	A-channel ADC output bit 2
B2_B	H3	DO	B-channel ADC output bit 2
B3_A	A3	DO	A-channel ADC output bit 3
B3_B	J3	DO	B-channel ADC output bit 3
B4_A	C4	DO	A-channel ADC output bit 4
B4_B	K3	DO	B-channel ADC output bit 4
B5_A	B4	DO	A-channel ADC output bit 5
B5_B	H4	DO	B-channel ADC output bit 5
B6_A	A4	DO	A-channel ADC output bit 6
B6_B	J4	DO	B-channel ADC output bit 6
B7_A	C5	DO	A-channel ADC output bit 7
B7_B	K4	DO	B-channel ADC output bit 7
B8_A	A5	DO	A-channel ADC output bit 8
B8_B	H5	DO	B-channel ADC output bit 8
B9_A	B5	DO	A-channel ADC output bit 9
B9_B	K5	DO	B-channel ADC output bit 9
BYPCM_A	B9	AO	A-channel CDS common reference, bypass-to-ground by a 0.1-μF capacitor
BYPCM_B	K10	AO	B-channel CDS common reference, bypass-to-ground by a 0.1-μF capacitor
BYPM_A	B10	AO	A-channel CDS negative reference, bypass-to-ground by a 500-pF to 1000-pF capacitor
BYPM_B	J10	AO	B-channel CDS negative reference, bypass-to-ground by a 500-pF to 1000-pF capacitor
BYPP_A	C8	AO	A-channel CDS positive reference, bypass-to-ground by a 500-pF to 1000-pF capacitor
BYPP_B	J8	AO	B-channel CDS positive reference, bypass-to-ground by a 500-pF to 1000-pF capacitor
CCDIN_A	C10	AI	A-channel CCD signal input
CCDIN_B	H10	AI	B-channel CCD signal input
CLPDM	F3	DI	Dummy clamp pulse, (active low)

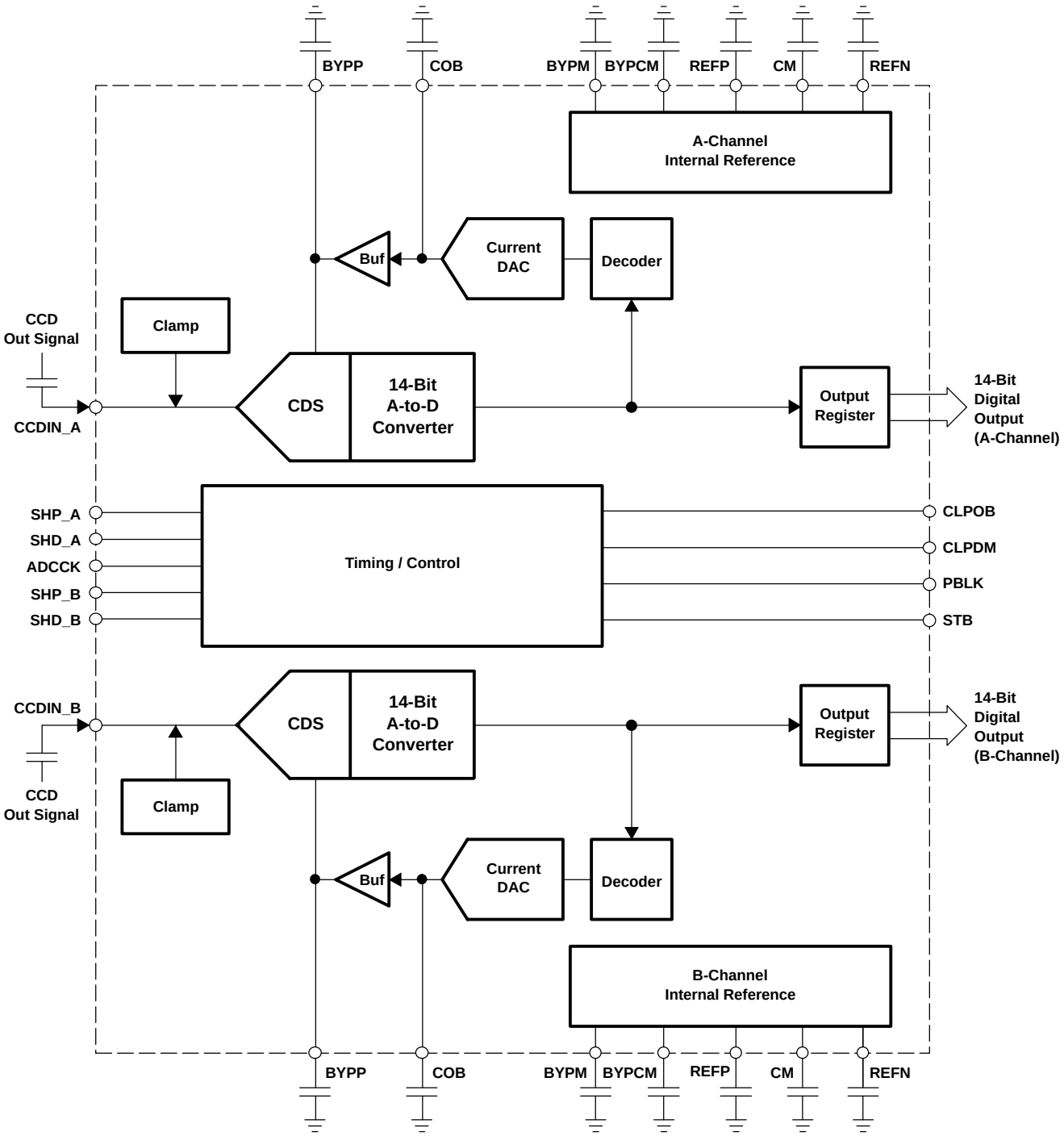
(1) P: Power Supply and Ground, DI: Digital Input, DO: Digital Output, AI: Analog Input, AO: Analog Output.

Terminal Functions (Continued)

TERMINAL NAME	TERMINAL NO.	TYPE(1)	DESCRIPTION
CLPOB	G1	DI	Optical black clamp pulse, (active low)
CM_A	D10	AO	A-channel ADC common reference, bypass-to-ground by a 0.1-μF capacitor
CM_B	G10	AO	B-channel ADC common reference, bypass-to-ground by a 0.1-μF capacitor
COB_A	B8	AO	A-channel OBC loop output voltage, connect a 0.1-μF capacitor between ground
COB_B	K8	AO	B-channel OBC loop output voltage, connect a 0.1-μF capacitor between ground
DGND	E2	P	Digital ground for digital outputs
	F2	P	
NC	A9, A10, C1, D2, D3, D4, D5, D6, D7, E4, E7, E8, F4, F7, F8, G3–G7, H8, J9, K9	–	Not connected, must be open
PBLK	G2	DI	A/D output preblanking. Low: all 0, High: normal output
REFN_A	D9	AO	A-channel ADC negative reference, bypass-to-ground a 0.1-μF capacitor
REFN_B	G9	AO	B-channel ADC negative reference, bypass-to-ground by a 0.1-μF capacitor
REFP_A	E10	AO	A-channel ADC positive reference, bypass-to-ground by a 0.1-μF capacitor
REFP_B	F10	AO	B-channel ADC positive reference, bypass-to-ground by a 0.1-μF capacitor
SHD_A	B1	DI	A-channel CCD data sampling pulse, (active low)
SHD_B	J1	DI	B-channel CCD data sampling pulse, (active low)
SHP_A	A1	DI	A-channel CCD ref sampling pulse, (active low)
SHP_B	J2	DI	B-channel CCD ref sampling pulse, (active low)
STB	E3	DI	Standby, low: normal operation, high: standby
VCC	A8, C3, D8, E1, F9, G8, H2 H7	P	Analog power supply
VDD	E1	P	Digital supply for digital outputs

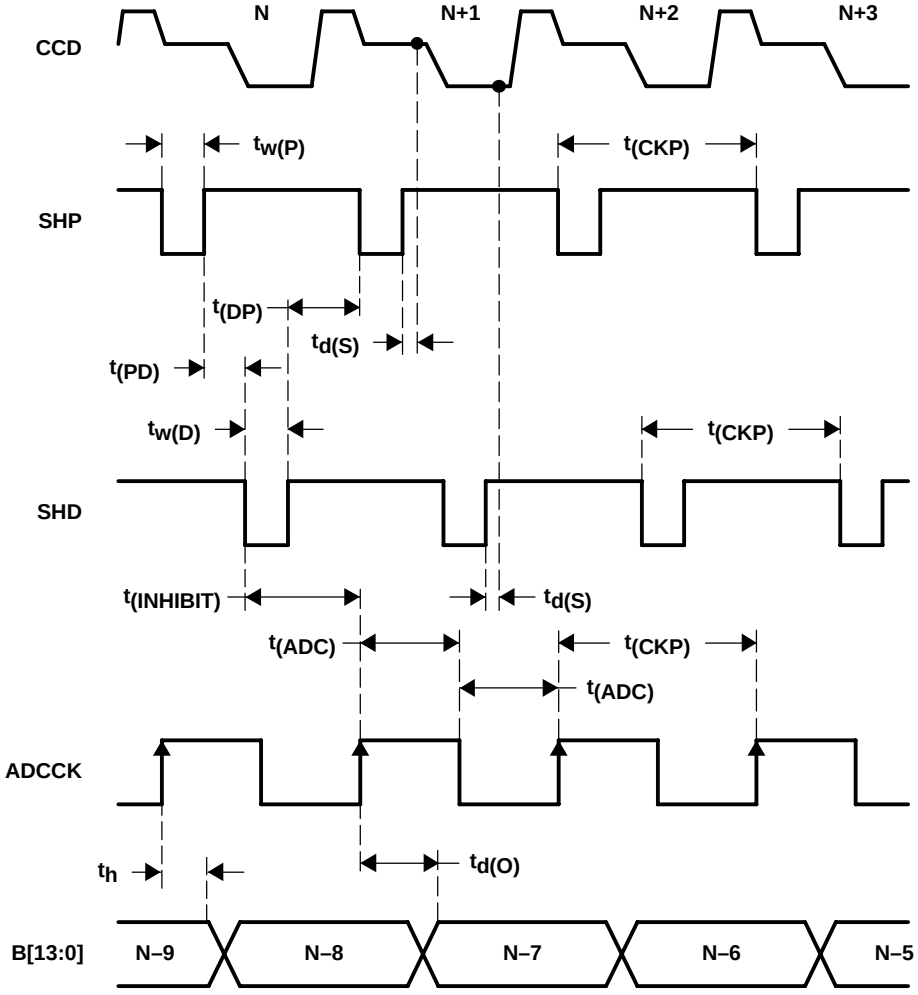
(1) P: Power Supply and Ground, DI: Digital Input, DO: Digital Output, AI: Analog Input, AO: Analog Output.

FUNCTIONAL BLOCK DIAGRAM



TIMING SPECIFICATION

Timing Specifications (for each channel)



PARAMETER		MIN	MAX	MAX	UNIT
$t_{(CKP)}$	Clock period	27			ns
$t_{(ADC)}$	ADCCK high or low level	10	13.8		ns
$t_{w(P)}$	SHP pulse width		6.9		ns
$t_{w(D)}$	SHD pulse width		6.9		ns
$t_{(PD)}$	SHP rising edge to SHD falling edge	4			ns
$t_{(DP)}$	SHD rising edge To SHP falling edge		6.9		ns
$t_{d(S)}$	Sampling delay		3		ns
$t_{(INHIBIT)}$	Inhibited clock period	10		20	ns
t_h	Output hold time	7			ns
$t_{d(O)}$	Output delay			27	ns
DL	Data latency		8		clocks

(1) $t_{(WP)} + t_{(PD)}$ should be nearly equal to $t_{(WD)} + t_{(DP)}$.

SYSTEM OVERVIEW

Introduction

The VSP2254 is a two channel high-resolution mixed-signal IC that contains key features associated with the processing of the CCD signal in a DVC. The VSP2254 integrates two channels of independent CCD processing path. Figure 1 shows a simplified block diagram of one channel of the VSP2254. The device includes a correlated double sampler (CDS), a 14-bit analog to digital converter (ADC), a black-level clamp loop, input clamp, timing generator, and voltage reference. An off-chip emitter follower buffer or preamp is needed between the CCD output and the VSP2254 CCDIN input. Both channels are driven common SHP/SHD, ADCCK, CLPOB, CLPDM, and STB.

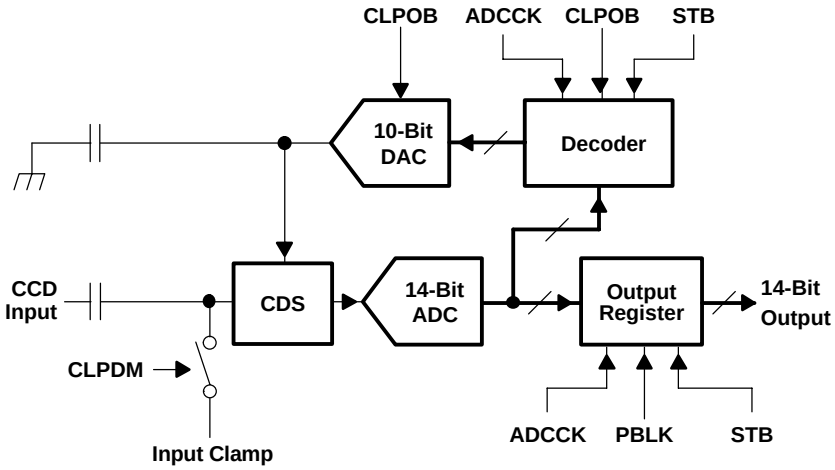


Figure 1. Simplified Block Diagram of VSP2254 (One Channel)

Correlated Double Sampler (CDS)

The output signal of a CCD image sensor is sampled twice during one pixel period: once at the reference interval and again at the data interval. Subtracting these two samples extracts the video information of the pixel and removes any noise which is common—or correlated—to both the intervals. Thus, a CDS is important to reduce the reset noise and the low-frequency noises that are present on the CCD output signal. Figure 2 shows the block diagram of the CDS.

The CDS is driven through an off-chip coupling capacitor $C_{IN.}$ (A 0.1-µF capacitor is recommended for C_{IN}.) AC-coupling is highly recommended, because the dc level of the CCD output signal is usually too high (several volts) for the CDS to work properly. The appropriate common-mode voltage for the CDS is around 0.5 V–1.5 V. The reference level sampling is performed while SHP is active and the voltage level is held on the sampling capacitor C_1 at the trailing edge of SHP. The data level sampling is performed while SHD is active and the voltage level is held on the sampling capacitor C_2 at the trailing edge of SHD. Then the subtraction of the two levels is performed by the switched-capacitor amplifier. The off-chip emitter follower buffer must be able to drive more than 10 pF, because the 10-pF sampling capacitor is seen at the input pin. (Usually, additional stray capacitance of a few pico farads is present.) The analog input signal range of the VSP2254 is about 1 Vp-p.

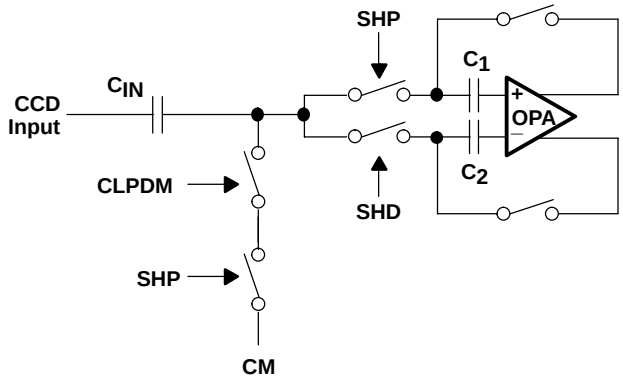


Figure 2. Block Diagram of CDS and Input Clamp

Input Clamp

The buffered CCD output is capacitively coupled to the VSP2254. The purpose of the input clamp is to restore the dc component of the input signal, which was lost with the ac-coupling and establish the desired dc bias point for the CDS. Figure 2 shows the block diagram of the input clamp. The input level is clamped to the internal reference voltage CM (1.5 V) during the dummy pixel interval. More specifically, the clamping function becomes active when both CLPDM and SHP are active.

14-Bit A/D Converter

The ADC utilizes a fully differential pipelined architecture of 1.5 bit per stage, which is well-suited for low-power, low-voltage and high-speed applications. The ADC assures 14-bit resolution for the entire full scale. The 1.5 bit per stage structure of the ADC is advantageous to realize a better linearity for a smaller signal level, because large linearity errors tend to occur at specific points in the full scale and the linearity gets better for a level of signal below that specific point.

Black Level Clamp Loop and 10-Bit DAC

To extract the video information correctly, the CCD signal must be referenced to a well-established black level. The VSP2254 has an auto-zero loop (calibration loop) to establish the black level using the CCD's optical black (OB) pixels. Figure 3 shows the block diagram of the black level clamp loop. The input signal level from the OB pixels is identified as the real black level and the loop is closed during this period (actually during the period while CLPOB = ACTIVE). While the auto-zero loop is closed, the difference between the ADC output code is evaluated and applied to the decoder, which then controls the 10-bit current DAC. The current DAC can charge or discharge the external capacitor at COB, dependent on the sign of the code difference. The loop adjusts the voltage at COB, which sets the offset of the CDS so as to make the code difference zero. Thus, the ADC output code converges to black level during CLPOB = ACTIVE and the black level derived from the OB pixels after the loop has converged. CLPOB performs OB clamp of both channels simultaneously.

A 0.1-μF bypass capacitor is recommended for COB and with this capacitor, the loop's time constant is 40.7 μs (typ) for the ADC output code from 0 LSB to 1543 LSB (the convergence curve becomes exponential). For the output code above 1543 LSB, the current DAC injects constant (maximum) current into the capacitor and the convergence curve becomes linear. The slew rate for that is 1530 V/s (typ). The loop not only eliminates the CCD's own black level offset, but also eliminates the offset of the VSP2254's CDS and ADC themselves.

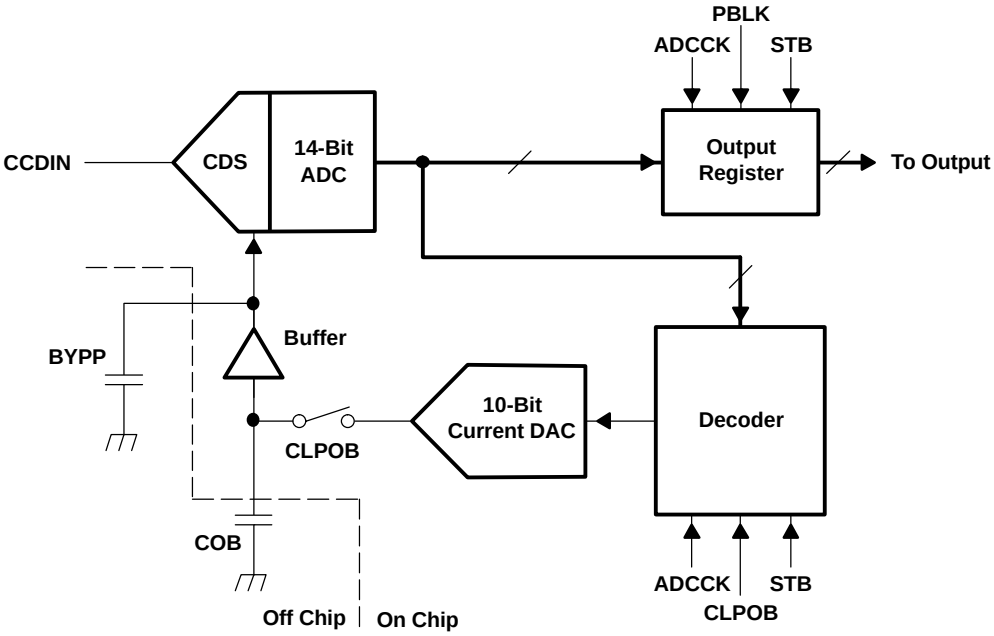


Figure 3. Block Diagram of Digital PGA and Black Level Clamp Loop

Preblanking and Data Latency

The VSP2254 has an input blanking (or preblanking) function. When PBLK = low, digital outputs all become zero at the ninth rising edge of ADCCK, counting from when PBLK becomes low to accommodate the clock latency of the VSP2254.

Data latency of the VSP2254 is seven clock cycles. The digital output data comes out at the rising edge of ADCCK with a delay of seven clock cycles.

Some CCDs have large transient output signals during blanking intervals. If the input voltage is higher than the supply rail or lower than the ground rail by 0.3 V, then protection diodes are turned on preventing the input voltage from going further. Such a high-swing signal may cause damage to the VSP2254 and should be avoided.

Standby Mode

For the purpose of power saving, the VSP2254 can be put into the standby mode (power-down mode) by forcing the STB input to a high level when the device is not in use. In this mode, all the function blocks are disabled and the digital outputs all go to zero. The consumption current drops to 5 mA. As all the bypass capacitors discharge during this mode, a substantial time (usually of the order of 200 ms–300 ms) is required to restore from the standby mode. STB is effective for both channels.

Timings

The CDS and the ADC are operated by SHP, SHD, and their derivative timing clocks generated by the on-chip timing generator. The output register and decoder are operated by ADCCK. The digital output data is synchronized with ADCCK. The timing relationship between the CCD signal, SHP, SHD, ADCCK, and the output data is shown on the VSP2254 timing specification. CLPOB is used to activate the black level clamp loop during the OB pixel interval and CLPDM is used to activate the input clamping during the dummy pixel interval. In the standby mode, ADCCK, SHP, SHD, CLPOB, and CLPDM are internally masked and pulled high.

Voltage Reference

All the reference voltages and bias currents used on the device are created from an internal band gap circuitry. The VSP2254 has symmetrical independent voltage reference for each channel.

Both channels of the CDS and the ADC use three main reference voltages, REFP (1.75 V), REFN (1.25 V), and CM (1.5 V) of the individual reference. REFP and REFN are buffered on-chip. CM is derived as the mid-voltage of the resistor chain connecting REFP and REFN internally. The ADC's full scale range is determined by twice the difference voltage between REFP and REFN.

REFP, REFN, and CM should be heavily decoupled with appropriate capacitors.

Power Supply, Grounding, and Device Decoupling Recommendations

The VSP2254 incorporates a high-precision, high-speed AD converter and analog circuitry, which are vulnerable to any extraneous noise from the rails or elsewhere.

The driver stage of the digital outputs (B[13:0]) is supplied through a dedicated supply pin (VDD) and should be separated from the other supply pins completely or at least with a ferrite bead. This ensures the most consistent results, since digital power lines often carry high levels of wide-band noise that would otherwise be coupled into the device and degrade the achievable performance. It is ecommended that analog and digital ground pins of the VSP2254 be separated.

Proper grounding, short lead length, and the use of ground planes are also important for high-frequency designs. Multilayer PC boards are recommended for the best performance, since they offer distinct advantages like minimizing ground impedance, separation of signal layers by ground layers, etc.

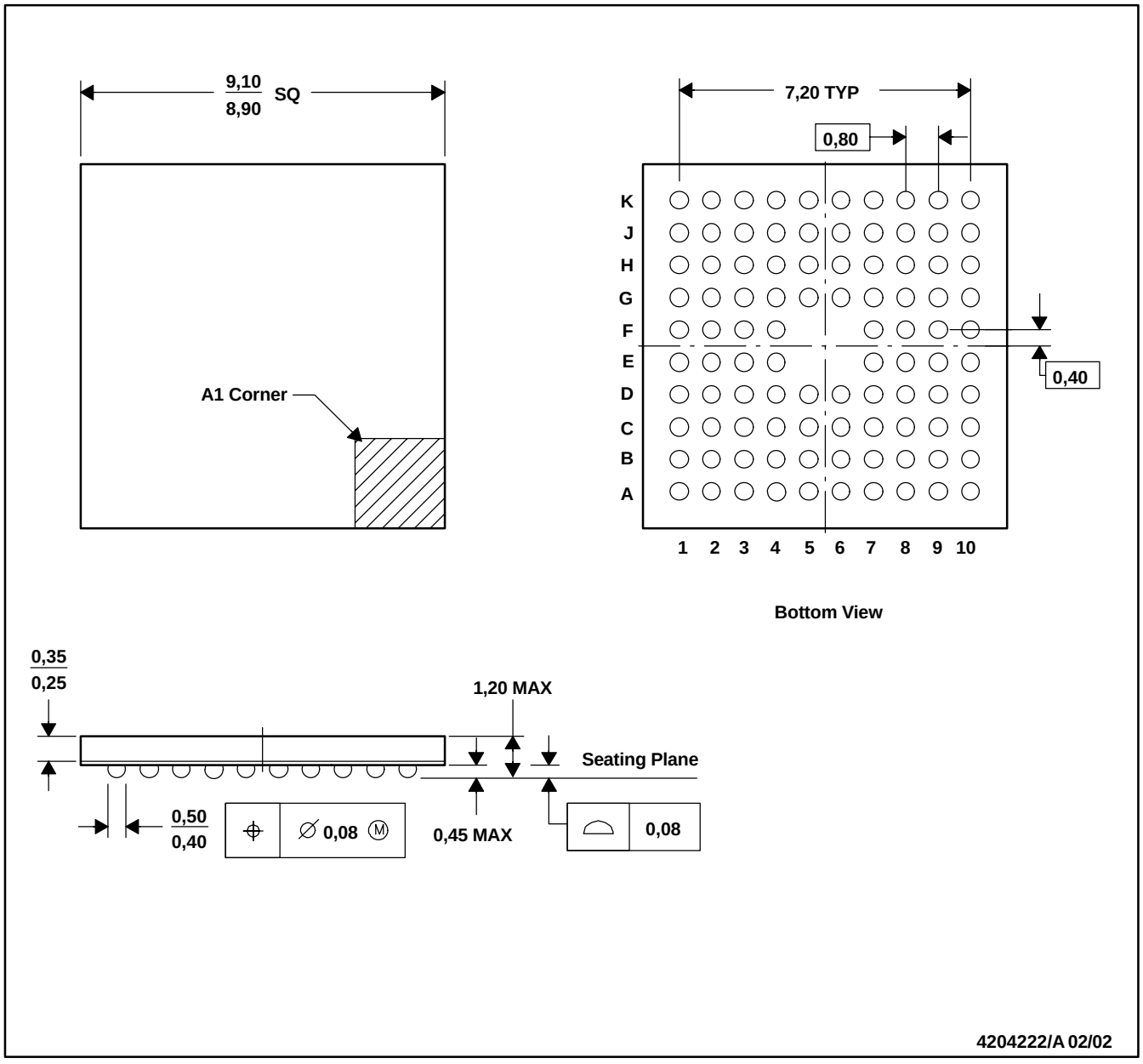
It is also recommended to keep the capacitive loading on the output data lines as low as possible (typically less than 15 pF). Larger capacitive loads demand higher charging current surges, which can feed back into the analog portion of the VSP2254 and affect the performance. If possible, external buffers or latches should be used, which provide the added benefit of isolating the VSP2254 from any digital noise activities on the data lines. In addition, resistors in series with each data line may help minimizing the surge current. Values in the range of 100 Ω to 200 Ω limits the instantaneous current the output stage has to provide for recharging the parasitic capacitance as the output levels change from low-to-high or high-to-low.

Because of the high-operation speed, the converter also generates high-frequency current transients and noises that are fed back into the supply and reference lines. This requires the supply and reference pins to be sufficiently bypassed. In most cases, 0.1-μF ceramic chip capacitors are adequate to decouple the reference pins. Supply pins should be decoupled to the ground plane with a parallel combination of tantalum (1 μF–22 μF) and ceramic (0.1 μF) capacitors. The effectiveness of the decoupling largely depends on the proximity to the individual pin. VDD should be decoupled to the proximity of DGND.

Attention must be paid to the bypassing of COB, BYPP, and BYPM, since these capacitor values determine important analog performances of the device.

MECHANICAL DATA

GSJ (S-PBGA-N96) **PLASTIC BALL GRID ARRAY**



NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. MicroStar Junior™ package configuration.
D. Fall within JEDEC MO-225.

MicroStar Junior is a trademark of Texas Instruments.

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