



**THE DATASHEET OF
PTRF1216IRGPR**

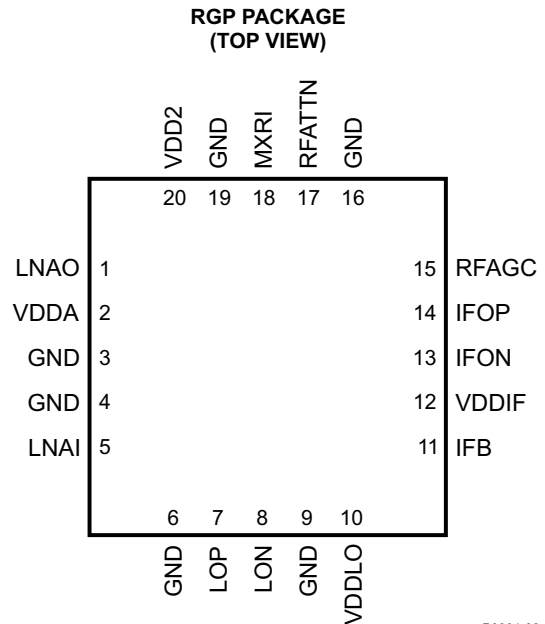


3.5-GHz, HIGH DYNAMIC RANGE, LOW-NOISE DOWN-CONVERTER

FEATURES

- Performs First Down-Conversion in 3.5-GHz Radios (3300–3800 MHz)
- Integrated LNA/Mixer/IF Amp/LO Buffer
- Provision for External Image Reject/Band-Pass Filter
- Low Noise-Figure/High Linearity
- Digital 10-dB Attenuator for High-Level Signals
- Frequency Range: 3.3–3.8 GHz
- 28 dB of Gain with 20 dB of Gain Control (10-dB Fixed)
- 2.5-dB Noise Figure, Typical
- LO Drive Level = 0 dBm, Typical

DEVICE INFORMATION



P0031-02

DESCRIPTION

The TRF1216 is the first of two integrated circuits used in the receiver section of Texas Instruments' 3.5-GHz radio chipset. The TRF1216 down-converts the 3.5-GHz input frequency to an intermediate frequency in the range of 400 MHz to 500 MHz. The device provides a differential output that passes through a SAW filter before connecting to a second down converter. For the best performance, Texas Instruments TRF1212 should be used to perform both the second down conversion and also provide the local oscillator for the TRF1216.

The TRF1216 includes a LNA with switchable attenuation, a balanced mixer, a variable gain IF amplifier and a differential LO Buffer for improved performance. In order to provide exceptional image rejection and extra jammer immunity, the TRF1216 offers a signal path to an off-chip filter. Specifications are provided assuming an in-band 2-dB insertion loss filter. To maximize input dynamic range, a 10-dB switchable attenuator is provided in the RF path as well as 10 dB of analog IF gain control. After the image reject filter, an on-chip Balun converts the signal from single ended to differential in order to provide better noise immunity at the mixer.



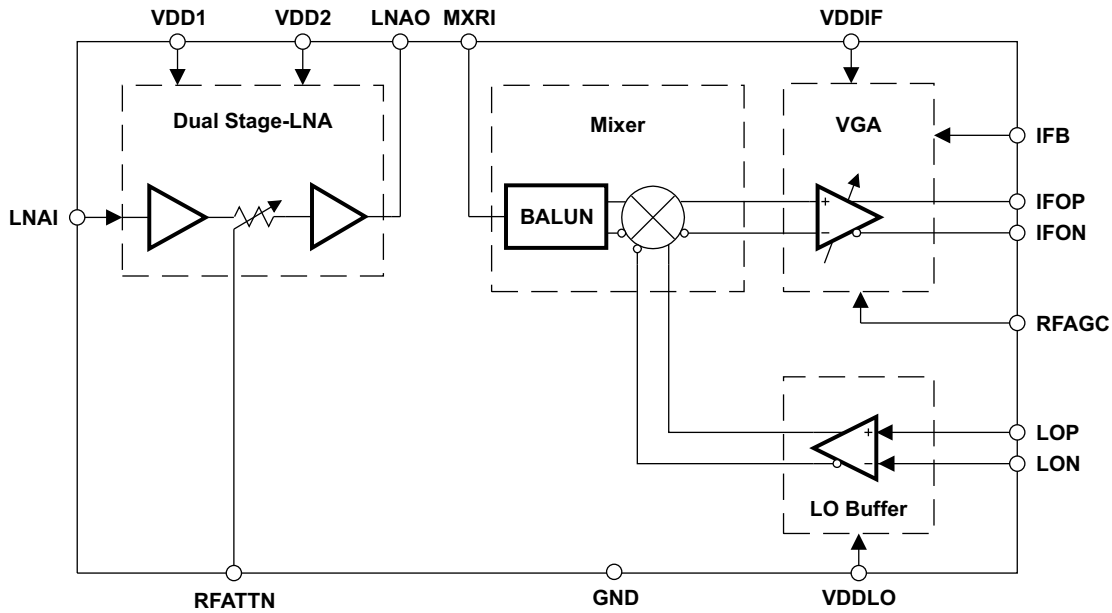
Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

BLOCK DIAGRAM

The detailed block diagram and the pin-out of the ASIC are shown in Figure 1 and Table 1.



B0084-01

Figure 1. Detailed Block Diagram of TRF1216

TERMINAL FUNCTIONS

TERMINAL NO.	NAME	I/O	TYPE	DESCRIPTION
1	LNAO	O	Analog	LNA Output, 50 Ω, ac-coupled
2	VDD1	I	Power	LNA1 DC Bias (+5 V nominal)
3, 4, 6, 9, 16, 19	GND	–	–	Ground
5	LNAI	I	Analog	RF input – Needs dc block and input matching for optimum noise figure
7	LOP	I	Analog	LO input positive, ac coupled
8	LON	I	Analog	LO input negative, ac coupled
10	VDDLO	I	Power	LO DC Bias (+5 V nominal)
11	IFB	–	–	Not connected for normal operation. IF Bias Adjustment. Do not ground this pin or connect to any other pin.
12	VDDIF	I	Power	IF Bias Network dc Bias (+5 V nominal)
13	IFON	O	Analog	IF output and bias (see the application schematic for connections).
14	IFOP	O	Analog	IF output and bias (see the application schematic for connections).
15	RFAGC	I	Analog	Input voltage for analog gain control $V_{RFAGC} = 0\text{ V to }1.5\text{ V}$ Max gain at $V_{RFAGC} = 0\text{ V}$ Min gain at $V_{RFAGC} = 1.5\text{ V}$
17	RFATTN	I	Digital	TTL control for switched attenuator TTL low – Attenuator switched in TTL high – Attenuator switched out
18	MXRI	I	Analog	Mixer Input 50 Ω
20	VDD2	–	Power	LNA2 dc bias (+5 V nominal)
Back	GND	–	–	Back of package has metal base that must be grounded for thermal and RF performance.

ABSOLUTE MAXIMUM RATINGS

		VALUES	UNIT
V_{DD}	DC supply voltage, VDD	0 to 5.5	V
P_{IN}	RF input power	10	dBm
T_J	Junction temperature	200	°C
P_D	Power dissipation	1100	mW
V_D	Digital input voltage	–0.3 to 5.5	V
V_A	Analog input voltage	–0.3 to 5	V
θ_{JC}	Thermal resistance junction-to-case ⁽¹⁾	9.1	°C/W
T_{stg}	Storage temperature	–40 to 105	°C
T_{op}	Operating temperature	–40 to 85	°C
	Lead temperature (40 Sec Max)	260	°C

(1) Thermal resistance is junction to ambient assuming thermal pad with nine thermal vias under package metal base. See the recommended PCB layout.

ELECTRICAL CHARACTERISTICS

The characteristics listed in the following tables are at $V_{CC} = 5\text{ V}$, $T_A = 25^\circ\text{C}$ unless otherwise specified.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
DC CHARACTERISTICS						
V_{DD}	Supply voltage			5	5.5	V
I_{DD}	Total supply current			175	200	mA
I_{LNA1}	LNA1 supply current	Pin 2 (VDD1)		35		mA
I_{LNA2}	LNA2 supply current	Pin 20 (VDD2)		35		mA
I_{IF}	IF AMP supply current	Pin 12 (VDDIF) plus IF drain bias on pins 13 and 14 (IFOP, IFON)		55		mA
I_{LO}	LO supply current	Pin 10 (VDDL0)		50		mA
V_{AGC}	Gain control voltage		0		2	V
I_{AGC}	Gain control current		0		100	μA
V_{IH}	Input high voltage		2.5		5	V
V_{IL}	Input low voltage		0		0.8	V
I_{IH}	Input high current				300	μA
I_{IL}	Input low current				–50	μA

DOWNCONVERTER CHARACTERISTICSUnless otherwise stated $V_{DD} = 5\text{ V}$, $FRF = 3500\text{ MHz}$, $T_A = 25^\circ\text{C}$

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
F_{RF}	RF input frequency		3300		3800	MHz
F_{LO}	LO input frequency		2800		3400	MHz
F_{IF}	IF output frequency		400	480	500	MHz
G	Maximum gain	$V_{AGC} = 0\text{ V}$, RFATTN disabled, Measured into 100- Ω differential load	27	30	33	dB
Δ_{AGC}	Analog gain control range	V_{AGC} from 0 to 1.5 V, Any RFATTN setting. Measured into 100- Ω differential load	7	10		dB
Δ_{ATTN}	Switched attenuator range	RFATTN from high-to-low, any VAGC setting. Measured into 100- Ω differential load	8.5	10	11.5	dB
G_{HG}	Gain flatness full band	Any 200-MHz band		1	2	dB
G_{NB}	Gain flatness / 6 MHz	Any 6-MHz band			0.4	dB
NF	Noise figure ⁽¹⁾	$V_{AGC} = 0\text{ V}$, RFATTN disabled		2.5		dB
		$V_{AGC} = 0\text{ V}$, RFATTN enabled		4.8		
		$V_{AGC} = 1.5\text{ V}$, RFATTN disabled		3.2		
		$V_{AGC} = 1.5\text{ V}$, RFATTN enabled		6.8		
IP-1dB	Input power at 1-dB compression	$V_{AGC} = 0\text{ V}$, RFATTN disabled		-17		dBm
		$V_{AGC} = 0\text{ V}$, RFATTN enabled		-6		
		$V_{AGC} = 1.5\text{ V}$, RFATTN disabled		-10		
		$V_{AGC} = 1.5\text{ V}$, RFATTN enabled		-4		
IIP3	Input 3rd order intercept point	$V_{AGC} = 0\text{ V}$, RFATTN disabled		-7		dBm
		$V_{AGC} = 0\text{ V}$, RFATTN enabled		-1		
		$V_{AGC} = 1.5\text{ V}$, RFATTN disabled		-5		
		$V_{AGC} = 1.5\text{ V}$, RFATTN enabled		5		
P_{LO}	LO input power	Referenced to 100- Ω differential		0		dBm
	LO to MXRI leakage	LO input = 3 dBm, $V_{AGC} = 0\text{ V}$	-35	-45		dB
	LO to IF leakage	LO input = 3 dBm, $V_{AGC} = 0\text{ V}$	-40	-50		dB
	LNAO to RXI isolation	$F_{RF} = 3300\text{ to }3800\text{ MHz}$, RFATTN = TTL High	40			dB

(1) Assured by lab characterization/design and not subject to production test.

TYPICAL CHARACTERISTICS

Measurements resulting in the following graphs were taken on the evaluation board of the ASIC (see Figure 9).

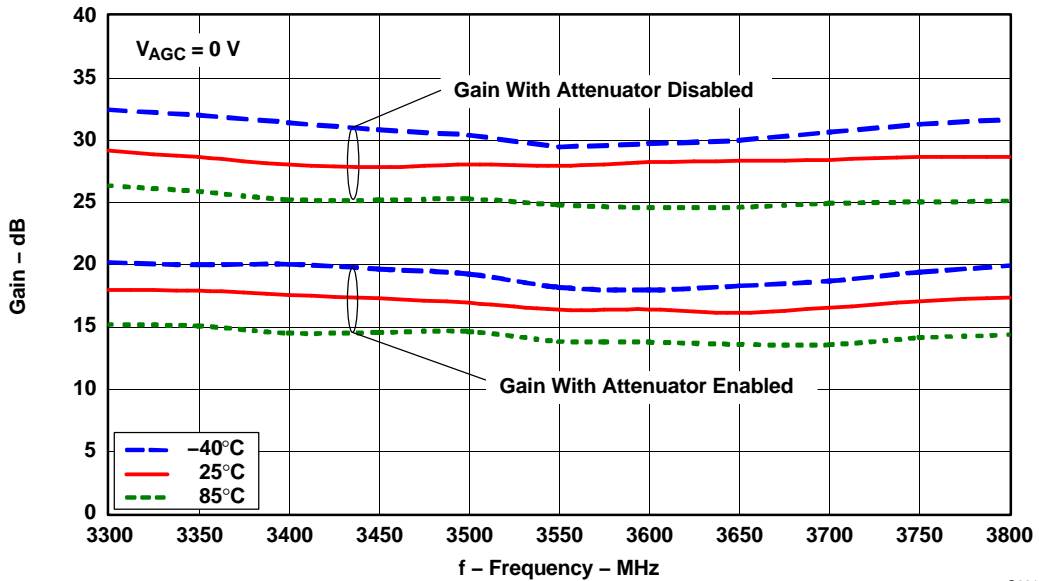


Figure 2. Gain vs Frequency for $V_{AGC} = 0\text{ V}$

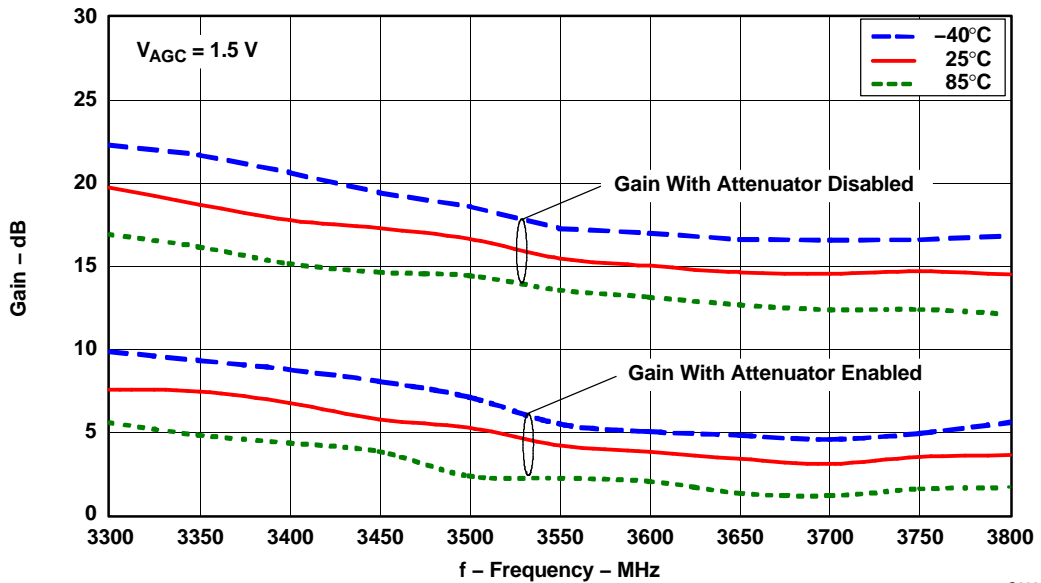
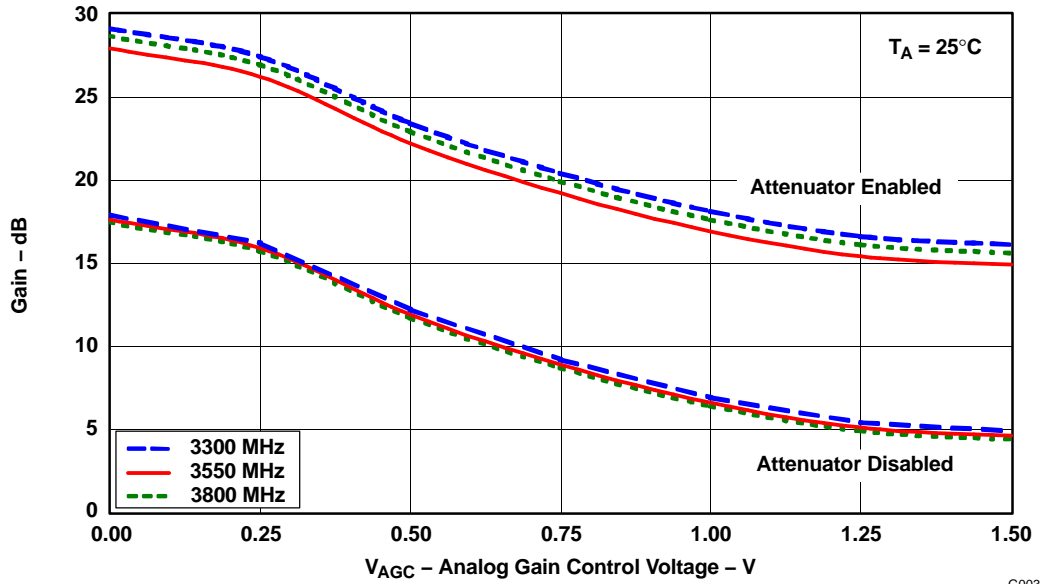


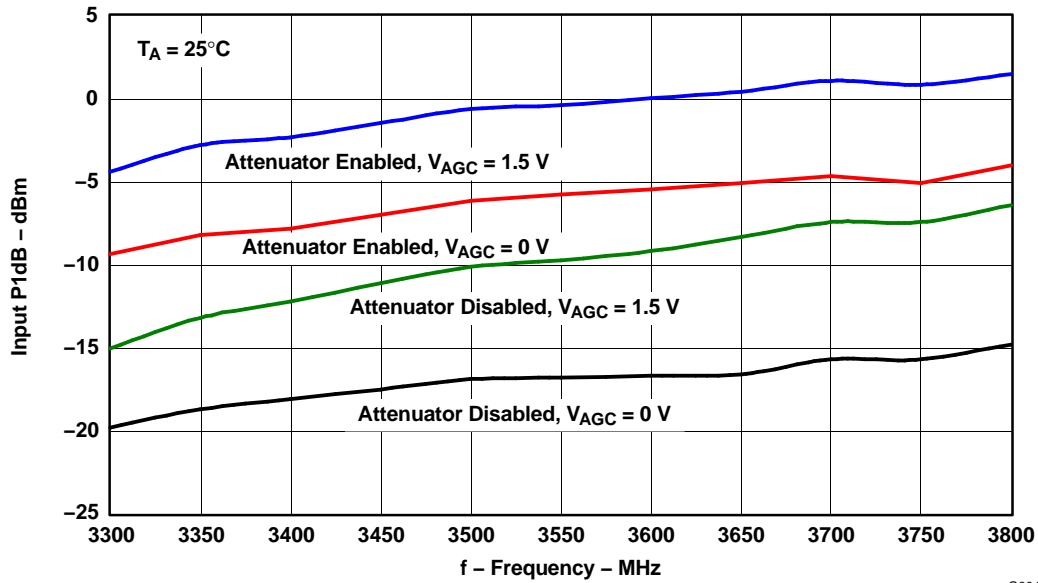
Figure 3. Gain vs Frequency for $V_{AGC} = 1.5\text{ V}$

TYPICAL CHARACTERISTICS (continued)



G003

Figure 4. Gain vs VAGC for Different Frequencies, ($T_A = 25^\circ\text{C}$)



G004

Figure 5. Input P1dB vs Frequency, ($T_A = 25^\circ\text{C}$)

TYPICAL CHARACTERISTICS (continued)

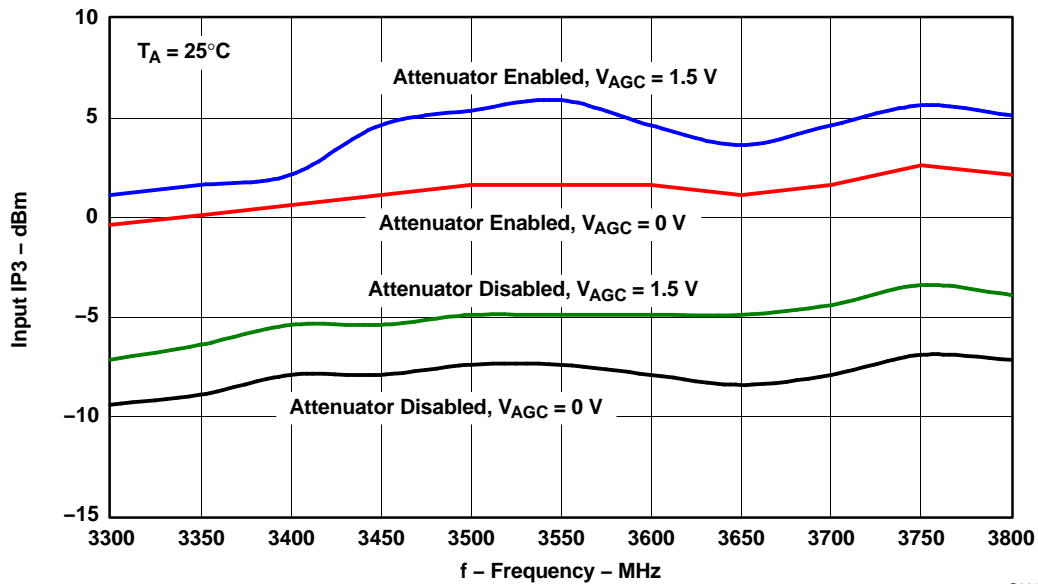


Figure 6. Input IP3 vs Frequency, ($T_A = 25^\circ\text{C}$)

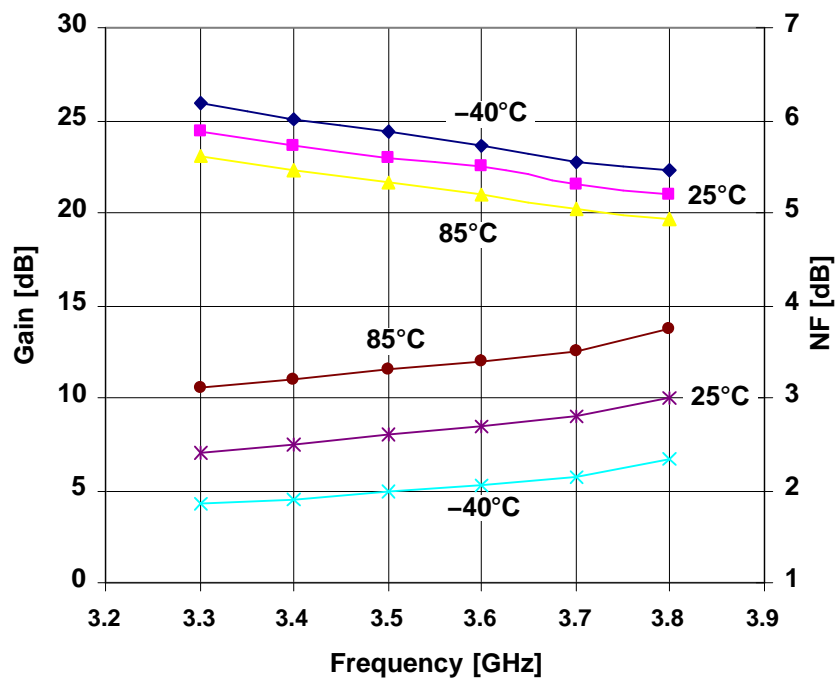


Figure 7. LNA Noise Figure vs Frequency With $V_{AGC} = 0\text{ V}$

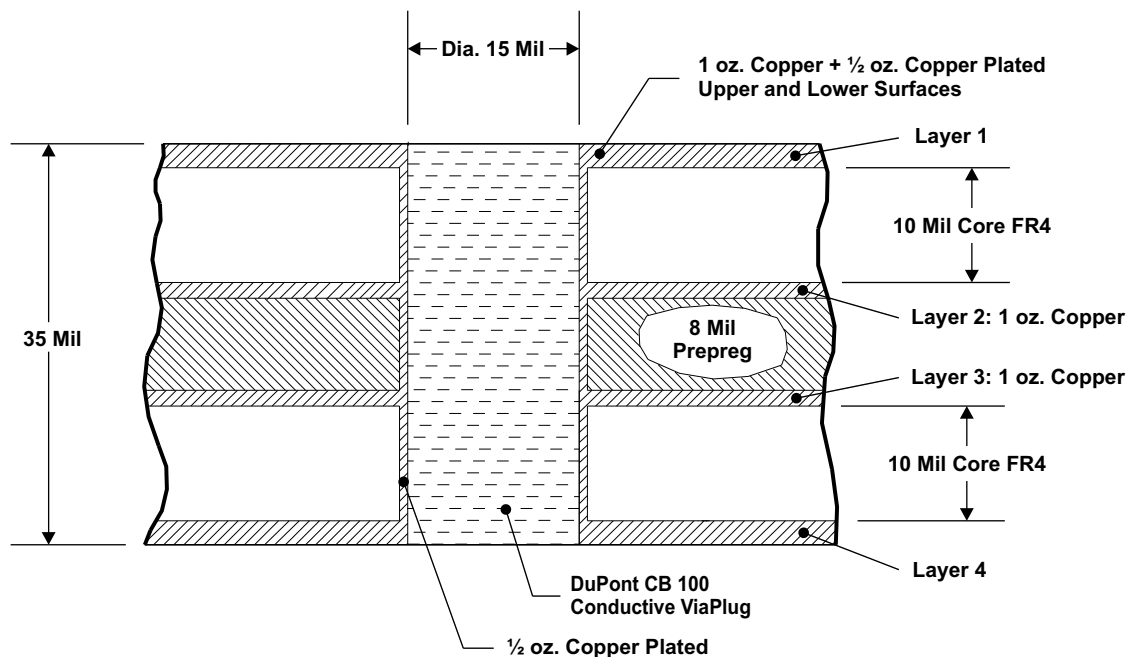
APPLICATION INFORMATION

A typical application schematic is shown in [Figure 9](#).

The PCB material recommendations are shown in [Table 1](#) and [Figure 8](#).

Table 1. PCB Recommendations

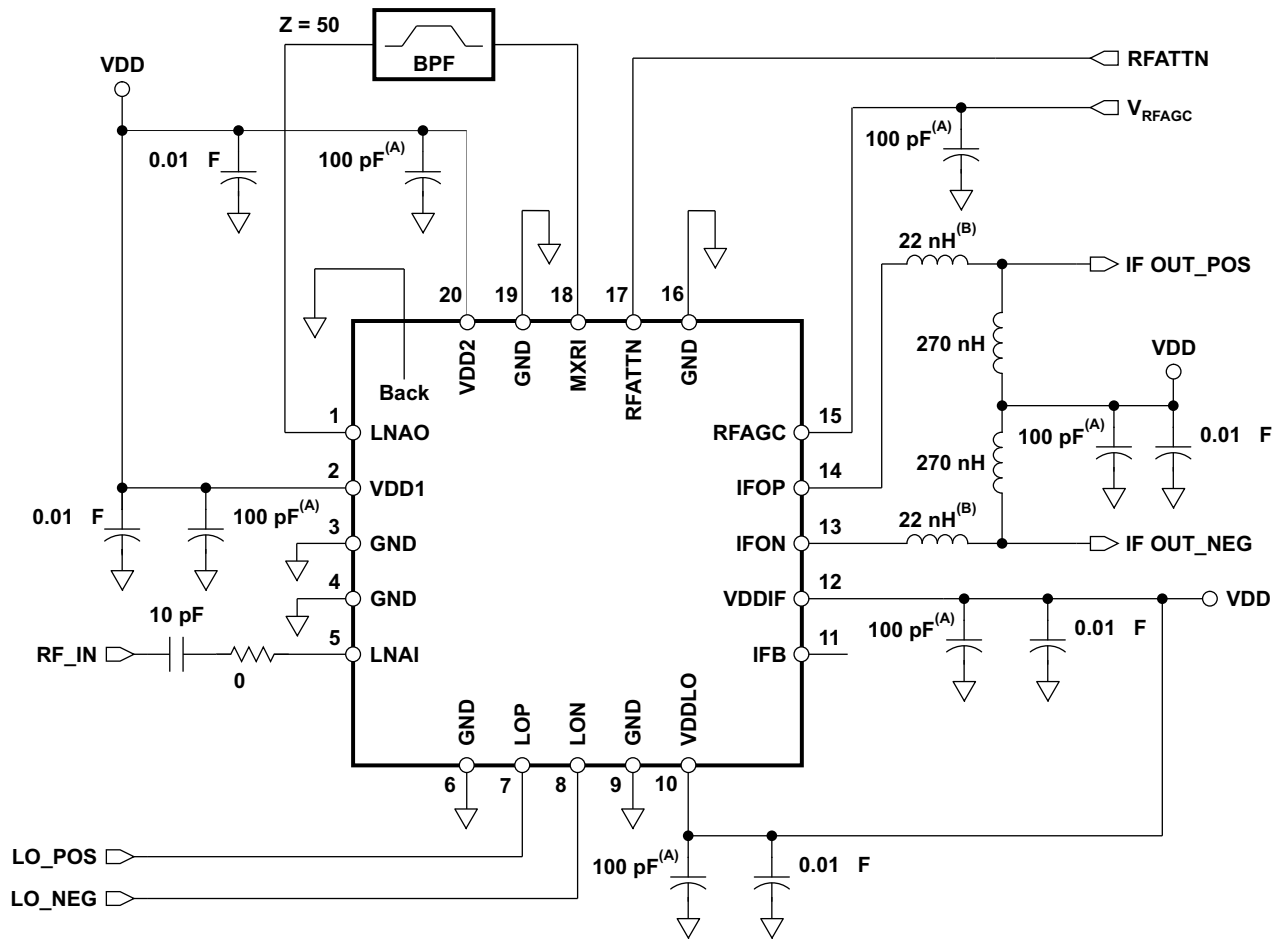
Board Material	FR4
Board Material Core Thickness	10 mil
Copper Thickness (starting)	1 oz
Prepreg Thickness	8 mil
Recommended Number of Layers	4
Via Plating Thickness	1/2 oz
Final Plate	White immersion tin
Final Board Thickness	33–37 mil



M0020-02

NOTE: Top and bottom surface finish: copper flash with 50–70 μm white tin immersion.

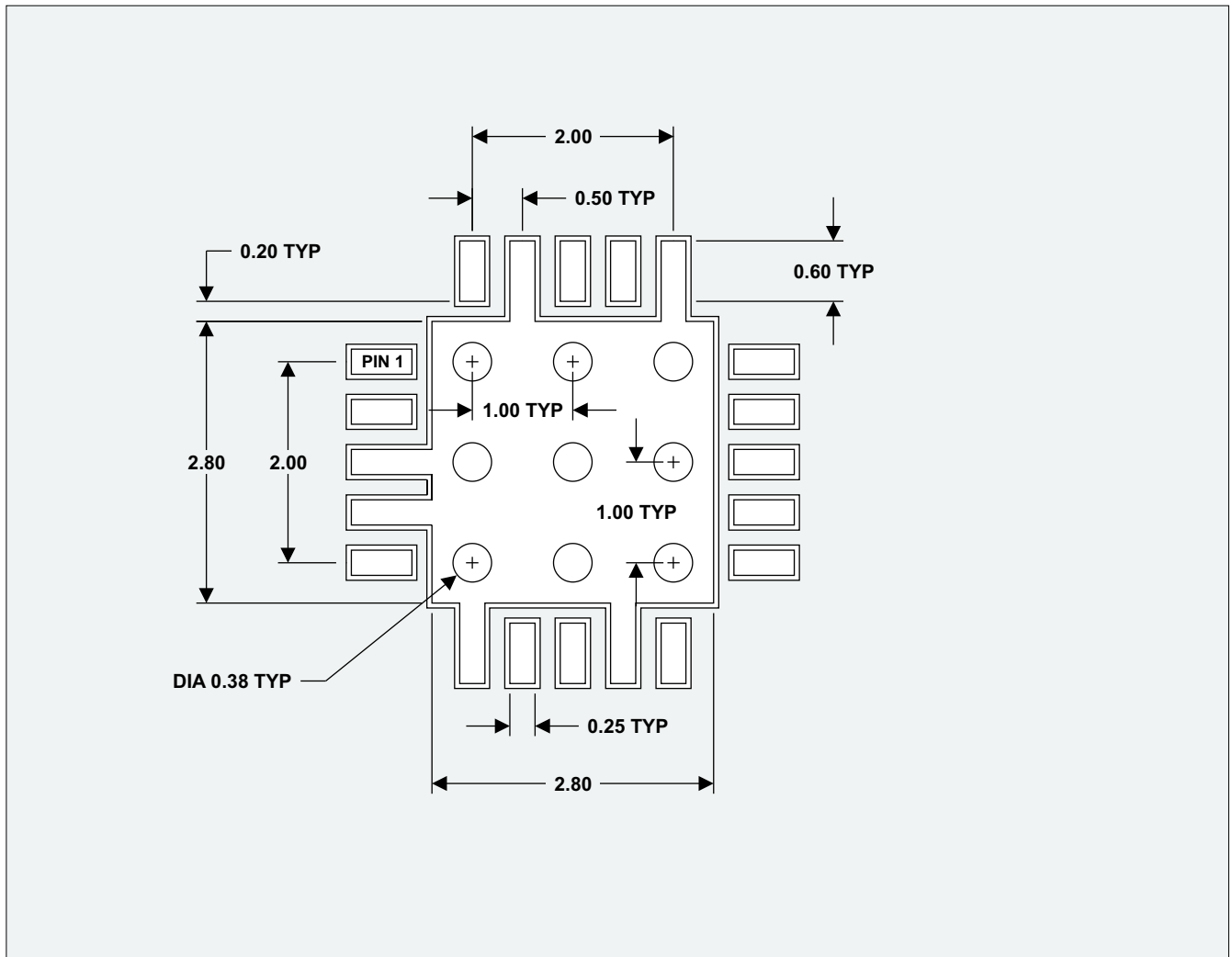
Figure 8. PCB Construction and Via Cross Section



S0122-01

- A. Place 100-pF capacitors close to package pins.
- B. Place 22-nH inductors close to package pins.

Figure 9. Recommended Application Schematic



 Solder Mask. No Solder Mask Under Chip, On Lead Pads or On Ground Connections.

Notes: 9 Via Holes, Each 0.38 mm.
Dimensions in mm

M0022-02

Figure 10. Recommended Pad Layout

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TRF1216IRGPR	ACTIVE	QFN	RGP	20	3000	Green (RoHS & no Sb/Br)	CU SN	Level-3-260C-168 HR	-40 to 85	TRF 1216	Samples
TRF1216IRGPRG3	ACTIVE	QFN	RGP	20	3000	Green (RoHS & no Sb/Br)	CU SN	Level-3-260C-168 HR	-40 to 85	TRF 1216	Samples
TRF1216IRGPT	ACTIVE	QFN	RGP	20		TBD	Call TI	Call TI	-40 to 85	TRF 1216	Samples
TRF1216IRGPTG3	ACTIVE	QFN	RGP	20		TBD	Call TI	Call TI	-40 to 85	TRF 1216	Samples

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBsolete: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and

continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION



QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TRF1216IRGPR	QFN	RGP	20	3000	330.0	12.4	4.3	4.3	1.5	8.0	12.0	Q2
TRF1216IRGPT	QFN	RGP	20	250	180.0	12.4	4.3	4.3	1.5	8.0	12.0	Q2

TAPE AND REEL BOX DIMENSIONS

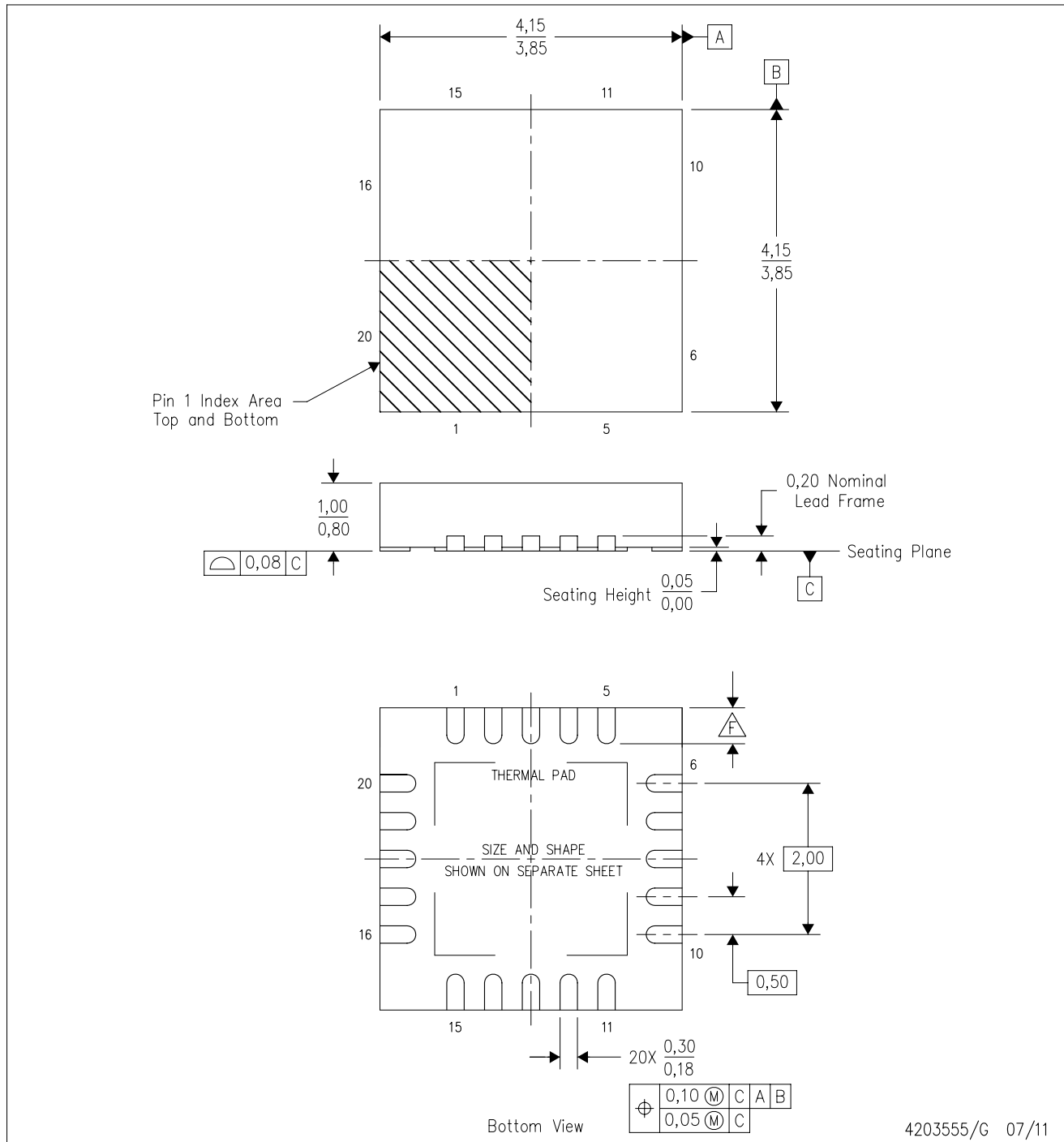


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TRF1216IRGPR	QFN	RGP	20	3000	338.1	338.1	20.6
TRF1216IRGPT	QFN	RGP	20	250	210.0	185.0	35.0

RGP (S-PVQFN-N20)

PLASTIC QUAD FLATPACK NO-LEAD



- NOTES:
- All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
 - This drawing is subject to change without notice.
 - QFN (Quad Flatpack No-Lead) package configuration.
 - The package thermal pad must be soldered to the board for thermal and mechanical performance.
 - See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.
- Check thermal pad mechanical drawing in the product datasheet for nominal lead length dimensions.

IMPORTANT NOTICE

Texas Instruments Incorporated and its subsidiaries (TI) reserve the right to make corrections, enhancements, improvements and other changes to its semiconductor products and services per JESD46, latest issue, and to discontinue any product or service per JESD48, latest issue. Buyers should obtain the latest relevant information before placing orders and should verify that such information is current and complete. All semiconductor products (also referred to herein as "components") are sold subject to TI's terms and conditions of sale supplied at the time of order acknowledgment.

TI warrants performance of its components to the specifications applicable at the time of sale, in accordance with the warranty in TI's terms and conditions of sale of semiconductor products. Testing and other quality control techniques are used to the extent TI deems necessary to support this warranty. Except where mandated by applicable law, testing of all parameters of each component is not necessarily performed.

TI assumes no liability for applications assistance or the design of Buyers' products. Buyers are responsible for their products and applications using TI components. To minimize the risks associated with Buyers' products and applications, Buyers should provide adequate design and operating safeguards.

TI does not warrant or represent that any license, either express or implied, is granted under any patent right, copyright, mask work right, or other intellectual property right relating to any combination, machine, or process in which TI components or services are used. Information published by TI regarding third-party products or services does not constitute a license to use such products or services or a warranty or endorsement thereof. Use of such information may require a license from a third party under the patents or other intellectual property of the third party, or a license from TI under the patents or other intellectual property of TI.

Reproduction of significant portions of TI information in TI data books or data sheets is permissible only if reproduction is without alteration and is accompanied by all associated warranties, conditions, limitations, and notices. TI is not responsible or liable for such altered documentation. Information of third parties may be subject to additional restrictions.

Resale of TI components or services with statements different from or beyond the parameters stated by TI for that component or service voids all express and any implied warranties for the associated TI component or service and is an unfair and deceptive business practice. TI is not responsible or liable for any such statements.

Buyer acknowledges and agrees that it is solely responsible for compliance with all legal, regulatory and safety-related requirements concerning its products, and any use of TI components in its applications, notwithstanding any applications-related information or support that may be provided by TI. Buyer represents and agrees that it has all the necessary expertise to create and implement safeguards which anticipate dangerous consequences of failures, monitor failures and their consequences, lessen the likelihood of failures that might cause harm and take appropriate remedial actions. Buyer will fully indemnify TI and its representatives against any damages arising out of the use of any TI components in safety-critical applications.

In some cases, TI components may be promoted specifically to facilitate safety-related applications. With such components, TI's goal is to help enable customers to design and create their own end-product solutions that meet applicable functional safety standards and requirements. Nonetheless, such components are subject to these terms.

No TI components are authorized for use in FDA Class III (or similar life-critical medical equipment) unless authorized officers of the parties have executed a special agreement specifically governing such use.

Only those TI components which TI has specifically designated as military grade or "enhanced plastic" are designed and intended for use in military/aerospace applications or environments. Buyer acknowledges and agrees that any military or aerospace use of TI components which have **not** been so designated is solely at the Buyer's risk, and that Buyer is solely responsible for compliance with all legal and regulatory requirements in connection with such use.

TI has specifically designated certain components as meeting ISO/TS16949 requirements, mainly for automotive use. In any case of use of non-designated products, TI will not be responsible for any failure to meet ISO/TS16949.

Products

Audio	www.ti.com/audio
Amplifiers	amplifier.ti.com
Data Converters	dataconverter.ti.com
DLP® Products	www.dlp.com
DSP	dsp.ti.com
Clocks and Timers	www.ti.com/clocks
Interface	interface.ti.com
Logic	logic.ti.com
Power Mgmt	power.ti.com
Microcontrollers	microcontroller.ti.com
RFID	www.ti-rfid.com
OMAP Applications Processors	www.ti.com/omap
Wireless Connectivity	www.ti.com/wirelessconnectivity

Applications

Automotive and Transportation	www.ti.com/automotive
Communications and Telecom	www.ti.com/communications
Computers and Peripherals	www.ti.com/computers
Consumer Electronics	www.ti.com/consumer-apps
Energy and Lighting	www.ti.com/energy
Industrial	www.ti.com/industrial
Medical	www.ti.com/medical
Security	www.ti.com/security
Space, Avionics and Defense	www.ti.com/space-avionics-defense
Video and Imaging	www.ti.com/video

TI E2E Community

e2e.ti.com

Looking for pricing, stock, or lifecycle information?

Click below to explore more details on WIN SOURCE:

 [View PTRF1216IRGPR on WIN SOURCE](#)

 [Texas Instruments](#) Information

Optimize Your Supply Chain with WIN SOURCE Solutions

-  Global Sourcing Solution
-  Obsolete Management
-  Cost Control Management
-  Shortage Management
-  Alternative Solution
-  Excess Inventory Management