THE DATASHEET OF

TRAC020LHEURO

TOTALLY RE-CONFIGURABLE ANALOG CIRCUIT - TRAC®

TRAC020LH

Issue 2 - MARCH 1999

DEVICE DESCRIPTION

The TRAC020LH is a Micro-Power version of the existing TRAC products. It also offers significant improvements in bandwidth and function accuracy.

The TRAC020LH is the latest addition to the TRAC family of Field Programmable Analog Devices (FPAD) which offers an integrated path from signal processing problems to working silicon solutions - in minutes! The Totally Reconfigurable Analog Circuit is a highly flexible single chip solution to the signal processing problems found in many markets.

Introducing a Top-Down, Structured design discipline, TRAC enables rapid implementation, prototyping and product release. Rather than working at the component level, TRAC champions the Computational Approach, providing designers with benefits formerly associated with programmable digital devices. TRAC brings a truly integrated Signal Processing problem solving process and offers a path to Custom Silicon for high volume applications.

APPLICATIONS

Many analog signal processing applications including:-

- Analog Computation
- Analog Signal Processing (ASP)
- Classical & Modern Control Systems
- Audio Applications
- Sonar and Ultrasonic Systems
- Analog Correlation
- Echo Cancellation
- Log, Linear and Modern Filter Design
- Instrumentation
- Transducer Characteristic Correction
- Vector Analysis

FEATURES AND BENEFITS

- Faster design and verification of signal processing solutions
- Instant working silicon
- Flexibility to react to changing requirements
- Stay thinking about analog problems mathematically - minimal circuit design
- Just as versatile as FPGA - and just as easy
- Complete more projects on time
- High level of integration and design secrecy
- Integration with other CAE systems
- Transparent design migration to semi-custom and future devices
- Less than 8 bytes to program
- Full industrial temperature range
- Standby mode for improved battery life
- Devices easily cascaded for more complex designs
- Combines silicon, software and support

ORDERING INFORMATION

PART NUMBER	PACKAGE	PART MARK
TRAC020LHQ36	QSOP36	TRAC020LH

For more information on Fast Analog Solutions and all our products see www.fas.co.uk

TRAC020LH

ABSOLUTE MAXIMUM RATINGS

Voltage on any pin = 7.0V (relative to V_{SS})
Operating Temperature = -40 to 85°C
Storage Temperature = -55 to 125°C

GENERAL ELECTRICAL CHARACTERISTICS

Test Conditions: Temperature = 25 °C, V_{DD} = 3.0V±0.15V, V_{SS} = -2.0V±0.10V

PARAMETER	CONDITIONS	MIN	TYPICAL	MAX
General Characteristics				
Dynamic Range			80dB	
Noise Voltage	10Hz-100kHz		15nV/$\sqrt{Hz}$	
Total Harmonic Distortion	100mV peak-peak 1.0V peak-peak		0.02% 0.08%	
Intermodulation Distortion			< 0.1%	
Supply Rejection			60dB	
Cell to cell crosstalk			-60dB	
Input Range (all IO pins)			V_{DD}-2.0V, V_{SS}+1.0V	
Slew Rate			4V/µS	
Supply Current				
Operating Current I_{DD}	Cells to NIP function $\overline{PD}$=V_{DD}	2.5mA	5.0mA	6.0mA
Operating Current I_{SS}		-2.5mA	-5.0mA	-6.0mA
Shutdown Current I_{DD}	$\overline{PD}$=V_{SS}			10µA
Cell Output Capability				
Sink Current			150µA	
Source Current			150µA	

ELECTRICAL CHARACTERISTICS OF THE CELL

Test Conditions: Temperature = 25 °C, V_{DD} = 3.0V±0.15V, V_{SS} = - 2.0V±0.10V

FUNCTION	PARAMETER	CONDITIONS	MIN	TYPICAL	MAX
Non Inverting Pass	Gain	V_{in} = ±800mV	0.996	1.000	1.004
	Input Resistance			60MΩ	
	Offset	V_{in}=0mV	-1.2mV	0mV	1.2mV
	Input Current			100nA	260nA
	Bandwidth (small signal)	20mV peak-peak		12MHz	
	Bandwidth (large signal)	500mV peak-peak		3MHz	
Negate	Gain	V_{in} = ±800mV	-1.010	-1.000	-0.990
	Input Resistance		30kΩ	40kΩ	50kΩ
	Offset	V_{in}=0mV	-2.4mV	0mV	2.4mV
	Bandwidth(small signal)	20mV peak-peak		7MHz	
	Bandwidth(large signal)	500mV peak-peak		3MHz	
Add	Gain	V_A=V_B =±400mV	-1.012	-1.000	-0.988
	Input Resistance		30kΩ	40kΩ	50kΩ
	Offset	V_{in}=0mV	-3.4mV	0mV	3.4mV
	Bandwidth (small signal)	20mV peak-peak		6MHz	
	Bandwidth (large signal)	500mV peak-peak		3MHz	
Log	Output Voltage	V_{in} =±1.000V	±625 mV	±685 mV	±745 mV
	Transfer Characteristic (Change in output for a 10x change in input voltage)	V_{in} =±10mV, ±100mV,±1000mV		±60mV	
	Input Resistance		30kΩ	40kΩ	50kΩ
Auxiliary	Gain	RF = RS =20kΩ,		-0.993	
	Input Current	RF = RS =20kΩ, V_{in} = 0 mV		100nA	
	Offset	RF = RS =20kΩ, V_{in} = 0mV		2.0mV	
	Output Saturation Voltage	V_{in} =±50mV	<V_{SS}+0.2V		>V_{DD}-1.7V
	Open Loop		300	700	

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ELECTRICAL CHARACTERISTICS OF THE CELL (Continued)

Test Conditions: Temperature = 25 °C, V_{DD} = 3.0V±0.15V, V_{SS} = - 2.0V±0.10V

FUNCTION	PARAMETER	CONDITIONS	MIN	TYPICAL	MAX
Alog	Output Voltage	V_{in} = ±685mV	± 0.80V	±1.00V	±1.2V
	Transfer Characteristic (Multiplication of the output voltage for fixed steps in input voltage)	V_{in} =±565mV, ±625mV, ±685mV steps		±10	
Rectify	Output Voltage	V_{in} = –685mV V_{in} = 685mV	+0.80V -5.0mV	+1.00V	+1.2V 5.0mV
	Transfer Characteristic (Multiplication of the output voltage for fixed steps in input voltage)	V_{in} =–565mV, –625mV, –685mV steps		+10	
Off	Attenuation	V_{in} =±1.0V	-60dB	-80dB	
LOG/ALOG	Gain	V_{in}= ±1.0V		1.00	
	Bandwidth (small signal)	20mV peak-peak		6MHz	
	Bandwidth (large signal)	500mV peak-peak		2MHz	
LOG/REC	Gain	V_{in}= ±1.0V		1.00	
	Bandwidth (small signal)	20mV peak-peak		6MHz	
	Bandwidth (large signal)	500mV peak-peak		2MHz	

ELECTRICAL CHARACTERISTICS OF THE LOGIC FUNCTIONS(V_{DD}-V_{SS}=5.0V±0.25V)

FUNCTION	CONDITIONS	MIN	TYPICAL	MAX
(VOH (for output pins DOUT, CLCR)	IOH=-4mA	4.0V (WRT V_{SS})		5.0V (WRT V_{SS})
VOL (for outputs DOUT, CLCR	IOH=4mA	0.0V (WRT V_{SS})		0.4V (WRT V_{SS})
IIH (for inputs DATA CLOCK, $\overline{\text{RESET}}$,$\overline{\text{PD}}$)	VIH=5V (WRT V_{SS})			1.0µA
IIL (for inputs DATA CLOCK, $\overline{\text{RESET}}$,$\overline{\text{PD}}$)	VIL=0V (WRT V_{SS})	-1.0µA		
Max. CLOCK frequency			10MHz	

DESCRIPTION OF PIN FUNCTIONS

DATA Serial programming data is input to the TRAC via this pin. Each TRAC cell contains a 3-bit shift register that allows each cell to be programmed to the required analog function.

$\overline{\text{RESET}}$ Active low - The pin resets all on-chip shift registers to the logic zero state, which sets all TRAC cells to the OFF function. The pin should be held high while the device is being programmed and when the analog functions are in use.

$\overline{\text{PD}}$ Active low - The pin switches off the bias generators to the analog cells, which turns off the supply current to all the TRAC cells. This does not influence the programming of the cells so this feature can be used to reduce power consumption for applications that have a standby mode. The pin should be held high while the device is being programmed and when the analog functions are in use. This pin is permanently held high (V_{DD}) on the TRAC development board.

CLOCK Used to clock in the serial data to program the TRAC device. The on-chip shift registers are positive edge triggered.

DOUT This pin is the serial data output from cell 20 on the TRAC device. This is used for validation of programming of the TRAC device. This pin also allows two or more TRAC devices to be connected in a serial architecture. This is done by connecting the DOUT pin of the first TRAC device to the DATA pin of the second TRAC device, and connecting the CLOCK pins.

CLCR Clock Clear. When the TRAC device is used in stand alone applications CLCR is used as a control pin. It allows the downloading circuitry to be switched off when the programming serial data from the EEPROM is complete.

IO3..IO22 These are the analog inputs / outputs for cells 1 to 20.

IO1,IO2 These are the analog inputs for cells 1 and 2.

V_{DD} TRAC positive supply rail (+3V)

A_{GND} Analog Ground

V_{SS} TRAC negative supply rail (-2V) - this will also be the system ground

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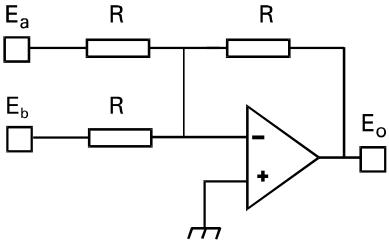
CELL FUNCTION DETAILS

ADD (code 011)
Can be represented as an operational amplifier with three resistors of equal value R. The virtual earth at the inverting input gives:-

$E_o = -R(E_a/R + E_b/R) = -(E_a + E_b)$

The output is the inverted sum of the input voltages.



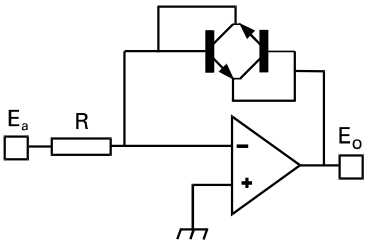
NEGATE (code 010)
The negate function is provided by an adder, but with only one input, therefore $E_o=-E_b$

NON INVERTING PASS (code 100)
Used for topological reasons. It provides a route through the cell with no modification. i.e. a unity gain amplifier

LOG (code 110)
Can be represented as an operational amplifier with a pair of back to back diodes in the negative feedback loop and an input resistor R. The virtual earth at the inverting input gives:-

$E_o = -kT/q \log (E_a/RI_o + 1)$

where
k = Boltzmann's constant
T = absolute temperature
q = electron charge
I_o=saturation current

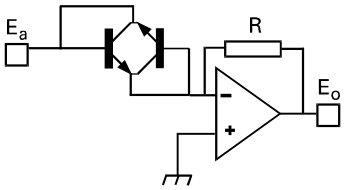


ANTI - LOG (code 101)

Similar to the log circuit except that the diodes and resistors are reversed. The output voltage is therfore given as :-

$E_o = -RI_o (\exp qE_a/KT - 1)$

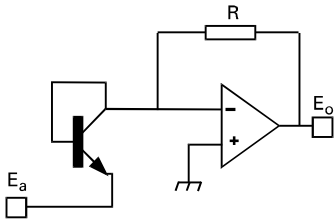
When the signal is processed through both log and anti-log the magnitude of the saturation current and absolute temperature cancel.



CELL FUNCTION DETAILS (Continued)

RECTIFIER (code 111)

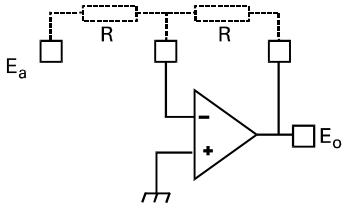
Similar to the anti-log function except that one of the diodes is removed so that a positive input gives zero output.



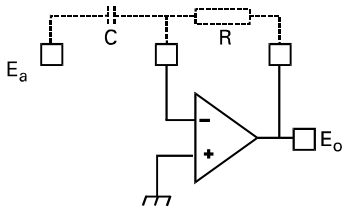
AUX (code 001)

As for an operational amplifier external components are used to provide the following functions - external components are shown dotted

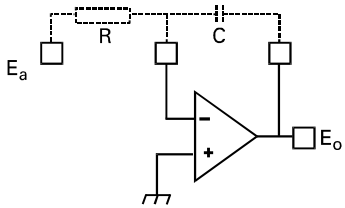
Amplification
Attenuation



Differentiation



Integration

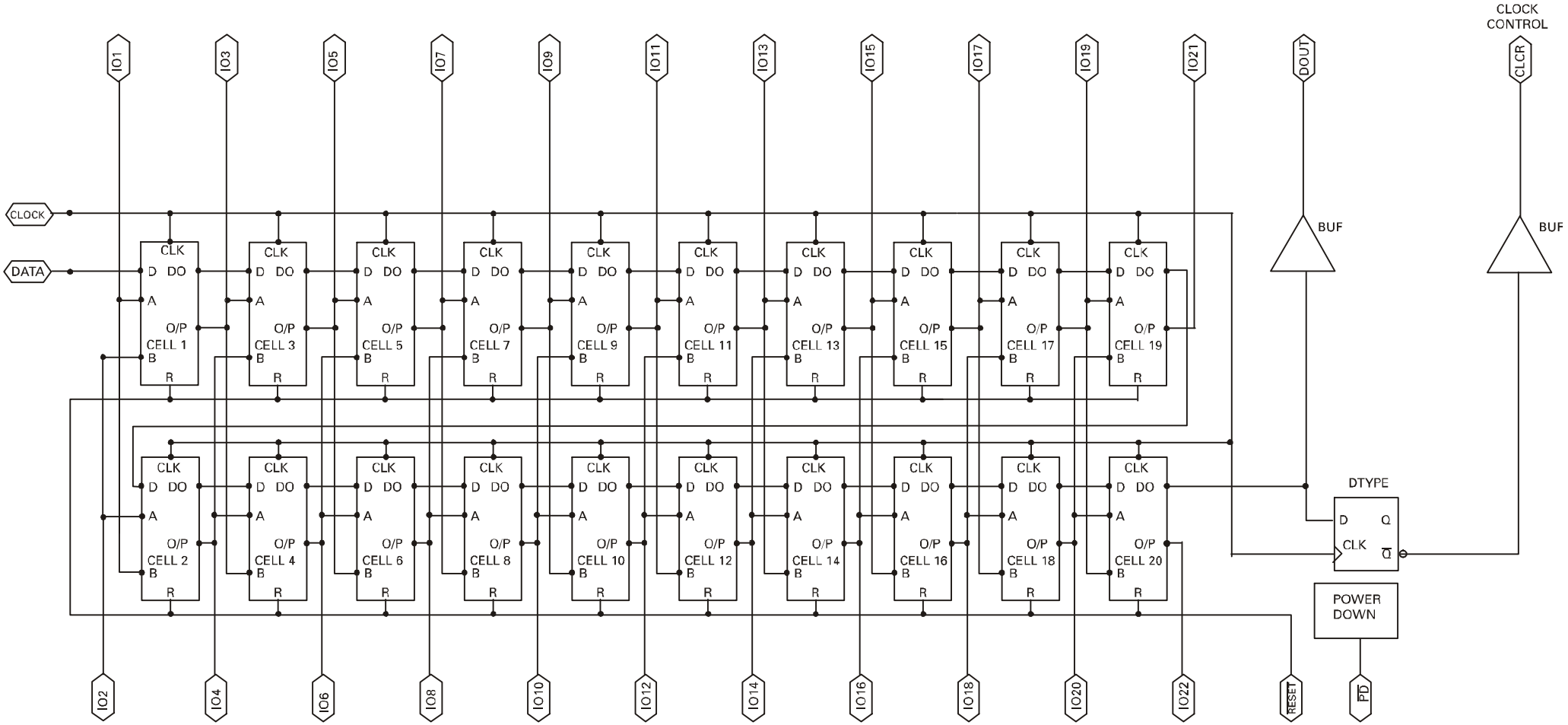


OFF (code 000)

In the off condition there is no signal path through the cell.

TRAC020LH

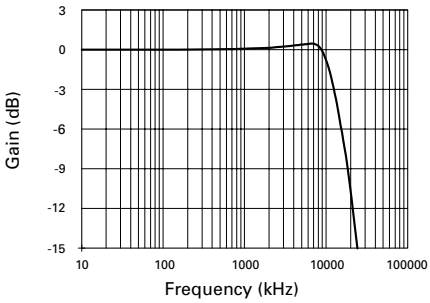
SCHEMATIC DIAGRAM



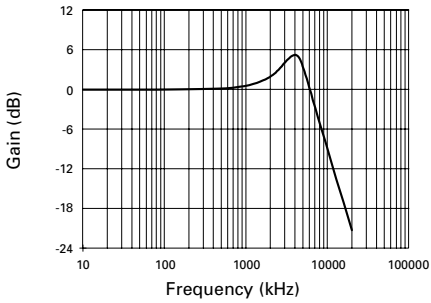
TRAC020LH

TYPICAL ELECTRICAL CHARACTERISTICS
Cell Frequency Responses, Small Signal Amplitude 20mV Pk-Pk

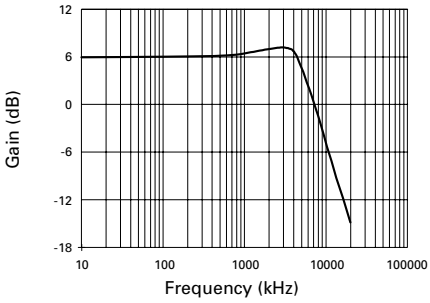
Test Conditions: Temperature = 25 °C, V_{DD} = 3.0V±0.15V, V_{SS} = - 2.0V±0.10V



NIP Small Signal Bandwidth

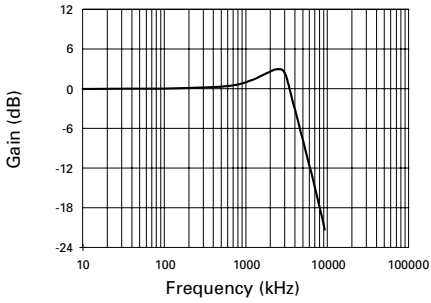


NEG Small Signal Bandwidth



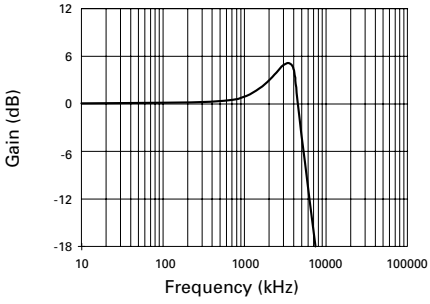
ADD Small Signal Bandwidth

(for both A and B inputs)



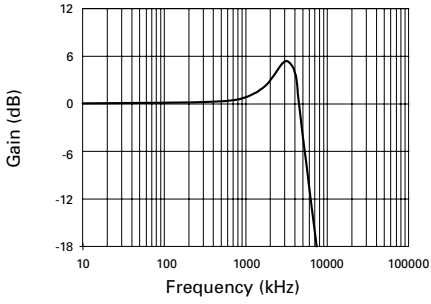
AUX Small Signal Bandwidth

(RS=RF=20K, RS Shunts preceeding OFF cell)



LOG/ALOG Small Signal Bandwidth

(26mV DC Biased)

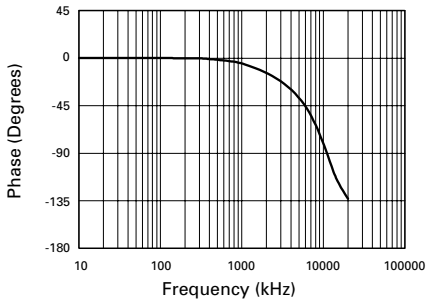


LOG/REC Small Signal Bandwidth

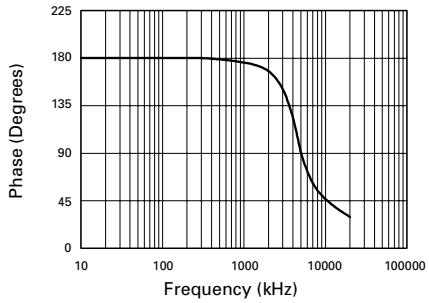
(26mV DC Biased)

TYPICAL ELECTRICAL CHARACTERISTICS
Cell Phase Delay, Small Signal Amplitude 20mV Pk-Pk

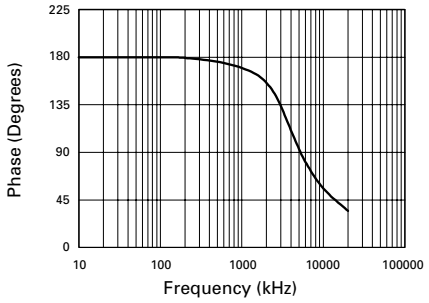
Test Conditions: Temperature = 25 °C, V_{DD} = 3.0V±0.15V, V_{SS} = - 2.0V±0.10V



NIP Phase Shift V Frequency

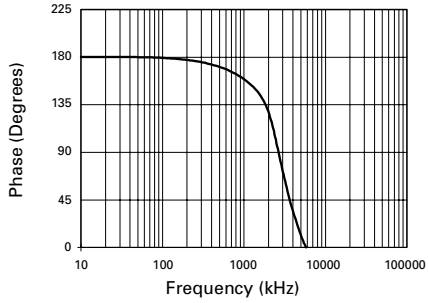


NEG Phase Shift V Frequency



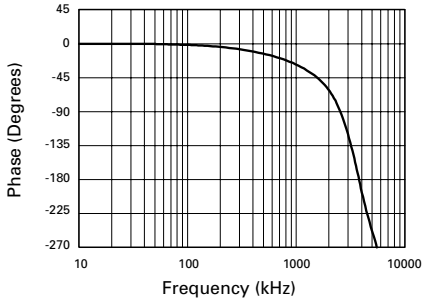
ADD Phase Shift V Frequency

(For both A and B inputs)



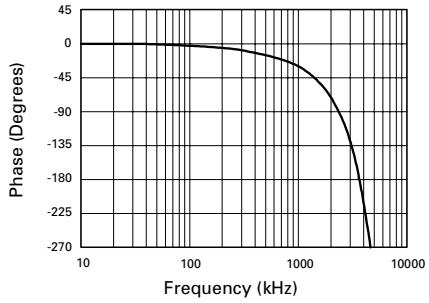
AUX Phase Shift V Frequency

(RS=RF=20K, RS Shunts preceeding OFF Cell)



LOG/ALOG Phase Shift V Frequency

(26mV DC Biased)



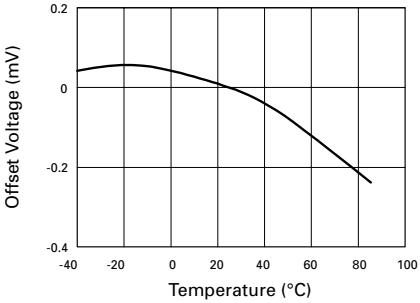
LOG/REC Phase Shift V Frequency

(26mV DC Biased)

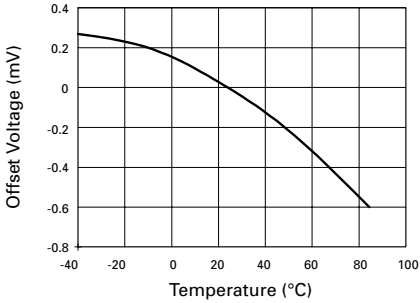
TRAC020LH

TYPICAL ELECTRICAL CHARACTERISTICS
Cell Offset Voltage against Temperature CharacteristicsTest Conditions:

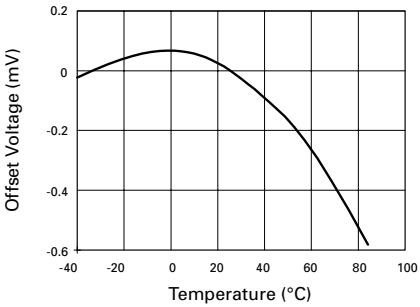
Temperature = 25 °C, V_{DD} = 3.0V±0.15V, V_{SS} = - 2.0V±0.10V



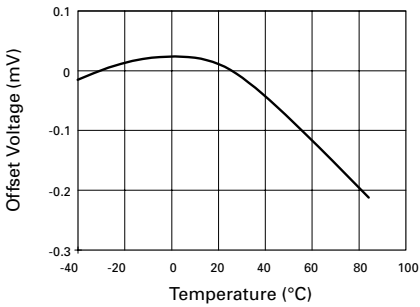
NIP Offset Voltage V Temp.



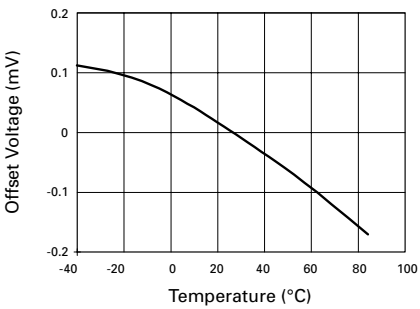
NEG Offset Voltage V Temp.



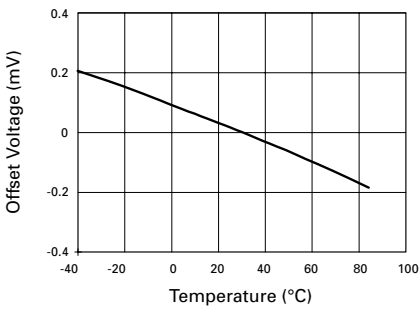
ADD Offset Voltage Vs Temp.



AUX Offset Voltage V Temp.



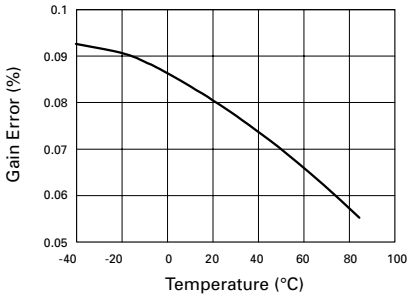
LOG/ALOG Offset Voltage V Temp.



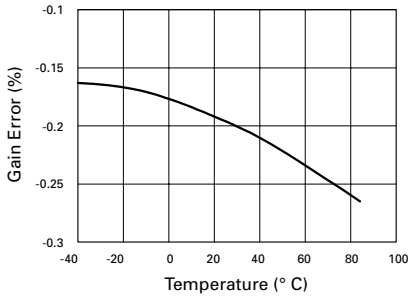
LOG/REC Offset Voltage V Temp.

TYPICAL ELECTRICAL CHARACTERISTICS
Cell Voltage Gain against Temperature Characteristics

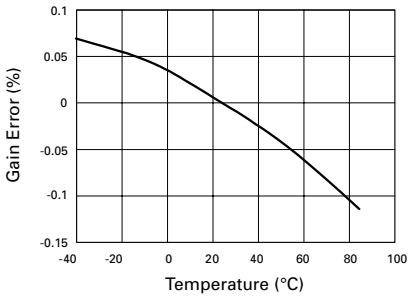
Test Conditions: Temperature = 25 °C, V_{DD} = 3.0V±0.15V, V_{SS} = - 2.0V±0.10V



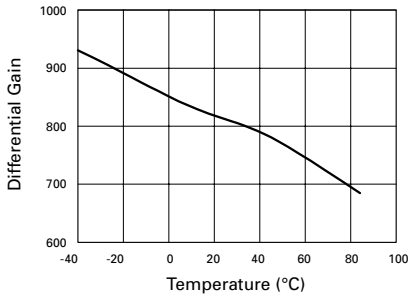
NIP Gain Error V Temp.



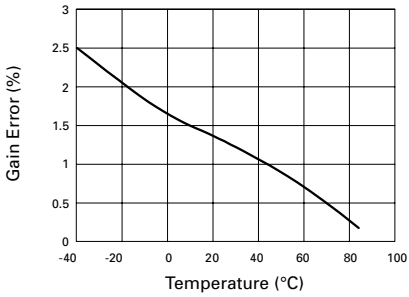
NEG Gain Error V Temp.



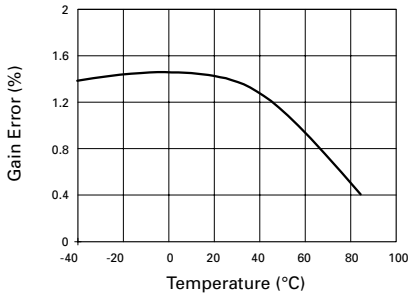
ADD Gain Error V Temp.



AUX Open Loop Gain V Temp.



LOG/ALOG Gain Error V Temp.

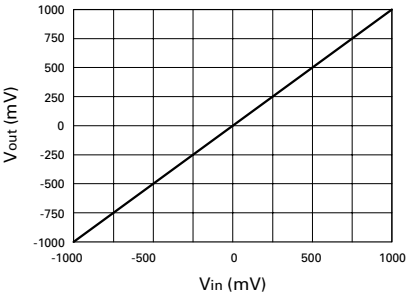


LOG/REC Gain Error V Temp.

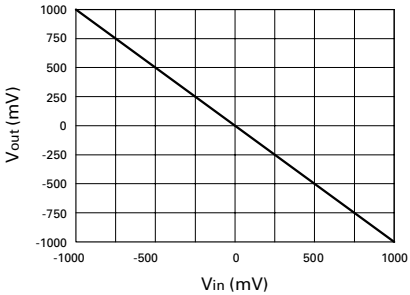
TRAC020LH

TYPICAL ELECTRICAL CHARACTERISTICS
Cell DC Transfer Characteristics

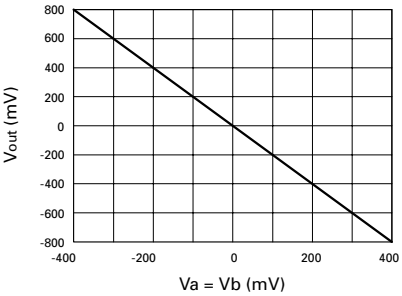
Test Conditions: Temperature = 25 °C, V_{DD} = 3.0V±0.15V, V_{SS} = - 2.0V±0.10V



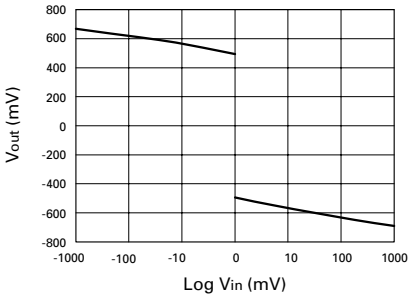
NIP DC Transfer Characteristics



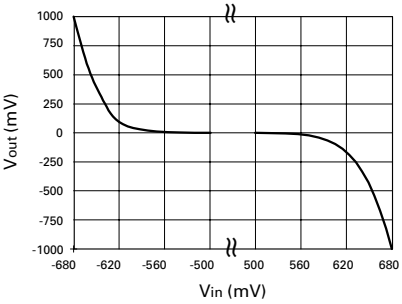
NEG DC Transfer Characteristics



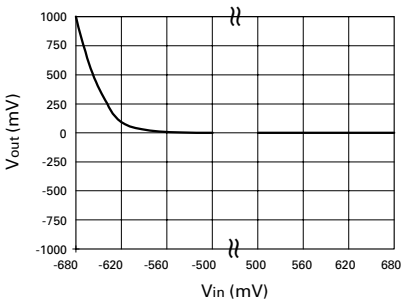
ADD DC Transfer Characteristics



LOG DC Transfer Characteristics



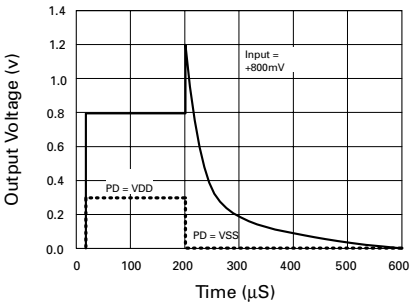
ALOG DC Transfer Characteristics



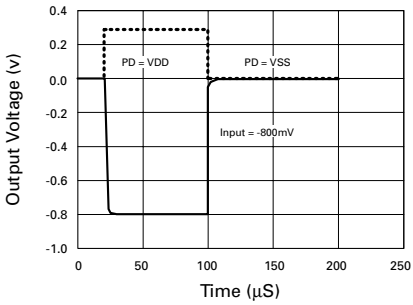
REC DC Transfer Characteristics

TYPICAL ELECTRICAL CHARACTERISTICS
Settling Performance for Power Down and Data Clocking

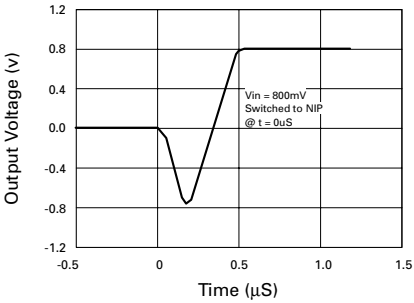
Test Conditions: Temperature = 25 °C, V_{DD} = 3.0V±0.15V, V_{SS} = - 2.0V±0.10V



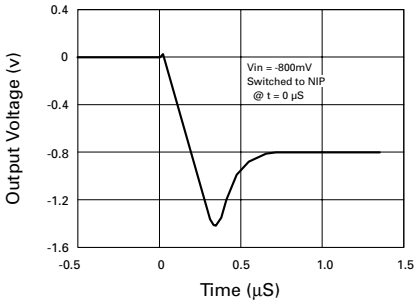
NIP Power Down Response



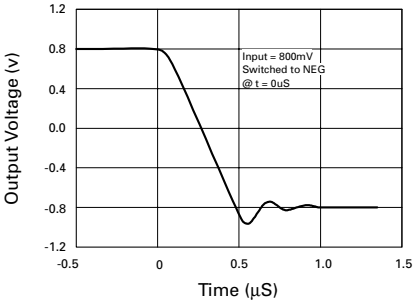
NIP Power Down Response



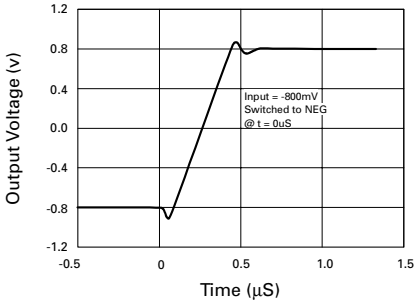
OFF Cell to NIP Cell Response



OFF Cell to NIP Cell Response



NIP Cell to NEG Cell Response

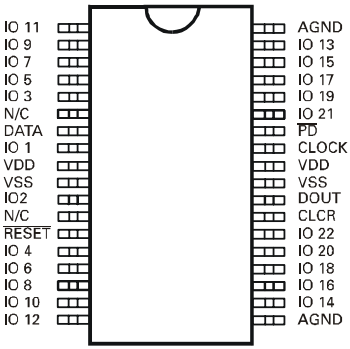


NIP Cell to NEG Cell Response

TRAC020LH

CONNECTION DIAGRAM

QSOP 36 Lead



Note:

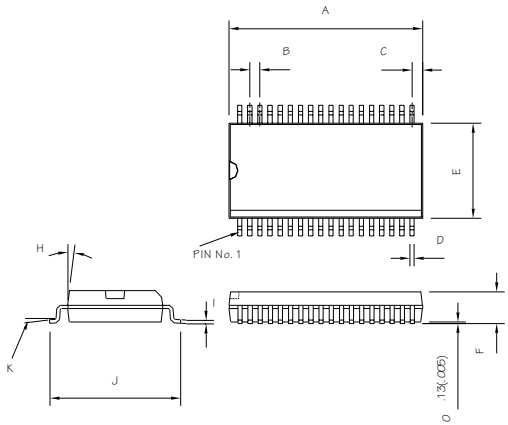
For clarity the IO pin definition has been changed from previous issue

TOP VIEW

(NOT TO SCALE)

PACKAGING INFORMATION

SYMBOL	QSOP 36 LEAD			
	MIN		MAX	
	MM	INCHES	MM	INCHES
A	15.20	.598	15.40	.606
B	0.8MM .031 INCHES BSC			
C	0.85MM .033 INCHES REF			
D	0.29	.011	0.39	.015
E	7.4 0	.291	7.60	.299
F	2.44	.096	2.64	.104
H	7 NOMINAL			
I	0.23	.0091	0.32	.0125
J	10.11	.398	10.51	.414
K	0°		8°	



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