THE DATASHEET OF

TPS65186RGZT

TPS65186 PMIC for E Ink® Vizplex™ Enabled Electronic Paper Display

1 Features

- Single Chip Power-Management Solution for E Ink® Vizplex™ Electronic Paper Displays
- Generates Positive and Negative Gates, Source Driver Voltages, and Back-Plane Bias From a Single, Low-Voltage Input Supply
- Supports 9.7 Inch and Larger Panel Size
- 3-V to 6-V Input Voltage Range
- Boost Converter for Positive Rail Base
- Inverting Buck-Boost Converter for Negative Rail Base
- Two Adjustable LDOs for Source Driver Supply
  - LDO1: 15 V, 120 mA (VPOS)
  - LDO2: –15 V, 120 mA (VNEG)
- Accurate Output Voltage Tracking
  - VPOS – VNEG = ±50 mV
- Two Charge Pumps for Gate Driver Supply
  - CP1: 22 V, 10 mA (VDDH)
  - CP2: –20 V, 12 mA, (VEE)
- Adjustable VCOM Driver for Accurate Panel-Backplane Biasing
  - 0 V to –5.11 V
  - ± 1.5% accuracy (±10 mV)
  - 9-Bit Control (10-mV Nominal Step Size)
- Integrated 10-Ω, 3.3-V Power Switch for Disabling System Power Rail to E-Ink Panel

2 Applications

- Power Supply for Active Matrix E Ink Vizplex Panels
- EPD Power Supplies
- E-Book Readers
- EPSON® S1D13522 (ISIS) Timing Controller
- EPSON® S1D13521 (Broadsheet) Timing Controller
- Application Processors With Integrated or Software Timing Controller (OMAP™)

3 Description

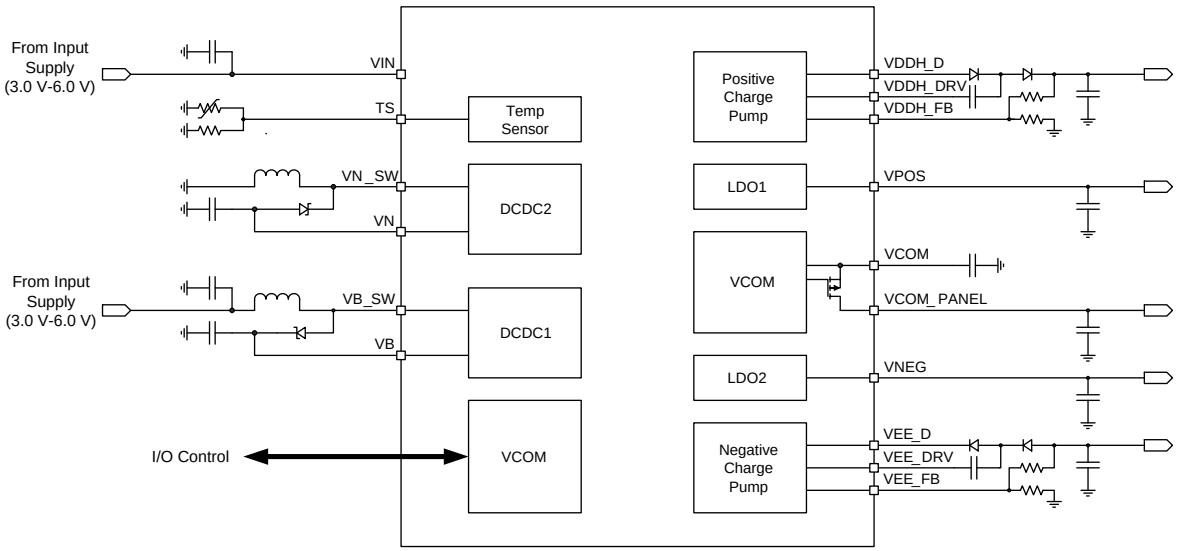
The TPS65186 device is a single-chip power supply designed to for E Ink Vizplex displays used in portable e-reader applications, and the device supports panel sizes up to 9.7 inches and greater. Two high-efficiency DC-DC boost converters generate ±16-V rails that are boosted to 22 V and –20 V by two change pumps to provide the gate driver supply for the Vizplex panel. Two tracking LDOs create the ±15-V source driver supplies that support up to 120-mA of output current. All rails are adjustable through the I^2C interface to accommodate specific panel requirements.

Device Information(1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
TPS65186	VQFN (48)	7.00 mm × 7.00 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Typical Application Schematic



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4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Original (July 2011) to Revision A **Page**

- Added *ESD Ratings* table, *Feature Description* section, *Device Functional Modes*, *Application and Implementation* section, *Power Supply Recommendations* section, *Layout* section, *Device and Documentation Support* section, and *Mechanical, Packaging, and Orderable Information* section ... 1
- Changed R_{OUT} from “TBD” to “5 Ω” ... 8

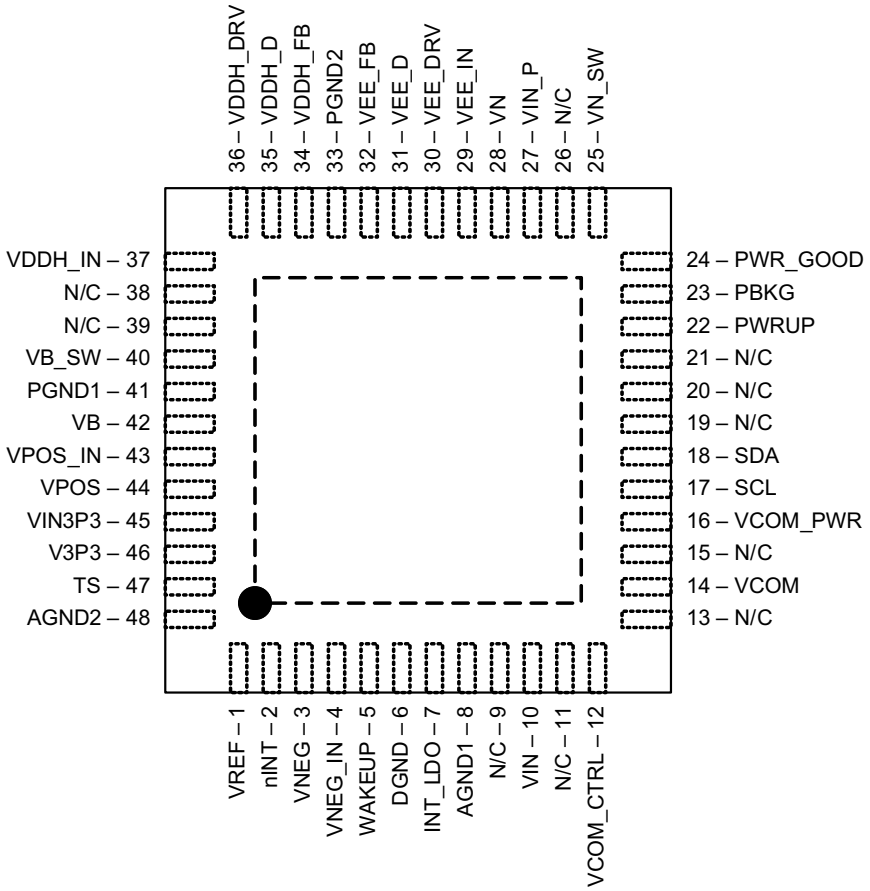
5 Description (continued)

Accurate back-plane biasing is provided by a linear amplifier that can be adjusted from 0 V to –5.11 V with 9-bit control through the serial interface; it can also source or sink current depending on panel condition. The TPS65186 supports automatic panel kickback voltage measurement, which eliminates the need for manual VCOM calibration in the production line. The measurement result can be stored in nonvolatile memory to become the new VCOM power-up default value.

TPS65186 is available in a 48-pin 7-mm × 7-mm^2 VQFN with 0.5-mm pitch.

6 Pin Configuration and Functions

RGZ Package
48-Pin VQFN
Top View



Pin Functions

PIN		I/O	DESCRIPTION
NAME	NO.		
AGND1	8	—	Analog ground for general analog circuitry
AGND2	48	—	Reference point to external thermistor and linearization resistor
DGND	6	—	Digital ground. Connect to ground plane.
INT_LDO	7	O	Filter pin for 2.7-V internal supply
nINT	2	O	Open drain interrupt pin (active low)
N/C	9, 11, 13, 15, 19, 20, 21, 26, 38, 39	—	Not internally connected

Pin Functions (continued)

PIN		I/O	DESCRIPTION
NAME	NO.		
PBKG	23	—	Die substrate. Connect to VN (–16 V) with short, wide trace. Wide copper trace will improve heat dissipation.
PGND1	41	—	Power ground for DCDC1
PGND2	33	—	Power ground for CP1 (VDDH) and CP2 (VEE) charge pumps
PWR_GOOD	24	O	Open-drain power good output pin. Pin is pulled low when one or more rails are disabled or not in regulation. DCDC1, DCDC2, and VCOM have no effect on this pin. (1)
PWRUP	22	I	Power-up pin. Pull this pin high to power up all output rails. (1)
SCL	17	I	Serial interface (I^2C) clock input
SDA	18	I/O	Serial interface (I^2C) data input/output
TS	47	I	Thermistor input pin. Connect a 10-kΩ NTC thermistor and a 43-kΩ linearization resistor between this pin and AGND.
V3P3	46	O	Output pin of 3.3-V power switch
VB	42	I	Feedback pin for boost converter (DCDC1) and supply for VPOS LDO and VDDH charge pump
VB_SW	40	O	Boost converter switch out (DCDC1)
VCOM	14	I	Filter pin for panel common-voltage driver
VCOM_CTRL	12	I	VCOM enable. Pull this pin high to enable the VCOM amplifier. When pin is pulled low and VN is enabled, VCOM discharge is enabled. (2)
VCOM_PWR	16	I	Internal supply input pin to VCOM buffer. Connect to the output of DCDC2.
VDDH_D	35	O	Base voltage output pin for positive charge pump (CP1)
VDDH_DRV	36	O	Driver output pin for positive charge pump (CP1)
VDDH_FB	34	I	Feedback pin for positive charge pump (CP1)
VDDH_IN	37	I	Input supply pin for positive charge pump (CP1)
VEE_D	31	I	Base voltage output pin for negative charge pump (CP2)
VEE_DRV	30	O	Driver output pin for negative charge pump (CP2)
VEE_FB	32	I	Feedback pin for negative charge pump (CP2)
VEE_IN	29	I	Input supply pin for negative charge pump (CP2) (VEE)
VIN	10	I	Input power supply to general circuitry
VIN3P3	45	I	Input pin to 3.3-V power switch
VIN_P	27	I	Input power supply to inverting buck-boost converter (DCDC2)
VN	28	I	Feedback pin for inverting buck-boost converter (DCDC2) and supply for VNEG LDO and VEE charge pump
VNEG	3	O	Negative supply output pin for panel source drivers
VNEG_IN	4	I	Input pin for LDO2 (VNEG)
VN_SW	25	O	Inverting buck-boost converter switch out (DCDC2)
VREF	1	O	Filter pin for 2.25-V internal reference to ADC
VPOS	44	O	Positive supply output pin for panel source drivers
VPOS_IN	43	I	Input pin for LDO1 (VPOS)
WAKEUP	5	I	Wake-up pin (active high). Pull this pin high to wake up from sleep mode. IC accepts I^2C commands after WAKEUP pin is pulled high but power rails remain disabled until PWRUP pin is pulled high. (3)
PowerPad	—	—	PowerPad, internally connected to PBKG. Connect to VN with short, wide trace. Wide copper trace will improve heat dissipation. PowerPad must not be connected to ground.

(1) There will be 0-ns of deglitch for PWRx.
(2) There will be 62.52-µs of deglitch for VCOM_CTRL.
(3) There will be 93.75-µs of deglitch for WAKEUP.

7 Specifications

7.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted) (1)(2)

		MIN	MAX	UNIT
	Input voltage at VIN(2), VIN_P, VIN3P3	–0.3	7	V
	Ground pins to system ground	–0.3	0.3	V
	Voltage at SDA, SCL, WAKEUP, PWRUP, VCOM_CTRL, VDDH_FB, VEE_FB, PWR_GOOD, nINT	–0.3	3.6	V
	Voltage on VB, VB_SW, VPOS_IN, VDDH_IN	–0.3	20	V
	Voltage on VN, VEE_IN, VCOM_PWR, VNEG_IN	–20	0.3	V
	Voltage from VIN_P to VN_SW	–0.3	30	V
	Peak output current	Internally limited		mA
	Continuous total power dissipation		2	W
T_J	Operating junction temperature	–10	125	°C
T_A	Operating ambient temperature(3)	–10	85	°C
T_{stg}	Storage temperature	–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute maximum rated conditions for extended periods may affect device reliability.
(2) All voltage values are with respect to network ground terminal.
(3) TI recommends that copper plane in proper size on board be in contact with die thermal pad to dissipate heat efficiently. Thermal pad is electrically connected to PBKG, which is supposed to be tied to the output of buck-boost converter. Thus wide copper trace in the buck-boost output will help heat dissipated efficiently.

7.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±2000	V
		Charged device model (CDM), per JEDEC specification JESD22-C101(2)	±500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

7.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
	Input voltage at VIN, VIN_P, VIN3P3	3	3.7	6	V
	Voltage at SDA, SCL, WAKEUP, PWRUP, VCOM_CTRL, VDDH_FB, VEE_FB, PWR_GOOD, nINT	0		3.6	V
T_A	Operating ambient temperature	–10		85	°C
T_J	Operating junction temperature	–10		125	°C

7.4 Thermal Information

THERMAL METRIC[1]		TPS65186 RGZ [VQFN] 48 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	30	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	15.6	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	6.6	°C/W
ψ_{JT}	Junction-to-top characterization parameter	0.2	°C/W
ψ_{JB}	Junction-to-board characterization parameter	6.6	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	0.9	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, SPRA953.

7.5 Electrical Characteristics

V_{IN} = 3.7 V, T_A = –10°C to 85ºC, Typical values are at T_A = 25ºC (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
INPUT VOLTAGE						
V_{IN}	Input voltage range		3	3.7	6	V
V_{UVLO}	Undervoltage lockout threshold	V_{IN} falling		2.9		V
V_{HYS}	Undervoltage lockout hysteresis	V_{IN} rising		400		mV
INPUT CURRENT						
I_Q	Operating quiescent current into V_{IN}	Device switching, no load		5.5		mA
I_{STD}	Operating quiescent current into V_{IN}	Device in standby mode		130		µA
I_{SLEEP}	Shutdown current	Device in sleep mode		3.5	10	µA
INTERNAL SUPPLIES						
VI_{NT_LDO}	Internal supply			2.7		V
C_{INT_LDO}	Nominal output capacitor	Capacitor tolerance ±10%	1	4.7		µF
V_{REF}	Internal supply			2.25		V
C_{REF}	Nominal output capacitor	Capacitor tolerance ±10%	3.3	4.7		µF
DCDC1 (POSITIVE BOOST REGULATOR)						
V_{IN}	Input voltage range		3	3.7	6	V
PG	Power good threshold	Fraction of nominal output voltage		90%		
	Power good time-out	Not tested in production		50		ms
V_{OUT}	Output voltage range			16		V
	DC set tolerance		–4.5%		4.5%	
I_{OUT}	Output current				250	mA
$R_{DS(ON)}$	MOSFET ON-resistance	V_{IN} = 3.7 V		350		mΩ
I_{LIMIT}	Switch current limit			1.5[1]		A
	Switch current accuracy		–30%		30%	
f_{SW}	Switching frequency			1		MHz
L_{DCDC1}	Inductor			2.2		µH
C_{DCDC1}	Nominal output capacitor	Capacitor tolerance ±10%	1	2 × 4.7		µF
ESR	Output capacitor ESR			20		mΩ

(1) Contact TI for 1-A, 2-A, or 2.5-A option.

Electrical Characteristics (continued)

V_{IN} = 3.7 V, T_A = –10°C to 85ºC, Typical values are at T_A = 25ºC (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
DCDC2 (INVERTING BUCK-BOOST REGULATOR)						
V_{IN}	Input voltage range		3	3.7	6	V
PG	Power good threshold	Fraction of nominal output voltage		90%		
	Power good time-out	Not tested in production		50		ms
V_{OUT}	Output voltage range			–16		V
	DC set tolerance		–4.5%		4.5%	
I_{OUT}	Output current				250	mA
$R_{DS(ON)}$	MOSFET ON-resistance	V_{IN} = 3.7 V		350		mΩ
I_{LIMIT}	Switch current limit			1.5 (1)		A
	Switch current accuracy		–30%		30%	
L_{DCDC1}	Inductor			4.7		µH
C_{DCDC1}	Nominal output capacitor	Capacitor tolerance ±10%	1	3x4.7		µF
ESR	Capacitor ESR			20		mΩ
LDO1 (VPOS)						
V_{POS_IN}	Input voltage range		15.2	16	16.8	V
PG	Power good threshold	Fraction of nominal output voltage		90%		
	Power good time-out	Not tested in production		50		ms
V_{SET}	Output voltage set value	V_{IN} = 16 V, VSET[2:0] = 0x3h to 0x6h	14.25	15	15	V
$V_{INTERVAL}$	Output voltage set resolution	V_{IN} = 16 V		250		mV
V_{OUTTOL}	Output tolerance	V_{SET} = 15 V, I_{LOAD} = 20 mA	–1%		1%	
$V_{DROPOUT}$	Dropout voltage	I_{LOAD} = 120 mA			250	mV
$V_{LOADREG}$	Load regulation – DC	I_{LOAD} = 10% to 90%			1%	
I_{LOAD}	Load current range				120	mA
I_{LIMIT}	Output current limit		120			mA
C_{LDO1}	Nominal output capacitor	Capacitor tolerance ±10%	1	4.7		µF
LDO2 (VNEG)						
V_{NEG_IN}	Input voltage range		16.8	16	–15.2	V
PG	Power good threshold	Fraction of nominal output voltage		90%		
	Power good time-out	Not tested in production		50		ms
V_{SET}	Output voltage set value	V_{IN} = –16 V VSET[2:0] = 0x3h to 0x6h	–15	–15	–14.25	V
$V_{INTERVAL}$	Output voltage set resolution	V_{IN} = –16 V		250		mV
V_{OUTTOL}	Output tolerance	V_{SET} = –15 V, I_{LOAD} = –20 mA	–1%		1%	
$V_{DROPOUT}$	Dropout voltage	I_{LOAD} = 120 mA			250	mV
$V_{LOADREG}$	Load regulation – DC	I_{LOAD} = 10% to 90% of $I_{LOAD,MAX}$			1%	
I_{LOAD}	Load current range				120	mA
I_{LIMIT}	Output current limit		120			mA
C_{LDO2}	Nominal output capacitor	Capacitor tolerance ±10%	1	4.7		µF

Electrical Characteristics (continued)

V_{IN} = 3.7 V, T_A = –10°C to 85ºC, Typical values are at T_A = 25ºC (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
LD01 (POS) AND LDO2 (VNEG) TRACKING						
V_{DIFF}	Difference between VPOS and VNEG	V_{SET} = ±15 V, I_{LOAD} = ±20 mA, 0°C to 60°C	–50		50	mV
VCOM DRIVER						
I_{VCOM}	Drive current			15		mA
V_{COM}	Allowed operating range	Outside this range VCOM is shut down and VCOMF interrupt is set	–5.5		1	V
	Accuracy	VCOM[8:0] = 0x07Dh (–1.25 V), V_{IN} = 3.4 V to 4.2 V, no load	–0.8%		0.8%	
		VCOM[8:0] = 0x07Dh (–1.25 V), V_{IN} = 3 V to 6 V, no load	–1.5%		1.5%	
	Output voltage range		–5.11		0	V
	Resolution	1LSB		10		mV
	Max number of EEPROM writes	V_{COM} calibration			100	
R_{OUT}	Output impedance	VCOM_CTRL = high, Hi-Z = 0		5		Ω
R_{IN}	Input impedance, HiZ state	HiZ = 1	150			MΩ
C_{VCOM}	Nominal output capacitor	Capacitor tolerance ±10%	3.3	4.7		µF
CP1 (VDDH) CHARGE PUMP						
V_{DDH_IN}	Input voltage range		15.2	16	16.8	V
PG	Power good threshold	Fraction of nominal output voltage		90%		
	Power good time-out	Not tested in production		50		ms
V_{FB}	Feedback voltage			0.998		V
	Accuracy	I_{LOAD} = 2 mA	–2%		2%	
V_{DDH_OUT}	Output voltage range	V_{SET} = 22 V, I_{LOAD} = 2 mA	21	22	23	V
I_{LOAD}	Load current range				10	mA
f_{SW}	Switching frequency			560		kHz
C_D	Driver capacitor			10		nF
C_O	Output capacitor		1	2.2		µF
CP2 (VEE) NEGATIVE CHARGE PUMP						
V_{EE_IN}	Input voltage range		16.8	–16	–15.2	V
PG	Power good threshold	Fraction of nominal output voltage		90%		
	Power good time-out	Not tested in production		50		ms
V_{FB}	Feedback voltage			–0.994		V
	Accuracy	I_{LOAD} = 2 mA	–2%		2%	
V_{EE_OUT}	Output voltage range	V_{SET} = –20 V, I_{LOAD} = 3 mA	–21	–20	–19	V
I_{LOAD}	Load current range				12	mA
f_{SW}	Switching frequency			560		kHz
C_D	Driver capacitor			10		nF
C_O	Nominal output capacitor	Capacitor tolerance ±10%	1	2.2		µF

Electrical Characteristics (continued)

V_{IN} = 3.7 V, T_A = –10°C to 85ºC, Typical values are at T_A = 25ºC (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
VIN3P3 TO V3P3 SWITCH						
$R_{DS(ON)}$	MOSFET ON-resistance	VIN3P3 = 3.3 V, I_D = 10 mA Over full temperature range		10.5		Ω
		VIN3P3 = 2.7 V, I_D = 10 mA Over full temperature range		12.3		
R_{DIS}	Discharge impedance to ground	V3P3EN = 0	800	1000	1200	Ω
THERMISTOR MONITOR(2)						
A_{TMS}	Temperature to voltage ratio	Not tested in production		–0.0161		V/°C
$Offset_{TMS}$	Offset	Temperature = 0°C		1.575		V
V_{TMS_HOT}	Temp hot trip voltage (T = 50°C)	TEMP_HOT_SET = 0x8C		0.768		V
V_{TMS_COOL}	Temp hot escape voltage (T = 45°C)	TEMP_COOL_SET = 0x82		0.845		V
V_{TMS_MAX}	Maximum input level			2.25		V
R_{NTC_PU}	Internal pullup resistor			7.307		kΩ
R_{LINEAR}	External linearization resistor			43		kΩ
ADC_{RES}	ADC resolution	Not tested in production, 1 bit		16.1		mV
ADC_{DEL}	ADC conversion time	Not tested in production		19		µs
$TMST_{TOL}$	Accuracy	Not tested in production	–1		1	LSB
LOGIC LEVELS AND TIMING CHARTERISTICS (SCL, SDA, nINT, PWR_GOOD, PWRUP)						
V_{OL}	Output low threshold level	I_O = 3 mA, sink current (SDA, nINT, PWR_GOOD)			0.4	V
V_{IL}	Input low threshold level				0.4	V
V_{IH}	Input high threshold level		1.2			V
$I_{(bias)}$	Input bias current	V_{IO} = 1.8 V			1	µA
$t_{deglitch}$	Deglitch time, WAKEUP pin	Not tested in production		500		µs
	Deglitch time, PWRUP pin	Not tested in production		400		
f_{SCL}	SCL clock frequency				400	kHz
	I^2C slave address	7-bit address			0 × 48h(3)	
OSCILLATOR						
f_{OSC}	Oscillator frequency			9		MHz
	Frequency accuracy	T_A = –40°C to 85°C	–10%		10%	
THERMAL SHUTDOWN						
T_{SHTDWN}	Thermal trip point			150		°C
	Thermal hysteresis			20		°C

(2) 10-kΩ Murata NCP18XH103F03RB thermistor (1%) in parallel with a linearization resistor (43 kΩ, 1%) are used at TS pin for panel temperature measurement.
(3) Contact TI for alternate address of 0 × 68h.

7.6 Timing Requirements: Data Transmission

V_{BAT} = 3.6 V ±5%, T_A = 25ºC, C_L = 100 pF (unless otherwise noted)

			MIN	NOM	MAX	UNIT
$f_{(SCL)}$	Serial clock frequency		100		400	kHz
$t_{HD;STA}$	Hold time (repeated) START condition. After this period, the first clock pulse is generated.	SCL = 100 kHz	4			µs
		SCL = 400 kHz	600			ns
t_{LOW}	LOW period of the SCL clock	SCL = 100 kHz	4.7			µs
		SCL = 400 kHz	1.3			
t_{HIGH}	HIGH period of the SCL clock	SCL = 100 kHz	4			µs
		SCL = 400 kHz	600			ns
$t_{SU;STA}$	Setup time for a repeated START condition	SCL = 100 kHz	4.7			µs
		SCL = 400 kHz	600			ns
$t_{HD;DAT}$	Data hold time	SCL = 100 kHz	0		3.45	µs
		SCL = 400 kHz	0		900	ns
$t_{SU;DAT}$	Data setup time	SCL = 100 kHz	250			ns
		SCL = 400 kHz	100			
t_r	Rise time of both SDA and SCL signals	SCL = 100 kHz			1000	ns
		SCL = 400 kHz			300	
t_f	Fall time of both SDA and SCL signals	SCL = 100 kHz			300	ns
		SCL = 400 kHz			300	
$t_{SU;STO}$	Setup time for STOP condition	SCL = 100 kHz	4			µs
		SCL = 400 kHz	600			ns
t_{BUF}	Bus Free Time Between Stop and Start Condition	SCL = 100 kHz	4.7			µs
		SCL = 400 kHz	1.3			
t_{SP}	Pulse width of spikes that must be suppressed by the input filter	SCL = 100 kHz	n/a		n/a	ns
		SCL = 400 kHz	0		50	
C_b	Capacitive load for each bus line	SCL = 100 kHz			400	pF
		SCL = 400 kHz			400	

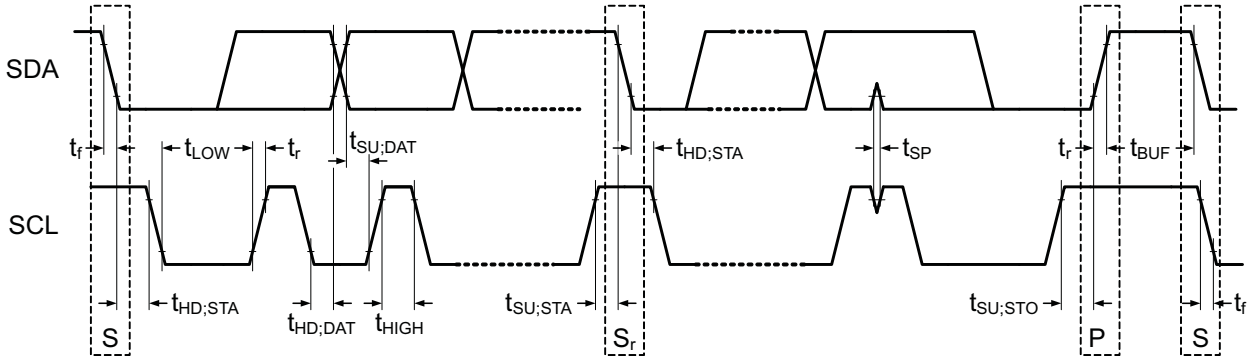
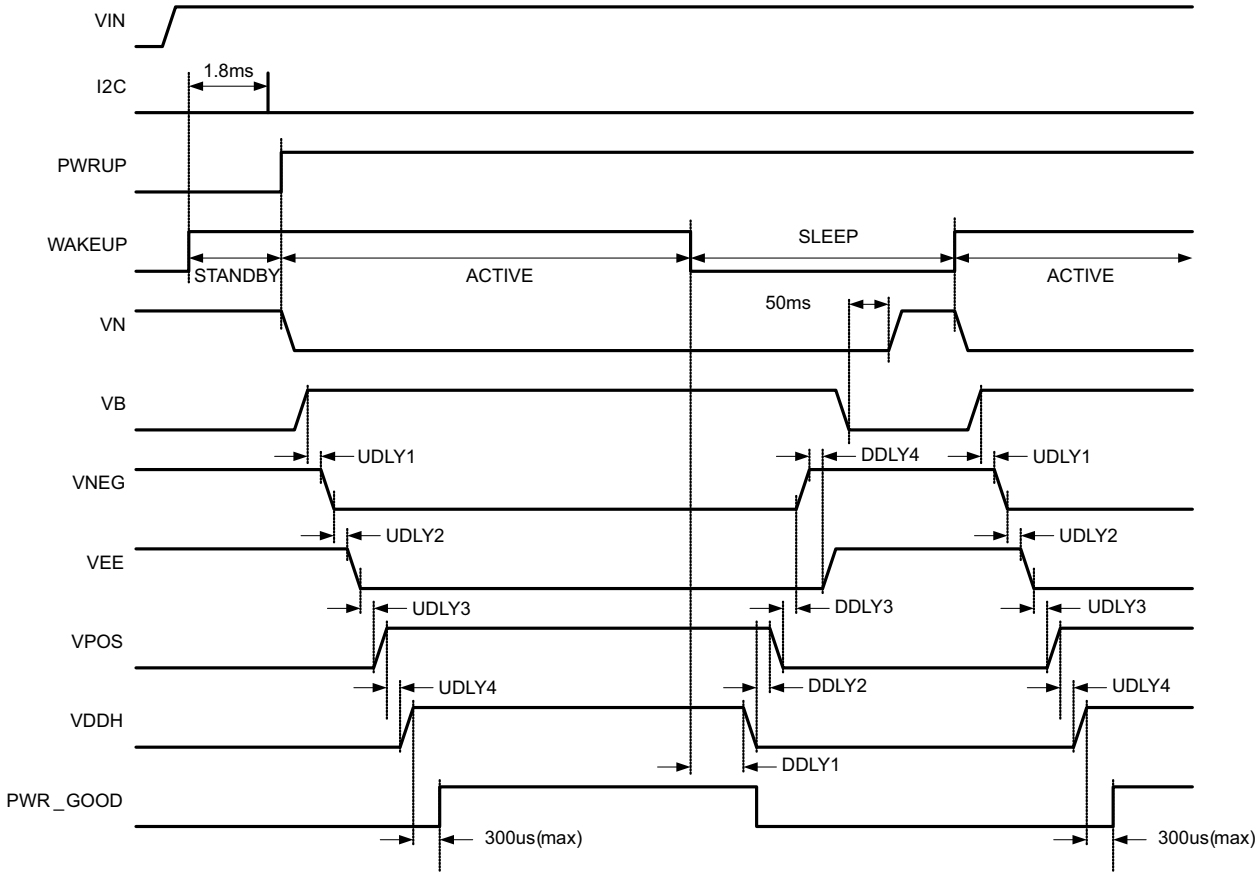


Figure 1. I²C Data Transmission Timing



Minimum delay time between WAKEUP rising edge and IC ready to accept I^2C transaction.

In this example, the first power-up sequence is started by pulling the PWRUP pin high (rising edge). Power-down is initiated by pulling the WAKEUP pin low (device enters sleep mode). The second power-up sequence is initiated by pulling the WAKEUP pin high while the PWRUP pin is also high (power up from sleep to active).

Figure 2. Power-Up and Power-Down Timing Diagram

7.7 Typical Characteristics

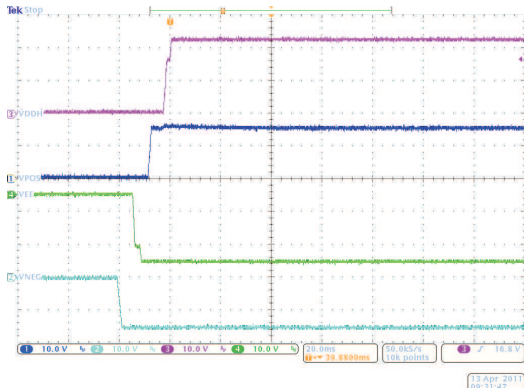


Figure 3. Default Power-Up Sequence

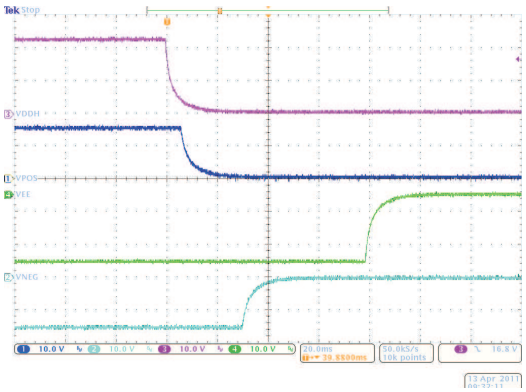
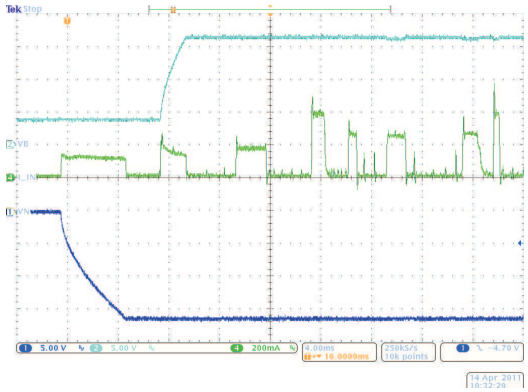
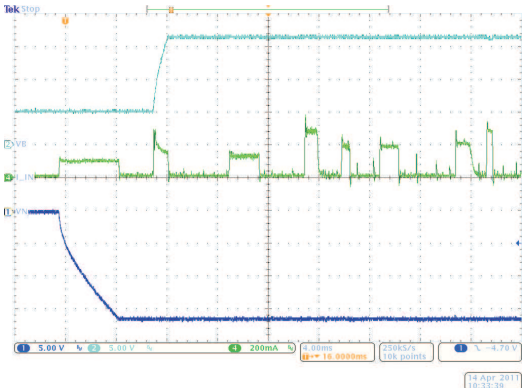


Figure 4. Default Power-Down Sequence



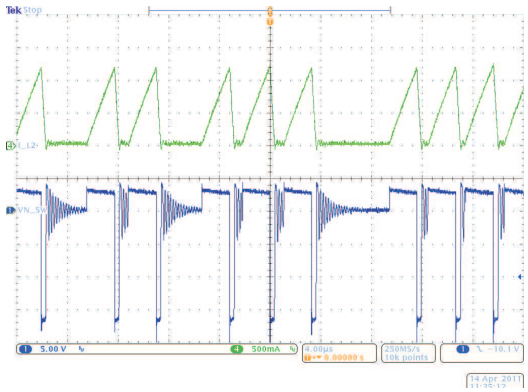
V_{IN} = 3.7 V C_{IN} = 100 µF

Figure 5. Inrush Current



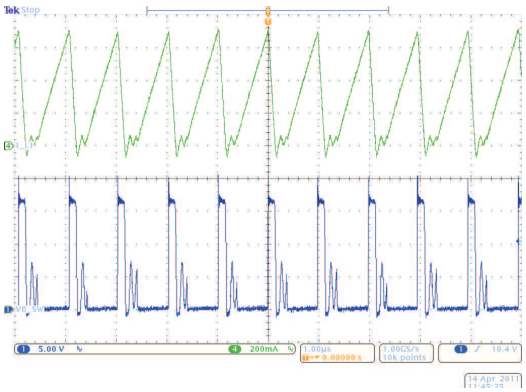
V_{IN} = 5 V C_{IN} = 100 µF

Figure 6. Inrush Current



V_{IN} = 3 V $R_{LOAD, VPOS}$ = 330 Ω $R_{LOAD, VNEG}$ = 330 Ω
No Load on VDDH, VEE

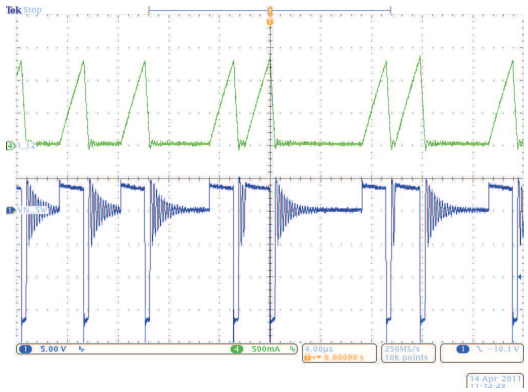
Figure 7. Switching Waveforms, VN



V_{IN} = 3 V $R_{LOAD, VPOS}$ = 330 Ω $R_{LOAD, VNEG}$ = 330 Ω
No Load on VDDH, VEE

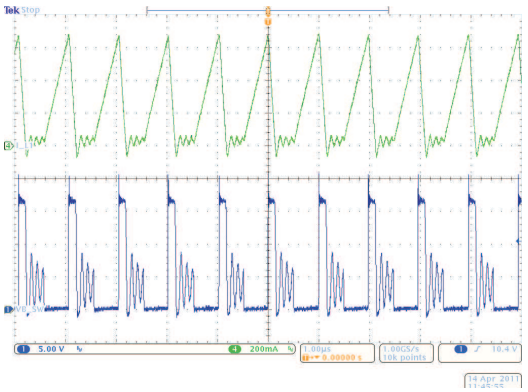
Figure 8. Switching Waveforms, VB

Typical Characteristics (continued)



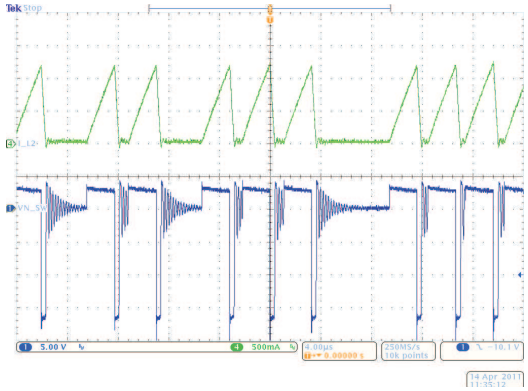
V_{IN} = 3.7 V $R_{LOAD, VPOS}$ = 330 Ω $R_{LOAD, VNEG}$ = 330 Ω
No Load on VDDH, VEE

Figure 9. Switching Waveforms, VN



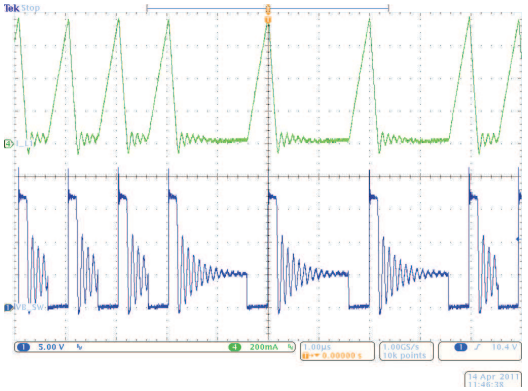
V_{IN} = 3.7 V $R_{LOAD, VPOS}$ = 330 Ω $R_{LOAD, VNEG}$ = 330 Ω
No Load on VDDH, VEE

Figure 10. Switching Waveforms, VB



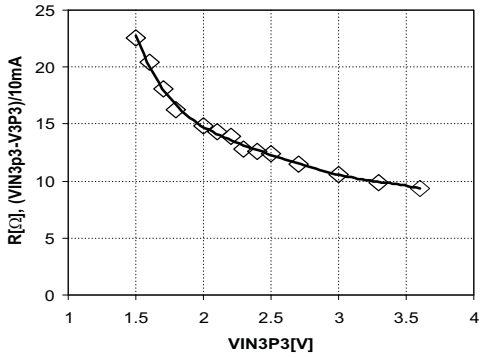
V_{IN} = 5 V $R_{LOAD, VPOS}$ = 330 Ω $R_{LOAD, VNEG}$ = 330 Ω
No Load on VDDH, VEE

Figure 11. Switching Waveforms, VN



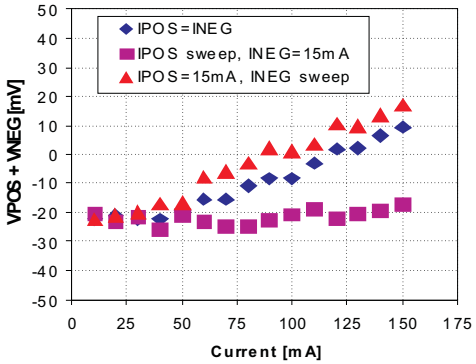
V_{IN} = 5 V $R_{LOAD, VPOS}$ = 330 Ω $R_{LOAD, VNEG}$ = 330 Ω
No Load on VDDH, VEE

Figure 12. Switching Waveforms, VB



V_{IN} = 3.7 V $I_{LOAD, V3p3}$ = 10 mA

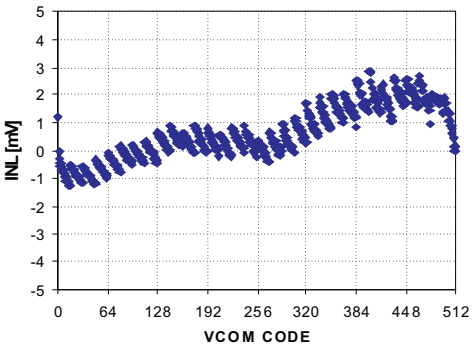
Figure 13. 3p3V Switch Impedance



V_{IN} = 3.7 V

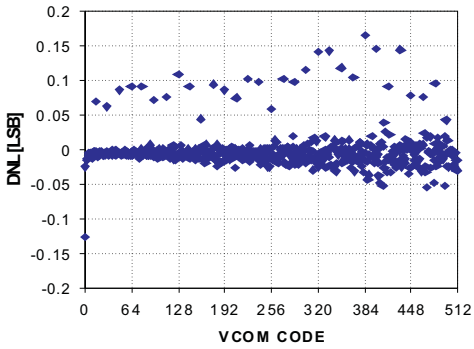
Figure 14. Source Driver Supply Tracking

Typical Characteristics (continued)



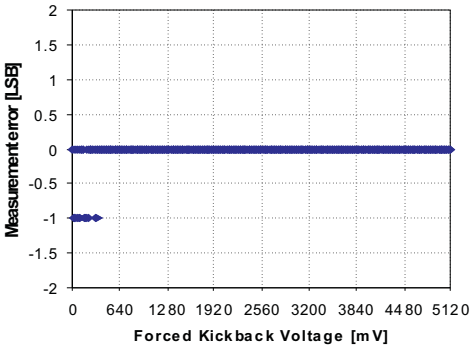
V_{IN} = 3.7 V $R_{LOAD, VCOM}$ = 1 kΩ

Figure 15. VCOM Integrated Non-Linearity



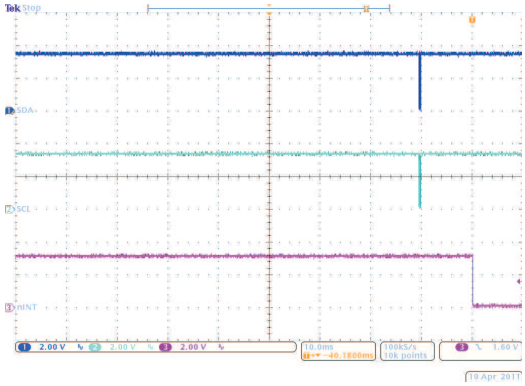
V_{IN} = 3.7 V $R_{LOAD, VCOM}$ = 1 kΩ

Figure 16. VCOM Differential Non-Linearity



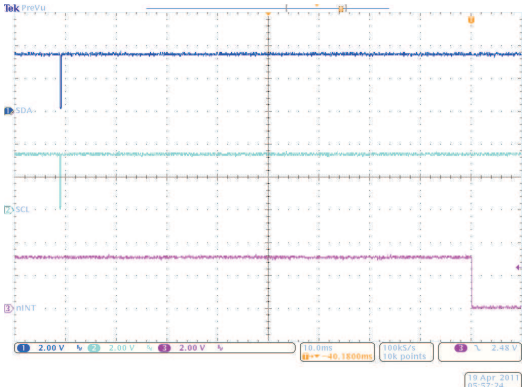
V_{IN} = 3.7 V

Figure 17. Kickback Voltage Measurement Error



V_{IN} = 3.7 V AVG[1:0] = 00 (Single Measurement)
Time from ACQ Bit Set to ACQC Interrupt Received

Figure 18. Kickback Voltage Measurement Timing



V_{IN} = 3.7 V AVG[1:0] = 11 (Eight Measurements)
Time from ACQ Bit Set to ACQC Interrupt Received

Figure 19. Kickback Voltage Measurement Timing

8 Detailed Description

8.1 Overview

The TPS65186 device provides two adjustable LDOs, inverting buck-boost converter, boost converter, thermistor monitoring, and flexible power-up and power-down sequencing. The system can be supplied by a regulated input voltage ranging from 3 V to 6 V. The device is characterized across a –10°C to 85°C temperature range, best suited for personal electronic applications.

The I^2C interface provides comprehensive features for using the TPS65186. All rails can be enabled or disabled. Power-up and power-down sequences can also be programmed through the I^2C interface, as well as thermistor configuration and interrupt configuration. Voltage adjustment can also be controlled by the I^2C interface.

The adjustable LDOs can supply up to 120 mA of current. The default output voltages for each LDO can be adjusted through the I^2C interface. LDO1 (VPOS) and LDO2 (VNEG) track each other in a way that they are of opposite sign but same magnitude. The sum of VLDO1 and VLOD2 is guaranteed to be less than 50 mV.

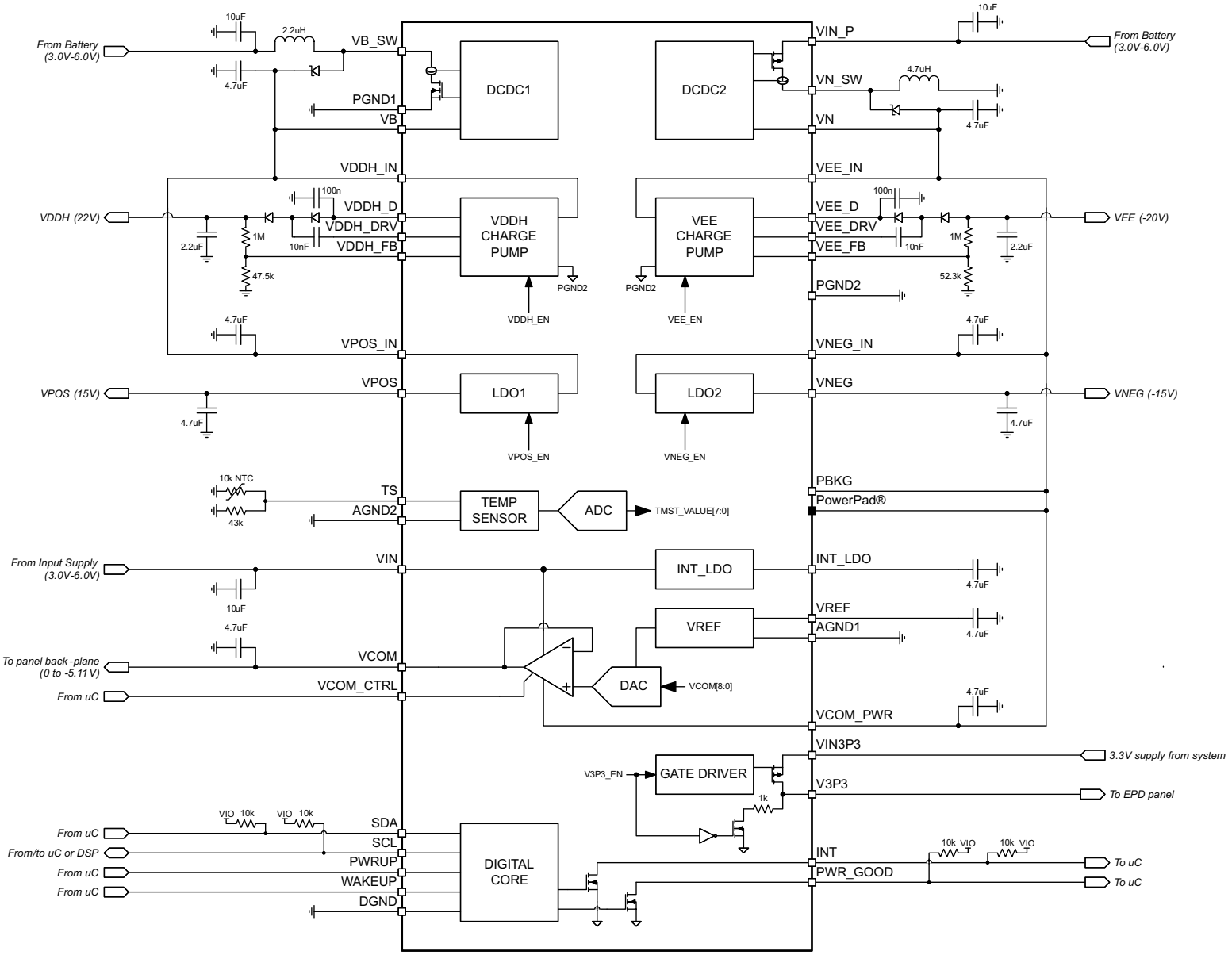
There are two charge pumps: VDDH and VEE 10 mA and 12 mA respectively. These charge pumps boost the DC-DC boost converters ±16-V rails to provide a gate channel supply.

The power good functionality is open-drain output, if any of the four power rails (CP1, CP2, LDO1, LDO2) are not in regulation, encounters a fault, or is disabled the pin is pulled low. PWR_GOOD remains low if one of the rails is not enabled by the host and only after all rails are in regulation PWR_GOOD is released to Hi-Z state (pulled up by external resistor).

The TPS65186 provides circuitry to bias and measure an external NTC to monitor the display panel temperature in a range from –10°C to 85°C with and accuracy of ±1°C from 0°C to 50°C. Temperature measurement are triggered by the controlling host and the last temperature reading is always stored in the TMST_VALUE register. Interrupts are issued when the temperature exceeds the programmable HOT, or drops below the programmable COLD threshold, or when the temperature has changed by more than a user-defined threshold from the baseline value.

This device is offered in a 48-Pin, 0.5-mm Pitch, 7 mm × 7 mm × 0.9 mm (VQFN) RGZ package.

8.2 Functional Block Diagram



8.3 Feature Description

8.3.1 Wake-Up and Power-Up Sequencing

The power-up and power-down order and timing is defined by user register settings. The default settings support the E Ink Vizplex panel and typically do not need to be changed.

In SLEEP mode the TPS65186 is completely turned off, the I^2C registers are reset, and the device does not accept any I^2C transaction. Pull the WAKEUP pin high with the PWRUP pin low and the device enters STANDBY mode that enables the I^2C interface. Write to the UPSEQ0 register to define the order in which the output rails are enabled at power-up and to the UPSEQ1 registers to define the power-up delays between rails. Finally, set the ACTIVE bit in the ENABLE register to 1 to execute the power-up sequence and bring up all power rails. Alternatively, pull the PWRUP pin high (rising edge).

After the ACTIVE bit has been set, the negative boost converter (VN) is powered up first, followed by the positive boost (VB). The positive boost enable is gated by the internal power-good signal of the negative boost. Once VB is in regulation, it issues an internal power-good signal and after delay time UDLY1 has expired, STROBE1 is issued. The rail assigned to STROBE1 will power up next and after its power-good signal has been asserted and delay time UDLY2 has expired, STROBE2 is issued. The sequence continues until STROBE4 has occurred and the last rail has been enabled.

To power down the device, set the STANDBY bit of the ENABLE register to 1 or pull the PWRUP pin low (falling edge) and the TPS65186 will power down in the order defined by DWNSEQx registers. The delay times DDLY2, DDLY3, and DDLY4 are weighted by a factor of DFCTR which allows the user to space out the power down of the rails to avoid crossing during discharge. DFCTR is located in register DWNSEQ1. The positive boost (VB) is shut down together with the last rail at STROBE4. However, the negative boost (VN) remains up and running for another 50 ms. Then VN is powered down and the device enters STANDBY or SLEEP mode, depending on the WAKEUP pin.

If either the ACTIVE bit is set or the PWRUP pin is pulled high while the device is powering down, the power-down sequence (STROBE1-4) is completed first, followed by a power-up sequence. VB and VN may or may not be powered down and depending on the relative timing of STROBE4 to the new power-up event.

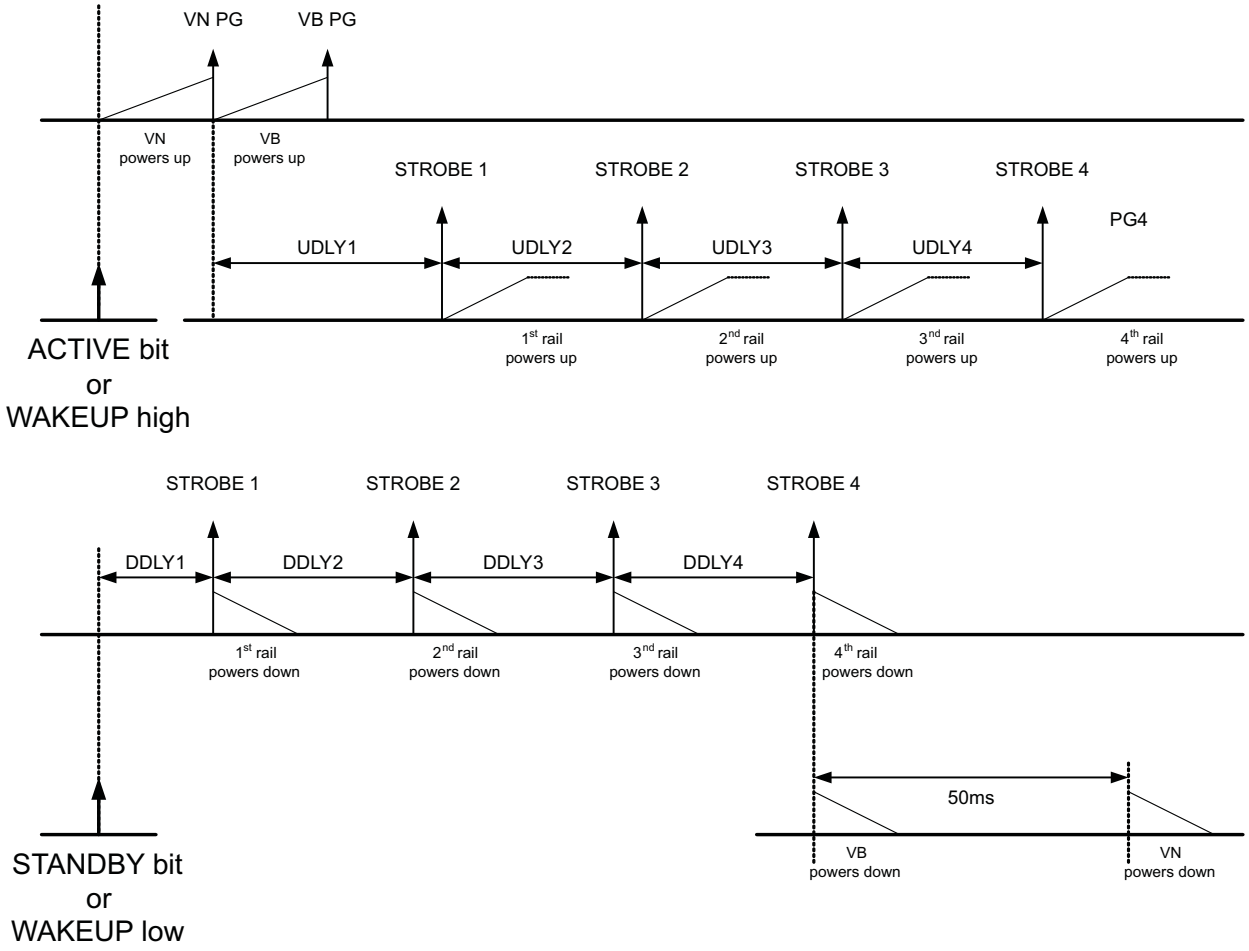
During power-up, if the STANDBY bit is set or the PWRUP pin is pulled low, the power-up sequence is aborted and the power-down sequence starts immediately.

8.3.2 Dependencies Between Rails

Charge pumps, LDOs, and VCOM driver are dependent on the positive and inverting buck-boost converters and several dependencies exist that affect the power-up sequencing. These dependencies are the following:

- Inverting buck-boost (DCDC2) must be in regulation before positive boost (DCDC1) can be enabled. Internally, DCDC1 enable is gated by DCDC2 power good.
- Positive boost (DCDC1) must be in regulation before LDO2 (VNEG) can be enabled. Internally LDO2 enable is gated DCDC1 power good.
- Positive boost (DCDC1) must be in regulation before VCOM can be enabled. Internally VCOM enable is gated by DCDC1 power good.
- Positive boost (DCDC1) must be in regulation before negative charge pump (CP2) can be enabled. Internally CP2 enable is gated by DCDC1 power good.
- Positive boost (DCDC1) must be in regulation before positive charge pump (CP1) can be enabled. Internally CP1 enable is gated by DCDC1 power good.
- LDO2 must be in regulation before LDO1 can be enabled. Internally LDO1 enable is gated by LDO2 power good.

Feature Description (continued)



TOP: Power-up sequence is defined by assigning strobes to individual rails. STROBE1 is the first strobe to occur after ACTIVE bit is set and STROBE4 is the last event in the sequence. Strobes are assigned to rails in UPSEQ0 register and delays between STROBES are defined in UPSEQ1 register.

BOTTOM: Power-down sequence is independent of power-up sequence. Strobes and delay times for power down sequence are set in DWNSEQ0 and DWNSEQ1 register.

Figure 20. Power-Up and Power-Down Sequence

8.3.3 Soft Start

TPS65186 supports soft start for all rails, that is, inrush current is limited during startup of DCDC1, DCDC2, LDO1, LDO2, CP1, and CP2. If DCDC1 or DCDC2 are unable to reach power-good status within 50 ms, the corresponding UV flag is set in the interrupt registers, the interrupt pin is pulled low, and the device enters STANDBY mode. LDO1, LDO2, positive and negative charge pumps also have a 50-ms power-good time-out limit. If either rail is unable to power up within 50 ms after it has been enabled, the corresponding UV flag is set and the interrupt pin is pulled low. However, the device will remain in ACTIVE mode in this case.

8.3.4 VPOS/VNEG Supply Tracking

LDO1 (VPOS) and LDO2 (VNEG) track each other in a way that they are of opposite sign but same magnitude. The sum of VLDO1 and VLOD2 is guaranteed to be less than 50 mV.

Feature Description (continued)

8.3.5 V3P3 Power Switch

The integrated power switch is used to cut the 3.3-V supply to the EPD panel and is controlled through the V3P3_EN pin of the ENABLE register. In SLEEP mode the switch is automatically turned off and its output is discharged to ground. The default power-up state is OFF. To turn the switch ON, set the V3P3_ENbit to 1.

8.3.6 VCOM Adjustment

VCOM is the output of a power-amplifier with an output voltage range of 0 V to –5.11 V, adjustable in 10-mV steps. In a typical application VCOM is connected to the VCOM terminal of the EPD panel and the amplifier is controlled through the VCOM_CTRL pin. With VCOM_CTRL high, the amplifier drives the VCOM pin to the voltage specified by the VCOM1 and VCOM2 register.

For ease of design, the VCOM_CTRL pin may also be tied to the battery or IO supply. In this case, VCOM is enabled with STROBE4 during the power-up sequence and disabled on STROBE1 of the power-down sequence. Therefore VCOM is the last rail to be enabled and the first to be disabled.

8.3.6.1 Kick-Back Voltage Measurement

TPS65186 can perform a voltage measurement on the VCOM pin to deter87/mine the kick-back voltage of the panel. This allows in-system calibration of VCOM. To perform a kick-back voltage measurement, follow these steps:

- Pull the WAKEUP pin and the PWRUP pin high to enable all output rails.
- Set the Hi-Z bit in the VCOM2 register. This puts the VCOM pin in a high-impedance state.
- Drive the panel with the Null waveform. Refer to E-Ink specification for detail.
- Set the ACQ bit in the VCOM2 register to 1. This starts the measurement routine.
- When the measurement is complete, the ACQC (Acquisition Complete) bit in the INT1 register is set and the nINT pin is pulled low.
- The measurement result is stored in the VCOM[8:0] bits of the VCOM1 and VCOM2 register.

The measurement result is not automatically programmed into nonvolatile memory. Changing the power-up default is described in *Storing the VCOM Power-Up Default Value in Memory*.

8.3.6.2 Storing the VCOM Power-Up Default Value in Memory

The power-up default value of VCOM can be user-set and programmed into nonvolatile memory. To do so, write the default value to the VCOM[8:0] bits of the VCOM1 and VCOM2 register, then set the PROG bit in VCOM2 register to 1. First, all power rails are shut down, then the VCOM[8:0] value is committed to nonvolatile memory such that it becomes the new power-up default. Once programming is complete, the PRGC bit in the INT1 register is set and the nINT pin is pulled low. To verify that the new value has been saved properly, first write the VCOM[8:0] bits to 0x000h, then pull the WAKEUP pin low. After the WAKEUP pin is pulled back high, read the VCOM[8:0] bits to verify that the new default value is correct.

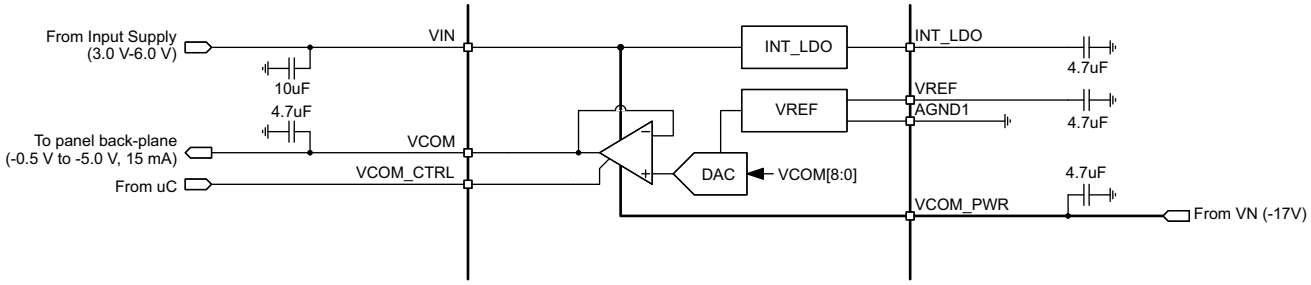


Figure 21. Block Diagram of VCOM Circuit

Feature Description (continued)

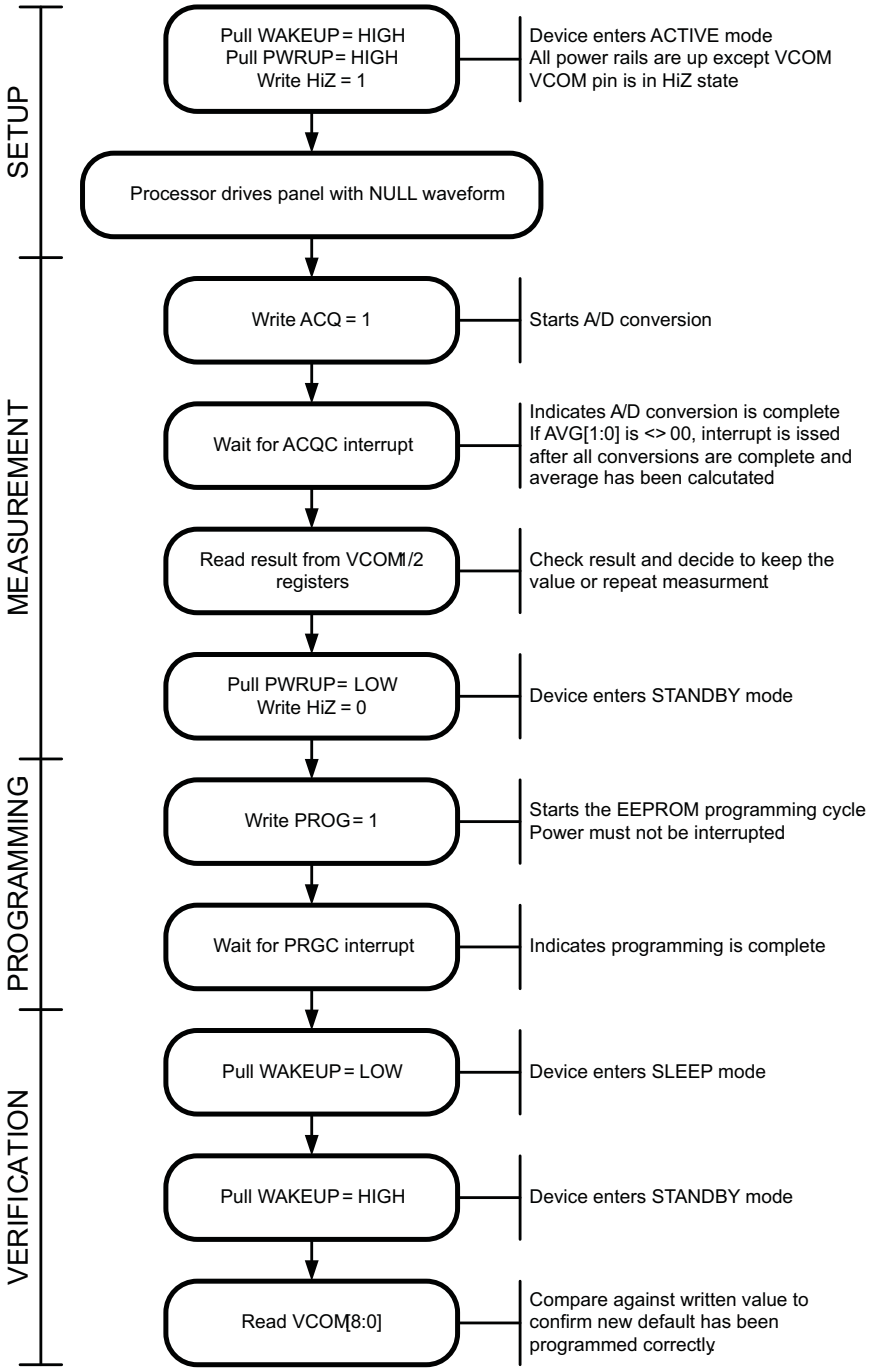


Figure 22. VCOM Calibration Flow

Feature Description (continued)

8.3.7 Fault Handling and Recovery

The TPS65186 monitors input/output voltages and die temperature; the device will take action if operating conditions are outside normal limits when the following are encountered:

- Thermal Shutdown (TSD)
- Positive Boost Undervoltage (VB_UV)
- Inverting Buck-Boost Undervoltage (VN_UV)
- Input Undervoltage Lockout (UVLO)

The TPS65186 shuts down all power rails and enters STANDBY mode. Shutdown follows the order defined by DWNSEQx registers. The exception is VCOM fault witch leads to immediate shutdown of all rails. Once a fault is detected, the PWR_GOOD and nINT pins are pulled low and the corresponding interrupt bit is set in the interrupt register. Power rails cannot be re-enabled unless the interrupt bits have been cleared by reading the INT1 and INT2 register. Alternatively, toggling the WAKEUP pin also resets the interrupt bits. As the PWRUP input is edge sensitive, the host must toggle the PWRUP pin to re-enable the rails through GPIO control, that is, it must bring the PWRUP pin low before asserting it again. Alternatively rails can be re-enbled through the I^2C interface.

Whenever the TPS65186 encounters undervoltage on VNEG (VNEG_UV), VPOS (VPOS_UV), VEE (VEE_UV), or VDDH (VDDH_UV), rails are not shut down but the PWR_GOOD and nINT is pulled low with the corresponding interrupt bit set. The device remains in ACTIVE mode and recovers automatically once the fault has been removed.

8.3.8 Power Good Pin

The power good pin (PWR_GOOD) is an open-drain output that is pulled high (by an external pullup resistor) when all four power rails (CP1, CP2, LDO1, LDO2) are in regulation and is pulled low if any of the rails encounters a fault or is disabled. PWR_GOOD remains low if one of the rails is not enabled by the host and only after all rails are in regulation PWR_GOOD is released to Hi-Z state (pulled up by external resistor).

8.3.9 Interrupt Pin

The interrupt pin (nINT) is an open-drain output that is pulled low whenever one or more of the INT1 or INT2 bits are set. The nINT pin is released (returns to Hi-Z state) and fault bits are cleared once the register with the set bit has been read by the host. If the fault persists, the nINT pin will be pulled low again after a maximum of 32 µs.

Interrupt events can be masked by re-setting the corresponding enable bit in the INT_EN1 and INT_EN2 register, that is, the user can determine which events cause the nINT pin to be pulled low. The status of the enable bits affects the nINT pin only and has no effect on any of the protection and monitoring circuits or the INT1/INT2 bits themselves.

Persisting faults such as thermal shutdown can cause the nINT pin to be pulled low for an extended period of time which can keep the host in a loop trying to resolve the interrupt. If this behavior is not desired, set the corresponding mask bit after receiving the interrupt and keep polling the INT1/INT2 register to see when the fault condition has disappeared. After the fault is resolved, unmask the interrupt bit again.

8.3.10 Panel Temperature Monitoring

The TPS65186 provides circuitry to bias and measure an external Negative Temperature Coefficient Resistor (NTC) to monitor the display panel temperature in a range from –10°C to 85°C with and accuracy of ±1°C from 0°C to 50°C. Temperature measurement must be triggered by the controlling host and the last temperature reading is always stored in the TMST_VALUE register. Interrupts are issued when the temperature exceeds the programmable HOT, or drops below the programmable COLD threshold, or when the temperature has changed by more than a user-defined threshold from the baseline value. Details are explained under *Hot, Cold, and Temperature-Change Interrupts*.

Feature Description (continued)

8.3.10.1 NTC Bias Circuit

Figure 23 shows the block diagram of the NTC bias and measurement circuit. The NTC is biased from an internally generated 2.25-V reference voltage through an integrated 7.307-kΩ bias resistor. A 43-kΩ resistor is connected parallel to the NTC to linearize the temperature response curve. The circuit is designed to work with a nominal 10-kΩ NTC and achieves accuracy of ±1°C from 0°C to 50°C. The voltage drop across the NTC is digitized by a 10-bit SAR ADC and translated into an 8-bit two's complement by digital per Table 1.

Table 1. ADC Output Value vs Temperature

TEMPERATURE	TMST_VALUE[7:0]
< –10°C	1111 0110
–10°C	1111 0110
–9°C	1111 0111
...	...
–2°C	1111 1110
–1°C	1111 1111
0°C	0000 0000
1°C	0000 0001
2°C	0000 0010
...	...
25°C	0001 1001
...	
85°C	0101 0101
> 85°C	0101 0101

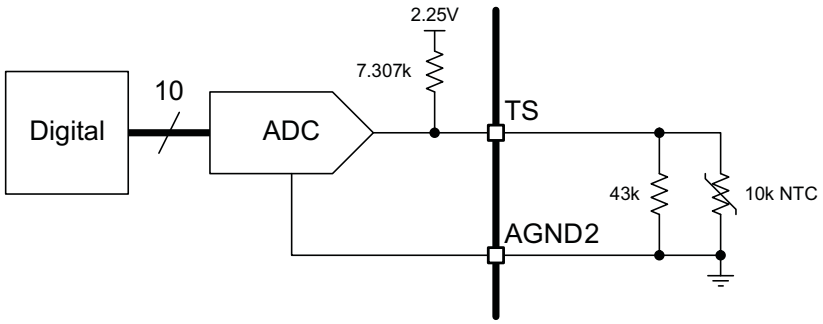


Figure 23. NTC Bias and Measurement Circuit

A temperature measurement is triggered by setting the READ_THERM bit of the TMST1 register to 1.During the A/D conversion the CONV_END bit of the TMST1 register reads 0, otherwise it reads 1. At the end of the A/D conversion the EOC bit in the INT2 register is set and the temperature value is available in the TMST_VALUE register.

8.3.10.2 Hot, Cold, and Temperature-Change Interrupts

Each temperature acquisition is compared against the programmable TMST_HOT and TMST_COLD thresholds and to the baseline temperature, to determine if the display is within allowed operating temperature range and if the temperature has changed by more than a user-defined threshold since the last update. The first temperature reading after the WAKEUP pin has been pulled high automatically becomes the baseline temperature. Any subsequent reading is compared against the baseline temperature. If the difference is equal or greater than the threshold value, an interrupt is issued (DTX bit in register INT1 is set to 1) and the latest value becomes the new baseline. If the difference is less than the threshold value, no action is taken. The threshold value is defined by DT[1:0] bits in the TMST1 register and has a default value of ±2°C. In summary:

- When the temperature is equal or less than the TMST_COLD[3:0] threshold, the TMST_COLD interrupt bit of the INT1 register is set, and the nINT pin is pulled low.
- When the temperature is greater than TMST_COLD but lower then TMST_HOT, no action is taken.
- When the temperature is equal or greater than the TMST_HOT[3:0] threshold, the TMST_HOT interrupt bit of the INT1 register is set, and the nINT pin is pulled low.
- If the last temperature is different from the baseline temperature by ±2°C (default) or more, the DTX interrupt bit of the INT1 register is set. The latest temperature becomes the new baseline temperature. By default the DTX interrupt is disabled, that is, the nINT pin is not pulled low unless the DTX_EN bit was previously set high.
- If the last temperature change is less than ±2°C (default), no action is taken.

8.3.10.3 Typical Application of the Temperature Monitor

In a typical application the temperature monitor and interrupts are used in the following manner:

- After the WAKEUP pin has been pulled high, the Application Processor (AP) writes 0x80h to the TMST1 register (address 0x0Dh). This starts the temperature measurement.
- The AP waits for the EOC interrupt. Alternatively the AP can poll the CONV_END bit in register TMST1. This will notify the AP that the A/D conversion is complete and the new temperature reading is available in the TMST_VALUE register (address (0x00h).
- The AP reads the temperature value from the TMST_VALUE register (address (0x00h).
- If the temperature changes by ±2°C (default) or more from the first reading, the processor is notified by the DTX interrupt. The A/P may or may not decide to select a different set of waveforms to drive the panel.
- If the temperature is outside the allowed operating range of the panel, the processor is notified by the THOT and TCOLD interrupts, respectively. The processor may or may not decide to continue with the page update.
- When an overtemperature or undertemperature has been detected, the AP must reset the TMST_HOT_EN or TMST_COLD_EN bits, respectively, to avoid the nINT pin to be continuously pulled low. The TMST_HOT and TMST_COLD interrupt bits then must be polled continuously, to determine when the panel temperature recovers to the normal operating range. Once the temperature has recovered, the TMST_HOT_EN or TMST_COLD_EN bits must be set to 1 again and normal operation can resume.

8.4 Device Functional Modes

The TPS65186 has three modes of operation, SLEEP, STANDBY, and ACTIVE. SLEEP mode is the lowest-power mode in which all internal circuitry is turned off. In STANDBY, all power rails are shut down but the device is ready to accept commands through the I^2C interface. In ACTIVE mode one or more power rails are enabled.

8.4.1 SLEEP

This is the lowest power mode of operation. All internal circuitry is turned off, registers are reset to default values and the device does not respond to I^2C communications. TPS65186 enters SLEEP mode whenever WAKEUP pin is pulled low.

8.4.2 STANDBY

In STANDBY all internal support circuitry is powered up and the device is ready to accept commands through the I^2C interface but none of the power rails are enabled. The device enters STANDBY mode when the WAKEUP pin is pulled high and either the PWRUP pin is pulled low or the STANDBY bit is set. The device also enters STANDBY mode if input undervoltage lockout (UVLO), positive boost undervoltage (VB_UV), or inverting buck-boost undervoltage (VN_UV) is detected, thermal shutdown occurs, or the PROG bit is set (see Figure 22)

8.4.3 ACTIVE

The device is in ACTIVE mode when any of the output rails are enabled and no fault condition is present. This is the normal mode of operation while the device is powered up.

8.4.4 Mode Transitions

8.4.4.1 SLEEP → ACTIVE

WAKEUP pin is pulled high with PWRUP pin high. Rails come up in the order defined by the UPSEQx registers (OK to tie WAKEUP and PWRUP pin together).

8.4.4.2 SLEEP → STANDBY

WAKEUP pin is pulled high with PWRUP pin low. Rails will remain powered down.

8.4.4.3 STANDBY → ACTIVE

WAKEUP pin is high and PWRRUP pin is pulled high (rising edge) or the ACTIVE bit is set. Output rails will power up in the order defined by the UPSEQx registers.

8.4.4.4 ACTIVE → STANDBY

WAKEUP pin is high and STANDBY bit is set or PWRUP pin is pulled low (falling edge). Rails are shut down in the order defined by DWNSEQx registers. Device also enters STANDBY in the event of thermal shutdown (TSD), undervoltage lockout (UVLO), positive boost or inverting buck-boost undervoltage (UV), VCOM fault (VCOMF), or when the PROG bit is set (see Figure 22).

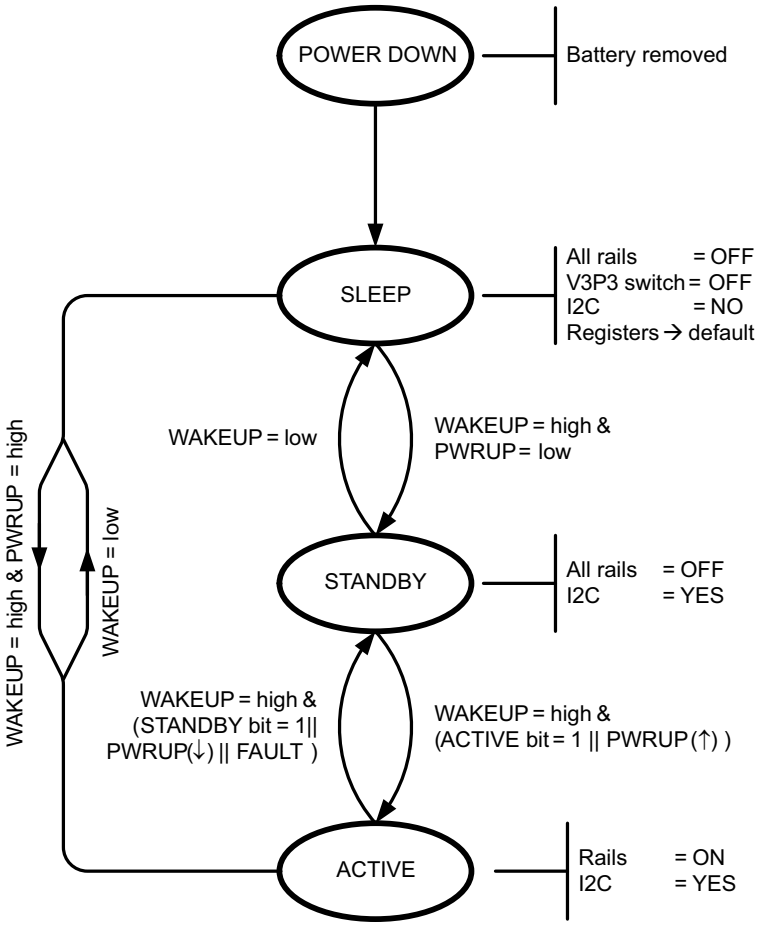
8.4.4.5 STANDBY → SLEEP

WAKEUP pin is pulled low while none of the output rails are enabled.

8.4.4.6 ACTIVE → SLEEP

WAKEUP pin is pulled low while at least one output rail is enabled. Rails are shut down in the order defined by DWNSEQx registers.

Device Functional Modes (continued)



NOTES:

||, & = logic OR, and AND.

(↑), (↓) = rising edge, falling edge

UVLO = Undervoltage Lockout

TSD = Thermal Shutdown

UV = Undervoltage

FAULT = UVLO || TSD || BOOST UV || VCOM fault

Figure 24. Global State Diagram

8.5 Programming

8.5.1 I²C Bus Operation

The TPS65186 hosts a slave I²C interface that supports data rates up to 400 kbit/s and auto-increment addressing and is compliant to I²C standard 3.0.

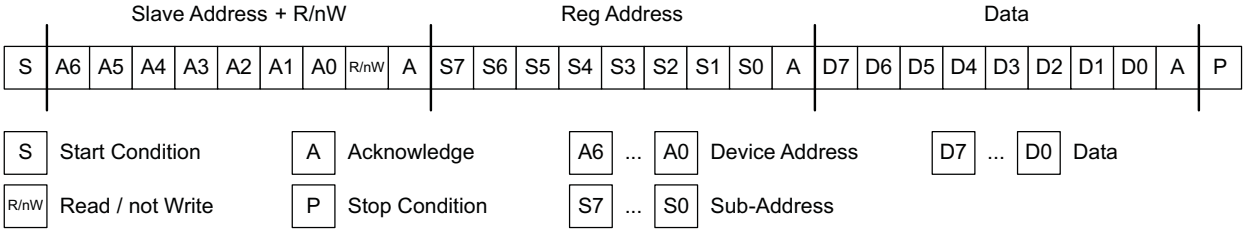


Figure 25. Subaddress in I²C Transmission

The I²C Bus is a communications link between a controller and a series of slave terminals. The link is established using a two-wire bus consisting of a serial clock signal (SCL) and a serial data signal (SDA). The serial clock is sourced from the controller in all cases where the serial data line is bidirectional for data communication between the controller and the slave terminals. Each device has an open drain output to transmit data on the serial data line. An external pullup resistor must be placed on the serial data line to pull the drain output high during data transmission.

Data transmission is initiated with a start bit from the controller as shown in Figure 27. The start condition is recognized when the SDA line transitions from high to low during the high portion of the SCL signal. Upon reception of a start bit, the device will receive serial data on the SDA input and check for valid address and control information. If the appropriate slave address bits are set for the device, then the device will issue an acknowledge pulse and prepare to receive the register address. Depending on the R/nW bit, the next byte received from the master is written to the addressed register (R/nW = 0) or the device responds with 8-bit data from the register (R/nW = 1). Data transmission is completed by either the reception of a stop condition or the reception of the data word sent to the device. A stop condition is recognized as a low to high transition of the SDA input during the high portion of the SCL signal. All other transitions of the SDA line must occur during the low portion of the SCL signal. An acknowledge is issued after the reception of valid address, sub-address and data words. The I²C interfaces will auto-sequence through register addresses, so that multiple data words can be sent for a given I²C transmission. See Figure 26 and Figure 27 for details.

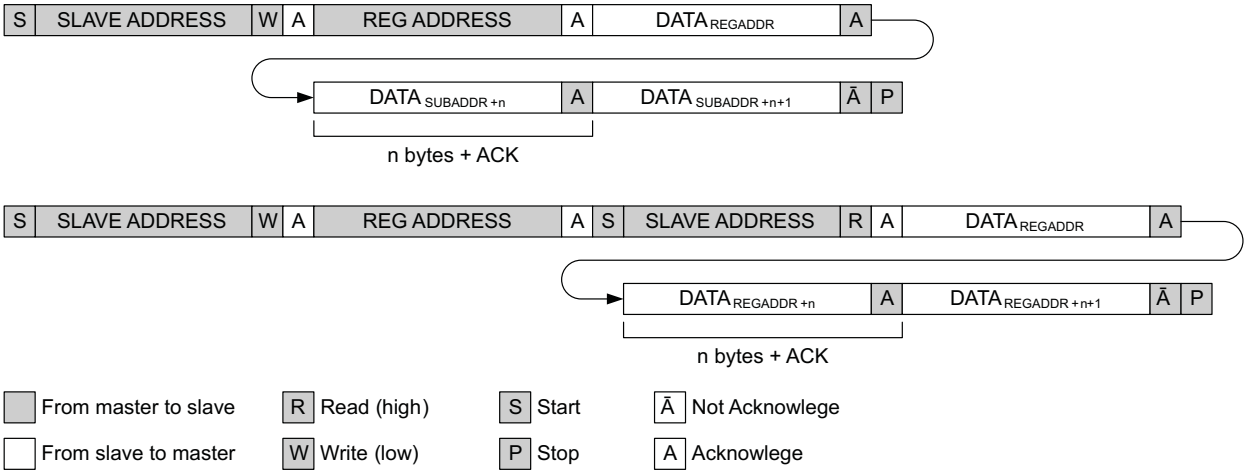


Figure 26. I²C Data Protocol

Programming (continued)

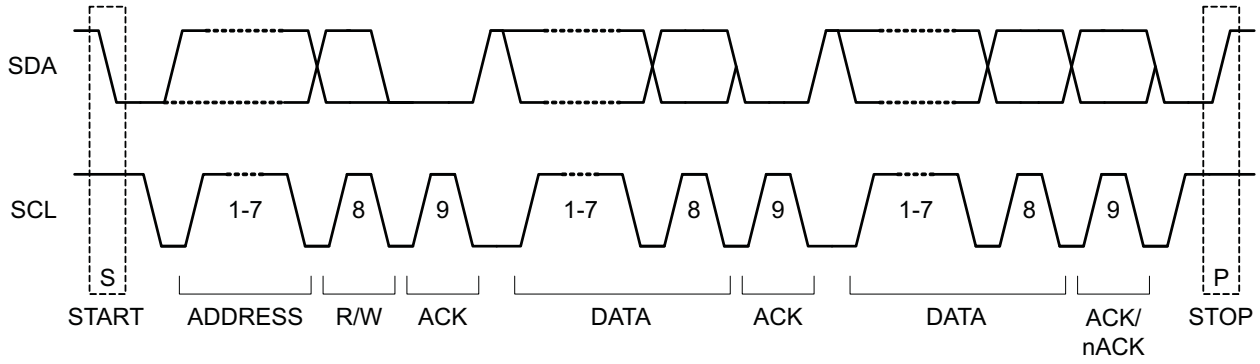


Figure 27. I²C Start/Stop/Acknowledge Protocol

8.6 Register Maps

REGISTER	ADDRESS (HEX)	NAME	DESCRIPTION
0	0x00	TMST_VALUE	Thermistor value read by ADC
1	0x01	ENABLE	Enable/disable bits for regulators
2	0x02	VADJ	VPOS/VNEG voltage adjustment
3	0x03	VCOM1	Voltage settings for VCOM
4	0x04	VCOM2	Voltage settings for VCOM + control
5	0x05	INT_EN1	Interrupt enable group1
6	0x06	INT_EN2	Interrupt enable group2
7	0x07	INT1	Interrupt group1
8	0x08	INT2	Interrupt group2
9	0x09	UPSEQ0	Power-up strobe assignment
10	0x0A	UPSEQ1	Power-up sequence delay times
11	0x0B	DWNSEQ0	Power-down strobe assignment
12	0x0C	DWNSEQ1	Power-down sequence delay times
13	0x0D	TMST1	Thermistor configuration
14	0x0E	TMST2	Thermistor hot temp set
15	0x0F	PG	Power good status each rails
16	0x10	REVID	Device revision ID information

8.6.1 Thermistor Readout (TMST_VALUE)

Address – 0x00h

DATA BIT	D7	D6	D5	D4	D3	D2	D1	D0
FIELD NAME	TMST_VALUE[7:0]							
READ/WRITE	R	R	R	R	R	R	R	R
RESET VALUE	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A

FIELD NAME	BIT DEFINITION
TMST_VALUE[7:0]	Temperature read-out 1111 0110 – < -10°C 1111 0110 – -10°C 1111 0111 – -9°C ... 1111 1110 – -2°C 1111 1111 – -1 °C 0000 0000 – 0 °C 0000 0001 – 1°C 0000 0010 – 2°C ... 0001 1001 – 25°C ... 0101 0101 – 85°C 0101 0101 – > 85°C

8.6.2 Enable (ENABLE)

Address – 0x01h

DATA BIT	D7	D6	D5	D4	D3	D2	D1	D0
FIELD NAME	ACTIVE	STANDBY	V3P3_EN	VCOM_EN	VDDH_EN	VPOS_EN	VEE_EN	VNEG_EN
READ/WRITE	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
RESET VALUE	0	0	0	0	0	0	0	0

FIELD NAME	BIT DEFINITION(1)
ACTIVE	STANDBY to ACTIVE transition bit 1 – Transition from STANDBY to ACTIVE mode. Rails power up as defined by UPSEQx registers 0 – no effect NOTE: After transition bit is cleared automatically
STANDBY	STANDBY to ACTIVE transition bit 1 – Transition from STANDBY to ACTIVE mode. Rails power up as defined by DWNSEQx registers 0 – no effect NOTE: After transition bit is cleared automatically. STANDBY bit has priority over AVTIVE.
V3P3_EN	VIN3P3 to V3P3 switch enable 1 – switch is ON 0 – switch is OFF
VCOM_EN	VCOM buffer enable 1 – enabled 0 – disabled
VDDH_EN	VDDH charge pump enable 1 – enabled 0 – disabled
VPOS_EN	VPOS LDO regulator enable 1 – enabled 0 – disabled NOTE: VPOS cannot be enabled before VNEG is enabled.
VEE_EN	VEE charge pump enable 1 – enabled 0 – disabled
VNEG_EN	VNEG LDO regulator enable 1 – enabled 0 – disabled NOTE: When VNEG is disabled VPOS will also be disabled.

(1) Enable bits always reflect actual status of the corresponding rail.

8.6.3 Voltage Adjustment Register (VADJ)

Address – 0x02h

DATA BIT	D7	D6	D5	D4	D3	D2	D1	D0
FIELD NAME	not used	not used	not used	not used	not used	VSET[2:0]		
READ/WRITE	R/W	R/W	R/W	R/W	R	R/W	R/W	R/W
RESET VALUE	0	0	1	0	0	0^{E2}	1^{E2}	1^{E2}

FIELD NAME	BIT DEFINITION
not used	N/A
not used	N/A
not used	N/A
not used	N/A
not used	N/A
VSET[2:0]	VPOS and VNEG voltage setting 000 - not valid 001 - not valid 010 - not valid 011 - ±15.000 V 100 - ±14.750 V 101 - ±14.500 V 110 - ±14.250 V 111 - reserved

8.6.4 VCOM 1 (VCOM1)

Address – 0x03h

DATA BIT	D7	D6	D5	D4	D3	D2	D1	D0
FIELD NAME	VCOM [7:0]							
READ/WRITE	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
RESET VALUE	0^{E2}	1^{E2}	1^{E2}	1^{E2}	1	1	0	1

FIELD NAME	BIT DEFINITION
VCOM[7:0]	VCOM voltage, least significant byte. See *VCOM 2 (VCOM2)* for details.

8.6.5 VCOM 2 (VCOM2)

Address – 0x04h

DATA BIT	D7	D6	D5	D4	D3	D2	D1	D0
FIELD NAME	ACQ	PROG	HiZ	AVG[1:0]		not used	not used	VCOM[8]
READ/WRITE	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
RESET VALUE	0	0	0	0	0	1	0	0[E2]

FIELD NAME	BIT DEFINITION
ACQ	Kick-back voltage acquisition bit 1 – starts kick-back voltage measurement routine 0 – no effect NOTE: After measurement is complete bit is cleared automatically and measurement result is reflected in VCOM[8:0] bits.
PROG	VCOM programming bit 1 – VCOM[8:0] value is committed to nonvolatile memory and becomes new power-up default 0 – no effect NOTE: After programming bit is cleared automatically and TPS65186 will enter STANDBY mode.
HiZ	VCOM HiZ bit 1 – VCOM pin is placed into hi-impedance state to allow VCOM measurement 0 – VCOM amplifier is connected to VCOM pin
AVG[1:0]	Number of acquisitions that is averaged to a single kick-back voltage measurement 00 – 1x 01 – 2x 10 – 4x 11 – 8x NOTE: When the ACQ bit is set, the state machine repeat the A/D conversion of the kick-back voltage AVD[1:0] times and returns a single, averaged, value to VCOM[8:0]
not used	N/A
not used	N/A
VCOM[8:0]	VCOM voltage adjustment VCOM = VCOM[8:0] x -10 mV in the range from 0 mV to –5.110 V 0x000h – 0 0000 0000 – –0 mV 0x001h – 0 0000 0001 – –10 mV 0x002h – 0 0000 0010 – –20 mV ... 0x07Dh - 0 0111 1101 – –1250 mV ... 0x1FEh – 1 1111 1110 – –5100 mV 0x1FFh – 1 1111 1111 – –5110 mV

8.6.6 Interrupt Enable 1 (INT_EN1)

Address – 0x05h

DATA BIT	D7	D6	D5	D4	D3	D2	D1	D0
FIELD NAME	DTX_EN	TSD_EN	HOT_EN	TMST_HOT_EN	TMST_COLD_EN	UVLO_EN	ACQC_EN	PRGC_EN
READ/WRITE	R	R/W	R/W	R/W	R/W	R/W	R	R
RESET VALUE	0	1	1	1	1	1	1	1

FIELD NAME	BIT DEFINITION(1)
DTX_EN	Panel temperature-change interrupt enable 1 – enabled 0 – disabled
TSD_EN	Thermal shutdown interrupt enable 1 – enabled 0 – disabled
HOT_EN	Thermal shutdown early warning enable 1 – enabled 0 – disabled
TMST_HOT_EN	Thermistor hot interrupt enable 1 – enabled 0 – disabled
TMST_COLD_EN	Thermistor cold interrupt enable 1 – enabled 0 – disabled
UVLO_EN	VIN undervoltage detect interrupt enable 1 – enabled 0 – disabled
ACQC_EN	VCOM acquisition complete interrupt enable 1 – enabled 0 – disabled
PRGC_EN	VCOM programming complete interrupt enable 1 – enabled 0 – disabled

(1) Enabled means nINT pin is pulled low when interrupt occurs.
Disabled means nINT pin is not pulled low when interrupt occurs.

8.6.7 Interrupt Enable 2 (INT_EN2)

Address – 0x06h

DATA BIT	D7	D6	D5	D4	D3	D2	D1	D0
FIELD NAME	VBUVEN	VDDHUVEN	VNUV_EN	VPOSUVEN	VEEUVEN	VCOMFEN	VNEGUVEN	EOCEN
READ/WRITE	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
RESET VALUE	1	1	1	1	1	1	1	1

FIELD NAME	BIT DEFINITION(1)
VBUVEN	Positive boost converter undervoltage detect interrupt enable 1 – enabled 0 – disabled
VDDHUVEN	VDDH undervoltage detect interrupt enable 1 – enabled 0 – disabled
VNUVEN	Inverting buck-boost converter undervoltage detect interrupt enable 1 – enabled 0 – disabled
VPOSUVEN	VPOS undervoltage detect interrupt enable 1 – enabled 0 – disabled
VEEUVEN	VEE undervoltage detect interrupt enable 1 – enabled 0 – disabled
VCOMFEN	VCOM FAULT interrupt enable 1 – enabled 0 – disabled
VNEGUVEN	VNEG undervoltage detect interrupt enable 1 – enabled 0 – disabled
EOCEN	Temperature ADC end of conversion interrupt enable 1 – enabled 0 – disabled

(1) Enabled means nINT pin is pulled low when interrupt occurs.
Disabled means nINT pin is not pulled low when interrupt occurs.

8.6.8 Interrupt 1 (INT1)

Address – 0x07h

DATA BIT	D7	D6	D5	D4	D3	D2	D1	D0
FIELD NAME	DTX	TSD	HOT	TMST_HOT	TMST_COLD	UVLO	ACQC	PRGC
READ/WRITE	R	R	R	R	R	R	R	R
RESET VALUE	0	N/A	N/A	N/A	N/A	N/A	0	0

FIELD NAME	BIT DEFINITION
DTX	Panel temperature-change interrupt 1 – temperature has changed by 3 deg or more over previous reading 0 – no significance
TSD	Thermal shutdown interrupt 1 – chip is in overtemperature shutdown 0 – no fault
HOT	Thermal shutdown early warning 1 – chip is approaching overtemperature shutdown 0 – no fault
TMST_HOT	Thermistor hot interrupt 1 – thermistor temperature is equal or greater than TMST_HOT threshold 0 – no fault
TMST_COLD	Thermistor cold interrupt 1 – thermistor temperature is equal or less than TMST_COLD threshold 0 – no fault
UVLO	VIN undervoltage detect interrupt 1 – input voltage is below UVLO threshold 0 – no fault
ACQC	VCOM acquisition complete 1 – VCOM measurement is compete 0 – no significance
PRGC	VCOM programming complete 1 – VCOM programming is complete 0 – no significance

8.6.9 Interrupt 2 (INT2)

Address – 0x08h

DATA BIT	D7	D6	D5	D4	D3	D2	D1	D0
FIELD NAME	VB_UV	VDDH_UV	VN_UV	VPOS_UV	VEE_UV	VCOMF	VNEG_UV	EOC
READ/WRITE	R	R	R	R	R	R	R	R
RESET VALUE	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A

FIELD NAME	BIT DEFINITION
VB_UV	Positive boost converter undervoltage detect interrupt 1 – under-voltage on DCDC1 detected 0 – no fault
VDDH_UV	VDDH undervoltage detect interrupt 1 – undervoltage on VDDH charge pump detected 0 – no fault
VN_UV	Inverting buck-boost converter undervoltage detect interrupt 1 – undervoltage on DCDC2 detected 0 – no fault
VPOS_UV	VPOS undervoltage detect interrupt 1 – undervoltage on LDO1(VPOS) detected 0 – no fault
VEE_UV	VEE undervoltage detect interrupt 1 – undervoltage on VEE charge pump detected 0 – no fault
VCOMF	VCOM fault detection 1 – fault on VCOM detected (VCOM is outside normal operating range) 0 – no fault
VNEG_UV	VNEG undervoltage detect interrupt 1 – undervoltage on LDO2(VNEG) detected 0 – no fault
EOC	ADC end of conversion interrupt 1 – ADC conversion is complete (temperature acquisition is complete) 0 – no significance

8.6.10 Power Up Sequence Register 0 (UPSEQ0)

Address – 0x09h

DATA BIT	D7	D6	D5	D4	D3	D2	D1	D0
FIELD NAME	VDDH_UP[1:0]		VPOS_UP[1:0]		VEE_UP[1:0]		VNEG_UP[1:0]	
READ/WRITE	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
RESET VALUE	1^{E2}	1^{E2}	1^{E2}	0^{E2}	0^{E2}	1^{E2}	0^{E2}	0^{E2}

FIELD NAME	BIT DEFINITION
VDDH_UP[1:0]	VDDH power-up order 00 – power up on STROBE1 01 – power up on STROBE2 10 – power up on STROBE3 11 – power up on STROBE4
VPOS_UP[1:0]	VPOS power-up order 00 – power up on STROBE1 01 – power up on STROBE2 10 – power up on STROBE3 11 – power up on STROBE4
VEE_UP[1:0]	VEE power-up order 00 – power up on STROBE1 01 – power up on STROBE2 10 – power up on STROBE3 11 – power up on STROBE4
VNEG_UP[1:0]	VNEG power-up order 00 – power up on STROBE1 01 – power up on STROBE2 10 – power up on STROBE3 11 – power up on STROBE4

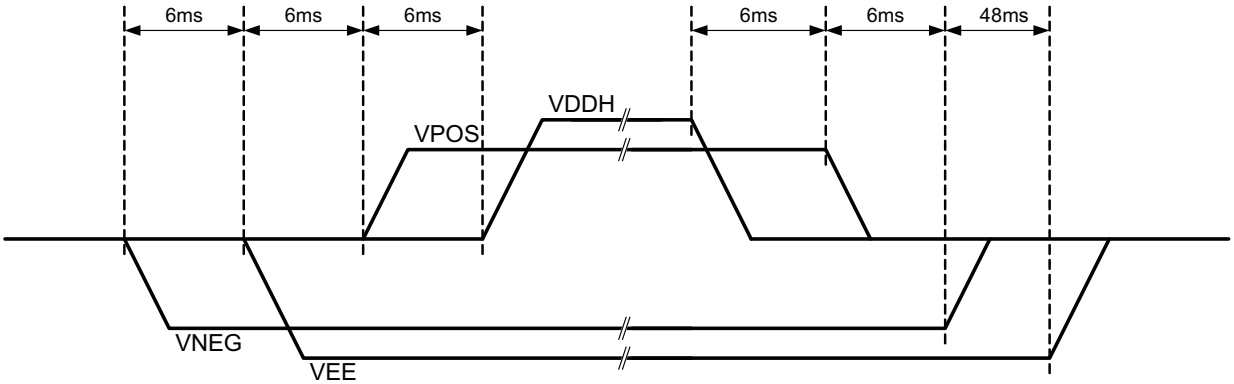


Figure 28. Default Power-Up/Power-Down Sequence

8.6.11 Power Up Sequence Register 1 (UPSEQ1)

Address – 0x0Ah

DATA BIT	D7	D6	D5	D4	D3	D2	D1	D0
FIELD NAME	UDLY4[1:0]		UDLY3[1:0]		UDLY2[1:0]		UDLY1[1:0]	
READ/WRITE	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
RESET VALUE	0^{E2}	1^{E2}	0^{E2}	1^{E2}	0^{E2}	1^{E2}	0^{E2}	1^{E2}

FIELD NAME	BIT DEFINITION
UDLY4[1:0]	DLY4 delay time set; defines the delay time from STROBE3 to STROBE4 during power up. 00 – 3 ms 01 – 6 ms 10 – 9 ms 11 – 12 ms
UDLY3[1:0]	DLY3 delay time set; defines the delay time from STROBE2 to STROBE3 during power up. 00 – 3 ms 01 – 6 ms 10 – 9 ms 11 – 12 ms
UDLY2[1:0]	DLY2 delay time set; defines the delay time from STROBE1 to STROBE2 during power up. 00 – 3 ms 01 – 6 ms 10 – 9 ms 11 – 12 ms
UDLY1[1:0]	DLY1 delay time set; defines the delay time from VN_PG high to STROBE1 during power up. 00 – 3 ms 01 – 6 ms 10 – 9 ms 11 – 12 ms

8.6.12 Power Down Sequence Register 0 (DWNSEQ0)

Address – 0x0Bh

DATA BIT	D7	D6	D5	D4	D3	D2	D1	D0
FIELD NAME	VDDH_DWN[1:0]		VPOS_DWN[1:0]		VEE_DWN[1:0]		VNEG_DWN[1:0]	
READ/WRITE	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
RESET VALUE	0^{E2}	0^{E2}	0^{E2}	1^{E2}	1^{E2}	1^{E2}	1^{E2}	0^{E2}

FIELD NAME	BIT DEFINITION
VDDH_DWN[1:0]	VDDH power-down order 00 – power down on STROBE1 01 – power down on STROBE2 10 – power down on STROBE3 11 – power down on STROBE4
VPOS_DWN[1:0]	VPOS power-down order 00 – power down on STROBE1 01 – power down on STROBE2 10 – power down on STROBE3 11 – power down on STROBE4
VEE_DWN[1:0]	VEE power-down order 00 – power down on STROBE1 01 – power down on STROBE2 10 – power down on STROBE3 11 – power down on STROBE4
VNEG_DWN[1:0]	VNEG power-down order 00 – power down on STROBE1 01 – power down on STROBE2 10 – power down on STROBE3 11 – power down on STROBE4

8.6.13 Power Down Sequence Register 1 (DWNSEQ1)

Address – 0x0Ch

DATA BIT	D7	D6	D5	D4	D3	D2	D1	D0
FIELD NAME	DDLY4[1:0]		DDLY3[1:0]		DDLY2[1:0]		DDLY1	DFCTR
READ/WRITE	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
RESET VALUE	1^{E2}	1^{E2}	1^{E2}	0^{E2}	0^{E2}	0^{E2}	0^{E2}	0^{E2}

FIELD NAME	BIT DEFINITION
DDLY4[1:0]	DLY4 delay time set; defines the delay time from STROBE3 to STROBE4 during power down. 00 – 6 ms 01 – 12 ms 10 – 24 ms 11 – 48 ms
DDLY3[1:0]	DLY3 delay time set; defines the delay time from STROBE2 to STROBE3 during power down. 00 – 6 ms 01 – 12 ms 10 – 24 ms 11 – 4 8ms
DDLY2[1:0]	DLY2 delay time set; defines the delay time from STROBE1 to STROBE2 during power down. 00 – 6 ms 01 – 12 ms 10 – 24 ms 11 – 48 ms
DDLY1	DLY2 delay time set; defines the delay time from WAKEUP low to STROBE1 during power down. 0 – 3 ms 1 – 6 ms
DFCTR	At power-down delay time DLY2[1:0], DLY3[1:0], DLY4[1:0] are multiplied with DFCTR[1:0] 0 – 1× 1 – 16×

8.6.14 Thermistor Register 1 (TMST1)

Address – 0x0Dh

DATA BIT	D7	D6	D5	D4	D3	D2	D1	D0
FIELD NAME	READ_THERM	not used	CONV_END	not used	not used	not used	DT[1:0]	
READ/WRITE	R/W	R/W	R	R/W	R/W	R/W	R/W	R/W
RESET VALUE	0	0	1	0	0	0	0	0

FIELD NAME	BIT DEFINITION
READ_THERM	Read thermistor value 1 – initiates temperature acquisition 0 – no effect NOTE: Bit is self-cleared after acquisition is completed
not used	N/A
CONV_END	ADC conversion done flag 1 – conversion is finished 0 – conversion is not finished
not used	N/A
not used	N/A
DT[1:0]	Panel temperature-change interrupt threshold 00 – 2°C 01 – 3°C 10 – 4°C 11 – 5°C DTX interrupt is issued when difference between most recent temperature reading and baseline temperature is equal to or greater than threshold value. See *Hot, Cold, and Temperature-Change Interrupts* for details.

8.6.15 Thermistor Register 2 (TMST2)

Address – 0x0Eh

DATA BIT	D7	D6	D5	D4	D3	D2	D1	D0
FIELD NAME	TMST_COLD[3:0]				TMST_HOT[3:0]			
READ/WRITE	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
RESET VALUE	0	1	1	1	1	0	0	0

FIELD NAME	BIT DEFINITION
TMST_COLD [3:0]	Thermistor COLD threshold 0000 – -7°C 0001 – -6°C 0010 – -5°C 0011 – -4°C 0100 – -3°C 0101 – -2°C 0110 – -1°C 0111 – 0°C 1000 – 1°C 1001 – 2°C 1010 – 3°C 1011 – 4°C 1100 – 5°C 1101 – 6°C 1110 – 7°C 1111 – 8°C NOTE: An interrupt is issued when thermistor temperature is equal or less than COLD threshold
TMST_HOT [3:0]	Thermistor HOT threshold 0000 – 42°C 0001 – 43°C 0010 – 44°C 0011 – 45°C 0100 – 46°C 0101 – 47°C 0110 – 48°C 0111 – 49°C 1000 – 50°C 1001 – 51°C 1010 – 52°C 1011 – 53°C 1100 – 54°C 1101 – 55°C 1110 – 56°C 1111 – 57°C NOTE: An interrupt is issued when thermistor temperature is equal or greater than HOT threshold

8.6.16 Power Good Status (PG)

Address – 0x0Fh

DATA BIT	D7	D6	D5	D4	D3	D2	D1	D0
FIELD NAME	VB_PG	VDDH_PG	VN_PG	VPOS_PG	VEE_PG	not used	VNEG_PG	not used
READ/WRITE	R	R	R	R	R	R	R	R
RESET VALUE	0	0	0	0	0	0	0	0

FIELD NAME	BIT DEFINITION(1)
VB_PG	Positive boost converter power good 1 – DCDC1 is in regulation 0 – DCDC1 is not in regulation or turned off
VDDH_PG	VDDH power good 1 – VDDH charge pump is in regulation 0 – VDDH charge pump is not in regulation or turned off
VN_PG	Inverting buck-boost power good 1 – DCDC2 is in regulation 0 – DCDC2 is not in regulation or turned off
VPOS_PG	VPOS power good 1 – LDO1(VPOS) is in regulation 0 – LDO1(VPOS) is not in regulation or turned off
VEE_PG	VEE power good 1 – VEE charge pump is in regulation 0 – VEE charge pump is not in regulation or turned off
not used	N/A
VNEG_PG	VNEG power good 1 – LDO2(VNEG) is in regulation 0 – LDO2(VNEG) is not in regulation or turned off
not used	N/A

(1) PG pin is pulled hi (Hi-Z state) when VDDH_PG = VPOS_PG = VEE_PG = VNEG_PG = 1

8.6.17 Revision and Version Control (REVID)

Address – 0x10h

DATA BIT	D7	D6	D5	D4	D3	D2	D1	D0
FIELD NAME	REVID[7:0]							
READ/WRITE	R	R	R	R	R	R	R	R
RESET VALUE	0	1	0	0	0^{E2}	1^{E2}	0^{E2}	1^{E2}

FIELD NAME	BIT DEFINITION
REVID[7:6]	MJREV
REVID[5:4]	MNREV
REVID[3:0]	VERSION
REVID [7:0]	0100 0101 - TPS65186 1p0 0101 0101 – TPS65186 1p1 0110 0101 – TPS65186 1p2

9 Application and Implementation

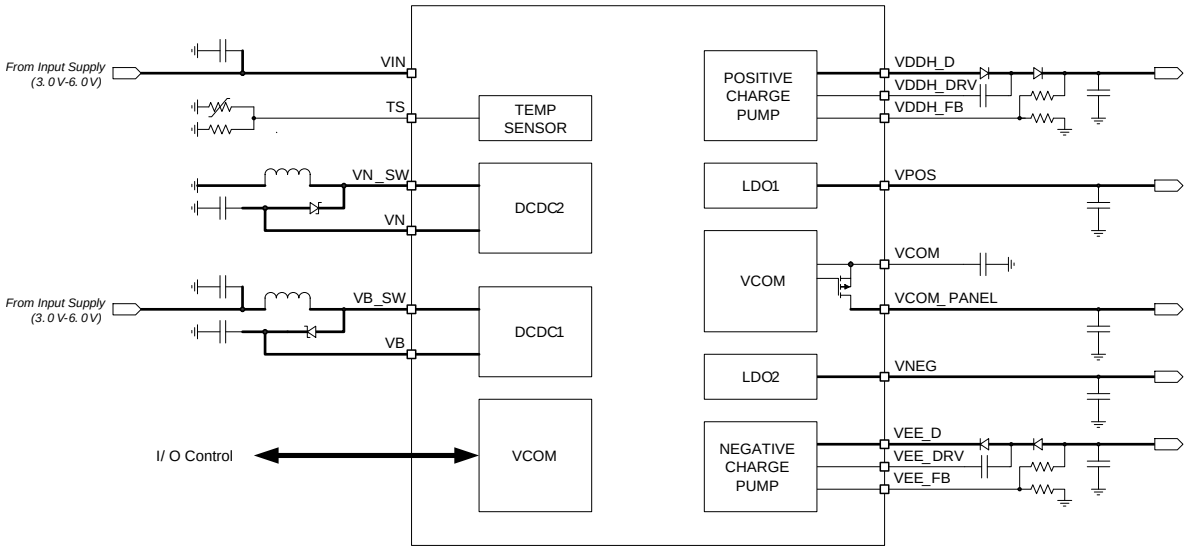
NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

The TPS65186 is used to power display screens in E-book applications, specifically E-Ink Vizplex display, by connecting the screen to the positive and negative charge pump, LDOs 1 and 2, and VCOM rails. The display screens size that can be supported up to 9.7 inches.

9.2 Typical Application



9.2.1 Design Requirements

For this design example, use the parameters listed in Table 2 as the input parameters.

Table 2. Design Parameters

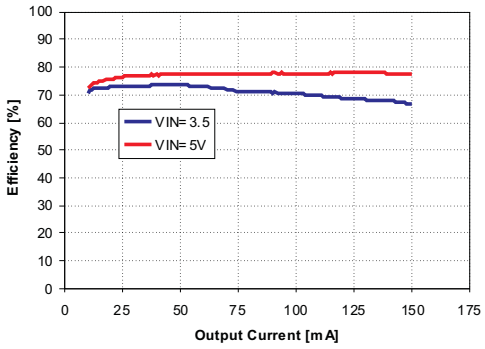
	VOLTAGE	SEQUENCE (STROBE)
VNEG (LDO2)	–15 V	1
VEE (Charge pump 2)	–20 V	2
VPOS (LDO1)	15 V	3
VDDH (Charge pump 1)	22 V	4

9.2.2 Detailed Design Procedure

Table 3. Recommended External Components

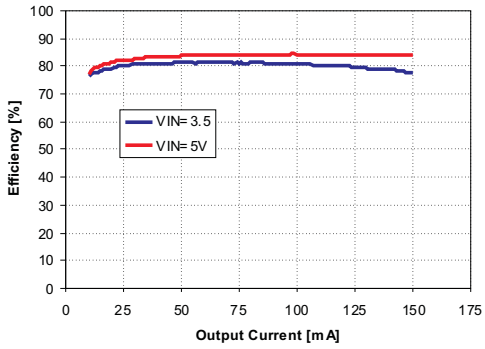
PART NUMBER	VALUE	SIZE	MANUFACTURER
INDUCTORS			
LQH44PN4R7MP0	4.7 µH	4 mm × 4 mm × 1.65 mm	Murata
NR4018T4R7M	4.7 µH	4 mm × 4 mm × 1.8 mm	Taiyo Yuden
VLS252015ET-2R2M	2.2 µH	2 mm × 2.5 mm × 1.5 mm	TDK
NR4012T2R2M	2.2 µH	4 mm × 4 mm × 1.2 mm	Taiyo Yuden
CAPACITORS			
GRM21BC81E475KA12L	4.7 µF, 25 V, X6S	805	Murata
GRM32ER71H475KA88L	4.7 µF, 50 V, X7R	1210	Murata
All other capacitors	X5R or better	—	—
DIODES			
BAS3010	—	SOD-323	Infineon
MBR130T1	—	SOD-123	ON-Semi
BAV99	—	SOT-23	Fairchild
THERMISTOR			
NCP18XH103F03RB	10 kΩ	603	Murata

9.2.3 Application Curves



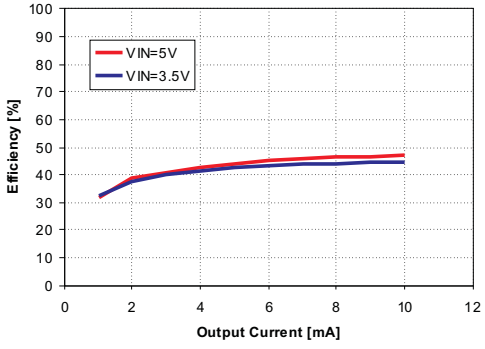
T = 25°C

Figure 29. VN DCDC Efficiency



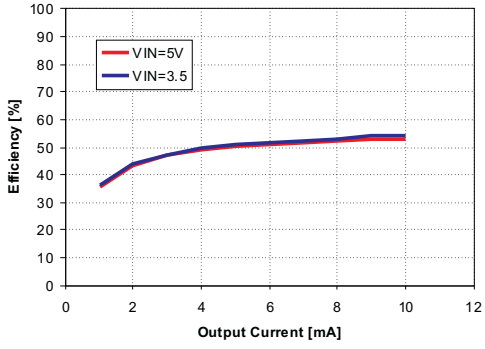
T = 25°C

Figure 30. VB DCDC Efficiency



T = 25°C

Figure 31. VEE Charge Pump Efficiency



T = 25°C

Figure 32. VDDH Charge Pump Efficiency

10 Power Supply Recommendations

The device is designed to operate with an input voltage supply range from 3 V to 6 V. This input supply can be from an externally regulated supply. If the input supply is located more than a few inches from the TPS65186, additional bulk capacitance may be required in addition to the ceramic bypass capacitors. An electrolytic capacitor with a value of 10 µF is a typical choice.

11 Layout

11.1 Layout Guidelines

1. PBKG (Die substrate) must connect to VN (–16 V) with short, wide trace. Wide copper trace will improve heat dissipation.
2. PowerPad is internally connected to PBKG and must not be connected to ground, but connected to VN with a short wide copper trace.
3. Inductor traces must be kept on the PCB top layer free of any vias.
4. Feedback traces must be routed away from any potential noise source to avoid coupling.
5. Output caps must be placed immediately at output pin.
6. Vin pins must be bypassed to ground with low ESR ceramic bypass capacitors.

11.2 Layout Example

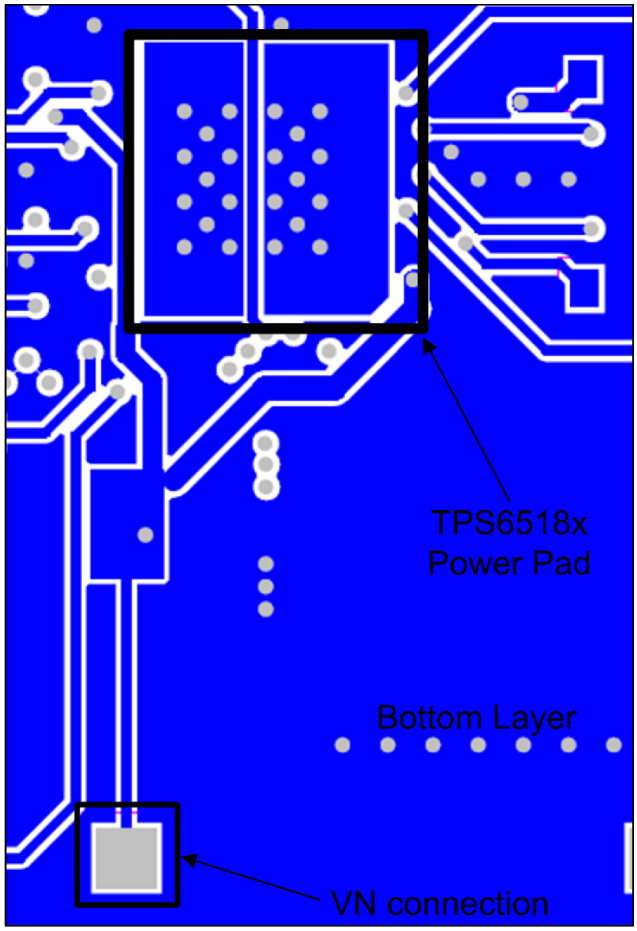


Figure 33. Layout Diagram

12 Device and Documentation Support

12.1 Device Support

12.1.1 Third-Party Products Disclaimer

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12.2 Community Resources

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Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

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E Ink is a registered trademark of E Ink Corporation.
EPSON is a registered trademark of Seiko Epson Corporation.

12.4 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

12.5 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TPS65186RGZR	ACTIVE	VQFN	RGZ	48	2500	RoHS & Green	NIPDAU	Level-3-260C-168 HR	-10 to 85	TPS65186	Samples
TPS65186RGZT	ACTIVE	VQFN	RGZ	48	250	RoHS & Green	NIPDAU	Level-3-260C-168 HR	-10 to 85	TPS65186	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

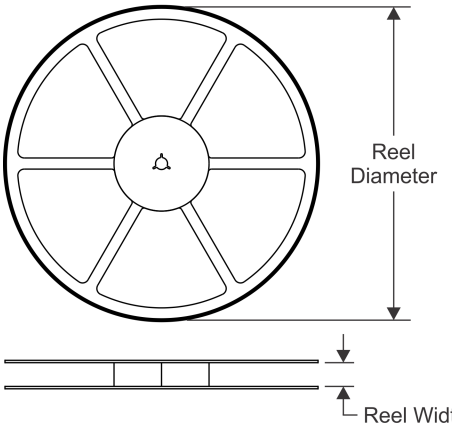
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

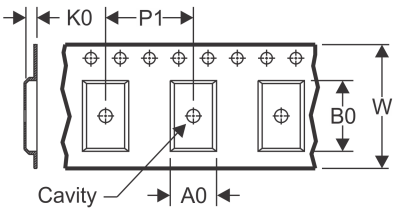
(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

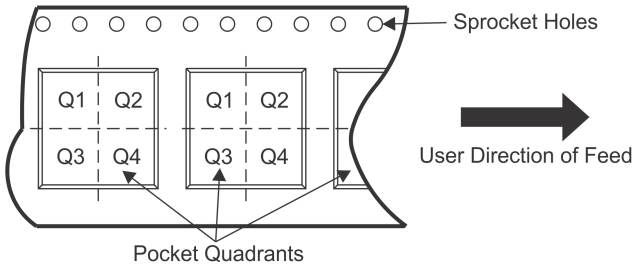


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

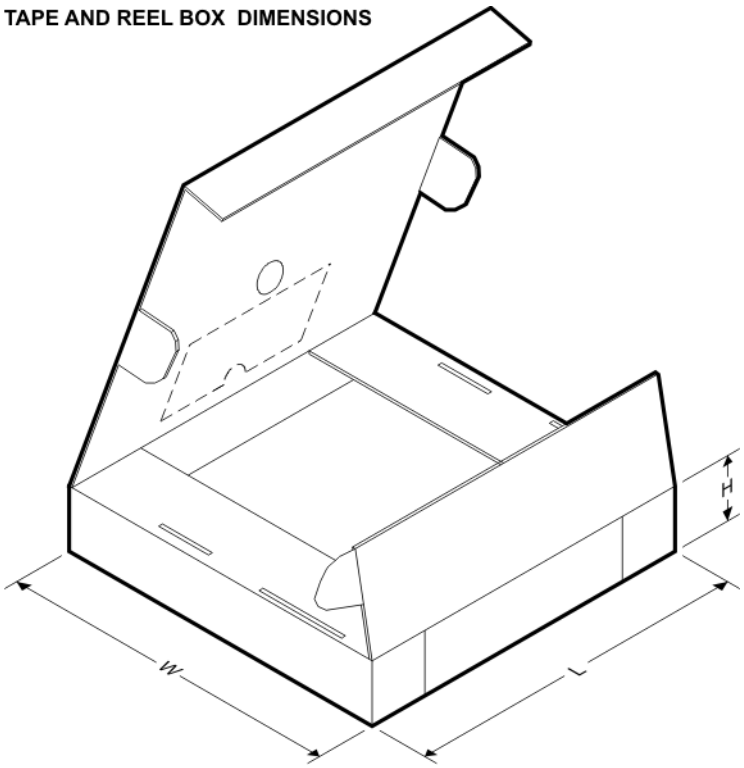
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS65186RGZR	VQFN	RGZ	48	2500	330.0	16.4	7.3	7.3	1.1	12.0	16.0	Q2
TPS65186RGZT	VQFN	RGZ	48	250	180.0	16.4	7.3	7.3	1.1	12.0	16.0	Q2

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS65186RGZR	VQFN	RGZ	48	2500	367.0	367.0	38.0
TPS65186RGZT	VQFN	RGZ	48	250	210.0	185.0	35.0

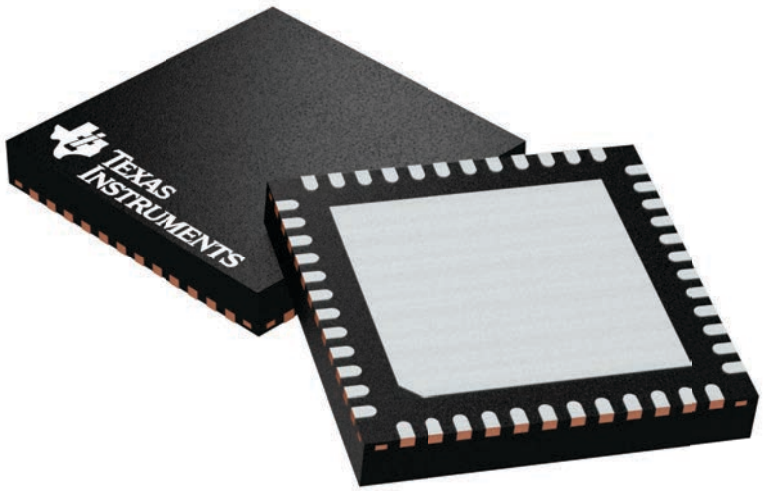
GENERIC PACKAGE VIEW

RGZ 48

VQFN - 1 mm max height

7 x 7, 0.5 mm pitch

PLASTIC QUADFLAT PACK- NO LEAD



Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

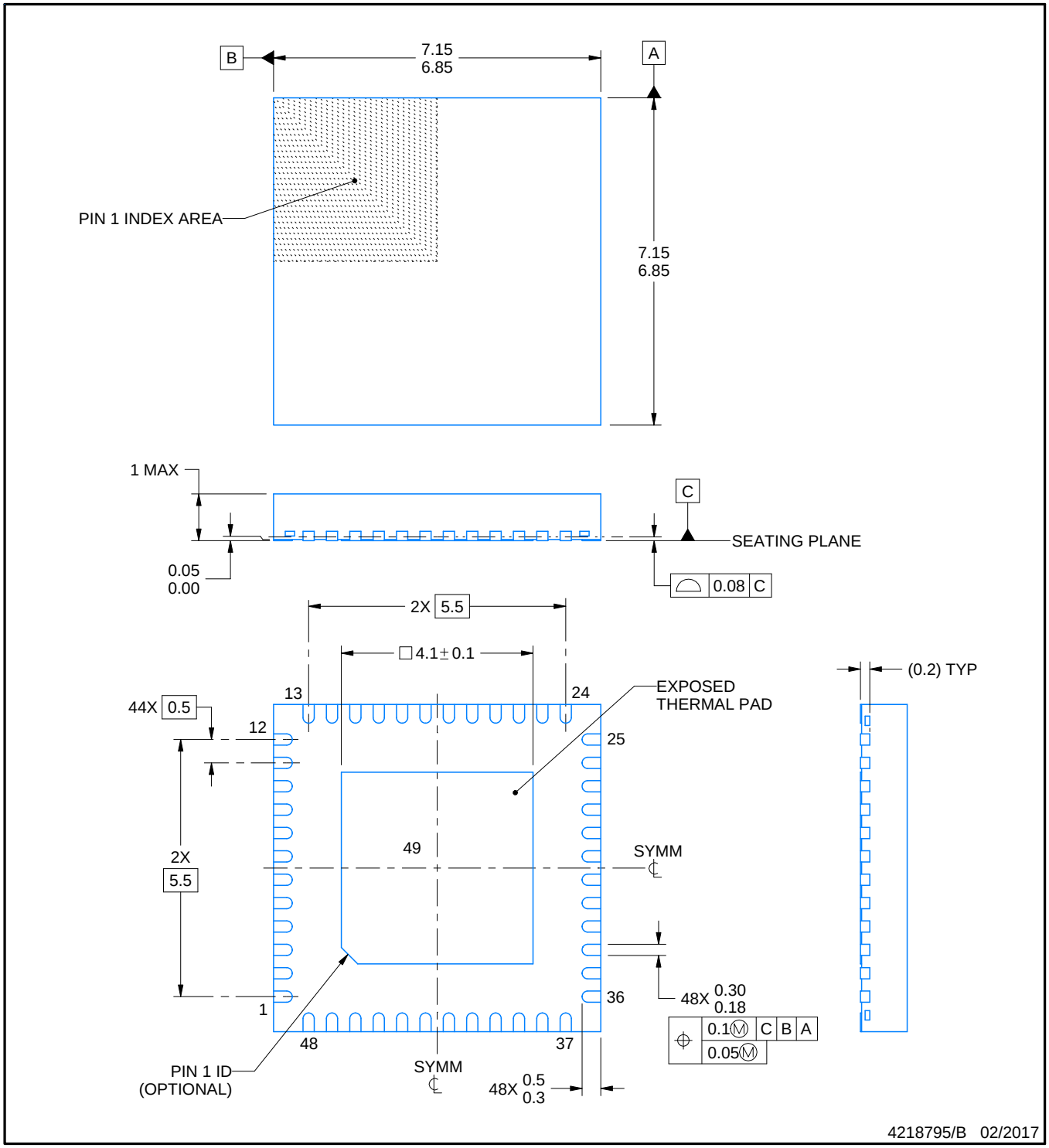
4224671/A

RGZ0048B

PACKAGE OUTLINE

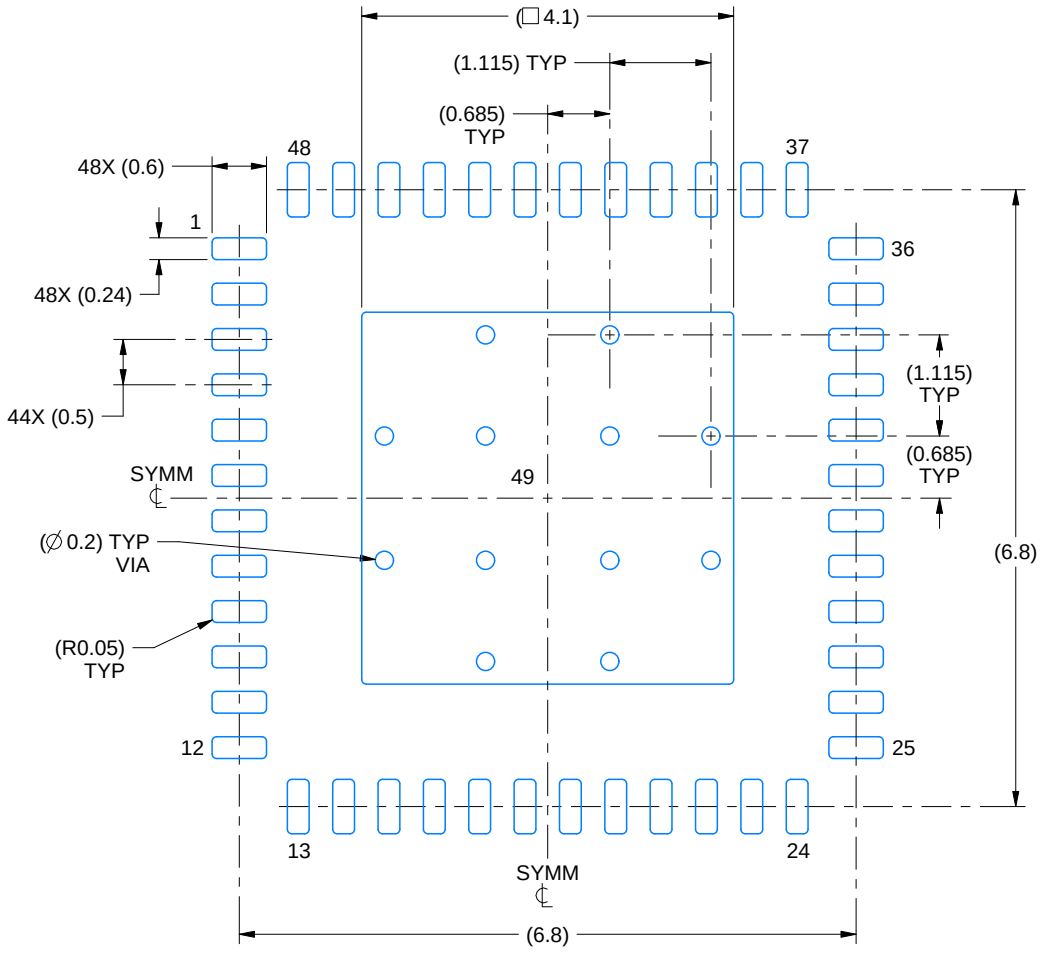
VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD

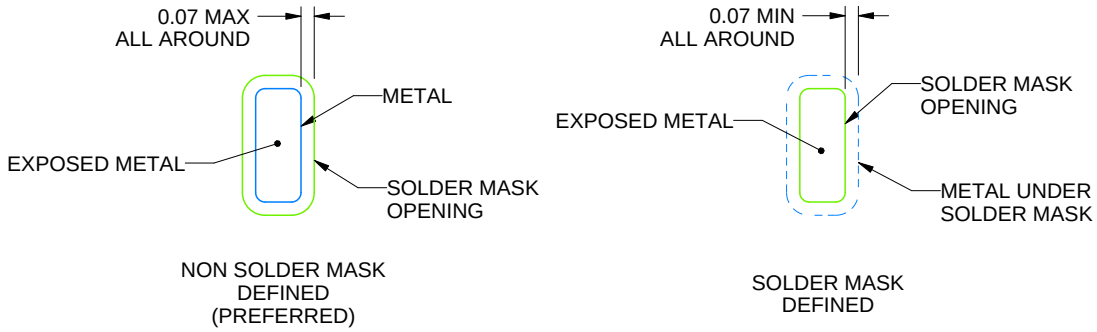


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:12X



SOLDER MASK DETAILS

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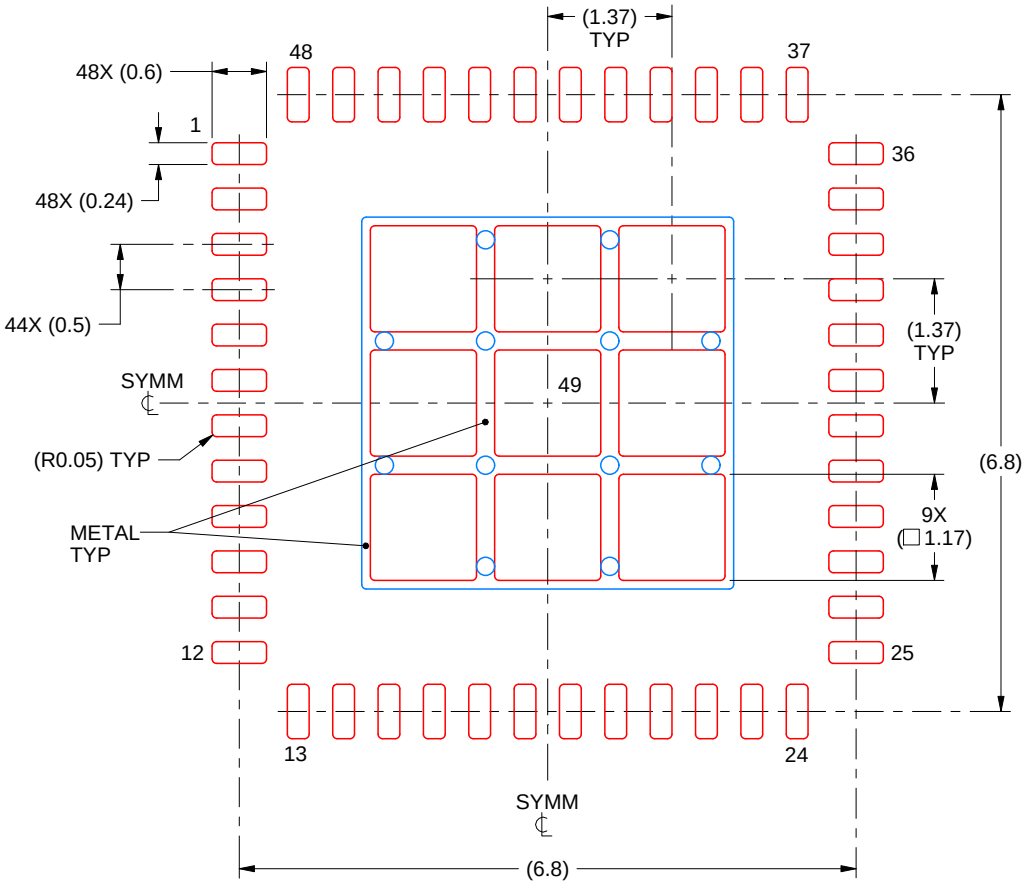
NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD 49
73% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
SCALE:12X

4218795/B 02/2017

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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