THE DATASHEET OF

TPS23841PJDR

HIGH-POWER, WIDE VOLTAGE RANGE, QUAD-PORT ETHERNET POWER SOURCING EQUIPMENT MANAGER

FEATURES

- **Quad-Port Power Management With Integrated Switches and Sense Resistors**
- **High Power PoE up to 25 W at PD Input Operating from a 53-V Minimum Input Power Rail**
- **Wide Range Single Supply: 21.5 V up to 57 V**
- **I_{CUT} = 615 mA, I_{LIM} = 650 mA Nominal**
- **IEEE 802.3af Compatible**
- **Individual Port 15-bit A/D Converters**
- **Auto, Semi-Auto and Power Management Modes**
- **Controlled Current Ramp Power-Up/Down for EMI Reduction**
- **Over-Temperature Protection**
- **DC Disconnect Detection, Supports AC Disconnect**
- **High-Speed 400-kHz I^2C Interface**
- **Supports Legacy PD Detection**
- **PowerPAD™ Package**
- **Comprehensive Power Management Software Available for MPS430 Microcontroller**

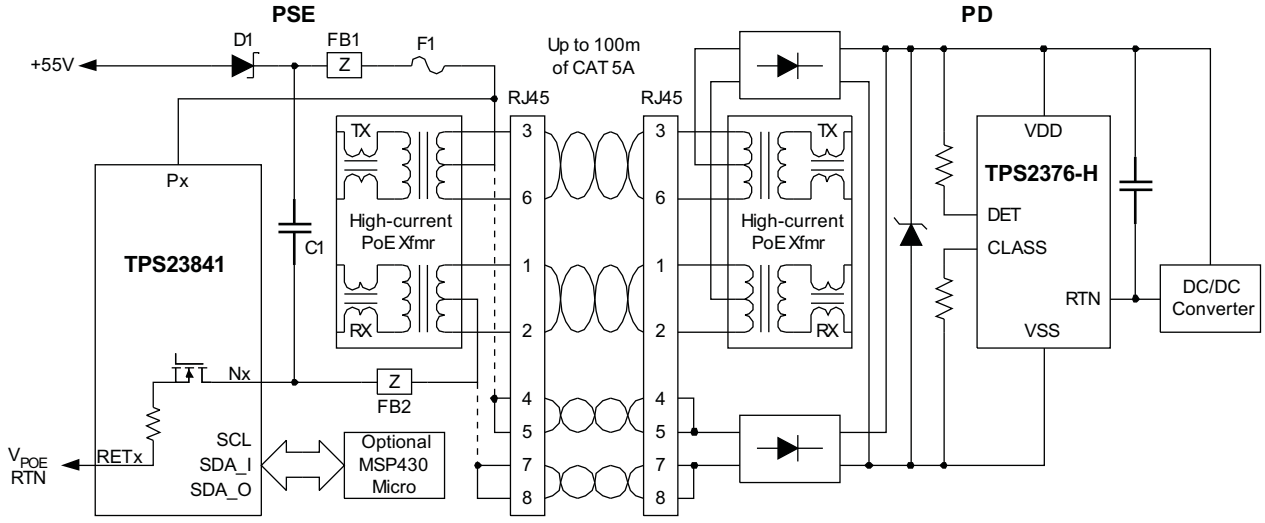
APPLICATIONS

- **Medical/Industrial Applications at 24 V**
- **High Power Ethernet Enterprise Switches**
- **SOHO Hubs, Ethernet Hubs**
- **Ethernet High Power Mid-Spans**
- **High Power PSE Injectors**

DESCRIPTION

The TPS23841 is a high-power, wide voltage range, quad-port sourcing equipment manager. The TPS23841 can provide up to 570 mA per port over a wide temperature range (-40°C to +125°C). Each port may operate from 21.5 V up to 57 V. The integrated output eliminates two external components per port (MOSFET and sense resistor) and survives 100-V transients. Four individual 15-bit A/D converters are used to measure signature resistance, voltage, current and die temperature, resulting in a simple and robust PSE solution. The TPS23841 comes with a comprehensive software solution to meet the most demanding applications which can serve as a core for all PoE system designs.

TYPICAL APPLICATION



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

PowerPAD is a trademark of Texas Instruments.

DESCRIPTION (CONTINUED)

The TPS23841 has three internal supply buses (10 V, 6.3 V and 3.3 V) generated from the 48-V input supply. These supplies are used to bias all internal digital and analog circuitry. Each supply has been brought out separately for proper bypassing to insure high performance. The digital supply (3.3 V) is available for powering external loads up to 2 mA. For more demanding loads it is highly recommended to use external buffers to prevent system degradation. When the TPS23841 is initially powered up an internal Power-on-Reset (POR) circuit resets all registers and sets all ports to the off state to ensure that the device is powered up in a known safe operating state.

The TPS23841 has three modes of operation; auto mode (AM), semi-auto mode (SAM) and power management mode (PMM).

- In auto mode the TPS23841 performs discovery, classification and delivery of power autonomously to a compliant PD without the need of a micro-controller.
- In semi-auto mode the TPS23841 operates in auto mode but users can access the contents of all read status registers and A/D registers through the I^2C serial interface. All write control registers are active except for D0 through D3 of port control register 1 (Address 0010) for limited port control. The semi-auto mode allows the TPS23841 to detect valid PD's without micro-controller intervention but adds a flexibility to perform power management activities.
- Power management mode (with a micro-controller) allows users additional capabilities of discovering non-compliant (legacy) PDs, performing AC Disconnect and advanced power management system control that are based on real time port voltages and currents. All functions in this mode are programmed and controlled through read/write registers over the I^2C interface. This allows users complete freedom in detecting and powering devices. A comprehensive software package is available that mates the power of the TPS23841 with the MSP430 micro-controller.

TPS23841 integrated output stage provides port power and low-side control. The internal low-side circuitry is designed with internal current sensing so there are no external resistors required. The output design ensures the power switches operate in the fully enhanced mode for low power dissipation.

The I^2C interface allows easy application of opto-coupler circuitry to maintain Ethernet port isolation when a ground based micro-controller is required. The TPS23841 five address pins (A1–A5) allow the device to be addressed at one of 31 possible I^2C addresses. Per-port write registers separately control each port state (discovery, classification, legacy, power up, etc) while the read registers contain status information of the entire process along with parametric values of discovery, classification, and real-time port operating current, voltage and die temperature.

The proprietary 15-bit integrating A/D converter is designed to meet the harsh environment where the PSEPM resides. The converter is set for maximum rejection of power line noise allowing it to make accurate measurements of line currents during discovery, classification and power delivery for reliable power management decisions.

The TPS23841 is available in either 64-pin PowerPAD™ down (PAP) or 64-pin PowerPAD up (PJD) packages.

ORDERING INFORMATION

TEMPERATURE RANGE $T_A = T_J$	PACKAGED DEVICES(1)	
	TQFP – 64 (PAP)(2)	TQFP – 64 (PJD)(2)
–40°C to 125°C	TPS23841PAP	TPS23841PJD

(1) The PAP and PJD packages are available taped and reeled. Add R suffix to device type (e.g.TPS23841PAPR) to order quantities of 1,000 devices per reel.
(2) PAP = PowerPad down, PJD = PowerPad up.

ABSOLUTE MAXIMUM RATINGS

over operating free-air temperature range (unless otherwise noted) (1)(2)

PARAMETER		VALUE	UNIT
	V10 current sourced	100	µA
	V3.3 current sourced	5	mA
	Applied voltage on CINT#, CT, RBIAS	–0.5 to 10	V
	Applied voltage on SCL, SDA_I, SDA_O, INTB, A1, A2, A3, A4, A5, MS, PORB, WD_DIS, ALT_A/B, AC_LO, AC_HI	–0.5 to 6	
	Applied voltage on V48, P#, N#	–0.5 to 80	
T_J	Junction operating temperature	–40 to 125	°C
T_{stg}	Storage temperature --55 to 150	–55 to 150	
T_{sol}	Lead temperature (soldering, 10 sec.)	260	

(1) Stresses beyond those listed under *absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *recommended operating conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltages are with respect to GND. Currents are positive into, negative out of the specified terminal. Consult Packaging Section of the Data book for thermal limitations and considerations of packages.

DISSIPATION RATINGS(1)

PACKAGE	THERMAL RESISTANCE JUNCTION TO CASE θ_{JC}	THERMAL RESISTANCE JUNCTION TO AMBIENT θ_{JA}
PAP	0.38°C/W	21.47°C/W
PJD	0.38°C/W	21.47°C/W

(1) Thermal Resistance measured using 2-oz copper trace and copper pad solder following layout recommendation in TI Publication PowerPAD Thermally Enhanced Package Technical Brief SLMA002.

RECOMMENDED OPERATING CONDITIONS

over operating free-air temperature range (unless otherwise noted)

PARAMETER		MIN	NOM	MAX	UNIT
V_{IN}	Input voltage, V48 pin	21.5	48	57	V
T_J	Junction temperature	-40		125	°C

ELECTRO STATIC DISCHARGE (ESD) PROTECTION

	MAX	UNIT
Human body model	1.5	kV
CDM	1	
Machine model	0.2	

ELECTRICAL CHARACTERISTICS

V48 = 48 V, R_T = 124 kΩ, C_T = 220 pF, C_{INT} = 0.027 µF (low leakage), –40°C to 125°C and $T_A = T_J$ (unless otherwise noted)

	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Power Supply						
	V48 quiescent current	Off mode (all ports)	4	9	12	mA
	V48 quiescent current	Powered mode (all ports)		10	14	
	V10, internal analog supply	I_{LOAD} = 0	9.75	10.5	11.5	V
	V3.3, internal digital supply	I_{LOAD} = 0 to 3 mA	3	3.3	3.7	
	V3.3 short circuit current	V = 0	3		12	mA
	V6.3, internal supply	I_{LOAD} = 0	5	6.3	7	V
	V2.5, internal reference supply	I_{LOAD} = 0	2.46	2.5	2.54	
	V_{UVLO_R}, V48 UVLO	Input voltage rising	16.0		21.5	
	V_{UVLO_F}, V48 UVLO	Input voltage falling	14		21	
	V_{HYSUV}, UVLO hysteresis		0.2	1.0	2.0	
	Internal POR time out(I^2C)	After all supplies are good I^2C activity is valid		8		Clock Pulses
	Internal POR time out (Port)	After all supplies are good Port active to I^2C commands		66000		
Port Discovery						
	Port off #P to #N input resistance		400	600		kΩ
	Discovery open circuit voltage			22	30	V
	Discovery 1 voltage loop control	70 µA < I_{PORT} < 3 mA	2.8	4.4		
	Discovery 2 voltage loop control	70 µA < I_{PORT} < 3 mA		8.8	10	
	Discovery current limit	P = N = 48 V	3	4	5	mA
	Auto-mode discovery resistance acceptance Band		19		26.5	kΩ
	Auto-mode discovery resistance low end rejection		0		15	
	Auto-mode discovery resistance high end rejection		33			
	Discovery1,2 A/D conversion scale factor	100 µA < I_{PORT} < 3 mA	5.30	6.10	6.75	count/µA
	Discovery1,2 A/D conversion time	I_{PORT}= 120 µA				ms
Port Classification						
	Classification voltage loop control	100 µA < I_{PORT} < 50 mA	15	17.5	20	V
	Classification current limit	P = N = 48 V	50	60	100	mA
	Class 0 to 1 detection threshold		5.5	6.5	7.5	
	Class 1 to 2 detection threshold		13	14.5	16	
	Class 2 to 3 detection threshold		21	23	25	
	Class 3 to 4 detection threshold		31	33	35	
	Class 4 to 0 detection threshold		45	48	51	
	Classification A/D conversion scale factor		375	424	475	Count/mA
	Classification A/D conversion time	I_{PORT} = 50 mA		18	22	ms

ELECTRICAL CHARACTERISTICS (continued)

V48 = 48 V, R_T = 124 kΩ, C_T = 220 pF, C_{INT} = 0.027 µF (low leakage), –40°C to 125°C and $T_A = T_J$ (unless otherwise noted)

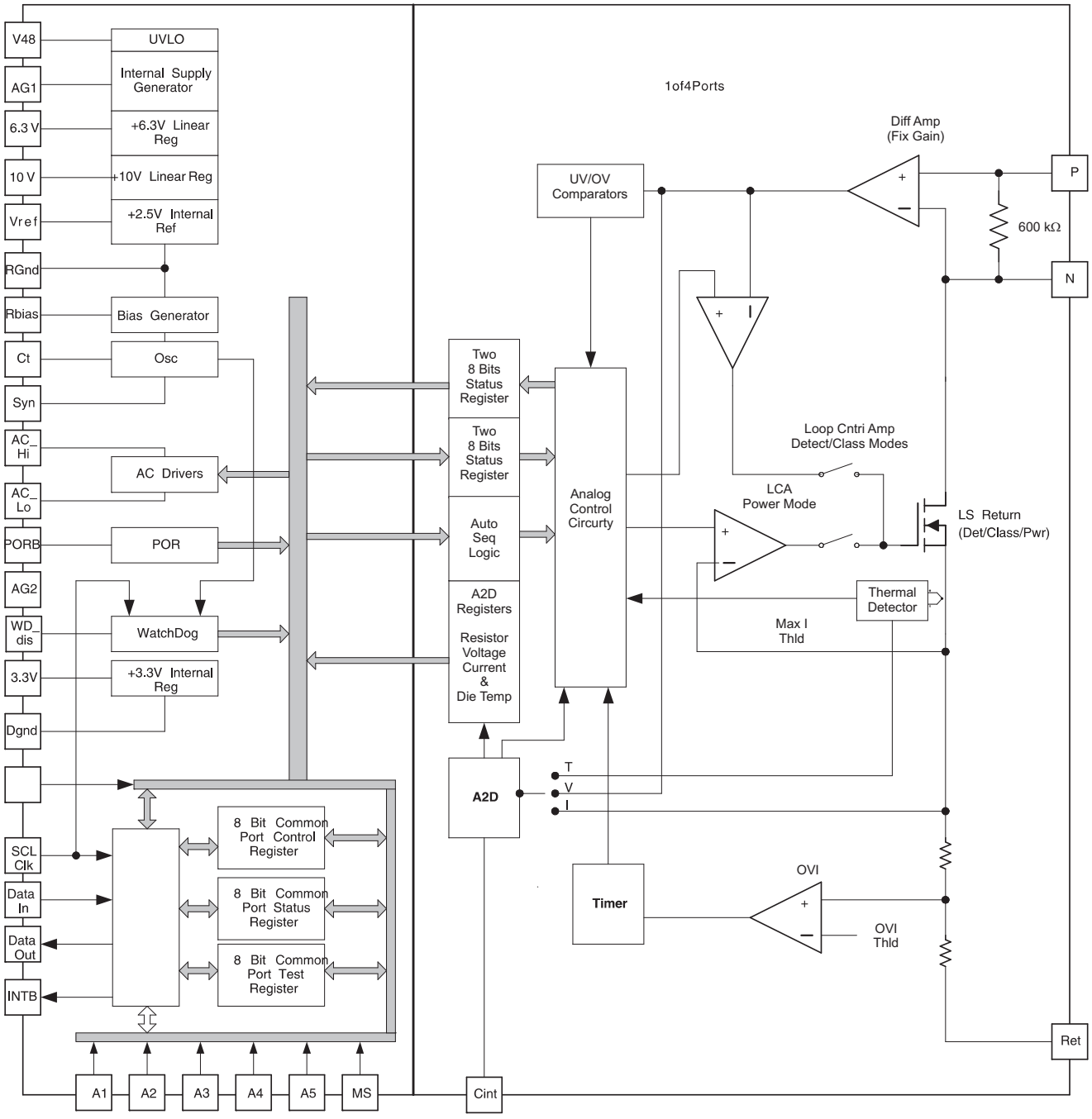
	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Port Legacy Detection						
	Legacy current limit	P = N = 48 V	2.6	3.5	4.3	mA
	Legacy voltage A/D conversion scale factor	100 mV < V_{PORT} < 17.5 V	1365	1400	1445	Count/V
	Legacy A/D conversion time	0 V < V_{PORT} < 15 V		18	22	ms
Port Powered Mode						
	Port on resistance	20 mA < I_{PORT} < 300 mA		1.3	1.8	Ω
I_{CUT}	Over current threshold	R_{BIAS} = 124 kΩ, C_T = 220 pF,	570	615	665	mA
I_{LIM}	Output current limit		600	650	700	
I_{LIM} - I_{CUT}	Threshold delta		2		70	
	Disconnect timer current threshold	R_{BIAS} = 124 kΩ, C_T = 220 pF		7.5	10	
T_{MPDO}	Disconnect detection time	I_{LOAD} < current threshold, R_{BIAS} = 124 kΩ, C_T = 220 pF	300		400	ms
	Port output UV		42.0	42.7	44.0	V
	Port output OV		54	55	56	
T_{OVLD}	Over current time out	R_{BIAS} = 124 kΩ, C_T = 220 pF	50		75	ms
T_{LIM}	Short circuit time out	RBIAS = 124 k., CT = 220 pF	50		75	
	Turn--off delay from UV/OV faults	RBIAS = 124 k., CT = 220 pF, After port enabled and ramped up		3		
	Port current A/D conversion scale factor	20 mA < I_{PORT} < 56 V	31	36.41	40	Count/mA
	Port current A/D conversion time	I_{PORT} < 300 mA		18	22	ms
	Port voltage A/D conversion scale factor	45 V < V_{PORT} < 56 V	335	353	370	Count/V
	Port voltage A/D conversion time			18	22	ms
	Port temperature A/D conversion		(17500 - counts)/16			°C
Port Disable Mode						
	Port N voltage	P = 48 V	47			V
AC LO and AC HI Specification						
	AC_LO, AC_HI – low output voltage		0		0.5	V
	AC_LO – high output voltage		3.0		5.0	
	AC_HI – high output voltage		5.0		7.0	

ELECTRICAL CHARACTERISTICS (continued)

V48 = 48 V, R_T = 124 kΩ, C_T = 220 pF, C_{INT} = 0.027 µF (low leakage), –40°C to 125°C and $T_A = T_J$ (unless otherwise noted)

	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Digital I²C DC Specifications						
	SCL, SDA_I, A1–A5 ,WD_DIS, ALTA/B, MS, PORB logic input threshold			1.5		V
	SCL, SDA_I input hysteresis			250		mV
	MS, PORB input hysteresis			150		
	WD_DIS, ALTA/B, MS, PORB input pulldown resistance	Input voltage 0.5 to 3 V		50		kΩ
	A1–A5 pull-down current			10		µA
	SDA_O logic high leakage	Drain = 5 V		100		nA
	SDA_O logic low	I_{SINK} = 10 mA		200		mV
	INTB logic high leakage	Drain = 6 V		10		µA
	INTB logic low	I_{SINK} = 10 mA		200		mV
Digital I²C Timing						
	SCL clock frequency		0		400	kHz
	Pulse duration	SCL high	0.6			µs
		SCL low	1.3			
	Rise time, SCL to SDA				0.300	
	Fall time, SCL to SDA				0.300	
	Setup time, SDA to SCL		0.250			
	Hold time, SCL to SDA		0.300		0.900	
	Bus free time between start and stop		1.3			
	Setup time, SCL to start condition		0.6			
	Hold time, start condition to SCL		0.6			
	Setup time, SCL to stop condition		0.6			

TPS23841 SINGLE PORT BLOCK DIAGRAM



TERMINAL FUNCTIONS

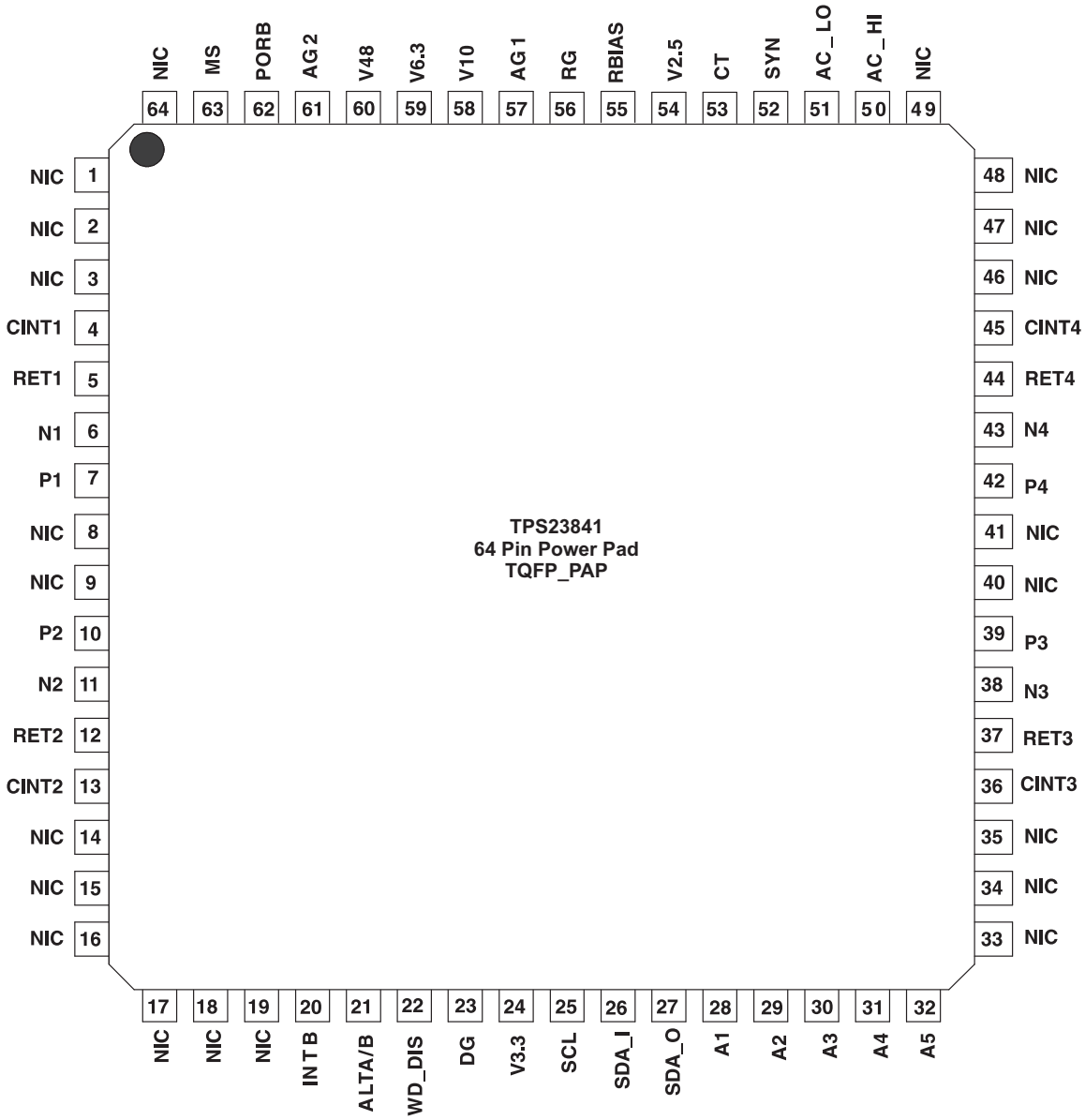
TERMINAL			I/O	DESCRIPTION
NAME	NO.			
	PAP	PJD		
POWER AND GROUND				
V48	60	5	I	48-V input to the device. This supply can have a range of 22 V to 57 V. This pin should be decoupled with a 0.1-µF capacitor from V48 to AG1 placed as close to the device as possible.
V10	58	7	O	10-V analog supply. The 10-V reference is generated internally and connects to the main internal analog power bus. A 0.1-µF de-coupling capacitor should terminate as close to this node and the AG1 pin as possible. Do not use for an external supply.
V6.3	59	6	O	6.3-V analog supply. A 0.1-µF de-coupling capacitor should terminate as close to this pin and the AG1 pin as possible. Do not use for an external supply.
V3.3	24	41	O	3.3-V logic supply. The 3.3-V supply is generated internally and connects to the internal logic power bus. A 0.1-µìF de-coupling capacitor should terminate as close to this node and the DG pin as possible. This output can be used as a low current supply to external logic.
V2.5	54	11	O	2.5-V reference supply. The V2.5 is generated internally and connects to the internal reference power bus. This pin should not be tied to any external supplies. A 0.1-µF de-coupling capacitor should terminate as close to this node and the RG pin as possible. Do not use for an external supply.
AG1	57	8	GND	Analog ground 1. This is the analog ground of the V6.3, V10 and V48 power systems. It should be externally tied to the common copper 48-V return plane. This pin should carry the low side of three de-coupling capacitors tied to V48, V10 and V6.3.
AG2	61	4	GND	Analog ground 2. This is the analog ground which ties to the substrate and ESD structures of the device. It should be externally tied to the common copper 48-V return plane. AG1 and AG2 must be tied together directly for the best noise immunity.
DG	23	42	GND	Digital ground. This pin connects to the internal logic ground bus. It should be externally tied to the common copper 48-V return plane.
RG	56	9	GND	Reference ground. This is a precision sense of the external ground plane. The integration capacitor (CINT) and the biasing resistor (RBIAS pin) should be tied to this ground. This ground should also be used to form a printed wiring board ground guard ring around the active node of the integration capacitor (CINT). It should tie to common copper 48-V return plane.
PORT ANALOG SIGNAL				
P1	7	58	I	Port Positive. 48-V load sense pin. Terminal voltage is monitored and controlled differentially with respect to each Port N pin Optionally, if the application warrants, this high side path can be protected with the use of a self resetting poly fuse.
P2	10	55	I	
P3	39	26	I	
P4	42	23	I	
N1	6	59	I	Port negative. 48-V load return pin. The low side of the load is switched and protected by internal circuitry that will limit the current.
N2	11	54	I	
N3	38	27	I	
N4	43	22	I	
RET1	5	60	I	48 V return pin
RET2	12	53	I	
RET3	37	28	I	
RET4	44	21	I	
CINT1	4	61	I	Integration capacitor. This capacitor is used for the ramp A/D converter signal integration. Connect A 0.027- µF capacitor from this pin to RG. To minimize errors use a polycarbonate, poly-polypropylene, polystyrene or teflon capacitor type to prevent leakage. Other types of capacitors can be used with increased conversion error.
CINT2	13	52	I	
CINT3	36	29	I	
CINT4	45	20	I	

TERMINAL FUNCTIONS (continued)

TERMINAL			I/O	DESCRIPTION
NAME	NO.			
	PAP	PJD		
ANALOG SIGNALS				
CT	53	12	I	This is a dual-purpose pin. When tied to an external capacitor this pin sets the internal clock. When the CT pin is grounded the SYN pin turns from a output to an input (see SYN pin description) The timing capacitor and the resistor on the RBIAS pin sets the internal clock frequency of the device. This internal clock is used for the internal state machine, integrating A/D counters, POR time out, faults and delay timers of each port. Using a 220-pF capacitor for CT and a 124-kΩ resistor for RBIAS sets the internal clock to 245 kHz and ensure IEEE 802.3af compliance along with maximizing the rejection of 60-Hz line frequency noise from A/D measurements.
RBIAS	55	10	I	Bias set resistor. This resistor sets all precision bias currents within the chip. This pin will regulate to 1.25V (V2.5/2) when a resistor is connected between RBIAS and RG. This voltage and RBIAS generate a current which is replicated and used throughout the chip. This resistor also works in conjunction with the capacitors on CT and CINT to set internal timing values. The RBIAS resistor should be connected RG. RBIAS is a high impedance input and care needs to be taken to avoid signal injection from the SYN pin or I^2C signals.
SYN	52	13	I/O	This is a dual purpose pin. When the CT pin is connected to a timing capacitor this output pin is a 0v to 3.3V pulse of the internal clock which can be used to drive other TPS23841 SYN pins for elimination of a timing capacitor. When the CT pin is grounded this pin becomes an input pin that can be driven from a master TPS23841 or any other clock generator signal.
AC_LO	51	14	O	Totem-pole output pin for AC Disconnect excitation.
AC_HI	50	15	O	Totem-pole output pin for AC Disconnect excitation.
DIGITAL SIGNALS				
SCL	25	40	I	Serial clock input pin for the I^2C interface.
SDA_I	26	39	I	Serial data input pin for the I^2C interface. When tied to the SDA_O pin, this connection becomes the standard bi-directional serial data line (SDA)
SDA_O	27	38	O	Serial data open drain output for the I^2C interface. When tied to the SDA_I pin, this connection becomes the standard bi-directional serial data line (SDA). This is a open drain output that can directly drive opto-coupler.
WD_DIS	22	43	I	The WD_DIS pin disables the watchdog timer function when connected to 3.3 V. The pin has internal 50-k. resistor to digital ground. The watchdog timer monitors the I^2C clock pin (SCL) and the internal oscillator activity in power management mode and only the internal oscillator activity in auto mode.
INTB	20	45	O	This is an open-drain output that goes low if a fault condition occurs on any of the 4 ports.
ALTA/B	21	44	I	When this input is set to logic low there is no back-off time after a discovery failure. When this pin set to a logic high there is a back-off time (approximately 2 seconds) before initiating another discovery cycle. This pin has an internal 50-kΩ resistor pull-down to digital ground.
A1	28	37	I	Address 1 through 5 These are the I^2C address select inputs. Select the appropriate binary address on these pins by connecting to the chip ground for a logic low or tying to the V3.3 pin for a logic high. Each address line has an internal current source pull-down to digital ground.
A2	29	36	I	
A3	30	35	I	
A4	31	34	I	
A5	32	33	I	
MS	63	2	I	The MS pin selects either the auto mode (MS low) or the power management mode, PMM, (MS high). This pin can be held low for controller-less standalone applications. When MS is low and the POR timing cycle is complete the chip will sequentially *Discover, Classify and Power on* each port. When MS is set high the ports are controlled by register setting via the I^2C bus. The MS pin has an internal 50-kΩ resistor pull-down to analog ground.
PORB	62	3	I	This pin can be used to override the internal POR. When held low, the I^2C interface, all the state machines, and registers are held in reset. When all internal and external supplies are within specification, and this pin is set to a logic high level, the POR delay will begin. The I^2C interface and registers will become active within 70µs of this event and communications to read or preset registers can begin. The reset delay for the remainder of the chip then extinguishes in 1 second. This pin has an internal 50-kΩ resistor pull-down to analog ground.

CONNECTION DIAGRAM

TQFP PACKAGE (TQFP – 64)(1)(2)
(TOP VIEW PAP Package)

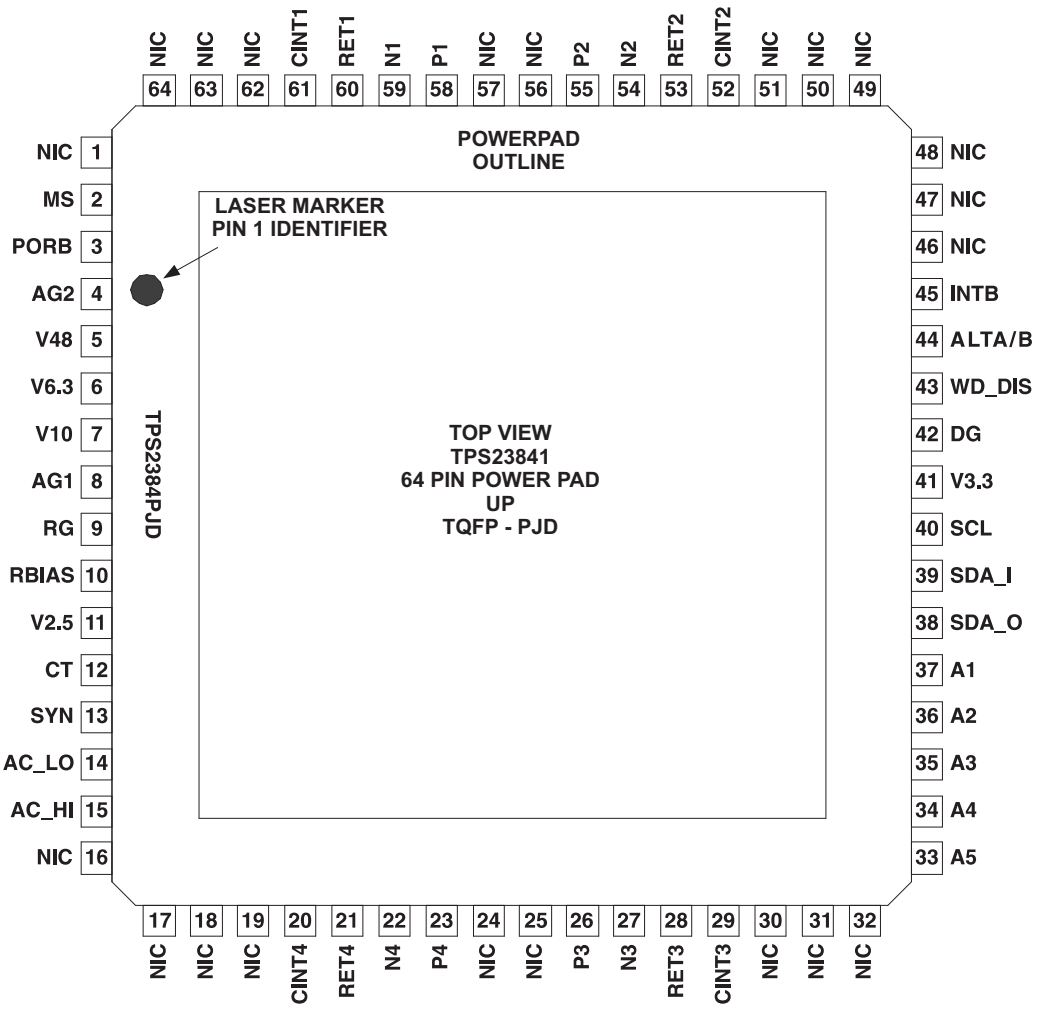


(1) NIC = No internal connection. Pins are floating.

(2) NIC pins can be tied to the ground plane for improved thermal characteristics and to prevent noise injection from unused pins.

(3) NIC pins next to CINT pins should be tied to ground to prevent noise injection into A/D converter.

TQFP PACKAGE (TQFP–64)(1)(2)
(TOP VIEW PJD Package)



(1) NIC = No internal connection. Pins are floating.

(2) NIC pins can be tied to the ground plane for improved thermal characteristics and to prevent noise injection from unused pins.

(3) NIC pins next to CINT pins should be tied to ground to prevent noise injection into A/D converter.

AUTO MODE FUNCTIONAL DESCRIPTION

Auto Mode

Auto mode (AM, MS = 0) operation is the basic approach for applying power to IEEE compliant PD's. When AM has been selected the TPS23841 automatically performs the following functions:

- Discovery of IEEE 802.3af compliant powered devices (PD's)
- Classification
- Power delivery
- Port over/under voltage detection, (if enabled, see Over/Under Voltage Fault section)
- Port over current detection (570 mA < I_{PORT} < 665 mA
- Port maximum current limit (600 mA < I_{PORT} < 700 mA)
- DC Disconnect (5 mA < I_{PORT} < 10 mA)
- Thermal shutdown protection (TSD), (T_J > 150°C)
- Internal oscillator watchdog

In AM the contents of all read registers are available via the I^2C interface. In addition all control registers except for the function bits can be written. This supports a semi-auto mode where the TPS23841 auto detects compliant PD's while a host can access the A/D registers and class information and then implement power management (including turning a port off, responding to faults, etc).

The write registers that are still active in AM are:

- All ports disable – Common Control register 0001b
- Over/Under Voltage Faults – Common Control register 0001b
- Software reset – Common Control register 0001b
- Disconnect disable – Port Control 1 register 0010b
- Discovery fault disable – Port Control 1 register 0010b
- Port enable – Port Control 2 register 0011b

For alternative B, semi-auto mode implementations which will manipulate the all ports disable or Port Enable bits, please contact the factory for additional application information.

AUTO MODE FUNCTIONAL DESCRIPTION (continued)

Auto Mode Functional Description

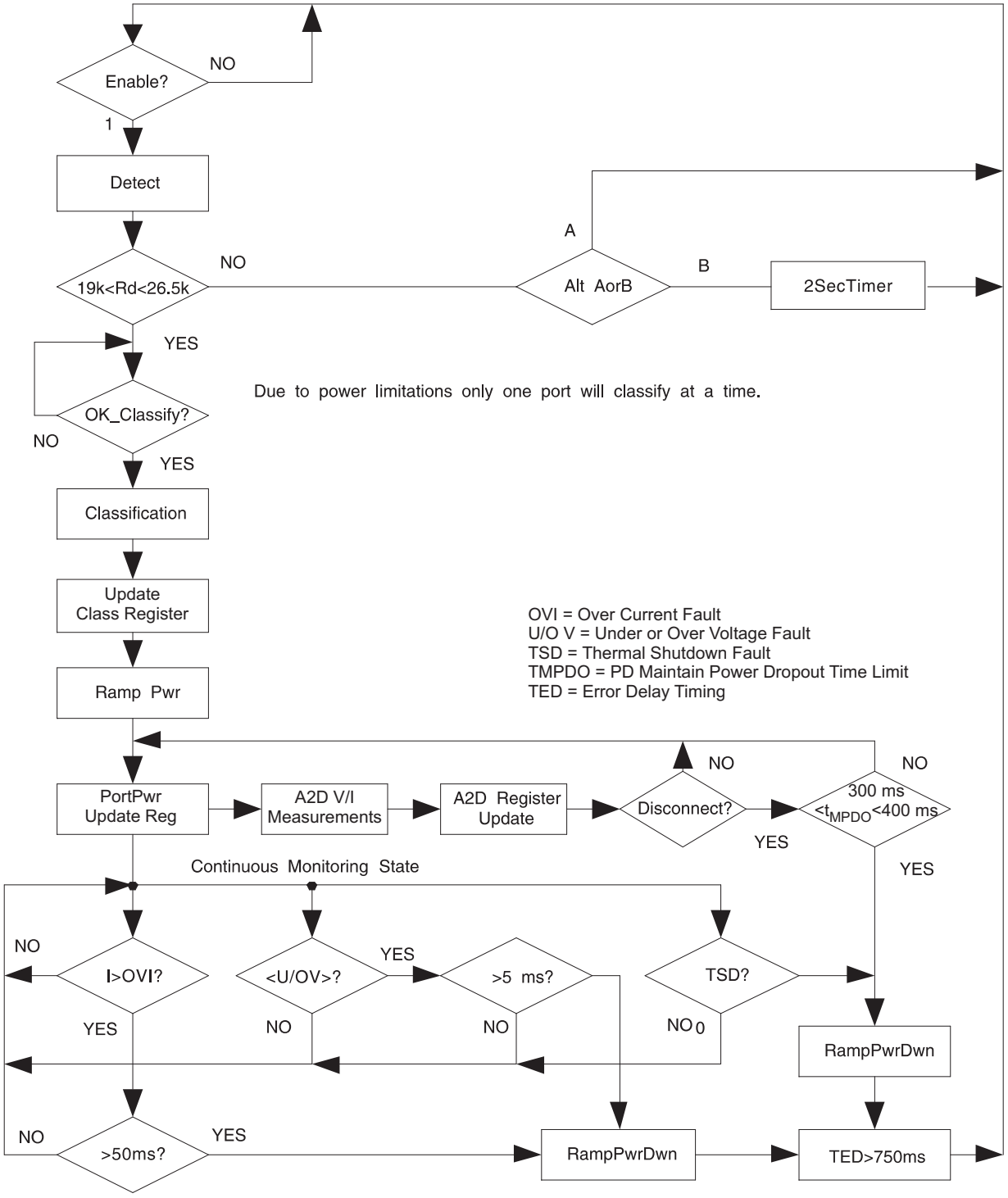


Figure 1. The Basic Flow for Auto Mode

AUTO MODE FUNCTIONAL DESCRIPTION (continued)

AM Discovery

The TPS23841 uses a four-point measurement technique using two low level probe signals (typically 4.4 V and 8.8V) during the discovery process to determine whether a valid PD is present. The use of a multipoint detection method for the PD resistor measurement allows accurate detection even when series steering diodes are present. The low level probe voltages also prevent damage to non-802.3 devices. When a valid PD has been detected the TPS23841 moves to classification. If a valid PD has not been detected the TPS23841 continues to cycle through the discovery process. The waveform in Figure 2 shows typical N-pin waveforms for the discovery of a valid PD and the failure to discovery due to a discovery resistor of 15 kΩ and 33kΩ.

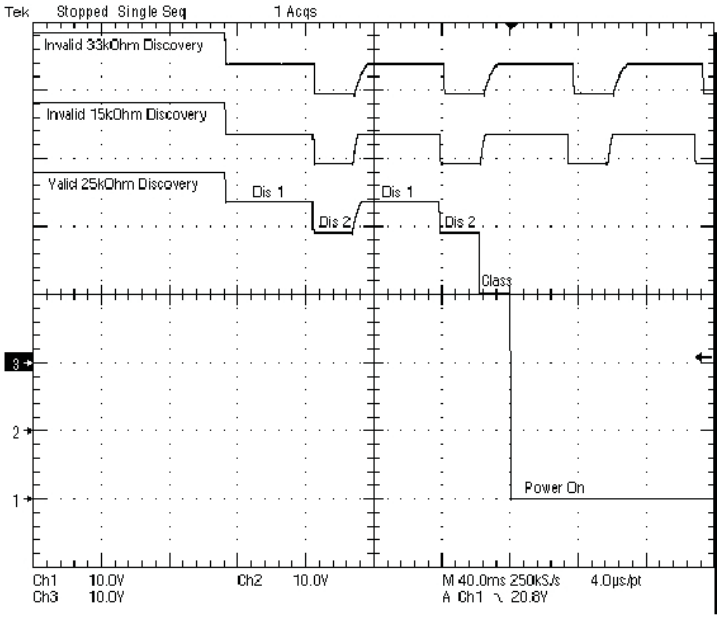


Figure 2.

AUTO MODE FUNCTIONAL DESCRIPTION (continued)

AM Classification

After a successful discovery of a valid PD the TPS23841 enters the classification function that identifies the power level based on the PD's current signature. The classification current level is measured at a reduced terminal voltage of 17.5V. During classification the power dissipation can be at its highest; therefore, to prevent over temperature shutdown in automode only one port classifies at a time. When multiple ports successfully discover and proceed to classification at the same time the auto sequencer processes each request separately allowing only one port to enter classification. Figure 3 shows all 4 ports successfully detecting a valid PD at the same time and than the classification of each port occurring separately.

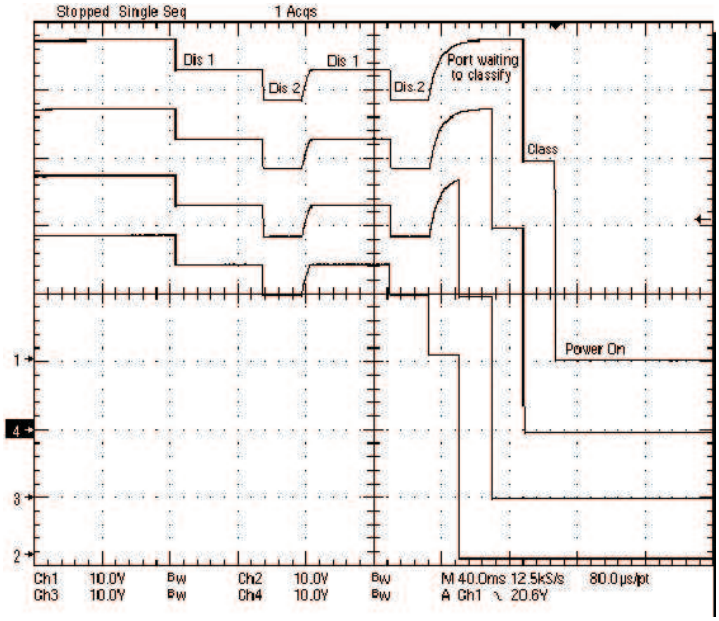


Figure 3.

AUTO MODE FUNCTIONAL DESCRIPTION (continued)

Upon completion of classification the port classification register is updated. In AM mode this information is not used but for semi-auto mode the class information can be used for power management. Figure 4 shows actual class currents and the class assignment which were stored in the register. These assignments are compliant with the IEEE 802.3af Standard

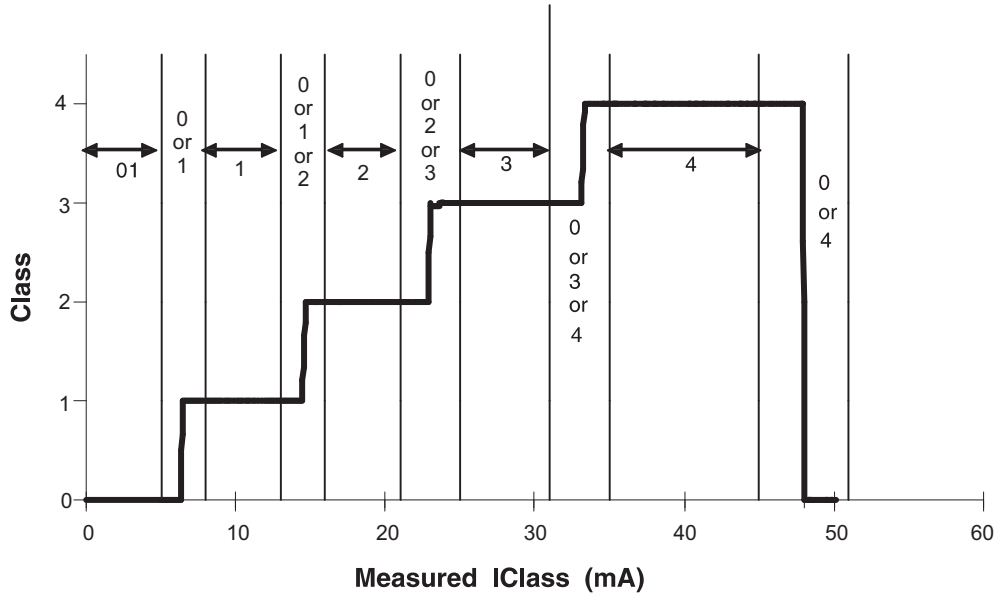


Figure 4.

AUTO MODE FUNCTIONAL DESCRIPTION (continued)

AM Power Delivery

After successfully discovery and classification of a valid PD the power is delivered by controlling the current to the PD until its current requirements are met or until the internal current limit is reached (approximately 650 mA). The power switch is fully enhanced after 500 µs. Figure 5 show the voltage and the current that is being applied to the PD during power-up and reaching the PD load of 250mA.

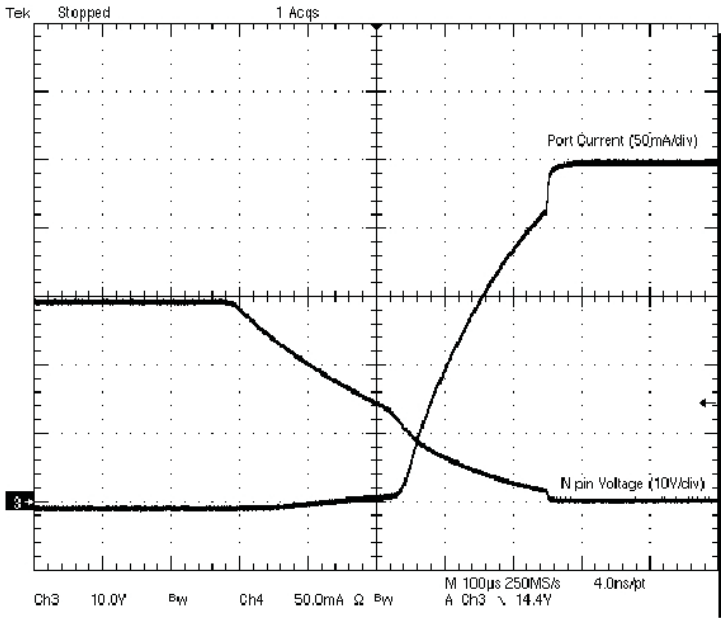


Figure 5.

After power has been applied to the PD the TPS23841 automatically enters the current and voltage sample mode. The sample mode performs 31 current measurements and 1 voltage measurement. Each measurement takes approximately 18 ms to complete. The port remains powered and the current/voltage measurement cycle continues until a fault condition occurs. The current and voltage measurements are both stored in the A/D current and voltage registers and can be accessed through the I^2C pins. This allows power management in the AM if it is desired.

AM Faults and INTB Output

AM faults are:

- Port under and over voltage faults, (if enabled, see Over/Under Voltage Fault section)
- Over current faults
- Under current (DC Disconnect) fault
- Thermal shutdown (TSD) fault
- Watchdog timer faults (disabled via WD_DIS pin)

Any one of the first four fault conditions listed above causes the port to shut down, and a 3-bit fault code to be latched into the affected port's Status Read 1 register (addr = 0100b). Watchdog faults cause all four ports to shut down. Faulted ports are temporarily disabled after a fault has been detected and latched.

The INTB pin is an open-drain, active-low output which is asserted if a fault condition occurs on any of the four ports. This indication is asserted for any of the port faults which result in a code displayed in the port status register (the faults listed in Table 8). In automode, the fault latch, the status register fault bits, and consequently, INTB assertion, are cleared by expiration of the 750-ms TED timer.

AUTO MODE FUNCTIONAL DESCRIPTION (continued)

Over/Under Voltage Fault

For the TPS23841, port over and undervoltge detection is disabled by default after device POR. This continuous voltage monitoring feature can subsequently be enabled by writing a logic 1 to bit D2 in the Common Control register, assuming usage under the direction of a higher level controller, (i.e., usage in semi-auto mode).

Over/under voltage faults are only processed after port power up has completed (voltage/power ramp to PD is done). The TPS23841 measures the voltage between the P and N pin and if this voltage drops below the under voltage threshold (typically 43 V) or increases above the over voltage threshold (typically 55 V) the voltage timer is turned on. When the voltage timer reaches its time-out limit that is set between 2 ms to 5 ms the corresponding port is turned off and the UV/OV fault code generated in the Port Status 1 register. If the over/under voltage condition is removed prior to the voltage timer reaching its limit the timer is reset and waits for the next event. Figure 6 shows a voltage fault lasting for more then 2 ms that has caused the port to shutdown.

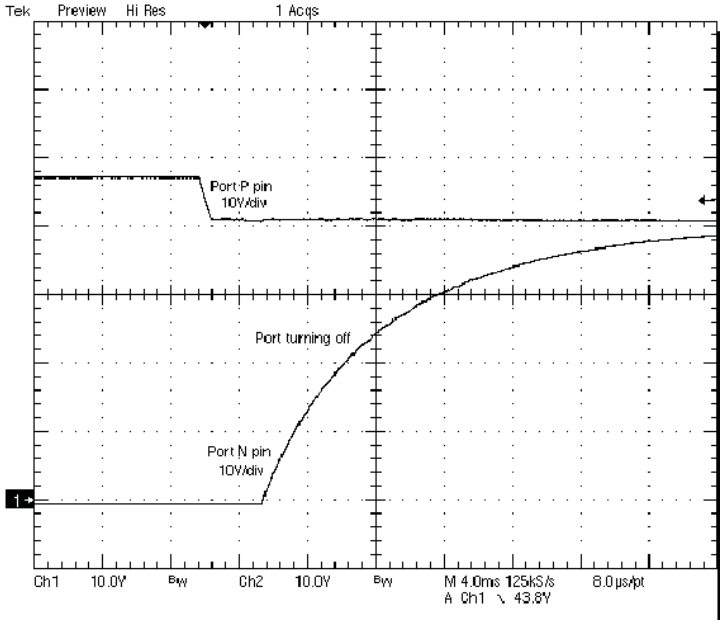


Figure 6.

AUTO MODE FUNCTIONAL DESCRIPTION (continued)

Over Current or Current Limit Faults

Over current or current limit faults are conditions when the load current that is being sensed trips either the I_{CUT} comparator (570 mA to 665 mA) or the I_{LIM} comparator (600 mA to 700 mA) and turns on the current fault timer. When the over current timer reaches its time out limit that is set between 50 ms to 75 ms the corresponding port is turned off and the over current fault code generated in the Port Status 1 register. If the over current condition goes away prior to the over current timer reaching its limit the timer is reset and waits for the next event. Figure 7 shows an over current fault lasting more than 50 ms that has caused the port to shut off.

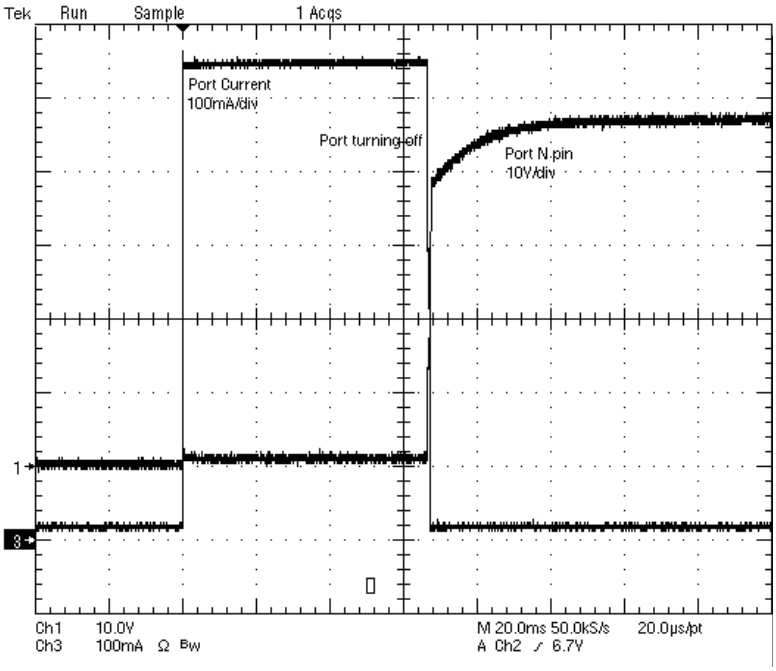


Figure 7.

AUTO MODE FUNCTIONAL DESCRIPTION (continued)

Under Current Fault (DC Modulated Disconnect)

Under current fault (dc modulated disconnect) is a condition when the load current that is being measured drops below 7.5mA and turns on the disconnect timer. If the disconnect timer reaches its time out limit that is set between 300ms to 400ms the corresponding port is turned off and the load disconnect fault code generated in the Port Status 1 register. If the under current condition goes away prior to the disconnect timer reaching its limit the timer is reset and the port remains powered.

Figure 8 shows DC Disconnect event. In this setup the load current was set right above the 7.5mA threshold. The duty cycle of the load was then adjusted until the off period exceeded the disconnect time out, causing turn-off of the port. The time-out period was > 300 ms.

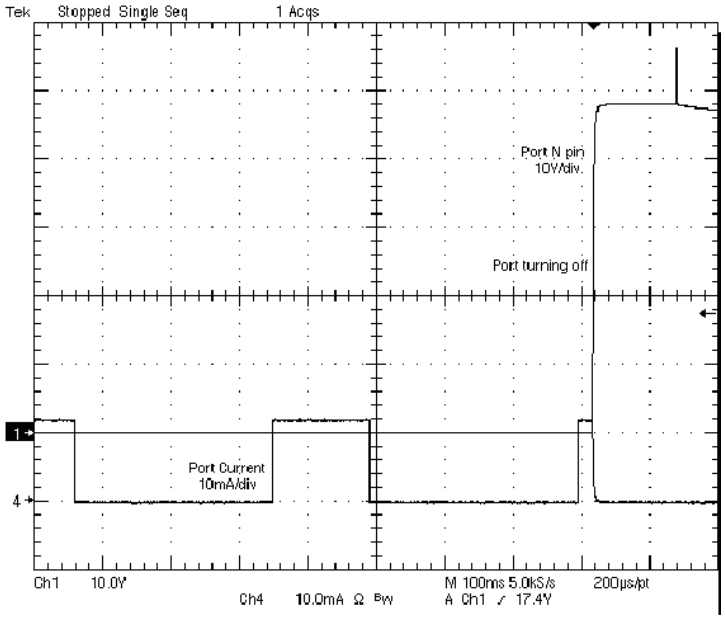


Figure 8.

POWER MANAGEMENT MODE FUNCTIONAL DESCRIPTION

Power Management Mode (PMM)

Power management mode (PMM) has been designed to work efficiently with simple low-cost microcontrollers such as those in the MSP430 family.

The power management mode uses 13 self-contained functions to completely control the device operation. You simply write/read through the I^2C pins and wait for the function done bit to be set. If an A/D measurement was performed during the function the results can be accessed by going to the read mode and addressing the proper register.

13 Funcitons

- **Disable:** Disable the port and reset all functions.
- **Discovery 1:** Enable the Discovery 1 condition which applies a 4.4 V across the PD and measure and store the resulting current.
- **Discovery 2:** Enable the Discovery 2 condition which applies a 8.8 V across the PD and measure and store the resulting current.
- **V Sample:** Measure the voltage between the P and N pins and store the result in the A/D voltage register.
- **Legacy:** Enable the 3.5-mA current source formeasuring capacitance and measure the voltage across the P and N terminals and store the result in the A/D voltage register.
- **Classify:** Enable the classification condition which applies 17.7 V across the PD and measure and store the resulting current.
- **Rup Pwr:** Turn on the output switch while controlling the current being delivered to the PD until the PD current needs are met or the max current is reached.
- **C Sample:** Continuous cycle of 31 current measurements and 1 voltage measurement. After each measurement the contents of the appropriate register are updated.
- **Rdwn:** Turn off the output switch while controlling current until output current reaches 0 mA.
- **AC LO:** Turns on low side output FET and measures voltage between P and N pin and store result in A/D voltage registers.
- **AC HI:** Turns on high side output FET and measures voltage between P and N pin and store result in A/D voltage registers.
- **ISample:** Measure the current and store the result in the A/D current register.
- **TSample:** Measure the internal die temperature and store the result in the A/D temperature register.

  Conversion times for A/D measurements performed as part of the functions listed above are generally as shown in the typical values in the Electrical Characteristics table. However, conversion time is somewhat dependant on the magnitude of the input signal being measured. Power management mode applications should take precautions to test the A/D DONE bit (MSB of the high byte) of the pertinent results register before accepting or using the returned value. A logic 1 at this bit location indicates the conversion is complete. Also, once an A/D conversion is in process on a given port, subsequent function calls to that port should wait until the currently executing conversion is complete. Commands written prior to completion may cause the results of the initial conversion to be written to the register of the subsequent function.

POWER MANAGEMENT MODE FUNCTIONAL DESCRIPTION (continued)

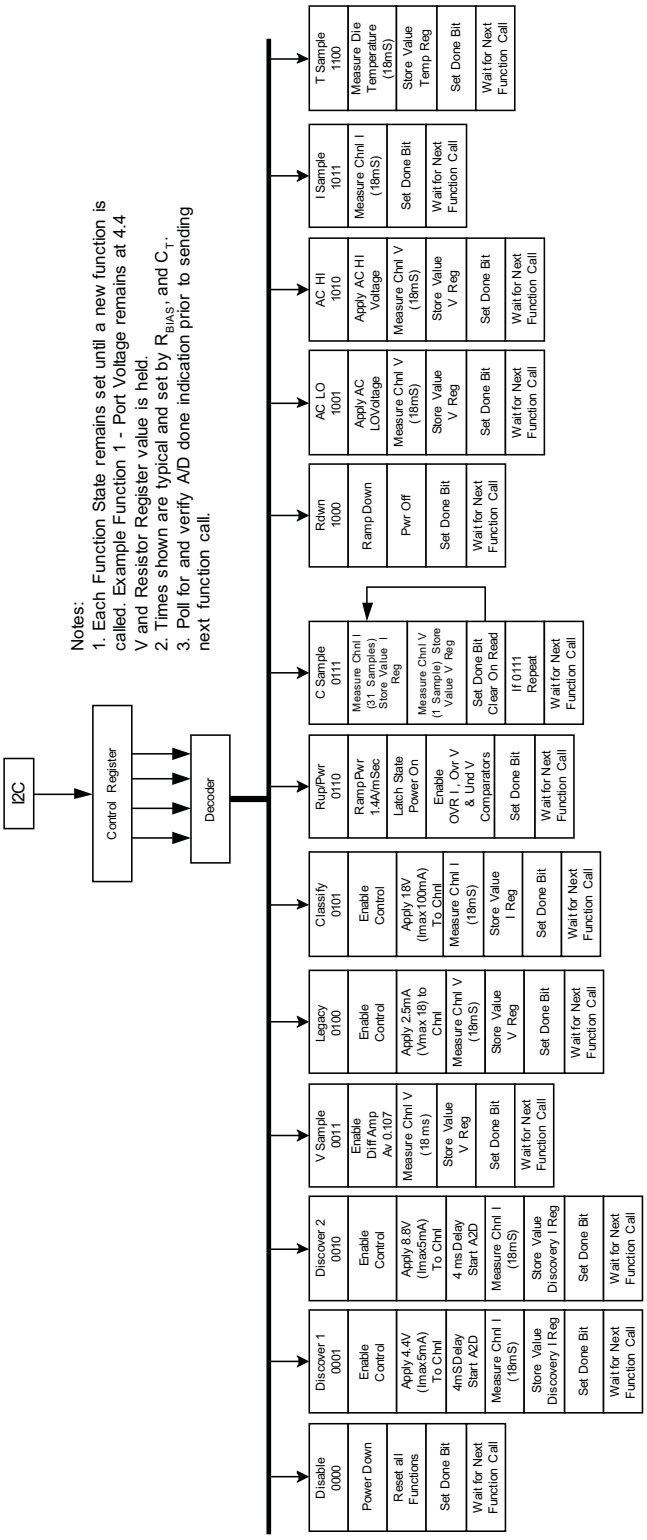


Figure 9.

POWER MANAGEMENT MODE FUNCTIONAL DESCRIPTION (continued)

PMM Discovery 1

PMM Discovery 1 function waveforms for the N and CINT pins are shown in Figure 10. The measurement is being performed using 25 kΩ impedance between the P and N pin. The Discovery 1 voltage is allowed to settle for approximately 5ms before the A/D begins integrating. The voltage on the CINT pin shows the A/D cycle. There are four distinct regions to any A/D cycle: pre-charge (to a known starting voltage), charge, coarse discharge, and fine discharge. CINT pin is very high impedance therefore extreme care must be taken to avoid any noise or leakage affecting this pin. For the measurements where CINT voltage is shown a buffer was used to prevent performance degradation. The A/D measurement time is approximately 18ms. The entire Discovery 1 function takes approximately 22 ms to complete. At the end of the A/D cycle the Discovery 1 current is stored in the Discovery Current Register and the function done bit is set. The applied Discovery 1 voltage level remains until a new function is called. The data for this measurement will remain stored in the Discovery Current Register until another Discovery 1 or 2 function is called.

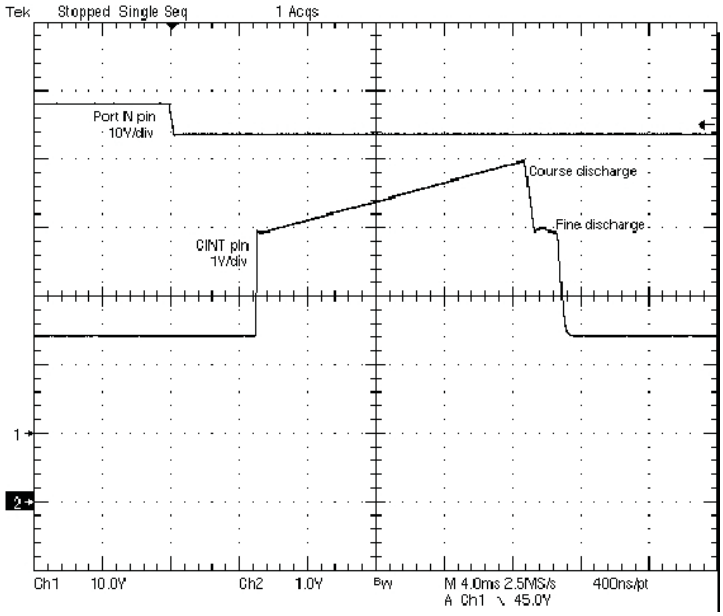


Figure 10.

POWER MANAGEMENT MODE FUNCTIONAL DESCRIPTION (continued)

PMM Discovery 2

PMM Discovery 2 function waveforms for the N and CINT pins are shown in Figure 11. Again the measurement is being performed using 25 kΩ impedance between the P and N pin. The Discovery 2 function was called after a Discovery 1 function so the voltage ramps from 4.4 V to 8.8 V below the P pin. The Discovery 2 voltage is given 5 ms to settle before the A/D begins to integrate. At the end of the A/D cycle the Discovery 2 current is stored in the Port Discovery Current Register and the function done bit is set. The applied Discovery 2 voltage level will remain until a new function is called. The data for this measurement will remain stored in the Discovery Current Register until another Discovery 1 or 2 function is called.

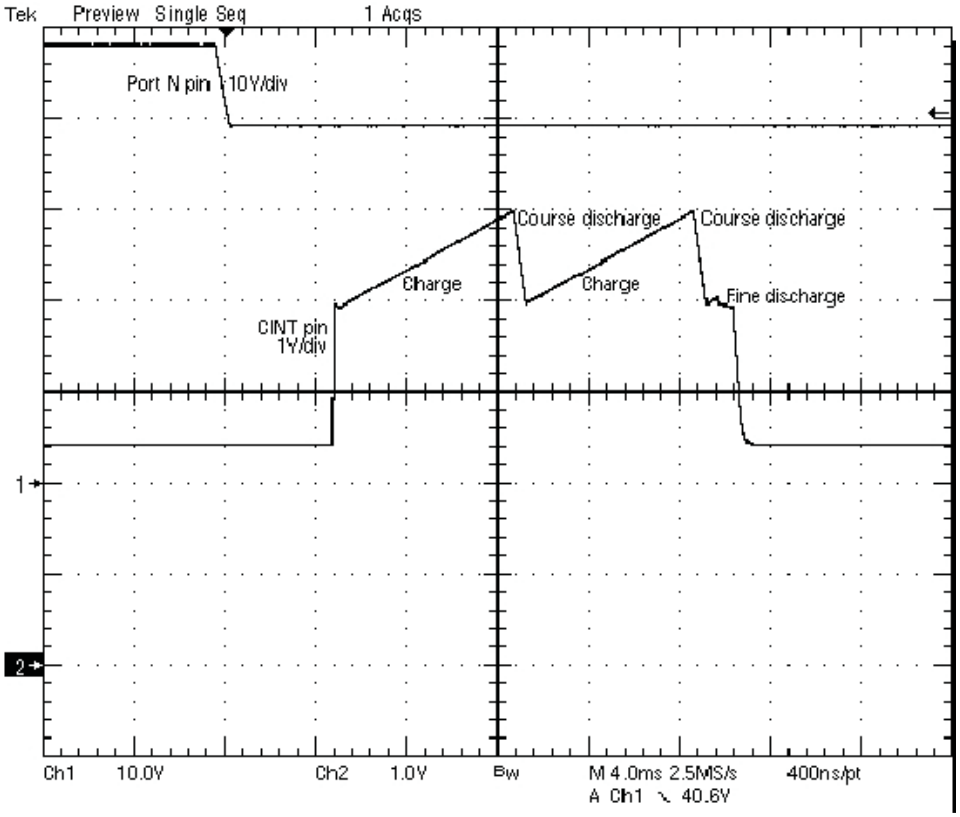


Figure 11.

PMM Classification

PMM Classification function looks similar to Discovery 1 and 2 except that the voltage between the P and N pins regulates to approximately 17.5 V. At the end of the A/D cycle the classification current is stored in the Port Current Register and the done bit is set. The applied classification level will remain until a new function is called. The data for this measurement remains stored in the Port Current Register until either the Classify or ISample function is called.

As indicated in the flow diagram of Figure 1, the TPS23841 in AM only performs classification at one port at a time. Similarly, PMM applications should take care to ensure that only one port per device is put into the classification mode at any one time to limit power dissipation in the package.

POWER MANAGEMENT MODE FUNCTIONAL DESCRIPTION (continued)

PMM Legacy

PMM Legacy function is used to detect PDs that are non compliant. Legacy detection uses a current source (typically 3.5 mA) as a test current while the A/D measures the average voltage for approximately 18 ms. The waveform shown in Figure 12 is the Legacy function charging a 10-µF capacitor. The capacitance charges to a value that is no greater than 20V below the P port voltage. As the capacitor is charging the A/D is accumulating counts in the voltage A/D register. Figure 13 shows the relationship between port capacitance and the number of counts. A user can characterize non-compliant PD's signatures and use the Legacy function to recognize these devices.

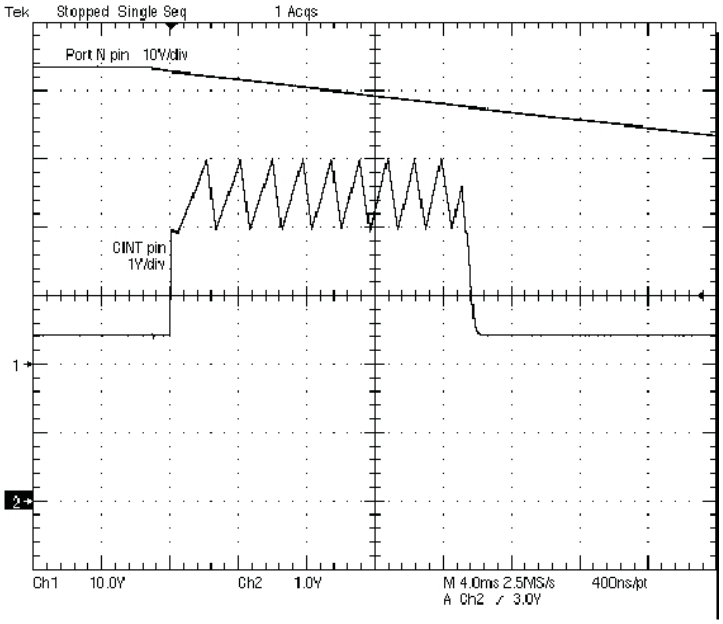


Figure 12.

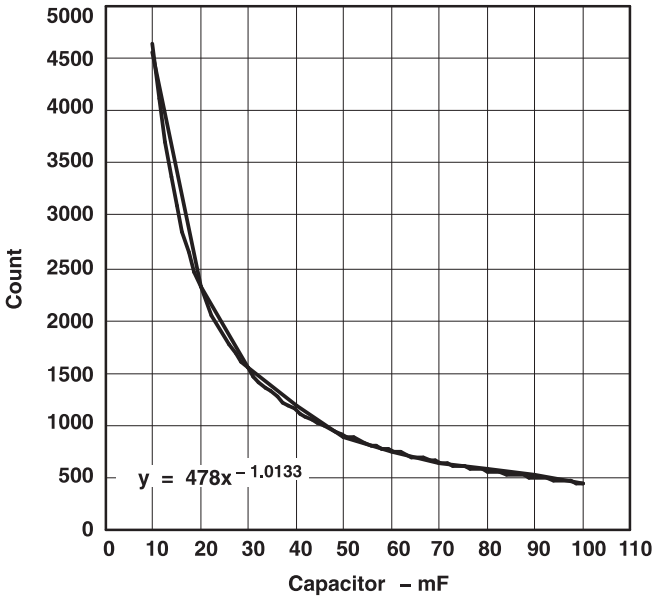


Figure 13.

POWER MANAGEMENT MODE FUNCTIONAL DESCRIPTION (continued)

PMM Rup Pwr

PMM Rup Pwr function turns on the port power by ramping up the current that is being delivered to the load in a controlled fashion. The output current ramps from 0 mA to I_{LIM} (typically 650 mA) in approximately 500 µs. Figure 14 shows the output voltage and current turning on for a 250-mA load.

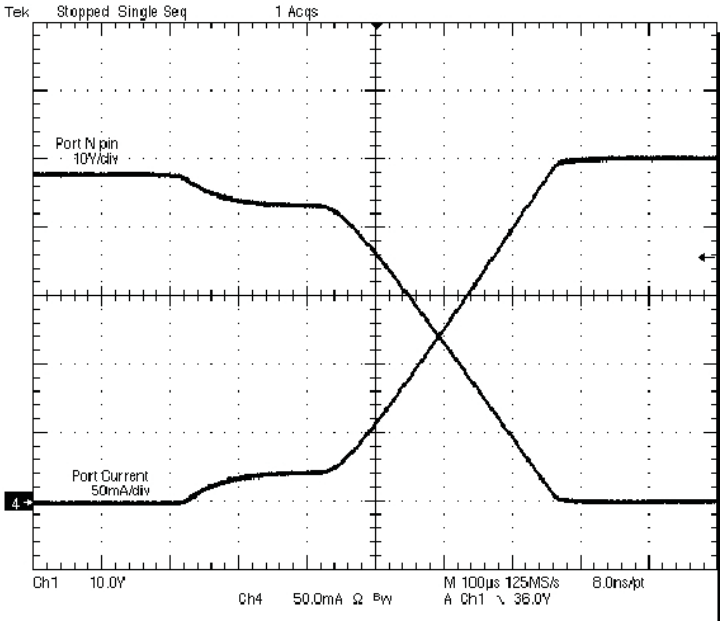


Figure 14.

PMM R_{DWN}

PMM R_{DWN} function turns off the port power by ramping down the current in a controlled fashion. The output current ramps from I_{LIM} (typically 650 mA) to 0mA in approximately 300µs. Figure 15 shows the output voltage and current shutting down for a 250-mA load.

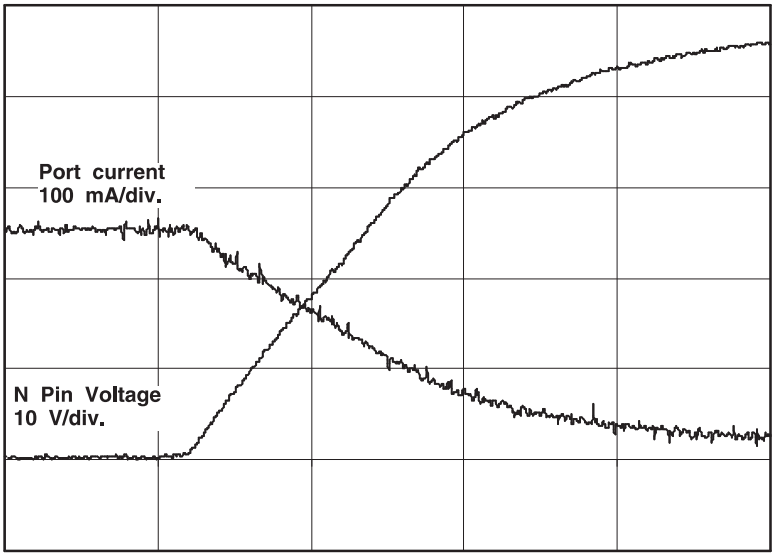


Figure 15.

POWER MANAGEMENT MODE FUNCTIONAL DESCRIPTION (continued)

Miscellaneous Functional Description

PMM Faults

PMM faults are the same as those shown in the AM Faults and INTB Output section. In PM mode, the port under- and over voltage and under-current faults can be enabled or disabled by writing to the control bits in the appropriate register. For the TPS23841, port under- and overvoltage detection is disabled by default after device POR or other reset operation. Under current detection, (DC Disconnect), is enabled by default. The enable state of these features can be toggled by writing to the corresponding control bit as defined in Table 5 andTable 6.

The PMM faults are:

- Port under- and over-voltage faults (enable/disable via Common Control register 0001b, bit D2)
- Overcurrent fault (cannot be disabled)
- Under-current (DC Disconnect) fault (enable/disable via Port Control register 0010b, bit D4)
- Thermal shutdown (TSD) fault (cannot be disabled)
- Watchdog fault (disable via WD_DIS pin)

Any one of these faults causes the port to shutdown. Once a fault has occurred the port can not be repowered until a Disable function is sent. The Disable function clears the fault latch and the fault register.

INTB pin operation is essentially the same in PMM as in AM, with the following exceptions:

- For load under-current to generate a fault shutdown and status indication, the condition of load current less than the threshold must be detected by the continuous sample (C_SAMPLE) function (0111b).
- In PMM only, a Watchdog timer fault also asserts INTB.

Watchdog Timer

TPS23841 has two watchdog timers. One monitors the I^2C clock and the other monitors the internal clock. When automode is selected and the watchdog timer has not been disabled only the internal clock is monitored. When in power management mode and the watchdog timer has not been disabled then both the I^2C and internal clocks are monitored. If there is no I^2C clock activity for approximately two seconds then all ports are disabled. There are three means to enable ports after a I^2C clock fault and they are:

1. Hard power reset
2. PORB pulse
3. Writing a software reset to the Common Control register.

In both auto mode and power management mode if the internal oscillator is lost for more than 20 ms all ports are disabled.

Loss of these signals is considered catastrophic since the system loses its ability to talk to each port. Therefore the watchdog timers disabling all ports protects the system.

This function can be easily over ridden by setting the WD_DIS pin high.

POWER MANAGEMENT MODE FUNCTIONAL DESCRIPTION (continued)

I²C Interface Description

The serial interface used in the TPS23841 is a standard 2-wire I²C slave architecture. The standard SDA line of the I²C architecture is broken out into independent input and output data paths. This feature simplifies earth grounded controller applications that require opto-isolators to keep the 48-V return of the Ethernet power system floating. For applications where opto-isolation is not required, the bidirectional property of the SDA line can be restored by connecting SDA_I to SDA_O. The SCL line is a unidirectional input only line as the TPS23841 is always accessed as a slave device and it never masters the bus.

Data transfers that require a data-flow reversal on the SDA line are 4-byte operations. This occurs during a TPS23841 port read cycle where a slave address byte is sent, followed by a port/register address byte write. A second slave address byte is sent followed by the data byte read using the port/register setup from the second byte in the sequence.

The I²C interface and the port read write registers are held in active reset until all input voltages are within specifications (V10, V6.3, V3.3 and V2.5) and the internal POR timer has timed out (see electrical specifications).

The I²C read cycle consists of the following steps 1 through 14 and is shown in Figure 16:

1. Start Sequence (S)
2. Device address field
3. Write
4. Acknowledge
5. Register/Port address
6. Acknowledge
7. Stop
8. Start
9. Device address field
10. Read
11. Acknowledge
12. Data Transfer
13. Acknowledge
14. Stop

Data write transfers to the TPS23841 do not require a data-flow reversal and as such only a 3-byte operation is required. The sequence in this case would be to send a slave device address byte, followed by a write of the port/register address followed by a write of the data byte for the addressed port.

The I²C write cycle consists of the following steps 1 through 9 and is also shown in Figure 16:

1. Start sequence (S)
2. Device address field
3. Write
4. Acknowledge
5. Register/Port address
6. Acknowledge
7. Data for TPS23841
8. Acknowledge
9. Stop

POWER MANAGEMENT MODE FUNCTIONAL DESCRIPTION (continued)

Start/Stop

The high-to-low transition of SDA_I while SCL is high defines the start condition. The low to high transition of SDA_I while SCL is high defines the stop condition. The master device initiates all start and stop conditions.

The first serial packet is enclosed within start and stop bits, consists of a 7-bit address field, read/write bit, and the acknowledge bit. The acknowledge bit is always generated by the device receiving the address or data field. Five of the seven address bits are used by the TPS23841. The value of the sixth and seventh bit is ignored and not used by the TPS23841.

Chip Address

The address field of the TPS23841 is 8 bits long and contains 5 bits of device address select and a read/write bit as and two spare bits per Table 1. The leading two bits are not used and are reserved for future port expansion. The five device address select bits follow this plan. These bits are compared against the hard-wired state of the corresponding device address select pins (A1–A5). When the field contents are equivalent to the pin logic states, the device is addressed. These bits are followed by LSB bit, which is used to set the read or write condition (1 for read and 0 for write). Following a start condition and an address field, the TPS23841 responds with an acknowledge by pulling the SDA_O line low during the 9th clock cycle if the address field is equivalent to the value programmed by the pins. The SDA_O line remains a stable low while the 9th clock pulse is high.

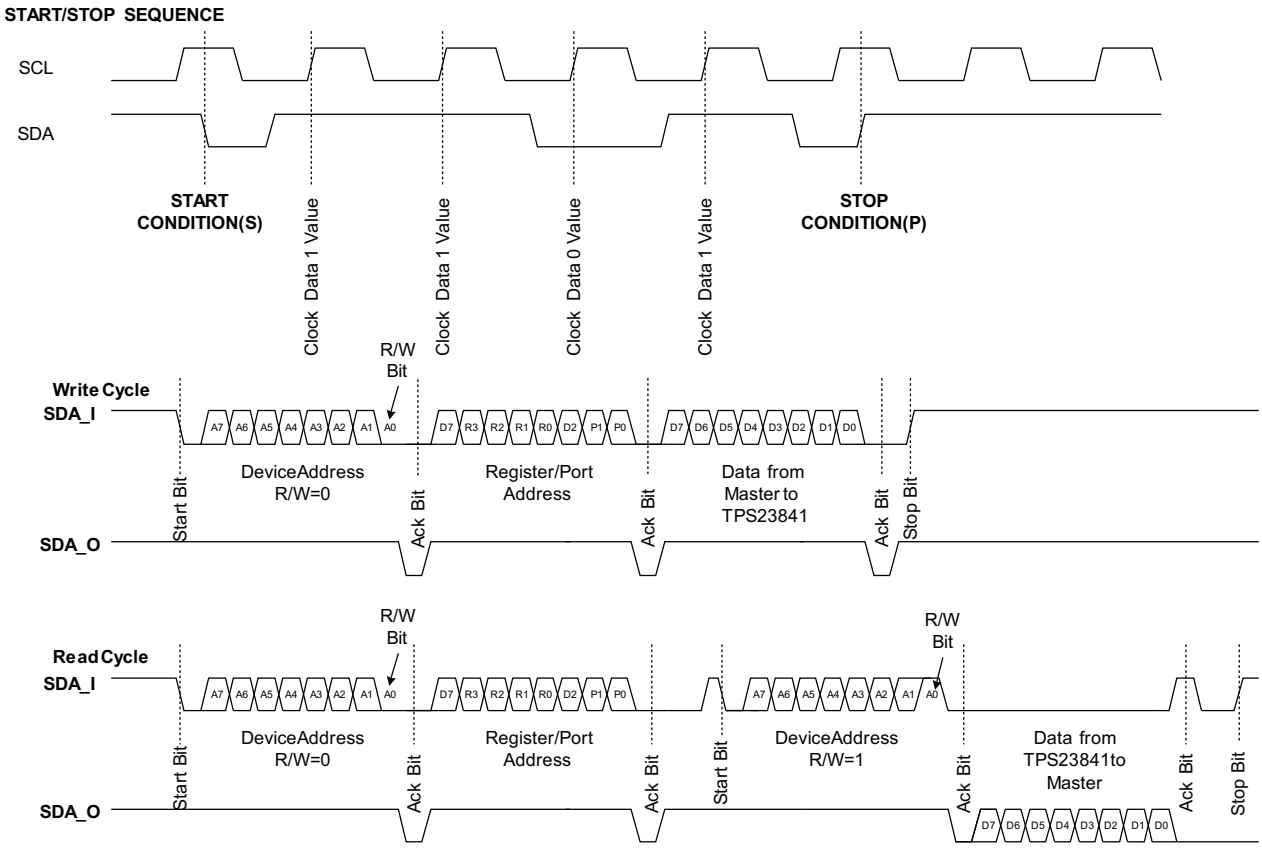


Figure 16. I^{2}C Read/Write Cycles

POWER MANAGEMENT MODE FUNCTIONAL DESCRIPTION (continued)

Chip Addressing

Table 1 shows the bit assignments during the addressing cycle.

Table 1. Address Selection Field

BIT	FUNCTION
A7	Future expansion (value not compared)
A6	Future expansion (value not compared)
A5	Device address. Compared with pin A5
A4	Device address. Compared with pin A4
A3	Device address. Compared with pin A3
A2	Device address. Compared with pin A2
A1	Device address LSB. Compared with pin A1
A0	Read/Write

Port/Register Cycle

After the chip address cycle, the TPS23841 accepts eight bits of port/register select data as defined in Table 2. The SCL line high-to-low transition after the eighth data bit then latches the selection of the appropriate internal register for the follow-on data read or write operation. After latching the eight-bit data field, the TPS23841 pulls the SDA_O line low for one clock cycle, for the acknowledge pulse.

Data Write Cycle

For a data write sequence, after the Port/Register address cycle, the TPS23841 accepts the eight bits of data as defined in the tables below. The data is latched into the previously selected Write Register, and the TPS23841 generates a data acknowledge pulse by pulling the SDA_O line low for one clock cycle. Common register functions act on all ports simultaneously. Per port registers are specific to the target port only.

To reset the interface, the host or master subsequently generates a stop bit by releasing the SDA_I line during the clock-high portion of an SCL pulse.

Data Read Cycles

For a data read sequence, after the register acknowledge bit, the master device generates a stop condition. This is followed by a second start condition, and re-transmitting the device address as described in chip address above. For this cycle, however, the R/W bit is set to a 1 to signal the read operation. The TPS23841 again responds with an acknowledge pulse. The address acknowledge is then followed by sequentially presenting each of the eight data bits on the SDA_O line (MSB first), to be read by the host device on the rising edges of SCL. After eight bits are transmitted, the host acknowledges by pulling the SDA_I line high for one clock pulse. The completed data transfer is terminated with the host generating a stop condition.

Table 2. Register/Port Addressing Map

BIT	FUNCTION	STATE	PRESET STATE
D7	Unused	0	0
D6	Register select MSB	0000 = Common Read - Port fault status, chip ID and rev. 0001 = Common Control Write - Software reset, ports disable and AC Disc. 0010 = Port Control Write 1 - Function calls; misc. fault disables 0011 = Port Control Write 2 - Port enable; A/D control 0100 = Port Status Read 1 - Fault status; device Class info. 0101 = Port Status Read 2 - Function and other status 0110 = Discovery Current - Lower Bits - A/D resistance results 0111 = Discovery Current - Upper Bits - A/D resistance results 1000 = Voltage-Lower Bits - A/D voltage reslts 1001 = Voltage - Upper Bits - A/D voltage results 1010 = Current - Lower Bits - A/D current results 1011 = Current - Upper Bits - A/D current results 1100 = Temperature - Lower Bits - A/D temperature results 1101 = Temperature - Upper Bits - A/D temperature results 1110 = unused 1111 = Common Write - Test mode selections - timer disables, discovery control, etc.	0000
D5	Register select Bit 2		
D4	Register select Bit 1		
D3	Register select LSB		
D2	Unused	0	0
D1	Port address MSB	00 = port 1 01 = port 2 10 = port 3 11 = port 4	00
D0	Port address LSB		

Table 3. Common Read, Register Select = 0000

BIT	FUNCTION	STATE	PRESET STATE
D7	Port 4 general Fault status	0 = no fault 1 = port fault(1)(2)	0
D6	Port 3 general Fault status	0 = no fault 1 = port fault(1) (2)	0
D5	Port 2 general Fault status	0 = no fault 1 = port fault (1) (2)	0
D4	Port 1 general Fault status	0 = no fault 1 = port fault (1) (2)	0
D3	Chip rev	00 = rev – 01 = rev 1 10 = rev 2 11 = rev 3	00
D2			
D1	Chip ID	00 = TPS23841 01= future use 10 = TPS2384 11 = reserved	00
D0			

(1) PMM faults cleared by Disable function.
(2) AM faults cleared by TED timer.

Table 4. Common Write, Register Select = 1111 (Test Register)(1)

BIT	FUNCTION	STATE	PRESET STATE
D7	Unused	0	0
D6	Thermal shutdown test	0 = normal operation 1 = force TSD condition (all ports off)	0
D5	POR disable	0 = normal POR timing 1 = force POR to a non-reset state	0
D4	Discovery timers	0 = normal (4-ms Discovery 1 and Discovery 2) 1 = timers disable	0
D3	Discovery 1 and 2	0 = normal operation 1 = all 4-port Discovery 1 and Discovery 2 – halt	0
D2	DC Disconnect timer	0 = DC Disconnect timer between 300 ms to 400 ms for loads less than 5 mA (IEEE standard) 1 = DC Disconnect timer 0 ms for loads less than 5 mA	0
D1	TED timer	0 = normal operation 1 = 750-ms TED timer disable	0
D0	Unused	0	0

(1) Test mode select; not intended for end--application use.

Table 5. Common Control Write, Register Select = 0001

BIT	FUNCTION	STATE	PRESET STATE
D7	Unused	0	0
D6	Unused	0	0
D5	Thermal shutdown fault(1)	0 = active 1 = disable	0
D4	AC high	0 = off 1 = AC_HI driver on	0
D3	AC low	0 = off 1 = AC_LO driver on	0
D2	Port over/under voltage faults	0 = disable 1 = active	0
D1	All ports disable(2)	0 = normal operation 1 = all ports shut down (no ramp)	0
D0	Software RESET	0 = normal operation 1 = reset all circuits and start a POR timing cycle	0

(1) Register 0001, bit D5 operation inhibited after device probe.
(2) Consult factory for alternative B, semi-auto mode implementations which write to bit D1.

Table 6. Port Control Write 1, Register Select = 0010 (One Per Port)

BIT	FUNCTION	STATE	PRESET STATE
D7	Unused	0	0
D6	Unused	0	0
D5	Discovery fault disable	0 = normal operation 1 = disable internal discovery fault limits (19 kΩ to 29.5 kΩ)	0
D4	DC Disconnect disable	0 = DC Disconnect active 1 = DC Disconnect disable (for AC Disconnect)	0
D3	Function Bit 3	0000 = Disable function (power down and reset all functions) 0001 = Discovery 1 function 0010 = Discovery 2 function 0011 = port voltage sample function (V sample) 0100 = legacy detection function 0101 = classification function 0110 = ramp up/power function (rup pwr) 0111 = continuous sample function C Sample) 1000 = ramp power down function R_{DWN}) 1001 = ac low 1010 = ac high 1011 = port current sample function (I sample) 1100 = die temperature sample function (T sample) 1101 = spare 1110 = spare 1111 = spare	0000
D2	Function Bit 2		
D1	Function Bit 1		
D0	Function Bit 0		

Table 7. Port Control Write 2, Register Select = 0011 (One Per Port)

BIT	FUNCTION	STATE	PRESET STATE
D7	Unused	0	0
D6	Unused	0	0
D5	Unused	0	0
D4	Port Enable(1)	0 = normal 1 = port disable	0
D3	A/D Start	0 = normal 1 = start A/D (self clearing)	0
D2	A/D Abort	0 = normal 1 = abort	0
D1	Unused	0	0
D0	Unused	0	0

(1) Consult factory for alternative B, semi-auto mode implementations which write to bit D4.

Table 8. Port Status Read 1, Register Select = 0100 (One Per Port)

BIT	FUNCTION	STATE	PRESET STATE
D7	Discovery Status	0 = normal 1 = discovery fail	0
D6	Function Done Bit	0 = normal 1 = function complete (self clearing by a new function write)	0
D5	Port Class	000 = class 0 001 = class 1 010 = class 2 011 = class 3 100 = class 4	000
D4	Port Class		
D3	Port Class		
D2	Fault status (MSB)	000 = no faults 001 = UV/OV fault 010 = thermal shutdown fault (TSD) 011 = overload current > 50-ms fault 100 = load disconnect 101 = reserved for future 110 = reserved for future 111 = reserved for future	000
D1	Fault status		
D0	Fault status (LSB)		

Table 9. Port Status Read 2, Register Select = 0101 (One Per Port)

BIT	FUNCTION	STATE	PRESET STATE
D7	Unused	0	0
D6	Unused	0	0
D5	Unused	0	0
D4	Watch dog timer	0 = not active 1 = active	0
D3	A/D status	0 = not active 1 = active (conversion in process)	0
D2	Function status (MSB)	000 = disabled 001 = searching 010 = power delivery 011 = fault 100 = test 101 = other fault 110 = undefined 111 = undefined	000
D1	Function status		
D0	Function status (LSB)		

A/D Results Registers (Discovery Current, Voltage, Current and Temperature)

Table 10. Discovery Current — Lower Bits, Register Select = 0110 (One Per Port)

BIT	FUNCTION	STATE	PRESET STATE
D7	A/D bit 7	A/D lower bits	0
D6	A/D bit 6		
D5	A/D bit 5		
D4	A/D bit 4		
D3	A/D bit 3		
D2	A/D bit 2		
D1	A/D bit 1		
D0	A/D bit 0		

Table 11. Discovery Current — Upper Bits, Register Select = 0111 (One Per Port)

BIT	FUNCTION	STATE	PRESET STATE
D7	Resistor measurement complete	0 = measurement active (bit set low at the start of Discovery 1 or Discovery 2) 1 = measurement complete (bit set high after A/D is completed during Discovery 1 or Discovery 2)	0
D6	A/D bit 14	A/D upper bits	0
D5	A/D bit 13		
D4	A/D bit 12		
D3	A/D bit 11		
D2	A/D bit 10		
D1	A/D bit 9		
D0	A/D bit 8		

Table 12. Voltage — Lower Bits, Register Select = 1000 (One Per Port)

BIT	FUNCTION	STATE	PRESET STATE
D7	A/D bit 7	A/D lower bits	0
D6	A/D bit 6		
D5	A/D bit 5		
D4	A/D bit 4		
D3	A/D bit 3		
D2	A/D bit 2		
D1	A/D bit 1		
D0	A/D bit 0		

Table 13. Voltage — Upper Bits, Register Select = 1001 (One Per Port)

BIT	FUNCTION	STATE	PRESET STATE
D7	Voltage measurement complete	0 = measurement active (bit set low when A/D begins a voltage measurement) 1 = measurement complete (bit set high after A/D has completed a voltage measurement)	0
D6	A/D bit 14	A/D upper bits	0
D5	A/D bit 13		
D4	A/D bit 12		
D3	A/D bit 11		
D2	A/D bit 10		
D1	A/D bit 9		
D0	A/D bit 8		

Table 14. Current — Lower Bits, Register Select = 1010 (One Per Port)

BIT	FUNCTION	STATE	PRESET STATE
D7	A/D bit 7	A/D lower bits	0
D6	A/D bit 6		
D5	A/D bit 5		
D4	A/D bit 4		
D3	A/D bit 3		
D2	A/D bit 2		
D1	A/D bit 1		
D0	A/D bit 0		

Table 15. Current — Upper Bits, Register Select = 1011 (One Per Port)

BIT	FUNCTION	STATE	PRESET STATE
D7	Current measurement complete	0 = measurement active (bit set low when A/D begins a current measurement) 1 = measurement complete (bit set high after A/D has completed a current measurement)	0
D6	A/D bit 14	A/D upper bits	0
D5	A/D bit 13		
D4	A/D bit 12		
D3	A/D bit 11		
D2	A/D bit 10		
D1	A/D bit 9		
D0	A/D bit 8		

Table 16. Temperature — Lower Bits, Register Select = 1100 (One Per Port)

BIT	FUNCTION	STATE	PRESET STATE
D7	A/D bit 7	A/D lower bits	0
D6	A/D bit 6		
D5	A/D bit 5		
D4	A/D bit 4		
D3	A/D bit 3		
D2	A/D bit 2		
D1	A/D bit 1		
D0	A/D bit 0		

Table 17. Temperature — Upper Bits, Register Select = 1101 (One Per Port)

BIT	FUNCTION	STATE	PRESET STATE
D7	Temperature measurement complete	0 = measurement active (bit set low when A/D begins a temperature measurement) 1 = measurement complete (bit set high after A/D has completed a temperature measurement)	0
D6	A/D bit 14	A/D upper bits	0
D5	A/D bit 13		
D4	A/D bit 12		
D3	A/D bit 11		
D2	A/D bit 10		
D1	A/D bit 9		
D0	A/D bit 8		

TPS23841 AC Drive Application Schematic

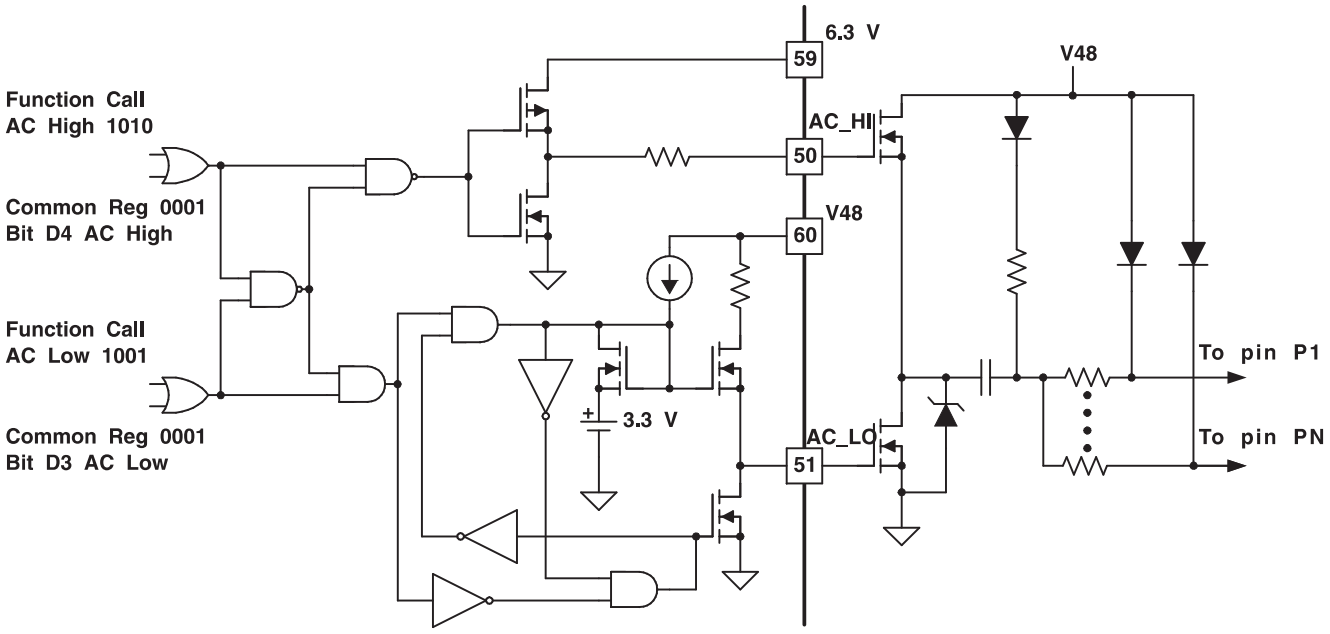
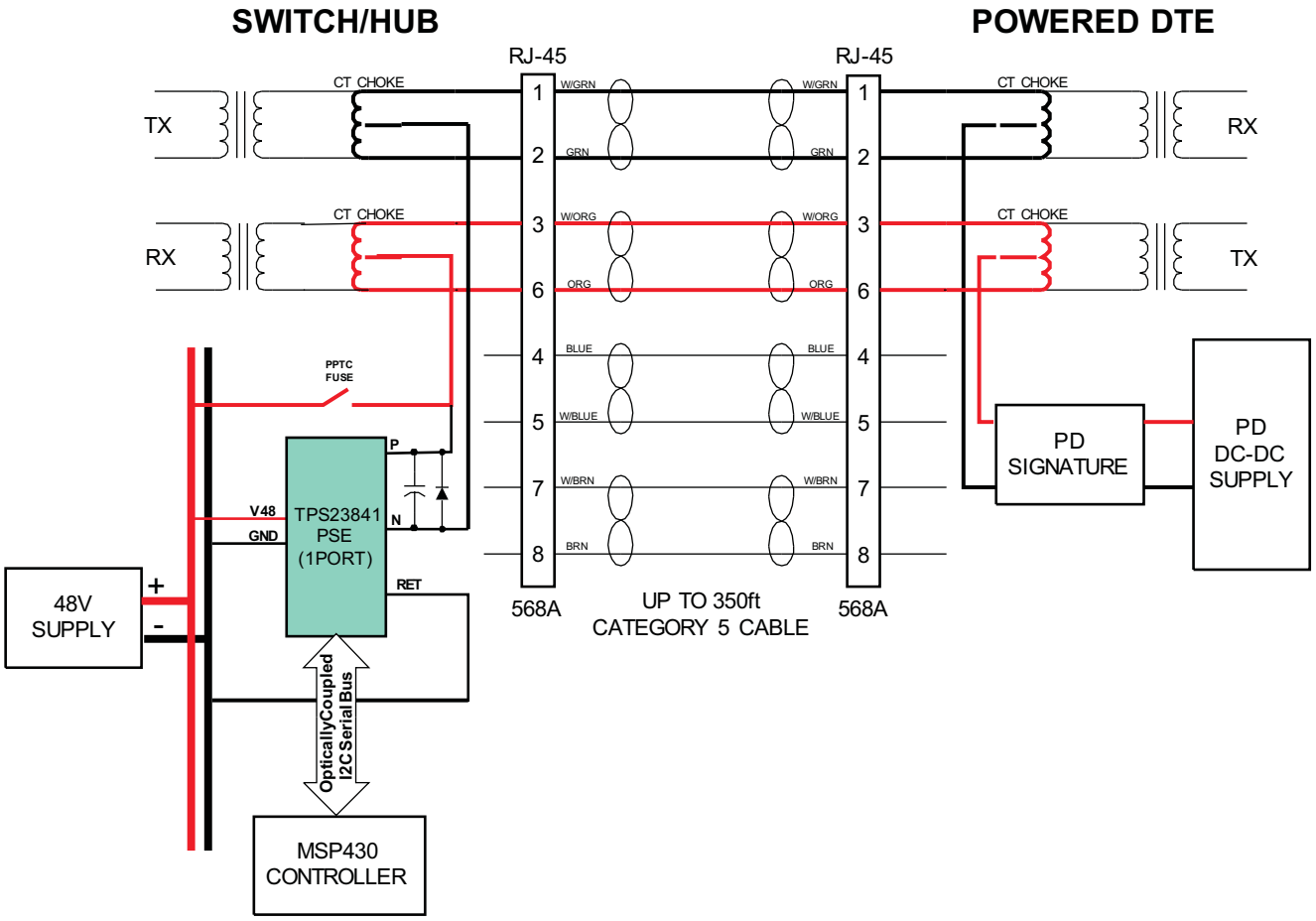


Figure 17. AC_HI and AC_LO With External FET Configuration

TPS23841 System Block Diagram



NOTE: A fuse may be required to provide additional protection if isolation is lost or the low-side current sense fails.

Figure 18.

TPS23841 Basic 4-Port (PMM) Isolated Configuration with AC Disconnect

TPS23841 basic 4-port isolated configuration with AC Disconnect (PAP pinout shown).

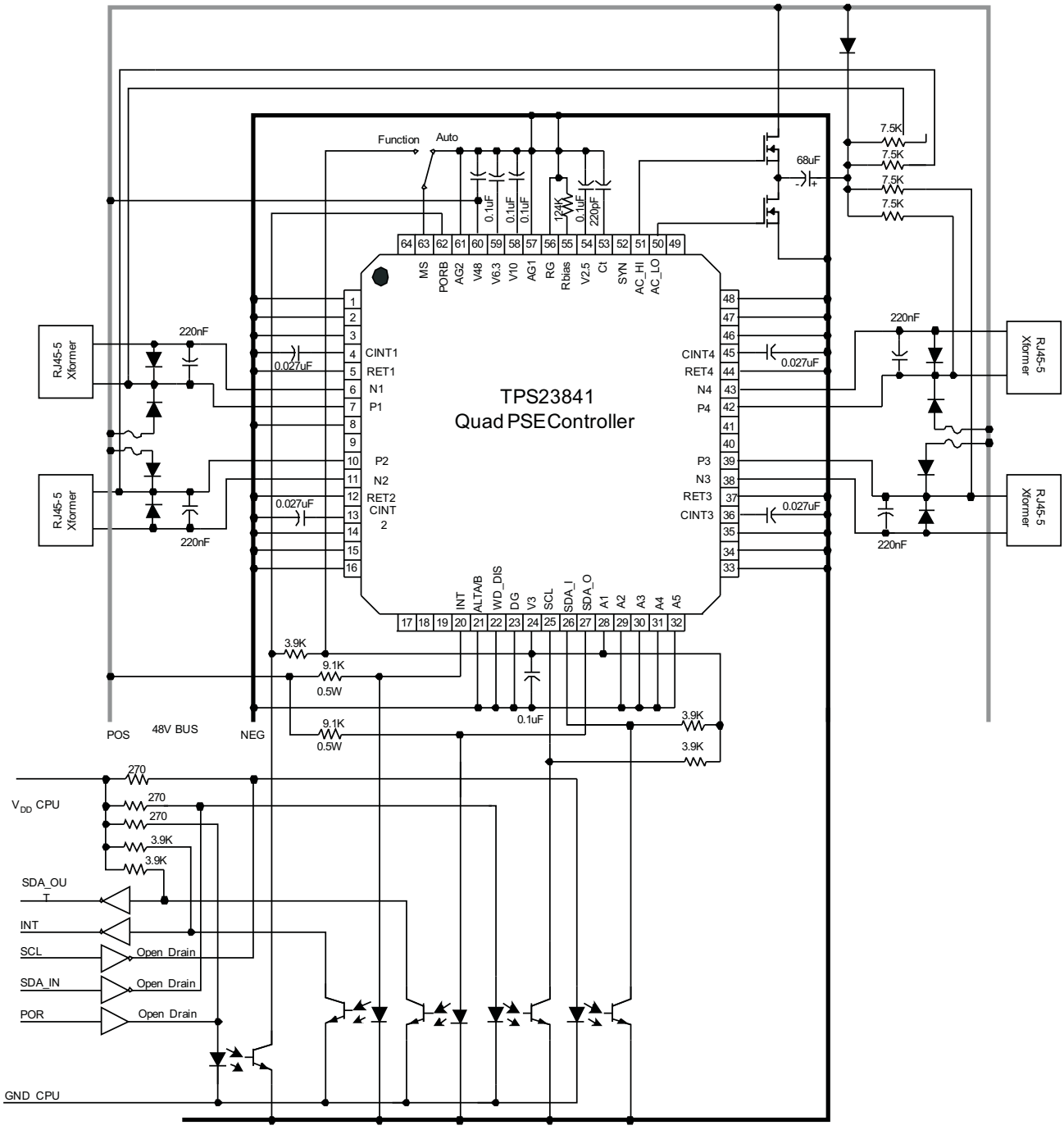
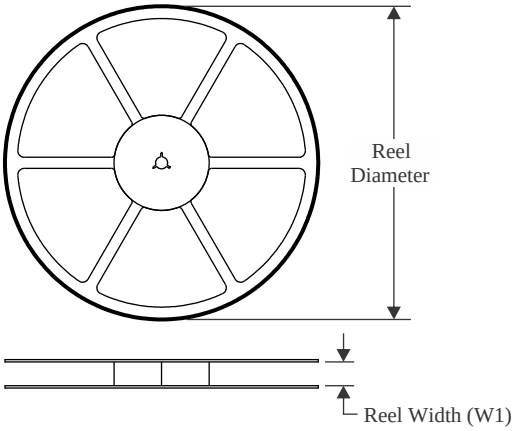


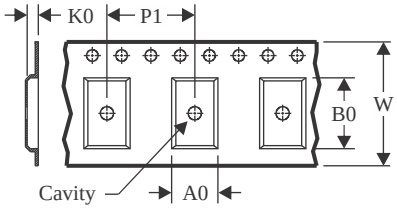
Figure 19.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

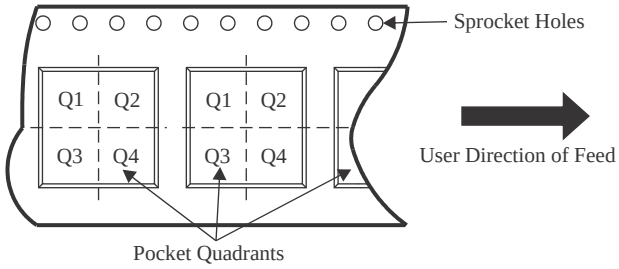


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

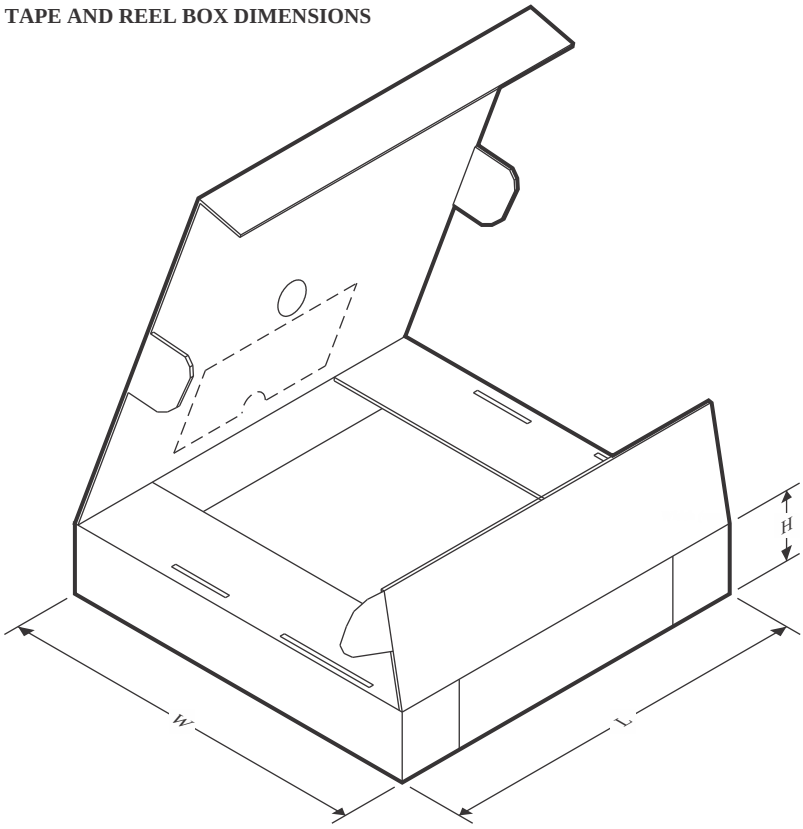
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS23841PAPR	HTQFP	PAP	64	1000	330.0	24.4	13.0	13.0	1.5	16.0	24.0	Q2

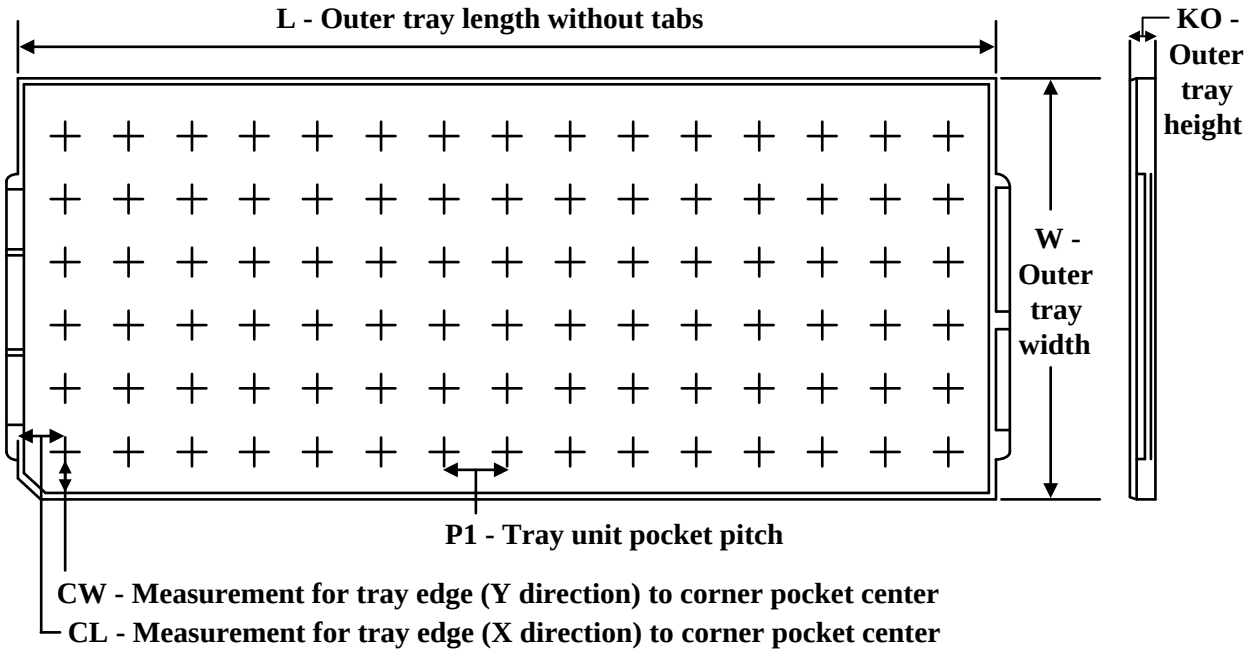
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS23841PAPR	HTQFP	PAP	64	1000	350.0	350.0	43.0

TRAY



Chamfer on Tray corner indicates Pin 1 orientation of packed units.

*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	Unit array matrix	Max temperature (°C)	L (mm)	W (mm)	K0 (µm)	P1 (mm)	CL (mm)	CW (mm)
TPS23841PAP	PAP	HTQFP	64	160	8 x 20	150	315	135.9	7620	15.2	13.1	13
TPS23841PJD	PJD	HTQFP	64	160	8 x 20	150	315	135.9	7620	15.2	13.1	13

GENERIC PACKAGE VIEW

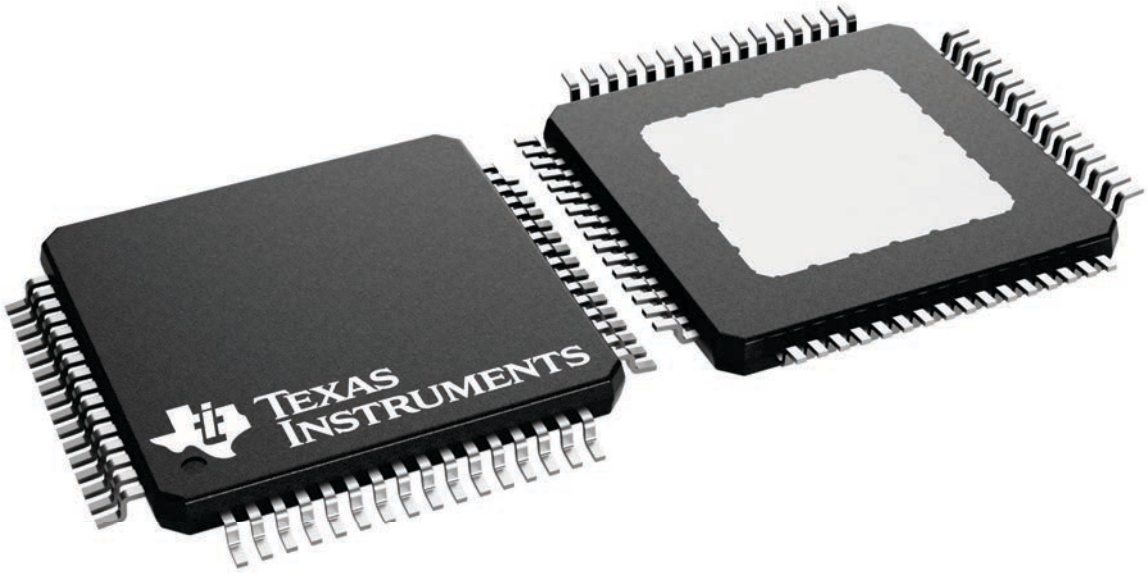
PAP 64

HTQFP - 1.2 mm max height

10 x 10, 0.5 mm pitch

QUAD FLATPACK

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



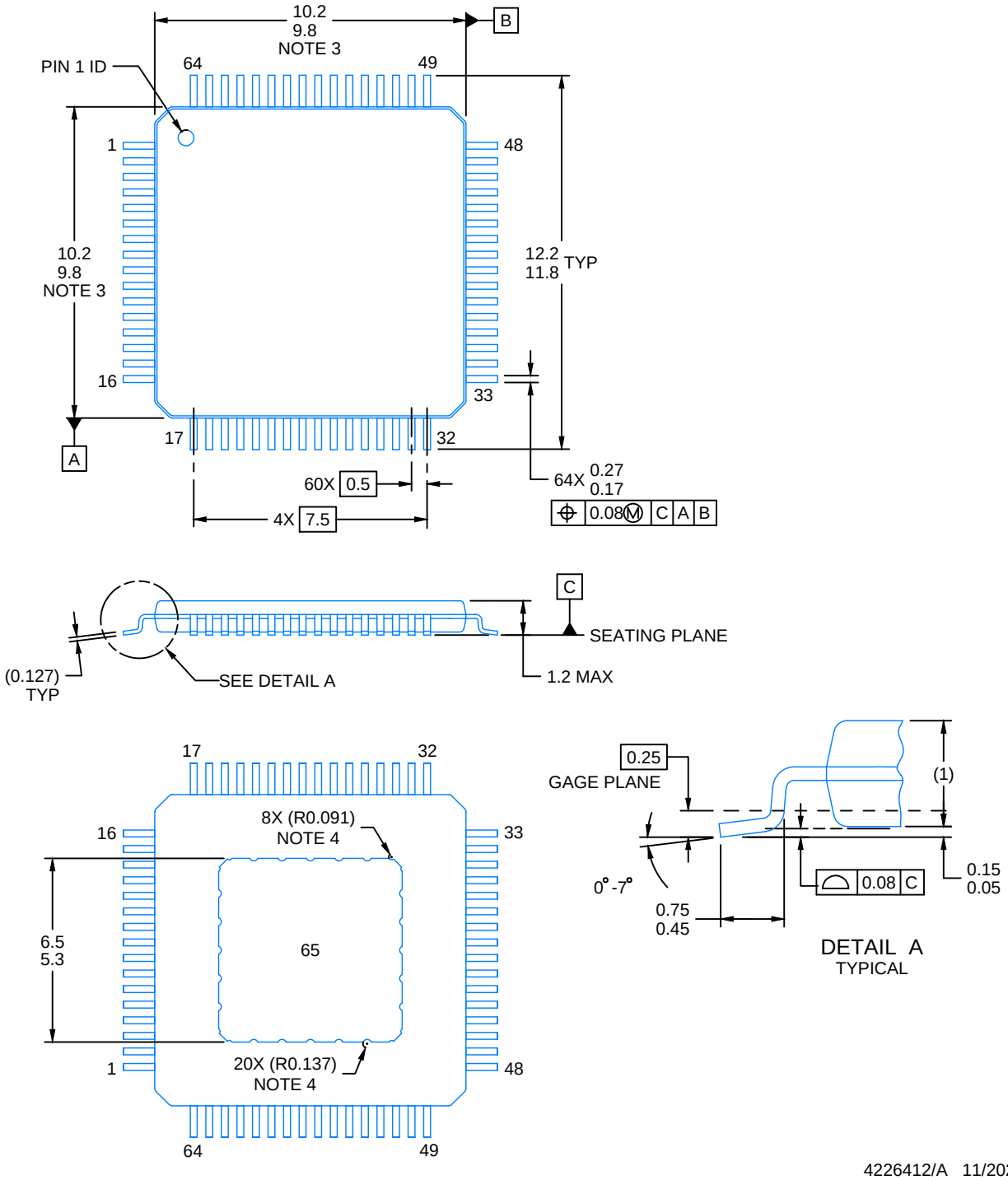
4226442/A

PACKAGE OUTLINE

PAP0064F

PowerPAD™ TQFP - 1.2 mm max height

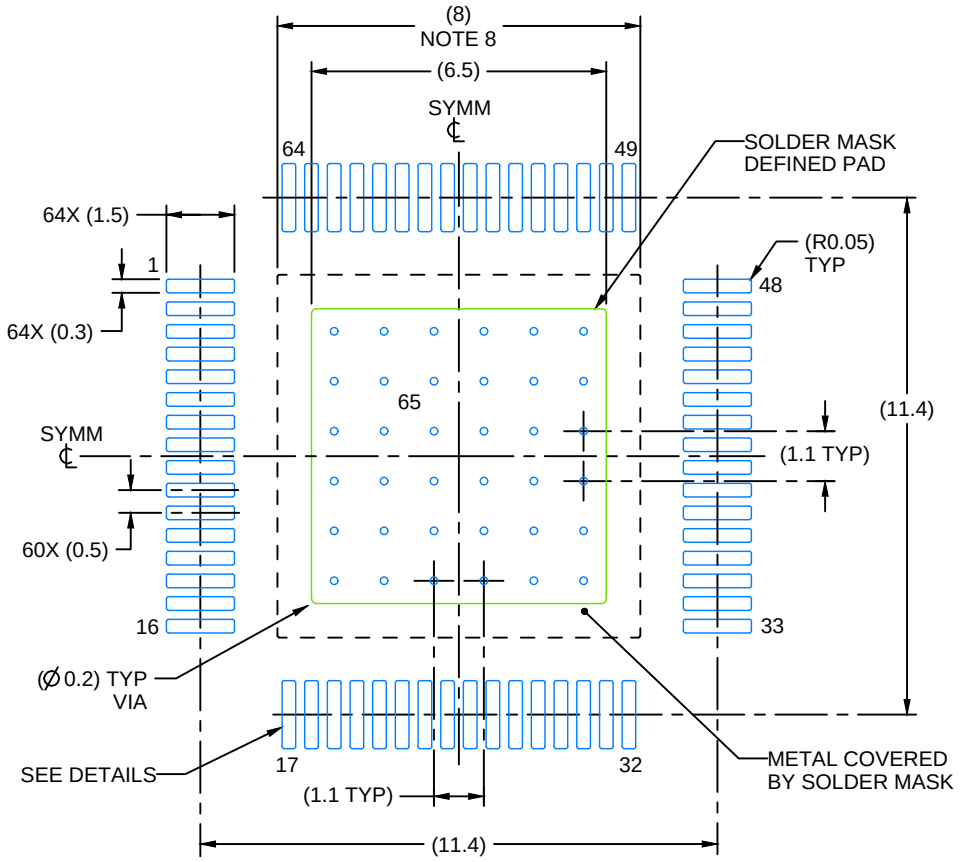
PLASTIC QUAD FLATPACK



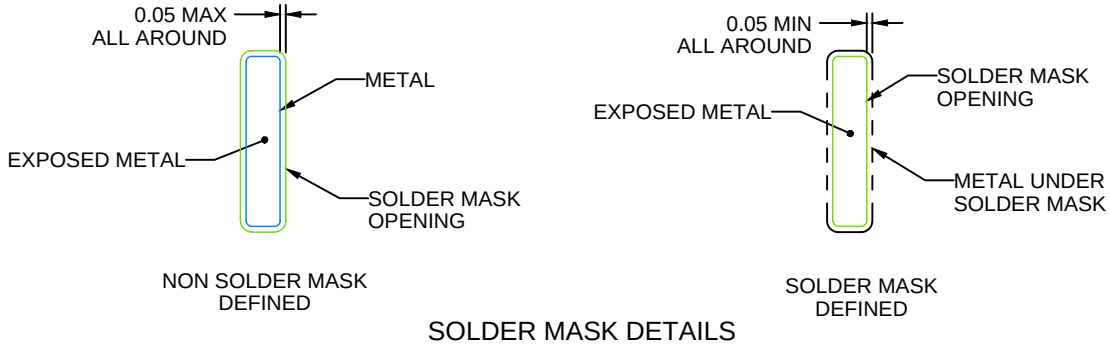
NOTES:

PowerPAD is a trademark of Texas Instruments.

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs.
4. Strap features may not be present.
5. Reference JEDEC registration MS-026.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:6X



NON SOLDER MASK
DEFINED

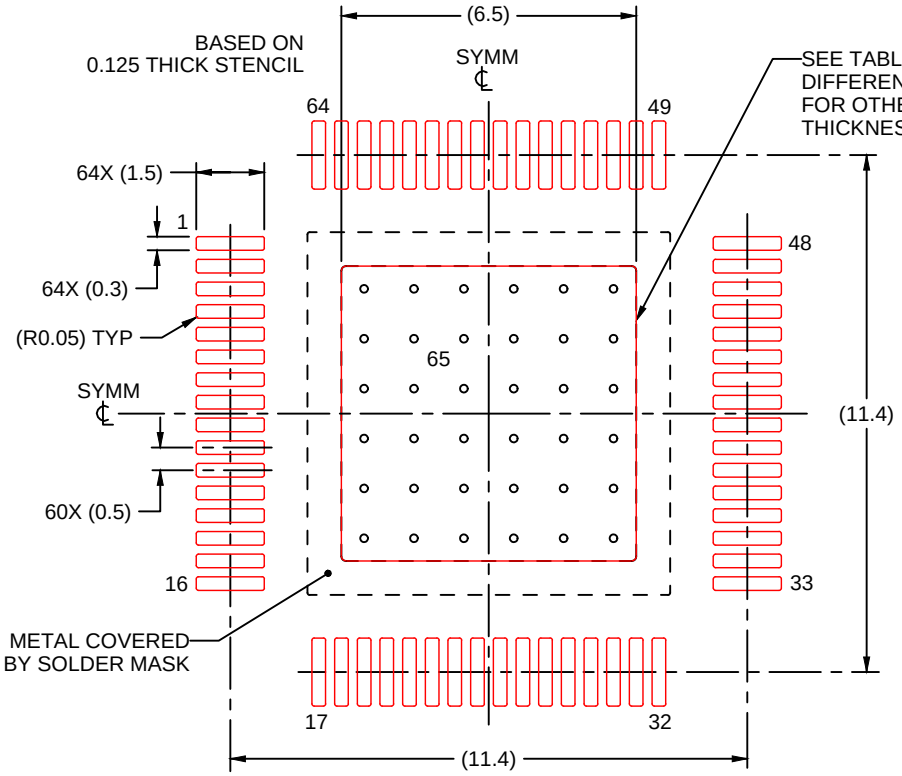
SOLDER MASK
DEFINED

SOLDER MASK DETAILS

4226412/A 11/2020

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
8. This package is designed to be soldered to a thermal pad on the board. See technical brief, Powerpad thermally enhanced package, Texas Instruments Literature No. SLMA002 (www.ti.com/lit/slma002) and SLMA004 (www.ti.com/lit/slma004).
9. Vias are optional depending on application, refer to device data sheet. It is recommended that vias under paste be filled, plugged or tented.
10. Size of metal pad may vary due to creepage requirement.



SOLDER PASTE EXAMPLE
EXPOSED PAD
100% PRINTED SOLDER COVERAGE BY AREA
SCALE:6X

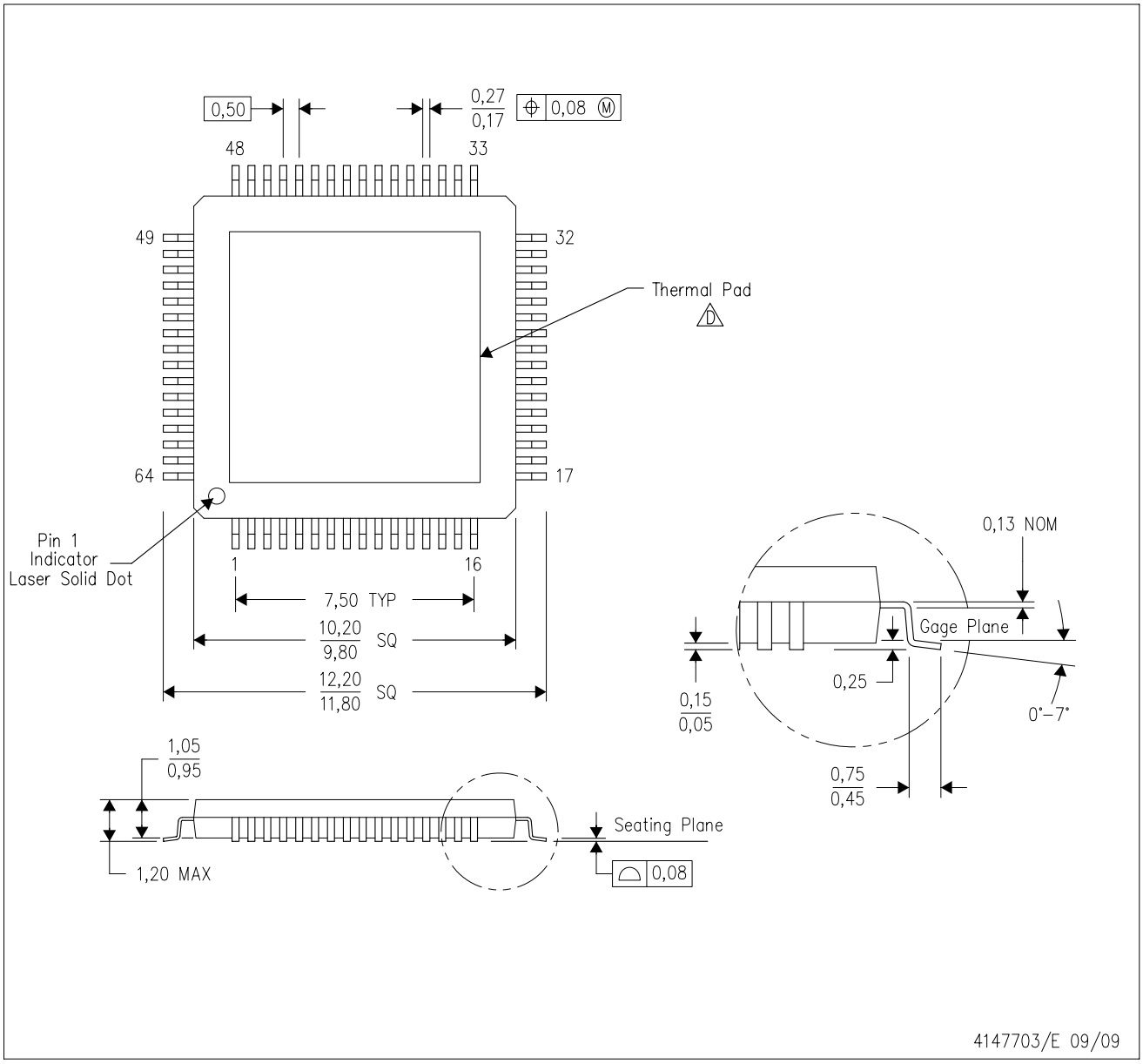
STENCIL THICKNESS	SOLDER STENCIL OPENING
0.1	7.27 X 7.27
0.125	6.5 X 6.5 (SHOWN)
0.15	5.93 X 5.93
0.175	5.49 X 5.49

4226412/A 11/2020

NOTES: (continued)

11. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
12. Board assembly site may have different recommendations for stencil design.

PJD (S–PQFP–G64) PowerPAD™ PLASTIC QUAD FLATPACK (DIE DOWN)



NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion
D. Refer to Technical Brief, PowerPad Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 for information regarding recommended board layout. This document is available at www.ti.com <http://www.ti.com>. See the product data sheet for details regarding the exposed thermal pad dimensions.
E. Falls within JEDEC MS–026

PowerPAD is a trademark of Texas Instruments.

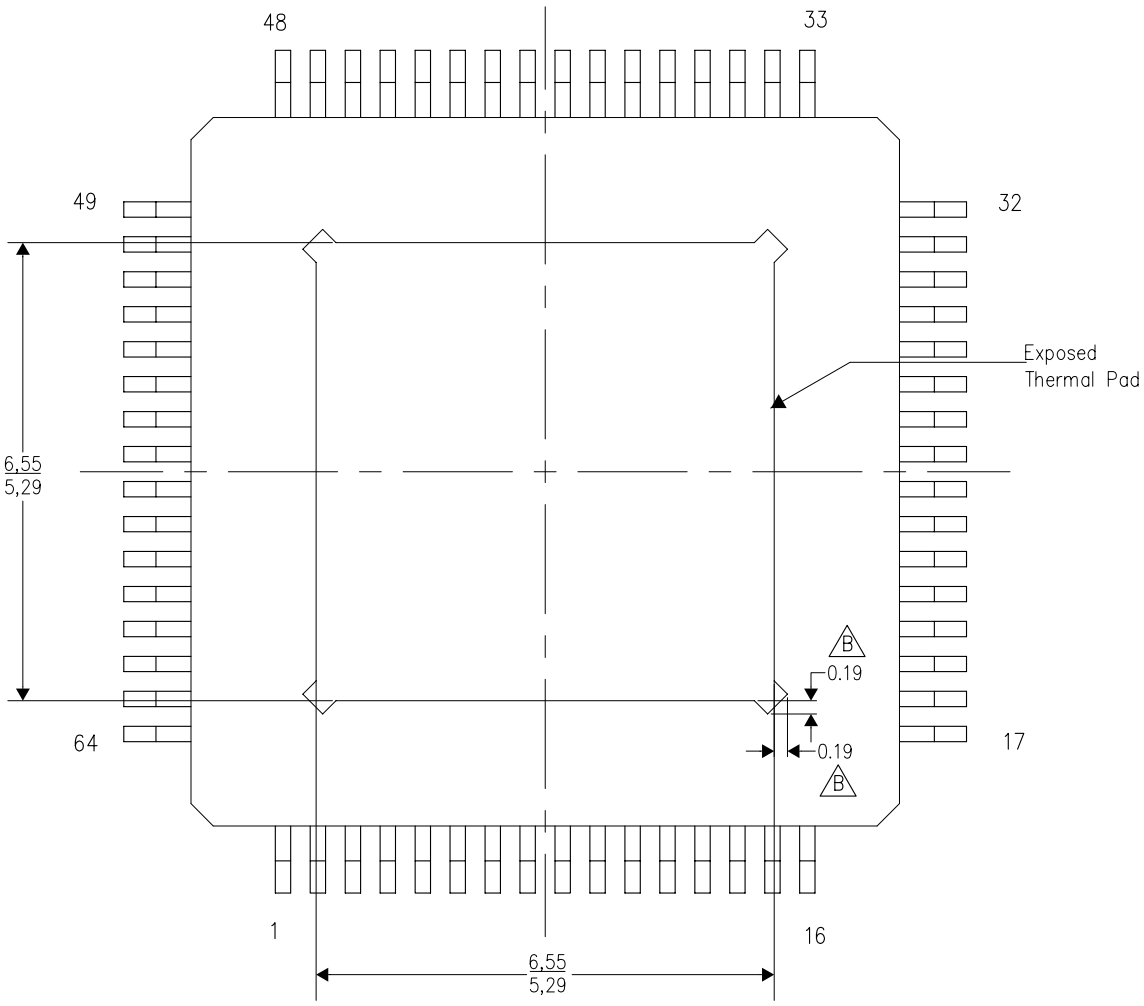
PJD (S–PQFP–G64) PowerPAD™ PLASTIC QUAD FLATPACK

THERMAL INFORMATION

This PowerPAD™ package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. This design optimizes the heat transfer from the integrated circuit (IC).

For additional information on the PowerPAD package and how to take advantage of its heat dissipating abilities, refer to Technical Brief, PowerPAD Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 and Application Brief, PowerPAD Made Easy, Texas Instruments Literature No. SLMA004. Both documents are available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



Top View

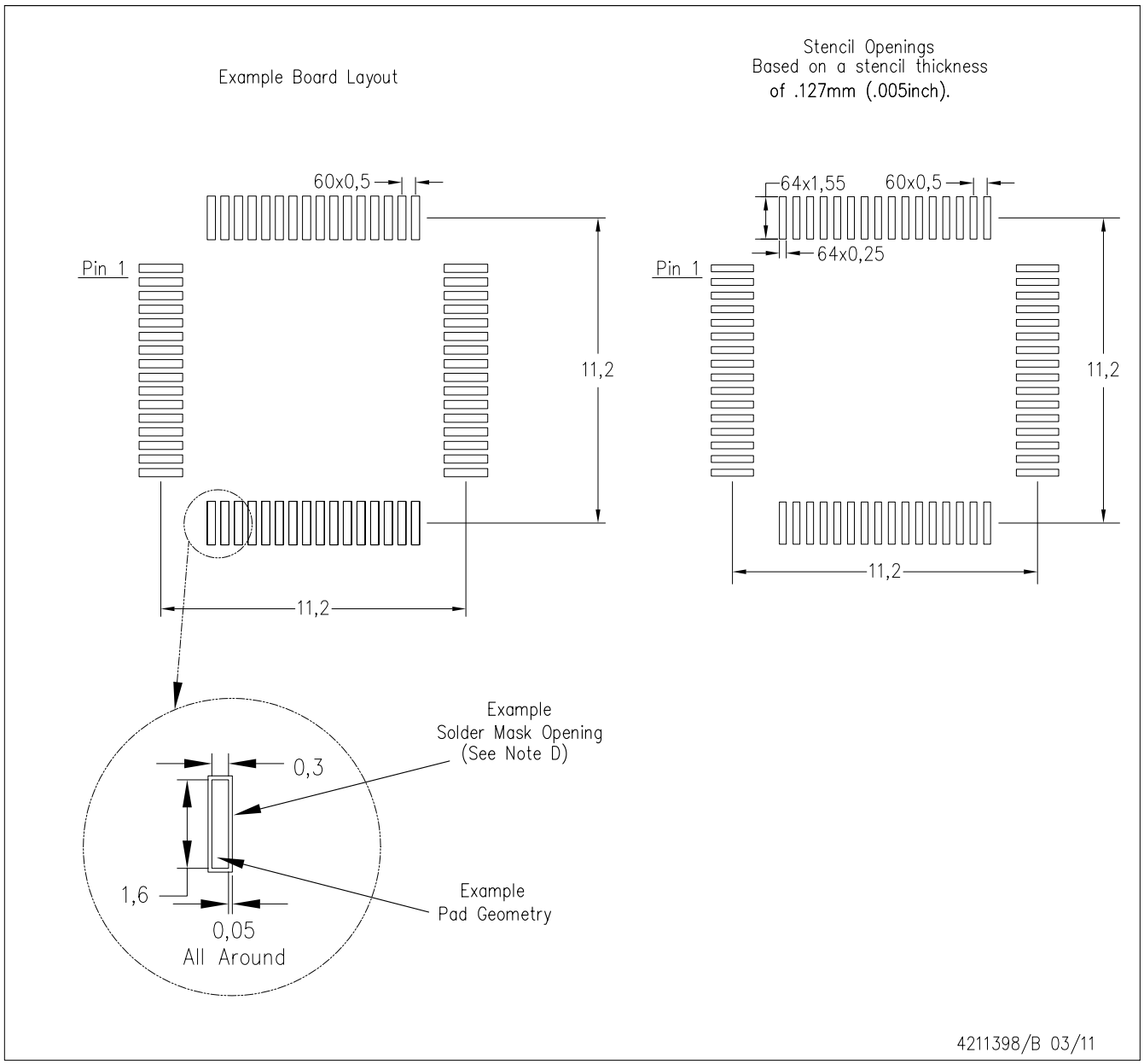
Exposed Thermal Pad Dimensions 4206330–4/B 10/10

NOTE: A. All linear dimensions are in millimeters

B Tie strap features may not be present.

PowerPAD is a trademark of Texas Instruments

PJD (S–PQFP–G64) PowerPAD™ PLASTIC QUAD FLATPACK



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC–7525 for other stencil recommendations.
D. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

IMPORTANT NOTICE AND DISCLAIMER

TI PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATA SHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES “AS IS” AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, regulatory or other requirements.

These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you will fully indemnify TI and its representatives against, any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

TI’s products are provided subject to TI’s Terms of Sale or other applicable terms available either on ti.com or provided in conjunction with such TI products. TI’s provision of these resources does not expand or otherwise alter TI’s applicable warranties or warranty disclaimers for TI products.

TI objects to and rejects any additional or different terms you may have proposed.

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265

Looking for pricing, stock, or lifecycle information?

Click below to explore more details on WIN SOURCE:

- View TPS23841PJDR on WIN SOURCE
- Texas Instruments Information

Optimize Your Supply Chain with WIN SOURCE Solutions

- Global Sourcing Solution
- Obsolete Management
- Cost Control Management
- Shortage Management
- Alternative Solution
- Excess Inventory Management