THE DATASHEET OF

TMS320F28068FPZT

www.win-source.net 0086-755-83957316

TMS320F28069, TMS320F28069M, TMS320F28069F, TMS320F28068M, TMS320F28068F
TMS320F28067, TMS320F28066, TMS320F28065, TMS320F28064, TMS320F28063
TMS320F28062, TMS320F28062F
SPRS698J – NOVEMBER 2010 – REVISED SEPTEMBER 2021

TMS320F2806x Real-Time Microcontrollers

1 Features

- High-efficiency 32-bit CPU (TMS320C28x)
  - 90 MHz (11.11-ns cycle time)
  - 16 × 16 and 32 × 32 Multiply and Accumulate (MAC) operations
  - 16 × 16 dual MAC
  - Harvard bus architecture
  - Atomic operations
  - Fast interrupt response and processing
  - Unified memory programming model
  - Code-efficient (in C/C++ and Assembly)
- Floating-Point Unit (FPU)
  - Native single-precision floating-point operations
- Programmable Control Law Accelerator (CLA)
  - 32-bit floating-point math accelerator
  - Executes code independently of the main CPU
- Viterbi, Complex Math, CRC Unit (VCU)
  - Extends C28x instruction set to support complex multiply, Viterbi operations, and Cyclic Redundency Check (CRC)
- Embedded memory
  - Up to 256KB of flash
  - Up to 100KB of RAM
  - 2KB of One-Time Programmable (OTP) ROM
- 6-channel Direct Memory Access (DMA)
- Low device and system cost
  - Single 3.3-V supply
  - No power sequencing requirement
  - Integrated power-on reset and brownout reset
  - Low-power operating modes
  - No analog support pin
- Endianness: Little endian
- JTAG boundary scan support
  - IEEE Standard 1149.1-1990 Standard Test Access Port and Boundary Scan Architecture
- Clocking
  - Two internal zero-pin oscillators
  - On-chip crystal oscillator/external clock input
  - Watchdog timer module
  - Missing clock detection circuitry
- Peripheral Interrupt Expansion (PIE) block that supports all peripheral interrupts
- Three 32-bit CPU timers
- Advanced control peripherals
- Up to 8 Enhanced Pulse-Width Modulator (ePWM) modules
  - 16 PWM channels total (8 HRPWM-capable)
  - Independent 16-bit timer in each module
- Three input Enhanced Capture (eCAP) modules
- Up to 4 High-Resolution Capture (HRCAP) modules
- Up to 2 Enhanced Quadrature Encoder Pulse (eQEP) modules
- 12-bit Analog-to-Digital Converter (ADC), dual Sample-and-Hold (S/H)
  - Up to 3.46 MSPS
  - Up to 16 channels
- On-chip temperature sensor
- 128-bit security key and lock
  - Protects secure memory blocks
  - Prevents reverse-engineering of firmware
- Serial port peripherals
  - Two Serial Communications Interface (SCI) [UART] modules
  - Two Serial Peripheral Interface (SPI) modules
  - One Inter-Integrated-Circuit (I2C) bus
  - One Multichannel Buffered Serial Port (McBSP) bus
  - One Enhanced Controller Area Network (eCAN)
  - Universal Serial Bus (USB) 2.0 (see Device Comparison for availability)
    - Full-speed device mode
    - Full-speed or low-speed host mode
- Up to 54 individually programmable, multiplexed General-Purpose Input/Output (GPIO) pins with input filtering
- Advanced debug features
  - Analysis and breakpoint functions
  - Real-time debug through hardware
- Package options
  - 80-pin PFP and 100-pin PZP PowerPAD™ Thermally Enhanced Thin Quad Flatpacks (HTQFPs)
  - 80-pin PN and 100-pin PZ Low-Profile Quad Flatpacks (LQFPs)
- Temperature options
  - T: –40°C to 105°C
  - S: –40°C to 125°C
  - Q: –40°C to 125°C (AEC Q100 qualification for automotive applications)

An IMPORTANT NOTICE at the end of this data sheet addresses availability, warranty, changes, use in safety-critical applications, intellectual property matters and other important disclaimers. PRODUCTION DATA.

2 Applications

- Air conditioner outdoor unit
- Door operator drive control
- Inverter & motor control
- On-board (OBC) & wireless charger
- Automated sorting equipment
- CNC control
- Textile machine
- Welding machine
- EV charging station power module
- Wireless vehicle charging module
- Energy storage power conversion system (PCS)
- Central inverter
- Micro inverter
- Solar power optimizer
- String inverter
- AC drive control module
- AC drive power stage module
- Linear motor power stage
- Servo drive control module
- Servo drive power stage module
- AC-input BLDC motor drive
- DC-input BLDC motor drive
- Industrial AC-DC
- Three phase UPS

3 Description

C2000™ 32-bit microcontrollers are optimized for processing, sensing, and actuation to improve closed-loop performance in real-time control applications such as industrial motor drives; solar inverters and digital power; electrical vehicles and transportation; motor control; and sensing and signal processing. The C2000 line includes the Premium performance MCUs and the Entry performance MCUs.

The F2806x family of microcontrollers (MCUs) provides the power of the C28x core and CLA coupled with highly integrated control peripherals in low pin-count devices. This family is code-compatible with previous C28x-based code, and also provides a high level of analog integration.

An internal voltage regulator allows for single-rail operation. Enhancements have been made to the HRPWM module to allow for dual-edge control (frequency modulation). Analog comparators with internal 10-bit references have been added and can be routed directly to control the ePWM outputs. The ADC converts from 0 to 3.3-V fixed full-scale range and supports ratio-metric V_{REFHI}/V_{REFLO} references. The ADC interface has been optimized for low overhead and latency.

To learn more about the C2000 MCUs, visit the C2000 Overview at www.ti.com/c2000.

Device Information

PART NUMBER(1)	PACKAGE	BODY SIZE
TMS320F28069PZP	HTQFP (100)	14.0 mm × 14.0 mm
TMS320F28069PFP	HTQFP (80)	12.0 mm × 12.0 mm
TMS320F28069PZ	LQFP (100)	14.0 mm × 14.0 mm
TMS320F28069PN	LQFP (80)	12.0 mm × 12.0 mm

(1) For more information on these devices, see Mechanical, Packaging, and Orderable Information.

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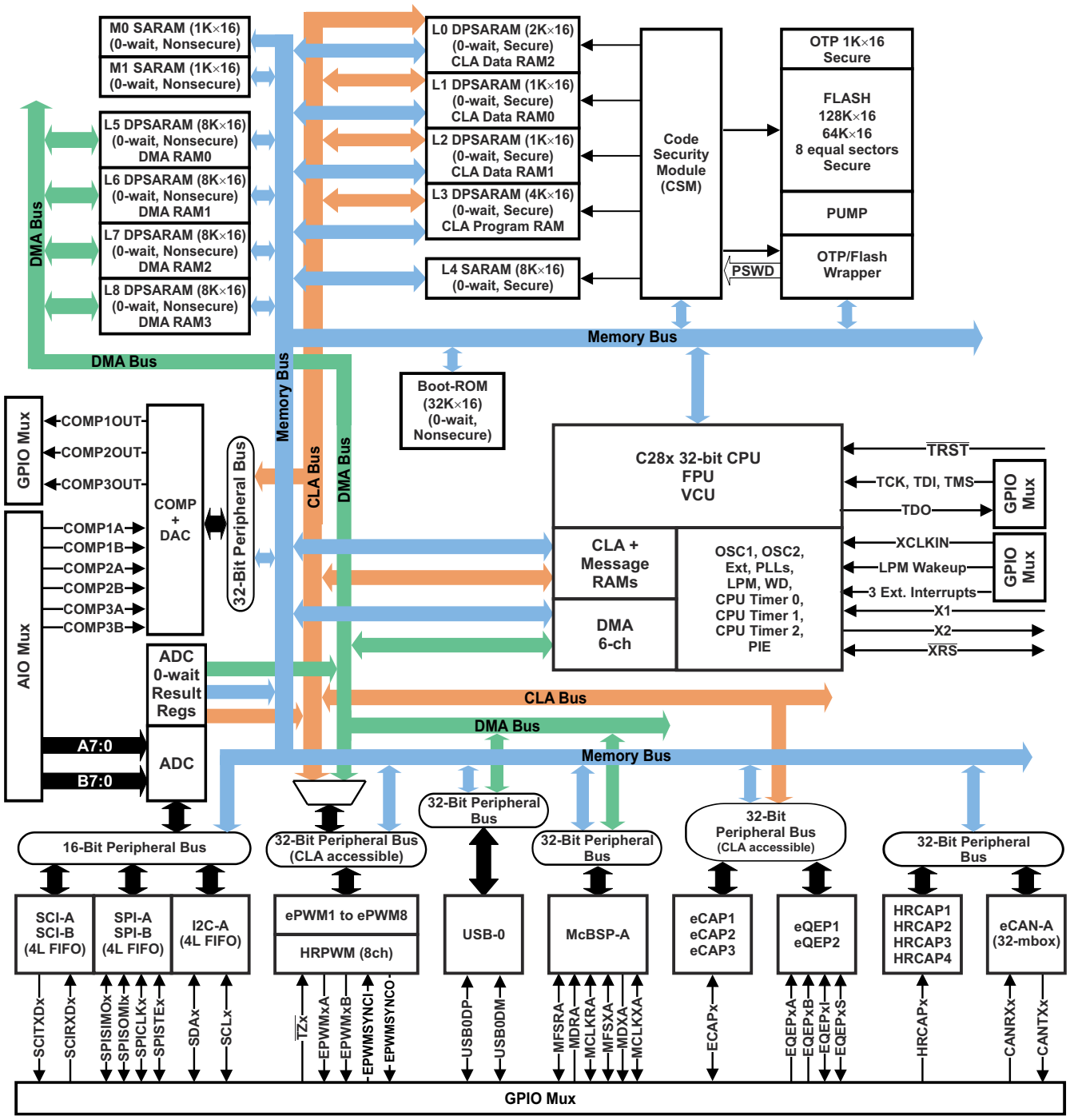
3.1 Functional Block Diagram

Figure 3-1 shows a functional block diagram of the device.



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A. Not all peripheral pins are available at the same time due to multiplexing.

Figure 3-1. Functional Block Diagram

3.2 System Device Diagram

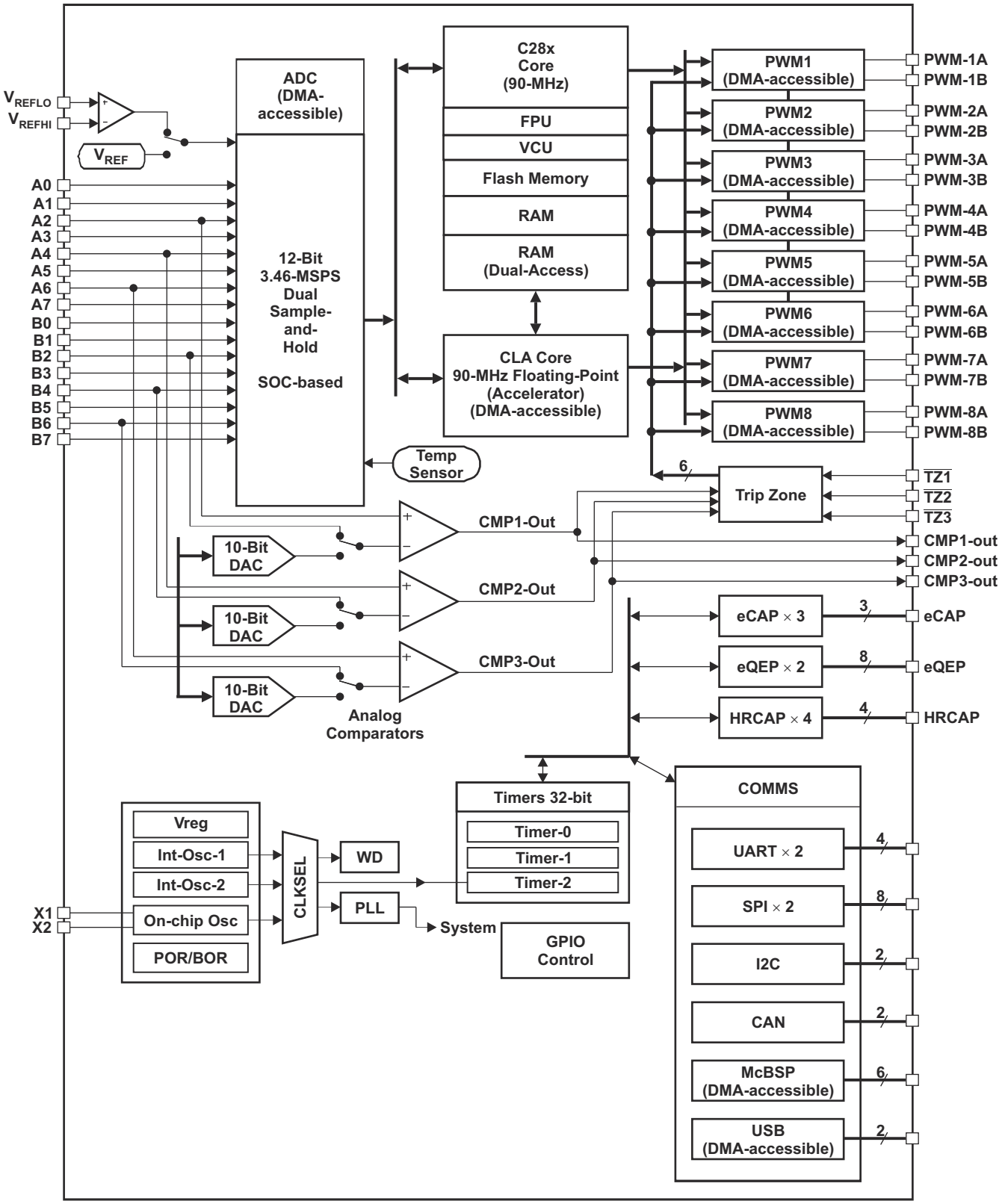

Figure 3-2. Peripheral Blocks

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4 Revision History

Changes from February 1, 2021 to May 30, 2021 (from Revision I (February 2021) to Revision J (May 2021)) **Page**

- Global Change: Updated/changed "emulation" to "debug" 1
- Added Q1 part numbers 1
- Updated/changed from "SCI" to "SCI/UART" 7
- Updated/changed *Device Compairson* table footnote to show correct part numbers 7
- Updated/changed the definition for VREGENZ 12
- Updated/changed oscillator footnote 38
- Updated/changed *Security* note 47
- Updated/changed Peripheral Frame information 64
- Added a row for Instaspin feature 66
- Updated/changed image, *Clock Tree*, to remove WDCLK label 70
- Updated/changed "CPU Watchdog Module" to remove WDCLK 77
- Added C2000 third-party search tool link 167

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5 Device Comparison

Table 5-1 lists the features of the TMS320F2806x devices.

Table 5-1. Device Comparison

FEATURE		TYPE (1)	28069 28069-Q1 **28069U**(2) (5) 28069M (2) (3) 28069M-Q1 28069F (2) (3) 28069F-Q1 **(90 MHz)**		**28068U**(2) (5) 28068M (2) (3) 28068F (2) (3) **(90 MHz)**		28067 28067-Q1 **28067U**(2) (5) **(90 MHz)**		28066 28066-Q1 **28066U**(2) (5) **(90 MHz)**		28065 28065-Q1 **28065U**(2) (5) **(90 MHz)**		28064 **28064U**(2) (5) **(90 MHz)**		28063 **28063U**(2) (5) **(90 MHz)**		28062 28062-Q1 **28062U**(2) (5) 28062F (2) (3) 28062F-Q1 **(90 MHz)**	
Package Type (PFP and PZP are PowerPAD HTQFPs. PN and PZ are LQFPs.)			**100-Pin PZ PZP**	**80-Pin PN PFP**	**100-Pin PZ PZP**	**80-Pin PN PFP**	**100-Pin PZ PZP**	**80-Pin PN PFP**	**100-Pin PZ PZP**	**80-Pin PN PFP**	**100-Pin PZ PZP**	**80-Pin PN PFP**	**100-Pin PZ PZP**	**80-Pin PN PFP**	**100-Pin PZ PZP**	**80-Pin PN PFP**	**100-Pin PZ PZP**	**80-Pin PN PFP**
Instruction cycle		–	11.11 ns		11.11 ns		11.11 ns		11.11 ns		11.11 ns		11.11 ns		11.11 ns		11.11 ns	
Floating-Point Unit (FPU)			Yes		Yes		Yes		Yes		Yes		Yes		Yes		Yes	
VCU			Yes		Yes		No		No		Yes		Yes		No		No	
CLA		0	Yes		No		No		No		Yes		No		No		No	
6-Channel DMA		0	Yes		Yes		Yes		Yes		Yes		Yes		Yes		Yes	
On-chip Flash (16-bit word)		–	128K		128K		128K		128K		64K		64K		64K		64K	
On-chip SARAM (16-bit word)		–	50K		50K		50K		34K		50K		50K		34K		26K	
Code security for on-chip Flash, SARAM, and OTP blocks		–	Yes		Yes		Yes		Yes		Yes		Yes		Yes		Yes	
Boot ROM (32K × 16)		–	Yes		Yes		Yes		Yes		Yes		Yes		Yes		Yes	
One-time programmable (OTP) ROM (16-bit word)		–	1K		1K		1K		1K		1K		1K		1K		1K	
ePWM channels		1	16	14	16	14	16	14	16	14	16	14	16	14	16	14	16	14
High-resolution ePWM Channels		1	8		8		8		8		8		8		8		8	
eCAP inputs		0	3		3		3		3		3		3		3		3	
HRCAP		0	4	1	4	1	4	1	4	1	4	1	4	1	4	1	4	1
eQEP modules		0	2	1	2	1	2	1	2	1	2	1	2	1	2	1	2	1
Watchdog timer		–	Yes		Yes		Yes		Yes		Yes		Yes		Yes		Yes	
12-Bit ADC	MSPS	3	3.46		3.46		3.46		3.46		3.46		3.46		3.46		3.46	
	Conversion Time		289 ns		289 ns		289 ns		289 ns		289 ns		289 ns		289 ns		289 ns	
	Channels		16	12	16	12	16	12	16	12	16	12	16	12	16	12	16	12
	Temperature Sensor		Yes		Yes		Yes		Yes		Yes		Yes		Yes		Yes	
	Dual Sample-and-Hold		Yes		Yes		Yes		Yes		Yes		Yes		Yes		Yes	
32-Bit CPU timers		–	3		3		3		3		3		3		3		3	
Comparators with Integrated DACs		0	3		3		3		3		3		3		3		3	
I2C		0	1		1		1		1		1		1		1		1	
McBSP		1	1		1		1		1		1		1		1		1	
eCAN		0	1		1		1		1		1		1		1		1	
SPI		1	2		2		2		2		2		2		2		2	
SCI/UART		0	2		2		2		2		2		2		2		2	
USB		0	1(2)		1(2)		1(2)		1(2)		1(2)		1(2)		1(2)		1(2)	
2-pin Oscillator			1		1		1		1		1		1		1		1	
0-pin Oscillator			2		2		2		2		2		2		2		2	
I/O pins (shared)	GPIO	–	54	40	54	40	54	40	54	40	54	40	54	40	54	40	54	40
	AIO	–	6		6		6		6		6		6		6		6	
External interrupts		–	3		3		3		3		3		3		3		3	
Supply voltage (nominal)		–	3.3 V		3.3 V		3.3 V		3.3 V		3.3 V		3.3 V		3.3 V		3.3 V	

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Table 5-1. Device Comparison (continued)

FEATURE		TYPE (1)	28069 28069-Q1 **28069U**(2) (5) 28069M (2) (3) 28069M-Q1 28069F (2) (3) 28069F-Q1 **(90 MHz)**		**28068U**(2) (5) 28068M (2) (3) 28068F (2) (3) **(90 MHz)**		28067 28067-Q1 **28067U**(2) (5) **(90 MHz)**		28066 28066-Q1 **28066U**(2) (5) **(90 MHz)**		28065 28065-Q1 **28065U**(2) (5) **(90 MHz)**		28064 **28064U**(2) (5) **(90 MHz)**		28063 **28063U**(2) (5) **(90 MHz)**		28062 28062-Q1 **28062U**(2) (5) 28062F (2) (3) 28062F-Q1 **(90 MHz)**	
Package Type (PFP and PZP are PowerPAD HTQFPs. PN and PZ are LQFPs.)			**100-Pin PZ PZP**	**80-Pin PN PFP**	**100-Pin PZ PZP**	**80-Pin PN PFP**	**100-Pin PZ PZP**	**80-Pin PN PFP**	**100-Pin PZ PZP**	**80-Pin PN PFP**	**100-Pin PZ PZP**	**80-Pin PN PFP**	**100-Pin PZ PZP**	**80-Pin PN PFP**	**100-Pin PZ PZP**	**80-Pin PN PFP**	**100-Pin PZ PZP**	**80-Pin PN PFP**
Temperature options	T: –40°C to 105°C	–	PZ	PN	PZ	PN	PZ	PN	PZ	PN	PZ	PN	PZ	PN	PZ	PN	PZ	PN
	S: –40°C to 125°C	–	PZP	PFP	PZP	PFP	PZP	PFP	PZP	PFP	PZP	PFP	PZP	PFP	PZP	PFP	PZP	PFP
	Q: –40°C to 125°C(5) (4)	–	PZP	PFP	PZP	PFP	PZP	PFP	PZP	PFP	PZP	PFP	PZP	PFP	PZP	PFP	PZP	PFP

(1) A type change represents a major functional feature difference in a peripheral module. Within a peripheral type, there may be minor differences between devices that do not affect the basic functionality of the module. These device-specific differences are listed in the *C2000 Real-Time Control Peripherals Reference Guide* and in the peripheral reference guides.
(2) USB is present on TMS320F2806xU, TMS320F2806xM, and TMS320F2806xF devices.
(3) TMS320F2806xF devices are InstaSPIN-FOC™-enabled MCUs. TMS320F2806xM devices are InstaSPIN-MOTION™-enabled MCUs. But instaSPIN-MOTION is no longer recommended for new designs and will not have application support. For more information, see Section 10.3 for a list of InstaSPIN Technical Reference Manuals.
(4) The letter Q refers to AEC Q100 qualification for automotive applications.
(5) The Q temperature option is ***not*** available on the TMS320F2806xU devices.

5.1 Related Products

For information about similar products, see the following links:

TMS320F2802x Microcontrollers
The F2802x series offers the lowest pin-count and Flash memory size options. InstaSPIN-FOC™ versions are available.

TMS320F2803x Microcontrollers
The F2803x series increases the pin-count and memory size options. The F2803x series also introduces the parallel control law accelerator (CLA) option.

TMS320F2805x Microcontrollers
The F2805x series is similar to the F2803x series but adds on-chip programmable gain amplifiers (PGAs). InstaSPIN-FOC and InstaSPIN-MOTION™ versions are available.

TMS320F2806x Microcontrollers
The F2806x series is the first to include a floating-point unit (FPU). The F2806x series also increases the pin-count, memory size options, and the quantity of peripherals. InstaSPIN-FOC™ and InstaSPIN-MOTION™ versions are available.

TMS320F2807x Microcontrollers
The F2807x series offers the most performance, largest pin counts, flash memory sizes, and peripheral options. The F2807x series includes the latest generation of accelerators, ePWM peripherals, and analog technology.

TMS320F28004x Microcontrollers
The F28004x series is a reduced version of the F2807x series with the latest generational enhancements. The F28004x series is the best roadmap option for those using the F2806x series. InstaSPIN-FOC and configurable logic block (CLB) versions are available.

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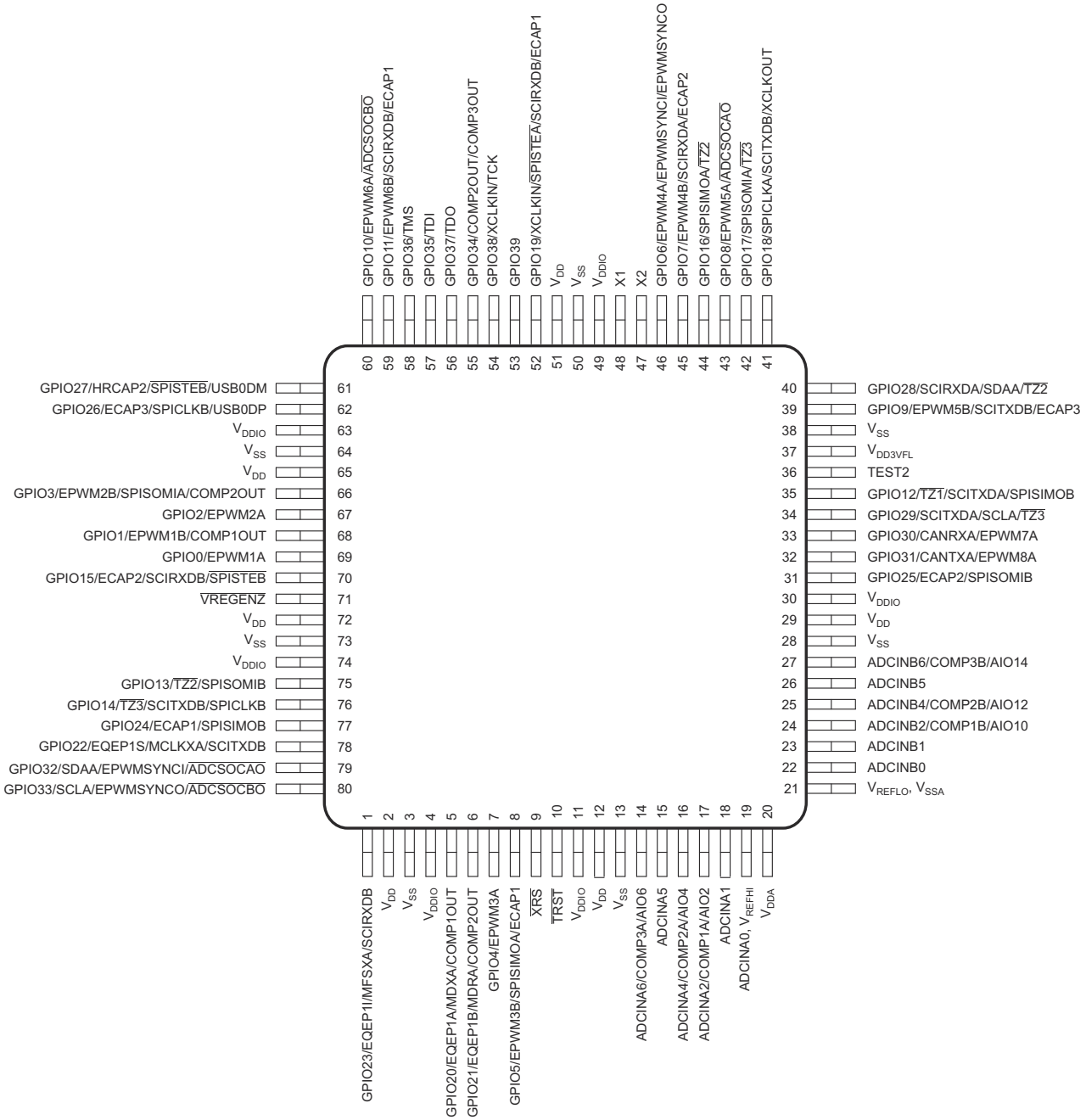
6 Terminal Configuration and Functions

6.1 Pin Diagrams

Figure 6-1 shows the pin assignments on the 80-pin PN and PFP packages. Figure 6-2 shows the pin assignments on the 100-pin PZ and PZP packages.



A. Pin 19: V_{REFHI} and ADCINA0 share the same pin on the 80-pin PN and PFP devices and their use is mutually exclusive to one another. Pin 21: V_{REFLO} is always connected to V_{SSA} on the 80-pin PN and PFP devices.

B. The PowerPAD is not connected to the ground on the die. To facilitate effective heat dissipation, the PowerPAD must be connected to the ground plane of the PCB. It should not be left unconnected. For more details, see *PowerPAD™ Thermally Enhanced Package*.

Figure 6-1. 80-Pin PN and PFP Packages (Top View)

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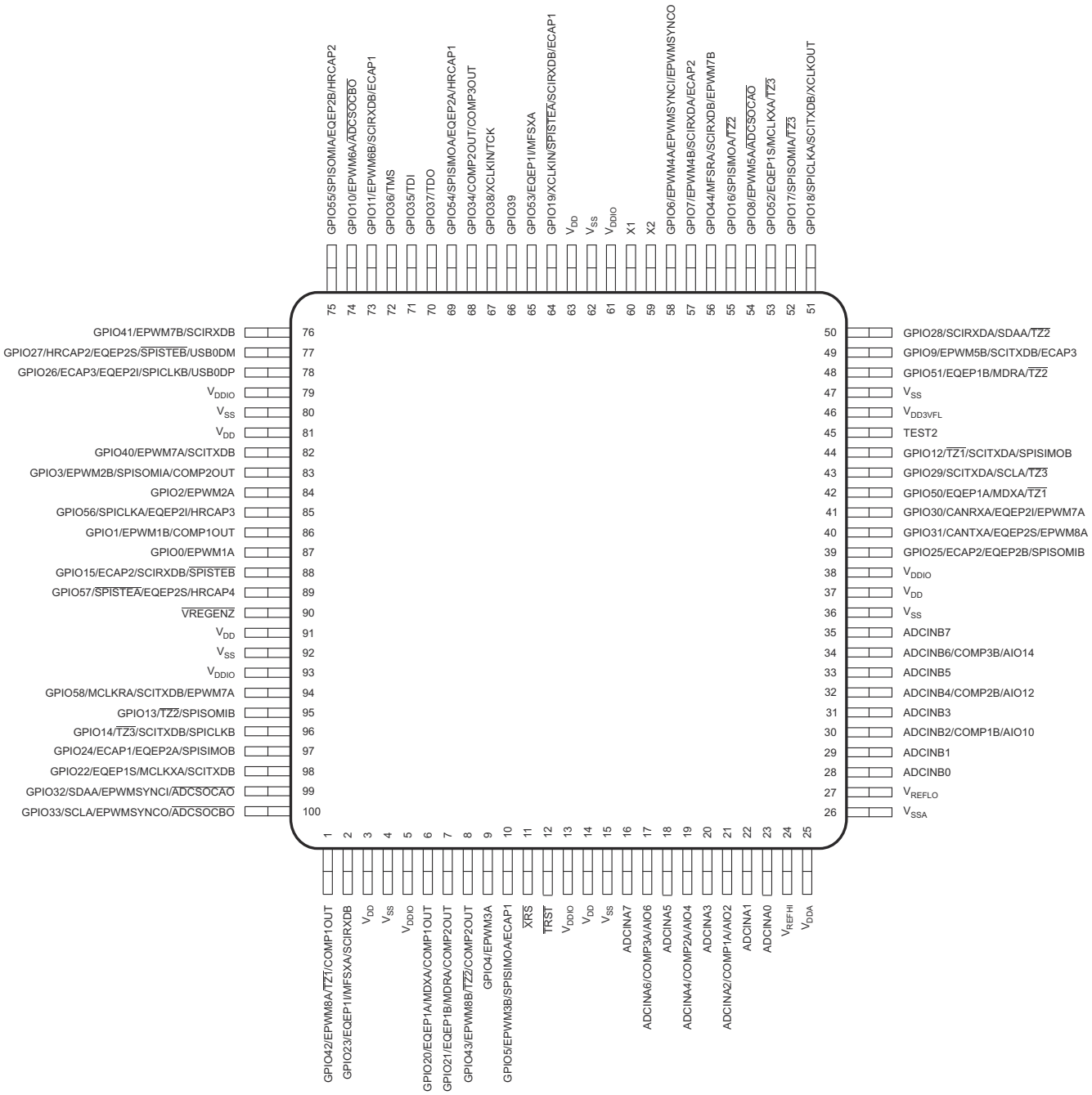

A. The PowerPAD is not connected to the ground on the die. To facilitate effective heat dissipation, the PowerPAD must be connected to the ground plane of the PCB. It should not be left unconnected. For more details, see *PowerPAD™ Thermally Enhanced Package*.

Figure 6-2. 100-Pin PZ and PZP Packages (Top View)

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Note

The PowerPAD™ should be soldered to the ground (GND) plane of the PCB because this will provide the best thermal conduction path. For this device, the PowerPAD is not electrically shorted to the internal die V_{SS}; therefore, the PowerPAD does not provide an electrical connection to the PCB ground. To make optimum use of the thermal efficiencies designed into the PowerPAD package, the PCB must be designed with this technology in mind. A thermal land is required on the surface of the PCB directly underneath the body of the PowerPAD. The thermal land should be soldered to the exposed lead frame die pad of the PowerPad package; the thermal land should be as large as needed to dissipate the required heat. An array of thermal vias should be used to connect the thermal pad to the internal GND plane of the board. See *PowerPAD™ Thermally Enhanced Package* for more details on using the PowerPAD package.

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6.2 Signal Descriptions

Section 6.2.1 describes the signals. With the exception of the JTAG pins, the GPIO function is the default at reset, unless otherwise mentioned. The peripheral signals that are listed under them are alternate functions. Some peripheral functions may not be available in all devices. See Table 5-1 for details. Inputs are not 5-V tolerant. All GPIO pins are I/O/Z and have an internal pullup (PU), which can be selectively enabled or disabled on a per-pin basis. This feature only applies to the GPIO pins. The pullups on the PWM pins are not enabled at reset. The pullups on other GPIO pins are enabled upon reset. The AIO pins do not have an internal pullup.

Note

When the on-chip voltage regulator (VREG) is used, the GPIO19, GPIO26–27, and GPIO34–38 pins could glitch during power up. This potential glitch will finish before the boot mode pins are read and will not affect boot behavior. If glitching is unacceptable in an application, 1.8 V could be supplied externally. Alternatively, adding a current-limiting resistor (for example, 470 Ω) in series with these pins and any external driver could be considered to limit the potential for degradation to the pin and/or external circuitry. There is no power-sequencing requirement when using an external 1.8-V supply. However, if the 3.3-V transistors in the level-shifting output buffers of the I/O pins are powered before the 1.8-V transistors, it is possible for the output buffers to turn on, causing a glitch to occur on the pin during power up. To avoid this behavior, power the V_{DD} pins before or simultaneously with the V_{DDIO} pins, ensuring that the V_{DD} pins have reached 0.7 V before the V_{DDIO} pins reach 0.7 V.

6.2.1 Signal Descriptions

PIN NAME	PIN NO.		I/O/Z[1]	DESCRIPTION
	PZ PZP	PN PFP		
JTAG				
$\overline{TRST}$	12	10	I	JTAG test reset with internal pulldown (PD). $\overline{TRST}$, when driven high, gives the scan system control of the operations of the device. If this signal is not connected or driven low, the device operates in its functional mode, and the test reset signals are ignored. **NOTE:** $\overline{TRST}$ is an active-high test pin and must be maintained low at all times during normal device operation. An external pulldown resistor is required on this pin. The value of this resistor should be based on drive strength of the debugger pods applicable to the design. A 2.2-kΩ resistor generally offers adequate protection. Because this is application-specific, TI recommends validating each target board for proper operation of the debugger and the application. (↓)
TCK	See GPIO38		I	See GPIO38. JTAG test clock with internal pullup. (↑)
TMS	See GPIO36		I	See GPIO36. JTAG test-mode select (TMS) with internal pullup. This serial control input is clocked into the TAP controller on the rising edge of TCK. (↑)
TDI	See GPIO35		I	See GPIO35. JTAG test data input (TDI) with internal pullup. TDI is clocked into the selected register (instruction or data) on a rising edge of TCK. (↑)
TDO	See GPIO37		O/Z	See GPIO37. JTAG scan out, test data output (TDO). The contents of the selected register (instruction or data) are shifted out of TDO on the falling edge of TCK. (8-mA drive)
FLASH				
V_{DD3VFL}	46	37		3.3-V Flash Core Power Pin. This pin should be connected to 3.3 V at all times.
TEST2	45	36	I/O	Test Pin. Reserved for TI. Must be left unconnected.

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PIN NAME	PIN NO.		I/O/Z[1]	DESCRIPTION
	PZ PZP	PN PFP		
CLOCK				
XCLKOUT	See GPIO18		O/Z	See GPIO18. Output clock derived from SYSCLKOUT. XCLKOUT is either the same frequency, one-half the frequency, or one-fourth the frequency of SYSCLKOUT. This is controlled by bits 1:0 (XCLKOUTDIV) in the XCLK register. At reset, XCLKOUT = SYSCLKOUT/4. The XCLKOUT signal can be turned off by setting XCLKOUTDIV to 3. The mux control for GPIO18 must also be set to XCLKOUT for this signal to propogate to the pin.
XCLKIN	See GPIO19 and GPIO38		I	See GPIO19 and GPIO38. External oscillator input. Pin source for the clock is controlled by the XCLKINSEL bit in the XCLK register, GPIO38 is the default selection. This pin feeds a clock from an external 3.3-V oscillator. In this case, the X1 pin, if available, must be tied to GND and the on-chip crystal oscillator must be disabled through bit 14 in the CLKCTL register. If a crystal or resonator is used, the XCLKIN path must be disabled by bit 13 in the CLKCTL register. **NOTE:** Designs that use the GPIO38/XCLKIN/TCK pin to supply an external clock for normal device operation may need to incorporate some hooks to disable this path during debug using the JTAG connector. This is to prevent contention with the TCK signal, which is active during JTAG debug sessions. The zero-pin internal oscillators may be used during this time to clock the device.
X1	60	48	I	On-chip 1.8-V crystal-oscillator input. To use this oscillator, a quartz crystal or a ceramic resonator must be connected across X1 and X2. In this case, the XCLKIN path must be disabled by bit 13 in the CLKCTL register. If this pin is not used, it must be tied to GND.
X2	59	47	O	On-chip crystal-oscillator output. A quartz crystal or a ceramic resonator must be connected across X1 and X2. If X2 is not used, it must be left unconnected.
RESET				
$\overline{XRS}$	11	9	I/OD	Device Reset (in) and Watchdog Reset (out). These devices have a built-in power-on reset (POR) and brownout reset (BOR) circuitry. During a power-on or brownout condition, this pin is driven low by the device. An external circuit may also drive this pin to assert a device reset. This pin is also driven low by the MCU when a watchdog reset occurs. During watchdog reset, the $\overline{XRS}$ pin is driven low for the watchdog reset duration of 512 OSCCLK cycles. A resistor with a value from 2.2 kΩ to 10 kΩ should be placed between $\overline{XRS}$ and V_{DDIO}. If a capacitor is placed between $\overline{XRS}$ and V_{SS} for noise filtering, it should be 100 nF or smaller. These values will allow the watchdog to properly drive the $\overline{XRS}$ pin to V_{OL} within 512 OSCCLK cycles when the watchdog reset is asserted. Regardless of the source, a device reset causes the device to terminate execution. The program counter points to the address contained at the location 0x3F FFC0. When reset is deactivated, execution begins at the location designated by the program counter. The output buffer of this pin is an open-drain device with an internal pullup. (↑) If this pin is driven by an external device, it should be done using an open-drain device.
ADC, COMPARATOR, ANALOG I/O				
ADCINA7	16	–	I	ADC Group A, Channel 7 input
ADCINA6	17	14	I	ADC Group A, Channel 6 input
COMP3A			I	Comparator Input 3A
AIO6			I/O	Digital AIO 6
ADCINA5	18	15	I	ADC Group A, Channel 5 input
ADCINA4	19	16	I	ADC Group A, Channel 4 input
COMP2A			I	Comparator Input 2A
AIO4			I/O	Digital AIO 4
ADCINA3	20	–	I	ADC Group A, Channel 3 input
ADCINA2	21	17	I	ADC Group A, Channel 2 input
COMP1A			I	Comparator Input 1A
AIO2			I/O	Digital AIO 2
ADCINA1	22	18	I	ADC Group A, Channel 1 input

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PIN NAME	PIN NO.		I/O/Z[1]	DESCRIPTION
	PZ PZP	PN PFP		
ADCINA0	23	19	I	ADC Group A, Channel 0 input. **NOTE:** V_{REFHI} and ADCINA0 share the same pin on the 80-pin PN and PFP devices and their use is mutually exclusive to one another.
V_{REFHI}	24	19		ADC External Reference High – only used when in ADC external reference mode. See Section 8.9.2.1. **NOTE:** V_{REFHI} and ADCINA0 share the same pin on the 80-pin PN and PFP devices and their use is mutually exclusive to one another.
ADCINB7	35	–	I	ADC Group B, Channel 7 input
ADCINB6	34	27	I	ADC Group B, Channel 6 input
COMP3B			I	Comparator Input 3B
AIO14			I/O	Digital AIO 14
ADCINB5	33	26	I	ADC Group B, Channel 5 input
ADCINB4	32	25	I	ADC Group B, Channel 4 input
COMP2B			I	Comparator Input 2B
AIO12			I/O	Digital AIO12
ADCINB3	31	–	I	ADC Group B, Channel 3 input
ADCINB2	30	24	I	ADC Group B, Channel 2 input
COMP1B			I	Comparator Input 1B
AIO10			I/O	Digital AIO 10
ADCINB1	29	23	I	ADC Group B, Channel 1 input
ADCINB0	28	22	I	ADC Group B, Channel 0 input
V_{REFLO}	27	21		ADC External Reference Low. **NOTE:** V_{REFLO} is always connected to V_{SSA} on the 80-pin PN and PFP devices.
CPU AND I/O POWER				
V_{DDA}	25	20		Analog Power Pin. Tie with a 2.2-µF capacitor (typical) close to the pin.
V_{SSA}	26	21		Analog Ground Pin. **NOTE:** V_{REFLO} is always connected to V_{SSA} on the 80-pin PN and PFP devices.
V_{DD}	3	2		CPU and Logic Digital Power Pins. When using internal VREG, place one 1.2-µF capacitor between each V_{DD} pin and ground. Higher value capacitors may be used.
	14	12		
	37	29		
	63	51		
	81	65		
	91	72		
V_{DDIO}	5	4		Digital I/O Buffers Power Pin. Single supply source when VREG is enabled. Place a decoupling capacitor on each pin. The exact value should be determined by the system voltage regulation solution.
	13	11		
	38	30		
	61	49		
	79	63		
	93	74		
V_{SS}	4	3		Digital Ground Pins
	15	13		
	36	28		
	47	38		
	62	50		
	80	64		
	92	73		

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PIN NAME	PIN NO. PZ PZP	PIN NO. PN PFP	I/O/Z[1]	DESCRIPTION
VOLTAGE REGULATOR CONTROL SIGNAL				
$\overline{\text{VREGENZ}}$	90	71	I	Internal voltage regulator (VREG) enable with internal pulldown. Tie directly to VSS (low) to enable the internal 1.8-V VREG. Tie directly to VDDIO (high) to disable the VREG and use an external 1.8-V supply.
GPIO AND PERIPHERAL SIGNALS [2]				
GPIO0	87	69	I/O/Z	General-purpose input/output 0
EPWM1A			O	Enhanced PWM1 Output A and HRPWM channel
Reserved			–	Reserved
Reserved			–	Reserved
GPIO1	86	68	I/O/Z	General-purpose input/output 1
EPWM1B			O	Enhanced PWM1 Output B
Reserved			–	Reserved
COMP1OUT			O	Direct output of Comparator 1
GPIO2	84	67	I/O/Z	General-purpose input/output 2
EPWM2A			O	Enhanced PWM2 Output A and HRPWM channel
Reserved			–	Reserved
Reserved			–	Reserved
GPIO3	83	66	I/O/Z	General-purpose input/output 3
EPWM2B			O	Enhanced PWM2 Output B
SPISOMIA			I/O	SPI-A slave out, master in
COMP2OUT			O	Direct output of Comparator 2
GPIO4	9	7	I/O/Z	General-purpose input/output 4
EPWM3A			O	Enhanced PWM3 output A and HRPWM channel
Reserved			–	Reserved
Reserved			–	Reserved
GPIO5	10	8	I/O/Z	General-purpose input/output 5
EPWM3B			O	Enhanced PWM3 output B
SPISIMOA			I/O	SPI-A slave in, master out
ECAP1			I/O	Enhanced Capture input/output 1
GPIO6	58	46	I/O/Z	General-purpose input/output 6
EPWM4A			O	Enhanced PWM4 output A and HRPWM channel
EPWMSYNCI			I	External ePWM sync pulse input
EPWMSYNCO			O	External ePWM sync pulse output
GPIO7	57	45	I/O/Z	General-purpose input/output 7
EPWM4B			O	Enhanced PWM4 output B
SCIRXDA			I	SCI-A receive data
ECAP2			I/O	Enhanced Capture input/output 2
GPIO8	54	43	I/O/Z	General-purpose input/output 8
EPWM5A			O	Enhanced PWM5 output A and HRPWM channel
Reserved			–	Reserved
$\overline{\text{ADCSOCAO}}$			O	ADC start-of-conversion A
GPIO9	49	39	I/O/Z	General-purpose input/output 9
EPWM5B			O	Enhanced PWM5 output B
SCITXDB			O	SCI-B transmit data
ECAP3			I/O	Enhanced Capture input/output 3

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PIN NAME	PIN NO.		I/O/Z[1]	DESCRIPTION
	PZ PZP	PN PFP		
GPIO10	74	60	I/O/Z	General-purpose input/output 10
EPWM6A			O	Enhanced PWM6 output A and HRPWM channel
Reserved			–	Reserved
$\overline{\text{ADCSOCBO}}$			O	ADC start-of-conversion B
GPIO11	73	59	I/O/Z	General-purpose input/output 11
EPWM6B			O	Enhanced PWM6 output B
SCIRXDB			I	SCI-B receive data
ECAP1			I/O	Enhanced Capture input/output 1
GPIO12	44	35	I/O/Z	General-purpose input/output 12
$\overline{\text{TZ1}}$			I	Trip Zone input 1
SCITXDA			O	SCI-A transmit data
SPISIMOB			I/O	SPI-B slave in, master out
GPIO13	95	75	I/O/Z	General-purpose input/output 13
$\overline{\text{TZ2}}$			I	Trip Zone input 2
Reserved			–	Reserved
SPISOMIB			I/O	SPI-B slave out, master in
GPIO14	96	76	I/O/Z	General-purpose input/output 14
$\overline{\text{TZ3}}$			I	Trip zone input 3
SCITXDB			O	SCI-B transmit data
SPICLKB			I/O	SPI-B clock input/output
GPIO15	88	70	I/O/Z	General-purpose input/output 15
ECAP2			I/O	Enhanced Capture input/output 2
SCIRXDB			I	SCI-B receive data
$\overline{\text{SPISTEB}}$			I/O	SPI-B slave transmit enable input/output
GPIO16	55	44	I/O/Z	General-purpose input/output 16
SPISIMOA			I/O	SPI-A slave in, master out
Reserved			–	Reserved
$\overline{\text{TZ2}}$			I	Trip Zone input 2
GPIO17	52	42	I/O/Z	General-purpose input/output 17
SPISOMIA			I/O	SPI-A slave out, master in
Reserved			–	Reserved
$\overline{\text{TZ3}}$			I	Trip zone input 3
GPIO18	51	41	I/O/Z	General-purpose input/output 18
SPICLKA			I/O	SPI-A clock input/output
SCITXDB			O	SCI-B transmit data
XCLKOUT			O/Z	Output clock derived from SYSCLKOUT. XCLKOUT is either the same frequency, one-half the frequency, or one-fourth the frequency of SYSCLKOUT. This is controlled by bits 1:0 (XCLKOUTDIV) in the XCLK register. At reset, XCLKOUT = SYSCLKOUT/4. The XCLKOUT signal can be turned off by setting XCLKOUTDIV to 3. The mux control for GPIO18 must also be set to XCLKOUT for this signal to propogate to the pin.
GPIO19	64	52	I/O/Z	General-purpose input/output 19
XCLKIN			I	External Oscillator Input. The path from this pin to the clock block is not gated by the mux function of this pin. Care must be taken not to enable this path for clocking if it is being used for the other peripheral functions.
$\overline{\text{SPISTEA}}$			I/O	SPI-A slave transmit enable input/output
SCIRXDB			I	SCI-B receive data
ECAP1			I/O	Enhanced Capture input/output 1

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PIN NAME	PIN NO.		I/O/Z[1]	DESCRIPTION
	PZ PZP	PN PFP		
GPIO20	6	5	I/O/Z	General-purpose input/output 20
EQEP1A			I	Enhanced QEP1 input A
MDXA			O	McBSP transmit serial data
COMP1OUT			O	Direct output of Comparator 1
GPIO21	7	6	I/O/Z	General-purpose input/output 21
EQEP1B			I	Enhanced QEP1 input B
MDRA			I	McBSP receive serial data
COMP2OUT			O	Direct output of Comparator 2
GPIO22	98	78	I/O/Z	General-purpose input/output 22
EQEP1S			I/O	Enhanced QEP1 strobe
MCLKXA			I/O	McBSP transmit clock
SCITXDB			O	SCI-B transmit data
GPIO23	2	1	I/O/Z	General-purpose input/output 23
EQEP1I			I/O	Enhanced QEP1 index
MFSXA			I/O	McBSP transmit frame synch
SCIRXDB			I	SCI-B receive data
GPIO24	97	77	I/O/Z	General-purpose input/output 24
ECAP1			I/O	Enhanced Capture input/output 1
EQEP2A			I	Enhanced QEP2 input A. **NOTE:** eQEP2 is available only in the PZ and PZP packages.
SPISIMOB			I/O	SPI-B slave in, master out
GPIO25	39	31	I/O/Z	General-purpose input/output 25
ECAP2			I/O	Enhanced Capture input/output 2
EQEP2B			I	Enhanced QEP2 input B. **NOTE:** eQEP2 is available only in the PZ and PZP packages.
SPISOMIB			I/O	SPI-B slave out, master in
GPIO26	78	62	I/O/Z	General-purpose input/output 26
ECAP3			I/O	Enhanced Capture input/output 3
EQEP2I			I/O	Enhanced QEP2 index. **NOTE:** eQEP2 is available only in the PZ and PZP packages.
SPICLKB			I/O	SPI-B clock input/output
USB0DP[3]			I/O	Positive Differential half of USB signal. To enable USB functionality on this pin, set the USBIOEN bit in the GPACTRL2 register.
GPIO27	77	61	I/O/Z	General-purpose input/output 27
HRCAP2			I	High-Resolution Input Capture 2
EQEP2S			I/O	Enhanced QEP2 strobe. **NOTE:** eQEP2 is available only in the PZ and PZP packages.
$\overline{\text{SPISTEB}}$			I/O	SPI-B slave transmit enable input/output
USB0DM[3]			I/O	Negative Differential half of USB signal. To enable USB functionality on this pin, set the USBIOEN bit in the GPACTRL2 register.
GPIO28	50	40	I/O/Z	General-purpose input/output 28
SCIRXDA			I	SCI-A receive data
SDAA			I/OD	I2C data open-drain bidirectional port
$\overline{\text{TZ2}}$			I	Trip zone input 2

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PIN NAME	PIN NO.		I/O/Z[1]	DESCRIPTION
	PZ PZP	PN PFP		
GPIO29	43	34	I/O/Z	General-purpose input/output 29
SCITXDA			O	SCI-A transmit data
SCLA			I/OD	I2C clock open-drain bidirectional port
$\overline{TZ3}$			I	Trip zone input 3
GPIO30	41	33	I/O/Z	General-purpose input/output 30
CANRXA			I	CAN receive
EQEP2I			I/O	Enhanced QEP2 index. **NOTE:** eQEP2 is available only in the PZ and PZP packages.
EPWM7A			O	Enhanced PWM7 Output A and HRPWM channel
GPIO31	40	32	I/O/Z	General-purpose input/output 31
CANTXA			O	CAN transmit
EQEP2S			I/O	Enhanced QEP2 strobe. **NOTE:** eQEP2 is available only in the PZ and PZP packages.
EPWM8A			O	Enhanced PWM8 Output A and HRPWM channel
GPIO32	99	79	I/O/Z	General-purpose input/output 32
SDAA			I/OD	I2C data open-drain bidirectional port
EPWMSYNCI			I	Enhanced PWM external sync pulse input
$\overline{ADCSOCAO}$			O	ADC start-of-conversion A
GPIO33	100	80	I/O/Z	General-purpose input/output 33
SCLA			I/OD	I2C clock open-drain bidirectional port
EPWMSYNCO			O	Enhanced PWM external synch pulse output
$\overline{ADCSOCBO}$			O	ADC start-of-conversion B
GPIO34	68	55	I/O/Z	General-purpose input/output 34
COMP2OUT			O	Direct output of Comparator 2
Reserved			–	Reserved
COMP3OUT			O	Direct output of Comparator 3
GPIO35	71	57	I/O/Z	General-purpose input/output 35
TDI			I	JTAG test data input (TDI) with internal pullup. TDI is clocked into the selected register (instruction or data) on a rising edge of TCK.
Reserved			–	Reserved
Reserved			–	Reserved
Reserved			–	Reserved
GPIO36	72	58	I/O/Z	General-purpose input/output 36
TMS			I	JTAG test-mode select (TMS) with internal pullup. This serial control input is clocked into the TAP controller on the rising edge of TCK.
Reserved			–	Reserved
Reserved			–	Reserved
Reserved			–	Reserved
GPIO37	70	56	I/O/Z	General-purpose input/output 37
TDO			O/Z	JTAG scan out, test data output (TDO). The contents of the selected register (instruction or data) are shifted out of TDO on the falling edge of TCK (8 mA drive).
Reserved			–	Reserved
Reserved			–	Reserved
Reserved			–	Reserved

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PIN NAME	PIN NO.		I/O/Z[1]	DESCRIPTION
	PZ PZP	PN PFP		
GPIO38	67	54	I/O/Z	General-purpose input/output 38
XCLKIN			I	External Oscillator Input. The path from this pin to the clock block is not gated by the mux function of this pin. Care must be taken to not enable this path for clocking if it is being used for the other functions.
TCK			I	JTAG test clock with internal pullup
Reserved			–	Reserved
Reserved			–	Reserved
Reserved			–	Reserved
GPIO39	66	53	I/O/Z	General-purpose input/output 39
Reserved			–	Reserved
Reserved			–	Reserved
Reserved			–	Reserved
GPIO40	82	–	I/O/Z	General-purpose input/output 40
EPWM7A			O	Enhanced PWM7 output A and HRPWM channel
SCITXDB			O	SCI-B transmit data
Reserved			–	Reserved
GPIO41	76	–	I/O/Z	General-purpose input/output 41
EPWM7B			O	Enhanced PWM7 output B
SCIRXDB			I	SCI-B receive data
Reserved			–	Reserved
GPIO42	1	–	I/O/Z	General-purpose input/output 42
EPWM8A			O	Enhanced PWM8 output A and HRPWM channel
$\overline{TZ1}$			I	Trip zone input 1
COMP1OUT			O	Direct output of Comparator 1
GPIO43	8	–	I/O/Z	General-purpose input/output 43
EPWM8B			O	Enhanced PWM8 output B
$\overline{TZ2}$			I	Trip zone input 2
COMP2OUT			O	Direct output of Comparator 2
GPIO44	56	–	I/O/Z	General-purpose input/output 44
MFSRA			I/O	McBSP receive frame synch
SCIRXDB			I	SCI-B receive data
EPWM7B			O	Enhanced PWM7 output B
GPIO50	42	–	I/O/Z	General-purpose input/output 50
EQEP1A			I	Enhanced QEP1 input A
MDXA			O	McBSP transmit serial data
$\overline{TZ1}$			I	Trip zone input 1
GPIO51	48	–	I/O/Z	General-purpose input/output 51
EQEP1B			I	Enhanced QEP1 input B
MDRA			I	McBSP receive serial data
$\overline{TZ2}$			I	Trip zone input 2
GPIO52	53	–	I/O/Z	General-purpose input/output 52
EQEP1S			I/O	Enhanced QEP1 strobe
MCLKXA			I/O	McBSP transmit clock
$\overline{TZ3}$			I	Trip zone input 3

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PIN NAME	PIN NO.		I/O/Z[1]	DESCRIPTION
	PZ PZP	PN PFP		
GPIO53	65	–	I/O/Z	General-purpose input/output 53
EQEP1I			I/O	Enhanced QEP1 index
MFSXA			I/O	McBSP transmit frame synch
Reserved			–	Reserved
GPIO54	69	–	I/O/Z	General-purpose input/output 54
SPISIMOA			I/O	SPI-A slave in, master out
EQEP2A			I	Enhanced QEP2 input A
HRCAP1			I	High-Resolution Input Capture 1
GPIO55	75	–	I/O/Z	General-purpose input/output 55
SPISOMIA			I/O	SPI-A slave out, master in
EQEP2B			I	Enhanced QEP2 input B
HRCAP2			I	High-Resolution Input Capture 2
GPIO56	85	–	I/O/Z	General-purpose input/output 56
SPICLKA			I/O	SPI-A clock input/output
EQEP2I			I/O	Enhanced QEP2 index
HRCAP3			I	High-Resolution Input Capture 3
GPIO57	89	–	I/O/Z	General-purpose input/output 57
$\overline{\text{SPISTEA}}$			I/O	SPI-A slave transmit enable input/output
EQEP2S			I/O	Enhanced QEP2 strobe
HRCAP4			I	High-Resolution Input Capture 4
GPIO58	94	–	I/O/Z	General-purpose input/output 58
MCLKRA			I/O	McBSP receive clock
SCITXDB			O	SCI-B transmit data
EPWM7A			O	Enhanced PWM7 output A and HRPWM channel

(1) I = Input, O = Output, Z = High Impedance, OD = Open Drain, ↑ = Pullup, ↓ = Pulldown
(2) The GPIO function (shown in bold italics) is the default at reset. The peripheral signals that are listed under them are alternate functions. For JTAG pins that have the GPIO functionality multiplexed, the input path to the GPIO block is always valid. The output path from the GPIO block and the path to the JTAG block from a pin is enabled or disabled based on the condition of the $\overline{\text{TRST}}$ signal. See the Systems Control and Interrupts chapter of the *TMS320x2806x Technical Reference Manual* .
(3) Depending on your USB application, additional pins may be required to maintain compliance with the USB 2.0 Specification. For more information, see the Universal Serial Bus (USB) Controller chapter of the *TMS320x2806x Technical Reference Manual* .

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7 Specifications

7.1 Absolute Maximum Ratings

Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under the Recommended Operating Conditions is not implied. Exposure to absolute-maximumrated conditions for extended periods may affect device reliability. All voltage values are with respect to VSS, unless otherwise noted.

over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT
Supply voltage	V_{DDIO} (I/O and Flash) with respect to V_{SS}	–0.3	4.6	V
	V_{DD} with respect to V_{SS}	–0.3	2.5	
Analog voltage	V_{DDA} with respect to V_{SSA}	–0.3	4.6	V
Input voltage	V_{IN} (3.3 V)	–0.3	4.6	V
	V_{IN} (X1)	–0.3	2.5	
Output voltage	V_O	–0.3	4.6	V
Input clamp current	Digital input (per pin), I_{IK} ($V_{IN} < V_{SS}$ or $V_{IN} > V_{DDIO}$)(1)	–20	20	mA
	Analog input (per pin), $I_{IKANALOG}$ ($V_{IN} < V_{SSA}$ or $V_{IN} > V_{DDA}$)	–20	20	
	Total for all inputs, $I_{IKTOTAL}$ ($V_{IN} < V_{SS}/V_{SSA}$ or $V_{IN} > V_{DDIO}/V_{DDA}$)	–20	20	
Output clamp current	I_{OK} ($V_O < 0$ or $V_O > V_{DDIO}$)	–20	20	mA
Junction temperature(2)	T_J	–40	150	°C
Storage temperature(2)	T_{stg}	–65	150	°C

(1) Continuous clamp current per pin is ±2 mA.
(2) Long-term high-temperature storage or extended use at maximum temperature conditions may result in a reduction of overall device life. For additional information, see *Semiconductor and IC Package Thermal Metrics*.

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7.2 ESD Ratings – Commercial

			VALUE	UNIT
TMS320F2806x, TMS320F2806xM, TMS320F2806xF, and TMS320F2806xU in 100-pin PZ package				
$V_{(ESD)}$	Electrostatic discharge (ESD)	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±2000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101 or ANSI/ESDA/JEDEC JS-002(2)	±500	
TMS320F2806x, TMS320F2806xM, TMS320F2806xF, and TMS320F2806xU in 80-pin PN package				
$V_{(ESD)}$	Electrostatic discharge (ESD)	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±2000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101 or ANSI/ESDA/JEDEC JS-002(2)	±500	
TMS320F2806x and TMS320F2806xU in 100-pin PZP package				
$V_{(ESD)}$	Electrostatic discharge (ESD)	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±2000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101 or ANSI/ESDA/JEDEC JS-002(2)	±500	
TMS320F2806x and TMS320F2806xU in 80-pin PFP package				
$V_{(ESD)}$	Electrostatic discharge (ESD)	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±2000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101 or ANSI/ESDA/JEDEC JS-002(2)	±500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

7.3 ESD Ratings – Automotive

				VALUE	UNIT
TMS320F2806x-Q1, TMS320F2806xM-Q1, TMS320F2806xF-Q1 in 100-pin PZP package					
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per AEC Q100-002(1)	All pins	±2000	V
		Charged device model (CDM), per AEC Q100-011	All pins	±500	
			Corner pins on 100-pin PZP: 1, 25, 26, 50, 51, 75, 76, 100	±750	
TMS320F2806x-Q1, TMS320F2806xM-Q1, TMS320F2806xF-Q1 in 80-pin PFP packages					
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per AEC Q100-002(1)	All pins	±2000	V
		Charged device model (CDM), per AEC Q100-011	All pins	±500	
			Corner pins on 80-pin PFP: 1, 20, 21, 40, 41, 60, 61, 80	±750	

(1) AEC Q100-002 indicates HBM stressing is done in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

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7.4 Recommended Operating Conditions

		MIN	NOM	MAX	UNIT
Device supply voltage, I/O, V_{DDIO}		2.97	3.3	3.63	V
Device supply voltage CPU, V_{DD} (When internal VREG is disabled and 1.8 V is supplied externally)		1.71	1.8	1.995	V
Supply ground, V_{SS}			0		V
Analog supply voltage, V_{DDA}		2.97	3.3	3.63	V
Analog ground, V_{SSA}			0		V
Device clock frequency (system clock)		2		90	MHz
High-level input voltage, V_{IH} (3.3 V)		2		V_{DDIO} + 0.3	V
Low-level input voltage, V_{IL} (3.3 V)		V_{SS} – 0.3		0.8	V
High-level output source current, $V_{OH} = V_{OH(MIN)}$, I_{OH}	All GPIO/AIO pins			–4	mA
	Group 2(1)			–8	
Low-level output sink current, $V_{OL} = V_{OL(MAX)}$, I_{OL}	All GPIO/AIO pins			4	mA
	Group 2(1)			8	
Junction temperature, T_J	T version	–40		105	°C
	S version	–40		125	
Ambient temperature, T_A	Q version(2) (AEC Q100 qualification)	–40		125	°C

(1) Group 2 pins are as follows: GPIO16, GPIO17, GPIO18, GPIO19, GPIO28, GPIO29, GPIO36, GPIO37.
(2) The Q temperature option is ***not*** available on the 2806x**U** devices.

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7.5 Power Consumption Summary

7.5.1 TMS320F2806x Current Consumption at 90-MHz SYSCLKOUT

MODE	TEST CONDITIONS	VREG ENABLED						VREG DISABLED							
		I_{DDIO} (1)		I_{DDA} (2)		I_{DD3VFL}		I_{DD}		I_{DDIO} (1)		I_{DDA} (2)		I_{DD3VFL}	
		TYP(3)	MAX	TYP(3)	MAX	TYP(3)	MAX	TYP(3)	MAX	TYP(3)	MAX	TYP(3)	MAX	TYP(3)	MAX
Operational (Flash)	The following peripheral clocks are enabled: • ePWM1, ePWM2, ePWM3, ePWM4, ePWM5, ePWM6, ePWM7, ePWM8 • eCAP1, eCAP2, eCAP3 • eQEP1, eQEP2 • eCAN • CLA • HRPWM • SCI-A, SCI-B • SPI-A, SPI-B • ADC • I2C • COMP1, COMP2, COMP3 • CPU-TIMER0, CPU-TIMER1, CPU-TIMER2 • McBSP • USB All PWM pins are toggled at 90 kHz. All I/O pins are left unconnected.(4) (6) Code is running out of flash with 3 wait states. XCLKOUT is turned off.	185 mA(7)	245 mA(7)	16 mA	22 mA	35 mA	40 mA	165 mA(7)	220 mA(7)	15 mA	20 mA	16 mA	22 mA	35 mA	40 mA
IDLE	Flash is powered down. XCLKOUT is turned off. All peripheral clocks are turned off.	22 mA	27 mA	15 µA	25 µA	5 µA	10 µA	21 mA	26 mA	120 µA	400 µA	15 µA	25 µA	5 µA	10 µA
STANDBY	Flash is powered down. Peripheral clocks are off.	9 mA	11 mA	15 µA	25 µA	5 µA	10 µA	8 mA	10 mA	120 µA	400 µA	15 µA	25 µA	5 µA	10 µA
HALT	Flash is powered down. Peripheral clocks are off. Input clock is disabled. (5)	75 µA		15 µA	25 µA	5 µA	10 µA	25 µA(8)		40 µA		15 µA	25 µA	5 µA	10 µA

(1) I_{DDIO} current is dependent on the electrical loading on the I/O pins.
(2) To realize the I_{DDA} currents shown for IDLE, STANDBY, and HALT, clock to the ADC module must be turned off explicitly by writing to the PCLKCR0 register.
(3) The TYP numbers are applicable over room temperature and nominal voltage.
(4) The following is done in a loop:
- Data is continuously transmitted out of SPI-A, SPI-B, SCI-A, eCAN-A, McBSP-A, and I2C ports.
- The hardware multiplier is exercised.
- Watchdog is reset.
- ADC is performing continuous conversion.
- COMP1 and COMP2 are continuously switching voltages.
- GPIO17 is toggled.

(5) If a quartz crystal or ceramic resonator is used as the clock source, the HALT mode shuts down the on-chip crystal oscillator.
(6) CLA is continuously performing polynomial calculations.

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(7) For F2806x devices that do not have CLA, subtract the I_{DD} current number for CLA (see Table 7-1) from the I_{DD} (VREG disabled)/I_{DDIO} (VREG enabled) current numbers listed in Section 7.5.1 for operational mode.

(8) To realize the I_{DD} number shown for HALT mode, the following must be done:

- PLL2 must be shut down by clearing bit 2 of the PLLCTL register.
- A value of 0x00FF must be written to the HRCAL register at address 0x6822.

Note

The peripheral - I/O multiplexing implemented in the device prevents all available peripherals from being used at the same time. This is because more than one peripheral function may share an I/O pin. It is, however, possible to turn on the clocks to all the peripherals at the same time, although such a configuration is not useful. If this is done, the current drawn by the device will be more than the numbers specified in the current consumption tables.

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7.5.2 Reducing Current Consumption

The 2806x devices incorporate a method to reduce the device current consumption. Because each peripheral unit has an individual clock-enable bit, significant reduction in current consumption can be achieved by turning off the clock to any peripheral module that is not used in a given application. Furthermore, any one of the three low-power modes could be taken advantage of to reduce the current consumption even further. Table 7-1 indicates the typical reduction in current consumption achieved by turning off the clocks.

Table 7-1. Typical Current Consumption by Various Peripherals (at 90 MHz)

PERIPHERAL MODULE(1) (3)	I_{DD} CURRENT REDUCTION (mA)
ADC	2(2)
I2C	3
ePWM	2
eCAP	2
eQEP	2
SCI	2
SPI	2
COMP/DAC	1
HRPWM	3
HRCAP	3
USB	12
CPU-TIMER	1
Internal zero-pin oscillator	0.5
CAN	2.5
CLA	20
McBSP	6

(1) All peripheral clocks (except CPU Timer clock) are disabled upon reset. Writing to or reading from peripheral registers is possible only after the peripheral clocks are turned on.
(2) This number represents the current drawn by the digital portion of the ADC module. Turning off the clock to the ADC module results in the elimination of the current drawn by the analog portion of the ADC (I_{DDA}) as well.
(3) For peripherals with multiple instances, the current quoted is per module. For example, the 2 mA value quoted for ePWM is for one ePWM module.

Note

I_{DDIO} current consumption is reduced by 15 mA (typical) when XCLKOUT is turned off.

Note

The baseline I_{DD} current (current when the core is executing a dummy loop with no peripherals enabled) is 40 mA, typical. To arrive at the I_{DD} current for a given application, the current-drawn by the peripherals (enabled by that application) must be added to the baseline I_{DD} current.

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Following are other methods to reduce power consumption further:

- The flash module may be powered down if code is run off SARAM. This results in a current reduction of 18 mA (typical) in the V_{DD} rail and 13 mA (typical) in the V_{DDIO} rail.
- Savings in I_{DDIO} may be realized by disabling the pullups on pins that assume an output function.
- To realize the lowest V_{DDA} current consumption in a low-power mode, see the respective analog chapter of the *TMS320x2806x Technical Reference Manual* to ensure each module is powered down as well.
- Power savings can be achieved by powering down the flash. This must be done by code running off RAM (not flash).

7.5.3 Current Consumption Graphs (VREG Enabled)

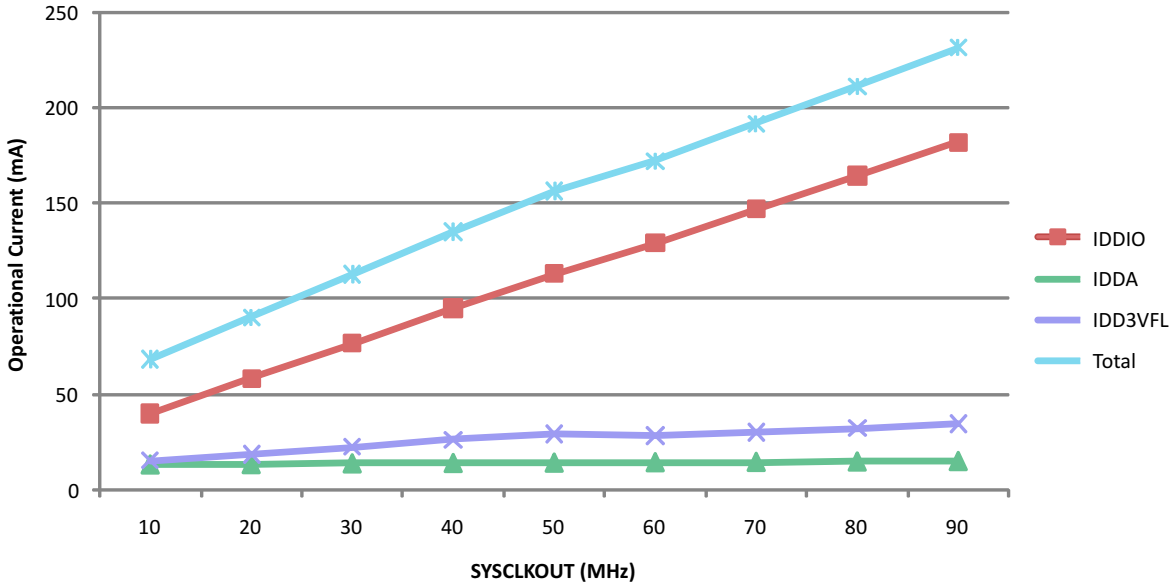

Figure 7-1. Typical Operational Current (Flash) Versus Frequency (Internal VREG)

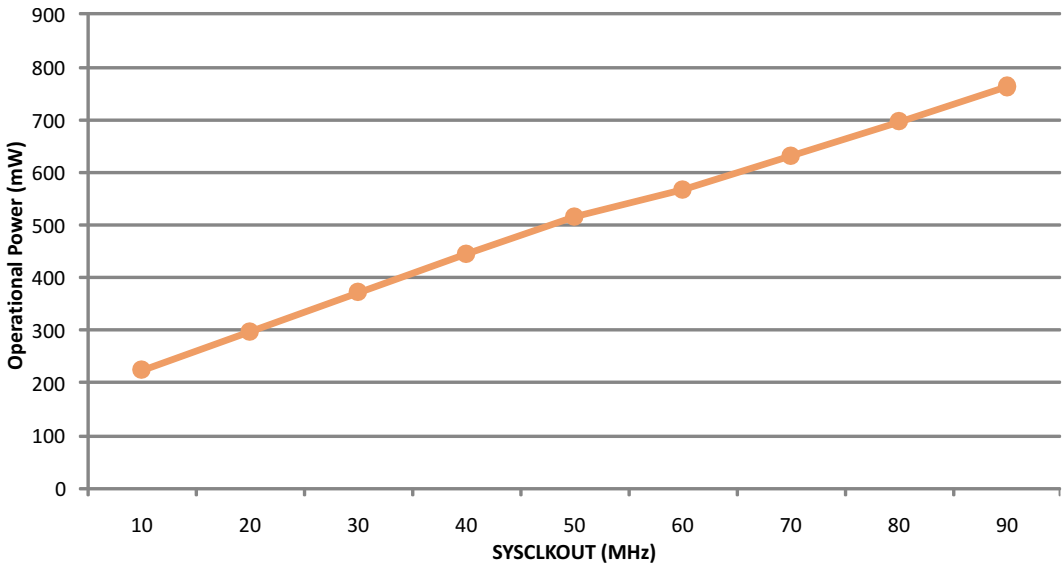

Figure 7-2. Typical Operational Power Versus Frequency (Internal VREG)

7.6 Electrical Characteristics

over recommended operating conditions (unless otherwise noted)(1)

PARAMETER			TEST CONDITIONS		MIN	TYP	MAX	UNIT
V_{OH}	High-level output voltage		I_{OH} = I_{OH} MAX		2.4			V
			I_{OH} = 50 µA		V_{DDIO} – 0.2			
V_{OL}	Low-level output voltage		I_{OL} = I_{OL} MAX				0.4	V
I_{IL}	Input current (low level)	Pin with pullup enabled	V_{DDIO} = 3.3 V, V_{IN} = 0 V	All GPIO	–80	–140	–205	µA
				$\overline{XRS}$ pin	–230	–300	–375	
		Pin with pulldown enabled	V_{DDIO} = 3.3 V, V_{IN} = 0 V				±2	
I_{IH}	Input current (high level)	Pin with pullup enabled	V_{DDIO} = 3.3 V, V_{IN} = V_{DDIO}				±2	µA
		Pin with pulldown enabled	V_{DDIO} = 3.3 V, V_{IN} = V_{DDIO}		28	50	80	
I_{OZ}	Output current, pullup or pulldown disabled		V_O = V_{DDIO} or 0 V				±2	µA
C_I	Input capacitance					2		pF
	V_{DDIO} BOR trip point		Falling V_{DDIO}		2.50	2.78	2.96	V
	V_{DDIO} BOR hysteresis					35		mV
	Supervisor reset release delay time		Time after BOR/POR/OVR event is removed to $\overline{XRS}$ release		400		800	µs
	VREG V_{DD} output		Internal VREG on			1.9		V

(1) When the on-chip VREG is used, its output is monitored by the POR/BOR circuit, which will reset the device should the core voltage (V_{DD}) go out of range.

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7.7 Thermal Resistance Characteristics

7.7.1 PFP PowerPAD Package

		°C/W(1)	AIR FLOW (lfm)(2)
$R\Theta_{JC}$	Junction-to-case thermal resistance	9.4	0
$R\Theta_{JB}$	Junction-to-board thermal resistance	4.6	0
$R\Theta_{JA}$ (High k PCB)	Junction-to-free air thermal resistance	25.8	0
		16.3	150
		15.2	250
		13.6	500
Psi_{JT}	Junction-to-package top	0.3	0
		0.4	150
		0.4	250
		0.5	500
Psi_{JB}	Junction-to-board	4.6	0
		4.4	150
		4.3	250
		4.3	500

(1) These values are based on a JEDEC-defined 2S2P system (with the exception of the Theta JC [$R\Theta_{JC}$] value, which is based on a JEDEC-defined 1S0P system) and will change based on environment as well as application. For more information, see these EIA/JEDEC standards:

- JESD51-2, *Integrated Circuits Thermal Test Method Environmental Conditions - Natural Convection (Still Air)*
- JESD51-3, *Low Effective Thermal Conductivity Test Board for Leaded Surface Mount Packages*
- JESD51-7, *High Effective Thermal Conductivity Test Board for Leaded Surface Mount Packages*
- JESD51-9, *Test Boards for Area Array Surface Mount Package Thermal Measurements*

(2) lfm = linear feet per minute

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7.7.2 PZP PowerPAD Package

		°C/W(1)	AIR FLOW (lfm)(2)
$R\Theta_{JC}$	Junction-to-case thermal resistance	9.4	0
$R\Theta_{JB}$	Junction-to-board thermal resistance	4.4	0
$R\Theta_{JA}$ (High k PCB)	Junction-to-free air thermal resistance	24.4	0
		15.1	150
		13.9	250
		12.4	500
Psi_{JT}	Junction-to-package top	0.3	0
		0.4	150
		0.4	250
		0.5	500
Psi_{JB}	Junction-to-board	4.5	0
		4.2	150
		4.2	250
		4.2	500

(1) These values are based on a JEDEC-defined 2S2P system (with the exception of the Theta JC [$R\Theta_{JC}$] value, which is based on a JEDEC-defined 1S0P system) and will change based on environment as well as application. For more information, see these EIA/JEDEC standards:

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- JESD51-9, *Test Boards for Area Array Surface Mount Package Thermal Measurements*

(2) lfm = linear feet per minute

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7.7.3 PN Package

		°C/W(1)	AIR FLOW (lfm)(2)
$R\Theta_{JC}$	Junction-to-case thermal resistance	7.9	0
$R\Theta_{JB}$	Junction-to-board thermal resistance	15.6	0
$R\Theta_{JA}$ (High k PCB)	Junction-to-free air thermal resistance	41.1	0
		31.2	150
		29.7	250
		27.5	500
Psi_{JT}	Junction-to-package top	0.4	0
		0.6	150
		0.7	250
		0.9	500
Psi_{JB}	Junction-to-board	15.3	0
		14.6	150
		14.4	250
		14.1	500

(1) These values are based on a JEDEC-defined 2S2P system (with the exception of the Theta JC [$R\Theta_{JC}$] value, which is based on a JEDEC-defined 1S0P system) and will change based on environment as well as application. For more information, see these EIA/JEDEC standards:

- JESD51-2, *Integrated Circuits Thermal Test Method Environmental Conditions - Natural Convection (Still Air)*
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- JESD51-7, *High Effective Thermal Conductivity Test Board for Leaded Surface Mount Packages*
- JESD51-9, *Test Boards for Area Array Surface Mount Package Thermal Measurements*

(2) lfm = linear feet per minute

7.7.4 PZ Package

		°C/W(1)	AIR FLOW (lfm)(2)
$R\Theta_{JC}$	Junction-to-case thermal resistance	7.2	0
$R\Theta_{JB}$	Junction-to-board thermal resistance	19.6	0
$R\Theta_{JA}$ (High k PCB)	Junction-to-free air thermal resistance	42.2	0
		32.4	150
		30.9	250
		28.7	500
Psi_{JT}	Junction-to-package top	0.4	0
		0.6	150
		0.7	250
		0.9	500
Psi_{JB}	Junction-to-board	19.1	0
		18.2	150
		17.9	250
		14.1	500

(1) These values are based on a JEDEC-defined 2S2P system (with the exception of the Theta JC [$R\Theta_{JC}$] value, which is based on a JEDEC-defined 1S0P system) and will change based on environment as well as application. For more information, see these EIA/JEDEC standards:

- JESD51-2, *Integrated Circuits Thermal Test Method Environmental Conditions - Natural Convection (Still Air)*
- JESD51-3, *Low Effective Thermal Conductivity Test Board for Leaded Surface Mount Packages*
- JESD51-7, *High Effective Thermal Conductivity Test Board for Leaded Surface Mount Packages*
- JESD51-9, *Test Boards for Area Array Surface Mount Package Thermal Measurements*

(2) lfm = linear feet per minute

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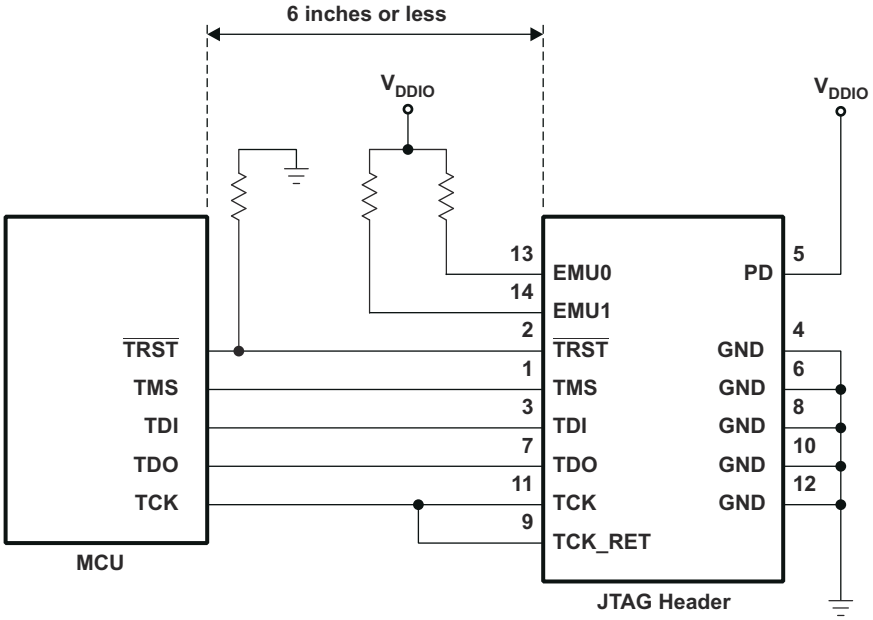
7.8 Thermal Design Considerations

Based on the end application design and operational profile, the I_{DD} and I_{DDIO} currents could vary. Systems that exceed the recommended maximum power dissipation in the end product may require additional thermal enhancements. Ambient temperature (T_A) varies with the end application and product design. The critical factor that affects reliability and functionality is T_J, the junction temperature, not the ambient temperature. Hence, care should be taken to keep T_J within the specified limits. T_{case} should be measured to estimate the operating junction temperature T_J. T_{case} is normally measured at the center of the package top-side surface. The thermal application report *Semiconductor and IC Package Thermal Metrics* helps to understand the thermal metrics and definitions.

7.9 Debug Probe Connection Without Signal Buffering for the MCU

Figure 7-3 shows the connection between the MCU and JTAG header for a single-processor configuration. If the distance between the JTAG header and the MCU is greater than 6 inches, the debug signals must be buffered. If the distance is less than 6 inches, buffering is typically not needed. Figure 7-3 shows the simpler, no-buffering situation. For the pullup and pulldown resistor values, see Section 6.2.



A. See Figure 8-54 for JTAG/GPIO multiplexing.

Figure 7-3. Debug Probe Connection Without Signal Buffering for the MCU

Note

The 2806x devices do not have EMU0/EMU1 pins. For designs that have a JTAG Header onboard, the EMU0/EMU1 pins on the header must be tied to V_{DDIO} through a 4.7-kΩ (typical) resistor.

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7.10 Parameter Information

7.10.1 Timing Parameter Symbology

Timing parameter symbols used are created in accordance with JEDEC Standard 100. To shorten the symbols, some of the pin names and other related terminology have been abbreviated as follows:

LOWERCASE SUBSCRIPTS AND THEIR MEANINGS:		LETTERS AND SYMBOLS AND THEIR MEANINGS:	
a	access time	H	High
c	cycle time (period)	L	Low
d	delay time	V	Valid
f	fall time	X	Unknown, changing, or don't care level
h	hold time	Z	High impedance
r	rise time		
su	setup time		
t	transition time		
v	valid time		
w	pulse duration (width)		

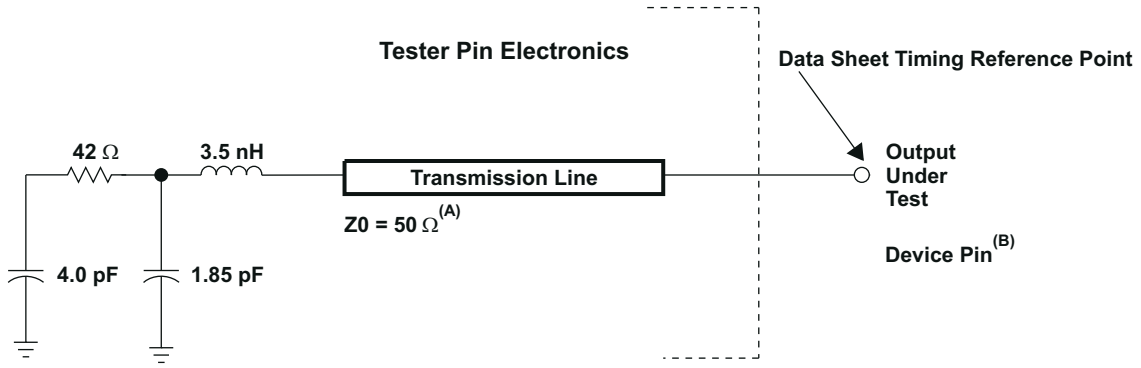
7.10.2 General Notes on Timing Parameters

All output signals from the 28x devices (including XCLKOUT) are derived from an internal clock such that all output transitions for a given half-cycle occur with a minimum of skewing relative to each other.

The signal combinations shown in the following timing diagrams may not necessarily represent actual cycles. For actual cycle examples, see the appropriate cycle description section of this document.

7.11 Test Load Circuit

This test load circuit is used to measure all switching characteristics provided in this document.



A. Input requirements in this data sheet are tested with an input slew rate of < 4 Volts per nanosecond (4 V/ns) at the device pin.

B. The data sheet provides timing at the device pin. For output timing analysis, the tester pin electronics and its transmission line effects must be taken into account. A transmission line with a delay of 2 ns or longer can be used to produce the desired transmission line effect. The transmission line is intended as a load only. It is not necessary to add or subtract the transmission line delay (2 ns or longer) from the data sheet timing.

Figure 7-4. 3.3-V Test Load Circuit

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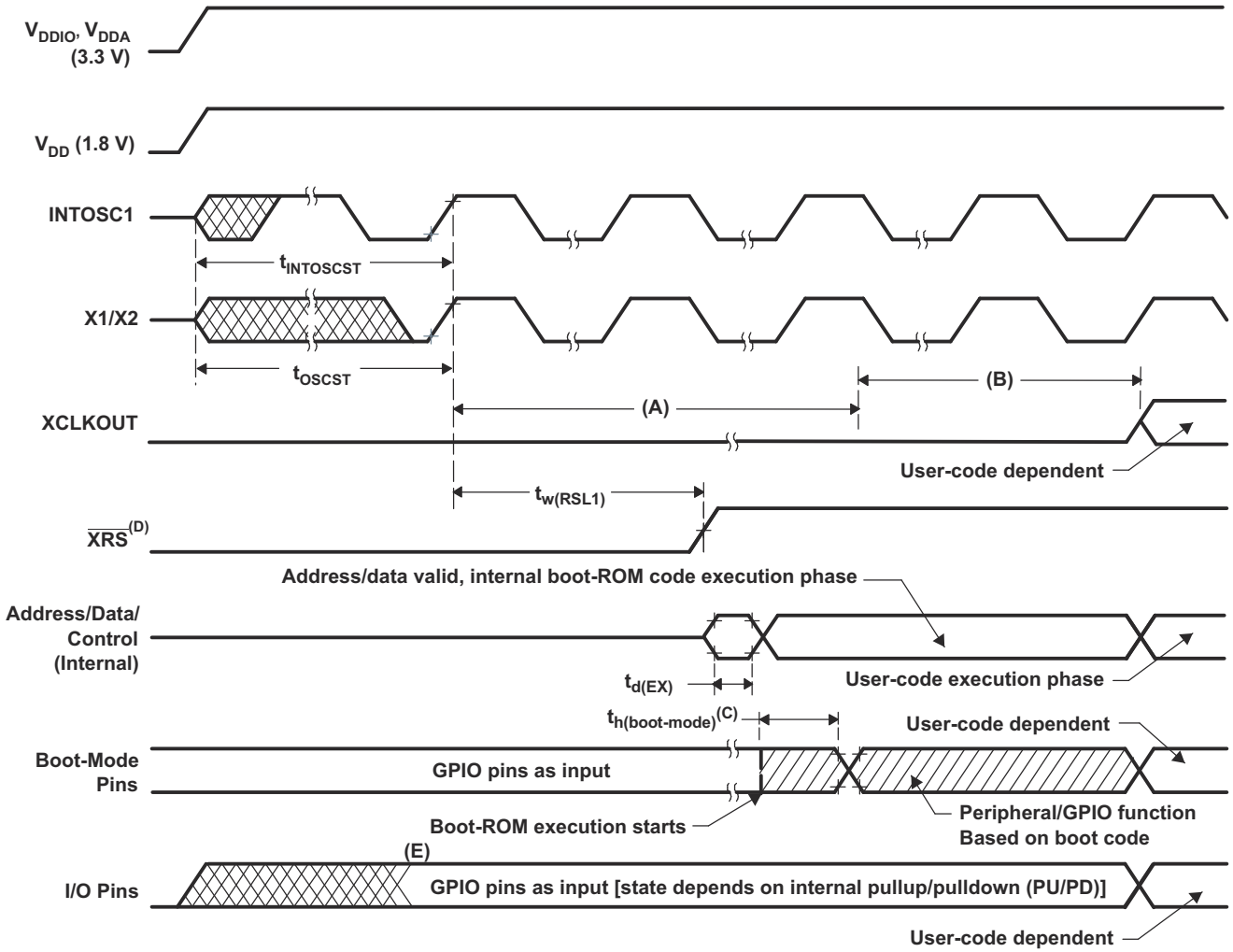
7.12 Power Sequencing

There is no power sequencing requirement needed to ensure the device is in the proper state after reset or to prevent the I/Os from glitching during power up or power down (GPIO19, GPIO26–27, GPIO34–38 do not have glitch-free I/Os). No voltage larger than a diode drop (0.7 V) above V_{DDIO} should be applied to any digital pin (for analog pins, this value is 0.7 V above V_{DDA}) before powering up the device. Voltages applied to pins on an unpowered device can bias internal p-n junctions in unintended ways and produce unpredictable results.



A. Upon power up, SYSCLKOUT is OSCCLK/4. Because the XCLKOUTDIV bits in the XCLK register come up with a reset state of 0, SYSCLKOUT is further divided by 4 before it appears at XCLKOUT. XCLKOUT = OSCCLK/16 during this phase.

B. Boot ROM configures the DIVSEL bits for /1 operation. XCLKOUT = OSCCLK/4 during this phase. XCLKOUT will not be visible at the pin until explicitly configured by user code.

C. After reset, the boot ROM code samples Boot Mode pins. Based on the status of the Boot Mode pin, the boot code branches to destination memory or boot code function. If boot ROM code executes after power-on conditions (in debugger environment), the boot code execution time is based on the current SYSCLKOUT speed. The SYSCLKOUT will be based on user environment and could be with or without PLL enabled.

D. Using the $\overline{XRS}$ pin is optional due to the on-chip POR circuitry.

E. The internal pullup or pulldown will take effect when BOR is driven high.

Figure 7-5. Power-on Reset

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7.12.1 Reset ($\overline{\text{XRS}}$) Timing Requirements

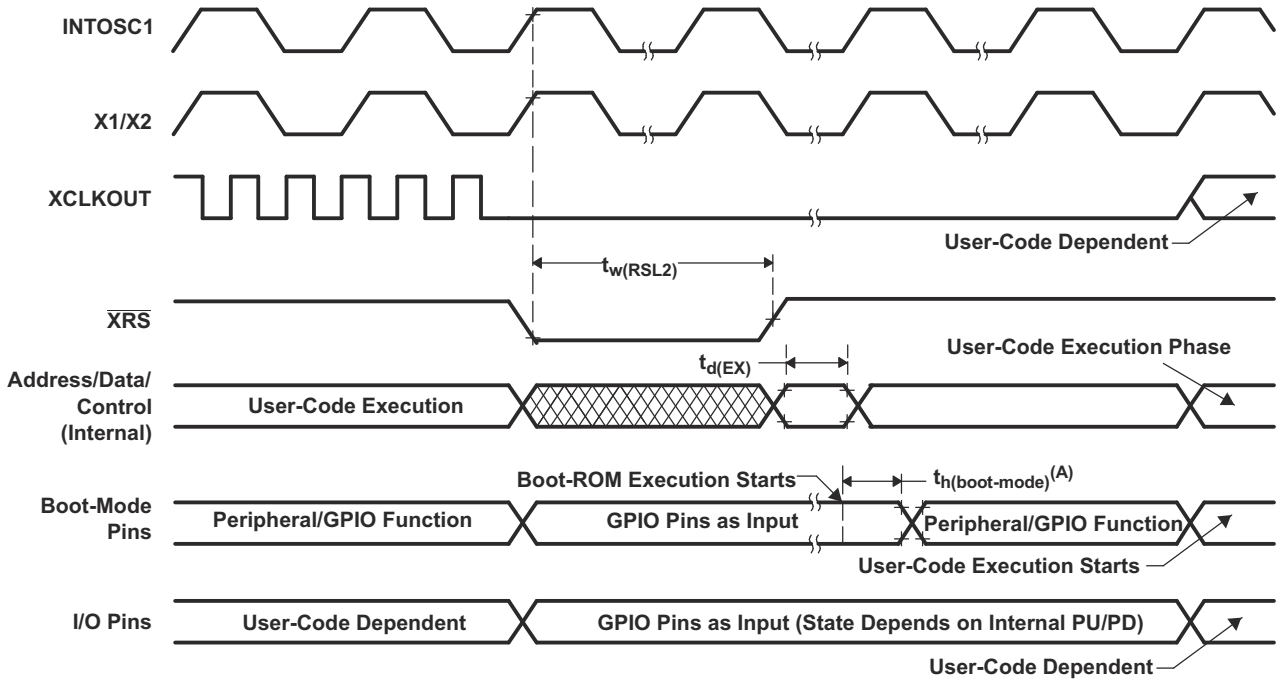
		MIN	MAX	UNIT
$t_{h(boot\text{-}mode)}$	Hold time for boot-mode pins	$1000t_{c(SCO)}$		cycles
$t_{w(RSL2)}$	Pulse duration, $\overline{\text{XRS}}$ low on warm reset	$32t_{c(OSCCLK)}$		cycles

7.12.2 Reset ($\overline{\text{XRS}}$) Switching Characteristics

over recommended operating conditions (unless otherwise noted)

PARAMETER		MIN	TYP	MAX	UNIT
$t_{w(RSL1)}$	Pulse duration, $\overline{\text{XRS}}$ driven by device		600		µs
$t_{w(WDRS)}$	Pulse duration, reset pulse generated by watchdog		$512t_{c(OSCCLK)}$		cycles
$t_{d(EX)}$	Delay time, address/data valid after $\overline{\text{XRS}}$ high		$32t_{c(OSCCLK)}$		cycles
$t_{INTOSCST}$	Start-up time, internal zero-pin oscillator		3		µs
t_{OSCST} (1)	On-chip crystal-oscillator start-up time	1	10		ms

(1) Dependent on crystal/resonator and board design.



A. After reset, the Boot ROM code samples BOOT Mode pins. Based on the status of the Boot Mode pin, the boot code branches to destination memory or boot code function. If Boot ROM code executes after power-on conditions (in debugger environment), the Boot code execution time is based on the current SYSCLKOUT speed. The SYSCLKOUT will be based on user environment and could be with or without PLL enabled.

Figure 7-6. Warm Reset

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Figure 7-7 shows an example for the effect of writing into PLLCR register. In the first phase, PLLCR = 0x0004 and SYSCLKOUT = OSCCLK × 2. The PLLCR is then written with 0x0008. Right after the PLLCR register is written, the PLL lock-up phase begins. During this phase, SYSCLKOUT = OSCCLK/2. After the PLL lock-up is complete, SYSCLKOUT reflects the new operating frequency, OSCCLK × 4.

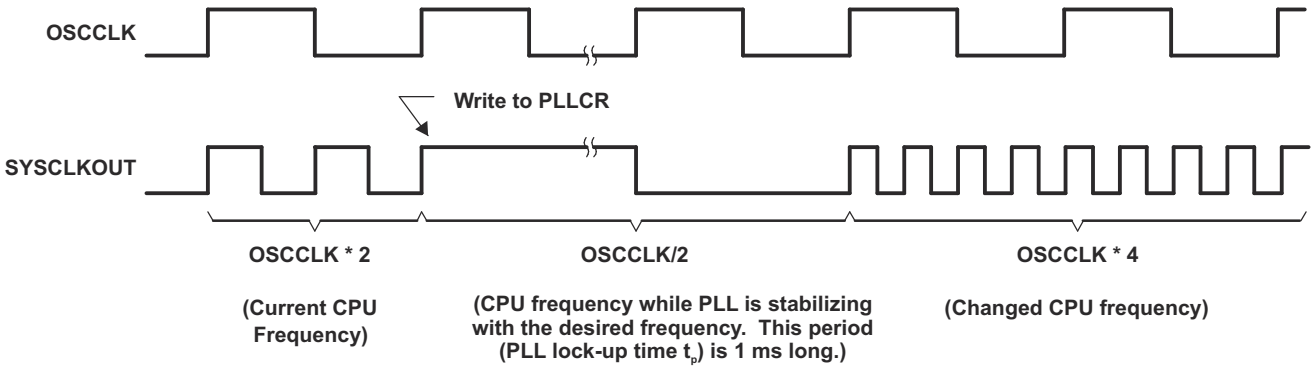

Figure 7-7. Example of Effect of Writing Into PLLCR Register

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7.13 Clock Specifications

7.13.1 Device Clock Table

This section provides the timing requirements and switching characteristics for the various clock options available on the 2806x MCUs. Section 7.13.1.1 lists the cycle times of various clocks.

7.13.1.1 2806x Clock Table and Nomenclature (90-MHz Devices)

		MIN	NOM	MAX	UNIT
SYSCLKOUT	$t_{c(SCO)}$, Cycle time	11.11		500	ns
	Frequency	2		90	MHz
LSPCLK(1)	$t_{c(LCO)}$, Cycle time	11.11	44.4(2)		ns
	Frequency		22.5(2)	90	MHz
ADC clock	$t_{c(ADCCLK)}$, Cycle time	22.22			ns
	Frequency			45	MHz

(1) Lower LSPCLK will reduce device power consumption.
(2) This is the default reset value if SYSCLKOUT = 90 MHz.

7.13.1.2 Device Clocking Requirements/Characteristics

		MIN	NOM	MAX	UNIT
On-chip oscillator (X1/X2 pins) (Crystal/Resonator)	$t_{c(OSC)}$, Cycle time	50		200	ns
	Frequency	5		20	MHz
External oscillator/clock source (XCLKIN pin) — PLL Enabled	$t_{c(CI)}$, Cycle time (C8)	33.3		200	ns
	Frequency	5		30	MHz
External oscillator/clock source (XCLKIN pin) — PLL Disabled	$t_{c(CI)}$, Cycle time (C8)	11.11		250	ns
	Frequency	4		90	MHz
Limp mode SYSCLKOUT (with /2 enabled)	Frequency range		1 to 5		MHz
XCLKOUT	$t_{c(XCO)}$, Cycle time (C1)	44.44		2000	ns
	Frequency	0.5		22.5	MHz
PLL lock time(1)	t_p			1	ms

(1) The PLLLOCKPRD register must be updated based on the number of OSCCLK cycles. If the zero-pin internal oscillators (10 MHz) are used as the clock source, then the PLLLOCKPRD register must be written with a value of 10,000 (minimum).

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7.13.1.3 Internal Zero-Pin Oscillator (INTOSC1/INTOSC2) Characteristics

PARAMETER		MIN	TYP	MAX	UNIT
Internal zero-pin oscillator 1 (INTOSC1) at 30°C(1) (2)	Frequency		10.000		MHz
Internal zero-pin oscillator 2 (INTOSC2) at 30°C(1) (2)	Frequency		10.000		MHz
Step size (coarse trim)			55		kHz
Step size (fine trim)			14		kHz
Temperature drift(3)			3.03	4.85	kHz/°C
Voltage (V_{DD}) drift(3)			175		Hz/mV

(1) Oscillator frequency will vary over temperature, see Figure 7-8. To compensate for oscillator temperature drift, see the *Oscillator Compensation Guide* and C2000Ware. .
(2) Frequency range ensured only when VREG is enabled, $\overline{\text{VREGENZ}}$ = V_{SS}.
(3) Output frequency of the internal oscillators follows the direction of both the temperature gradient and voltage (V_{DD}) gradient. For example:
- Increase in temperature will cause the output frequency to increase per the temperature coefficient.
- Decrease in voltage (V_{DD}) will cause the output frequency to decrease per the voltage coefficient.

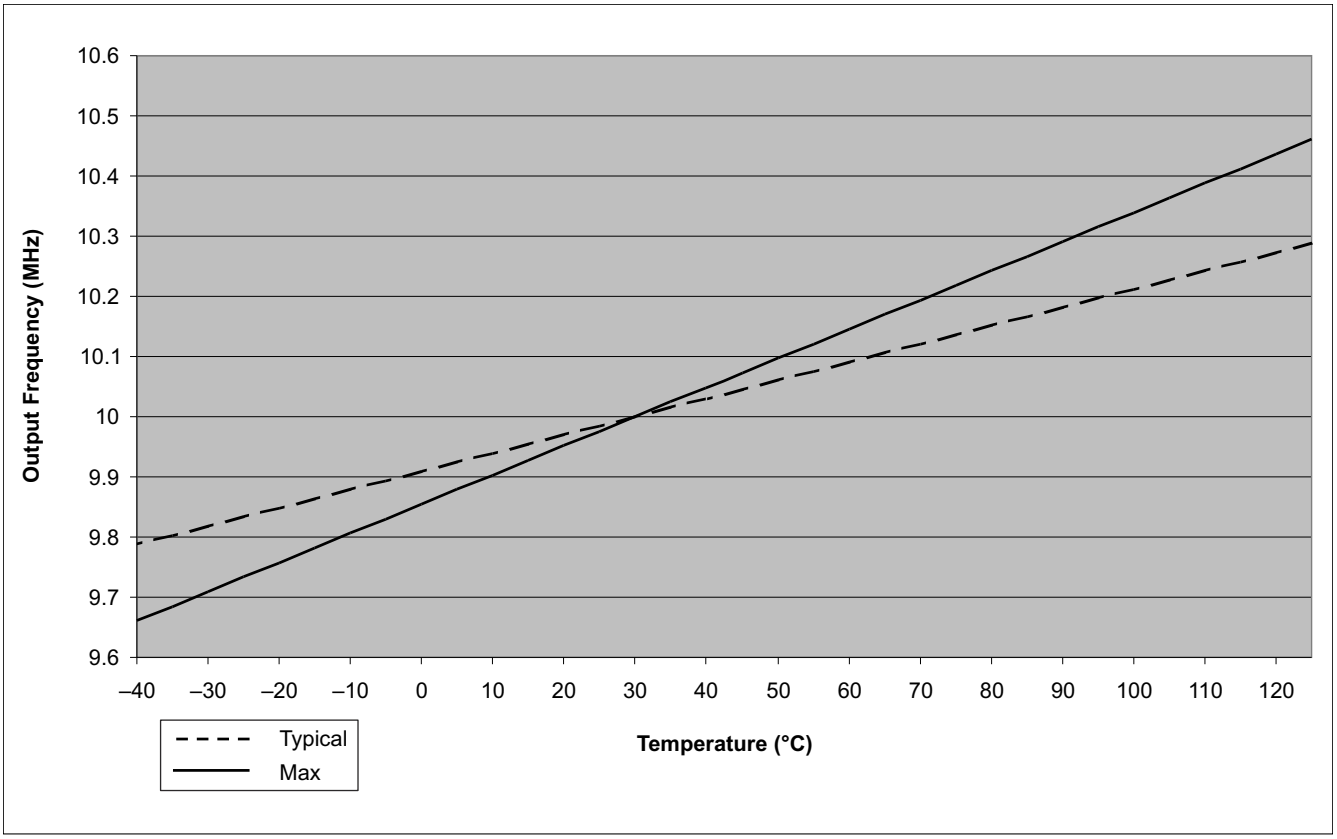

Figure 7-8. Zero-Pin Oscillator Frequency Movement With Temperature

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7.13.2 Clock Requirements and Characteristics

7.13.2.1 XCLKIN Timing Requirements – PLL Enabled

NO.			MIN	MAX	UNIT
C9	$t_{f(CI)}$	Fall time, XCLKIN		6	ns
C10	$t_{r(CI)}$	Rise time, XCLKIN		6	ns
C11	$t_{w(CIL)}$	Pulse duration, XCLKIN low as a percentage of $t_{c(OSCCLK)}$	45%	55%	
C12	$t_{w(CIH)}$	Pulse duration, XCLKIN high as a percentage of $t_{c(OSCCLK)}$	45%	55%	

7.13.2.2 XCLKIN Timing Requirements – PLL Disabled

NO.				MIN	MAX	UNIT
C9	$t_{f(CI)}$	Fall time, XCLKIN	Up to 20 MHz		6	ns
			20 MHz to 90 MHz		2	
C10	$t_{r(CI)}$	Rise time, XCLKIN	Up to 20 MHz		6	ns
			20 MHz to 90 MHz		2	
C11	$t_{w(CIL)}$	Pulse duration, XCLKIN low as a percentage of $t_{c(OSCCLK)}$		45%	55%	
C12	$t_{w(CIH)}$	Pulse duration, XCLKIN high as a percentage of $t_{c(OSCCLK)}$		45%	55%	

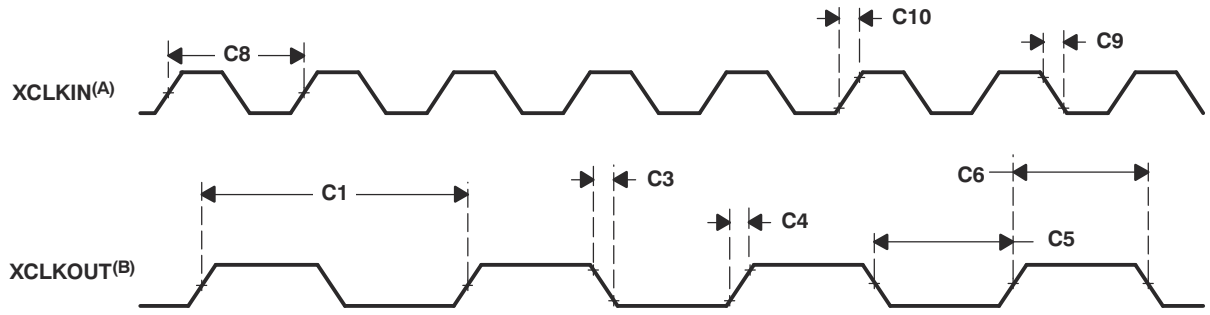
The possible configuration modes are shown in Table 8-15.

7.13.2.3 XCLKOUT Switching Characteristics (PLL Bypassed or Enabled)

over recommended operating conditions (unless otherwise noted)(1) (2)

NO.	PARAMETER		MIN	MAX	UNIT
C3	$t_{f(XCO)}$	Fall time, XCLKOUT		5	ns
C4	$t_{r(XCO)}$	Rise time, XCLKOUT		5	ns
C5	$t_{w(XCOL)}$	Pulse duration, XCLKOUT low	H – 2	H + 2	ns
C6	$t_{w(XCOH)}$	Pulse duration, XCLKOUT high	H – 2	H + 2	ns

(1) A load of 40 pF is assumed for these parameters.
(2) $H = 0.5t_{c(XCO)}$



A. The relationship of XCLKIN to XCLKOUT depends on the divide factor chosen. The waveform relationship shown is intended to illustrate the timing parameters only and may differ based on actual configuration.
B. XCLKOUT configured to reflect SYSCLKOUT.

Figure 7-9. Clock Timing

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7.14 Flash Timing

7.14.1 Flash/OTP Endurance for T Temperature Material

		ERASE/PROGRAM TEMPERATURE(1)	MIN	TYP	MAX	UNIT
N_f	Flash endurance for the array (write/erase cycles)	0°C to 105°C (ambient)	20000	50000		cycles
N_{OTP}	OTP endurance for the array (write cycles)	0°C to 30°C (ambient)			1	write

(1) Write/erase operations outside of the temperature ranges indicated are not specified and may affect the endurance numbers.

7.14.2 Flash/OTP Endurance for S Temperature Material

		ERASE/PROGRAM TEMPERATURE(1)	MIN	TYP	MAX	UNIT
N_f	Flash endurance for the array (write/erase cycles)	0°C to 125°C (ambient)	20000	50000		cycles
N_{OTP}	OTP endurance for the array (write cycles)	0°C to 30°C (ambient)			1	write

(1) Write/erase operations outside of the temperature ranges indicated are not specified and may affect the endurance numbers.

7.14.3 Flash/OTP Endurance for Q Temperature Material

		ERASE/PROGRAM TEMPERATURE(1) (2)	MIN	TYP	MAX	UNIT
N_f	Flash endurance for the array (write/erase cycles)	–40°C to 125°C (ambient)	20000	50000		cycles
N_{OTP}	OTP endurance for the array (write cycles)	–40°C to 30°C (ambient)			1	write

(1) Write/erase operations outside of the temperature ranges indicated are not specified and may affect the endurance numbers.
(2) The "Q" temperature option is ***not*** available on the 2806x**U** devices.

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7.14.4 Flash Parameters at 90-MHz SYSCLKOUT

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
Program Time(1)	16-Bit Word			50		µs
	16K Sector			500	2000(2)	ms
	8K Sector			250	2000(2)	ms
	4K Sector			125	2000(2)	ms
Erase Time(3)	16K Sector			2	15(2)	s
	8K Sector			2	15(2)	
	4K Sector			2	15(2)	
I_{DDP} (4)	V_{DD} current consumption during Erase/Program cycle	VREG disabled		80		mA
I_{DDIOP} (4)	V_{DDIO} current consumption during Erase/Program cycle			60		
I_{DDIOP} (4)	V_{DDIO} current consumption during Erase/Program cycle	VREG enabled		120		mA

(1) Program time is at the maximum device frequency. The programming time indicated in this table is applicable only when all the required code/data is available in the device RAM, ready for programming. Program time includes overhead of the flash state machine but does not include the time to transfer the following into RAM:

- the code that uses flash API to program the flash
- the Flash API itself
- Flash data to be programmed

(2) The parameters mentioned in the MAX column are for the first 100 Erase/Program cycles.

(3) The on-chip flash memory is in an erased state when the device is shipped from TI. As such, erasing the flash memory is not required before programming, when programming the device for the first time. However, the erase operation is needed on all subsequent programming operations.

(4) Typical parameters as seen at room temperature including function call overhead, with all peripherals off. It is important to maintain a stable power supply during the entire flash programming process. It is conceivable that device current consumption during flash programming could be higher than normal operating conditions. The power supply used should ensure V_{MIN} on the supply rails at all times, as specified in the Recommended Operating Conditions of the data sheet. Any brownout or interruption to power during erasing/programming could potentially corrupt the password locations and lock the device permanently. Powering a target board (during flash programming) through the USB port is not recommended, as the port may be unable to respond to the power demands placed during the programming process.

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7.14.5 Flash/OTP Access Timing

PARAMETER		MIN	MAX	UNIT
$t_{a(fp)}$	Paged Flash access time	36		ns
$t_{a(fr)}$	Random Flash access time	36		ns
$t_{a(OTP)}$	OTP access time	60		ns

7.14.6 Flash Data Retention Duration

PARAMETER		TEST CONDITIONS	MIN	MAX	UNIT
$t_{retention}$	Data retention duration	T_J = 55°C	15		years

Table 7-2. Minimum Required Flash/OTP Wait States at Different Frequencies

SYSCLKOUT (MHz)	SYSCLKOUT (ns)	PAGE WAIT STATE(1)	RANDOM WAIT STATE(1)	OTP WAIT STATE
90	11.11	3	3	5
80	12.5	2	2	4
70	14.29	2	2	4
60	16.67	2	2	3
55	18.18	1	1	3
50	20	1	1	2
45	22.22	1	1	2
40	25	1	1	2
35	28.57	1	1	2
30	33.33	1	1	1

(1) Page and random wait state must be ≥ 1.

The equations to compute the Flash page wait state and random wait state in Table 7-2 are as follows:

$$\text{Flash Page Wait State} = \left[\left(\frac{t_{a(f\cdot p)}}{t_{c(SCO)}}\right) - 1\right] \text{ round up to the next highest integer, or 1, whichever is larger}$$

$$\text{Flash Random Wait State} = \left[\left(\frac{t_{a(f\cdot r)}}{t_{c(SCO)}}\right) - 1\right] \text{ round up to the next highest integer, or 1, whichever is larger}$$

The equation to compute the OTP wait state in Table 7-2 is as follows:

$$\text{OTP Wait State} = \left[\left(\frac{t_{a(OTP)}}{t_{c(SCO)}}\right) - 1\right] \text{ round up to the next highest integer, or 1, whichever is larger}$$

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8 Detailed Description

8.1 Overview

8.1.1 CPU

The 2806x (C28x) family is a member of the TMS320C2000™ microcontroller (MCU) platform. The C28x-based controllers have the same 32-bit fixed-point architecture as existing C28x MCUs. Each C28x-based controller, including the 2806x device, is a very efficient C/C++ engine, enabling users to develop not only their system control software in a high-level language, but also enabling development of math algorithms using C/C++. The device is as efficient at MCU math tasks as it is at system control tasks that typically are handled by microcontroller devices. This efficiency removes the need for a second processor in many systems. The 32 × 32-bit MAC 64-bit processing capabilities enable the controller to handle higher numerical resolution problems efficiently. Add to this the fast interrupt response with automatic context save of critical registers, resulting in a device that is capable of servicing many asynchronous events with minimal latency. The device has an 8-level-deep protected pipeline with pipelined memory accesses. This pipelining enables it to execute at high speeds without resorting to expensive high-speed memories. Special branch-look-ahead hardware minimizes the latency for conditional discontinuities. Special store conditional operations further improve performance.

8.1.2 Control Law Accelerator (CLA)

The C28x CLA is a single-precision (32-bit) floating-point unit that extends the capabilities of the C28x CPU by adding parallel processing. The CLA is an independent processor with its own bus structure, fetch mechanism, and pipeline. Eight individual CLA tasks, or routines, can be specified. Each task is started by software or a peripheral such as the ADC, ePWM, eCAP, eQEP, or CPU Timer 0. The CLA executes one task at a time to completion. When a task completes, the main CPU is notified by an interrupt to the PIE and the CLA automatically begins the next highest-priority pending task. The CLA can directly access the ADC Result registers, ePWM+HRPWM, eCAP, and eQEP registers. Dedicated message RAMs provide a method to pass additional data between the main CPU and the CLA.

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8.1.3 Viterbi, Complex Math, CRC Unit (VCU)

The C28x VCU enhances the processing power of C2000™ devices by adding additional assembly instructions to target complex math, Viterbi decode, and CRC calculations. The VCU instructions accelerate many applications, including the following:

- Orthogonal frequency-division multiplex (OFDM) used in the PRIME and G3 standards for power line communications
- Short-range radar complex math calculations
- Power calculations
- Memory and data communication packet checks (CRC)

The VCU features include:

- Instructions to support Cyclic Redundancy Checks (CRCs), which is a polynomial code checksum.
  - CRC8
  - CRC16
  - CRC32
- Instructions to support a flexible software implementation of a Viterbi decoder
  - Branch metric calculations for a code rate of 1/2 or 1/3
  - Add-Compare Select or Viterbi Butterfly in five cycles per butterfly
  - Traceback in three cycles per stage
  - Easily supports a constraint length of K = 7 used in PRIME and G3 standards
- Complex math arithmetic unit
  - Single-cycle Add or Subtract
  - 2-cycle multiply
  - 2-cycle multiply and accumulate (MAC)
  - Single-cycle repeat MAC
- Independent register space

8.1.4 Memory Bus (Harvard Bus Architecture)

As with many MCU-type devices, multiple buses are used to move data between the memories and peripherals and the CPU. The memory bus architecture contains a program read bus, data read bus, and data write bus. The program read bus consists of 22 address lines and 32 data lines. The data read and write buses consist of 32 address lines and 32 data lines each. The 32-bit-wide data buses enable single cycle 32-bit operations. The multiple bus architecture, commonly termed Harvard Bus, enables the C28x to fetch an instruction, read a data value and write a data value in a single cycle. All peripherals and memories attached to the memory bus prioritize memory accesses. Generally, the priority of memory bus accesses can be summarized as follows:

Highest:	Data Writes	(Simultaneous data and program writes cannot occur on the memory bus.)
	Program Writes	(Simultaneous data and program writes cannot occur on the memory bus.)
	Data Reads	
	Program Reads	(Simultaneous program reads and fetches cannot occur on the memory bus.)
Lowest:	Fetches	(Simultaneous program reads and fetches cannot occur on the memory bus.)

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8.1.5 Peripheral Bus

To enable migration of peripherals between various Texas Instruments (TI) MCU family of devices, the devices adopt a peripheral bus standard for peripheral interconnect. The peripheral bus bridge multiplexes the various buses that make up the processor Memory Bus into a single bus consisting of 16 address lines and 16 or 32 data lines and associated control signals. Three versions of the peripheral bus are supported. One version supports only 16-bit accesses (called peripheral frame 2). Another version supports both 16- and 32-bit accesses (called peripheral frame 1).

8.1.6 Real-Time JTAG and Analysis

The devices implement the standard IEEE 1149.1 (**IEEE Standard 1149.1-1990 Standard Test Access Port and Boundary Scan Architecture**) JTAG interface for in-circuit based debug. interface for in-circuit based debug. Additionally, the devices support real-time mode of operation allowing modification of the contents of memory, peripheral, and register locations while the processor is running and executing code and servicing interrupts. The user can also single step through non-time-critical code while enabling time-critical interrupts to be serviced without interference. The device implements the real-time mode in hardware within the CPU. This is a feature unique to the 28x family of devices, requiring no software monitor. Additionally, special analysis hardware is provided that allows setting of hardware breakpoint or data/address watch-points and generating various user-selectable break events when a match occurs.

8.1.7 Flash

The F28069, F28069F, F28069M, F28068F, F28068M, F28067, and F28066 devices contain 128K × 16 of embedded flash memory, segregated into eight 16K × 16 sectors. The F28065, F28064, F28063, F28062, and F28062F devices contain 64K × 16 of embedded flash memory, segregated into eight 8K × 16 sectors. All devices also contain a single 1K × 16 of OTP memory at address range 0x3D 7800 to 0x3D 7BF9. The user can individually erase, program, and validate a flash sector while leaving other sectors untouched. However, it is not possible to use one sector of the flash or the OTP to execute flash algorithms that erase or program other sectors. Special memory pipelining is provided to enable the flash module to achieve higher performance. The flash/OTP is mapped to both program and data space; therefore, it can be used to execute code or store data information. Addresses 0x3F 7FF0 to 0x3F 7FF5 are reserved for data variables and should not contain program code.

Note

The Flash and OTP wait states can be configured by the application. This allows applications running at slower frequencies to configure the flash to use fewer wait states.

Flash effective performance can be improved by enabling the flash pipeline mode in the Flash options register. With this mode enabled, effective performance of linear code execution will be much faster than the raw performance indicated by the wait-state configuration alone. The exact performance gain when using the Flash pipeline mode is application-dependent.

For more information on the Flash options, Flash wait state, and OTP wait-state registers, see the Systems Control and Interrupts chapter of the *TMS320x2806x Technical Reference Manual* .

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8.1.8 M0, M1 SARAMs

All devices contain these two blocks of single-access memory, each 1K × 16 in size. The stack pointer points to the beginning of block M1 on reset. The M0 and M1 blocks, like all other memory blocks on C28x devices, are mapped to both program and data space. Hence, the user can use M0 and M1 to execute code or for data variables. The partitioning is performed within the linker. The C28x device presents a unified memory map to the programmer. This makes for easier programming in high-level languages.

8.1.9 L4 SARAM, and L0, L1, L2, L3, L5, L6, L7, and L8 DPSARAMs

The device contains up to 48K × 16 of single-access RAM. To ascertain the exact size for a given device, see the device-specific memory map figures in Section 8.2. This block is mapped to both program and data space. L0 is 2K in size. L1 and L2 are each 1K in size. L3 is 4K in size. L4, L5, L6, L7, and L8 are each 8K in size. L0, L1, and L2 are shared with the CLA, which can use these blocks for its data space. L3 is shared with the CLA, which can use this block for its program space. L5, L6, L7, and L8 are shared with the DMA, which can use these blocks for its data space. DPSARAM refers to the dual-port configuration of these blocks.

8.1.10 Boot ROM

The Boot ROM is factory-programmed with boot-loading software. Boot-mode signals are provided to tell the bootloader software what boot mode to use on power up. The user can select to boot normally or to download new software from an external connection or to select boot software that is programmed in the internal Flash/ROM. The Boot ROM also contains standard tables, such as SIN/COS waveforms, for use in math-related algorithms.

Table 8-1. Boot Mode Selection

MODE	GPIO37/TDO	GPIO34/COMP2OUT/ COMP3OUT	$\overline{\text{TRST}}$	MODE
3	1	1	0	GetMode
2	1	0	0	Wait (see Section 8.1.11 for description)
1	0	1	0	SCI
0	0	0	0	Parallel IO
EMU	x	x	1	Debug Boot

8.1.10.1 Debug Boot

When the debug probe is connected, the GPIO37/TDO pin cannot be used for boot mode selection. In this case, the boot ROM detects that a debug probe is connected and uses the contents of two reserved SARAM locations in the PIE vector table to determine the boot mode. If the content of either location is invalid, then the *Wait* boot option is used. All boot mode options can be accessed in debug boot.

8.1.10.2 GetMode

The default behavior of the *GetMode* option is to boot to flash. This behavior can be changed to another boot option by programming two locations in the OTP. If the content of either OTP location is invalid, then boot to flash is used. One of the following loaders can be specified: SCI, SPI, I2C, CAN, or OTP.

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8.1.10.3 Peripheral Pins Used by the Bootloader

Table 8-2 shows which GPIO pins are used by each peripheral bootloader. Refer to the GPIO mux table to see if these conflict with any of the peripherals you would like to use in your application.

Table 8-2. Peripheral Bootload Pins

BOOTLOADER	PERIPHERAL LOADER PINS
SCI	SCIRXDA (GPIO28) SCITXDA (GPIO29)
Parallel Boot	Data (GPIO31,30,5:0) 28x Control (AIO6) Host Control (AIO12)
SPI	SPISIMOA (GPIO16) SPISOMIA (GPIO17) SPICLKA (GPIO18) $\overline{\text{SPISTEA}}$ (GPIO19)
I2C	SDAA (GPIO28) SCLA (GPIO29)
CAN	CANRXA (GPIO30) CANTXA (GPIO31)

8.1.11 Security

The devices support high levels of security to protect the user firmware from being reverse-engineered. The security features a 128-bit password (hardcoded for 16 wait states), which the user programs into the flash. One code security module (CSM) is used to protect the flash/OTP and the L0/L1 SARAM blocks. The security feature prevents unauthorized users from examining the memory contents through the JTAG port, or trying to boot-load some undesirable software that would export the secure memory contents. To enable access to the secure blocks, the user must write the correct 128-bit KEY value that matches the value stored in the password locations within the Flash.

In addition to the CSM, the debug code security logic (ECSL) has been implemented to prevent unauthorized users from stepping through secure code. Any code or data access to CSM secure memory while the debug probe is connected will trip the ECSL and break the debug probe connection. To allow debug of secure code, while maintaining the CSM protection against secure memory reads, the user must write the correct value into the lower 64 bits of the KEY register (KEY0 – KEY3), which matches the value stored in the lower 64 bits of the password locations within the flash. Dummy reads of all 128 bits of the password in the flash must still be performed. If the lower 64 bits of the password locations (PWL0 – PWL3) are all ones (unprogrammed), then the KEY value does not need to match. During debug of secure code, operations like single-stepping is possible. However, the actual contents of the secure memory cannot be seen in the CCS window.

When power is applied to a secure device that is connected to a JTAG debug probe, the CPU will start executing and may execute an instruction that performs an access to a protected area. If this happens, the ECSL will trip and cause the JTAG circuitry to be deactivated. Under this condition, a host (such as a computer running CCS or flash programming software) would not be able to establish connection with the device.

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The solution is to use the *Wait* boot option. In this mode, the device loops around a software breakpoint to allow a debug probe to be connected without tripping security. These devices do not support a hardware wait-in-reset mode.

Note

- When the code-security passwords are programmed, all addresses from 0x3F 7F80 to 0x3F 7FF5 cannot be used as program code or data. These locations must be programmed to 0x0000.
- If reprogramming of a secure device via JTAG may be needed in future, it is important to design the board in such a way that the device could be put in Wait boot mode upon power-up (when reprogramming is warranted). Otherwise, ECSL may deactivate the JTAG circuitry and prevent connection to the device, as mentioned earlier. If reconfiguring the device for Wait boot mode in the field is not practical, some mechanism must be implemented in the firmware to detect when a firmware update is warranted. Code could then branch to the desired bootloader in the bootROM. It could also branch to the Wait bootmode, at which point the JTAG debug probe could be connected, device unsecured and programming accomplished through JTAG itself.
- If the code security feature is not used, addresses 0x3F 7F80 to 0x3F 7FEF may be used for code or data. Addresses 0x3F 7FF0 to 0x3F 7FF5 are reserved for data and should not contain program code.
- The 128-bit password (at 0x3F 7FF8 to 0x3F 7FFF) ***must not*** be programmed to zeros. Doing so would permanently lock the device.

Code Security Module Disclaimer

THE CODE SECURITY MODULE (CSM) INCLUDED ON THIS DEVICE WAS DESIGNED TO PASSWORD PROTECT THE DATA STORED IN THE ASSOCIATED MEMORY (EITHER ROM OR FLASH) AND IS WARRANTED BY TEXAS INSTRUMENTS (TI), IN ACCORDANCE WITH ITS STANDARD TERMS AND CONDITIONS, TO CONFORM TO TI'S PUBLISHED SPECIFICATIONS FOR THE WARRANTY PERIOD APPLICABLE FOR THIS DEVICE.

TI DOES NOT, HOWEVER, WARRANT OR REPRESENT THAT THE CSM CANNOT BE COMPROMISED OR BREACHED OR THAT THE DATA STORED IN THE ASSOCIATED MEMORY CANNOT BE ACCESSED THROUGH OTHER MEANS. MOREOVER, EXCEPT AS SET FORTH ABOVE, TI MAKES NO WARRANTIES OR REPRESENTATIONS CONCERNING THE CSM OR OPERATION OF THIS DEVICE, INCLUDING ANY IMPLIED WARRANTIES OF MERCHANTABILITY OR FITNESS FOR A PARTICULAR PURPOSE.

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8.1.12 Peripheral Interrupt Expansion (PIE) Block

The PIE block serves to multiplex numerous interrupt sources into a smaller set of interrupt inputs. The PIE block can support up to 96 peripheral interrupts. On the F2806x, 72 of the possible 96 interrupts are used by peripherals. The 96 interrupts are grouped into blocks of 8 and each group is fed into 1 of 12 CPU interrupt lines (INT1 to INT12). Each of the 96 interrupts is supported by its own vector stored in a dedicated RAM block that can be overwritten by the user. The vector is automatically fetched by the CPU on servicing the interrupt. Eight CPU clock cycles are needed to fetch the vector and save critical CPU registers. Hence the CPU can quickly respond to interrupt events. Prioritization of interrupts is controlled in hardware and software. Each individual interrupt can be enabled or disabled within the PIE block.

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8.1.13 External Interrupts (XINT1 to XINT3)

The devices support three masked external interrupts (XINT1–XINT3). Each of the interrupts can be selected for negative, positive, or both negative and positive edge triggering and can also be enabled or disabled. These interrupts also contain a 16-bit free-running up counter, which is reset to zero when a valid interrupt edge is detected. This counter can be used to accurately time-stamp the interrupt. There are no dedicated pins for the external interrupts. XINT1, XINT2, and XINT3 interrupts can accept inputs from GPIO0–GPIO31 pins.

8.1.14 Internal Zero Pin Oscillators, Oscillator, and PLL

The device can be clocked by either of the two internal zero-pin oscillators, an external oscillator, or by a crystal attached to the on-chip oscillator circuit. A PLL is provided supporting up to 16 input-clock-scaling ratios. The PLL ratios can be changed on-the-fly in software, enabling the user to scale back on operating frequency if lower power operation is desired. Refer to Section 7, Specifications, for timing details. The PLL block can be set in bypass mode. A second PLL (PLL2) feeds the HRCAP module.

8.1.15 Watchdog

Each device contains two watchdogs: CPU-watchdog that monitors the core and NMI-watchdog that is a missing clock-detect circuit. The user software must regularly reset the CPU-watchdog counter within a certain time frame; otherwise, the CPU-watchdog generates a reset to the processor. The CPU-watchdog can be disabled if necessary. The NMI-watchdog engages only in case of a clock failure and can either generate an interrupt or a device reset.

8.1.16 Peripheral Clocking

The clocks to each individual peripheral can be enabled or disabled to reduce power consumption when a peripheral is not in use. Additionally, the system clock to the serial ports (except I2C) can be scaled relative to the CPU clock.

8.1.17 Low-power Modes

The devices are full static CMOS devices. Three low-power modes are provided:

- IDLE: Places CPU in low-power mode. Peripheral clocks may be turned off selectively and only those peripherals that must function during IDLE are left operating. An enabled interrupt from an active peripheral or the watchdog timer will wake the processor from IDLE mode.
- STANDBY: Turns off clock to CPU and peripherals. This mode leaves the oscillator and PLL functional. An external interrupt event will wake the processor and the peripherals. Execution begins on the next valid cycle after detection of the interrupt event
- HALT: This mode basically shuts down the device and places it in the lowest possible power-consumption mode. If the internal zero-pin oscillators are used as the clock source, the HALT mode turns them off, by default. To keep these oscillators from shutting down, the INTOSCnHALTI bits in CLKCTL register may be used. The zero-pin oscillators may thus be used to clock the CPU-watchdog in this mode. If the on-chip crystal oscillator is used as the clock source, it is shut down in this mode. A reset or an external signal (through a GPIO pin) or the CPU-watchdog can wake the device from this mode.

The CPU clock (OSCCLK) and the watchdog clock source should be from the same clock source before attempting to put the device into HALT or STANDBY.

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8.1.18 Peripheral Frames 0, 1, 2, 3 (PFn)

The device segregates peripherals into four sections. The mapping of peripherals is as follows:

PF0:	PIE:	PIE Interrupt Enable and Control Registers Plus PIE Vector Table
	Flash:	Flash Waitstate Registers
	Timers:	CPU-Timers 0, 1, 2 Registers
	CSM:	Code Security Module KEY Registers
	ADC:	ADC Result Registers
	CLA:	Control Law Accelrator Registers and Message RAMs
PF1:	GPIO:	GPIO MUX Configuration and Control Registers
	eCAN:	Enhanced Control Area Network Configuration and Control Registers
PF2:	SYS:	System Control Registers
	SCI:	Serial Communications Interface (SCI) Control and RX/TX Registers
	SPI:	Serial Port Interface (SPI) Control and RX/TX Registers
	ADC:	ADC Status, Control, and Configuration Registers
	I2C:	Inter-Integrated Circuit Module and Registers
	XINT:	External Interrupt Registers
PF3:	McBSP:	Multichannel Buffered Serial Port Registers
	ePWM:	Enhanced Pulse Width Modulator Module and Registers
	eCAP:	Enhanced Capture Module and Registers
	eQEP:	Enhanced Quadrature Encoder Pulse Module and Registers
	Comparators:	Comparator Modules
	USB:	Universal Serial Bus Module and Registers

8.1.19 General-Purpose Input/Output (GPIO) Multiplexer

Most of the peripheral signals are multiplexed with general-purpose input/output (GPIO) signals. This enables the user to use a pin as GPIO if the peripheral signal or function is not used. On reset, GPIO pins are configured as inputs. The user can individually program each pin for GPIO mode or peripheral signal mode. For specific inputs, the user can also select the number of input qualification cycles. This is to filter unwanted noise glitches. The GPIO signals can also be used to bring the device out of specific low-power modes.

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8.1.20 32-Bit CPU-Timers (0, 1, 2)

CPU-Timers 0, 1, and 2 are identical 32-bit timers with presettable periods and with 16-bit clock prescaling. The timers have a 32-bit count-down register, which generates an interrupt when the counter reaches zero. The counter is decremented at the CPU clock speed divided by the prescale value setting. When the counter reaches zero, it is automatically reloaded with a 32-bit period value.

CPU-Timer 0 is for general use and is connected to the PIE block. CPU-Timer 1 is also for general use and can be connected to INT13 of the CPU. CPU-Timer 2 is reserved for SYS/BIOS. CPU-Timer 2 is connected to INT14 of the CPU. If SYS/BIOS is not being used, CPU-Timer 2 is available for general use.

CPU-Timer 2 can be clocked by any one of the following:

- SYSCLKOUT (default)
- Internal zero-pin oscillator 1 (INTOSC1)
- Internal zero-pin oscillator 2 (INTSOC2)
- External clock source

8.1.21 Control Peripherals

The devices support the following peripherals that are used for embedded control and communication:

ePWM:	The enhanced PWM peripheral supports independent/complementary PWM generation, adjustable dead-band generation for leading/trailing edges, latched/cycle-by-cycle trip mechanism. Some of the PWM pins support the HRPWM high-resolution duty and period features. The type 1 module found on 2806x devices also supports increased dead-band resolution, enhanced SOC and interrupt generation, and advanced triggering including trip functions based on comparator outputs.
eCAP:	The enhanced capture peripheral uses a 32-bit time base and registers up to four programmable events in continuous/one-shot capture modes. This peripheral can also be configured to generate an auxiliary PWM signal.
eQEP:	The enhanced QEP peripheral uses a 32-bit position counter, supports low-speed measurement using capture unit and high-speed measurement using a 32-bit unit timer. This peripheral has a watchdog timer to detect motor stall and input error detection logic to identify simultaneous edge transition in QEP signals.
ADC:	The ADC block is a 12-bit converter. The ADC has up to 16 single-ended channels pinned out, depending on the device. The ADC also contains two sample-and-hold units for simultaneous sampling.
Comparator:	Each comparator block consists of one analog comparator along with an internal 10-bit reference for supplying one input of the comparator.
HRCAP:	The high-resolution capture peripheral operates in normal capture mode through a 16-bit counter clocked off of the HCCAPCLK or in high-resolution capture mode by using built-in calibration logic in conjunction with a TI-supplied calibration library.

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8.1.22 Serial Port Peripherals

The devices support the following serial communication peripherals:

SPI: The SPI is a high-speed, synchronous serial I/O port that allows a serial bit stream of programmed length (1 to 16 bits) to be shifted into and out of the device at a programmable bit-transfer rate. Normally, the SPI is used for communications between the MCU and external peripherals or another processor. Typical applications include external I/O or peripheral expansion through devices such as shift registers, display drivers, and ADCs. Multidevice communications are supported by the master/slave operation of the SPI. The SPI contains a 4-level receive and transmit FIFO for reducing interrupt servicing overhead.

SCI: The serial communications interface is a 2-wire asynchronous serial port, commonly known as UART. The SCI contains a 4-level receive and transmit FIFO for reducing interrupt servicing overhead.

I2C: The inter-integrated circuit (I2C) module provides an interface between an MCU and other devices compliant with Philips Semiconductors Inter-IC bus (I2C-bus®) specification version 2.1 and connected by way of an I^2C-bus. External components attached to this 2-wire serial bus can transmit/receive up to 8-bit data to or from the MCU through the I2C module. The I2C contains a 4-level receive-and-transmit FIFO for reducing interrupt servicing overhead.

eCAN: This is the enhanced version of the CAN peripheral. The eCAN supports 32 mailboxes, time-stamping of messages, and is compliant with ISO 11898-1 (CAN 2.0B).

McBSP: The multichannel buffered serial port (McBSP) connects to E1/T1 lines, phone-quality codecs for modem applications or high-quality stereo audio DAC devices. The McBSP receive and transmit registers are supported by the DMA to significantly reduce the overhead for servicing this peripheral. Each McBSP module can be configured as an SPI as required.

USB: The USB peripheral, which conforms to the USB 2.0 specification, may be used as either a full-speed (12-Mbps) device controller, or a full-speed (12-Mbps) or low-speed (1.5-Mbps) host controller. The controller supports a total of six user-configurable endpoints—all of which can be accessed through DMA, in addition to a dedicated control endpoint for endpoint zero. All packets transmitted or received are buffered in 4KB of dedicated endpoint memory. The USB peripheral supports all three transfer types: Control, Interrupt, and Bulk. Because of the complexity of the USB peripheral and the associated protocol overhead, a full software library with application examples is provided within C2000Ware.

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8.2 Memory Maps

In Figure 8-1 through Figure 8-8, the following apply:

- Memory blocks are not to scale.
- Peripheral Frame 0, Peripheral Frame 1, Peripheral Frame 2, and Peripheral Frame 3 memory maps are restricted to data memory only. A user program cannot access these memory maps in program space.
- *Protected* means the order of Write-followed-by-Read operations is preserved rather than the pipeline order.
- Certain memory ranges are EALLOW protected against spurious writes after configuration.
- Locations 0x3D 7C80–0x3D 7CC0 contain the internal oscillator and ADC calibration routines. These locations are not programmable by the user.
- All devices with USB have the USB control registers mapped from 0x4000 to 0x4FFF and 2K ×16 RAM from 0x40000 to 0x40800. When the clock to the USB module is enabled, this RAM is connected to the USB controller and acts as the FIFO RAM. When the clock to the USB module is disabled, this RAM is remapped to the CPU-accessible address space and can be used as general-purpose RAM.

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	Data Space	Prog Space
0x00 0000	*M0 Vector RAM (Enabled if VMAP = 0)*	
0x00 0040	M0 SARAM (1K × 16, 0-Wait)	
0x00 0400	M1 SARAM (1K × 16, 0-Wait)	
0x00 0800	Peripheral Frame 0	Reserved
0x00 0D00	PIE Vector - RAM (256 × 16) (Enabled if VMAP = 1, ENPIE = 1)	
0x00 0E00	Peripheral Frame 0	
0x00 1400	CLA Registers	
0x00 1480	CLA-to-CPU Message RAM	
0x00 1500	CPU-to-CLA Message RAM	
0x00 1580	Reserved	
0x00 2000	Reserved	
0x00 4000	USB Control Registers(A)	Reserved
0x00 5000	Peripheral Frame 3 (4K × 16, Protected) DMA-Accessible	
0x00 6000	Peripheral Frame 1 (4K × 16, Protected)	
0x00 7000	Peripheral Frame 2 (4K × 16, Protected)	
0x00 8000	L0 DPSARAM (2K × 16) (0-Wait, Secure Zone + ECSL, CLA Data RAM2)	
0x00 8800	L1 DPSARAM (1K × 16) (0-Wait, Secure Zone + ECSL, CLA Data RAM 0)	
0x00 8C00	L2 DPSARAM (1K × 16) (0-Wait, Secure Zone + ECSL, CLA Data RAM 1)	
0x00 9000	L3 DPSARAM (4K × 16) (0-Wait, Secure Zone + ECSL, CLA Program RAM)	
0x00 A000	L4 SARAM (8K × 16) (0-Wait, Secure Zone + ECSL)	
0x00 C000	L5 DPSARAM (8K × 16) (0-Wait, DMA RAM 0)	
0x00 E000	L6 DPSARAM (8K × 16) (0-Wait, DMA RAM 1)	
0x01 0000	L7 DPSARAM (8K × 16) (0-Wait, DMA RAM 2)	
0x01 2000	L8 DPSARAM (8K × 16) (0-Wait, DMA RAM 3)	
0x01 4000	Reserved	
0x3D 7800	User OTP (1K × 16, Secure Zone + ECSL)	
0x3D 7BFA	Reserved	
0x3D 7C80	Calibration Data	
0x3D 7CC0	Get_mode function	
0x3D 7CD0	Reserved	
0x3D 7E80	PARTID	
0x3D 7E82	Calibration Data	
0x3D 7EB0	Reserved	
0x3D 8000	FLASH (128K × 16, 8 Sectors, Secure Zone + ECSL)	
0x3F 7FF8	128-Bit Password	
0x3F 8000	FAST, SpinTAC, and IQmath Libraries(B)(C) (16K × 16, 0-Wait State)	
0x3F F3B0	Boot ROM (16K × 16, 0-Wait State)	
0x3F FFC0	*CPU Vector Table (32 Vectors, Enabled if VMAP = 1)*	

A. On non-USB devices, 0x00 4000–0x00 4FFF is Reserved.
B. FAST™ and SpinTAC™ libraries exist only on F2806xM and F2806xF devices.
C. The ROM contents from 0x3F 8000–0x3F F3AF differ between F2806x parts and F2806xM/F2806xF parts. See the respective memory map figures in the Boot ROM chapter of the *TMS320x2806x Technical Reference Manual* .

Figure 8-1. 28069, 28069F, 28069M Memory Map

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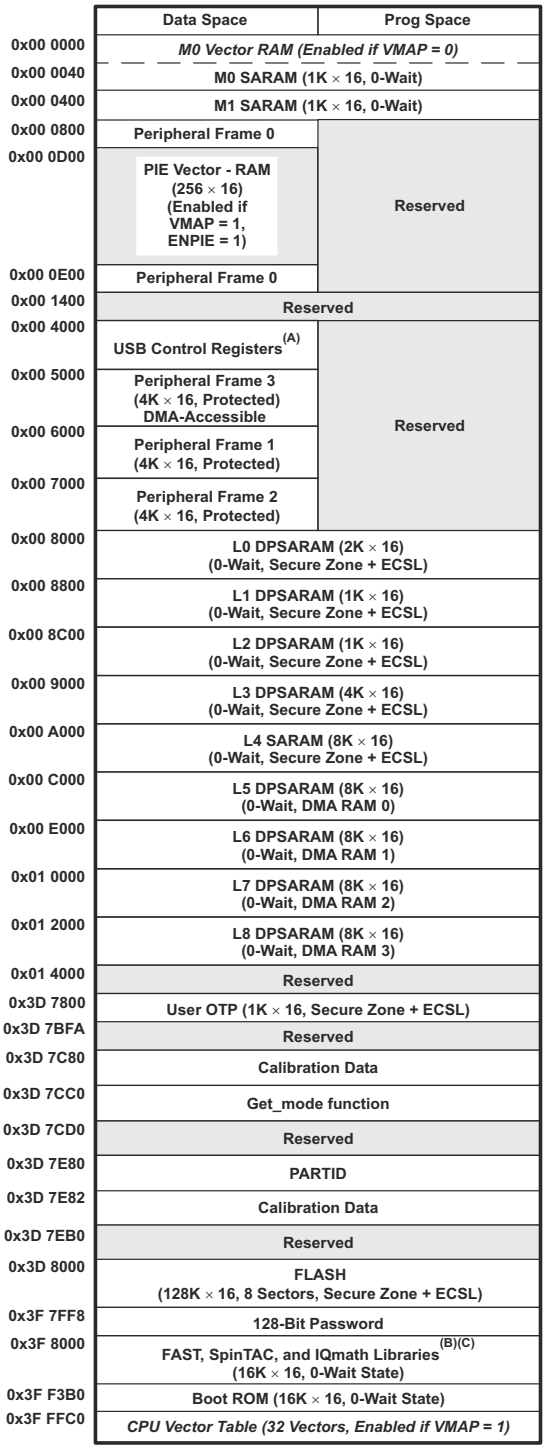

A. On non-USB devices, 0x00 4000–0x00 4FFF is Reserved.

B. FAST™ and SpinTAC™ libraries exist only on F2806xM and F2806xF devices.

C. The ROM contents from 0x3F 8000–0x3F F3AF differ between F2806x parts and F2806xM/F2806xF parts. See the respective memory map figures in the Boot ROM chapter of the *TMS320x2806x Technical Reference Manual* .

Figure 8-2. 28068F, 28068M Memory Map

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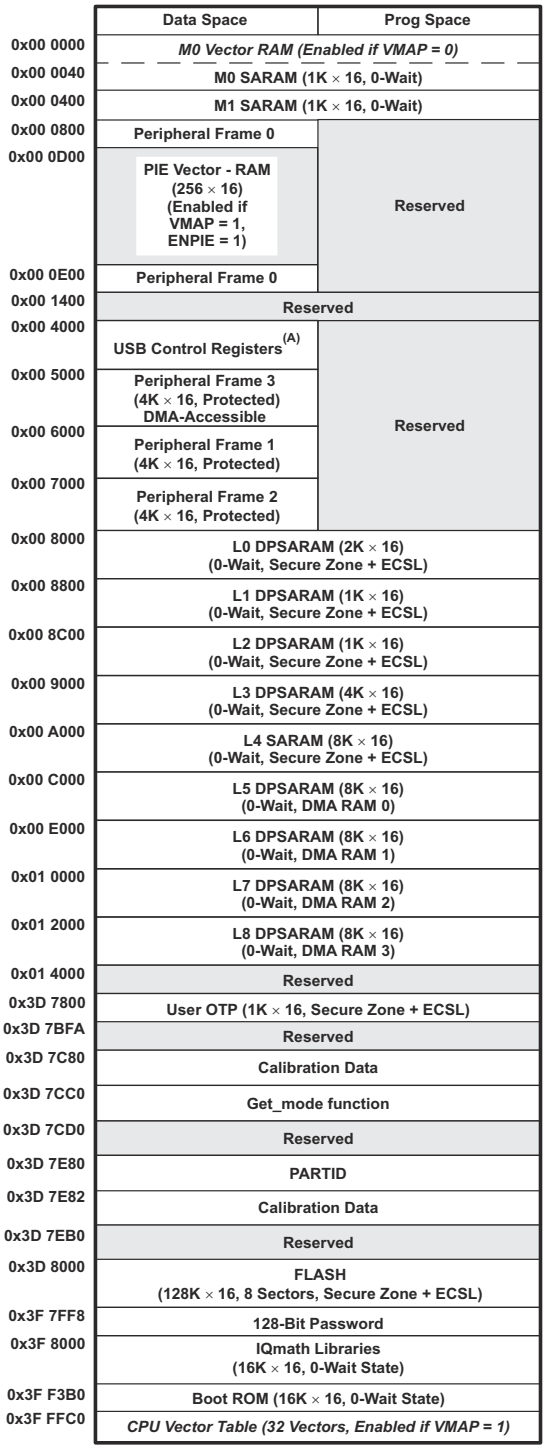

A. On non-USB devices, 0x00 4000–0x00 4FFF is Reserved.

Figure 8-3. 28067 Memory Map

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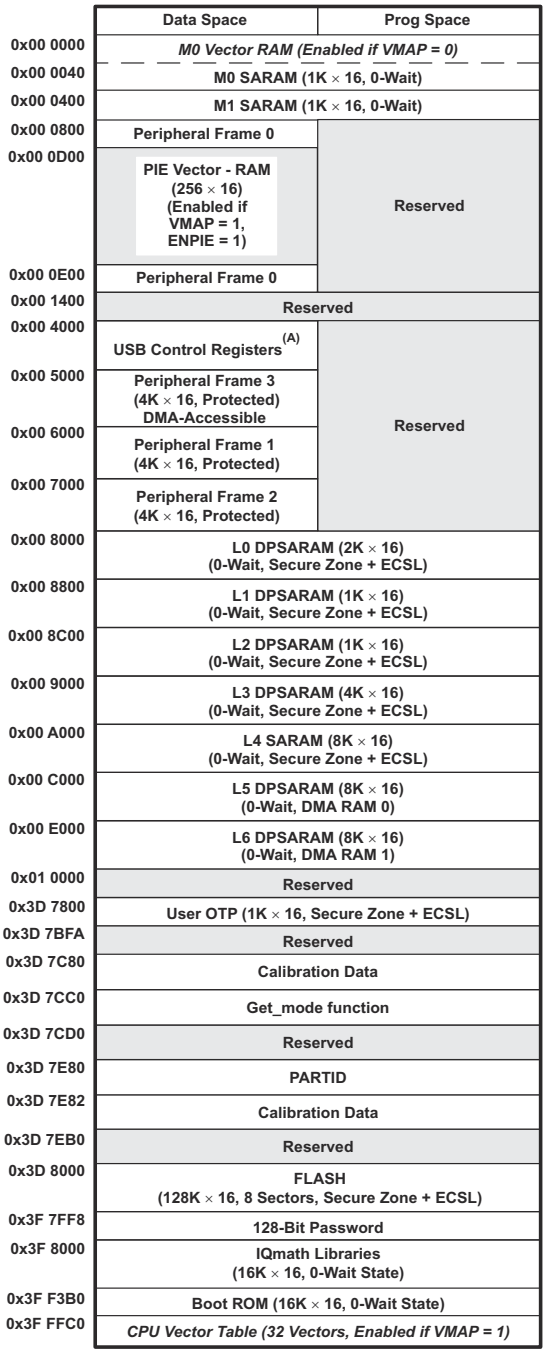

A. On non-USB devices, 0x00 4000–0x00 4FFF is Reserved.

Figure 8-4. 28066 Memory Map

	Data Space	Prog Space
0x00 0000	*M0 Vector RAM (Enabled if VMAP = 0)*	
0x00 0040	M0 SARAM (1K × 16, 0-Wait)	
0x00 0400	M1 SARAM (1K × 16, 0-Wait)	
0x00 0800	Peripheral Frame 0	Reserved
0x00 0D00	PIE Vector - RAM (256 × 16) (Enabled if VMAP = 1, ENPIE = 1)	
0x00 0E00	Peripheral Frame 0	
0x00 1400	CLA Registers	
0x00 1480	CLA-to-CPU Message RAM	
0x00 1500	CPU-to-CLA Message RAM	
0x00 1580	Reserved	
0x00 2000	Reserved	
0x00 4000	USB Control Registers (A)	Reserved
0x00 5000	Peripheral Frame 3 (4K × 16, Protected) DMA-Accessible	
0x00 6000	Peripheral Frame 1 (4K × 16, Protected)	
0x00 7000	Peripheral Frame 2 (4K × 16, Protected)	
0x00 8000	L0 DPSARAM (2K × 16) (0-Wait, Secure Zone + ECSL, CLA Data RAM2)	
0x00 8800	L1 DPSARAM (1K × 16) (0-Wait, Secure Zone + ECSL, CLA Data RAM 0)	
0x00 8C00	L2 DPSARAM (1K × 16) (0-Wait, Secure Zone + ECSL, CLA Data RAM 1)	
0x00 9000	L3 DPSARAM (4K × 16) (0-Wait, Secure Zone + ECSL, CLA Program RAM)	
0x00 A000	L4 SARAM (8K × 16) (0-Wait, Secure Zone + ECSL)	
0x00 C000	L5 DPSARAM (8K × 16) (0-Wait, DMA RAM 0)	
0x00 E000	L6 DPSARAM (8K × 16) (0-Wait, DMA RAM 1)	
0x01 0000	L7 DPSARAM (8K × 16) (0-Wait, DMA RAM 2)	
0x01 2000	L8 DPSARAM (8K × 16) (0-Wait, DMA RAM 3)	
0x01 4000	Reserved	
0x3D 7800	User OTP (1K × 16, Secure Zone + ECSL)	
0x3D 7BFA	Reserved	
0x3D 7C80	Calibration Data	
0x3D 7CC0	Get_mode function	
0x3D 7CD0	Reserved	
0x3D 7E80	PARTID	
0x3D 7E82	Calibration Data	
0x3D 7EB0	Reserved	
0x3E 8000	FLASH (64K × 16, 8 Sectors, Secure Zone + ECSL)	
0x3F 7FF8	128-Bit Password	
0x3F 8000	IQmath Libraries (16K × 16, 0-Wait State)	
0x3F F3B0	Boot ROM (16K × 16, 0-Wait State)	
0x3F FFC0	*CPU Vector Table (32 Vectors, Enabled if VMAP = 1)*	

A. On non-USB devices, 0x00 4000–0x00 4FFF is Reserved.

Figure 8-5. 28065 Memory Map

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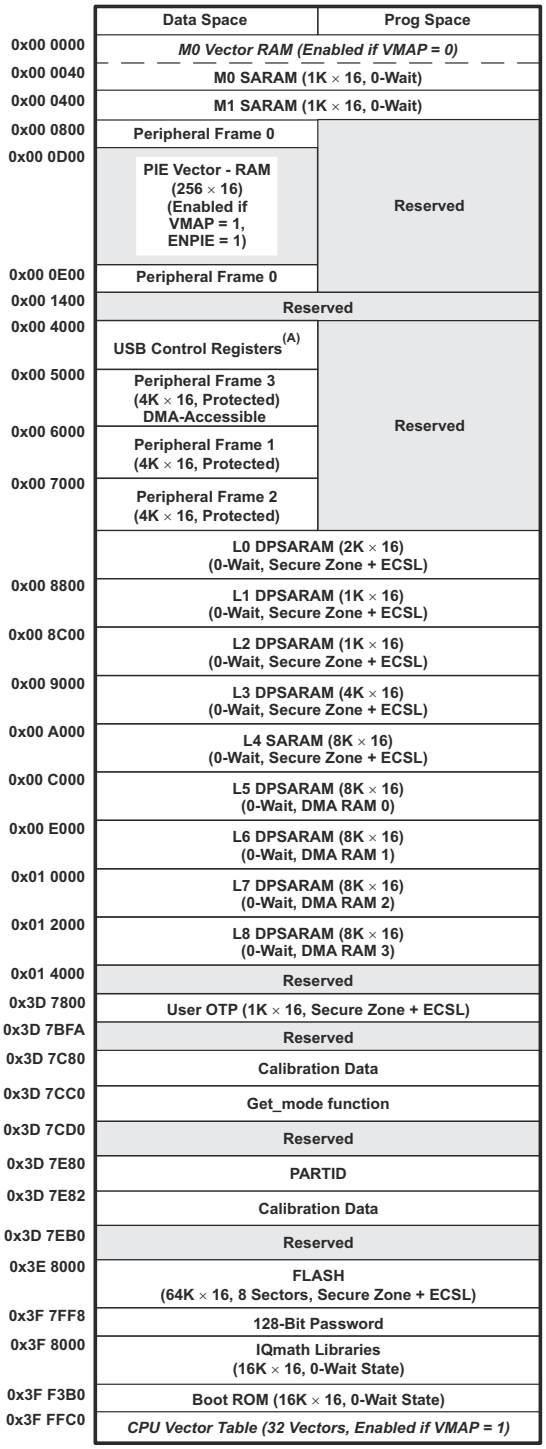
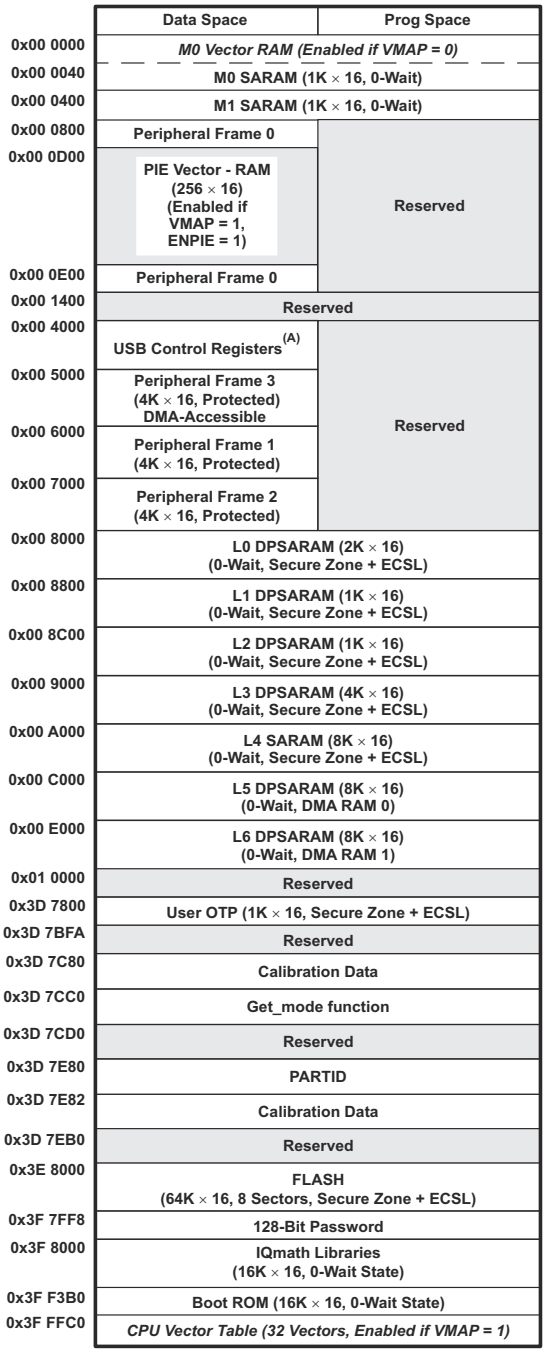


A. On non-USB devices, 0x00 4000–0x00 4FFF is Reserved.

Figure 8-6. 28064 Memory Map



A. On non-USB devices, 0x00 4000–0x00 4FFF is Reserved.

Figure 8-7. 28063 Memory Map

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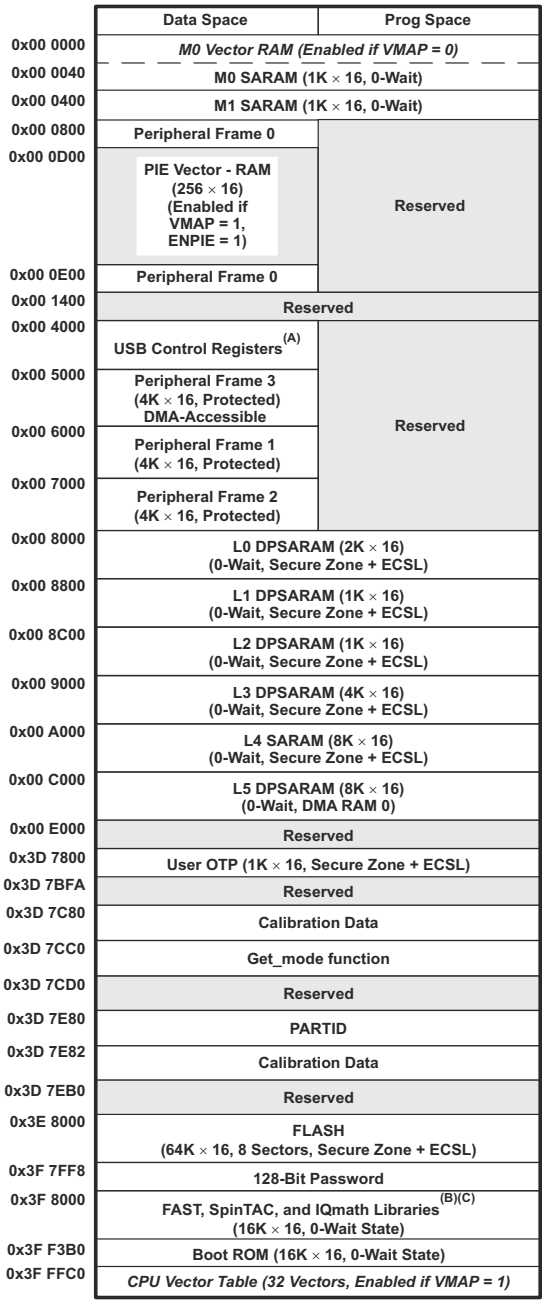

A. On non-USB devices, 0x00 4000–0x00 4FFF is Reserved.

B. FAST™ and SpinTAC™ libraries exist only on F2806xM and F2806xF devices.

C. The ROM contents from 0x3F 8000–0x3F F3AF differ between F2806x parts and F2806xM/F2806xF parts. See the respective memory map figures in the Boot ROM chapter of the *TMS320x2806x Technical Reference Manual* .

Figure 8-8. 28062, 28062F Memory Map

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Table 8-3. Addresses of Flash Sectors in 28069, 28069F, 28069M, 28068F, 28068M, F28067, F28066

ADDRESS RANGE	PROGRAM AND DATA SPACE
0x3D 8000 to 0x3D BFFF	Sector H (16K × 16)
0x3D C000 to 0x3D FFFF	Sector G (16K × 16)
0x3E 0000 to 0x3E 3FFF	Sector F (16K × 16)
0x3E 4000 to 0x3E 7FFF	Sector E (16K × 16)
0x3E 8000 to 0x3E BFFF	Sector D (16K × 16)
0x3E C000 to 0x3E FFFF	Sector C (16K × 16)
0x3F 0000 to 0x3F 3FFF	Sector B (16K × 16)
0x3F 4000 to 0x3F 7FF5	Sector A (16K × 16)
0x3F 7FF6 to 0x3F 7FF7	Boot-to-Flash Entry Point (program branch instruction here)
0x3F 7FF8 to 0x3F 7FFF	Security Password (128-Bit) (Do not program to all zeros)

Table 8-4. Addresses of Flash Sectors in F28065, F28064, F28063, 28062, 28062F

ADDRESS RANGE	PROGRAM AND DATA SPACE
0x3E 8000 to 0x3E 9FFF	Sector H (8K × 16)
0x3E A000 to 0x3E BFFF	Sector G (8K × 16)
0x3E C000 to 0x3E DFFF	Sector F (8K × 16)
0x3E E000 to 0x3E FFFF	Sector E (8K × 16)
0x3F 0000 to 0x3F 1FFF	Sector D (8K × 16)
0x3F 2000 to 0x3F 3FFF	Sector C (8K × 16)
0x3F 4000 to 0x3F 5FFF	Sector B (8K × 16)
0x3F 6000 to 0x3F 7FF5	Sector A (8K × 16)
0x3F 7FF6 to 0x3F 7FF7	Boot-to-Flash Entry Point (program branch instruction here)
0x3F 7FF8 to 0x3F 7FFF	Security Password (128-Bit) (Do not program to all zeros)

Note

Addresses 0x3F 7FF0 to 0x3F 7FF5 are reserved for data and should not contain program code.

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Peripheral Frame 1 and Peripheral Frame 2 are grouped together to enable these blocks to be write/read peripheral block protected. The protected mode makes sure that all accesses to these blocks happen as written. Because of the pipeline, a write immediately followed by a read to different memory locations, will appear in reverse order on the memory bus of the CPU. This can cause problems in certain peripheral applications where the user expected the write to occur first (as written). The CPU supports a block protection mode where a region of memory can be protected so that operations occur as written (the penalty is extra cycles are added to align the operations). This mode is programmable and by default, it protects the selected zones.

The wait states for the various spaces in the memory map area are listed in Table 8-5.

Table 8-5. Wait States

AREA	WAIT STATES (CPU)	COMMENTS
M0 and M1 SARAMs	0-wait	Fixed
Peripheral Frame 0	0-wait	
Peripheral Frame 1	0-wait (writes) 2-wait (reads)	Cycles can be extended by peripheral-generated ready. Back-to-back write operations to Peripheral Frame 1 registers will incur a 1-cycle stall (1-cycle delay).
Peripheral Frame 2	0-wait (writes) 2-wait (reads)	Fixed. Cycles cannot be extended by the peripheral.
Peripheral Frame 3	0-wait (writes) 2-wait (reads)	Assumes no conflict between CPU and CLA/DMA cycles. The wait states can be extended by peripheral-generated ready.
L0–L8 SARAM	0-wait data and program	Assumes no CPU conflicts
OTP	Programmable 1-wait minimum	Programmed through the Flash registers. 1-wait is minimum number of wait states allowed.
FLASH	Programmable 0-wait Paged min 1-wait Random min Random ≥ Paged	Programmed through the Flash registers.
FLASH Password	16-wait fixed	Wait states of password locations are fixed.
Boot-ROM	0-wait	

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8.3 Register Maps

The devices contain four peripheral register spaces. The spaces are categorized as follows:

Peripheral Frame 0: These are peripherals that are mapped directly to the CPU memory bus, which supports 16-bit and 32-bit accesses. See Table 8-6.

Peripheral Frame 1: These are peripherals that are mapped to the 32-bit peripheral bus. See Table 8-7.

Peripheral Frame 2: These are peripherals that are mapped to the 16-bit peripheral bus. See Table 8-8.

Peripheral Frame 3: These are peripherals that are mapped to the 32-bit peripheral bus. See Table 8-9.

Table 8-6. Peripheral Frame 0 Registers

NAME(1)	ADDRESS RANGE	SIZE (×16)	EALLOW PROTECTED(2)
Device Debug registers	0x00 0880 to 0x00 0984	261	Yes
System Power Control registers	0x00 0985 to 0x00 0987	3	Yes
FLASH registers(3)	0x00 0A80 to 0x00 0ADF	96	Yes
Code Security Module registers	0x00 0AE0 to 0x00 0AEF	16	Yes
ADC registers (0 wait read only)	0x00 0B00 to 0x00 0B0F	16	No
CPU-TIMER0, CPU-TIMER1, CPU-TIMER2 registers	0x00 0C00 to 0x00 0C3F	64	No
PIE registers	0x00 0CE0 to 0x00 0CFF	32	No
PIE Vector Table	0x00 0D00 to 0x00 0DFF	256	Yes
DMA registers	0x00 1000 to 0x00 11FF	512	Yes
CLA registers	0x00 1400 to 0x00 147F	128	Yes
CLA to CPU Message RAM (CPU writes ignored)	0x00 1480 to 0x00 14FF	128	NA
CPU to CLA Message RAM (CLA writes ignored)	0x00 1500 to 0x00 157F	128	NA

(1) Registers in Frame 0 support 16-bit and 32-bit accesses.
(2) If registers are EALLOW protected, then writes cannot be performed until the EALLOW instruction is executed. The EDIS instruction disables writes to prevent stray code or pointers from corrupting register contents.
(3) The Flash Registers are also protected by the Code Security Module (CSM).

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Table 8-7. Peripheral Frame 1 Registers

NAME	ADDRESS RANGE	SIZE (×16)	EALLOW PROTECTED
eCAN-A registers	0x00 6000 to 0x00 61FF	512	(1)
HRCAP1 registers	0x00 6AC0 to 0x00 6ADF	32	(1)
HRCAP2 registers	0x00 6AE0 to 0x00 6AFF	32	(1)
HRCAP3 registers	0x00 6C80 to 0x00 6C9F	32	(1)
HRCAP4 registers	0x00 6CA0 to 0x00 6CBF	32	(1)
GPIO registers	0x00 6F80 to 0x00 6FFF	128	(1)

(1) Some registers are EALLOW protected. See the module reference guide for more information.

Table 8-8. Peripheral Frame 2 Registers

NAME	ADDRESS RANGE	SIZE (×16)	EALLOW PROTECTED
System Control registers	0x00 7010 to 0x00 702F	32	Yes
SPI-A registers	0x00 7040 to 0x00 704F	16	No
SCI-A registers	0x00 7050 to 0x00 705F	16	No
NMI Watchdog Interrupt registers	0x00 7060 to 0x00 706F	16	Yes
External Interrupt registers	0x00 7070 to 0x00 707F	16	Yes
ADC registers	0x00 7100 to 0x00 717F	128	(1)
SPI-B registers	0x00 7740 to 0x00 774F	16	No
SCI-B registers	0x00 7750 to 0x00 775F	16	No
I2C-A registers	0x00 7900 to 0x00 793F	64	(1)

(1) Some registers are EALLOW protected. See the module reference guide for more information.

Table 8-9. Peripheral Frame 3 Registers

NAME	ADDRESS RANGE	SIZE (×16)	EALLOW PROTECTED
USB0 registers	0x00 4000 to 0x00 4FFF	4096	No
McBSP-A registers	0x00 5000 to 0x00 503F	64	No
Comparator 1 registers	0x00 6400 to 0x00 641F	32	(1)
Comparator 2 registers	0x00 6420 to 0x00 643F	32	(1)
Comparator 3 registers	0x00 6440 to 0x00 645F	32	(1)
ePWM1 + HRPWM1 registers	0x00 6800 to 0x00 683F	64	(1)
ePWM2 + HRPWM2 registers	0x00 6840 to 0x00 687F	64	(1)
ePWM3 + HRPWM3 registers	0x00 6880 to 0x00 68BF	64	(1)
ePWM4 + HRPWM4 registers	0x00 68C0 to 0x00 68FF	64	(1)
ePWM5 + HRPWM5 registers	0x00 6900 to 0x00 693F	64	(1)
ePWM6 + HRPWM6 registers	0x00 6940 to 0x00 697F	64	(1)
ePWM7 + HRPWM7 registers	0x00 6980 to 0x00 69BF	64	(1)
ePWM8 + HRPWM8 registers	0x00 69C0 to 0x00 69FF	64	(1)
eCAP1 registers	0x00 6A00 to 0x00 6A1F	32	No
eCAP2 registers	0x00 6A20 to 0x00 6A3F	32	No
eCAP3 registers	0x00 6A40 to 0x00 6A57	32	No
eQEP1 registers	0x00 6B00 to 0x00 6B3F	64	(1)
eQEP2 registers	0x00 6B40 to 0x00 6B7F	64	(1)

(1) Some registers are EALLOW protected. See the module reference guide for more information.

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8.4 Device Debug Registers

These registers are used to control the protection mode of the C28x CPU and to monitor some critical device signals. The registers are defined in Table 8-10.

Table 8-10. Device Debug Registers

NAME	ADDRESS RANGE	SIZE (×16)	DESCRIPTION			EALLOW PROTECTED
DEVICECNF	0x0880–0x0881	2	Device Configuration Register			Yes
PARTID	0x3D 7E80	1	Part ID Register	TMS320F28069PZP/PZ	0x009E	No
				TMS320F28069**U**PZP/PZ	0x009F	
				TMS320F28069**M**PZP/PZ	0x009E	
				TMS320F28069**F**PZP/PZ	0x009E	
				TMS320F28069PFP/PN	0x009C	
				TMS320F28069**U**PFP/PN	0x009D	
				TMS320F28069**M**PFP/PN	0x009C	
				TMS320F28069**F**PFP/PN	0x009C	
				TMS320F28068**U**PZP/PZ	0x008F	
				TMS320F28068**M**PZP/PZ	0x008E	
				TMS320F28068**F**PZP/PZ	0x008E	
				TMS320F28068**U**PFP/PN	0x008D	
				TMS320F28068**M**PFP/PN	0x008C	
				TMS320F28068**F**PFP/PN	0x008C	
				TMS320F28067PZP/PZ	0x008A	
				TMS320F28067**U**PZP/PZ	0x008B	
				TMS320F28067PFP/PN	0x0088	
				TMS320F28067**U**PFP/PN	0x0089	
				TMS320F28066PZP/PZ	0x0086	
				TMS320F28066**U**PZP/PZ	0x0087	
				TMS320F28066PFP/PN	0x0084	
				TMS320F28066**U**PFP/PN	0x0085	
				TMS320F28065PZP/PZ	0x007E	
				TMS320F28065**U**PZP/PZ	0x007F	
				TMS320F28065PFP/PN	0x007C	
				TMS320F28065**U**PFP/PN	0x007D	
				TMS320F28064PZP/PZ	0x006E	
				TMS320F28064**U**PZP/PZ	0x006F	
				TMS320F28064PFP/PN	0x006C	
				TMS320F28064**U**PFP/PN	0x006D	
				TMS320F28063PZP/PZ	0x006A	
				TMS320F28063**U**PZP/PZ	0x006B	
				TMS320F28063PFP/PN	0x0068	
				TMS320F28063**U**PFP/PN	0x0069	
				TMS320F28062PZP/PZ	0x0066	
				TMS320F28062**U**PZP/PZ	0x0067	
				TMS320F28062**F**PZP/PZ	0x0066	
				TMS320F28062PFP/PN	0x0064	
				TMS320F28062**U**PFP/PN	0x0065	
				TMS320F28062**F**PFP/PN	0x0064	

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Table 8-10. Device Debug Registers (continued)

NAME	ADDRESS RANGE	SIZE (×16)	DESCRIPTION			EALLOW PROTECTED
CLASSID	0x0882	1	Class ID Register	TMS320F28069	0x009F	No
				TMS320F28069**U**	0x009F	
				TMS320F28069**M**	0x009F	
				TMS320F28069**F**	0x009F	
				TMS320F28068**U**	0x008F	
				TMS320F28068**M**	0x008F	
				TMS320F28068**F**	0x008F	
				TMS320F28067	0x008F	
				TMS320F28067**U**	0x008F	
				TMS320F28066	0x008F	
				TMS320F28066**U**	0x008F	
				TMS320F28065	0x007F	
				TMS320F28065**U**	0x007F	
				TMS320F28064	0x006F	
				TMS320F28064**U**	0x006F	
				TMS320F28063	0x006F	
				TMS320F28063**U**	0x006F	
				TMS320F28062	0x006F	
				TMS320F28062**U**	0x006F	
				TMS320F28062**F**	0x006F	
REVID	0x0883	1	Revision ID Register	0x0000 - Silicon Rev. 0 - TMX		No
				0x0001 - Silicon Rev. A - TMS		
				0x0002 - Silicon Rev. B - TMS		
Instaspin feature	0x3D7FBE	1		0xFFFF = Normal part		No
				0xFF7F = Fast only (F part)		
				0xFF3F = Fast + Sping (M part)		

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8.5 VREG, BOR, POR

Although the core and I/O circuitry operate on two different voltages, these devices have an on-chip VREG to generate the V_{DD} voltage from the V_{DDIO} supply. This eliminates the cost and space of a second external regulator on an application board. Additionally, internal power-on reset (POR) and brownout reset (BOR) circuits monitor both the V_{DD} and V_{DDIO} rails during power-up and run mode.

8.5.1 On-chip VREG

A linear regulator generates the core voltage (V_{DD}) from the V_{DDIO} supply. Therefore, although capacitors are required on each V_{DD} pin to stabilize the generated voltage, power need not be supplied to these pins to operate the device. Conversely, the VREG can be disabled, should power or redundancy be the primary concern of the application.

8.5.1.1 Using the On-chip VREG

To use the on-chip VREG, the $\overline{\text{VREGENZ}}$ pin should be tied low and the appropriate recommended operating voltage should be supplied to the V_{DDIO} and V_{DDA} pins. In this case, the V_{DD} voltage needed by the core logic will be generated by the VREG. Each V_{DD} pin requires on the order of 1.2 µF (minimum) capacitance for proper regulation of the VREG. These capacitors should be located as close as possible to the V_{DD} pins. Driving an external load with the internal VREG is not supported.

8.5.1.2 Disabling the On-chip VREG

To conserve power, it is also possible to disable the on-chip VREG and supply the core logic voltage to the V_{DD} pins with a more efficient external regulator. To enable this option, the $\overline{\text{VREGENZ}}$ pin must be tied high.

8.5.2 On-chip Power-On Reset (POR) and Brownout Reset (BOR) Circuit

Two on-chip supervisory circuits, the power-on reset (POR) and the brownout reset (BOR) remove the burden of monitoring the V_{DD} and V_{DDIO} supply rails from the application board. The purpose of the POR is to create a clean reset throughout the device during the entire power-up procedure. The trip point is a looser, lower trip point than the BOR, which watches for dips in the V_{DD} or V_{DDIO} rail during device operation. The POR function is present on both V_{DD} and V_{DDIO} rails at all times. After initial device power-up, the BOR function is present on V_{DDIO} at all times, and on V_{DD} when the internal VREG is enabled ($\overline{\text{VREGENZ}}$ pin is tied low). Both functions tie the $\overline{\text{XRS}}$ pin low when one of the voltages is below their respective trip point. V_{DD} BOR and overvoltage trip points are outside of the recommended operating voltages. Proper device operation cannot be ensured. If overvoltage or undervoltage conditions affecting the system is a concern for an application, an external voltage supervisor should be added. Figure 8-9 shows the VREG, POR, and BOR. To disable both the V_{DD} and V_{DDIO} BOR functions, a bit is provided in the BORCFG register. For details, see the Systems Control and Interrupts chapter of the *TMS320x2806x Technical Reference Manual* .

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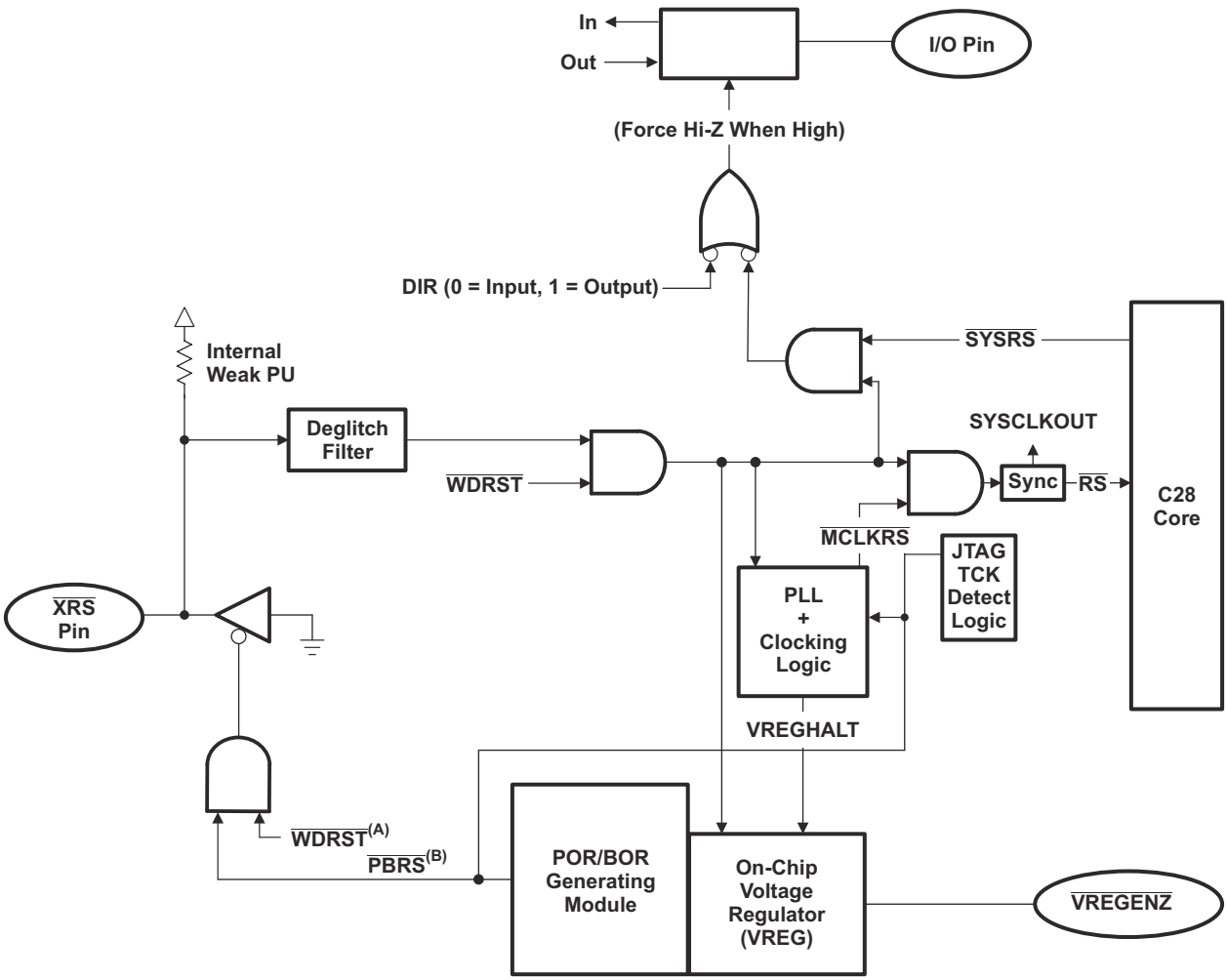

A. $\overline{\text{WDRST}}$ is the reset signal from the CPU-watchdog.
B. $\overline{\text{PBRS}}$ is the reset signal from the POR/BOR module.

Figure 8-9. VREG + POR + BOR + Reset Signal Connectivity

8.6 System Control

This section describes the oscillator and clocking mechanisms, the watchdog function and the low-power modes.

Table 8-11. PLL, Clocking, Watchdog, and Low-Power Mode Registers

NAME	ADDRESS	SIZE (×16)	DESCRIPTION(1)
BORCFG	0x00 0985	1	BOR Configuration Register
XCLK	0x00 7010	1	XCLKOUT Control
PLLSTS	0x00 7011	1	PLL Status Register
CLKCTL	0x00 7012	1	Clock Control Register
PLLLOCKPRD	0x00 7013	1	PLL Lock Period
INTOSC1TRIM	0x00 7014	1	Internal Oscillator 1 Trim Register
INTOSC2TRIM	0x00 7016	1	Internal Oscillator 2 Trim Register
PCLKCR2	0x00 7019	1	Peripheral Clock Control Register 2
LOSPCP	0x00 701B	1	Low-Speed Peripheral Clock Prescaler Register
PCLKCR0	0x00 701C	1	Peripheral Clock Control Register 0
PCLKCR1	0x00 701D	1	Peripheral Clock Control Register 1
LPMCR0	0x00 701E	1	Low-Power Mode Control Register 0
PCLKCR3	0x00 7020	1	Peripheral Clock Control Register 3
PLLCR	0x00 7021	1	PLL Control Register
SCSR	0x00 7022	1	System Control and Status Register
WDCNTR	0x00 7023	1	Watchdog Counter Register
WDKEY	0x00 7025	1	Watchdog Reset Key Register
WDCR	0x00 7029	1	Watchdog Control Register
JTAGDEBUG	0x00 702A	1	JTAG Port Debug Register
PLL2CTL	0x00 7030	1	PLL2 Configuration Register
PLL2MULT	0x00 7032	1	PLL2 Multiplier Register
PLL2STS	0x00 7034	1	PLL2 Lock Status Register
SYSCLK2CNTR	0x00 7036	1	SYSCLK2 Clock Counter Register
EPWMCFG	0x00 703A	1	ePWM DMA/CLA Configuration Register

(1) All registers in this table are EALLOW protected.

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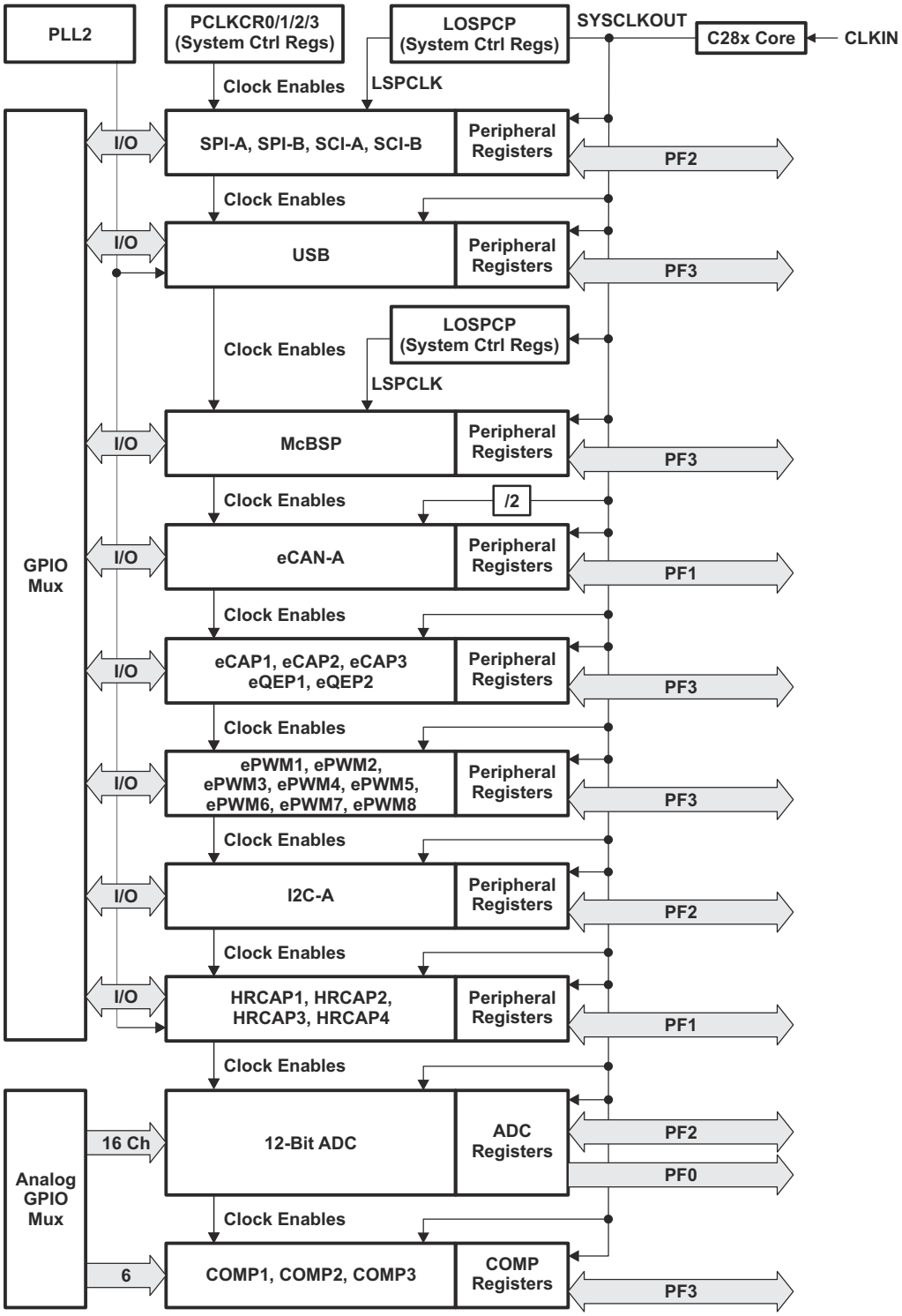
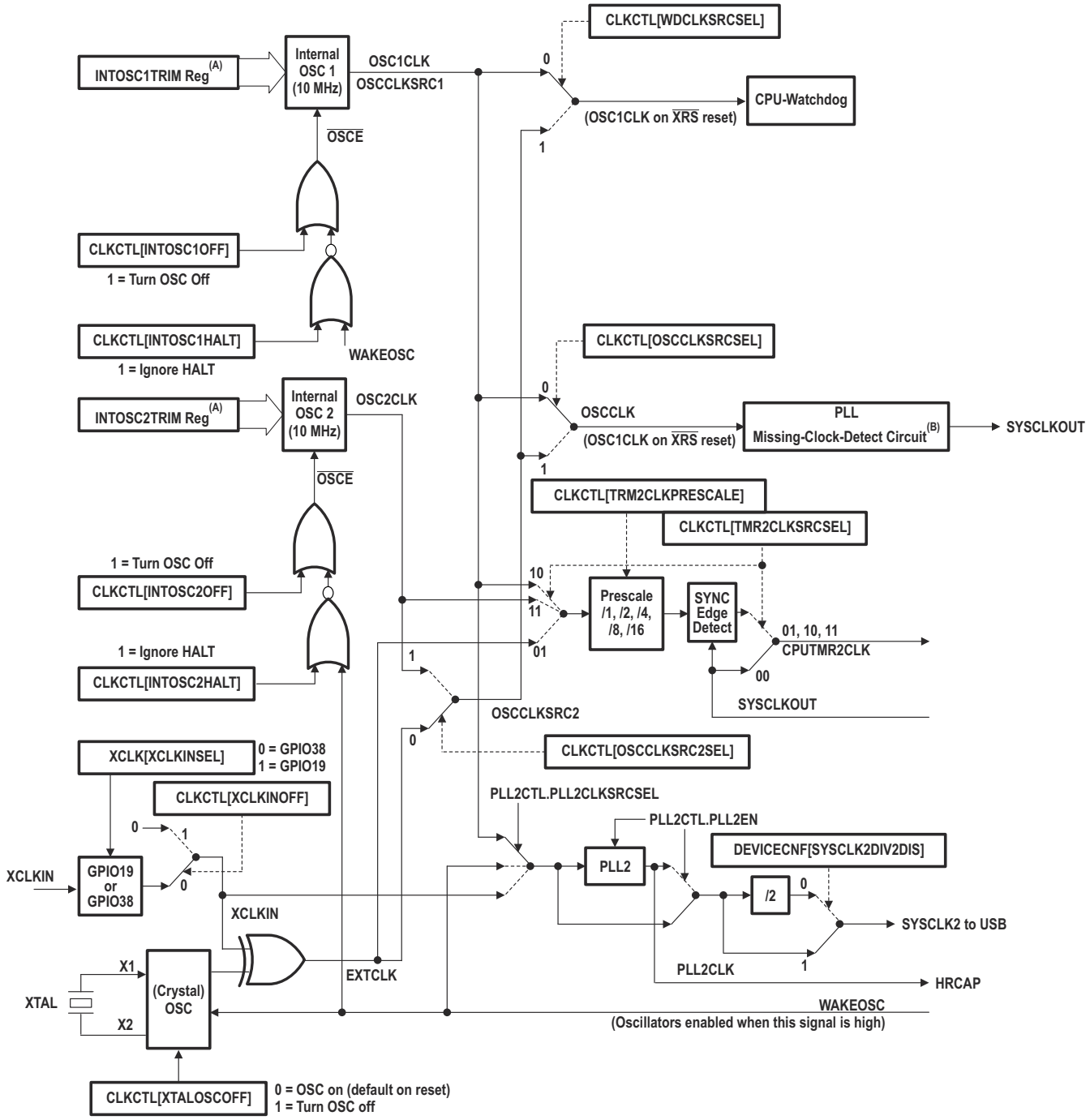
Figure 8-10 shows the various clock domains that are discussed. Figure 8-11 shows the various clock sources (both internal and external) that can provide a clock for device operation.



A. CLKIN is the clock into the CPU. CLKIN is passed out of the CPU as SYSCLKOUT (that is, CLKIN is the same frequency as SYSCLKOUT).

Figure 8-10. Clock and Reset Domains



A. Register loaded from TI OTP-based calibration function.

B. See Section 8.6.5 for details on missing clock detection.

Figure 8-11. Clock Tree

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8.6.1 Internal Zero Pin Oscillators

The F2806x devices contain two independent internal zero pin oscillators. By default both oscillators are turned on at power up, and internal oscillator 1 is the default clock source at this time. For power savings, unused oscillators may be powered down by the user. The center frequency of these oscillators is determined by their respective oscillator trim registers, written to in the calibration routine as part of the boot ROM execution. See Section 8.9 for more information on these oscillators.

8.6.2 Crystal Oscillator Option

The on-chip crystal oscillator X1 and X2 pins are 1.8-V level signals and must never have 3.3-V level signals applied to them. If a system 3.3-V external oscillator is to be used as a clock source, it should be connected to the XCLKIN pin only. The X1 pin is not intended to be used as a single-ended clock input, it should be used with X2 and a crystal.

The typical specifications for the external quartz crystal (fundamental mode, parallel resonant) are listed in Table 8-12. Furthermore, ESR range = 30 to 150 Ω. For Table 8-12, Cshunt should be less than or equal to 5 pF.

Table 8-12. Typical Specifications for External Quartz Crystal

FREQUENCY (MHz)	R_d (Ω)	C_{L1} (pF)	C_{L2} (pF)
5	2200	18	18
10	470	15	15
15	0	15	15
20	0	12	12

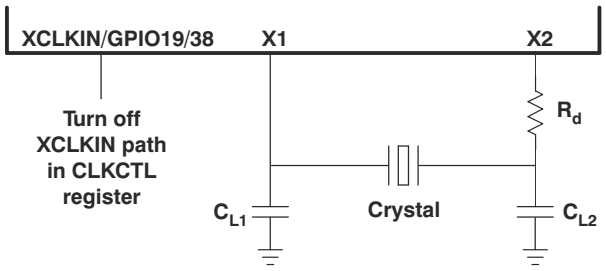

Figure 8-12. Using the On-chip Crystal Oscillator

Note

1. C_{L1} and C_{L2} are the total capacitance of the circuit board and components excluding the IC and crystal. The value is usually approximately twice the value of the load capacitance of the crystal.
2. The load capacitance of the crystal is described in the crystal specifications of the manufacturers.
3. TI recommends that customers have the resonator/crystal vendor characterize the operation of their device with the MCU chip. The resonator/crystal vendor has the equipment and expertise to tune the tank circuit. The vendor can also advise the customer regarding the proper tank component values that will produce proper start-up and stability over the entire operating range.

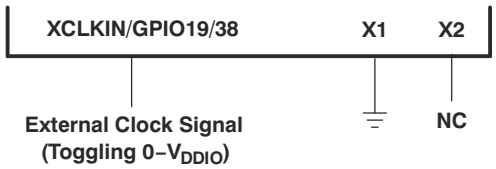

Figure 8-13. Using a 3.3-V External Oscillator

8.6.3 PLL-Based Clock Module

The devices have an on-chip, PLL-based clock module. This module provides all the necessary clocking signals for the device, as well as control for low-power mode entry. The PLL has a 5-bit ratio control PLLCR[DIV] to select different CPU clock rates. The watchdog module should be disabled before writing to the PLLCR register. The watchdog module can be re-enabled (if need be) after the PLL module has stabilized, which takes 1 ms. The input clock and PLLCR[DIV] bits should be chosen in such a way that the output frequency of the PLL (VCOCLK) is at least 50 MHz.

Table 8-13. PLL Settings

PLLCR[DIV] VALUE(2) (3)	SYSCLKOUT (CLKIN)		
	PLLSTS[DIVSEL] = 0 or 1(1)	PLLSTS[DIVSEL] = 2	PLLSTS[DIVSEL] = 3
00000 (PLL bypass)	OSCCLK/4 (Default)(2)	OSCCLK/2	OSCCLK
00001	(OSCCLK * 1)/4	(OSCCLK * 1)/2	(OSCCLK * 1)/1
00010	(OSCCLK * 2)/4	(OSCCLK * 2)/2	(OSCCLK * 2)/1
00011	(OSCCLK * 3)/4	(OSCCLK * 3)/2	(OSCCLK * 3)/1
00100	(OSCCLK * 4)/4	(OSCCLK * 4)/2	(OSCCLK * 4)/1
00101	(OSCCLK * 5)/4	(OSCCLK * 5)/2	(OSCCLK * 5)/1
00110	(OSCCLK * 6)/4	(OSCCLK * 6)/2	(OSCCLK * 6)/1
00111	(OSCCLK * 7)/4	(OSCCLK * 7)/2	(OSCCLK * 7)/1
01000	(OSCCLK * 8)/4	(OSCCLK * 8)/2	(OSCCLK * 8)/1
01001	(OSCCLK * 9)/4	(OSCCLK * 9)/2	(OSCCLK * 9)/1
01010	(OSCCLK * 10)/4	(OSCCLK * 10)/2	(OSCCLK * 10)/1
01011	(OSCCLK * 11)/4	(OSCCLK * 11)/2	(OSCCLK * 11)/1
01100	(OSCCLK * 12)/4	(OSCCLK * 12)/2	(OSCCLK * 12)/1
01101	(OSCCLK * 13)/4	(OSCCLK * 13)/2	(OSCCLK * 13)/1
01110	(OSCCLK * 14)/4	(OSCCLK * 14)/2	(OSCCLK * 14)/1
01111	(OSCCLK * 15)/4	(OSCCLK * 15)/2	(OSCCLK * 15)/1
10000	(OSCCLK * 16)/4	(OSCCLK * 16)/2	(OSCCLK * 16)/1
10001	(OSCCLK * 17)/4	(OSCCLK * 17)/2	(OSCCLK * 17)/1
10010	(OSCCLK * 18)/4	(OSCCLK * 18)/2	(OSCCLK * 18)/1

(1) By default, PLLSTS[DIVSEL] is configured for /4. (The boot ROM changes this to /1.) PLLSTS[DIVSEL] must be 0 before writing to the PLLCR and should be changed only after PLLSTS[PLLLOCKS] = 1.
(2) The PLL control register (PLLCR) and PLL Status Register (PLLSTS) are reset to their default state by the $\overline{\text{XRS}}$ signal or a watchdog reset only. A reset issued by the debugger or the missing clock detect logic has no effect.
(3) This register is EALLOW protected. See the Systems Control and Interrupts chapter of the *TMS320x2806x Technical Reference Manual* for more information.

Table 8-14. CLKIN Divide Options

PLLSTS [DIVSEL]	CLKIN DIVIDE
0	/4
1	/4
2	/2
3	/1

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The PLL-based clock module provides four modes of operation:

- I**NTOSC1 (Internal Zero-pin Oscillator 1):** This is the on-chip internal oscillator 1. This can provide the clock for the Watchdog block, core and CPU-Timer 2
- **INTOSC2 (Internal Zero-pin Oscillator 2):** This is the on-chip internal oscillator 2. This can provide the clock for the Watchdog block, core and CPU-Timer 2. Both INTOSC1 and INTOSC2 can be independently chosen for the Watchdog block, core and CPU-Timer 2.
- **Crystal/Resonator Operation:** The on-chip (crystal) oscillator enables the use of an external crystal/ resonator attached to the device to provide the time base. The crystal/resonator is connected to the X1/X2 pins. Some devices may not have the X1/X2 pins. See Section 6.2.1 for details.
- **External Clock Source Operation:** If the on-chip (crystal) oscillator is not used, this mode allows it to be bypassed. The device clocks are generated from an external clock source input on the XCLKIN pin. The XCLKIN is multiplexed with GPIO19 or GPIO38 pin. The XCLKIN input can be selected as GPIO19 or GPIO38 through the XCLKINSEL bit in XCLK register. The CLKCTL[XCLKINOFF] bit disables this clock input (forced low). If the clock source is not used or the respective pins are used as GPIOs, the user should disable at boot time.

Before changing clock sources, ensure that the target clock is present. If a clock is not present, then that clock source must be disabled (using the CLKCTL register) before switching clocks.

Table 8-15. Possible PLL Configuration Modes

PLL MODE	REMARKS	PLLSTS[DIVSEL]	CLKIN AND SYSCLKOUT
PLL Off	Invoked by the user setting the PLLOFF bit in the PLLSTS register. The PLL block is disabled in this mode. This can be useful to reduce system noise and for low-power operation. The PLLCR register must first be set to 0x0000 (PLL Bypass) before entering this mode. The CPU clock (CLKIN) is derived directly from the input clock on either X1/X2, X1 or XCLKIN.	0, 1 2 3	OSCCLK/4 OSCCLK/2 OSCCLK/1
PLL Bypass	PLL Bypass is the default PLL configuration upon power-up or after an external reset ($\overline{\text{XRS}}$). This mode is selected when the PLLCR register is set to 0x0000 or while the PLL locks to a new frequency after the PLLCR register has been modified. In this mode, the PLL is bypassed but the PLL is not turned off.	0, 1 2 3	OSCCLK/4 OSCCLK/2 OSCCLK/1
PLL Enable	Achieved by writing a non-zero value n into the PLLCR register. Upon writing to the PLLCR the device will switch to PLL Bypass mode until the PLL locks.	0, 1 2 3	OSCCLK * n/4 OSCCLK * n/2 OSCCLK * n/1

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8.6.4 USB and HRCAP PLL Module (PLL2)

In addition to the main system PLL, these devices also contain a second PLL (PLL2) which can be used to clock the USB and HRCAP peripherals. The PLL supports multipliers of 1 to 15 and has a fixed divide-by-two on its output.

PLL2 may be clocked from the following three sources by modifying the PLL2CLKSRCSEL bits appropriately in the PLL2CTL register:

- INTOSC1 (Internal Zero-pin Oscillator 1): This is the on-chip internal oscillator 1 and provides a 10-MHz clock. If used as a clock source for HRCAP, the oscillator compensation routine should be called frequently. Because of accuracy requirements, INTOSC1 cannot be used as a clock source for the USB.
- Crystal/Resonator Operation: The (crystal) oscillator enables the use of an external crystal or resonator attached to the device to provide the time base. The crystal or resonator is connected to the X1/X2 pins.
- External Clock Source Operation: This mode allows the reference clock to be derived from an external single-ended clock source connected to either GPIO19 or GPIO38. The XCLKINSEL bit in the XCLK register should be set appropriately to enable the selected GPIO to drive XCLKIN.

Note

For proper operation of the USB module, PLL2 should be configured to generate a 120-MHz clock. This will be divided by two to yield the desired 60 MHz for the USB peripheral.

HRCAP supports a maximum clock input frequency of 120 MHz.

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8.6.5 Loss of Input Clock (NMI Watchdog Function)

The 2806x devices may be clocked from either one of the internal zero-pin oscillators (INTOSC1/INTOSC2), the on-chip crystal oscillator, or from an external clock input. Regardless of the clock source, in PLL-enabled and PLL-bypass mode, if the input clock to the PLL vanishes, the PLL will issue a limp-mode clock at its output. This limp-mode clock continues to clock the CPU and peripherals at a typical frequency of 1–5 MHz.

When the limp mode is activated, a $\overline{\text{CLOCKFAIL}}$ signal is generated that is latched as an NMI interrupt. Depending on how the NMIRESETSEL bit has been configured, a reset to the device can be fired immediately or the NMI watchdog counter can issue a reset when it overflows. In addition to this, the Missing Clock Status (MCLKSTS) bit is set. The NMI interrupt could be used by the application to detect the input clock failure and initiate necessary corrective action such as switching over to an alternative clock source (if available) or initiate a shut-down procedure for the system.

If the software does not respond to the clock-fail condition, the NMI watchdog triggers a reset after a preprogrammed time interval. Figure 8-14 shows the interrupt mechanisms involved.

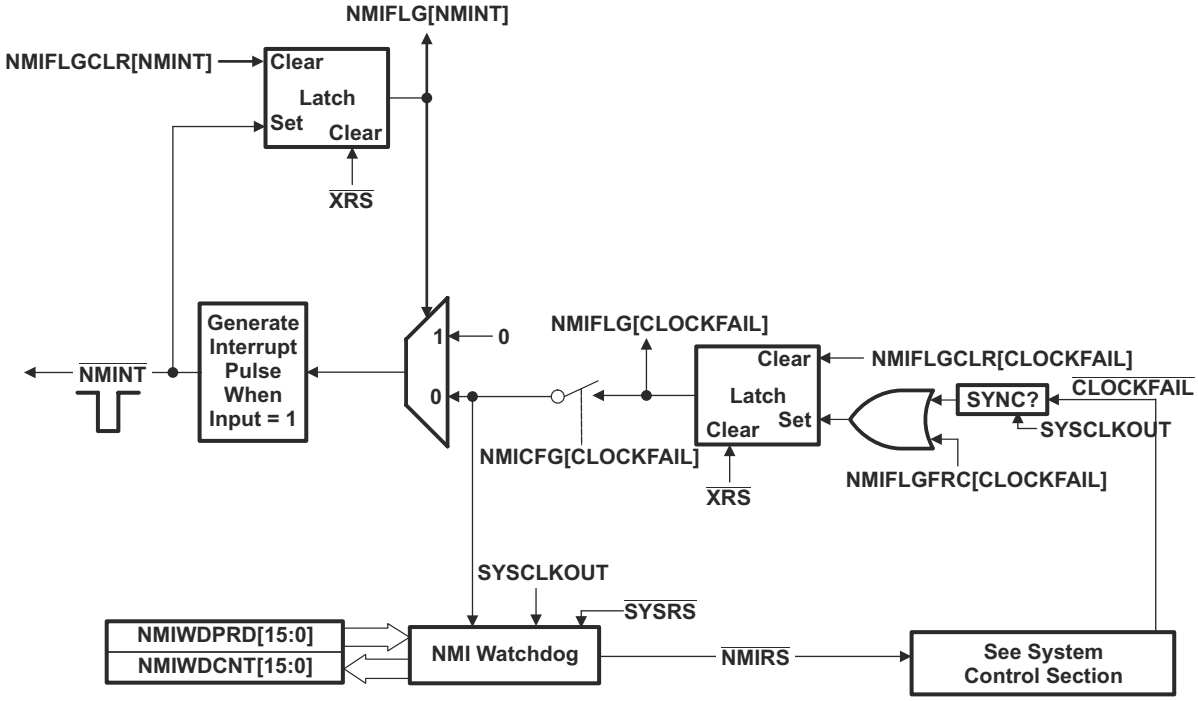

Figure 8-14. NMI-Watchdog

8.6.6 CPU Watchdog Module

The CPU watchdog module on the 2806x device is similar to the one used on the 281x/280x/283xx devices. This module generates an output pulse, 512 oscillator clocks wide (OSCCLK), whenever the 8-bit watchdog up counter has reached its maximum value. To prevent this, the user must disable the counter or the software must periodically write a 0x55 + 0xAA sequence into the watchdog key register that resets the watchdog counter. Figure 8-15 shows the various functional blocks within the watchdog module.

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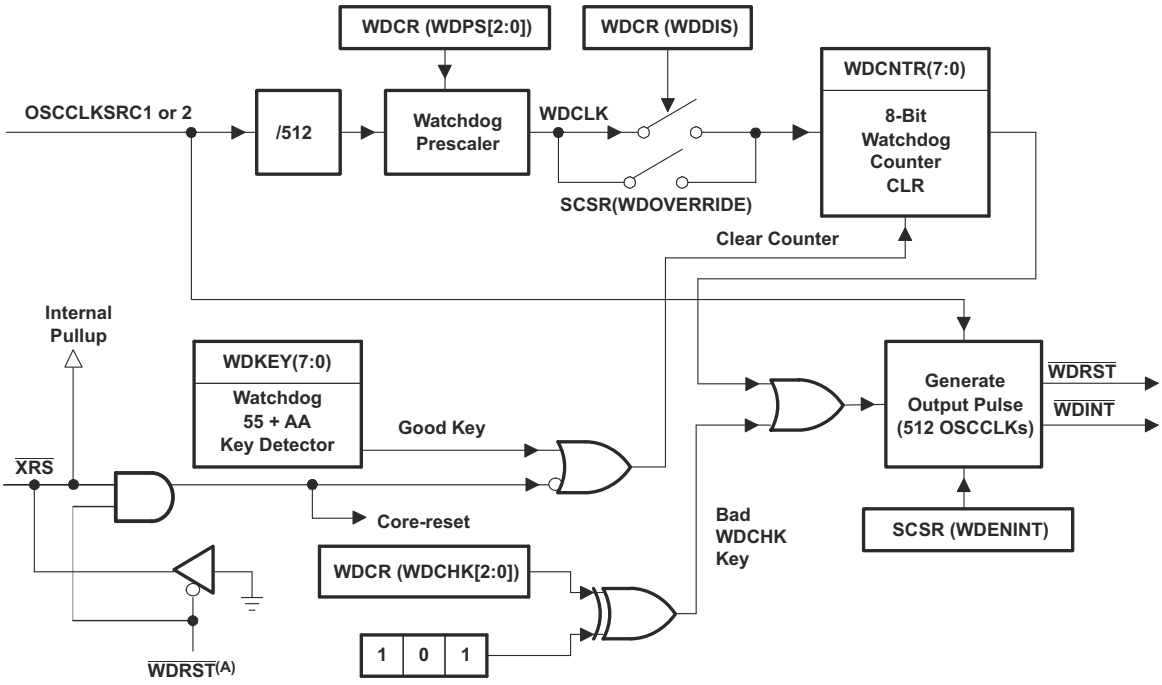
Normally, when the input clocks are present, the CPU-watchdog counter decrements to initiate a CPU-watchdog reset or WDINT interrupt. However, when the external input clock fails, the CPU-watchdog counter stops decrementing (that is, the watchdog counter does not change with the limp-mode clock).

Note

The CPU-watchdog is different from the NMI watchdog. The CPU-watchdog is the legacy watchdog that is present in all 28x devices.

Note

Applications in which the correct CPU operating frequency is absolutely critical should implement a mechanism by which the MCU will be held in reset, should the input clocks ever fail. For example, an R-C circuit may be used to trigger the $\overline{XRS}$ pin of the MCU, should the capacitor ever get fully charged. An I/O pin may be used to discharge the capacitor on a periodic basis to prevent it from getting fully charged. Such a circuit would also help in detecting failure of the flash memory.



A. The $\overline{WDRST}$ signal is driven low for 512 OSCCLK cycles.

Figure 8-15. CPU Watchdog Module

The $\overline{WDINT}$ signal enables the watchdog to be used as a wakeup from IDLE/STANDBY mode.

In STANDBY mode, all peripherals are turned off on the device. The only peripheral that remains functional is the CPU-watchdog. This module will run off OSCCLK. The $\overline{WDINT}$ signal is fed to the LPM block so that it can wake the device from STANDBY (if enabled). See Section 8.7 for more details.

In IDLE mode, the $\overline{WDINT}$ signal can generate an interrupt to the CPU, through the PIE, to take the CPU out of IDLE mode.

In HALT mode, the CPU-watchdog can be used to wake up the device through a device reset.

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8.7 Low-power Modes Block

Table 8-16 summarizes the various modes.

Table 8-16. Low-power Modes

MODE	LPMCR0(1:0)	OSCCLK	CLKIN	SYSCLKOUT	EXIT(1)
IDLE	00	On	On	On	$\overline{XRS}$, CPU-watchdog interrupt, any enabled interrupt
STANDBY	01	On (CPU-watchdog still running)	Off	Off	$\overline{XRS}$, CPU-watchdog interrupt, GPIO Port A signal, debugger(2)
HALT(3)	1X	Off (on-chip crystal oscillator and PLL turned off, zero-pin oscillator and CPU-watchdog state dependent on user code.)	Off	Off	$\overline{XRS}$, GPIO Port A signal, debugger(2), CPU-watchdog

(1) The EXIT column lists which signals or under what conditions the low-power mode is exited. A low signal, on any of the signals, exits the low-power condition. This signal must be kept low long enough for an interrupt to be recognized by the device. Otherwise, the low-power mode will not be exited and the device will go back into the indicated low-power mode.
(2) The JTAG port can still function even if the CPU clock (CLKIN) is turned off.
(3) The WDCLK must be active for the device to go into HALT mode.

The various low-power modes operate as follows:

IDLE Mode:	This mode is exited by any enabled interrupt that is recognized by the processor. The LPM block performs no tasks during this mode as long as the LPMCR0(LPM) bits are set to 0,0.
STANDBY Mode:	Any GPIO port A signal (GPIO[31:0]) can wake the device from STANDBY mode. The user must select which signals will wake the device in the GPIOLPMSEL register. The selected signals are also qualified by the OSCCLK before waking the device. The number of OSCCLKs is specified in the LPMCR0 register.
HALT Mode:	CPU-watchdog, $\overline{XRS}$, and any GPIO port A signal (GPIO[31:0]) can wake the device from HALT mode. The user selects the signal in the GPIOLPMSEL register.

Note

The low-power modes do not affect the state of the output pins (PWM pins included). They will be in whatever state the code left them in when the IDLE instruction was executed. See the Systems Control and Interrupts chapter of the *TMS320x2806x Technical Reference Manual* for more details.

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8.8 Interrupts

Figure 8-16 shows how the various interrupt sources are multiplexed.

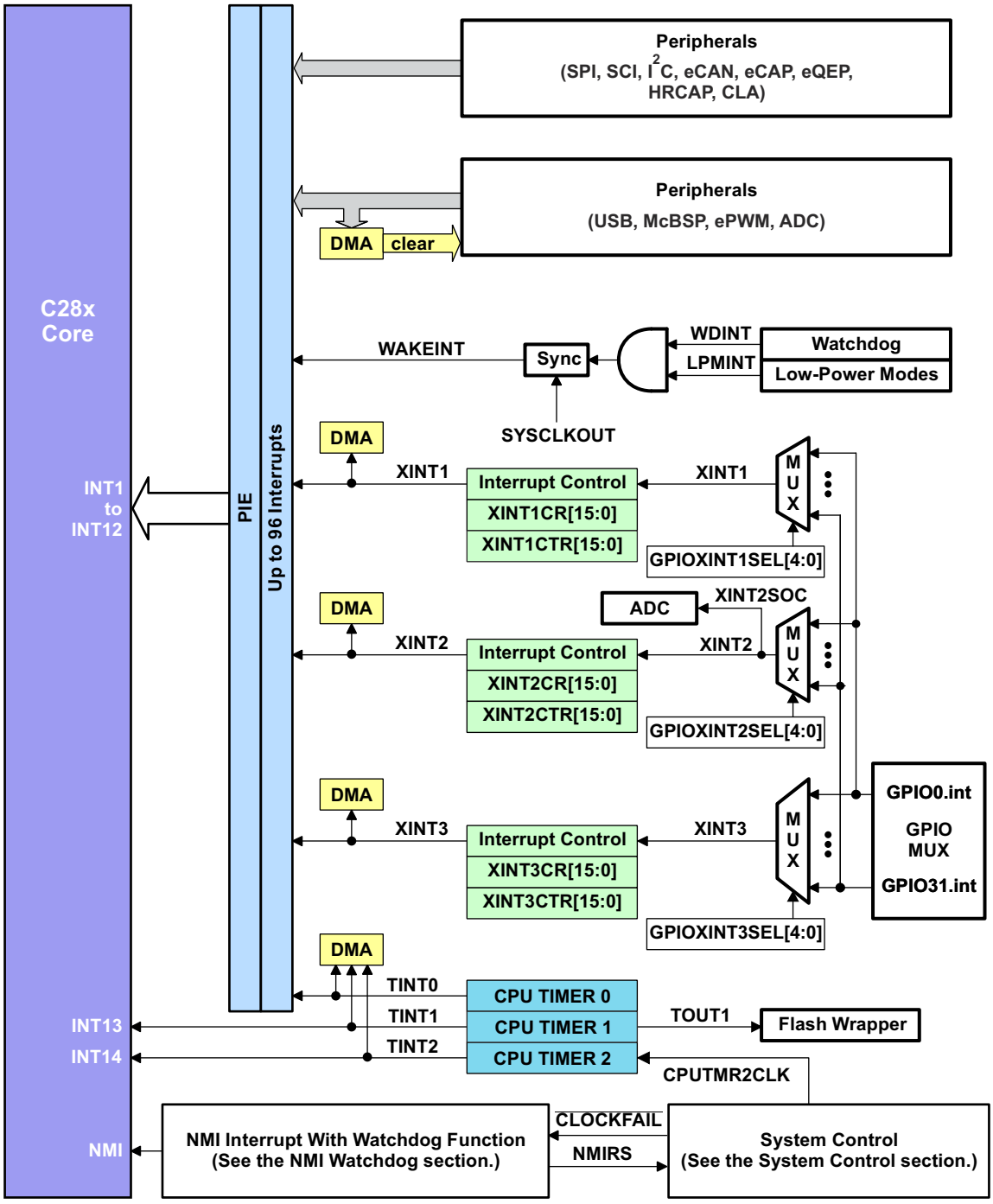

Figure 8-16. External and PIE Interrupt Sources

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Eight PIE block interrupts are grouped into one CPU interrupt. In total, 12 CPU interrupt groups, with 8 interrupts per group equals 96 possible interrupts. Table 8-17 shows the interrupts used by 2806x devices.

The TRAP #VectorNumber instruction transfers program control to the interrupt service routine (ISR) corresponding to the vector specified. The TRAP #0 instruction attempts to transfer program control to the address pointed to by the reset vector. The PIE vector table does not, however, include a reset vector. Therefore, the TRAP #0 instruction should not be used when the PIE is enabled. Doing so will result in undefined behavior.

When the PIE is enabled, the TRAP #1 to TRAP #12 instructions will transfer program control to the ISR corresponding to the first vector within the PIE group. For example: the TRAP #1 instruction fetches the vector from INT1.1, the TRAP #2 instruction fetches the vector from INT2.1, and so forth.

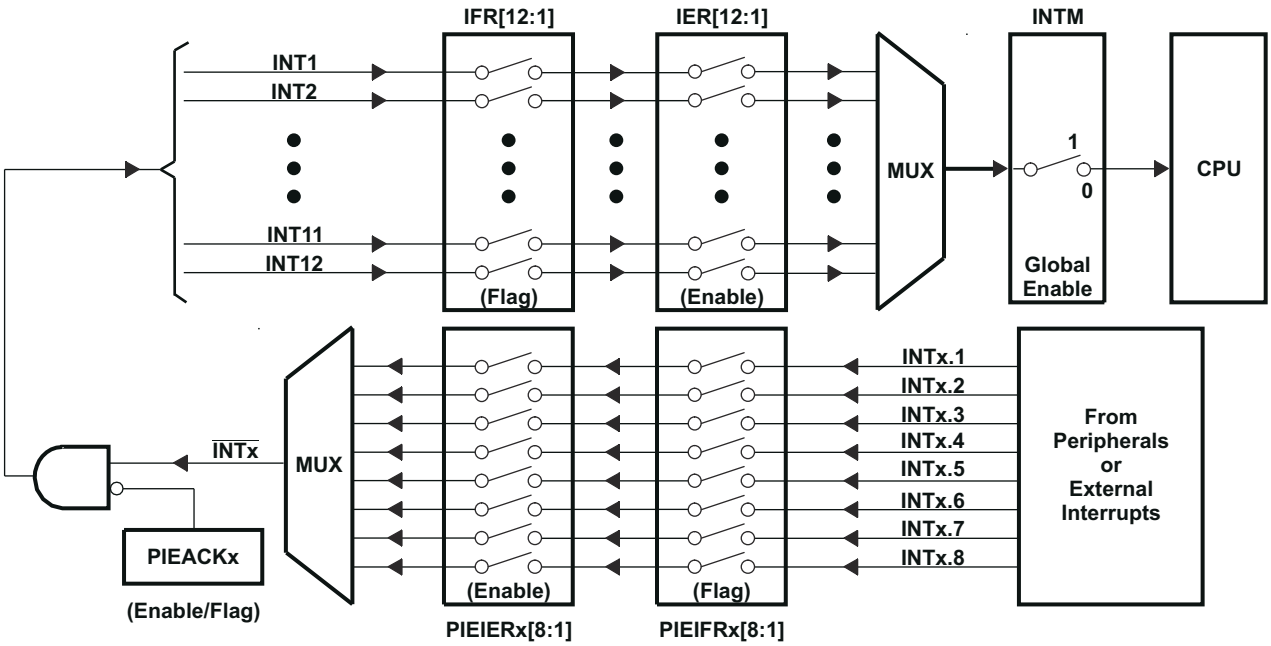

Figure 8-17. Multiplexing of Interrupts Using the PIE Block

Out of 96 possible interrupts, some interrupts are not used. These interrupts are reserved for future devices. These interrupts can be used as software interrupts if they are enabled at the PIEIFRx level, provided none of the interrupts within the group is being used by a peripheral. Otherwise, interrupts coming in from peripherals may be lost by accidentally clearing their flag while modifying the PIEIFR. To summarize, there are two safe cases when the reserved interrupts could be used as software interrupts:

1. No peripheral within the group is asserting interrupts.
2. No peripheral interrupts are assigned to the group (for example, PIE group 7).

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Table 8-17. PIE MUXed Peripheral Interrupt Vector Table

	INTx.8	INTx.7	INTx.6	INTx.5	INTx.4	INTx.3	INTx.2	INTx.1
INT1.y	WAKEINT (LPM/WD) 0xD4E	TINT0 (TIMER 0) 0xD4C	ADCINT9 (ADC) 0xD4A	XINT2 Ext. int. 2 0xD48	XINT1 Ext. int. 1 0xD46	Reserved – 0xD44	ADCINT2 (ADC) 0xD42	ADCINT1 (ADC) 0xD40
INT2.y	EPWM8_TZINT (ePWM8) 0xD5E	EPWM7_TZINT (ePWM7) 0xD5C	EPWM6_TZINT (ePWM6) 0xD5A	EPWM5_TZINT (ePWM5) 0xD58	EPWM4_TZINT (ePWM4) 0xD56	EPWM3_TZINT (ePWM3) 0xD54	EPWM2_TZINT (ePWM2) 0xD52	EPWM1_TZINT (ePWM1) 0xD50
INT3.y	EPWM8_INT (ePWM8) 0xD6E	EPWM7_INT (ePWM7) 0xD6C	EPWM6_INT (ePWM6) 0xD6A	EPWM5_INT (ePWM5) 0xD68	EPWM4_INT (ePWM4) 0xD66	EPWM3_INT (ePWM3) 0xD64	EPWM2_INT (ePWM2) 0xD62	EPWM1_INT (ePWM1) 0xD60
INT4.y	HRCAP2_INT (HRCAP2) 0xD7E	HRCAP1_INT (HRCAP1) 0xD7C	Reserved – 0xD7A	Reserved – 0xD78	Reserved – 0xD76	ECAP3_INT (eCAP3) 0xD74	ECAP2_INT (eCAP2) 0xD72	ECAP1_INT (eCAP1) 0xD70
INT5.y	USB0_INT (USB0) 0xD8E	Reserved – 0xD8C	Reserved – 0xD8A	HRCAP4_INT (HRCAP4) 0xD88	HRCAP3_INT (HRCAP3) 0xD86	Reserved – 0xD84	EQEP2_INT (eQEP2) 0xD82	EQEP1_INT (eQEP1) 0xD80
INT6.y	Reserved – 0xD9E	Reserved – 0xD9C	MXINTA (McBSP-A) 0xD9A	MRINTA (McBSP-A) 0xD98	SPITXINTB (SPI-B) 0xD96	SPIRXINTB (SPI-B) 0xD94	SPITXINTA (SPI-A) 0xD92	SPIRXINTA (SPI-A) 0xD90
INT7.y	Reserved – 0xDAE	Reserved – 0xDAC	DINTCH6 (DMA) 0xDAA	DINTCH5 (DMA) 0xDA8	DINTCH4 (DMA) 0xDA6	DINTCH3 (DMA) 0xDA4	DINTCH2 (DMA) 0xDA2	DINTCH1 (DMA) 0xDA0
INT8.y	Reserved – 0xDBE	Reserved – 0xDBC	Reserved – 0xDBA	Reserved – 0xDB8	Reserved – 0xDB6	Reserved – 0xDB4	I2CINT2A (I2C-A) 0xDB2	I2CINT1A (I2C-A) 0xDB0
INT9.y	Reserved – 0xDCE	Reserved – 0xDCC	ECAN1_INTA (CAN-A) 0xDCA	ECAN0_INTA (CAN-A) 0xDC8	SCITXINTB (SCI-B) 0xDC6	SCIRXINTB (SCI-B) 0xDC4	SCITXINTA (SCI-A) 0xDC2	SCIRXINTA (SCI-A) 0xDC0
INT10.y	ADCINT8 (ADC) 0xDDE	ADCINT7 (ADC) 0xDDC	ADCINT6 (ADC) 0xDDA	ADCINT5 (ADC) 0xDD8	ADCINT4 (ADC) 0xDD6	ADCINT3 (ADC) 0xDD4	ADCINT2 (ADC) 0xDD2	ADCINT1 (ADC) 0xDD0
INT11.y	CLA1_INT8 (CLA) 0xDEE	CLA1_INT7 (CLA) 0xDEC	CLA1_INT6 (CLA) 0xDEA	CLA1_INT5 (CLA) 0xDE8	CLA1_INT4 (CLA) 0xDE6	CLA1_INT3 (CLA) 0xDE4	CLA1_INT2 (CLA) 0xDE2	CLA1_INT1 (CLA) 0xDE0
INT12.y	LUF (CLA) 0xDFE	LVF (CLA) 0xDFC	Reserved – 0xDFA	Reserved – 0xDF8	Reserved – 0xDF6	Reserved – 0xDF4	Reserved – 0xDF2	XINT3 Ext. Int. 3 0xDF0

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Table 8-18. PIE Configuration and Control Registers

NAME	ADDRESS	SIZE (×16)	DESCRIPTION(1)
PIECTRL	0x0CE0	1	PIE, Control Register
PIEACK	0x0CE1	1	PIE, Acknowledge Register
PIEIER1	0x0CE2	1	PIE, INT1 Group Enable Register
PIEIFR1	0x0CE3	1	PIE, INT1 Group Flag Register
PIEIER2	0x0CE4	1	PIE, INT2 Group Enable Register
PIEIFR2	0x0CE5	1	PIE, INT2 Group Flag Register
PIEIER3	0x0CE6	1	PIE, INT3 Group Enable Register
PIEIFR3	0x0CE7	1	PIE, INT3 Group Flag Register
PIEIER4	0x0CE8	1	PIE, INT4 Group Enable Register
PIEIFR4	0x0CE9	1	PIE, INT4 Group Flag Register
PIEIER5	0x0CEA	1	PIE, INT5 Group Enable Register
PIEIFR5	0x0CEB	1	PIE, INT5 Group Flag Register
PIEIER6	0x0CEC	1	PIE, INT6 Group Enable Register
PIEIFR6	0x0CED	1	PIE, INT6 Group Flag Register
PIEIER7	0x0CEE	1	PIE, INT7 Group Enable Register
PIEIFR7	0x0CEF	1	PIE, INT7 Group Flag Register
PIEIER8	0x0CF0	1	PIE, INT8 Group Enable Register
PIEIFR8	0x0CF1	1	PIE, INT8 Group Flag Register
PIEIER9	0x0CF2	1	PIE, INT9 Group Enable Register
PIEIFR9	0x0CF3	1	PIE, INT9 Group Flag Register
PIEIER10	0x0CF4	1	PIE, INT10 Group Enable Register
PIEIFR10	0x0CF5	1	PIE, INT10 Group Flag Register
PIEIER11	0x0CF6	1	PIE, INT11 Group Enable Register
PIEIFR11	0x0CF7	1	PIE, INT11 Group Flag Register
PIEIER12	0x0CF8	1	PIE, INT12 Group Enable Register
PIEIFR12	0x0CF9	1	PIE, INT12 Group Flag Register
Reserved	0x0CFA – 0x0CFF	6	Reserved

(1) The PIE configuration and control registers are not protected by EALLOW mode. The PIE vector table is protected.

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8.8.1 External Interrupts

Table 8-19. External Interrupt Registers

NAME	ADDRESS	SIZE (×16)	DESCRIPTION
XINT1CR	0x00 7070	1	XINT1 configuration register
XINT2CR	0x00 7071	1	XINT2 configuration register
XINT3CR	0x00 7072	1	XINT3 configuration register
XINT1CTR	0x00 7078	1	XINT1 counter register
XINT2CTR	0x00 7079	1	XINT2 counter register
XINT3CTR	0x00 707A	1	XINT3 counter register

Each external interrupt can be enabled or disabled or qualified using positive, negative, or both positive and negative edge. For more information, see the Systems Control and Interrupts chapter of the *TMS320x2806x Technical Reference Manual* .

8.8.1.1 External Interrupt Electrical Data/Timing

8.8.1.1.1 External Interrupt Timing Requirements

			MIN(1)	MAX	UNIT
$t_{w(INT)}$ (2)	Pulse duration, INT input low/high	Synchronous	$1t_{c(SCO)}$		cycles
		With qualifier	$1t_{c(SCO)} + t_{w(IQSW)}$		cycles

(1) For an explanation of the input qualifier parameters, see Section 8.9.15.1.2.1.
(2) This timing is applicable to any GPIO pin configured for ADCSOC functionality.

8.8.1.1.2 External Interrupt Switching Characteristics

over recommended operating conditions (unless otherwise noted)(1)

PARAMETER		MIN	MAX	UNIT
$t_{d(INT)}$	Delay time, INT low/high to interrupt-vector fetch		$t_{w(IQSW)} + 12t_{c(SCO)}$	cycles

(1) For an explanation of the input qualifier parameters, see Section 8.9.15.1.2.1.

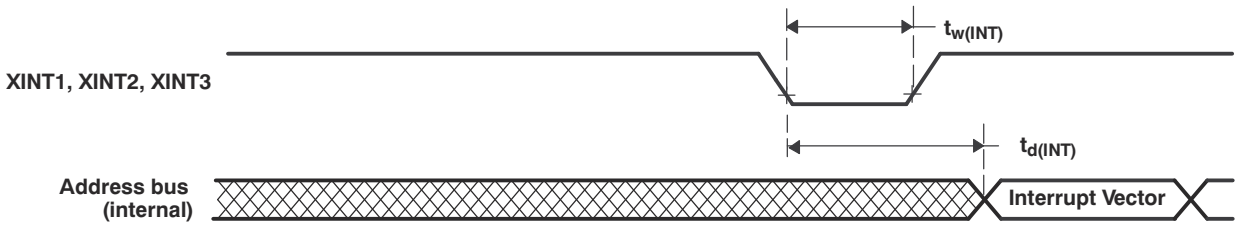

Figure 8-18. External Interrupt Timing

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8.9 Peripherals

8.9.1 CLA Overview

The CLA extends the capabilities of the C28x CPU by adding parallel processing. Time-critical control loops serviced by the CLA can achieve low ADC sample to output delay. Thus, the CLA enables faster system response and higher frequency control loops. Using the CLA for time-critical tasks frees the main CPU to perform other system and communication functions concurently. A list of major features of the CLA follows.

- Clocked at the same rate as the main CPU (SYSCLKOUT)
- An independent architecture allowing CLA algorithm execution independent of the main C28x CPU
  - Complete bus architecture:
    - Program address bus and program data bus
    - Data address bus, data read bus, and data write bus
  - Independent eight-stage pipeline
  - 12-bit program counter (MPC)
  - Four 32-bit result registers (MR0 to MR3)
  - Two 16-bit auxillary registers (MAR0, MAR1)
  - Status register (MSTF)
- Instruction set includes:
  - IEEE single-precision (32-bit) floating-point math operations
  - Floating-point math with parallel load or store
  - Floating-point multiply with parallel add or subtract
  - 1/X and 1/sqrt(X) estimations
  - Data type conversions
  - Conditional branch and call
  - Data load and store operations
- The CLA program code can consist of up to eight tasks or ISRs.
  - The start address of each task is specified by the MVECT registers.
  - No limit on task size as long as the tasks fit within the CLA program memory space.
  - One task at a time is serviced to completion. Tasks are not nested.
  - Upon task completion, a task-specific interrupt is flagged within the PIE.
  - When a task finishes, the next highest-priority pending task is automatically started.
- Task trigger mechanisms:
  - C28x CPU through the IACK instruction
  - Task1 to Task7: the corresponding ADC, ePWM, eQEP, or eCAP module interrupt. For example:
    - Task1: ADCINT1 or EPWM1_INT
    - Task2: ADCINT2 or EPWM2_INT
    - Task4: ADCINT4 or EPWM4_INT or EQEPx_INT or ECAPx_INT
    - Task7: ADCINT7 or EPWM7_INT or EQEPx_INT or ECAPx_INT
  - Task8: ADCINT8 or by CPU Timer 0 or EQEPx_INT or ECAPx_INT.
- Memory and Shared Peripherals:
  - Two dedicated message RAMs for communication between the CLA and the main CPU
  - The C28x CPU can map CLA program and data memory to the main CPU space or CLA space.
  - The CLA has direct access to the ADC Result registers, comparator registers, and the eCAP, eQEP, and ePWM+HRPWM registers.

Figure 8-19 shows the CLA block diagram. Table 8-20 lists the CLA control registers.

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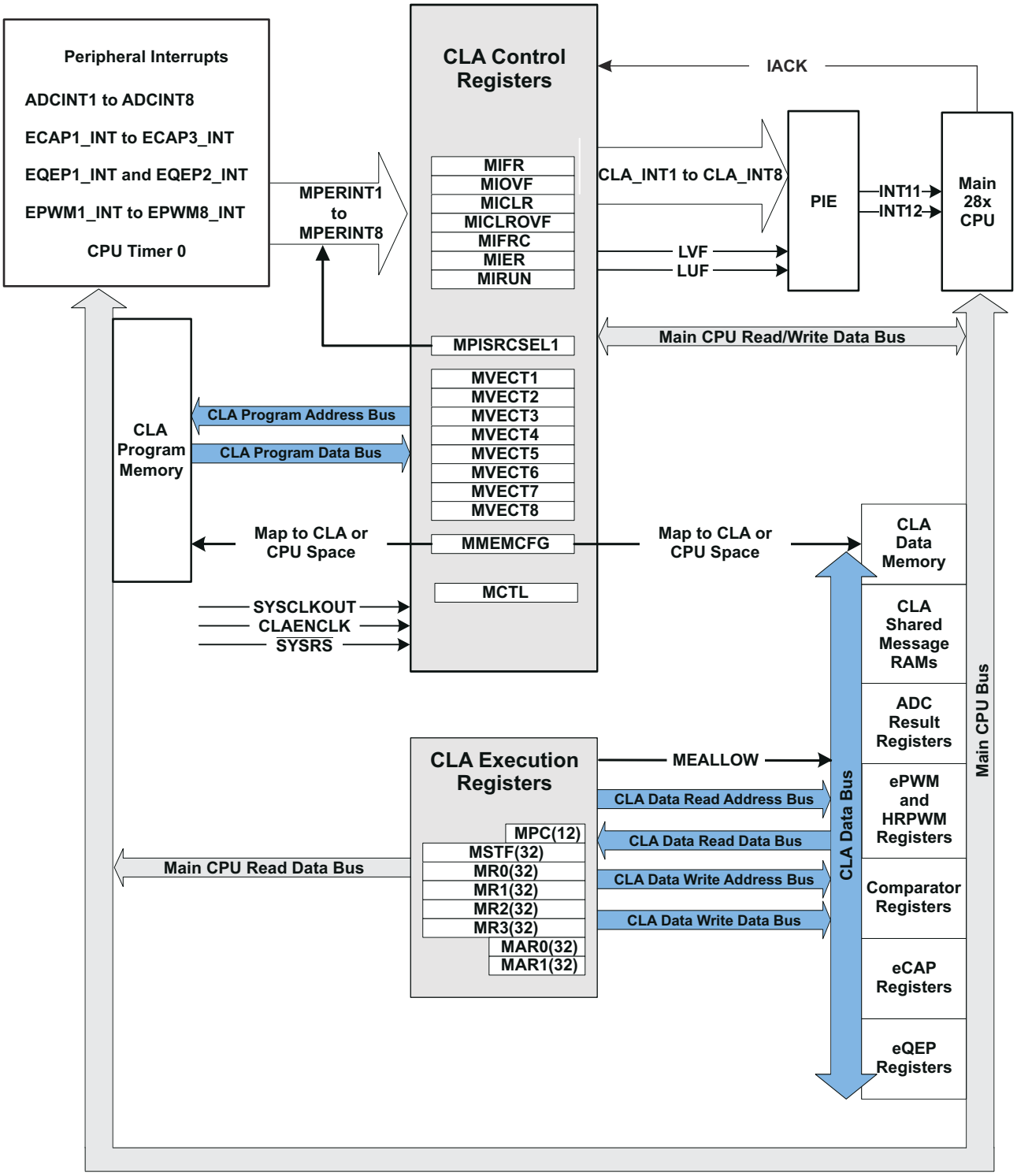

Figure 8-19. CLA Block Diagram

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Table 8-20. CLA Control Registers

REGISTER NAME	CLA1 ADDRESS	SIZE (×16)	EALLOW PROTECTED	DESCRIPTION(1)
MVECT1	0x1400	1	Yes	CLA Interrupt/Task 1 Start Address
MVECT2	0x1401	1	Yes	CLA Interrupt/Task 2 Start Address
MVECT3	0x1402	1	Yes	CLA Interrupt/Task 3 Start Address
MVECT4	0x1403	1	Yes	CLA Interrupt/Task 4 Start Address
MVECT5	0x1404	1	Yes	CLA Interrupt/Task 5 Start Address
MVECT6	0x1405	1	Yes	CLA Interrupt/Task 6 Start Address
MVECT7	0x1406	1	Yes	CLA Interrupt/Task 7 Start Address
MVECT8	0x1407	1	Yes	CLA Interrupt/Task 8 Start Address
MCTL	0x1410	1	Yes	CLA Control Register
MMEMCFG	0x1411	1	Yes	CLA Memory Configure Register
MPISRCSEL1	0x1414	2	Yes	Peripheral Interrupt Source Select Register 1
MIFR	0x1420	1	Yes	Interrupt Flag Register
MIOVF	0x1421	1	Yes	Interrupt Overflow Register
MIFRC	0x1422	1	Yes	Interrupt Force Register
MICLR	0x1423	1	Yes	Interrupt Clear Register
MICLROVF	0x1424	1	Yes	Interrupt Overflow Clear Register
MIER	0x1425	1	Yes	Interrupt Enable Register
MIRUN	0x1426	1	Yes	Interrupt RUN Register
MIPCTL	0x1427	1	Yes	Interrupt Priority Control Register
MPC(2)	0x1428	1	–	CLA Program Counter
MAR0(2)	0x142A	1	–	CLA Aux Register 0
MAR1(2)	0x142B	1	–	CLA Aux Register 1
MSTF(2)	0x142E	2	–	CLA STF Register
MR0(2)	0x1430	2	–	CLA R0H Register
MR1(2)	0x1434	2	–	CLA R1H Register
MR2(2)	0x1438	2	–	CLA R2H Register
MR3(2)	0x143C	2	–	CLA R3H Register

(1) All registers in this table are CSM-protected.
(2) The main C28x CPU has read-only access to this register for debug purposes. The main CPU cannot perform CPU or debugger writes to this register.

Table 8-21. CLA Message RAM

ADDRESS RANGE	SIZE (×16)	DESCRIPTION
0x1480 – 0x14FF	128	CLA to CPU Message RAM
0x1500 – 0x157F	128	CPU to CLA Message RAM

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8.9.2 Analog Block

A 12-bit ADC core is implemented that has different timings than the 12-bit ADC used on the F280x and F2833x devices. The ADC wrapper is modified to incorporate the new timings and also other enhancements to improve the timing control of start of conversions. Figure 8-20 shows the interaction of the analog module with the rest of the F2806x system.

80-Pin	100-Pin
VDDA	VDDA
VREFLO Tied To VSSA	VSSA
	VREFLO
VREFHI Tied To A0	VREFHI
	A0
A1	A1
A2	A2
	A3
A4	A4
A5	A5
A6	A6
	A7
B0	B0
B1	B1
B2	B2
	B3
B4	B4
B5	B5
B6	B6
	B7

Signal Pinout

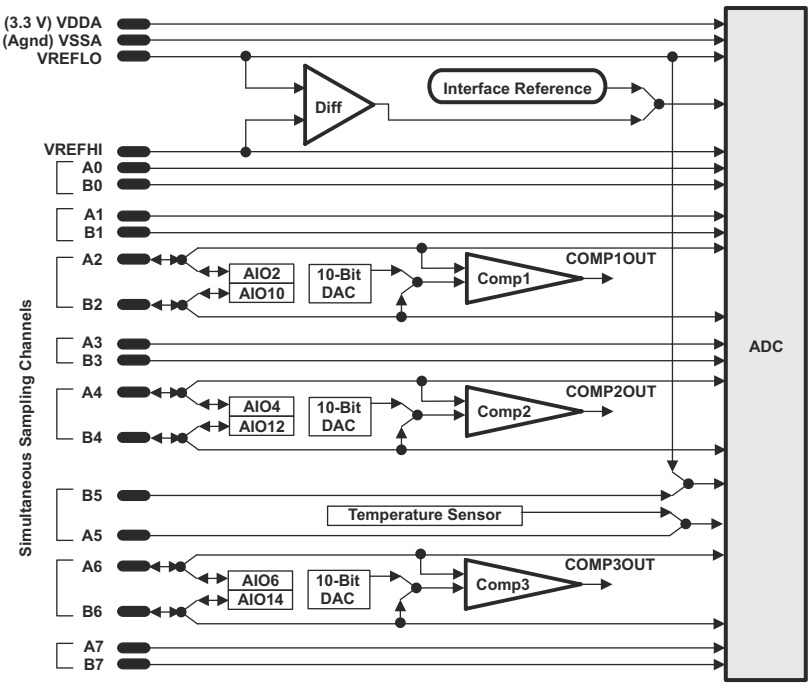

Figure 8-20. Analog Pin Configurations

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8.9.2.1 Analog-to-Digital Converter (ADC)

8.9.2.1.1 Features

The core of the ADC contains a single 12-bit converter fed by two sample-and-hold circuits. The sample-and-hold circuits can be sampled simultaneously or sequentially. These, in turn, are fed by a total of up to 16 analog input channels. The converter can be configured to run with an internal band-gap reference to create true-voltage based conversions or with a pair of external voltage references (V_{REFHI}/V_{REFLO}) to create ratiometric-based conversions.

Contrary to previous ADC types, this ADC is not sequencer-based. The user can easily create a series of conversions from a single trigger. However, the basic principle of operation is centered around the configurations of individual conversions, called SOCs, or Start-Of-Conversions.

Functions of the ADC module include:

- 12-bit ADC core with built-in dual sample-and-hold (S/H)
- Simultaneous sampling or sequential sampling modes
- Full range analog input: 0 V to 3.3 V fixed, or V_{REFHI}/V_{REFLO} ratiometric. The digital value of the input analog voltage is derived by:
  - Internal Reference ($V_{REFLO} = V_{SSA}$. V_{REFHI} must not exceed V_{DDA} when using either internal or external reference modes.)

$$\text{Digital Value} = 0, \quad \text{when input} \le 0\ \text{V}$$

$$\text{Digital Value} = 4096 \times \frac{\text{Input Analog Voltage} - V_{REFLO}}{3.3}, \quad \text{when } 0\ \text{V} < \text{input} < 3.3\ \text{V}$$

$$\text{Digital Value} = 4095, \quad \text{when input} \ge 3.3\ \text{V}$$

  - External Reference (V_{REFHI}/V_{REFLO} connected to external references. V_{REFHI} must not exceed V_{DDA} when using either internal or external reference modes.)

$$\text{Digital Value} = 0, \quad \text{when input} \le 0\ \text{V}$$

$$\text{Digital Value} = 4096 \times \frac{\text{Input Analog Voltage} - V_{REFLO}}{V_{REFHI} - V_{REFLO}}, \quad \text{when } 0\ \text{V} < \text{input} < V_{REFHI}$$

$$\text{Digital Value} = 4095, \quad \text{when input} \ge V_{REFHI}$$

- Up to 16-channel, multiplexed inputs
- 16 SOCs, configurable for trigger, sample window, and channel
- 16 result registers (individually addressable) to store conversion values
- Multiple trigger sources
  - S/W – software immediate start
  - ePWM 1–8
  - GPIO XINT2
  - CPU Timer 0, CPU Timer 1, CPU Timer 2
  - ADCINT1, ADCINT2
- 9 flexible PIE interrupts, can configure interrupt request after any conversion

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Table 8-22. ADC Configuration and Control Registers

REGISTER NAME	ADDRESS	SIZE (×16)	EALLOW PROTECTED	DESCRIPTION
ADCCTL1	0x7100	1	Yes	Control 1 Register
ADCCTL2	0x7101	1	Yes	Control 2 Register
ADCINTFLG	0x7104	1	No	Interrupt Flag Register
ADCINTFLGCLR	0x7105	1	No	Interrupt Flag Clear Register
ADCINTOVF	0x7106	1	No	Interrupt Overflow Register
ADCINTOVFCLR	0x7107	1	No	Interrupt Overflow Clear Register
INTSEL1N2	0x7108	1	Yes	Interrupt 1 and 2 Selection Register
INTSEL3N4	0x7109	1	Yes	Interrupt 3 and 4 Selection Register
INTSEL5N6	0x710A	1	Yes	Interrupt 5 and 6 Selection Register
INTSEL7N8	0x710B	1	Yes	Interrupt 7 and 8 Selection Register
INTSEL9N10	0x710C	1	Yes	Interrupt 9 Selection Register (reserved Interrupt 10 Selection)
SOCPRICTL	0x7110	1	Yes	SOC Priority Control Register
ADCSAMPLEMODE	0x7112	1	Yes	Sampling Mode Register
ADCINTSOCSEL1	0x7114	1	Yes	Interrupt SOC Selection 1 Register (for 8 channels)
ADCINTSOCSEL2	0x7115	1	Yes	Interrupt SOC Selection 2 Register (for 8 channels)
ADCSOCFLG1	0x7118	1	No	SOC Flag 1 Register (for 16 channels)
ADCSOCFRC1	0x711A	1	No	SOC Force 1 Register (for 16 channels)
ADCSOCOVF1	0x711C	1	No	SOC Overflow 1 Register (for 16 channels)
ADCSOCOVFCLR1	0x711E	1	No	SOC Overflow Clear 1 Register (for 16 channels)
ADCSOC0CTL to ADCSOC15CTL	0x7120 – 0x712F	1	Yes	SOC0 Control Register to SOC15 Control Register
ADCREFTRIM	0x7140	1	Yes	Reference Trim Register
ADCOFFTRIM	0x7141	1	Yes	Offset Trim Register
COMPHYSTCTL	0x714C	1	Yes	Comparator Hysteresis Control Register
ADCREV	0x714F	1	No	Revision Register

Table 8-23. ADC Result Registers (Mapped to PF0)

REGISTER NAME	ADDRESS	SIZE (×16)	EALLOW PROTECTED	DESCRIPTION
ADCRESULT0 to ADCRESULT15	0xB00 to 0xB0F	1	No	ADC Result 0 Register to ADC Result 15 Register

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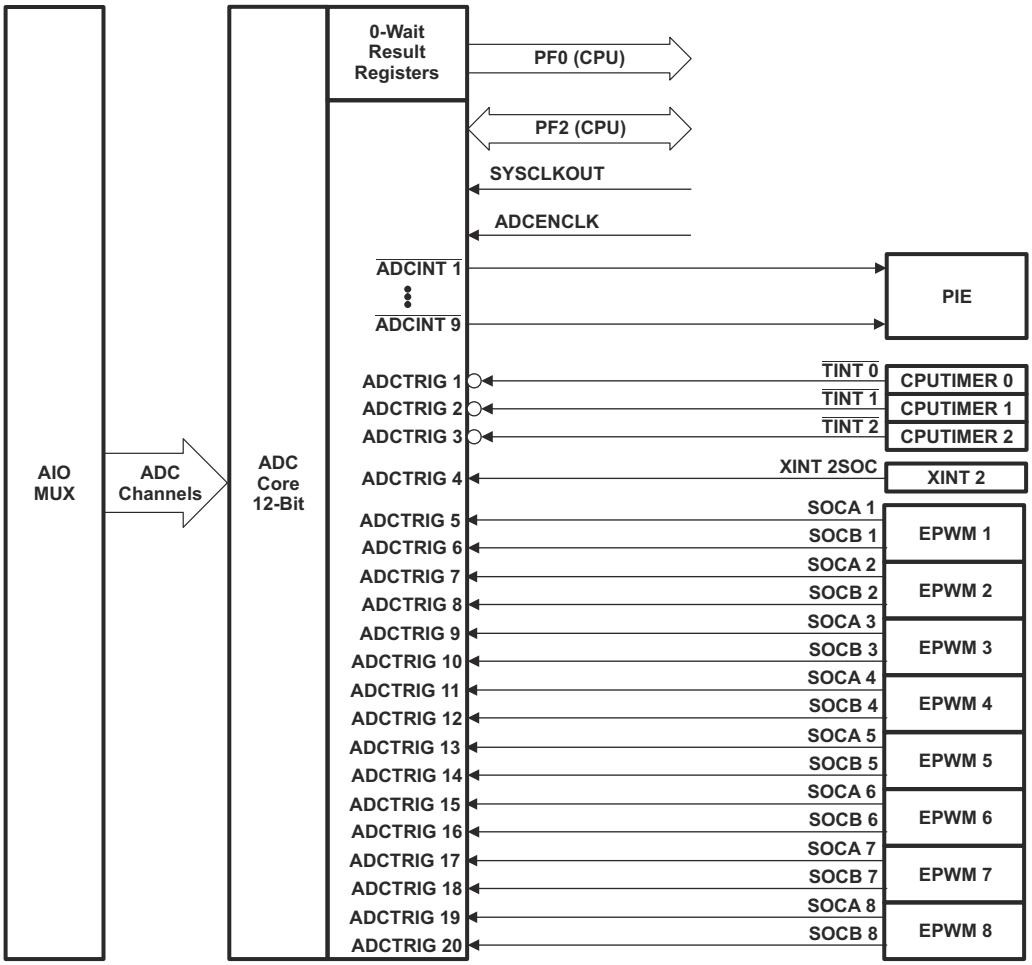

Figure 8-21. ADC Connections

ADC Connections if the ADC is Not Used

TI recommends keeping the connections for the analog power pins, even if the ADC is not used. Following is a summary of how the ADC pins should be connected, if the ADC is not used in an application:

- V_{DDA} – Connect to V_{DDIO}
- V_{SSA} – Connect to V_{SS}
- V_{REFLO} – Connect to V_{SS}
- ADCINAn, ADCINBn, V_{REFHI} – Connect to V_{SSA}

When the ADC module is used in an application, unused ADC input pins should be connected to analog ground (V_{SSA}).

Note

TI recommends that unused ADCIN pins which are multiplexed with AIO function be grounded through a 1-kΩ resistor. This recommendation is intended to prevent any inadvertent software activation of the AIO output logic-high driving directly to ground; this condition can cause permanent device damage by exceeding I_{OH} Absolute Maximum.

When the ADC is not used, be sure that the clock to the ADC module is not turned on to realize power savings.

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8.9.2.1.2 ADC Start-of-Conversion Electrical Data/Timing

8.9.2.1.2.1 External ADC Start-of-Conversion Switching Characteristics

over recommended operating conditions (unless otherwise noted)

PARAMETER		MIN	MAX	UNIT
$t_{w(ADCSOCL)}$	Pulse duration, $\overline{ADCSOCxO}$ low	$32t_{c(HCO)}$		cycles

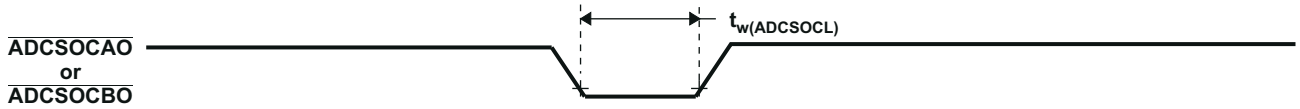

Figure 8-22. $\overline{ADCSOCAO}$ or $\overline{ADCSOCBO}$ Timing

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8.9.2.1.3 On-Chip Analog-to-Digital Converter (ADC) Electrical Data/Timing

8.9.2.1.3.1 ADC Electrical Characteristics

PARAMETER		MIN	TYP	MAX	UNIT
DC SPECIFICATIONS					
Resolution		12			Bits
ADC clock	90-MHz device	0.001		45	MHz
Sample Window		7		64	ADC Clocks
ACCURACY					
INL (Integral nonlinearity)(1)		–4		4	LSB
DNL (Differential nonlinearity), no missing codes		–1		1.5	LSB
Offset error (2)	Executing a single self-recalibration(3)	–20		20	LSB
	Executing periodic self-recalibration(4)	–4		4	
Overall gain error with internal reference		–60		60	LSB
Overall gain error with external reference		–40		40	LSB
Channel-to-channel offset variation		–4		4	LSB
Channel-to-channel gain variation		–4		4	LSB
ADC temperature coefficient with internal reference			–50		ppm/°C
ADC temperature coefficient with external reference			–20		ppm/°C
V_{REFLO}			–100		µA
V_{REFHI}			100		µA
ANALOG INPUT					
Analog input voltage with internal reference		0		3.3	V
Analog input voltage with external reference		V_{REFLO}		V_{REFHI}	V
V_{REFLO} input voltage(5)		V_{SSA}		0.66	V
V_{REFHI} input voltage(6)		2.64		V_{DDA}	V
	with $V_{REFLO} = V_{SSA}$	1.98		V_{DDA}	
Input capacitance			5		pF
Input leakage current			±2		µA

(1) INL will degrade when the ADC input voltage goes above V_{DDA}.
(2) 1 LSB has the weighted value of full-scale range (FSR)/4096. FSR is 3.3 V with internal reference and V_{REFHI} - V_{REFLO} for external reference.
(3) For more details, see the *TMS320F2806x MCUs Silicon Errata*.
(4) Periodic self-recalibration will remove system-level and temperature dependencies on the ADC zero offset error.
(5) V_{REFLO} is always connected to V_{SSA} on the 80-pin PN and PFP devices.
(6) V_{REFHI} must not exceed V_{DDA} when using either internal or external reference modes. Because V_{REFHI} is tied to ADCINA0 on the 80-pin PN and PFP devices, the input signal on ADCINA0 must not exceed V_{DDA}.

8.9.2.1.3.2 ADC Power Modes

ADC OPERATING MODE	CONDITIONS	I_{DDA}	UNIT
Mode A – Operating Mode	ADC Clock Enabled Band gap On (ADCBGPWD = 1) Reference On (ADCREFPWD = 1) ADC Powered Up (ADCPWDN = 1)	16	mA
Mode B – Quick Wake Mode	ADC Clock Enabled Band gap On (ADCBGPWD = 1) Reference On (ADCREFPWD = 1) ADC Powered Up (ADCPWDN = 0)	4	mA

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ADC OPERATING MODE	CONDITIONS	I_{DDA}	UNIT
Mode C – Comparator-Only Mode	ADC Clock Enabled Band gap On (ADCBGPWD = 1) Reference On (ADCREFPWD = 0) ADC Powered Up (ADCPWDN = 0)	1.5	mA
Mode D – Off Mode	ADC Clock Enabled Band gap On (ADCBGPWD = 0) Reference On (ADCREFPWD = 0) ADC Powered Up (ADCPWDN = 0)	0.075	mA

8.9.2.1.3.3 Internal Temperature Sensor

8.9.2.1.3.3.1 Temperature Sensor Coefficient

PARAMETER(1)		MIN	TYP	MAX	UNIT
T_{SLOPE}	Degrees C of temperature movement per measured ADC LSB change of the temperature sensor		0.18(3) (2)		°C/LSB
T_{OFFSET}	ADC output at 0°C of the temperature sensor		1750		LSB

(1) The temperature sensor slope and offset are given in terms of ADC LSBs using the internal reference of the ADC. Values must be adjusted accordingly in external reference mode to the external reference voltage.
(2) Output of the temperature sensor (in terms of LSBs) is sign-consistent with the direction of the temperature movement. Increasing temperatures will give increasing ADC values relative to an initial value; decreasing temperatures will give decreasing ADC values relative to an initial value.
(3) ADC temperature coeffieicient is accounted for in this specification

8.9.2.1.3.4 ADC Power-Up Control Bit Timing

8.9.2.1.3.4.1 ADC Power-Up Delays

PARAMETER(1)		MIN	MAX	UNIT
$t_{d(PWD)}$	Delay time for the ADC to be stable after power up		1	ms

(1) Timings maintain compatibility to the ADC module. The 2806x ADC supports driving all 3 bits at the same time $t_{d(PWD)}$ ms before first conversion.

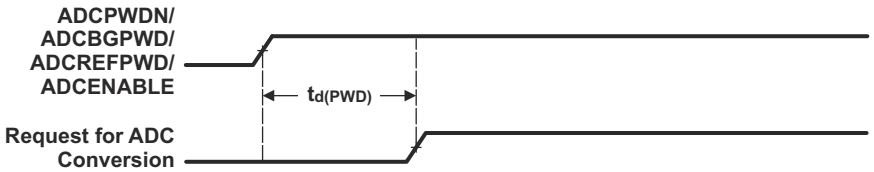

Figure 8-23. ADC Conversion Timing

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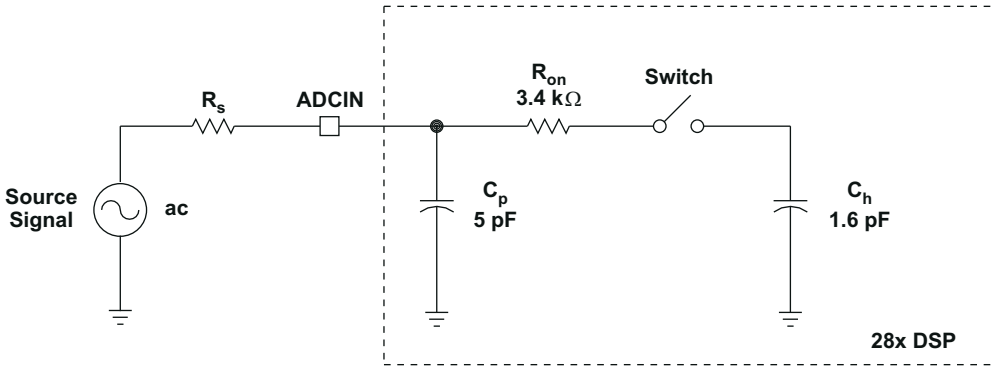

Typical Values of the Input Circuit Components:

Switch Resistance (R_{on}): 3.4 kΩ
Sampling Capacitor (C_h): 1.6 pF
Parasitic Capacitance (C_p): 5 pF
Source Resistance (R_s): 50 Ω

Figure 8-24. ADC Input Impedance Model

8.9.2.1.3.5 ADC Sequential and Simultaneous Timings

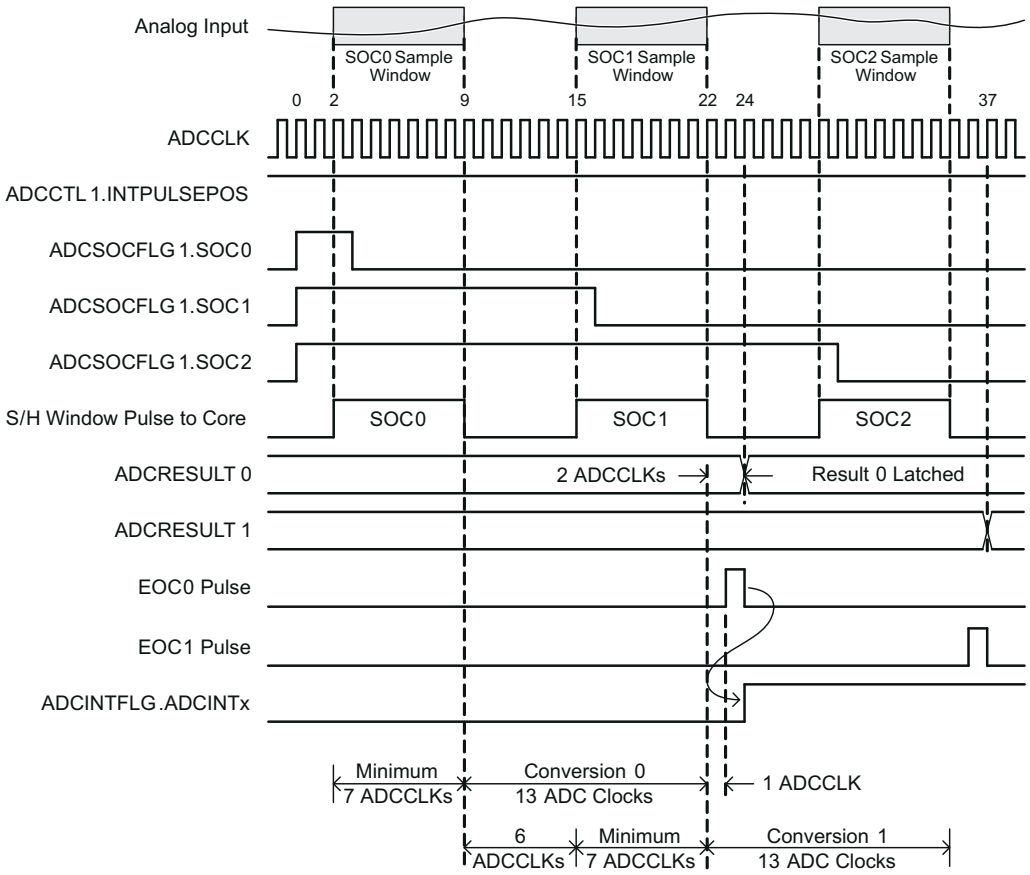

Figure 8-25. Timing Example for Sequential Mode / Late Interrupt Pulse

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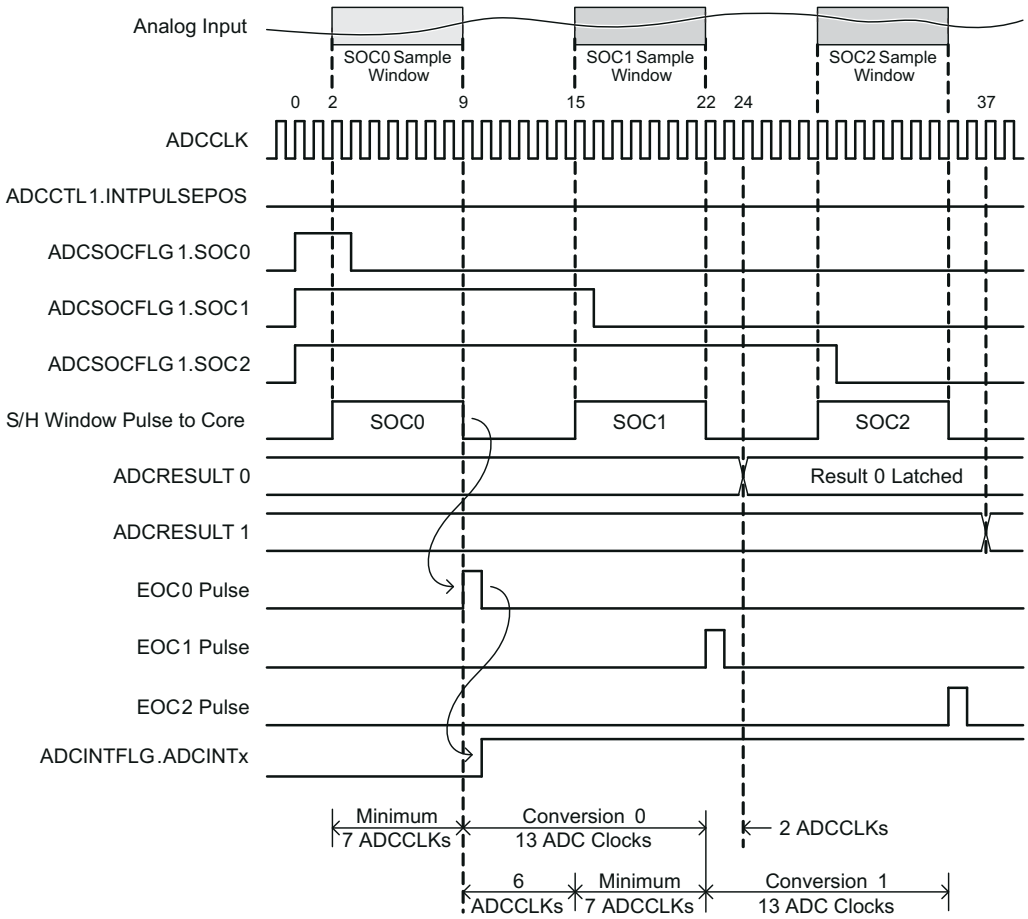

Figure 8-26. Timing Example for Sequential Mode / Early Interrupt Pulse

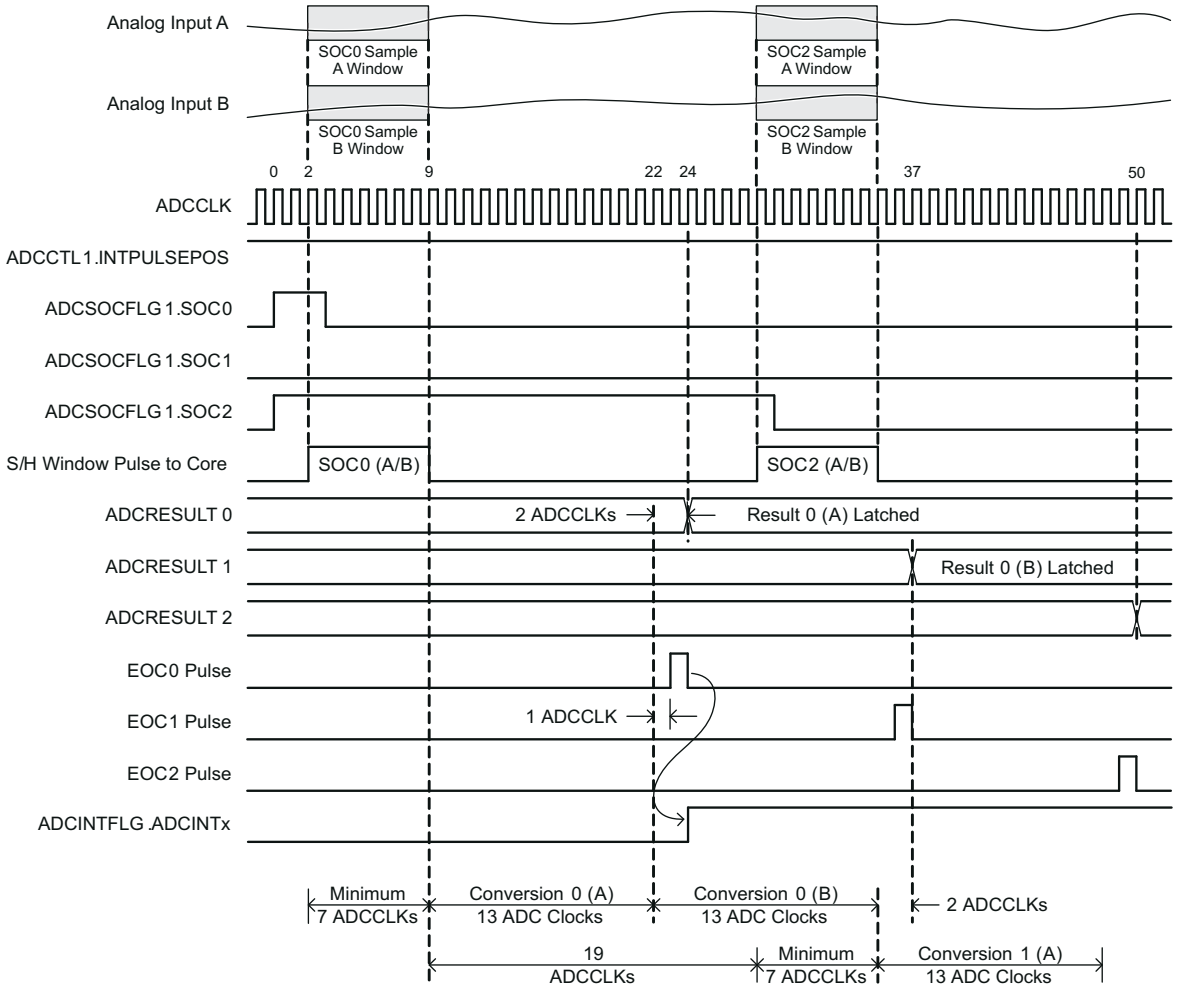

Figure 8-27. Timing Example for Simultaneous Mode / Late Interrupt Pulse

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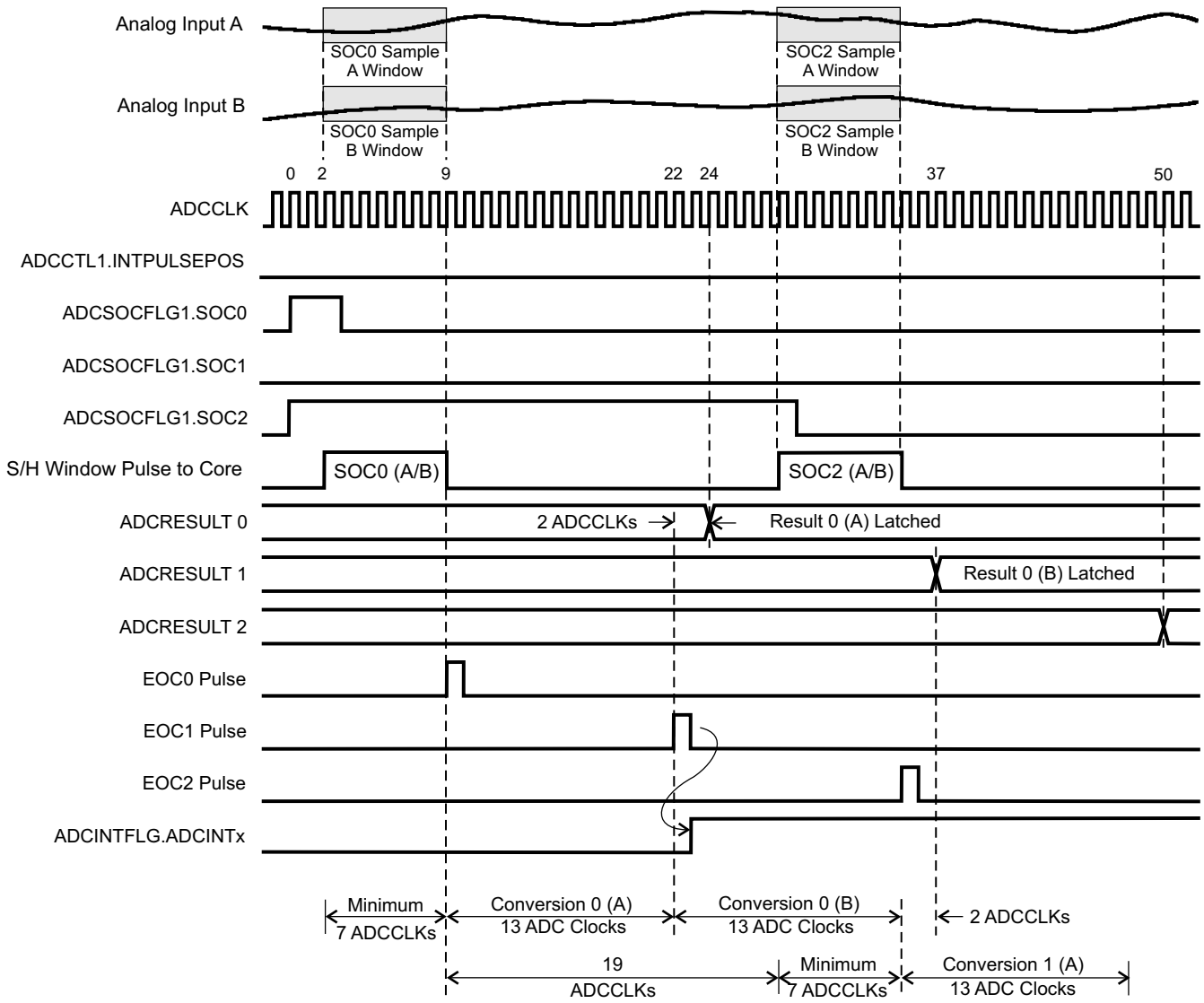

Figure 8-28. Timing Example for Simultaneous Mode / Early Interrupt Pulse

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8.9.2.2 ADC MUX

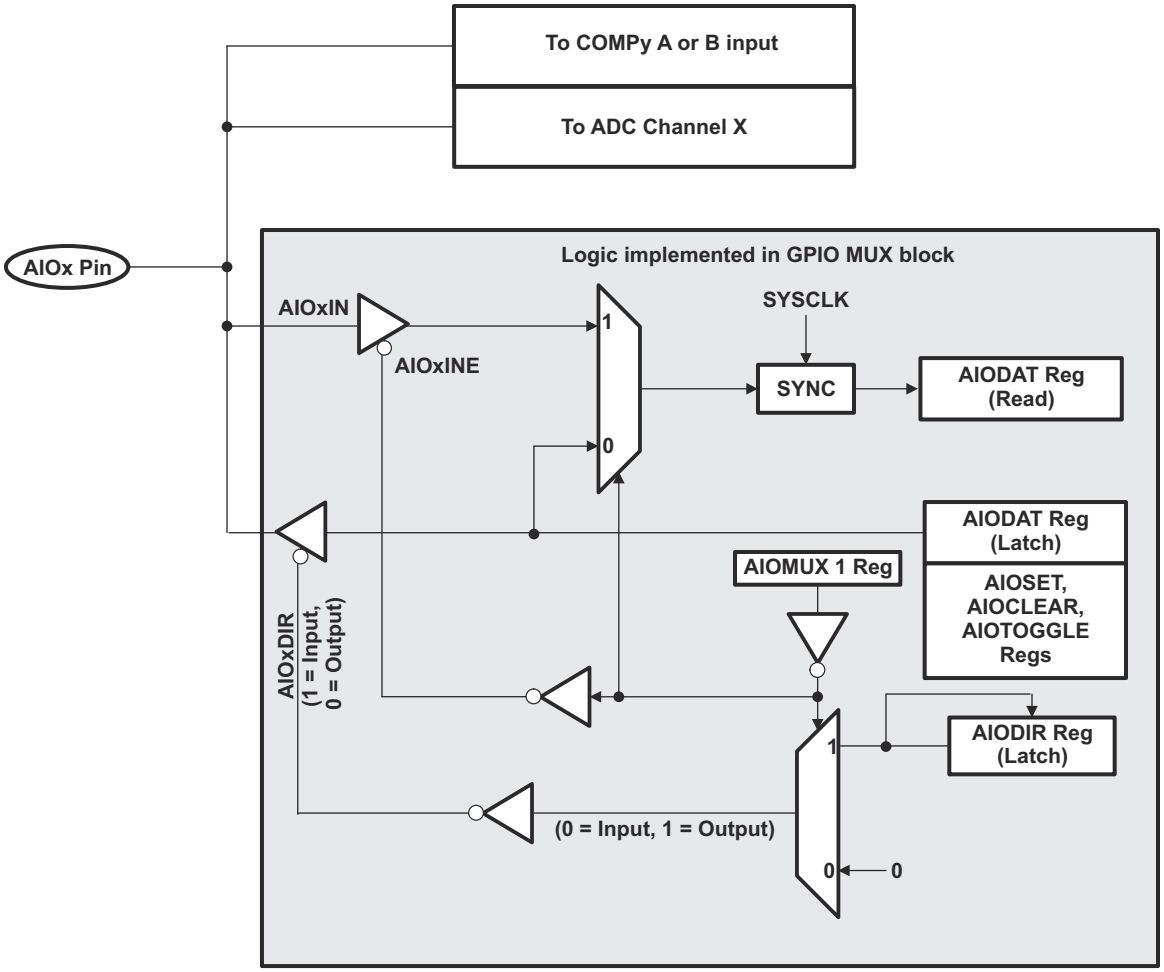

Figure 8-29. AIOx Pin Multiplexing

The ADC channel and Comparator functions are always available. The digital I/O function is available only when the respective bit in the AIOMUX1 register is 0. In this mode, reading the AIODAT register reflects the actual pin state.

The digital I/O function is disabled when the respective bit in the AIOMUX1 register is 1. In this mode, reading the AIODAT register reflects the output latch of the AIODAT register and the input digital I/O buffer is disabled to prevent analog signals from generating noise.

On reset, the digital function is disabled. If the pin is used as an analog input, users should keep the AIO function disabled for that pin.

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8.9.2.3 Comparator Block

Figure 8-30 shows the interaction of the Comparator modules with the rest of the system.

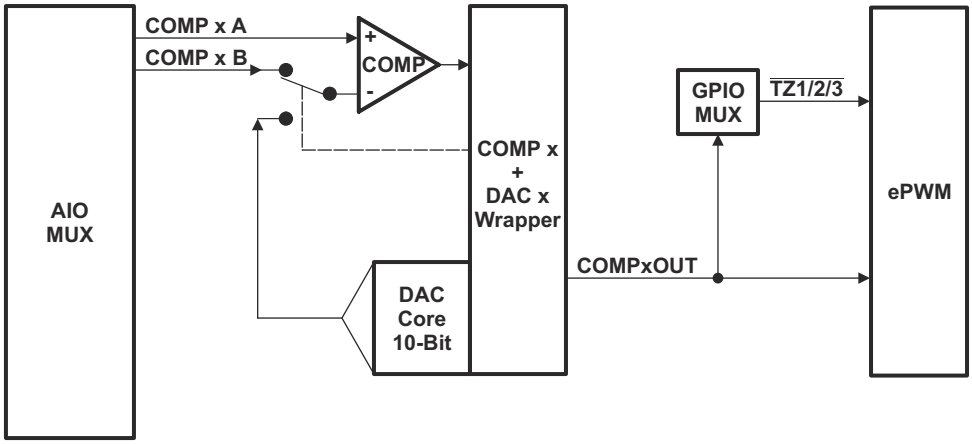

Figure 8-30. Comparator Block Diagram

Table 8-24. Comparator Control Registers

REGISTER NAME	COMP1 ADDRESS	COMP2 ADDRESS	COMP3 ADDRESS	SIZE (×16)	EALLOW PROTECTED	DESCRIPTION
COMPCTL	0x6400	0x6420	0x6440	1	Yes	Comparator Control Register
COMPSTS	0x6402	0x6422	0x6442	1	No	Comparator Status Register
DACCTL	0x6404	0x6424	0x6444	1	Yes	DAC Control Register
DACVAL	0x6406	0x6426	0x6446	1	No	DAC Value Register
RAMPMAXREF_ ACTIVE	0x6408	0x6428	0x6448	1	No	Ramp Generator Maximum Reference (Active) Register
RAMPMAXREF_ SHDW	0x640A	0x642A	0x644A	1	No	Ramp Generator Maximum Reference (Shadow) Register
RAMPDECVAL_ ACTIVE	0x640C	0x642C	0x644C	1	No	Ramp Generator Decrement Value (Active) Register
RAMPDECVAL_ SHDW	0x640E	0x642E	0x644E	1	No	Ramp Generator Decrement Value (Shadow) Register
RAMPSTS	0x6410	0x6430	0x6450	1	No	Ramp Generator Status Register

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8.9.2.3.1 On-Chip Comparator/DAC Electrical Data/Timing

8.9.2.3.1.1 Electrical Characteristics of the Comparator/DAC

CHARACTERISTIC	MIN	TYP	MAX	UNIT
Comparator				
Comparator Input Range		$V_{SSA} – V_{DDA}$		V
Comparator response time to PWM Trip Zone (Async)		30		ns
Input Offset		±5		mV
Input Hysteresis(1)		35		mV
DAC				
DAC Output Range		$V_{SSA} – V_{DDA}$		V
DAC resolution		10		bits
DAC settling time		See Figure 8-31.		
DAC Gain		–1.5%		
DAC Offset		10		mV
Monotonic		Yes		
INL		±3		LSB

(1) Hysteresis on the comparator inputs is achieved with a Schmidt trigger configuration. This results in an effective 100-kΩ feedback resistance between the output of the comparator and the non-inverting input of the comparator.

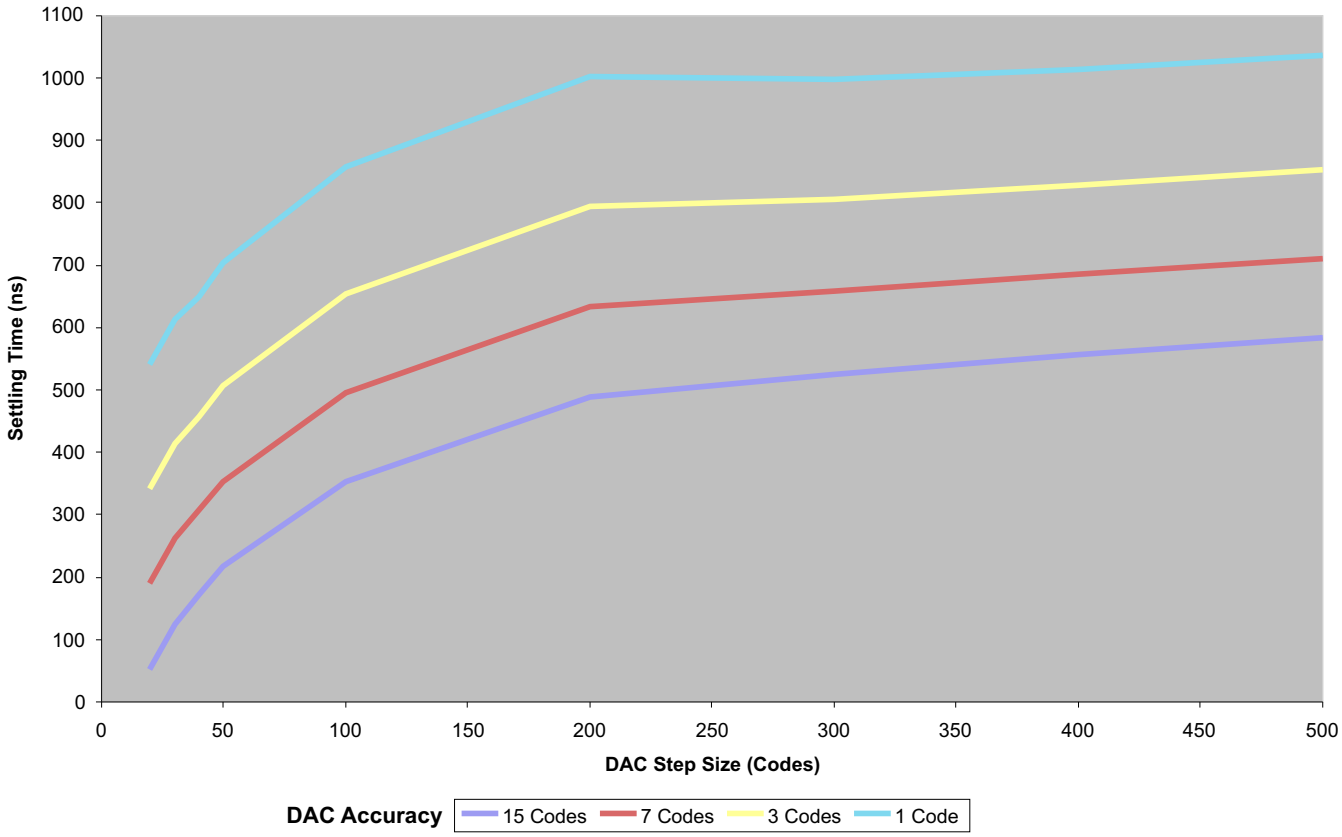

Figure 8-31. DAC Settling Time

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8.9.3 Detailed Descriptions

Integral Nonlinearity

Integral nonlinearity refers to the deviation of each individual code from a line drawn from zero to full scale. The point used as zero occurs one-half LSB before the first code transition. The full-scale point is defined as level one-half LSB beyond the last code transition. The deviation is measured from the center of each particular code to the true straight line between these two points.

Differential Nonlinearity

An ideal ADC exhibits code transitions that are exactly 1 LSB apart. DNL is the deviation from this ideal value. A differential nonlinearity error of less than ±1 LSB ensures no missing codes.

Zero Offset

The major carry transition should occur when the analog input is at zero volts. Zero error is defined as the deviation of the actual transition from that point.

Gain Error

The first code transition should occur at an analog value one-half LSB above negative full scale. The last transition should occur at an analog value one and one-half LSB below the nominal full scale. Gain error is the deviation of the actual difference between first and last code transitions and the ideal difference between first and last code transitions.

Signal-to-Noise Ratio + Distortion (SINAD)

SINAD is the ratio of the rms value of the measured input signal to the rms sum of all other spectral components below the Nyquist frequency, including harmonics but excluding DC. The value for SINAD is expressed in decibels.

Effective Number of Bits (ENOB)

For a sine wave, SINAD can be expressed in terms of the number of bits. Using the following formula, $N = \frac{(SINAD - 1.76)}{6.02}$ it is possible to get a measure of performance expressed as N, the effective number of bits. Thus, effective number of bits for a device for sine wave inputs at a given input frequency can be calculated directly from its measured SINAD.

Total Harmonic Distortion (THD)

THD is the ratio of the rms sum of the first nine harmonic components to the rms value of the measured input signal and is expressed as a percentage or in decibels.

Spurious Free Dynamic Range (SFDR)

SFDR is the difference in dB between the rms amplitude of the input signal and the peak spurious signal.

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8.9.4 Serial Peripheral Interface (SPI) Module

The device includes the 4-pin serial peripheral interface (SPI) module. Up to two SPI modules are available. The SPI is a high-speed, synchronous serial I/O port that allows a serial bit stream of programmed length (1 to 16 bits) to be shifted into and out of the device at a programmable bit-transfer rate. Normally, the SPI is used for communications between the MCU and external peripherals or another processor. Typical applications include external I/O or peripheral expansion through devices such as shift registers, display drivers, and ADCs. Multidevice communications are supported by the master/slave operation of the SPI.

The SPI module features include:

- Four external pins:
  - SPISOMI: SPI slave-output/master-input pin
  - SPISIMO: SPI slave-input/master-output pin
  - $\overline{\text{SPISTE}}$: SPI slave transmit-enable pin
  - SPICLK: SPI serial-clock pin

Note

All four pins can be used as GPIO if the SPI module is not used.

- Two operational modes: master and slave

  Baud rate: 125 different programmable rates.

$$\text{Baud rate} = \frac{\text{LSPCLK}}{(\text{SPIBRR} + 1)} \qquad \text{when SPIBRR} = 3 \text{ to } 127$$

$$\text{Baud rate} = \frac{\text{LSPCLK}}{4} \qquad \text{when SPIBRR} = 0, 1, 2$$

- Data word length: 1 to 16 data bits
- Four clocking schemes (controlled by clock polarity and clock phase bits) include:
  - Falling edge without phase delay: SPICLK active-high. SPI transmits data on the falling edge of the SPICLK signal and receives data on the rising edge of the SPICLK signal.
  - Falling edge with phase delay: SPICLK active-high. SPI transmits data one half-cycle ahead of the falling edge of the SPICLK signal and receives data on the falling edge of the SPICLK signal.
  - Rising edge without phase delay: SPICLK inactive-low. SPI transmits data on the rising edge of the SPICLK signal and receives data on the falling edge of the SPICLK signal.
  - Rising edge with phase delay: SPICLK inactive-low. SPI transmits data one half-cycle ahead of the rising edge of the SPICLK signal and receives data on the rising edge of the SPICLK signal.
- Simultaneous receive and transmit operation (transmit function can be disabled in software)
- Transmitter and receiver operations are accomplished through either interrupt-driven or polled algorithms.
- Nine SPI module control registers: In control register frame beginning at address 7040h.

Note

All registers in this module are 16-bit registers that are connected to Peripheral Frame 2. When a register is accessed, the register data is in the lower byte (7–0), and the upper byte (15–8) is read as zeros. Writing to the upper byte has no effect.

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Enhanced feature:

- 4-level transmit/receive FIFO
- Delayed transmit control
- Bidirectional 3 wire SPI mode support
- Audio data receive support through $\overline{\text{SPISTE}}$ inversion

The SPI port operation is configured and controlled by the registers listed in Table 8-25 and Table 8-26.

Table 8-25. SPI-A Registers

NAME	ADDRESS	SIZE (×16)	EALLOW PROTECTED	DESCRIPTION(1)
SPICCR	0x7040	1	No	SPI-A Configuration Control Register
SPICTL	0x7041	1	No	SPI-A Operation Control Register
SPISTS	0x7042	1	No	SPI-A Status Register
SPIBRR	0x7044	1	No	SPI-A Baud Rate Register
SPIRXEMU	0x7046	1	No	SPI-A Receive Debug Buffer Register
SPIRXBUF	0x7047	1	No	SPI-A Serial Input Buffer Register
SPITXBUF	0x7048	1	No	SPI-A Serial Output Buffer Register
SPIDAT	0x7049	1	No	SPI-A Serial Data Register
SPIFFTX	0x704A	1	No	SPI-A FIFO Transmit Register
SPIFFRX	0x704B	1	No	SPI-A FIFO Receive Register
SPIFFCT	0x704C	1	No	SPI-A FIFO Control Register
SPIPRI	0x704F	1	No	SPI-A Priority Control Register

(1) Registers in this table are mapped to Peripheral Frame 2. This space only allows 16-bit accesses. 32-bit accesses produce undefined results.

Table 8-26. SPI-B Registers

NAME	ADDRESS	SIZE (×16)	EALLOW PROTECTED	DESCRIPTION(1)
SPICCR	0x7740	1	No	SPI-B Configuration Control Register
SPICTL	0x7741	1	No	SPI-B Operation Control Register
SPISTS	0x7742	1	No	SPI-B Status Register
SPIBRR	0x7744	1	No	SPI-B Baud Rate Register
SPIRXEMU	0x7746	1	No	SPI-B Receive Debug Buffer Register
SPIRXBUF	0x7747	1	No	SPI-B Serial Input Buffer Register
SPITXBUF	0x7748	1	No	SPI-B Serial Output Buffer Register
SPIDAT	0x7749	1	No	SPI-B Serial Data Register
SPIFFTX	0x774A	1	No	SPI-B FIFO Transmit Register
SPIFFRX	0x774B	1	No	SPI-B FIFO Receive Register
SPIFFCT	0x774C	1	No	SPI-B FIFO Control Register
SPIPRI	0x774F	1	No	SPI-B Priority Control Register

(1) Registers in this table are mapped to Peripheral Frame 2. This space only allows 16-bit accesses. 32-bit accesses produce undefined results.

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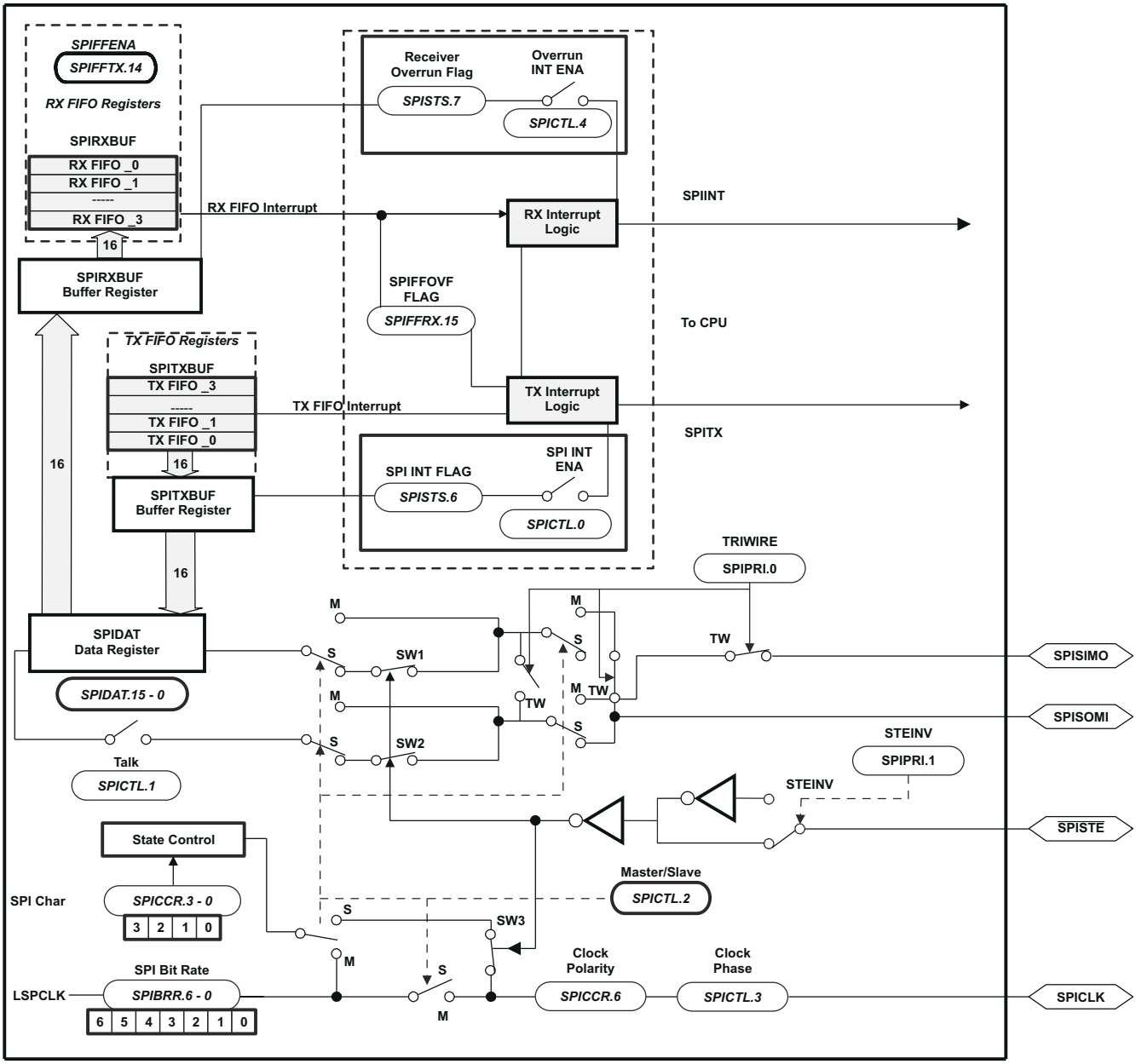
Figure 8-32 is a block diagram of the SPI in slave mode.



A. $\overline{\text{SPISTE}}$ is driven low by the master for a slave device.

Figure 8-32. SPI Module Block Diagram (Slave Mode)

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8.9.4.1 SPI Master Mode Electrical Data/Timing

Section 8.9.4.1.1 lists the master mode timing (clock phase = 0) and Section 8.9.4.1.2 lists the master mode timing (clock phase = 1). Figure 8-33 and Figure 8-34 show the timing waveforms.

8.9.4.1.1 SPI Master Mode External Timing (Clock Phase = 0)

NO.	PARAMETER(1) (2) (3) (4) (5)		BRR EVEN		BRR ODD		UNIT
			MIN	MAX	MIN	MAX	
1	$t_{c(SPC)M}$	Cycle time, SPICLK	$4t_{c(LSPCLK)}$	$128t_{c(LSPCLK)}$	$5t_{c(LSPCLK)}$	$127t_{c(LSPCLK)}$	ns
2	$t_{w(SPC1)M}$	Pulse duration, SPICLK first pulse	$0.5t_{c(SPC)M} - 10$	$0.5t_{c(SPC)M} + 10$	$0.5t_{c(SPC)M} + 0.5t_{c(LSPCLK)} - 10$	$0.5t_{c(SPC)M} + 0.5t_{c(LSPCLK)} + 10$	ns
3	$t_{w(SPC2)M}$	Pulse duration, SPICLK second pulse	$0.5t_{c(SPC)M} - 10$	$0.5t_{c(SPC)M} + 10$	$0.5t_{c(SPC)M} - 0.5t_{c(LSPCLK)} - 10$	$0.5t_{c(SPC)M} - 0.5t_{c(LSPCLK)} + 10$	ns
4	$t_{d(SIMO)M}$	Delay time, SPICLK to SPISIMO valid		10		10	ns
5	$t_{v(SIMO)M}$	Valid time, SPISIMO valid after SPICLK	$0.5t_{c(SPC)M} - 10$		$0.5t_{c(SPC)M} - 0.5t_{c(LSPCLK)} - 10$		ns
8	$t_{su(SOMI)M}$	Setup time, SPISOMI before SPICLK	26		26		ns
9	$t_{h(SOMI)M}$	Hold time, SPISOMI valid after SPICLK	0		0		ns
23	$t_{d(SPC)M}$	Delay time, $\overline{\text{SPISTE}}$ active to SPICLK	$1.5t_{c(SPC)M} - 3t_{c(SYSCLK)} - 10$		$1.5t_{c(SPC)M} - 3t_{c(SYSCLK)} - 10$		ns
24	$t_{d(STE)M}$	Delay time, SPICLK to $\overline{\text{SPISTE}}$ inactive	$0.5t_{c(SPC)M} - 10$		$0.5t_{c(SPC)M} - 0.5t_{c(LSPCLK)} - 10$		ns

(1) The MASTER / SLAVE bit (SPICTL.2) is set and the CLOCK PHASE bit (SPICTL.3) is cleared.
(2) $t_{c(SPC)}$ = SPI clock cycle time = LSPCLK/4 or LSPCLK/(SPIBRR +1)
(3) $t_{c(LCO)}$ = LSPCLK cycle time
(4) Internal clock prescalers must be adjusted such that the SPI clock speed is limited to the following SPI clock rate:
Master mode transmit 25-MHz MAX, master mode receive 12.5-MHz MAX
Slave mode transmit 12.5-MAX, slave mode receive 12.5-MHz MAX.
(5) The active edge of the SPICLK signal referenced is controlled by the clock polarity bit (SPICCR.6).

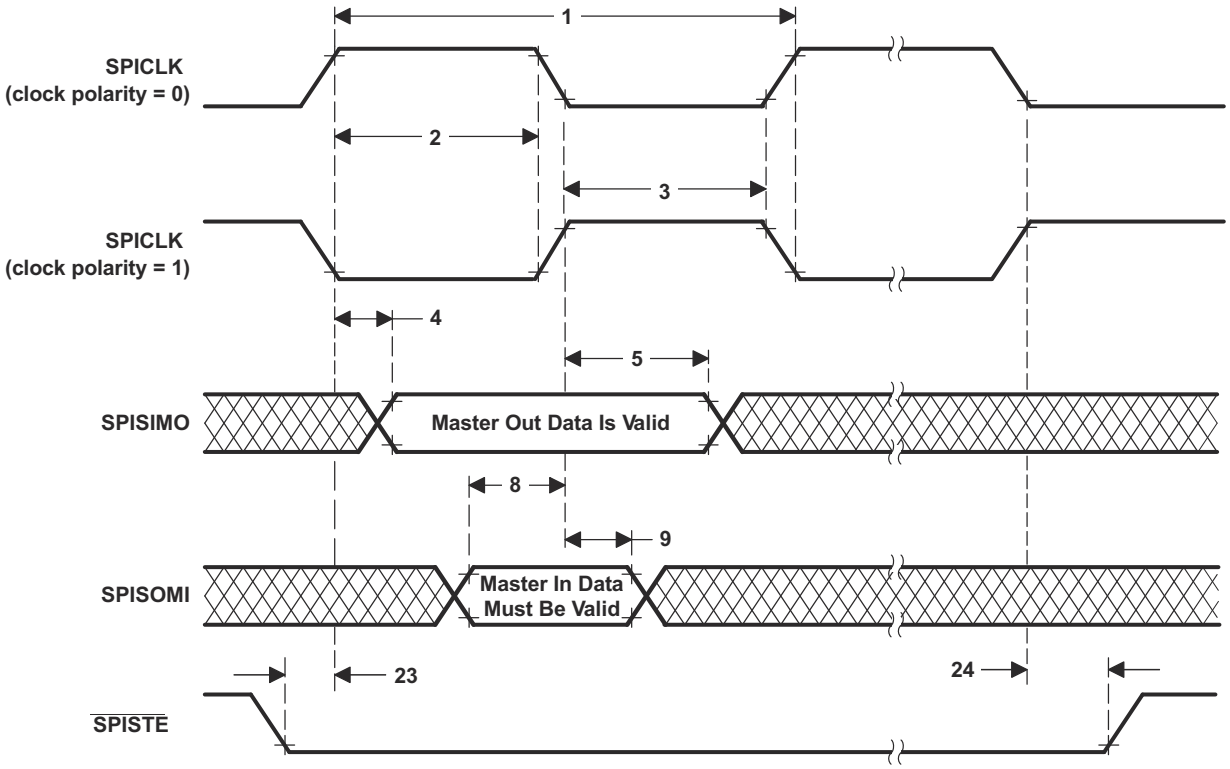

Figure 8-33. SPI Master Mode External Timing (Clock Phase = 0)

8.9.4.1.2 SPI Master Mode External Timing (Clock Phase = 1)

NO.	PARAMETER(1) (2) (3) (4) (5)		BRR EVEN		BRR ODD		UNIT
			MIN	MAX	MIN	MAX	
1	$t_{c(SPC)M}$	Cycle time, SPICLK	$4t_{c(LSPCLK)}$	$128t_{c(LSPCLK)}$	$5t_{c(LSPCLK)}$	$127t_{c(LSPCLK)}$	ns
2	$t_{w(SPC1)M}$	Pulse duration, SPICLK first pulse	$0.5t_{c(SPC)M} - 10$	$0.5t_{c(SPC)M} + 10$	$0.5t_{c(SPC)M} - 0.5t_{c(LSPCLK)} - 10$	$0.5t_{c(SPC)M} - 0.5t_{c(LSPCLK)} + 10$	ns
3	$t_{w(SPC2)M}$	Pulse duration, SPICLK second pulse	$0.5t_{c(SPC)M} - 10$	$0.5t_{c(SPC)M} + 10$	$0.5t_{c(SPC)M} + 0.5t_{c(LSPCLK)} - 10$	$0.5t_{c(SPC)M} + 0.5t_{c(LSPCLK)} + 10$	ns
6	$t_{d(SIMO)M}$	Delay time, SPISIMO valid to SPICLK	$0.5t_{c(SPC)M} - 10$		$0.5t_{c(SPC)M} + 0.5t_{c(LSPCLK)} - 10$		ns
7	$t_{v(SIMO)M}$	Valid time, SPISIMO valid after SPICLK	$0.5t_{c(SPC)M} - 10$		$0.5t_{c(SPC)M} - 0.5t_{c(LSPCLK)} - 10$		ns
10	$t_{su(SOMI)M}$	Setup time, SPISOMI before SPICLK	26		26		ns
11	$t_{h(SOMI)M}$	Hold time, SPISOMI valid after SPICLK	0		0		ns
23	$t_{d(SPC)M}$	Delay time, $\overline{\text{SPISTE}}$ active to SPICLK	$2t_{c(SPC)M} - 3t_{c(SYSCLK)} - 10$		$2t_{c(SPC)M} - 3t_{c(SYSCLK)} - 10$		ns
24	$t_{d(STE)M}$	Delay time, SPICLK to $\overline{\text{SPISTE}}$ inactive	$0.5t_{c(SPC)} - 10$		$0.5t_{c(SPC)} - 0.5t_{c(LSPCLK)} - 10$		ns

(1) The MASTER/SLAVE bit (SPICTL.2) is set and the CLOCK PHASE bit (SPICTL.3) is set.
(2) $t_{c(SPC)}$ = SPI clock cycle time = LSPCLK/4 or LSPCLK/(SPIBRR + 1)
(3) Internal clock prescalers must be adjusted such that the SPI clock speed is limited to the following SPI clock rate:
Master mode transmit 25 MHz MAX, master mode receive 12.5 MHz MAX
Slave mode transmit 12.5 MHz MAX, slave mode receive 12.5 MHz MAX.
(4) $t_{c(LCO)}$ = LSPCLK cycle time
(5) The active edge of the SPICLK signal referenced is controlled by the CLOCK POLARITY bit (SPICCR.6).

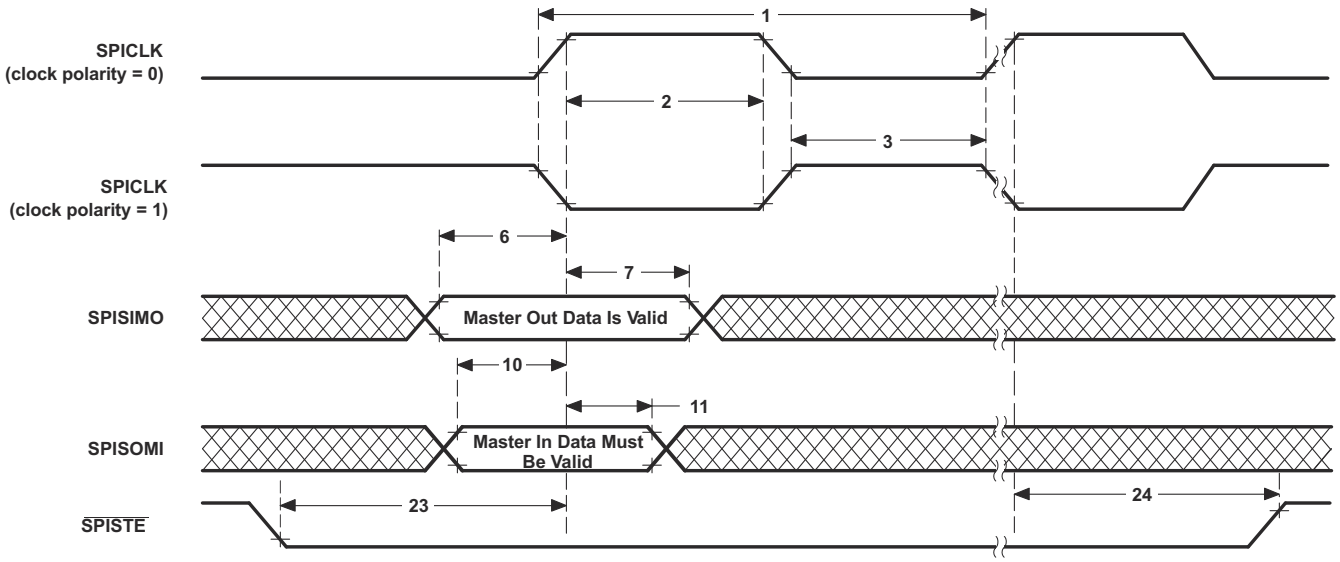

Figure 8-34. SPI Master Mode External Timing (Clock Phase = 1)

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8.9.4.2 SPI Slave Mode Electrical Data/Timing

Section 8.9.4.2.1 lists the slave mode timing (clock phase = 0) and Section 8.9.4.2.2 lists the slave mode timing (clock phase = 1). Figure 8-35 and Figure 8-36 show the timing waveforms.

8.9.4.2.1 SPI Slave Mode External Timing (Clock Phase = 0)

NO.	PARAMETER(1) (2) (4) (3) (5)		MIN	MAX	UNIT
12	$t_{c(SPC)S}$	Cycle time, SPICLK	$4t_{c(SYSCLK)}$		ns
13	$t_{w(SPC1)S}$	Pulse duration, SPICLK first pulse	$2t_{c(SYSCLK)} - 1$		ns
14	$t_{w(SPC2)S}$	Pulse duration, SPICLK second pulse	$2t_{c(SYSCLK)} - 1$		ns
15	$t_{d(SOMI)S}$	Delay time, SPICLK to SPISOMI valid		21	ns
16	$t_{v(SOMI)S}$	Valid time, SPISOMI data valid after SPICLK	0		ns
19	$t_{su(SIMO)S}$	Setup time, SPISIMO valid before SPICLK	$1.5t_{c(SYSCLK)}$		ns
20	$t_{h(SIMO)S}$	Hold time, SPISIMO data valid after SPICLK	$1.5t_{c(SYSCLK)}$		ns
25	$t_{su(STE)S}$	Setup time, $\overline{\text{SPISTE}}$ active before SPICLK	$1.5t_{c(SYSCLK)}$		ns
26	$t_{h(STE)S}$	Hold time, $\overline{\text{SPISTE}}$ inactive after SPICLK	$1.5t_{c(SYSCLK)}$		ns

(1) The MASTER / SLAVE bit (SPICTL.2) is cleared and the CLOCK PHASE bit (SPICTL.3) is cleared.
(2) $t_{c(SPC)}$ = SPI clock cycle time = LSPCLK/4 or LSPCLK/(SPIBRR + 1)
(3) $t_{c(LCO)}$ = LSPCLK cycle time
(4) Internal clock prescalers must be adjusted such that the SPI clock speed is limited to the following SPI clock rate:
Master mode transmit 25-MHz MAX, master mode receive 12.5-MHz MAX
Slave mode transmit 12.5-MHz MAX, slave mode receive 12.5-MHz MAX.
(5) The active edge of the SPICLK signal referenced is controlled by the CLOCK POLARITY bit (SPICCR.6).

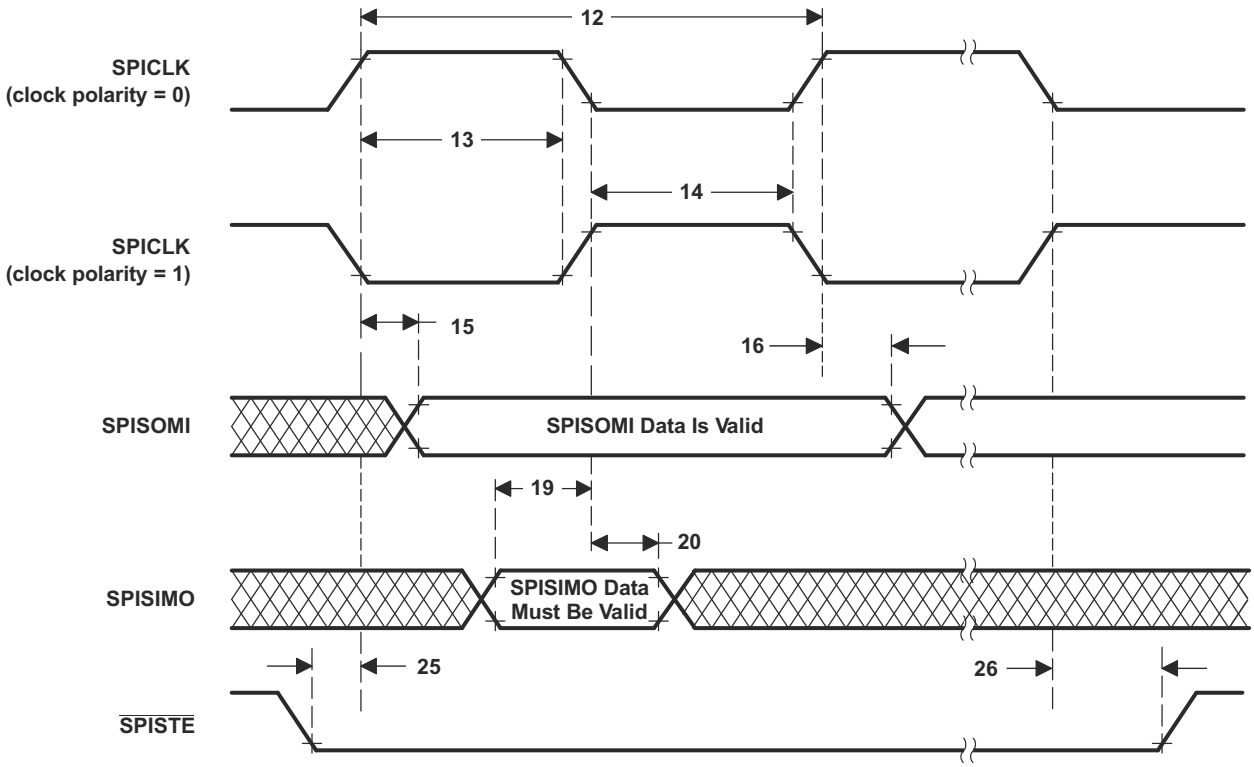

Figure 8-35. SPI Slave Mode External Timing (Clock Phase = 0)

8.9.4.2.2 SPI Slave Mode External Timing (Clock Phase = 1)

NO.	PARAMETER(1) (2) (3) (4)		MIN	MAX	UNIT
12	$t_{c(SPC)S}$	Cycle time, SPICLK	$4t_{c(SYSCLK)}$		ns
13	$t_{w(SPC1)S}$	Pulse duration, SPICLK first pulse	$2t_{c(SYSCLK)} - 1$		ns
14	$t_{w(SPC2)S}$	Pulse duration, SPICLK second pulse	$2t_{c(SYSCLK)} - 1$		ns
17	$t_{d(SOMI)S}$	Delay time, SPICLK to SPISOMI valid		21	ns
18	$t_{v(SOMI)S}$	Valid time, SPISOMI data valid after SPICLK	0		ns
21	$t_{su(SIMO)S}$	Setup time, SPISIMO valid before SPICLK	$1.5t_{c(SYSCLK)}$		ns
22	$t_{h(SIMO)S}$	Hold time, SPISIMO data valid after SPICLK	$1.5t_{c(SYSCLK)}$		ns
25	$t_{su(STE)S}$	Setup time, $\overline{\text{SPISTE}}$ active before SPICLK	$1.5t_{c(SYSCLK)}$		ns
26	$t_{h(STE)S}$	Hold time, $\overline{\text{SPISTE}}$ inactive after SPICLK	$1.5t_{c(SYSCLK)}$		ns

(1) The MASTER / SLAVE bit (SPICTL.2) is cleared and the CLOCK PHASE bit (SPICTL.3) is cleared.
(2) $t_{c(SPC)}$ = SPI clock cycle time = LSPCLK/4 or LSPCLK/(SPIBRR + 1)
(3) Internal clock prescalers must be adjusted such that the SPI clock speed is limited to the following SPI clock rate:
Master mode transmit 25-MHz MAX, master mode receive 12.5-MHz MAX
Slave mode transmit 12.5-MHz MAX, slave mode receive 12.5-MHz MAX.
(4) The active edge of the SPICLK signal referenced is controlled by the CLOCK POLARITY bit (SPICCR.6).

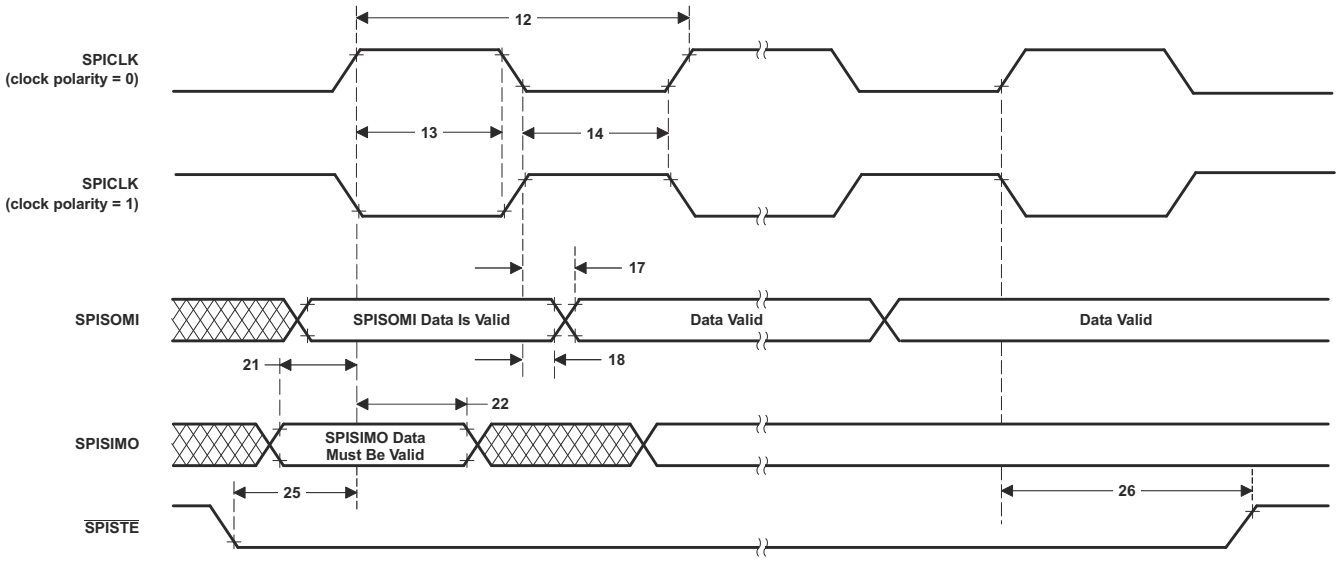

Figure 8-36. SPI Slave Mode External Timing (Clock Phase = 1)

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8.9.5 Serial Communications Interface (SCI) Module

The devices include two serial communications interface (SCI) modules (SCI-A, SCI-B). The SCI module supports digital communications between the CPU and other asynchronous peripherals that use the standard non-return-to-zero (NRZ) format. The SCI receiver and transmitter are double-buffered, and each has its own separate enable and interrupt bits. Both can be operated independently or simultaneously in the full-duplex mode. To ensure data integrity, the SCI checks received data for break detection, parity, overrun, and framing errors. The bit rate is programmable to over 65000 different speeds through a 16-bit baud-select register.

Features of each SCI module include:

- Two external pins:
  - SCITXD: SCI transmit-output pin
  - SCIRXD: SCI receive-input pin

Note

Both pins can be used as GPIO if not used for SCI.

  - Baud rate programmable to 64K different rates:

$$\text{Baud rate} = \frac{\text{LSPCLK}}{(\text{BRR} + 1) * 8} \qquad \text{when BRR} \neq 0$$

$$\text{Baud rate} = \frac{\text{LSPCLK}}{16} \qquad \text{when BRR} = 0$$

- Data-word format
  - One start bit
  - Data-word length programmable from 1 to 8 bits
  - Optional even/odd/no parity bit
  - One or 2 stop bits
- Four error-detection flags: parity, overrun, framing, and break detection
- Two wake-up multiprocessor modes: idle-line and address bit
- Half- or full-duplex operation
- Double-buffered receive and transmit functions
- Transmitter and receiver operations can be accomplished through interrupt-driven or polled algorithms with status flags.
  - Transmitter: TXRDY flag (transmitter-buffer register is ready to receive another character) and TX EMPTY flag (transmitter-shift register is empty)
  - Receiver: RXRDY flag (receiver-buffer register is ready to receive another character), BRKDT flag (break condition occurred), and RX ERROR flag (monitoring four interrupt conditions)
- Separate enable bits for transmitter and receiver interrupts (except BRKDT)
- NRZ (non-return-to-zero) format

Note

All registers in this module are 8-bit registers that are connected to Peripheral Frame 2. When a register is accessed, the register data is in the lower byte (7–0), and the upper byte (15–8) is read as zeros. Writing to the upper byte has no effect.

Enhanced features:

- Auto baud-detect hardware logic
- 4-level transmit/receive FIFO

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The SCI port operation is configured and controlled by the registers listed in Table 8-27 and Table 8-28.

Table 8-27. SCI-A Registers

NAME[1]	ADDRESS	SIZE (×16)	EALLOW PROTECTED	DESCRIPTION
SCICCRA	0x7050	1	No	SCI-A Communications Control Register
SCICTL1A	0x7051	1	No	SCI-A Control Register 1
SCIHBAUDA	0x7052	1	No	SCI-A Baud Register, High Bits
SCILBAUDA	0x7053	1	No	SCI-A Baud Register, Low Bits
SCICTL2A	0x7054	1	No	SCI-A Control Register 2
SCIRXSTA	0x7055	1	No	SCI-A Receive Status Register
SCIRXEMUA	0x7056	1	No	SCI-A Receive Debug Data Buffer Register
SCIRXBUFA	0x7057	1	No	SCI-A Receive Data Buffer Register
SCITXBUFA	0x7059	1	No	SCI-A Transmit Data Buffer Register
SCIFFTXA[2]	0x705A	1	No	SCI-A FIFO Transmit Register
SCIFFRXA[2]	0x705B	1	No	SCI-A FIFO Receive Register
SCIFFCTA[2]	0x705C	1	No	SCI-A FIFO Control Register
SCIPRIA	0x705F	1	No	SCI-A Priority Control Register

(1) Registers in this table are mapped to Peripheral Frame 2 space. This space only allows 16-bit accesses. 32-bit accesses produce undefined results.
(2) These registers are new registers for the FIFO mode.

Table 8-28. SCI-B Registers

NAME[1]	ADDRESS	SIZE (×16)	DESCRIPTION
SCICCRB	0x7750	1	SCI-B Communications Control Register
SCICTL1B	0x7751	1	SCI-B Control Register 1
SCIHBAUDB	0x7752	1	SCI-B Baud Register, High Bits
SCILBAUDB	0x7753	1	SCI-B Baud Register, Low Bits
SCICTL2B	0x7754	1	SCI-B Control Register 2
SCIRXSTB	0x7755	1	SCI-B Receive Status Register
SCIRXEMUB	0x7756	1	SCI-B Receive Debug Data Buffer Register
SCIRXBUFB	0x7757	1	SCI-B Receive Data Buffer Register
SCITXBUFB	0x7759	1	SCI-B Transmit Data Buffer Register
SCIFFTXB[2]	0x775A	1	SCI-B FIFO Transmit Register
SCIFFRXB[2]	0x775B	1	SCI-B FIFO Receive Register
SCIFFCTB[2]	0x775C	1	SCI-B FIFO Control Register
SCIPRIB	0x775F	1	SCI-B Priority Control Register

(1) Registers in this table are mapped to Peripheral Frame 2 space. This space only allows 16-bit accesses. 32-bit accesses produce undefined results.
(2) These registers are new registers for the FIFO mode.

Figure 8-37 shows the SCI module block diagram.

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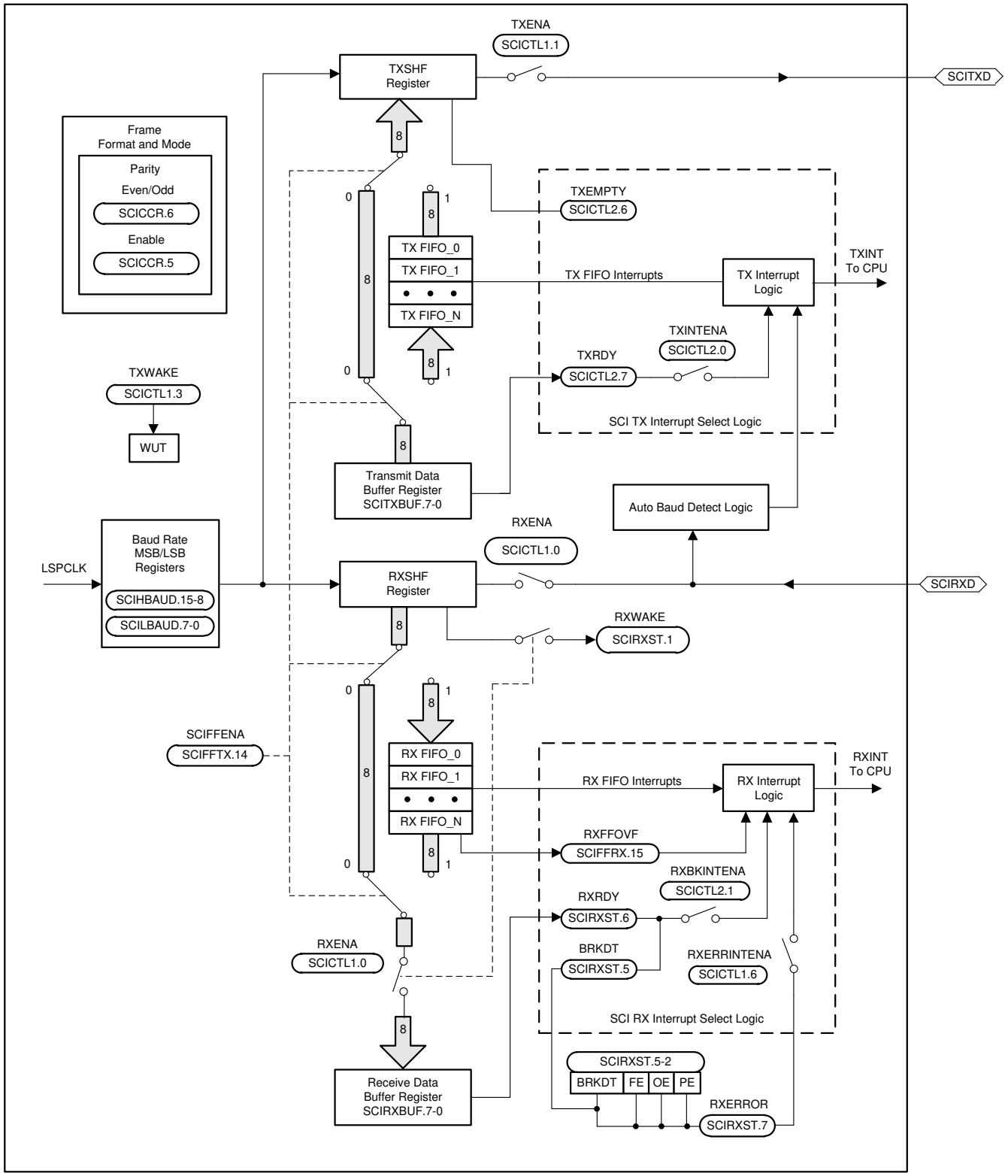
TXENA
SCICTL1.1
TXSHF Register
SCITXD
Frame Format and Mode
Parity
Even/Odd
SCICCR.6
Enable
SCICCR.5
TXEMPTY
SCICTL2.6
TX FIFO_0
TX FIFO_1
TX FIFO_N
TX FIFO Interrupts
TX Interrupt Logic
TXINT To CPU
TXINTENA
SCICTL2.0
TXRDY
SCICTL2.7
TXWAKE
SCICTL1.3
WUT
SCI TX Interrupt Select Logic
Transmit Data Buffer Register SCITXBUF.7-0
Auto Baud Detect Logic
RXENA
SCICTL1.0
LSPCLK
Baud Rate MSB/LSB Registers
SCIHBAUD.15-8
SCILBAUD.7-0
RXSHF Register
SCIRXD
RXWAKE
SCIRXST.1
SCIFFENA
SCIFFTX.14
RX FIFO_0
RX FIFO_1
RX FIFO_N
RX FIFO Interrupts
RX Interrupt Logic
RXINT To CPU
RXFFOVF
SCIFFRX.15
RXBKINTENA
SCICTL2.1
RXRDY
SCIRXST.6
BRKDT
SCIRXST.5
RXERRINTENA
SCICTL1.6
SCI RX Interrupt Select Logic
RXENA
SCICTL1.0
Receive Data Buffer Register SCIRXBUF.7-0
SCIRXST.5-2
BRKDT
FE
OE
PE
RXERROR
SCIRXST.7

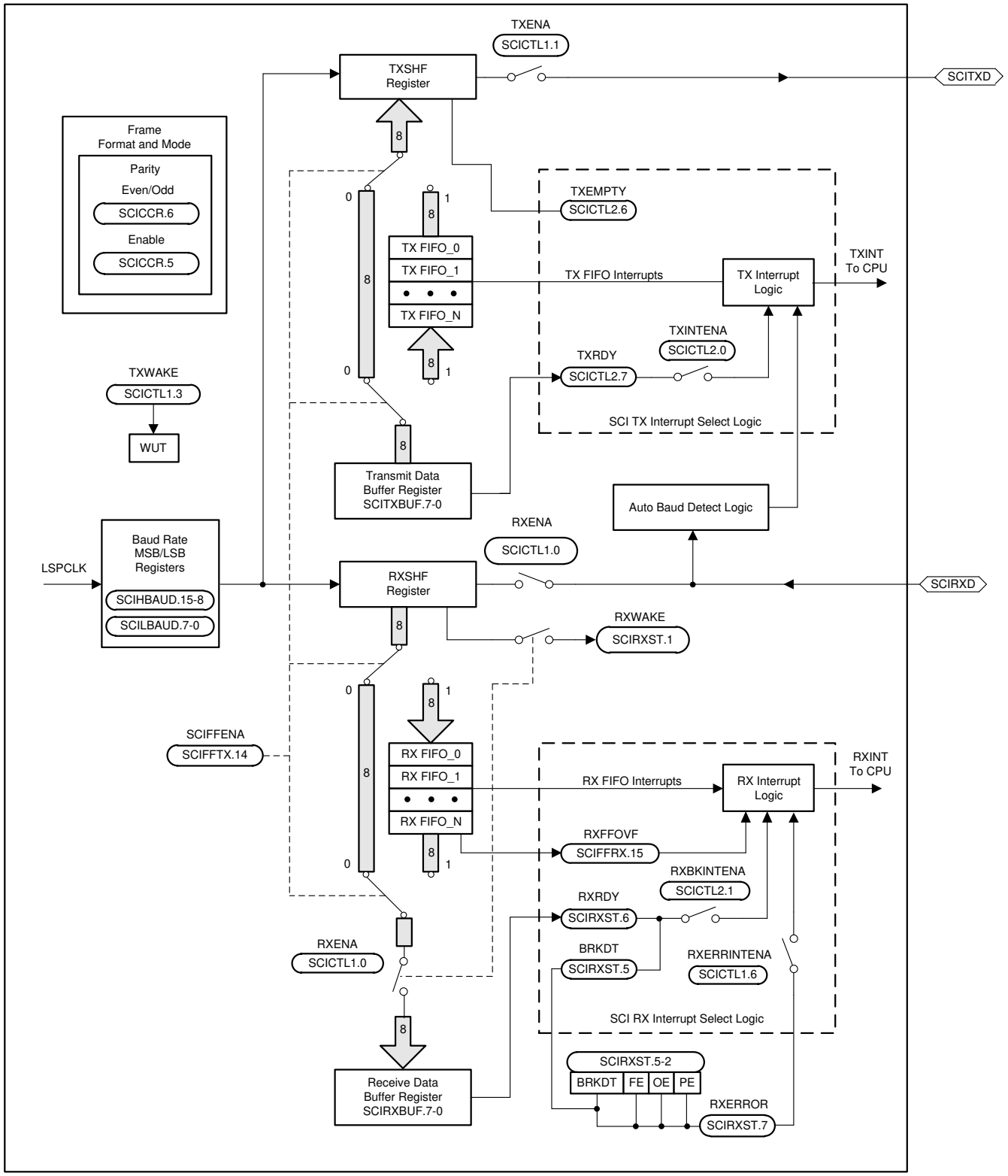

Figure 8-37. Serial Communications Interface (SCI) Module Block Diagram

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8.9.6 Multichannel Buffered Serial Port (McBSP) Module

The McBSP module has the following features:

- Compatible to McBSP in TMS320C28x/TMS320F28x DSP devices
- Full-duplex communication
- Double-buffered data registers that allow a continuous data stream
- Independent framing and clocking for receive and transmit
- External shift clock generation or an internal programmable frequency shift clock
- A wide selection of data sizes including 8-, 12-, 16-, 20-, 24-, or 32-bits
- 8-bit data transfers with LSB or MSB first
- Programmable polarity for both frame synchronization and data clocks
- Highly programmable internal clock and frame generation
- Direct interface to industry-standard CODECs, Analog Interface Chips (AICs), and other serially connected analog-to-digital (A/D) and digital-to-analog (D/A) devices
- Works with SPI-compatible devices
- The following application interfaces can be supported on the McBSP:
  - T1/E1 framers
  - IOM-2 compliant devices
  - AC97-compliant devices (the necessary multiphase frame synchronization capability is provided.)
  - IIS-compliant devices
  - SPI
- McBSP clock rate,

$$CLKG = \frac{CLKSRG}{(1 + CLKGDV)}$$

where CLKSRG source could be LSPCLK, CLKX, or CLKR. Serial port performance is limited by I/O buffer switching speed. Internal prescalers must be adjusted such that the peripheral speed is less than the I/O buffer speed limit.

Note

See Section 8.9 for maximum I/O pin toggling speed.

Note

On the 80-pin package, only the clock-stop mode (SPI) of the McBSP is supported.

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Figure 8-38 shows the block diagram of the McBSP module.

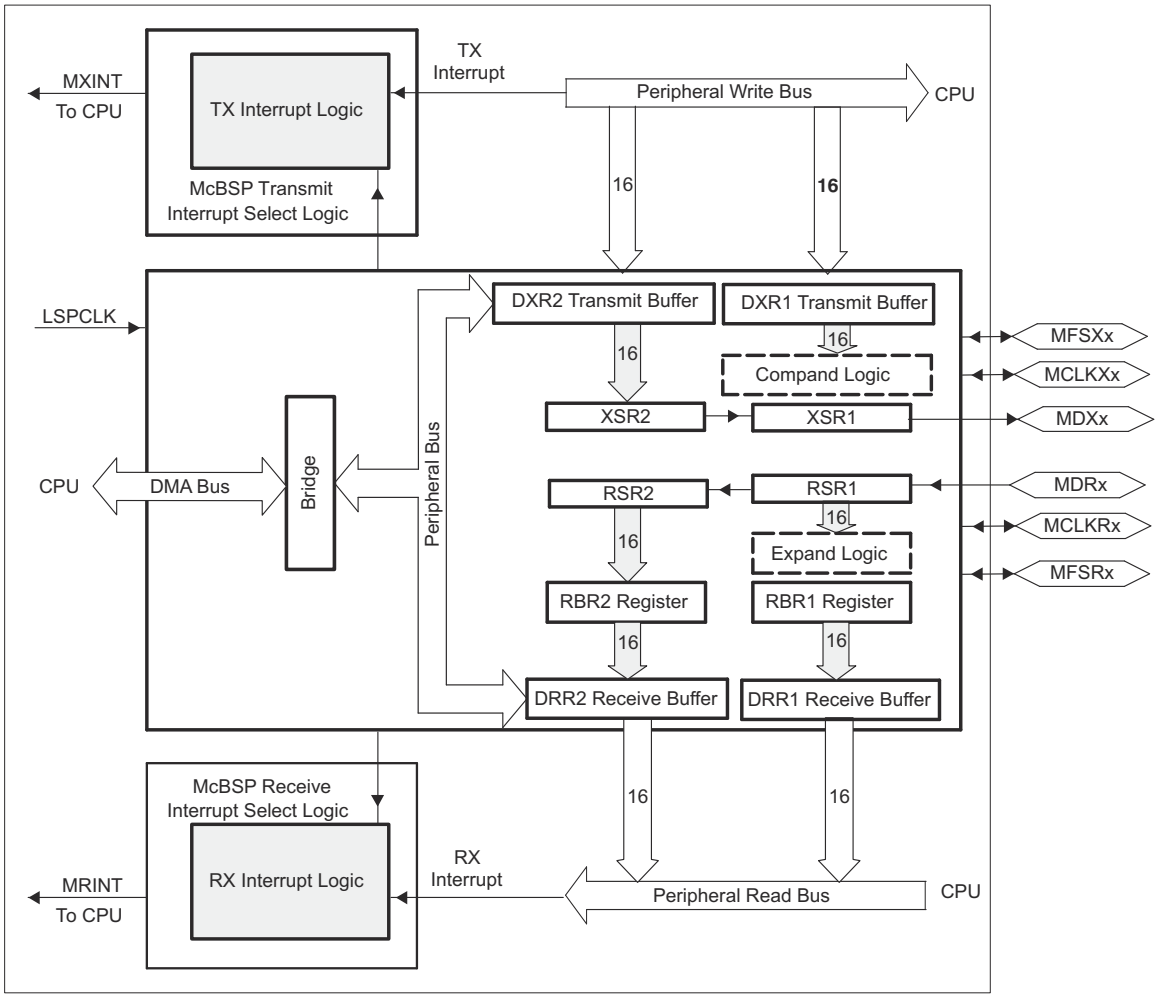

Figure 8-38. McBSP Module

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Table 8-29 provides a summary of the McBSP registers.

Table 8-29. McBSP Register Summary

NAME	McBSP-A ADDRESS	TYPE	RESET VALUE	DESCRIPTION
Data Registers, Receive, Transmit				
DRR2	0x5000	R	0x0000	McBSP Data Receive Register 2
DRR1	0x5001	R	0x0000	McBSP Data Receive Register 1
DXR2	0x5002	W	0x0000	McBSP Data Transmit Register 2
DXR1	0x5003	W	0x0000	McBSP Data Transmit Register 1
McBSP Control Registers				
SPCR2	0x5004	R/W	0x0000	McBSP Serial Port Control Register 2
SPCR1	0x5005	R/W	0x0000	McBSP Serial Port Control Register 1
RCR2	0x5006	R/W	0x0000	McBSP Receive Control Register 2
RCR1	0x5007	R/W	0x0000	McBSP Receive Control Register 1
XCR2	0x5008	R/W	0x0000	McBSP Transmit Control Register 2
XCR1	0x5009	R/W	0x0000	McBSP Transmit Control Register 1
SRGR2	0x500A	R/W	0x0000	McBSP Sample Rate Generator Register 2
SRGR1	0x500B	R/W	0x0000	McBSP Sample Rate Generator Register 1
Multichannel Control Registers				
MCR2	0x500C	R/W	0x0000	McBSP Multichannel Register 2
MCR1	0x500D	R/W	0x0000	McBSP Multichannel Register 1
RCERA	0x500E	R/W	0x0000	McBSP Receive Channel Enable Register Partition A
RCERB	0x500F	R/W	0x0000	McBSP Receive Channel Enable Register Partition B
XCERA	0x5010	R/W	0x0000	McBSP Transmit Channel Enable Register Partition A
XCERB	0x5011	R/W	0x0000	McBSP Transmit Channel Enable Register Partition B
PCR	0x5012	R/W	0x0000	McBSP Pin Control Register
RCERC	0x5013	R/W	0x0000	McBSP Receive Channel Enable Register Partition C
RCERD	0x5014	R/W	0x0000	McBSP Receive Channel Enable Register Partition D
XCERC	0x5015	R/W	0x0000	McBSP Transmit Channel Enable Register Partition C
XCERD	0x5016	R/W	0x0000	McBSP Transmit Channel Enable Register Partition D
RCERE	0x5017	R/W	0x0000	McBSP Receive Channel Enable Register Partition E
RCERF	0x5018	R/W	0x0000	McBSP Receive Channel Enable Register Partition F
XCERE	0x5019	R/W	0x0000	McBSP Transmit Channel Enable Register Partition E
XCERF	0x501A	R/W	0x0000	McBSP Transmit Channel Enable Register Partition F
RCERG	0x501B	R/W	0x0000	McBSP Receive Channel Enable Register Partition G
RCERH	0x501C	R/W	0x0000	McBSP Receive Channel Enable Register Partition H
XCERG	0x501D	R/W	0x0000	McBSP Transmit Channel Enable Register Partition G
XCERH	0x501E	R/W	0x0000	McBSP Transmit Channel Enable Register Partition H
MFFINT	0x5023	R/W	0x0000	McBSP Interrupt Enable Register

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8.9.6.1 McBSP Electrical Data/Timing

8.9.6.1.1 McBSP Transmit and Receive Timing

8.9.6.1.1.1 McBSP Timing Requirements

NO.(1) (2)				MIN	MAX	UNIT
		McBSP module clock (CLKG, CLKX, CLKR) range		1		kHz
					20(3) (4)	MHz
		McBSP module cycle time (CLKG, CLKX, CLKR) range		50(4)		ns
					1	ms
M11	$t_{c(CKRX)}$	Cycle time, CLKR/X	CLKR/X ext	2P		ns
M12	$t_{w(CKRX)}$	Pulse duration, CLKR/X high or CLKR/X low	CLKR/X ext	P – 7		ns
M13	$t_{r(CKRX)}$	Rise time, CLKR/X	CLKR/X ext		7	ns
M14	$t_{f(CKRX)}$	Fall time, CLKR/X	CLKR/X ext		7	ns
M15	$t_{su(FRH-CKRL)}$	Setup time, external FSR high before CLKR low	CLKR int	18		ns
			CLKR ext	2		
M16	$t_{h(CKRL-FRH)}$	Hold time, external FSR high after CLKR low	CLKR int	0		ns
			CLKR ext	6		
M17	$t_{su(DRV-CKRL)}$	Setup time, DR valid before CLKR low	CLKR int	18		ns
			CLKR ext	2		
M18	$t_{h(CKRL-DRV)}$	Hold time, DR valid after CLKR low	CLKR int	0		ns
			CLKR ext	6		
M19	$t_{su(FXH-CKXL)}$	Setup time, external FSX high before CLKX low	CLKX int	18		ns
			CLKX ext	2		
M20	$t_{h(CKXL-FXH)}$	Hold time, external FSX high after CLKX low	CLKX int	0		ns
			CLKX ext	6		

(1) Polarity bits CLKRP = CLKXP = FSRP = FSXP = 0. If the polarity of any of the signals is inverted, then the timing references of that signal are also inverted.
(2) 2P = 1/CLKG in ns. CLKG is the output of sample rate generator mux. CLKG = CLKSRG/(1 + CLKGDV). CLKSRG can be LSPCLK, CLKX, CLKR as source. CLKSRG ≤ (SYSCLKOUT/2). McBSP performance is limited by I/O buffer switching speed.
(3) Internal clock prescalers must be adjusted such that the McBSP clock (CLKG, CLKX, CLKR) speeds are not greater than the I/O buffer speed limit (20 MHz).
(4) Maximum McBSP module clock frequency decreases to 10 MHz for internal CLKR.

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8.9.6.1.1.2 McBSP Switching Characteristics

over recommended operating conditions (unless otherwise noted)

NO.	PARAMETER[1] [2]				MIN	MAX	UNIT
M1	$t_{c(CKRX)}$	Cycle time, CLKR/X		CLKR/X int	2P		ns
M2	$t_{w(CKRXH)}$	Pulse duration, CLKR/X high		CLKR/X int	D – 5[3]	D + 5[3]	ns
M3	$t_{w(CKRXL)}$	Pulse duration, CLKR/X low		CLKR/X int	C – 5[3]	C + 5[3]	ns
M4	$t_{d(CKRH-FRV)}$	Delay time, CLKR high to internal FSR valid		CLKR int	0	4	ns
				CLKR ext	3	27	
M5	$t_{d(CKXH-FXV)}$	Delay time, CLKX high to internal FSX valid		CLKX int	0	4	ns
				CLKX ext	3	27	
M6	$t_{dis(CKXH-DXHZ)}$	Disable time, CLKX high to DX high impedance following last data bit		CLKX int		8	ns
				CLKX ext		14	
M7	$t_{d(CKXH-DXV)}$	Delay time, CLKX high to DX valid. This applies to all bits except the first bit transmitted.		CLKX int		9	ns
				CLKX ext		28	
		Delay time, CLKX high to DX valid	DXENA = 0	CLKX int		8	
				CLKX ext		14	
		Only applies to first bit transmitted when in Data Delay 1 or 2 (XDATDLY=01b or 10b) modes	DXENA = 1	CLKX int		P + 8	
				CLKX ext		P + 14	
M8	$t_{en(CKXH-DX)}$	Enable time, CLKX high to DX driven	DXENA = 0	CLKX int	0		ns
				CLKX ext	6		
		Only applies to first bit transmitted when in Data Delay 1 or 2 (XDATDLY=01b or 10b) modes	DXENA = 1	CLKX int	P		
				CLKX ext	P + 6		
M9	$t_{d(FXH-DXV)}$	Delay time, FSX high to DX valid	DXENA = 0	FSX int		8	ns
				FSX ext		14	
		Only applies to first bit transmitted when in Data Delay 0 (XDATDLY=00b) mode.	DXENA = 1	FSX int		P + 8	
				FSX ext		P + 14	
M10	$t_{en(FXH-DX)}$	Enable time, FSX high to DX driven	DXENA = 0	FSX int	0		ns
				FSX ext	6		
		Only applies to first bit transmitted when in Data Delay 0 (XDATDLY=00b) mode	DXENA = 1	FSX int	P		
				FSX ext	P + 6		

(1) Polarity bits CLKRP = CLKXP = FSRP = FSXP = 0. If the polarity of any of the signals is inverted, then the timing references of that signal are also inverted.
(2) 2P = 1/CLKG in ns.
(3) C = CLKRX low pulse width = P
D = CLKRX high pulse width = P

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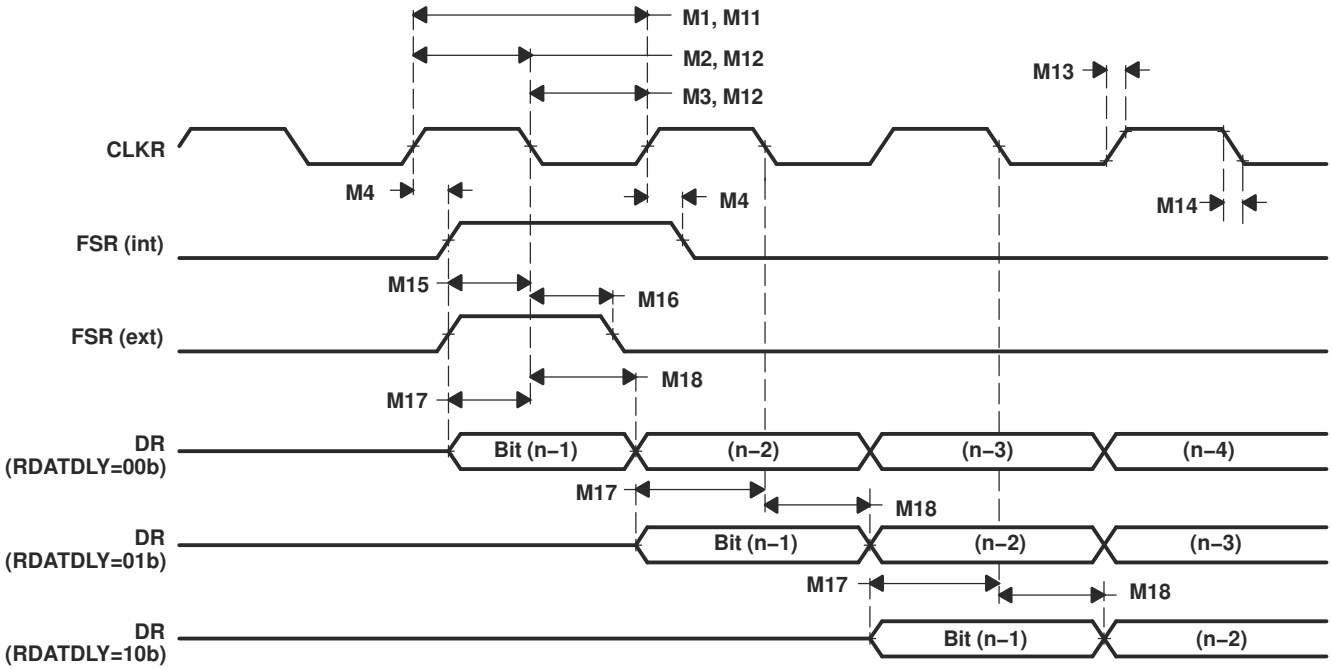

Figure 8-39. McBSP Receive Timing

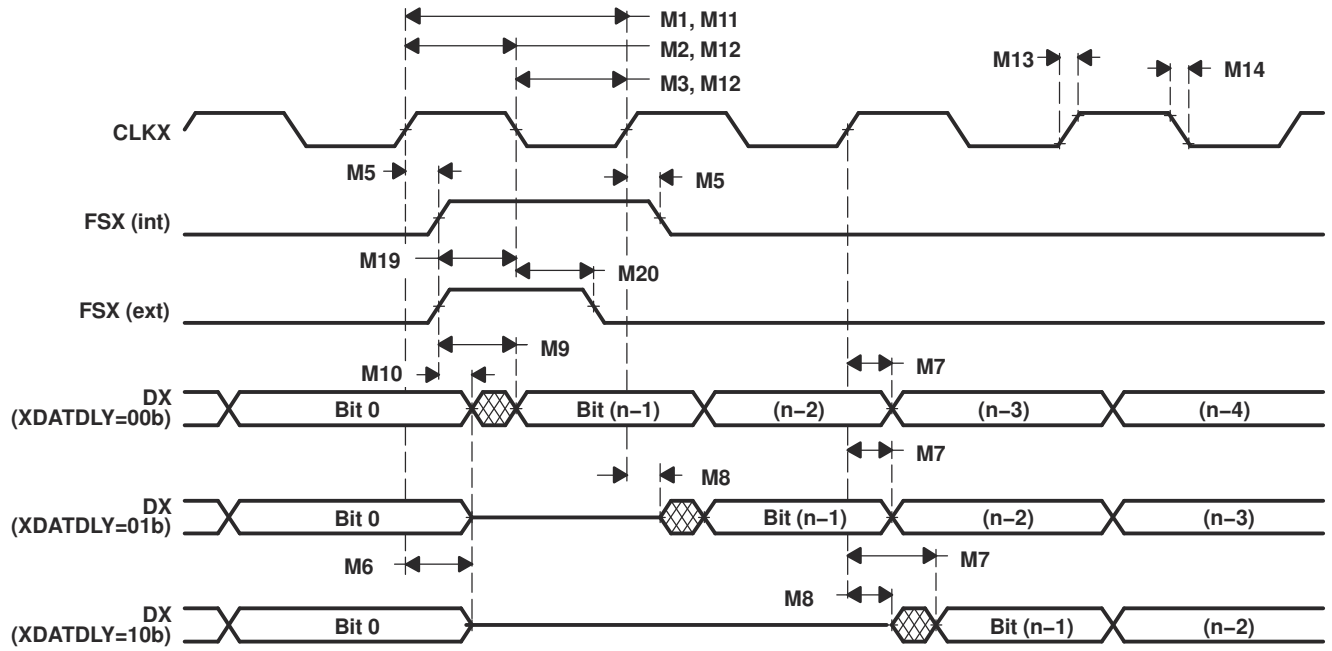

Figure 8-40. McBSP Transmit Timing

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8.9.6.1.2 McBSP as SPI Master or Slave Timing

8.9.6.1.2.1 McBSP as SPI Master or Slave Timing Requirements (CLKSTP = 10b, CLKXP = 0)

NO.(1)			MASTER		SLAVE		UNIT
			MIN	MAX	MIN	MAX	
M30	$t_{su(DRV-CKXL)}$	Setup time, DR valid before CLKX low	30		8P – 10		ns
M31	$t_{h(CKXL-DRV)}$	Hold time, DR valid after CLKX low	1		8P – 10		ns
M32	$t_{su(BFXL-CKXH)}$	Setup time, FSX low before CLKX high			8P + 10		ns
M33	$t_{c(CKX)}$	Cycle time, CLKX	2P(2)		16P		ns

(1) For all SPI slave modes, CLKX has to be a minimum of 8 CLKG cycles. Furthermore, CLKG should be LSPCLK/2 by setting CLKSM = CLKGDV = 1.
(2) 2P = 1/CLKG

8.9.6.1.2.2 McBSP as SPI Master or Slave Switching Characteristics (CLKSTP = 10b, CLKXP = 0)

over recommended operating conditions (unless otherwise noted)

NO.	PARAMETER		MASTER		SLAVE		UNIT
			MIN	MAX	MIN	MAX	
M24	$t_{h(CKXL-FXL)}$	Hold time, FSX low after CLKX low	2P(1)				ns
M25	$t_{d(FXL-CKXH)}$	Delay time, FSX low to CLKX high	P				ns
M26	$t_{d(CKXH-DXV)}$	Delay time, CLKX high to DX valid	–2	0	3P + 6	5P + 20	ns
M28	$t_{dis(FXH-DXHZ)}$	Disable time, DX high impedance following last data bit from FSX high	6		6P + 6		ns
M29	$t_{d(FXL-DXV)}$	Delay time, FSX low to DX valid	6		4P + 6		ns

(1) 2P = 1/CLKG

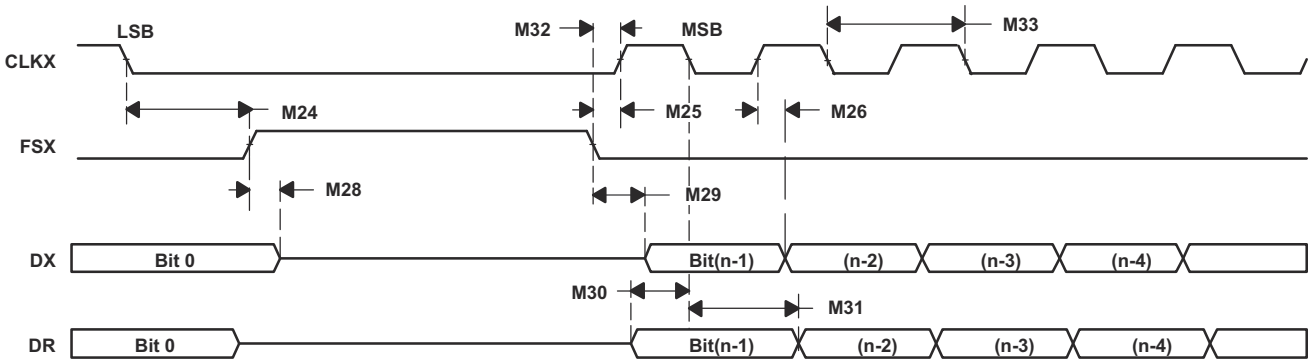

Figure 8-41. McBSP Timing as SPI Master or Slave: CLKSTP = 10b, CLKXP = 0

8.9.6.1.2.3 McBSP as SPI Master or Slave Timing Requirements (CLKSTP = 11b, CLKXP = 0)

NO.[1]			MASTER		SLAVE		UNIT
			MIN	MAX	MIN	MAX	
M39	$t_{su(DRV-CKXH)}$	Setup time, DR valid before CLKX high	30		8P – 10		ns
M40	$t_{h(CKXH-DRV)}$	Hold time, DR valid after CLKX high	1		8P – 10		ns
M41	$t_{su(FXL-CKXH)}$	Setup time, FSX low before CLKX high			16P + 10		ns
M42	$t_{c(CKX)}$	Cycle time, CLKX	2P[2]		16P		ns

(1) For all SPI slave modes, CLKX has to be a minimum of 8 CLKG cycles. Furthermore, CLKG should be LSPCLK/2 by setting CLKSM = CLKGDV = 1.
(2) 2P = 1/CLKG

8.9.6.1.2.4 McBSP as SPI Master or Slave Switching Characteristics (CLKSTP = 11b, CLKXP = 0)

over recommended operating conditions (unless otherwise noted)

NO.	PARAMETER		MASTER		SLAVE		UNIT
			MIN	MAX	MIN	MAX	
M34	$t_{h(CKXL-FXL)}$	Hold time, FSX low after CLKX low	P				ns
M35	$t_{d(FXL-CKXH)}$	Delay time, FSX low to CLKX high	2P[1]				ns
M36	$t_{d(CKXL-DXV)}$	Delay time, CLKX low to DX valid	–2	0	3P + 6	5P + 20	ns
M37	$t_{dis(CKXL-DXHZ)}$	Disable time, DX high impedance following last data bit from CLKX low	P + 6		7P + 6		ns
M38	$t_{d(FXL-DXV)}$	Delay time, FSX low to DX valid	6		4P + 6		ns

(1) 2P = 1/CLKG

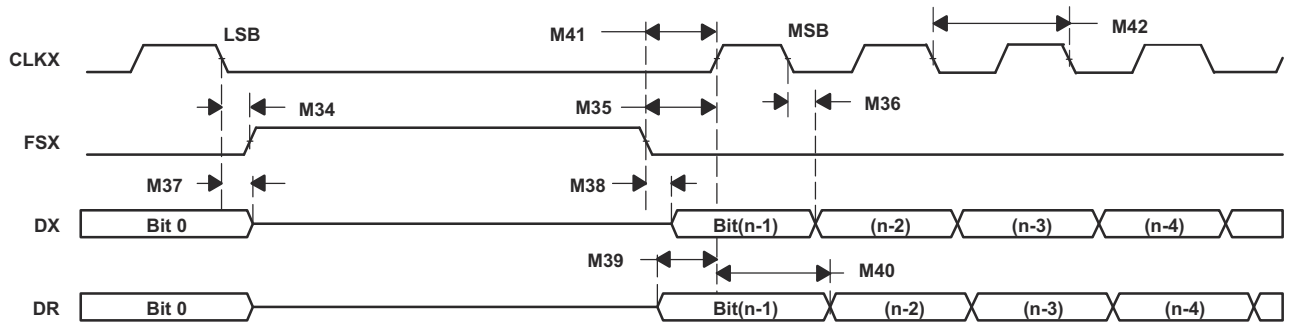

Figure 8-42. McBSP Timing as SPI Master or Slave: CLKSTP = 11b, CLKXP = 0

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8.9.6.1.2.5 McBSP as SPI Master or Slave Timing Requirements (CLKSTP = 10b, CLKXP = 1)

NO.(1)			MASTER		SLAVE		UNIT
			MIN	MAX	MIN	MAX	
M49	$t_{su(DRV-CKXH)}$	Setup time, DR valid before CLKX high	30		8P – 10		ns
M50	$t_{h(CKXH-DRV)}$	Hold time, DR valid after CLKX high	1		8P – 10		ns
M51	$t_{su(FXL-CKXL)}$	Setup time, FSX low before CLKX low			8P + 10		ns
M52	$t_{c(CKX)}$	Cycle time, CLKX	2P(2)		16P		ns

(1) For all SPI slave modes, CLKX has to be a minimum of 8 CLKG cycles. Furthermore, CLKG should be LSPCLK/2 by setting CLKSM = CLKGDV = 1.
(2) 2P = 1/CLKG

8.9.6.1.2.6 McBSP as SPI Master or Slave Switching Characteristics (CLKSTP = 10b, CLKXP = 1)

over recommended operating conditions (unless otherwise noted)

NO.	PARAMETER		MASTER		SLAVE		UNIT
			MIN	MAX	MIN	MAX	
M43	$t_{h(CKXH-FXL)}$	Hold time, FSX low after CLKX high	2P(1)				ns
M44	$t_{d(FXL-CKXL)}$	Delay time, FSX low to CLKX low	P				ns
M45	$t_{d(CKXL-DXV)}$	Delay time, CLKX low to DX valid	–2	0	3P + 6	5P + 20	ns
M47	$t_{dis(FXH-DXHZ)}$	Disable time, DX high impedance following last data bit from FSX high	6		6P + 6		ns
M48	$t_{d(FXL-DXV)}$	Delay time, FSX low to DX valid	6		4P + 6		ns

(1) 2P = 1/CLKG

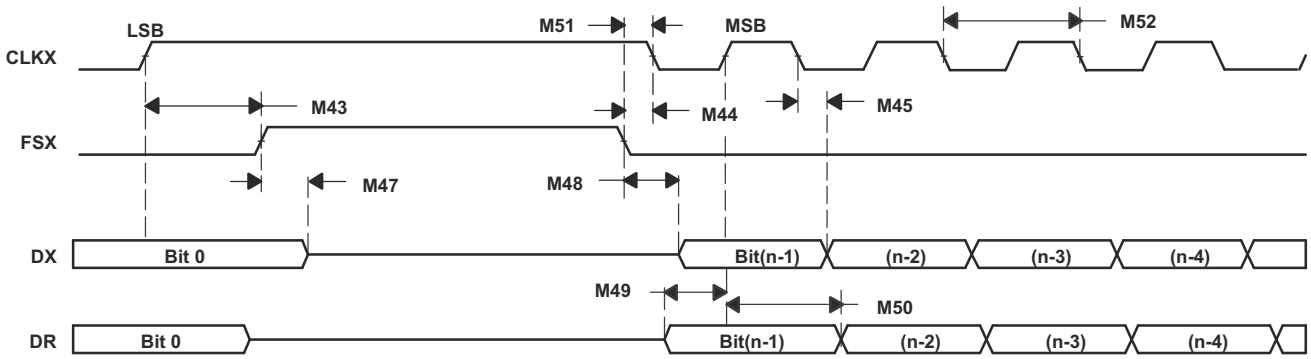

Figure 8-43. McBSP Timing as SPI Master or Slave: CLKSTP = 10b, CLKXP = 1

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8.9.6.1.2.7 McBSP as SPI Master or Slave Timing Requirements (CLKSTP = 11b, CLKXP = 1)

NO.[1]			MASTER		SLAVE		UNIT
			MIN	MAX	MIN	MAX	
M58	$t_{su(DRV-CKXL)}$	Setup time, DR valid before CLKX low	30		8P – 10		ns
M59	$t_{h(CKXL-DRV)}$	Hold time, DR valid after CLKX low	1		8P – 10		ns
M60	$t_{su(FXL-CKXL)}$	Setup time, FSX low before CLKX low			16P + 10		ns
M61	$t_{c(CKX)}$	Cycle time, CLKX	2P[2]		16P		ns

(1) For all SPI slave modes, CLKX has to be a minimum of 8 CLKG cycles. Furthermore, CLKG should be LSPCLK/2 by setting CLKSM = CLKGDV = 1.
(2) 2P = 1/CLKG

8.9.6.1.2.8 McBSP as SPI Master or Slave Switching Characteristics (CLKSTP = 11b, CLKXP = 1)

over recommended operating conditions (unless otherwise noted)[1]

NO.	PARAMETER		MASTER		SLAVE		UNIT
			MIN	MAX	MIN	MAX	
M53	$t_{h(CKXH-FXL)}$	Hold time, FSX low after CLKX high	P				ns
M54	$t_{d(FXL-CKXL)}$	Delay time, FSX low to CLKX low	2P[1]				ns
M55	$t_{d(CKXH-DXV)}$	Delay time, CLKX high to DX valid	–2	0	3P + 6	5P + 20	ns
M56	$t_{dis(CKXH-DXHZ)}$	Disable time, DX high impedance following last data bit from CLKX high	P + 6		7P + 6		ns
M57	$t_{d(FXL-DXV)}$	Delay time, FSX low to DX valid	6		4P + 6		ns

(1) 2P = 1/CLKG

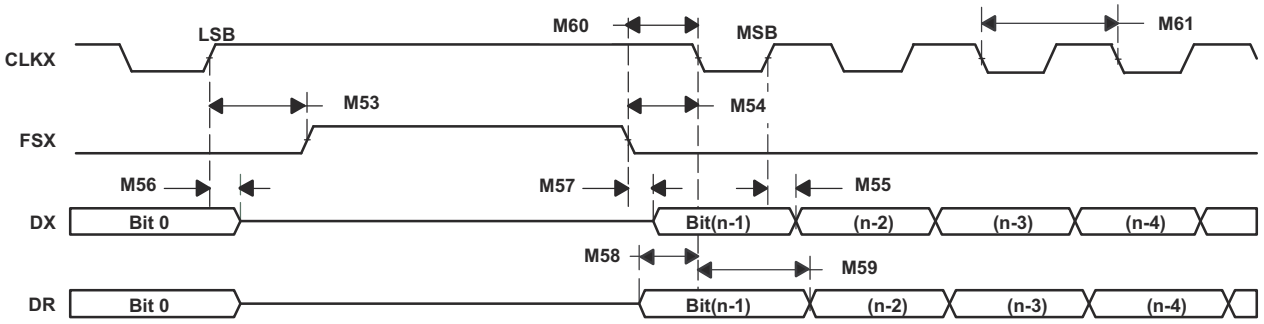

Figure 8-44. McBSP Timing as SPI Master or Slave: CLKSTP = 11b, CLKXP = 1

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8.9.7 Enhanced Controller Area Network (eCAN) Module

The CAN module (eCAN-A) has the following features:

- Fully compliant with CAN protocol, version 2.0B
- Supports data rates up to 1 Mbps
- Thirty-two mailboxes, each with the following properties:
  - Configurable as receive or transmit
  - Configurable with standard or extended identifier
  - Has a programmable receive mask
  - Supports data and remote frame
  - Composed of 0 to 8 bytes of data
  - Uses a 32-bit timestamp on receive and transmit message
  - Protects against reception of new message
  - Holds the dynamically programmable priority of transmit message
  - Employs a programmable interrupt scheme with two interrupt levels
  - Employs a programmable alarm on transmission or reception time-out
- Low-power mode
- Programmable wake-up on bus activity
- Automatic reply to a remote request message
- Automatic retransmission of a frame in case of loss of arbitration or error
- 32-bit local network time counter synchronized by a specific message (communication in conjunction with mailbox 16)
- Self-test mode
  - Operates in a loopback mode receiving its own message. A "dummy" acknowledge is provided, thereby eliminating the need for another node to provide the acknowledge bit.

Note

For a SYSCLKOUT of 90 MHz, the smallest bit rate possible is 6.25 kbps.

The F2806x CAN has passed the conformance test per ISO/DIS 16845. Contact TI for test report and exceptions.

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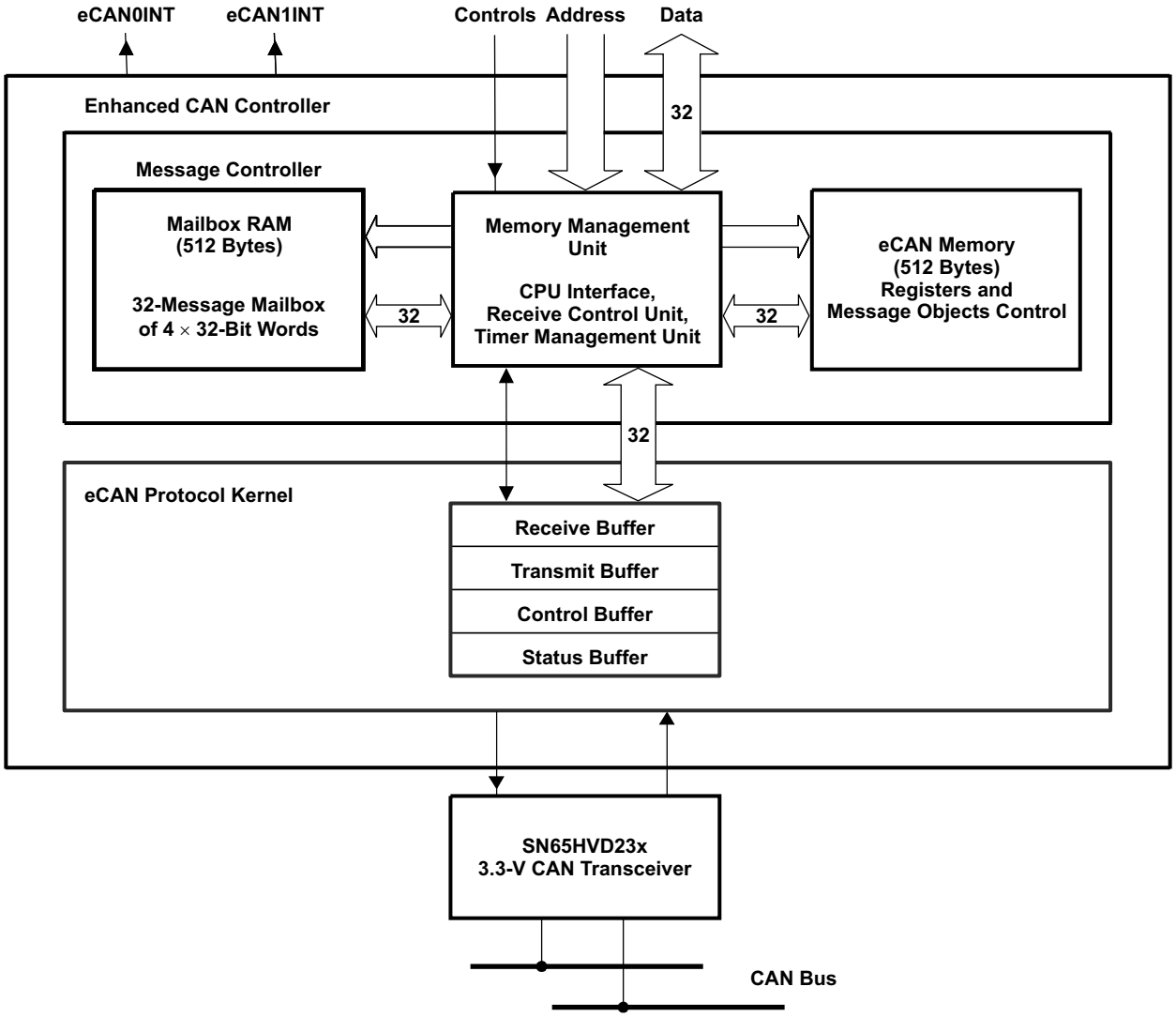

Figure 8-45. eCAN Block Diagram and Interface Circuit

Table 8-30. 3.3-V eCAN Transceivers

PART NUMBER	SUPPLY VOLTAGE	LOW-POWER MODE	SLOPE CONTROL	VREF	OTHER	T_A
SN65HVD230	3.3 V	Standby	Adjustable	Yes	–	–40°C to 85°C
SN65HVD230Q	3.3 V	Standby	Adjustable	Yes	–	–40°C to 125°C
SN65HVD231	3.3 V	Sleep	Adjustable	Yes	–	–40°C to 85°C
SN65HVD231Q	3.3 V	Sleep	Adjustable	Yes	–	–40°C to 125°C
SN65HVD232	3.3 V	None	None	None	–	–40°C to 85°C
SN65HVD232Q	3.3 V	None	None	None	–	–40°C to 125°C
SN65HVD233	3.3 V	Standby	Adjustable	None	Diagnostic Loopback	–40°C to 125°C
SN65HVD234	3.3 V	Standby and Sleep	Adjustable	None	–	–40°C to 125°C
SN65HVD235	3.3 V	Standby	Adjustable	None	Autobaud Loopback	–40°C to 125°C
ISO1050	3–5.5 V	None	None	None	Built-in Isolation Low Prop Delay Thermal Shutdown Fail-safe Operation Dominant Time-Out	–55°C to 105°C

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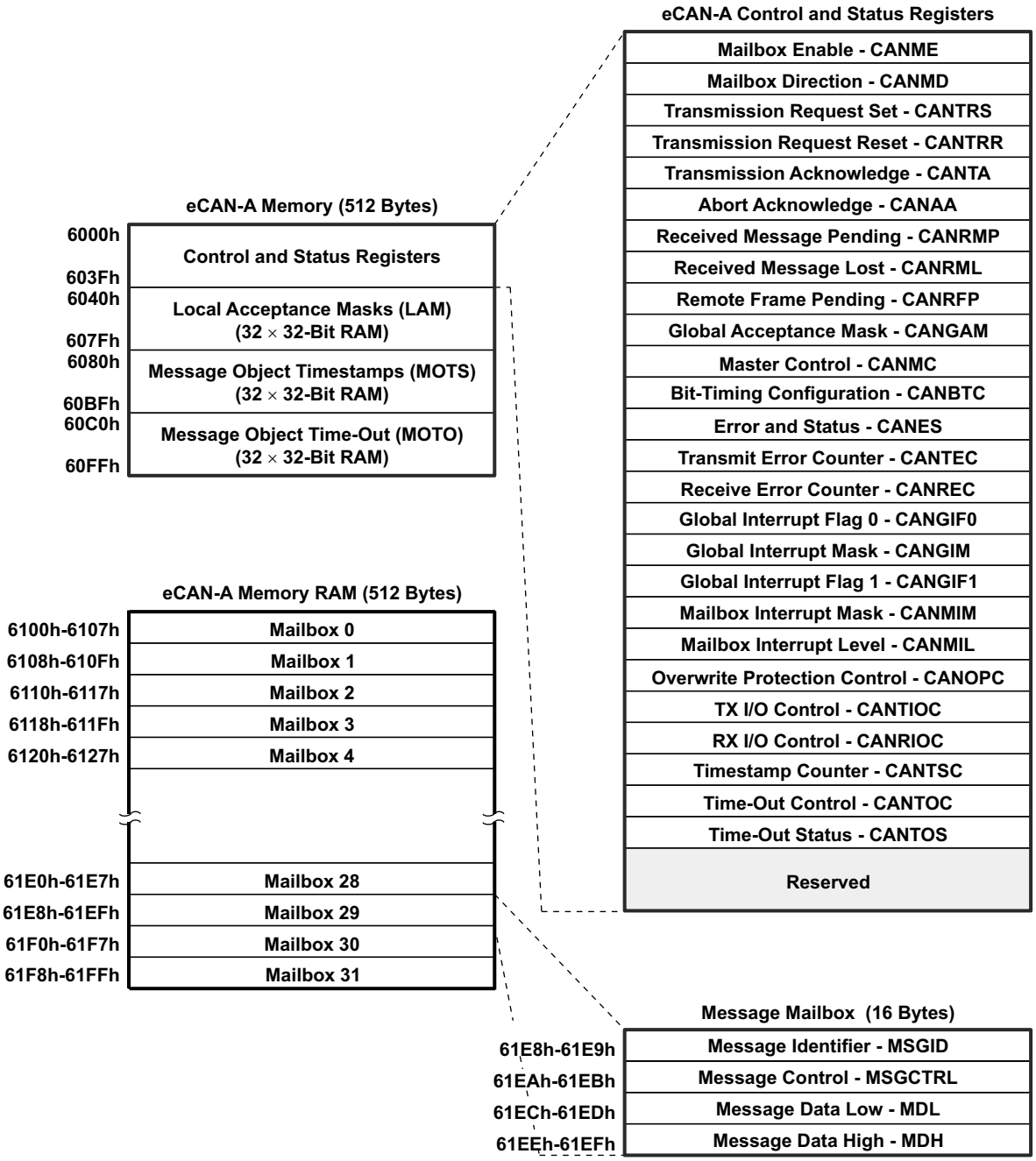

Figure 8-46. eCAN-A Memory Map

Note

If the eCAN module is not used in an application, the RAM available (LAM, MOTS, MOTO, and mailbox RAM) can be used as general-purpose RAM. The CAN module clock should be enabled for this.

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The CAN registers listed in Table 8-31 are used by the CPU to configure and control the CAN controller and the message objects. eCAN control registers only support 32-bit read/write operations. Mailbox RAM can be accessed as 16 bits or 32 bits. All 32-bit accesses are aligned to an even boundary.

Table 8-31. CAN Registers

REGISTER NAME(1)	eCAN-A ADDRESS	SIZE (×32)	DESCRIPTION
CANME	0x6000	1	Mailbox enable
CANMD	0x6002	1	Mailbox direction
CANTRS	0x6004	1	Transmit request set
CANTRR	0x6006	1	Transmit request reset
CANTA	0x6008	1	Transmission acknowledge
CANAA	0x600A	1	Abort acknowledge
CANRMP	0x600C	1	Receive message pending
CANRML	0x600E	1	Receive message lost
CANRFP	0x6010	1	Remote frame pending
CANGAM	0x6012	1	Global acceptance mask
CANMC	0x6014	1	Master control
CANBTC	0x6016	1	Bit-timing configuration
CANES	0x6018	1	Error and status
CANTEC	0x601A	1	Transmit error counter
CANREC	0x601C	1	Receive error counter
CANGIF0	0x601E	1	Global interrupt flag 0
CANGIM	0x6020	1	Global interrupt mask
CANGIF1	0x6022	1	Global interrupt flag 1
CANMIM	0x6024	1	Mailbox interrupt mask
CANMIL	0x6026	1	Mailbox interrupt level
CANOPC	0x6028	1	Overwrite protection control
CANTIOC	0x602A	1	TX I/O control
CANRIOC	0x602C	1	RX I/O control
CANTSC	0x602E	1	Timestamp counter (Reserved in SCC mode)
CANTOC	0x6030	1	Time-out control (Reserved in SCC mode)
CANTOS	0x6032	1	Time-out status (Reserved in SCC mode)

(1) These registers are mapped to Peripheral Frame 1.

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8.9.8 Inter-Integrated Circuit (I2C)

The device contains one I2C Serial Port. Figure 8-47 shows how the I2C peripheral module interfaces within the device.

The I2C module has the following features:

- Compliance with the Philips Semiconductors I^2C-bus specification (version 2.1):
  - Support for 1-bit to 8-bit format transfers
  - 7-bit and 10-bit addressing modes
  - General call
  - START byte mode
  - Support for multiple master-transmitters and slave-receivers
  - Support for multiple slave-transmitters and master-receivers
  - Combined master transmit/receive and receive/transmit mode
  - Data transfer rate of from 10 kbps up to 400 kbps (I2C Fast-mode rate)
- One 4-word receive FIFO and one 4-word transmit FIFO
- One interrupt that can be used by the CPU. This interrupt can be generated as a result of one of the following conditions:
  - Transmit-data ready
  - Receive-data ready
  - Register-access ready
  - No-acknowledgment received
  - Arbitration lost
  - Stop condition detected
  - Addressed as slave
- An additional interrupt that can be used by the CPU when in FIFO mode
- Module enable/disable capability
- Free data format mode

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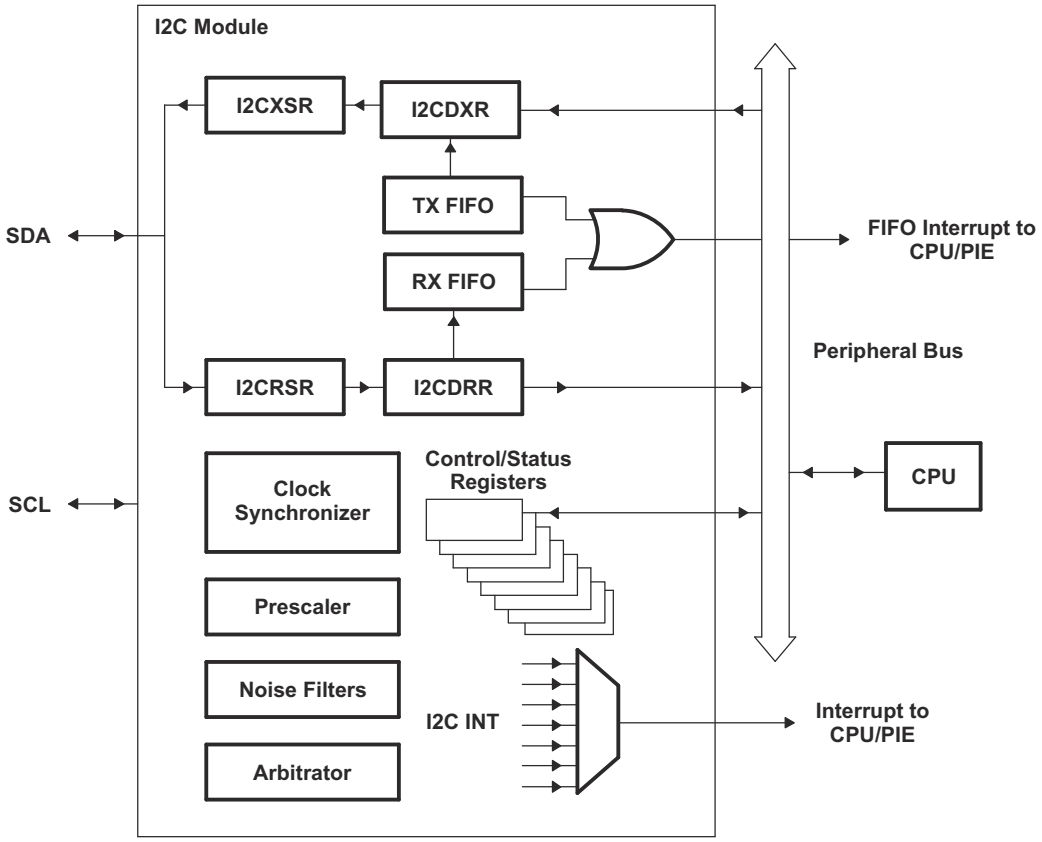

A. The I2C registers are accessed at the SYSCLKOUT rate. The internal timing and signal waveforms of the I2C port are also at the SYSCLKOUT rate.

B. The clock enable bit (I2CAENCLK) in the PCLKCRO register turns off the clock to the I2C port for low-power operation. Upon reset, I2CAENCLK is clear, which indicates the peripheral internal clocks are off.

Figure 8-47. I2C Peripheral Module Interfaces

The registers in Table 8-32 configure and control the I2C port operation.

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Table 8-32. I2C-A Registers

NAME	ADDRESS	EALLOW PROTECTED	DESCRIPTION
I2COAR	0x7900	No	I2C own address register
I2CIER	0x7901	No	I2C interrupt enable register
I2CSTR	0x7902	No	I2C status register
I2CCLKL	0x7903	No	I2C clock low-time divider register
I2CCLKH	0x7904	No	I2C clock high-time divider register
I2CCNT	0x7905	No	I2C data count register
I2CDRR	0x7906	No	I2C data receive register
I2CSAR	0x7907	No	I2C slave address register
I2CDXR	0x7908	No	I2C data transmit register
I2CMDR	0x7909	No	I2C mode register
I2CISRC	0x790A	No	I2C interrupt source register
I2CPSC	0x790C	No	I2C prescaler register
I2CFFTX	0x7920	No	I2C FIFO transmit register
I2CFFRX	0x7921	No	I2C FIFO receive register
I2CRSR	–	No	I2C receive shift register (not accessible to the CPU)
I2CXSR	–	No	I2C transmit shift register (not accessible to the CPU)

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8.9.8.1 I2C Electrical Data/Timing

Section 8.9.8.1.1 shows the I2C timing requirements. Section 8.9.8.1.2 shows the I2C switching characteristics.

8.9.8.1.1 I2C Timing Requirements

			MIN	MAX	UNIT
$t_{h(SDA-SCL)START}$	Hold time, START condition, SCL fall delay after SDA fall		0.6		µs
$t_{su(SCL-SDA)START}$	Setup time, Repeated START, SCL rise before SDA fall delay		0.6		µs
$t_{h(SCL-DAT)}$	Hold time, data after SCL fall		0		µs
$t_{su(DAT-SCL)}$	Setup time, data before SCL rise		100		ns
$t_{r(SDA)}$	Rise time, SDA	Input tolerance	20	300	ns
$t_{r(SCL)}$	Rise time, SCL	Input tolerance	20	300	ns
$t_{f(SDA)}$	Fall time, SDA	Input tolerance	11.4	300	ns
$t_{f(SCL)}$	Fall time, SCL	Input tolerance	11.4	300	ns
$t_{su(SCL-SDA)STOP}$	Setup time, STOP condition, SCL rise before SDA rise delay		0.6		µs

8.9.8.1.2 I2C Switching Characteristics

over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	MAX	UNIT
f_{SCL}	SCL clock frequency	I2C clock module frequency is from 7 MHz to 12 MHz and I2C prescaler and clock divider registers are configured appropriately.		400	kHz
V_{il}	Low level input voltage			0.3 V_{DDIO}	V
V_{ih}	High level input voltage		0.7 V_{DDIO}		V
V_{hys}	Input hysteresis		0.05 V_{DDIO}		V
V_{ol}	Low level output voltage	3-mA sink current	0	0.4	V
t_{LOW}	Low period of SCL clock	I2C clock module frequency is from 7 MHz to 12 MHz and I2C prescaler and clock divider registers are configured appropriately.	1.3		µs
t_{HIGH}	High period of SCL clock	I2C clock module frequency is from 7 MHz to 12 MHz and I2C prescaler and clock divider registers are configured appropriately.	0.6		µs
I_I	Input current with an input voltage from 0.1 V_{DDIO} to 0.9 V_{DDIO} MAX		–10	10	µA

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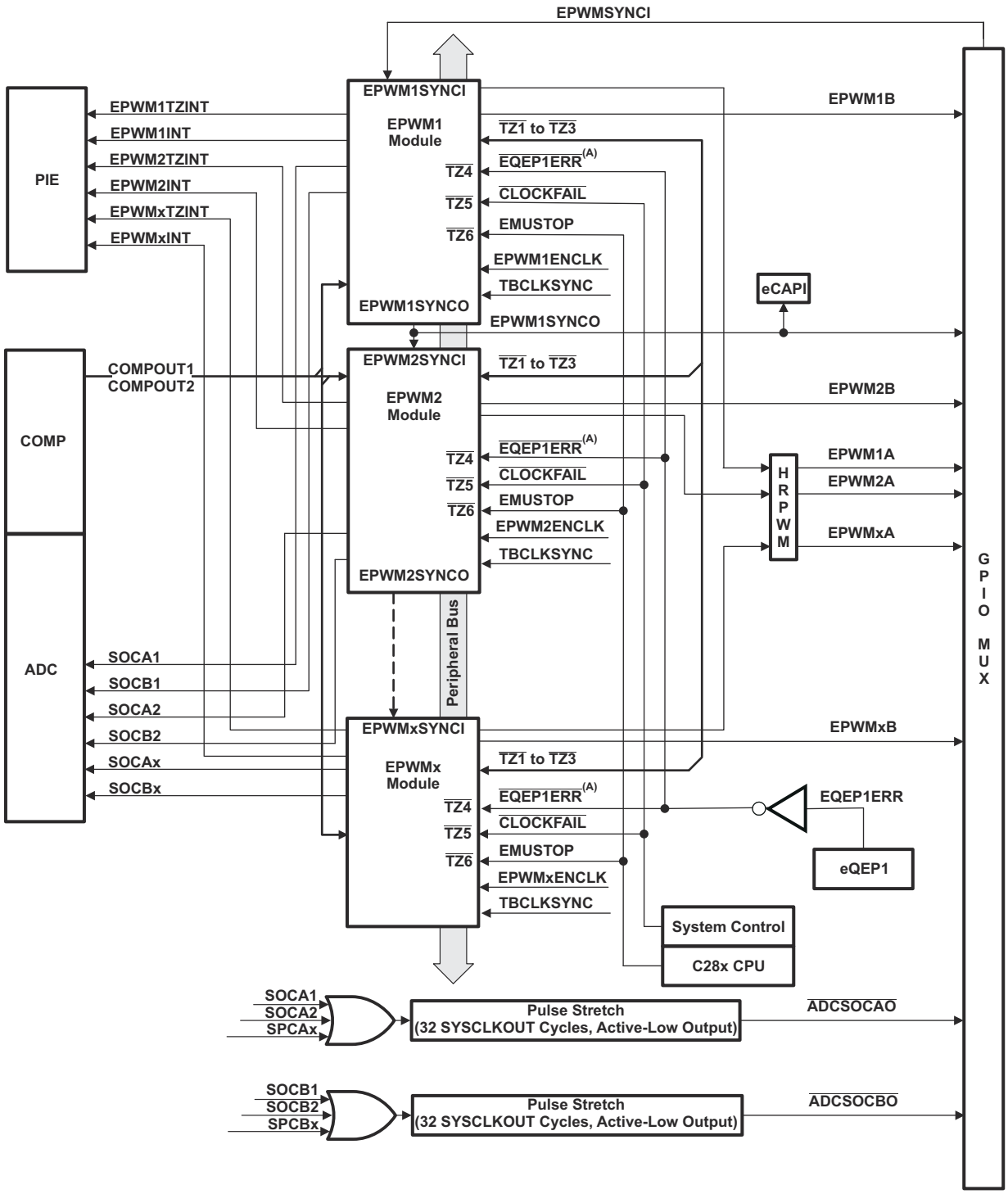
8.9.9 Enhanced Pulse Width Modulator (ePWM) Modules (ePWM1 to ePWM8)

The devices contain up to eight enhanced PWM (ePWM) modules. Figure 8-48 shows a block diagram of multiple ePWM modules. Figure 8-49 shows the signal interconnections with the ePWM.

Table 8-33 and Table 8-34 show the complete ePWM register set per module.



A. This signal exists only on devices with an eQEP1 module.

Figure 8-48. ePWM

Table 8-33. ePWM1–ePWM4 Control and Status Registers

NAME	ePWM1	ePWM2	ePWM3	ePWM4	SIZE (×16)/ #SHADOW	DESCRIPTION
TBCTL	0x6800	0x6840	0x6880	0x68C0	1/0	Time Base Control Register
TBSTS	0x6801	0x6841	0x6881	0x68C1	1/0	Time Base Status Register
TBPHSHR	0x6802	0x6842	0x6882	0x68C2	1/0	Time Base Phase HRPWM Register
TBPHS	0x6803	0x6843	0x6883	0x68C3	1/0	Time Base Phase Register
TBCTR	0x6804	0x6844	0x6884	0x68C4	1/0	Time Base Counter Register
TBPRD	0x6805	0x6845	0x6885	0x68C5	1/1	Time Base Period Register Set
TBPRDHR	0x6806	0x6846	0x6886	0x68C6	1/1	Time Base Period High-Resolution Register(1)
CMPCTL	0x6807	0x6847	0x6887	0x68C7	1/0	Counter Compare Control Register
CMPAHR	0x6808	0x6848	0x6888	0x68C8	1/1	Time Base Compare A HRPWM Register
CMPA	0x6809	0x6849	0x6889	0x68C9	1/1	Counter Compare A Register Set
CMPB	0x680A	0x684A	0x688A	0x68CA	1/1	Counter Compare B Register Set
AQCTLA	0x680B	0x684B	0x688B	0x68CB	1/0	Action Qualifier Control Register For Output A
AQCTLB	0x680C	0x684C	0x688C	0x68CC	1/0	Action Qualifier Control Register For Output B
AQSFRC	0x680D	0x684D	0x688D	0x68CD	1/0	Action Qualifier Software Force Register
AQCSFRC	0x680E	0x684E	0x688E	0x68CE	1/1	Action Qualifier Continuous S/W Force Register Set
DBCTL	0x680F	0x684F	0x688F	0x68CF	1/1	Dead-Band Generator Control Register
DBRED	0x6810	0x6850	0x6890	0x68D0	1/0	Dead-Band Generator Rising Edge Delay Count Register
DBFED	0x6811	0x6851	0x6891	0x68D1	1/0	Dead-Band Generator Falling Edge Delay Count Register
TZSEL	0x6812	0x6852	0x6892	0x68D2	1/0	Trip Zone Select Register(1)
TZDCSEL	0x6813	0x6853	0x6893	0x68D3	1/0	Trip Zone Digital Compare Register
TZCTL	0x6814	0x6854	0x6894	0x68D4	1/0	Trip Zone Control Register(1)
TZEINT	0x6815	0x6855	0x6895	0x68D5	1/0	Trip Zone Enable Interrupt Register(1)
TZFLG	0x6816	0x6856	0x6896	0x68D6	1/0	Trip Zone Flag Register (1)
TZCLR	0x6817	0x6857	0x6897	0x68D7	1/0	Trip Zone Clear Register(1)
TZFRC	0x6818	0x6858	0x6898	0x68D8	1/0	Trip Zone Force Register(1)
ETSEL	0x6819	0x6859	0x6899	0x68D9	1/0	Event Trigger Selection Register
ETPS	0x681A	0x685A	0x689A	0x68DA	1/0	Event Trigger Prescale Register
ETFLG	0x681B	0x685B	0x689B	0x68DB	1/0	Event Trigger Flag Register
ETCLR	0x681C	0x685C	0x689C	0x68DC	1/0	Event Trigger Clear Register
ETFRC	0x681D	0x685D	0x689D	0x68DD	1/0	Event Trigger Force Register
PCCTL	0x681E	0x685E	0x689E	0x68DE	1/0	PWM Chopper Control Register
HRCNFG	0x6820	0x6860	0x68A0	0x68E0	1/0	HRPWM Configuration Register(1)
HRMSTEP	0x6826	-	-	-	1/0	HRPWM MEP Step Register
HRPCTL	0x6828	0x6868	0x68A8	0x68E8	1/0	High-resolution Period Control Register(1)
TBPRDHRM	0x682A	0x686A	0x68AA	0x68EA	1/W(2)	Time Base Period HRPWM Register Mirror
TBPRDM	0x682B	0x686B	0x68AB	0x68EB	1/W(2)	Time Base Period Register Mirror
CMPAHRM	0x682C	0x686C	0x68AC	0x68EC	1/W(2)	Compare A HRPWM Register Mirror
CMPAM	0x682D	0x686D	0x68AD	0x68ED	1/W(2)	Compare A Register Mirror
DCTRIPSEL	0x6830	0x6870	0x68B0	0x68F0	1/0	Digital Compare Trip Select Register (1)
DCACTL	0x6831	0x6871	0x68B1	0x68F1	1/0	Digital Compare A Control Register(1)
DCBCTL	0x6832	0x6872	0x68B2	0x68F2	1/0	Digital Compare B Control Register(1)
DCFCTL	0x6833	0x6873	0x68B3	0x68F3	1/0	Digital Compare Filter Control Register(1)
DCCAPCT	0x6834	0x6874	0x68B4	0x68F4	1/0	Digital Compare Capture Control Register(1)

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Table 8-33. ePWM1–ePWM4 Control and Status Registers (continued)

NAME	ePWM1	ePWM2	ePWM3	ePWM4	SIZE (×16)/ #SHADOW	DESCRIPTION
DCFOFFSET	0x6835	0x6875	0x68B5	0x68F5	1/1	Digital Compare Filter Offset Register
DCFOFFSETCNT	0x6836	0x6876	0x68B6	0x68F6	1/0	Digital Compare Filter Offset Counter Register
DCFWINDOW	0x6837	0x6877	0x68B7	0x68F7	1/0	Digital Compare Filter Window Register
DCFWINDOWCNT	0x6838	0x6878	0x68B8	0x68F8	1/0	Digital Compare Filter Window Counter Register
DCCAP	0x6839	0x6879	0x68B9	0x68F9	1/1	Digital Compare Counter Capture Register

(1) Registers that are EALLOW protected.
(2) W = Write to shadow register

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Table 8-34. ePWM5–ePWM8 Control and Status Registers

NAME	ePWM5	ePWM6	ePWM7	ePWM8	SIZE (×16)/ #SHADOW	DESCRIPTION
TBCTL	0x6900	0x6940	0x6980	0x69C0	1/0	Time Base Control Register
TBSTS	0x6901	0x6941	0x6981	0x69C1	1/0	Time Base Status Register
TBPHSHR	0x6902	0x6942	0x6982	0x69C2	1/0	Time Base Phase HRPWM Register
TBPHS	0x6903	0x6943	0x6983	0x69C3	1/0	Time Base Phase Register
TBCTR	0x6904	0x6944	0x6984	0x69C4	1/0	Time Base Counter Register
TBPRD	0x6905	0x6945	0x6985	0x69C5	1/1	Time Base Period Register Set
TBPRDHR	0x6906	0x6946	0x6986	0x69C6	1/1	Time Base Period High-Resolution Register(1)
CMPCTL	0x6907	0x6947	0x6987	0x69C7	1/0	Counter Compare Control Register
CMPAHR	0x6908	0x6948	0x6988	0x69C8	1/1	Time Base Compare A HRPWM Register
CMPA	0x6909	0x6949	0x6989	0x69C9	1/1	Counter Compare A Register Set
CMPB	0x690A	0x694A	0x698A	0x69CA	1/1	Counter Compare B Register Set
AQCTLA	0x690B	0x694B	0x698B	0x69CB	1/0	Action Qualifier Control Register For Output A
AQCTLB	0x690C	0x694C	0x698C	0x69CC	1/0	Action Qualifier Control Register For Output B
AQSFRC	0x690D	0x694D	0x698D	0x69CD	1/0	Action Qualifier Software Force Register
AQCSFRC	0x690E	0x694E	0x698E	0x69CE	1/1	Action Qualifier Continuous S/W Force Register Set
DBCTL	0x690F	0x694F	0x698F	0x69CF	1/1	Dead-Band Generator Control Register
DBRED	0x6910	0x6950	0x6990	0x69D0	1/0	Dead-Band Generator Rising Edge Delay Count Register
DBFED	0x6911	0x6951	0x6991	0x69D1	1/0	Dead-Band Generator Falling Edge Delay Count Register
TZSEL	0x6912	0x6952	0x6992	0x69D2	1/0	Trip Zone Select Register(1)
TZDCSEL	0x6913	0x6953	0x6993	0x69D3	1/0	Trip Zone Digital Compare Register
TZCTL	0x6914	0x6954	0x6994	0x69D4	1/0	Trip Zone Control Register(1)
TZEINT	0x6915	0x6955	0x6995	0x69D5	1/0	Trip Zone Enable Interrupt Register(1)
TZFLG	0x6916	0x6956	0x6996	0x69D6	1/0	Trip Zone Flag Register (1)
TZCLR	0x6917	0x6957	0x6997	0x69D7	1/0	Trip Zone Clear Register(1)
TZFRC	0x6918	0x6958	0x6998	0x69D8	1/0	Trip Zone Force Register(1)
ETSEL	0x6919	0x6959	0x6999	0x69D9	1/0	Event Trigger Selection Register
ETPS	0x691A	0x695A	0x699A	0x69DA	1/0	Event Trigger Prescale Register
ETFLG	0x691B	0x695B	0x699B	0x69DB	1/0	Event Trigger Flag Register
ETCLR	0x691C	0x695C	0x699C	0x69DC	1/0	Event Trigger Clear Register
ETFRC	0x691D	0x695D	0x699D	0x69DD	1/0	Event Trigger Force Register
PCCTL	0x691E	0x695E	0x699E	0x69DE	1/0	PWM Chopper Control Register
HRCNFG	0x6920	0x6960	0x69A0	0x69E0	1/0	HRPWM Configuration Register(1)
HRMSTEP	-	-	-	-	1/0	HRPWM MEP Step Register
HRPCTL	0x6928	0x6968	0x69A8	0x69E8	1/0	High-resolution Period Control Register(1)
TBPRDHRM	0x692A	0x696A	0x69AA	0x69EA	1/W(2)	Time Base Period HRPWM Register Mirror
TBPRDM	0x692B	0x696B	0x69AB	0x69EB	1/W(2)	Time Base Period Register Mirror
CMPAHRM	0x692C	0x696C	0x69AC	0x69EC	1/W(2)	Compare A HRPWM Register Mirror
CMPAM	0x692D	0x696D	0x69AD	0x69ED	1/W(2)	Compare A Register Mirror
DCTRIPSEL	0x6930	0x6970	0x69B0	0x69F0	1/0	Digital Compare Trip Select Register (1)
DCACTL	0x6931	0x6971	0x69B1	0x69F1	1/0	Digital Compare A Control Register(1)
DCBCTL	0x6932	0x6972	0x69B2	0x69F2	1/0	Digital Compare B Control Register(1)

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Table 8-34. ePWM5–ePWM8 Control and Status Registers (continued)

NAME	ePWM5	ePWM6	ePWM7	ePWM8	SIZE (×16)/ #SHADOW	DESCRIPTION
DCFCTL	0x6933	0x6973	0x69B3	0x69F3	1/0	Digital Compare Filter Control Register(1)
DCCAPCT	0x6934	0x6974	0x69B4	0x69F4	1/0	Digital Compare Capture Control Register(1)
DCFOFFSET	0x6935	0x6975	0x69B5	0x69F5	1/1	Digital Compare Filter Offset Register
DCFOFFSETCNT	0x6936	0x6976	0x69B6	0x69F6	1/0	Digital Compare Filter Offset Counter Register
DCFWINDOW	0x6937	0x6977	0x69B7	0x69F7	1/0	Digital Compare Filter Window Register
DCFWINDOWCNT	0x6938	0x6978	0x69B8	0x69F8	1/0	Digital Compare Filter Window Counter Register
DCCAP	0x6939	0x6979	0x69B9	0x69F9	1/1	Digital Compare Counter Capture Register

(1) Registers that are EALLOW protected.
(2) W = Write to shadow register

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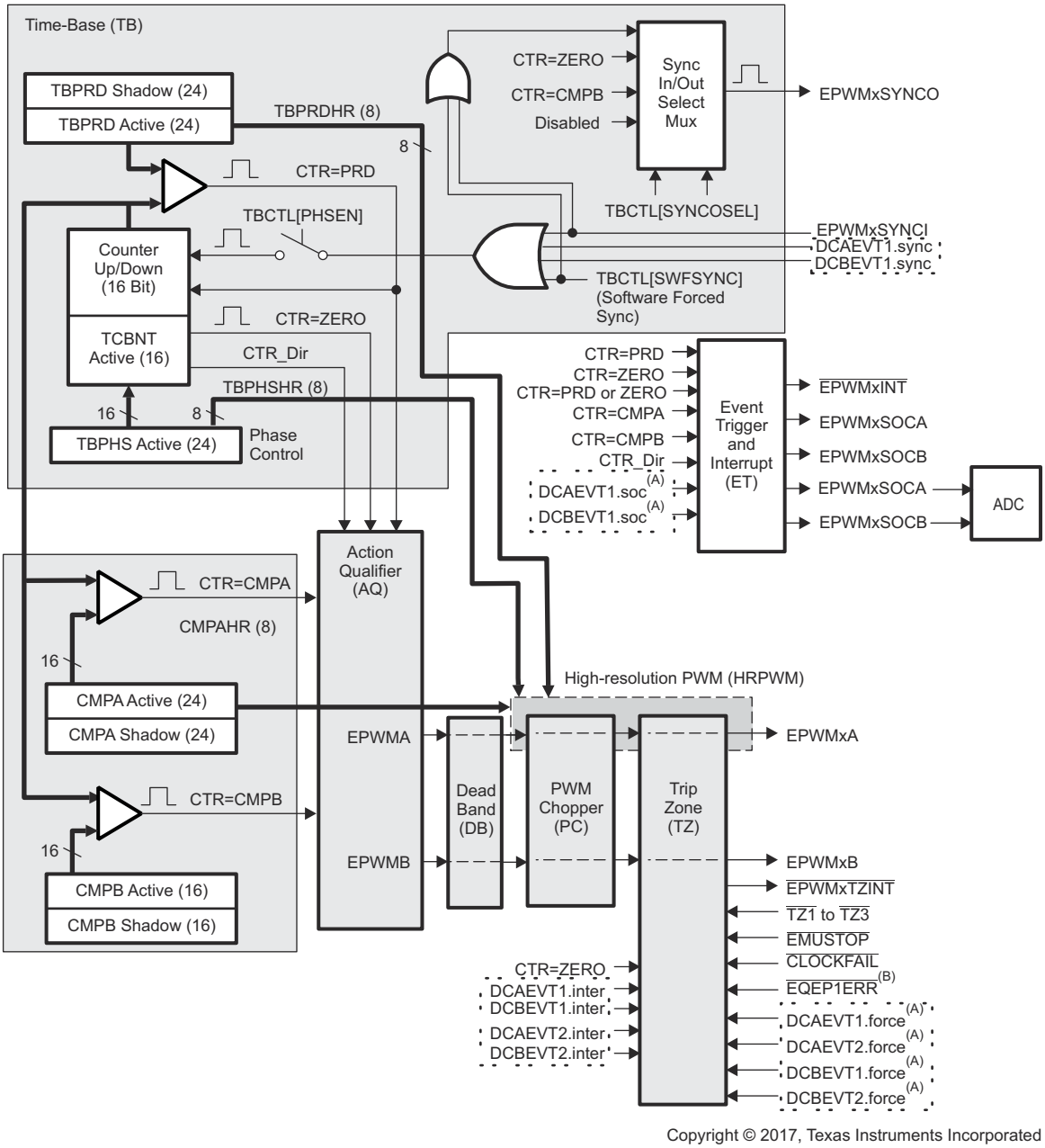

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A. These events are generated by the Type 1 ePWM digital compare (DC) submodule based on the levels of the COMPxOUT and $\overline{TZ}$ signals.

B. This signal exists only on devices with an eQEP1 module.

Figure 8-49. ePWM Submodules Showing Critical Internal Signal Interconnections

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8.9.9.1 ePWM Electrical Data/Timing

PWM refers to PWM outputs on ePWM1–8. Section 8.9.9.1.1 shows the PWM timing requirements and Section 8.9.9.1.2, switching characteristics.

8.9.9.1.1 ePWM Timing Requirements

			MIN(1)	MAX	UNIT
$t_{w(SYCIN)}$	Sync input pulse width	Asynchronous	$2t_{c(SCO)}$		cycles
		Synchronous	$2t_{c(SCO)}$		cycles
		With input qualifier	$1t_{c(SCO)} + t_{w(IQSW)}$		cycles

(1) For an explanation of the input qualifier parameters, see Section 8.9.15.1.2.1.

8.9.9.1.2 ePWM Switching Characteristics

over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	MAX	UNIT
$t_{w(PWM)}$	Pulse duration, PWMx output high/low		33.33		ns
$t_{w(SYNCOUT)}$	Sync output pulse width		$8t_{c(SCO)}$		cycles
$t_{d(PWM)tza}$	Delay time, trip input active to PWM forced high Delay time, trip input active to PWM forced low	no pin load		25	ns
$t_{d(TZ-PWM)HZ}$	Delay time, trip input active to PWM Hi-Z			20	ns

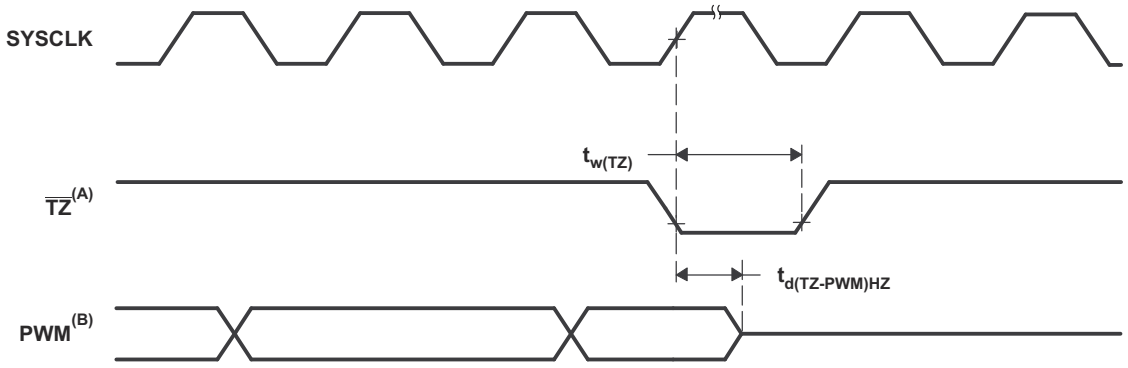
8.9.9.2 Trip-Zone Input Timing

Section 8.9.9.2.1 lists the trip-zone input timing requirements. Figure 8-50 shows the PWM Hi-Z characteristics.

8.9.9.2.1 Trip-Zone Input Timing Requirements

			MIN(1)	MAX	UNIT
$t_{w(TZ)}$	Pulse duration, $\overline{TZ}$x input low	Asynchronous	$2t_{c(TBCLK)}$		cycles
		Synchronous	$2t_{c(TBCLK)}$		cycles
		With input qualifier	$2t_{c(TBCLK)} + t_{w(IQSW)}$		cycles

(1) For an explanation of the input qualifier parameters, see Section 8.9.15.1.2.1.



A. $\overline{TZ}$ - $\overline{TZ1}$, $\overline{TZ2}$, $\overline{TZ3}$, $\overline{TZ4}$, $\overline{TZ5}$, $\overline{TZ6}$

B. PWM refers to all the PWM pins in the device. The state of the PWM pins after $\overline{TZ}$ is taken high depends on the PWM recovery software.

Figure 8-50. PWM Hi-Z Characteristics

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8.9.10 High-Resolution PWM (HRPWM)

This module combines multiple delay lines in a single module and a simplified calibration system by using a dedicated calibration delay line. For each ePWM module there is one HR delay line.

The HRPWM module offers PWM resolution (time granularity) that is significantly better than what can be achieved using conventionally derived digital PWM methods. The key points for the HRPWM module are:

- Significantly extends the time resolution capabilities of conventionally derived digital PWM
- This capability can be used in both single edge (duty cycle and phase-shift control) as well as dual edge control for frequency/period modulation.
- Finer time granularity control or edge positioning is controlled through extensions to the Compare A and Phase registers of the ePWM module.
- HRPWM capabilities, when available on a particular device, are offered only on the A signal path of an ePWM module (that is, on the EPWMxA output). EPWMxB output has conventional PWM capabilities.

Note

The minimum SYSCLKOUT frequency allowed for HRPWM is 60 MHz.

Note

When dual-edge high-resolution is enabled (high-resolution period mode), the PWMxB channel will have ±1–2 TBCLK cycles of jitter on the output.

8.9.10.1 HRPWM Electrical Data/Timing

Section 8.9.10.1.1 shows the high-resolution PWM switching characteristics.

8.9.10.1.1 High-Resolution PWM Characteristics

PARAMETER(1)	MIN	TYP	MAX	UNIT
Micro Edge Positioning (MEP) step size(2)		150	310	ps

(1) The HRPWM operates at a minimum SYSCLKOUT frequency of 60 MHz.
(2) The MEP step size will be largest at high temperature and minimum voltage on V_{DD}. MEP step size will increase with higher temperature and lower voltage and decrease with lower temperature and higher voltage.
Applications that use the HRPWM feature should use MEP Scale Factor Optimizer (SFO) estimation software functions. See the TI software libraries for details of using SFO function in end applications. SFO functions help to estimate the number of MEP steps per SYSCLKOUT period dynamically while the HRPWM is in operation.

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8.9.11 Enhanced Capture Module (eCAP1)

The device contains an enhanced capture (eCAP) module. Figure 8-51 shows a functional block diagram of a module.

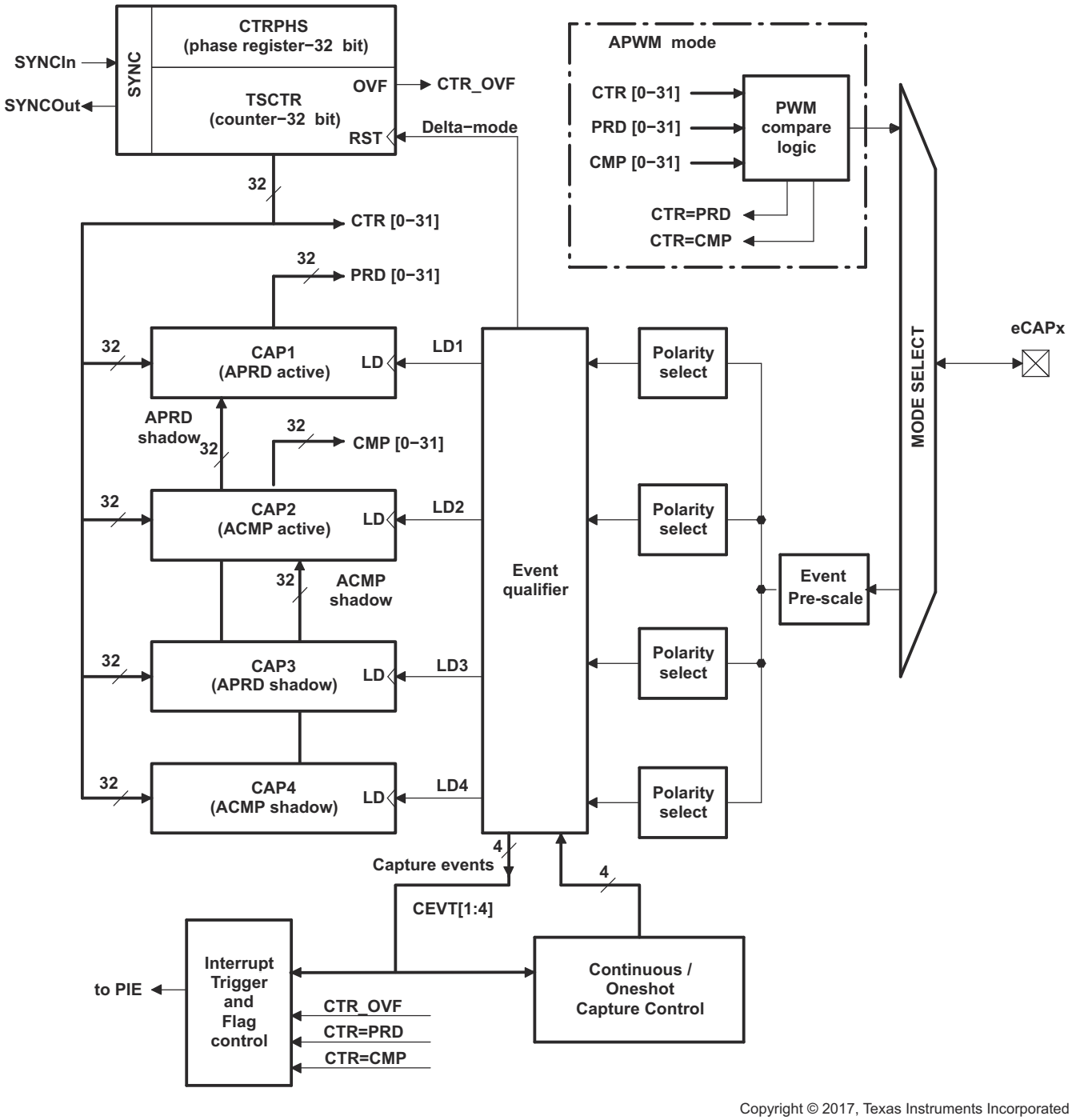

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Figure 8-51. eCAP Functional Block Diagram

The eCAP module is clocked at the SYSCLKOUT rate.

The clock enable bits (ECAP1 ENCLK) in the PCLKCR1 register turn off the eCAP module individually (for low-power operation). Upon reset, ECAP1ENCLK is set to low, indicating that the peripheral clock is off.

Table 8-35. eCAP Control and Status Registers

NAME	eCAP1	eCAP2	eCAP3	SIZE (×16)	EALLOW PROTECTED	DESCRIPTION
TSCTR	0x6A00	0x6A20	0x6A40	2	No	Timestamp Counter
CTRPHS	0x6A02	0x6A22	0x6A42	2	No	Counter Phase Offset Value Register
CAP1	0x6A04	0x6A24	0x6A44	2	No	Capture 1 Register
CAP2	0x6A06	0x6A26	0x6A46	2	No	Capture 2 Register
CAP3	0x6A08	0x6A28	0x6A48	2	No	Capture 3 Register
CAP4	0x6A0A	0x6A2A	0x6A4A	2	No	Capture 4 Register
Reserved	0x6A0C to 0x6A12	0x6A2C to 0x6A32	0x6A4C to 0x6A52	8	No	Reserved
ECCTL1	0x6A14	0x6A34	0x6A54	1	No	Capture Control Register 1
ECCTL2	0x6A15	0x6A35	0x6A55	1	No	Capture Control Register 2
ECEINT	0x6A16	0x6A36	0x6A56	1	No	Capture Interrupt Enable Register
ECFLG	0x6A17	0x6A37	0x6A57	1	No	Capture Interrupt Flag Register
ECCLR	0x6A18	0x6A38	0x6A58	1	No	Capture Interrupt Clear Register
ECFRC	0x6A19	0x6A39	0x6A59	1	No	Capture Interrupt Force Register
Reserved	0x6A1A to 0x6A1F	0x6A3A to 0x6A3F	0x6A5A to 0x6A5F	6	No	Reserved

8.9.11.1 eCAP Electrical Data/Timing

Section 8.9.11.1.1 shows the eCAP timing requirement and Section 8.9.11.1.2 shows the eCAP switching characteristics.

8.9.11.1.1 Enhanced Capture (eCAP) Timing Requirement

			MIN[1]	MAX	UNIT
$t_{w(CAP)}$	Capture input pulse width	Asynchronous	$2t_{c(SCO)}$		cycles
		Synchronous	$2t_{c(SCO)}$		
		With input qualifier	$1t_{c(SCO)} + t_{w(IQSW)}$		

(1) For an explanation of the input qualifier parameters, see Section 8.9.15.1.2.1.

8.9.11.1.2 eCAP Switching Characteristics

over recommended operating conditions (unless otherwise noted)

PARAMETER		MIN	MAX	UNIT
$t_{w(APWM)}$	Pulse duration, APWMx output high/low	20		ns

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8.9.12 High-Resolution Capture Modules (HRCAP1 to HRCAP4)

The device contains up to four high-resolution capture (HRCAP) modules. The High-Resolution Capture (HRCAP) module measures the difference between external pulses with a typical resolution of 300 ps.

Uses for the HRCAP include:

- Capacitive touch applications
- High-resolution period and duty cycle measurements of pulse train cycles
- Instantaneous speed measurements
- Instantaneous frequency measurements
- Voltage measurements across an isolation boundary
- Distance measurement (sonar) and scanning

The HRCAP module features include:

- Pulse width capture in either non-high-resolution or high-resolution modes
- Difference (Delta) mode pulse width capture
- Typical high-resolution capture on the order of 300 ps resolution on each edge
- Interrupt on either falling or rising edge
- Continuous mode capture of pulse widths in 2-deep buffer
- Calibration logic for precision high-resolution capture
- All of the above resources are dedicated to a single input pin
- HRCAP calibration software library supplied by TI is used for both calibration and calculating fractional pulse widths

The HRCAP module includes one capture channel in addition to a high-resolution calibration block, which connects internally to the last available ePWMxA HRPWM channel when calibrating (that is, if there are eight ePWMs with HRPWM capability, it will be HRPWM8A).

Each HRCAP channel has the following independent key resources:

- Dedicated input capture pin
- 16-bit HRCAP clock which is either equal to the PLL2 output frequency (asynchronous to SYSCLK2) or SYSCLKOUT
- High-resolution pulse width capture in a 2-deep buffer

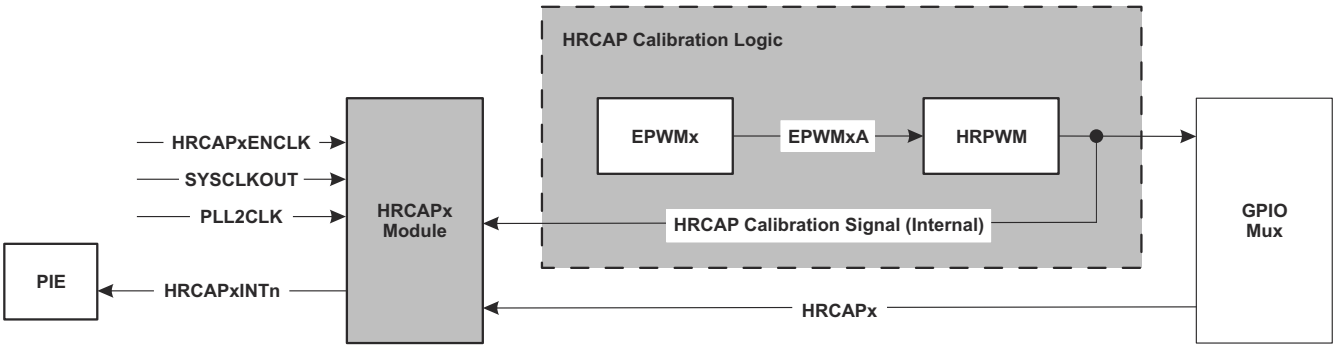

Figure 8-52. HRCAP Functional Block Diagram

Table 8-36. HRCAP Registers

NAME	HRCAP1	HRCAP2	HRCAP3	HRCAP4	SIZE (×16)	DESCRIPTION
HCCTL	0x6AC0	0x6AE0	0x6C80	0x6CA0	1	HRCAP Control Register(1)
HCIFR	0x6AC1	0x6AE1	0x6C81	0x6CA1	1	HRCAP Interrupt Flag Register
HCICLR	0x6AC2	0x6AE2	0x6C82	0x6CA2	1	HRCAP Interrupt Clear Register(1)
HCIFRC	0x6AC3	0x6AE3	0x6C83	0x6CA3	1	HRCAP Interrupt Force Register(1)
HCCOUNTER	0x6AC4	0x6AE4	0x6C84	0x6CA4	1	HRCAP 16-bit Counter Register
HCCAPCNTRISE0	0x6AD0	0x6AF0	0x6C90	0x6CB0	1	HRCAP Capture Counter on Rising Edge 0 Register
HCCAPCNTFALL0	0x6AD2	0x6AF2	0x6C92	0x6CB2	1	HRCAP Capture Counter on Falling Edge 0 Register
HCCAPCNTRISE1	0x6AD8	0x6AF8	0x6C98	0x6CB8	1	HRCAP Capture Counter on Rising Edge 1 Register
HCCAPCNTFALL1	0x6ADA	0x6AFA	0x6C9A	0x6CBA	1	HRCAP Capture Counter on Falling Edge 1 Register

(1) Registers that are EALLOW-protected.

8.9.12.1 HRCAP Electrical Data/Timing

8.9.12.1.1 High-Resolution Capture (HRCAP) Timing Requirements

		MIN	NOM	MAX	UNIT
$t_{c(HCCAPCLK)}$	Cycle time, HRCAP capture clock	8.333		10.204	ns
$t_{w(HRCAP)}$	Pulse width, HRCAP capture	$7t_{c(HCCAPCLK)}$ (1)			ns
	HRCAP step size(2)		300		ps

(1) The listed minimum pulse width does not take into account the limitation that all relevant HCCAP registers must be read and RISE/FALL event flags cleared within the pulse width to ensure valid capture data.
(2) HRCAP step size will increase with low voltage and high temperature and decrease with high voltage and low temperature. Applications that use the HRCAP in high-resolution mode should use the HRCAP calibration functions to dynamically calibrate for varying operating conditions.

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8.9.13 Enhanced Quadrature Encoder Modules (eQEP1, eQEP2)

The device contains up to two enhanced quadrature encoder (eQEP) modules. Table 8-37 provides a summary of the eQEP registers.

Table 8-37. eQEP Control and Status Registers

NAME	eQEP1 ADDRESS	eQEP2 ADDRESS	eQEP1 SIZE(×16)/ #SHADOW	REGISTER DESCRIPTION
QPOSCNT	0x6B00	0x6B40	2/0	eQEP Position Counter
QPOSINIT	0x6B02	0x6B42	2/0	eQEP Initialization Position Count
QPOSMAX	0x6B04	0x6B44	2/0	eQEP Maximum Position Count
QPOSCMP	0x6B06	0x6B46	2/1	eQEP Position-compare
QPOSILAT	0x6B08	0x6B48	2/0	eQEP Index Position Latch
QPOSSLAT	0x6B0A	0x6B4A	2/0	eQEP Strobe Position Latch
QPOSLAT	0x6B0C	0x6B4C	2/0	eQEP Position Latch
QUTMR	0x6B0E	0x6B4E	2/0	eQEP Unit Timer
QUPRD	0x6B10	0x6B50	2/0	eQEP Unit Period Register
QWDTMR	0x6B12	0x6B52	1/0	eQEP Watchdog Timer
QWDPRD	0x6B13	0x6B53	1/0	eQEP Watchdog Period Register
QDECCTL	0x6B14	0x6B54	1/0	eQEP Decoder Control Register
QEPCTL	0x6B15	0x6B55	1/0	eQEP Control Register
QCAPCTL	0x6B16	0x6B56	1/0	eQEP Capture Control Register
QPOSCTL	0x6B17	0x6B57	1/0	eQEP Position-compare Control Register
QEINT	0x6B18	0x6B58	1/0	eQEP Interrupt Enable Register
QFLG	0x6B19	0x6B59	1/0	eQEP Interrupt Flag Register
QCLR	0x6B1A	0x6B5A	1/0	eQEP Interrupt Clear Register
QFRC	0x6B1B	0x6B5B	1/0	eQEP Interrupt Force Register
QEPSTS	0x6B1C	0x6B5C	1/0	eQEP Status Register
QCTMR	0x6B1D	0x6B5D	1/0	eQEP Capture Timer
QCPRD	0x6B1E	0x6B5E	1/0	eQEP Capture Period Register
QCTMRLAT	0x6B1F	0x6B5F	1/0	eQEP Capture Timer Latch
QCPRDLAT	0x6B20	0x6B60	1/0	eQEP Capture Period Latch
Reserved	0x6B21 to 0x6B3F	0x6B61 to 0x6B7F	31/0	

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Figure 8-53 shows the block diagram of the eQEP module.

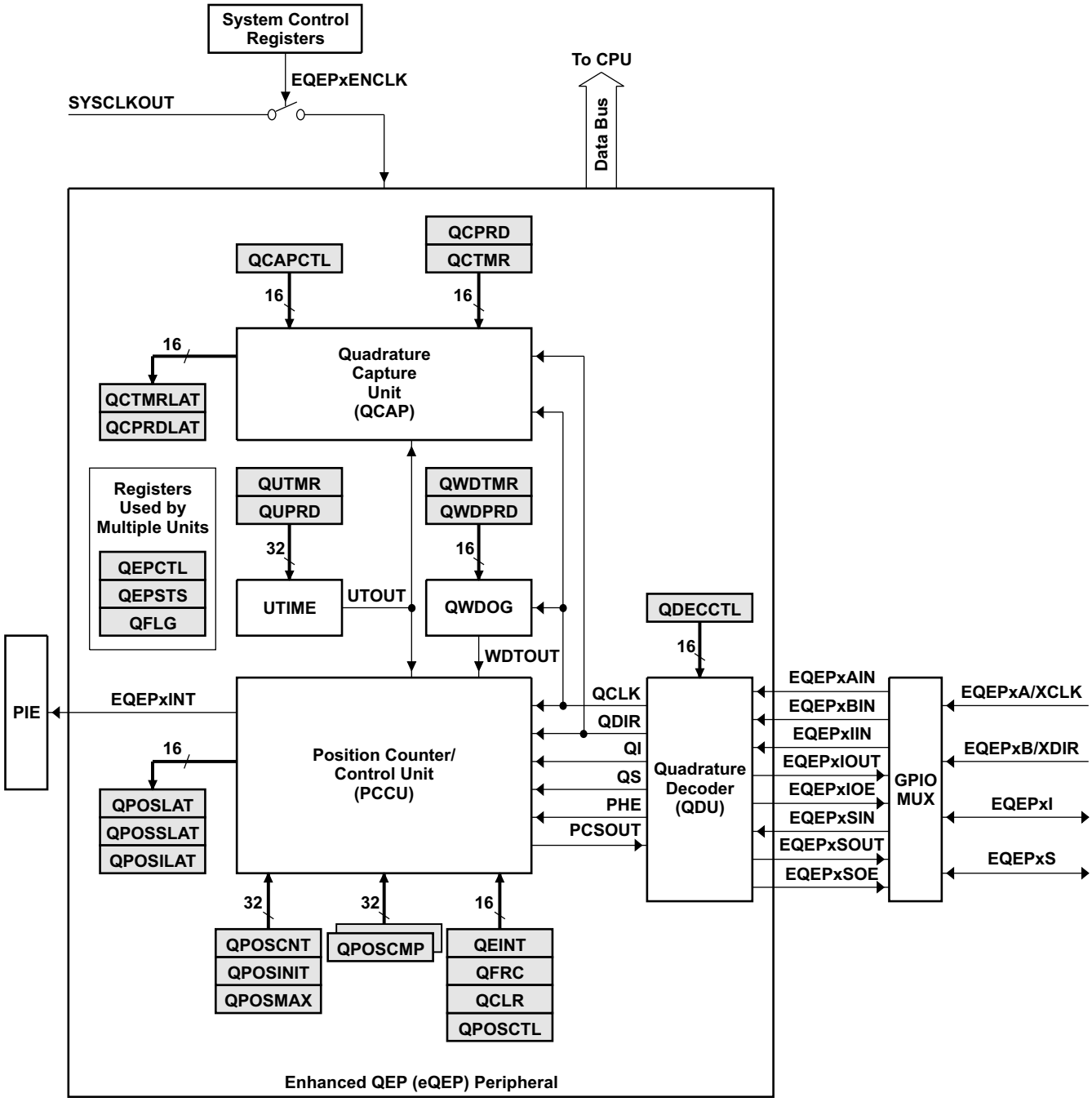

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Figure 8-53. eQEP Functional Block Diagram

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8.9.13.1 eQEP Electrical Data/Timing

Section 8.9.13.1.1 shows the eQEP timing requirement and Section 8.9.13.1.2 shows the eQEP switching characteristics.

8.9.13.1.1 Enhanced Quadrature Encoder Pulse (eQEP) Timing Requirements

			MIN(1)	MAX	UNIT
$t_{w(QEPP)}$	QEP input period	Asynchronous(2)/Synchronous	$2t_{c(SCO)}$		cycles
		With input qualifier	$2[1t_{c(SCO)} + t_{w(IQSW)}]$		
$t_{w(INDEXH)}$	QEP Index Input High time	Asynchronous(2)/Synchronous	$2t_{c(SCO)}$		cycles
		With input qualifier	$2t_{c(SCO)} + t_{w(IQSW)}$		
$t_{w(INDEXL)}$	QEP Index Input Low time	Asynchronous(2)/Synchronous	$2t_{c(SCO)}$		cycles
		With input qualifier	$2t_{c(SCO)} + t_{w(IQSW)}$		
$t_{w(STROBH)}$	QEP Strobe High time	Asynchronous(2)/Synchronous	$2t_{c(SCO)}$		cycles
		With input qualifier	$2t_{c(SCO)} + t_{w(IQSW)}$		
$t_{w(STROBL)}$	QEP Strobe Input Low time	Asynchronous(2)/Synchronous	$2t_{c(SCO)}$		cycles
		With input qualifier	$2t_{c(SCO)} + t_{w(IQSW)}$		

(1) For an explanation of the input qualifier parameters, see Section 8.9.15.1.2.1.
(2) Refer to the *TMS320F2806x MCUs Silicon Errata* for limitations in the asynchronous mode.

8.9.13.1.2 eQEP Switching Characteristics

over recommended operating conditions (unless otherwise noted)

PARAMETER		MIN	MAX	UNIT
$t_{d(CNTR)xin}$	Delay time, external clock to counter increment		$4t_{c(SCO)}$	cycles
$t_{d(PCS-OUT)QEP}$	Delay time, QEP input edge to position compare sync output		$6t_{c(SCO)}$	cycles

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8.9.14 JTAG Port

On the 2806x device, the JTAG port is reduced to five pins ($\overline{\text{TRST}}$, TCK, TDI, TMS, TDO). TCK, TDI, TMS, and TDO pins are also GPIO pins. The $\overline{\text{TRST}}$ signal selects either JTAG or GPIO operating mode for the pins in Figure 8-54. During debug, the GPIO function of these pins are not available. If the GPIO38/TCK/XCLKIN pin is used to provide an external clock, an alternate clock source should be used to clock the device during debug because this pin will be needed for the TCK function.

Note

In 2806x devices, the JTAG pins may also be used as GPIO pins. Care should be taken in the board design to ensure that the circuitry connected to these pins do not affect the debug capabilities of the JTAG pin function. Any circuitry connected to these pins should not prevent the debug probe from driving (or being driven by) the JTAG pins for successful debug.

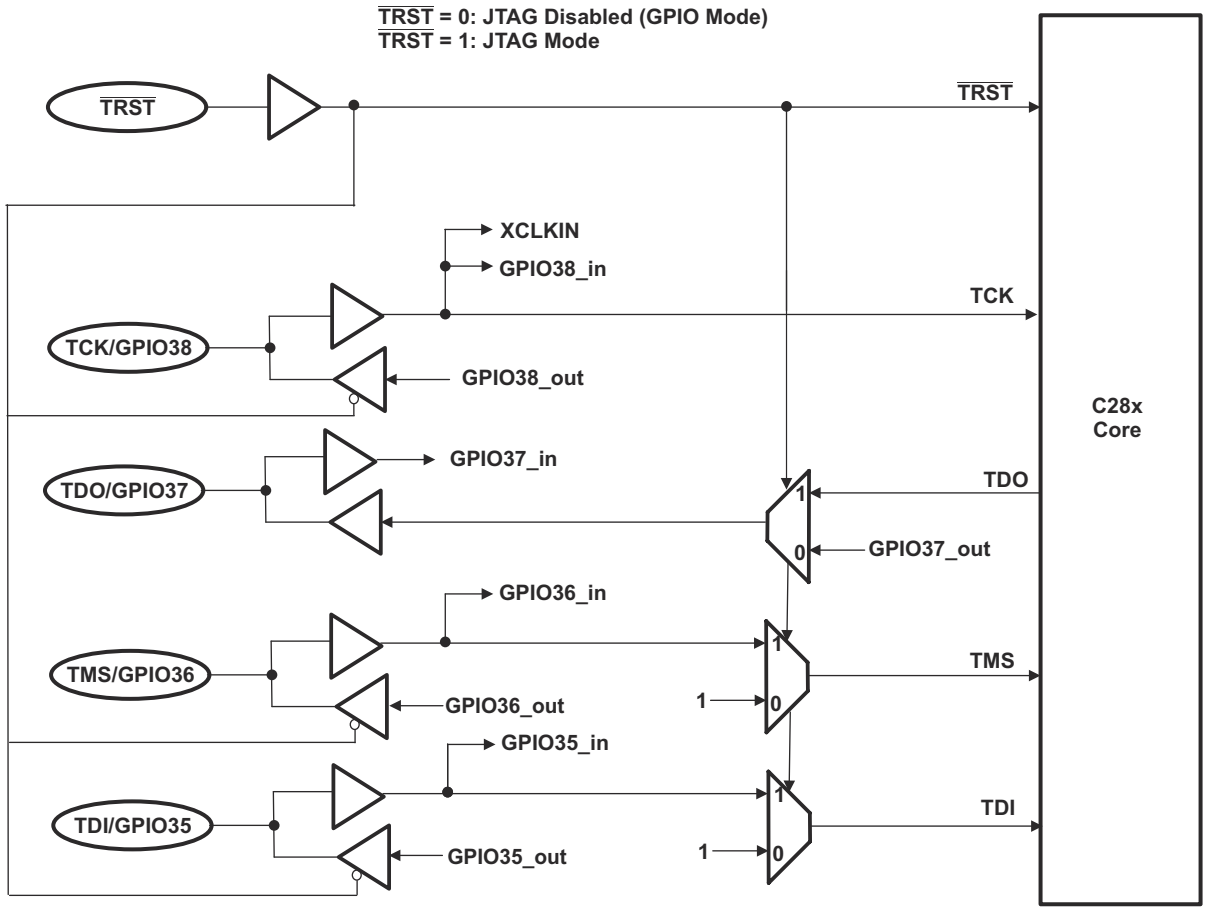

Figure 8-54. JTAG/GPIO Multiplexing

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8.9.15 General-Purpose Input/Output (GPIO) MUX

The GPIO MUX can multiplex up to three independent peripheral signals on a single GPIO pin in addition to providing individual pin bit-banging I/O capability.

The device supports 45 GPIO pins. The GPIO control and data registers are mapped to Peripheral Frame 1 to enable 32-bit operations on the registers (along with 16-bit operations). Table 8-38 shows the GPIO register mapping.

Table 8-38. GPIO Registers

NAME	ADDRESS	SIZE (×16)	DESCRIPTION
GPIO CONTROL REGISTERS (EALLOW PROTECTED)			
GPACTRL	0x6F80	2	GPIO A Control Register (GPIO0 to 31)
GPAQSEL1	0x6F82	2	GPIO A Qualifier Select 1 Register (GPIO0 to 15)
GPAQSEL2	0x6F84	2	GPIO A Qualifier Select 2 Register (GPIO16 to 31)
GPAMUX1	0x6F86	2	GPIO A MUX 1 Register (GPIO0 to 15)
GPAMUX2	0x6F88	2	GPIO A MUX 2 Register (GPIO16 to 31)
GPADIR	0x6F8A	2	GPIO A Direction Register (GPIO0 to 31)
GPAPUD	0x6F8C	2	GPIO A Pullup Disable Register (GPIO0 to 31)
GPBCTRL	0x6F90	2	GPIO B Control Register (GPIO32 to 44)
GPBQSEL1	0x6F92	2	GPIO B Qualifier Select 1 Register (GPIO32 to 44)
GPBQSEL2	0x6F94	2	GPIO B Qualifier Select 2 Register
GPBMUX1	0x6F96	2	GPIO B MUX 1 Register (GPIO32 to 44)
GPBMUX2	0x6F98	2	GPIO B MUX 2 Register (GPIO50 to 58)
GPBDIR	0x6F9A	2	GPIO B Direction Register (GPIO32 to 44)
GPBPUD	0x6F9C	2	GPIO B Pullup Disable Register (GPIO32 to 44)
AIOMUX1	0x6FB6	2	Analog, I/O mux 1 register (AIO0 to AIO15)
AIODIR	0x6FBA	2	Analog, I/O Direction Register (AIO0 to AIO15)
GPIO DATA REGISTERS (NOT EALLOW PROTECTED)			
GPADAT	0x6FC0	2	GPIO A Data Register (GPIO0 to 31)
GPASET	0x6FC2	2	GPIO A Data Set Register (GPIO0 to 31)
GPACLEAR	0x6FC4	2	GPIO A Data Clear Register (GPIO0 to 31)
GPATOGGLE	0x6FC6	2	GPIO A Data Toggle Register (GPIO0 to 31)
GPBDAT	0x6FC8	2	GPIO B Data Register (GPIO32 to 44)
GPBSET	0x6FCA	2	GPIO B Data Set Register (GPIO32 to 44)
GPBCLEAR	0x6FCC	2	GPIO B Data Clear Register (GPIO32 to 44)
GPBTOGGLE	0x6FCE	2	GPIO B Data Toggle Register (GPIO32 to 44)
AIODAT	0x6FD8	2	Analog I/O Data Register (AIO0 to AIO15)
AIOSET	0x6FDA	2	Analog I/O Data Set Register (AIO0 to AIO15)
AIOCLEAR	0x6FDC	2	Analog I/O Data Clear Register (AIO0 to AIO15)
AIOTOGGLE	0x6FDE	2	Analog I/O Data Toggle Register (AIO0 to AIO15)
GPIO INTERRUPT AND LOW-POWER MODES SELECT REGISTERS (EALLOW PROTECTED)			
GPIOXINT1SEL	0x6FE0	1	XINT1 GPIO Input Select Register (GPIO0 to 31)
GPIOXINT2SEL	0x6FE1	1	XINT2 GPIO Input Select Register (GPIO0 to 31)
GPIOXINT3SEL	0x6FE2	1	XINT3 GPIO Input Select Register (GPIO0 to 31)
GPIOLPMSEL	0x6FE8	2	LPM GPIO Select Register (GPIO0 to 31)

Note

There is a two-SYSCLKOUT cycle delay from when the write to the GPxMUXn/AIOMUXn and GPxQSELn registers occurs to when the action is valid.

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Table 8-39. GPIOA MUX

	DEFAULT AT RESET PRIMARY I/O FUNCTION(1) (2)	PERIPHERAL SELECTION 1	PERIPHERAL SELECTION 2	PERIPHERAL SELECTION 3
GPAMUX1 REGISTER BITS	**(GPAMUX1 BITS = 00)**	**(GPAMUX1 BITS = 01)**	**(GPAMUX1 BITS = 10)**	**(GPAMUX1 BITS = 11)**
1-0	GPIO0	EPWM1A (O)	Reserved	Reserved
3-2	GPIO1	EPWM1B (O)	Reserved	COMP1OUT (O)
5-4	GPIO2	EPWM2A (O)	Reserved	Reserved
7-6	GPIO3	EPWM2B (O)	SPISOMIA (I/O)	COMP2OUT (O)
9-8	GPIO4	EPWM3A (O)	Reserved	Reserved
11-10	GPIO5	EPWM3B (O)	SPISIMOA (I/O)	ECAP1 (I/O)
13-12	GPIO6	EPWM4A (O)	EPWMSYNCI (I)	EPWMSYNCO (O)
15-14	GPIO7	EPWM4B (O)	SCIRXDA (I)	ECAP2 (I/O)
17-16	GPIO8	EPWM5A (O)	Reserved	$\overline{\text{ADCSOCAO}}$ (O)
19-18	GPIO9	EPWM5B (O)	SCITXDB (O)	ECAP3 (I/O)
21-20	GPIO10	EPWM6A (O)	Reserved	$\overline{\text{ADCSOCBO}}$ (O)
23-22	GPIO11	EPWM6B (O)	SCIRXDB (I)	ECAP1 (I/O)
25-24	GPIO12	$\overline{\text{TZ1}}$ (I)	SCITXDA (O)	SPISIMOB (I/O)
27-26	GPIO13	$\overline{\text{TZ2}}$ (I)	Reserved	SPISOMIB (I/O)
29-28	GPIO14	$\overline{\text{TZ3}}$ (I)	SCITXDB (O)	SPICLKB (I/O)
31-30	GPIO15	ECAP2 (I/O)	SCIRXDB (I)	$\overline{\text{SPISTEB}}$ (I/O)
GPAMUX2 REGISTER BITS	**(GPAMUX2 BITS = 00)**	**(GPAMUX2 BITS = 01)**	**(GPAMUX2 BITS = 10)**	**(GPAMUX2 BITS = 11)**
1-0	GPIO16	SPISIMOA (I/O)	Reserved	$\overline{\text{TZ2}}$ (I)
3-2	GPIO17	SPISOMIA (I/O)	Reserved	$\overline{\text{TZ3}}$ (I)
5-4	GPIO18	SPICLKA (I/O)	SCITXDB (O)	XCLKOUT (O)
7-6	GPIO19/XCLKIN	$\overline{\text{SPISTEA}}$ (I/O)	SCIRXDB (I)	ECAP1 (I/O)
9-8	GPIO20	EQEP1A (I)	MDXA (O)	COMP1OUT (O)
11-10	GPIO21	EQEP1B (I)	MDRA (I)	COMP2OUT (O)
13-12	GPIO22	EQEP1S (I/O)	MCLKXA (I/O)	SCITXDB (O)
15-14	GPIO23	EQEP1I (I/O)	MFSXA (I/O)	SCIRXDB (I)
17-16	GPIO24	ECAP1 (I/O)	EQEP2A(3) (I)	SPISIMOB (I/O)
19-18	GPIO25	ECAP2 (I/O)	EQEP2B(3) (I)	SPISOMIB (I/O)
21-20	GPIO26(4)	ECAP3 (I/O)	EQEP2I(3) (I/O)	SPICLKB (I/O)
23-22	GPIO27(4)	HRCAP2 (I)	EQEP2S(3) (I/O)	$\overline{\text{SPISTEB}}$ (I/O)
25-24	GPIO28	SCIRXDA (I)	SDAA (I/OD)	$\overline{\text{TZ2}}$ (I)
27-26	GPIO29	SCITXDA (O)	SCLA (I/OD)	$\overline{\text{TZ3}}$ (I)
29-28	GPIO30	CANRXA (I)	EQEP2I(3) (I/O)	EPWM7A (O)
31-30	GPIO31	CANTXA (O)	EQEP2S(3) (I/O)	EPWM8A (O)

(1) The word "Reserved" means that there is no peripheral assigned to this GPxMUX1/2 register setting. Should it be selected, the state of the pin will be undefined and the pin may be driven. This selection is a reserved configuration for future expansion.
(2) I = Input, O = Output, OD = Open Drain
(3) The eQEP2 peripheral is not available on the 80-pin PN or PFP package.
(4) To enable the USB functionality on GPIO26 (USB0DP, positive differential half of the USB signal) and GPIO27 (USB0DM, negative differential half of the USB signal), set the USBIOEN bit in the GPACTRL2 register. Depending on your USB application, additional pins may be required to maintain compliance with the USB 2.0 Specification. For more information, see the Universal Serial Bus (USB) Controller chapter of the *TMS320x2806x Technical Reference Manual* .

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Table 8-40. GPIOB MUX

	DEFAULT AT RESET PRIMARY I/O FUNCTION(1) (2)	PERIPHERAL SELECTION 1	PERIPHERAL SELECTION 2	PERIPHERAL SELECTION 3
GPBMUX1 REGISTER BITS	(GPBMUX1 BITS = 00)	(GPBMUX1 BITS = 01)	(GPBMUX1 BITS = 10)	(GPBMUX1 BITS = 11)
1-0	GPIO32	SDAA (I/OD)	EPWMSYNCI (I)	ADCSOCAO (O)
3-2	GPIO33	SCLA (I/OD)	EPWMSYNCO (O)	ADCSOCBO (O)
5-4	GPIO34	COMP2OUT (O)	Reserved	COMP3OUT (O)
7-6	GPIO35 (TDI)	Reserved	Reserved	Reserved
9-8	GPIO36 (TMS)	Reserved	Reserved	Reserved
11-10	GPIO37 (TDO)	Reserved	Reserved	Reserved
13-12	GPIO38/XCLKIN (TCK)	Reserved	Reserved	Reserved
15-14	GPIO39	Reserved	Reserved	Reserved
17-16	GPIO40(3)	EPWM7A (O)	SCITXDB (O)	Reserved
19-18	GPIO41(3)	EPWM7B (O)	SCIRXDB (I)	Reserved
21-20	GPIO42(3)	EPWM8A (O)	TZ1 (I)	COMP1OUT (O)
23-22	GPIO43(3)	EPWM8B (O)	TZ2 (I)	COMP2OUT (O)
25-24	GPIO44(3)	MFSRA (I/O)	SCIRXDB (I)	EPWM7B (O)
27-26	Reserved	Reserved	Reserved	Reserved
29-28	Reserved	Reserved	Reserved	Reserved
31-30	Reserved	Reserved	Reserved	Reserved
GPBMUX2 REGISTER BITS	**(GPBMUX2 BITS = 00)**	**(GPBMUX2 BITS = 01)**	**(GPBMUX2 BITS = 10)**	**(GPBMUX2 BITS = 11)**
1-0	Reserved	Reserved	Reserved	Reserved
3-2	Reserved	Reserved	Reserved	Reserved
5-4	GPIO50(3)	EQEP1A (I)	MDXA (O)	TZ1 (I)
7-6	GPIO51(3)	EQEP1B (I)	MDRA (I)	TZ2 (I)
9-8	GPIO52(3)	EQEP1S (I/O)	MCLKXA (I/O)	TZ3 (I)
11-10	GPIO53(3)	EQEP1I (I/O)	MFSXA (I/O)	Reserved
13-12	GPIO54(3)	SPISIMOA (I/O)	EQEP2A (I)	HRCAP1 (I)
15-14	GPIO55(3)	SPISOMIA (I/O)	EQEP2B (I)	HRCAP2 (I)
17-16	GPIO56(3)	SPICLKA (I/O)	EQEP2I (I/O)	HRCAP3 (I)
19-18	GPIO57(3)	SPISTEA (I/O)	EQEP2S (I/O)	HRCAP4 (I)
21-20	GPIO58(3)	MCLKRA (I/O)	SCITXDB (O)	EPWM7A (O)
23-22	Reserved	Reserved	Reserved	Reserved
25-24	Reserved	Reserved	Reserved	Reserved
27-26	Reserved	Reserved	Reserved	Reserved
29-28	Reserved	Reserved	Reserved	Reserved
31-30	Reserved	Reserved	Reserved	Reserved

(1) The word "Reserved" means that there is no peripheral assigned to this GPxMUX1/2 register setting. Should it be selected, the state of the pin will be undefined and the pin may be driven. This selection is a reserved configuration for future expansion.
(2) I = Input, O = Output, OD = Open Drain
(3) This pin is not available in the 80-pin PN or PFP package.

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Table 8-41. Analog MUX for 100-Pin PZ and 100-Pin PZP Packages

		DEFAULT AT RESET
	AIOx AND PERIPHERAL SELECTION 1	PERIPHERAL SELECTION 2 AND PERIPHERAL SELECTION 3
AIOMUX1 REGISTER BITS	AIOMUX1 BITS = 0,x	AIOMUX1 BITS = 1,x
1-0	ADCINA0 (I)	ADCINA0 (I)
3-2	ADCINA1 (I)	ADCINA1 (I)
5-4	AIO2 (I/O)	ADCINA2 (I), COMP1A (I)
7-6	ADCINA3 (I)	ADCINA3 (I)
9-8	AIO4 (I/O)	ADCINA4 (I), COMP2A (I)
11-10	ADCINA5 (I)	ADCINA5 (I)
13-12	AIO6 (I/O)	ADCINA6 (I), COMP3A (I)
15-14	ADCINA7 (I)	ADCINA7 (I)
17-16	ADCINB0 (I)	ADCINB0 (I)
19-18	ADCINB1 (I)	ADCINB1 (I)
21-20	AIO10 (I/O)	ADCINB2 (I), COMP1B (I)
23-22	ADCINB3 (I)	ADCINB3 (I)
25-24	AIO12 (I/O)	ADCINB4 (I), COMP2B (I)
27-26	ADCINB5 (I)	ADCINB5 (I)
29-28	AIO14 (I/O)	ADCINB6 (I), COMP3B (I)
31-30	ADCINB7 (I)	ADCINB7 (I)

Table 8-42. Analog MUX for 80-Pin PN and 80-Pin PFP Packages

		DEFAULT AT RESET(1)
	AIOx AND PERIPHERAL SELECTION 1	PERIPHERAL SELECTION 2 AND PERIPHERAL SELECTION 3
AIOMUX1 REGISTER BITS	AIOMUX1 BITS = 0,x	AIOMUX1 BITS = 1,x
1-0	ADCINA0 (I), V_{REFHI} (I)	ADCINA0 (I), V_{REFHI} (I)
3-2	ADCINA1 (I)	ADCINA1 (I)
5-4	AIO2 (I/O)	ADCINA2 (I), COMP1A (I)
7-6	–	–
9-8	AIO4 (I/O)	ADCINA4 (I), COMP2A (I)
11-10	ADCINA5 (I)	ADCINA5 (I)
13-12	AIO6 (I/O)	ADCINA6 (I), COMP3A (I)
15-14	–	–
17-16	ADCINB0 (I)	ADCINB0 (I)
19-18	ADCINB1 (I)	ADCINB1 (I)
21-20	AIO10 (I/O)	ADCINB2 (I), COMP1B (I)
23-22	–	–
25-24	AIO12 (I/O)	ADCINB4 (I), COMP2B (I)
27-26	ADCINB5 (I)	ADCINB5 (I)
29-28	AIO14 (I/O)	ADCINB6 (I), COMP3B (I)
31-30	–	–

(1) I = Input, O = Output

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The user can select the type of input qualification for each GPIO pin through the GPxQSEL1/2 registers from four choices:

- Synchronization To SYSCLKOUT Only (GPxQSEL1/2 = 0, 0): This is the default mode of all GPIO pins at reset and it simply synchronizes the input signal to the system clock (SYSCLKOUT).
- Qualification Using Sampling Window (GPxQSEL1/2 = 0, 1 and 1, 0): In this mode the input signal, after synchronization to the system clock (SYSCLKOUT), is qualified by a specified number of cycles before the input is allowed to change.
- The sampling period is specified by the QUALPRD bits in the GPxCTRL register and is configurable in groups of 8 signals. The sampling period specifies a multiple of SYSCLKOUT cycles for sampling the input signal. The sampling window is either 3-samples or 6-samples wide and the output is only changed when ALL samples are the same (all 0s or all 1s) as shown in Figure 4-18 (for 6 sample mode).
- No Synchronization (GPxQSEL1/2 = 1,1): This mode is used for peripherals where synchronization is not required (synchronization is performed within the peripheral).

Due to the multilevel multiplexing that is required on the device, there may be cases where a peripheral input signal can be mapped to more then one GPIO pin. Also, when an input signal is not selected, the input signal will default to either a 0 or 1 state, depending on the peripheral.

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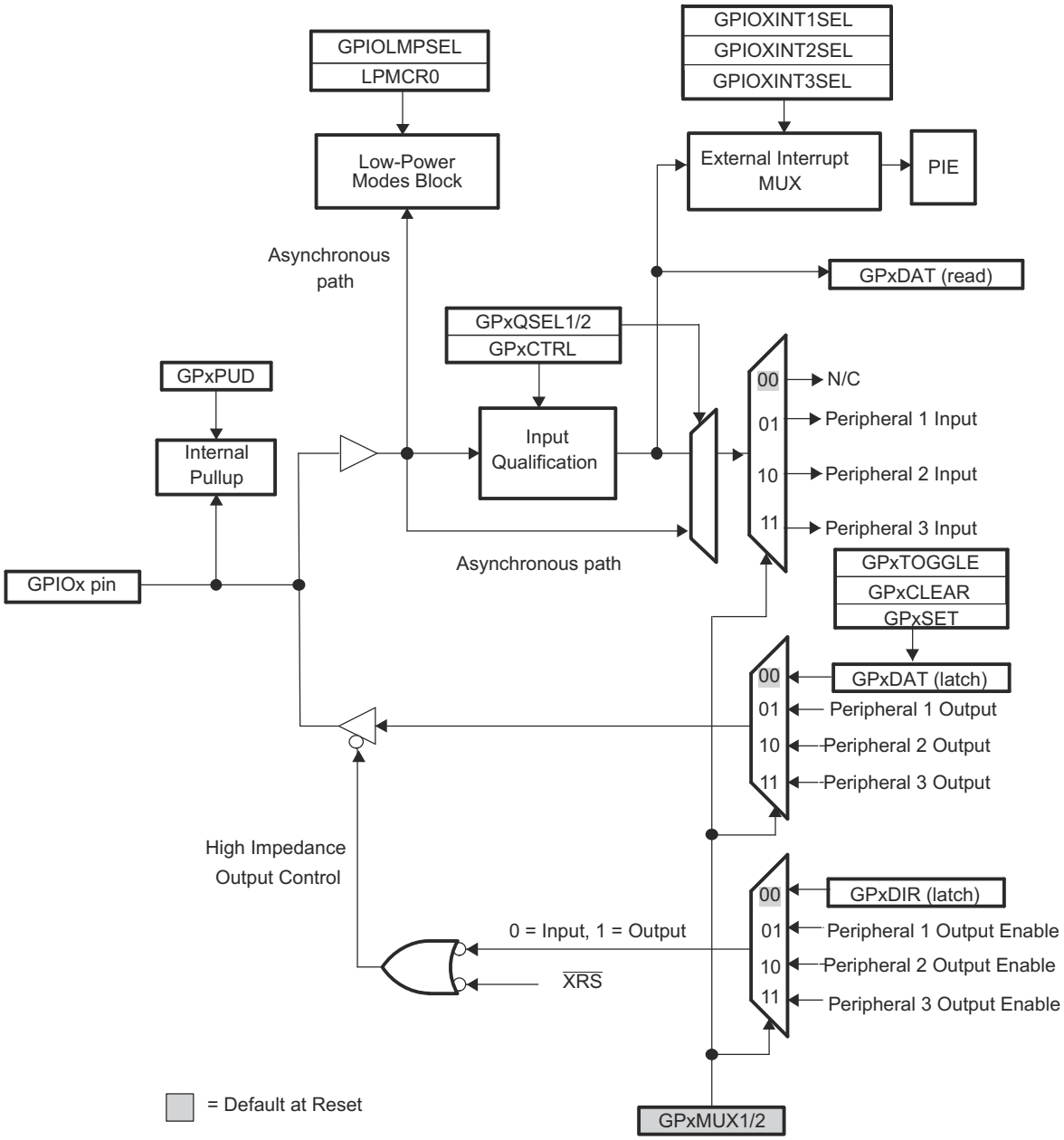

A. x stands for the port, either A or B. For example, GPxDIR refers to either the GPADIR and GPBDIR register depending on the particular GPIO pin selected.

B. GPxDAT latch/read are accessed at the same memory location.

C. This is a generic GPIO MUX block diagram. Not all options may be applicable for all GPIO pins. See the Systems Control and Interrupts chapter of the *TMS320x2806x Technical Reference Manual* for pin-specific variations.

Figure 8-55. GPIO Multiplexing

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8.9.15.1 GPIO Electrical Data/Timing

8.9.15.1.1 GPIO Output Timing

8.9.15.1.1.1 General-Purpose Output Switching Characteristics

over recommended operating conditions (unless otherwise noted)

PARAMETER			MIN	MAX	UNIT
$t_{r(GPO)}$	Rise time, GPIO switching low to high	All GPIOs		13[1]	ns
$t_{f(GPO)}$	Fall time, GPIO switching high to low	All GPIOs		13[1]	ns
f_{GPO}	Toggling frequency			22.5	MHz

(1) Rise time and fall time vary with electrical loading on I/O pins. Values given in Section 8.9.15.1.1.1 are applicable for a 40-pF load on I/O pins.

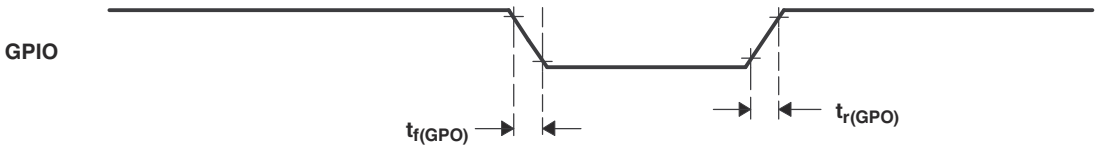


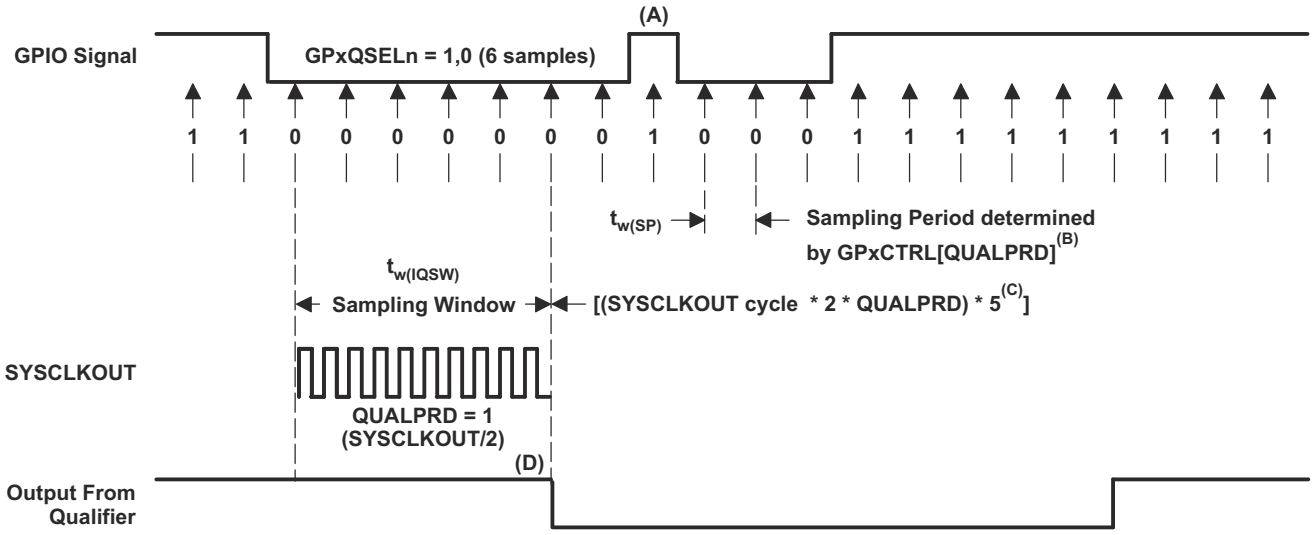
Figure 8-56. General-Purpose Output Timing

8.9.15.1.2 GPIO Input Timing

8.9.15.1.2.1 General-Purpose Input Timing Requirements

			MIN	MAX	UNIT
$t_{w(SP)}$	Sampling period	QUALPRD = 0	$1t_{c(SCO)}$		cycles
		QUALPRD ≠ 0	$2t_{c(SCO)}$ * QUALPRD		
$t_{w(IQSW)}$	Input qualifier sampling window		$t_{w(SP)}$ * (n(1) – 1)		cycles
$t_{w(GPI)}$ (2)	Pulse duration, GPIO low/high	Synchronous mode	$2t_{c(SCO)}$		cycles
		With input qualifier	$t_{w(IQSW)} + t_{w(SP)} + 1t_{c(SCO)}$		

(1) "n" represents the number of qualification samples as defined by GPxQSELn register.
(2) For $t_{w(GPI)}$, pulse width is measured from V_{IL} to V_{IL} for an active-low signal and V_{IH} to V_{IH} for an active-high signal.



A. This glitch will be ignored by the input qualifier. The QUALPRD bit field specifies the qualification sampling period. The QUALPRD bit field value can vary from 00 to 0xFF. If QUALPRD = 00, then the sampling period is one SYSCLKOUT cycle. For any other value "n", the qualification sampling period in 2n SYSCLKOUT cycles (that is, at every 2n SYSCLKOUT cycles, the GPIO pin will be sampled).
B. The qualification period selected through the GPxCTRL register applies to groups of eight GPIO pins.
C. The qualification block can take either three or six samples. The GPxQSELn Register selects which sample mode is used.
D. In the example shown, for the qualifier to detect the change, the input should be stable for 10 SYSCLKOUT cycles or greater. In other words, the inputs should be stable for (5 × QUALPRD × 2) SYSCLKOUT cycles. This would ensure five sampling periods for detection to occur. Because external signals are driven asynchronously, an 13-SYSCLKOUT-wide pulse ensures reliable recognition.

Figure 8-57. Sampling Mode

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8.9.15.1.3 Sampling Window Width for Input Signals

The following section summarizes the sampling window width for input signals for various input qualifier configurations.

Sampling frequency denotes how often a signal is sampled with respect to SYSCLKOUT.

Sampling frequency = SYSCLKOUT/(2 × QUALPRD), if QUALPRD ≠ 0

Sampling frequency = SYSCLKOUT, if QUALPRD = 0

Sampling period = SYSCLKOUT cycle × 2 × QUALPRD, if QUALPRD ≠ 0

In the preceding samples, SYSCLKOUT cycle indicates the time period of SYSCLKOUT.

Sampling period = SYSCLKOUT cycle, if QUALPRD = 0

In a given sampling window, either three or six samples of the input signal are taken to determine the validity of the signal. This is determined by the value written to GPxQSELn register.

Case 1:

Qualification using three samples

Sampling window width = (SYSCLKOUT cycle × 2 × QUALPRD) × 2, if QUALPRD ≠ 0

Sampling window width = (SYSCLKOUT cycle) × 2, if QUALPRD = 0

Case 2:

Qualification using six samples

Sampling window width = (SYSCLKOUT cycle × 2 × QUALPRD) × 5, if QUALPRD ≠ 0

Sampling window width = (SYSCLKOUT cycle) × 5, if QUALPRD = 0

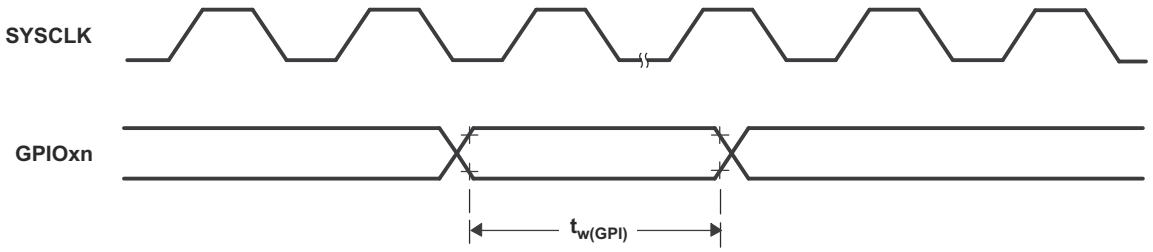

Figure 8-58. General-Purpose Input Timing

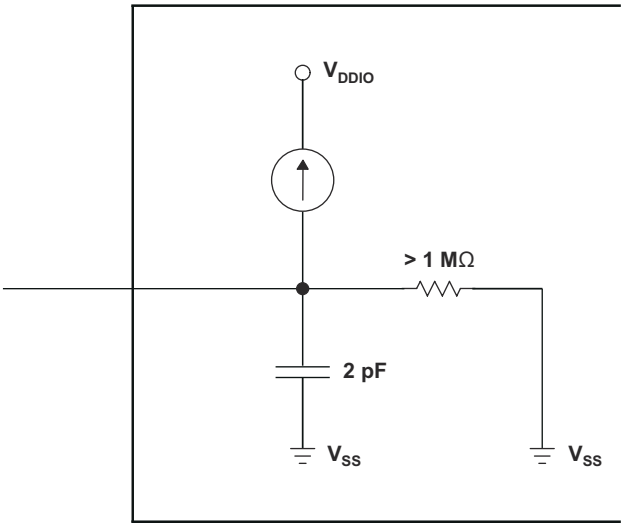

Figure 8-59. Input Resistance Model for a GPIO Pin With an Internal Pullup

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8.9.15.1.4 Low-Power Mode Wakeup Timing

Section 8.9.15.1.4.1 shows the timing requirements, Section 8.9.15.1.4.2 shows the switching characteristics, and Figure 8-60 shows the timing diagram for IDLE mode.

8.9.15.1.4.1 IDLE Mode Timing Requirements

			MIN[1] MAX	UNIT
$t_{w(WAKE-INT)}$	Pulse duration, external wake-up signal	Without input qualifier	$2t_{c(SCO)}$	cycles
		With input qualifier	$5t_{c(SCO)} + t_{w(IQSW)}$	

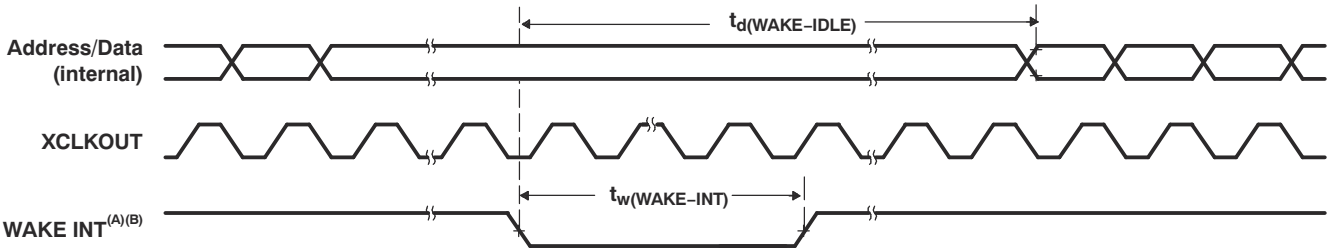
(1) For an explanation of the input qualifier parameters, see Section 8.9.15.1.2.1.

8.9.15.1.4.2 IDLE Mode Switching Characteristics

over recommended operating conditions (unless otherwise noted)[1]

PARAMETER		TEST CONDITIONS	MIN MAX	UNIT
$t_{d(WAKE-IDLE)}$	Delay time, external wake signal to program execution resume [2]			cycles
	• Wake up from flash – Flash module in active state	Without input qualifier	$20t_{c(SCO)}$	cycles
		With input qualifier	$20t_{c(SCO)} + t_{w(IQSW)}$	
	• Wake up from flash – Flash module in sleep state	Without input qualifier	$1050t_{c(SCO)}$	cycles
		With input qualifier	$1050t_{c(SCO)} + t_{w(IQSW)}$	
	• Wake up from SARAM	Without input qualifier	$20t_{c(SCO)}$	cycles
		With input qualifier	$20t_{c(SCO)} + t_{w(IQSW)}$	

(1) For an explanation of the input qualifier parameters, see Section 8.9.15.1.2.1.
(2) This is the time taken to begin execution of the instruction that immediately follows the IDLE instruction. Execution of an ISR (triggered by the wake-up signal) involves additional latency.



A. WAKE INT can be any enabled interrupt, $\overline{\text{WDINT}}$ or $\overline{\text{XRS}}$. After the IDLE instruction is executed, a delay of five OSCCLK cycles (minimum) is needed before the wake-up signal could be asserted.
B. From the time the IDLE instruction is executed to place the device into low-power mode (LPM), wakeup should not be initiated until at least four OSCCLK cycles have elapsed.

Figure 8-60. IDLE Entry and Exit Timing

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8.9.15.1.4.3 STANDBY Mode Timing Requirements

			MIN	MAX	UNIT
$t_{w(WAKE-INT)}$	Pulse duration, external wake-up signal	Without input qualification	$3t_{c(OSCCLK)}$		cycles
		With input qualification(1)	(2 + QUALSTDBY) * $t_{c(OSCCLK)}$		

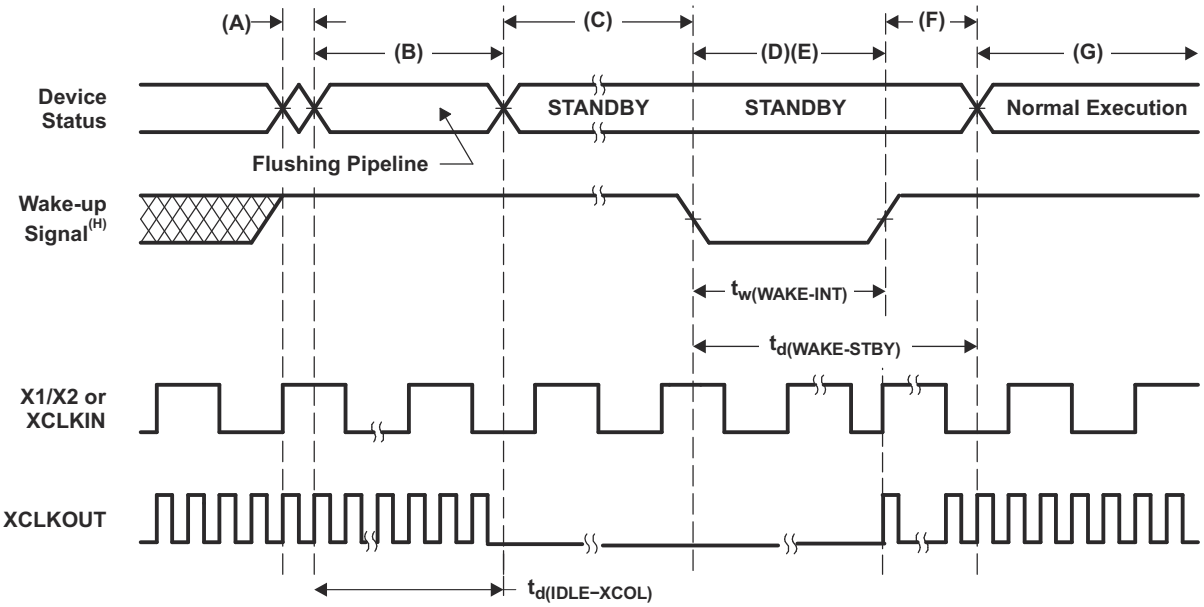
(1) QUALSTDBY is a 6-bit field in the LPMCR0 register.

8.9.15.1.4.4 STANDBY Mode Switching Characteristics

over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	MAX	UNIT
$t_{d(IDLE-XCOL)}$	Delay time, IDLE instruction executed to XCLKOUT low		$32t_{c(SCO)}$	$45t_{c(SCO)}$	cycles
$t_{d(WAKE-STBY)}$	Delay time, external wake signal to program execution resume(1)				cycles
	• Wake up from flash – Flash module in active state	Without input qualifier		$100t_{c(SCO)}$	cycles
		With input qualifier		$100t_{c(SCO)} + t_{w(WAKE-INT)}$	
	• Wake up from flash – Flash module in sleep state	Without input qualifier		$1125t_{c(SCO)}$	cycles
		With input qualifier		$1125t_{c(SCO)} + t_{w(WAKE-INT)}$	
	• Wake up from SARAM	Without input qualifier		$100t_{c(SCO)}$	cycles
		With input qualifier		$100t_{c(SCO)} + t_{w(WAKE-INT)}$	

(1) This is the time taken to begin execution of the instruction that immediately follows the IDLE instruction. Execution of an ISR (triggered by the wake-up signal) involves additional latency.



A. IDLE instruction is executed to put the device into STANDBY mode.

B. The PLL block responds to the STANDBY signal. SYSCLKOUT is held for the number of cycles indicated below before being turned off:

- 16 cycles, when DIVSEL = 00 or 01
- 32 cycles, when DIVSEL = 10
- 64 cycles, when DIVSEL = 11

This delay enables the CPU pipeline and any other pending operations to flush properly.

C. Clock to the peripherals are turned off. However, the PLL and watchdog are not shut down. The device is now in STANDBY mode. After the IDLE instruction is executed, a delay of five OSCCLK cycles (minimum) is needed before the wake-up signal could be asserted.

D. The external wake-up signal is driven active.

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E. The wake-up signal fed to a GPIO pin to wake up the device must meet the minimum pulse width requirement. Furthermore, this signal must be free of glitches. If a noisy signal is fed to a GPIO pin, the wake-up behavior of the device will not be deterministic and the device may not exit low-power mode for subsequent wake-up pulses.
F. After a latency period, the STANDBY mode is exited.
G. Normal execution resumes. The device will respond to the interrupt (if enabled).
H. From the time the IDLE instruction is executed to place the device into low-power mode (LPM), wakeup should not be initiated until at least four OSCCLK cycles have elapsed.

Figure 8-61. STANDBY Entry and Exit Timing Diagram

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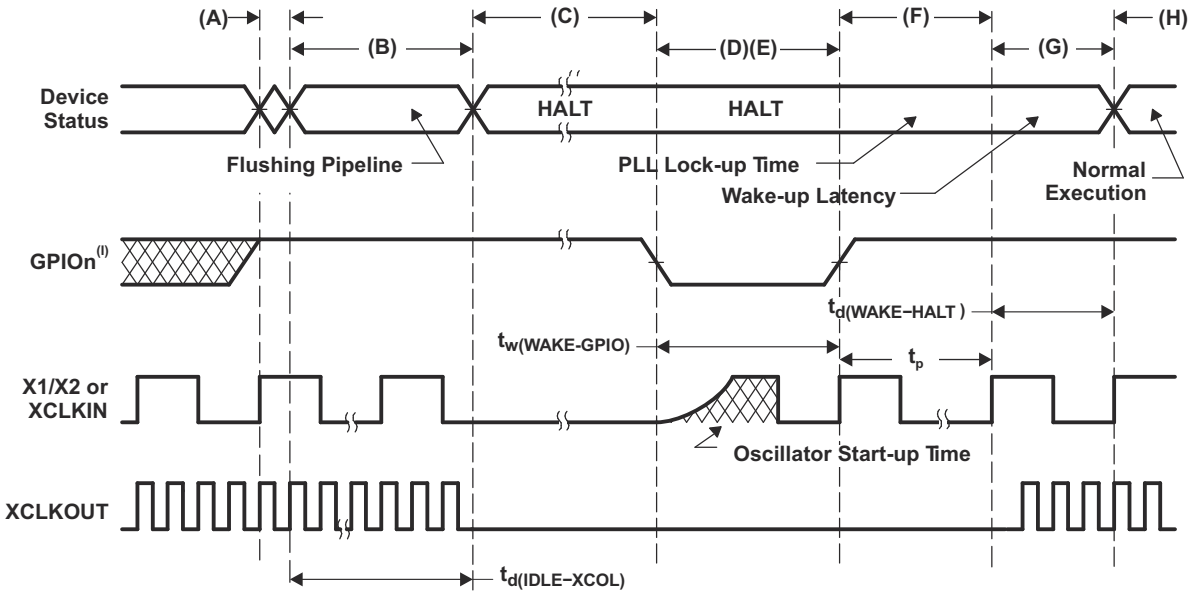
8.9.15.1.4.5 HALT Mode Timing Requirements

		MIN	MAX	UNIT
$t_{w(WAKE-GPIO)}$	Pulse duration, GPIO wake-up signal	$t_{oscst} + 2t_{c(OSCCLK)}$		cycles
$t_{w(WAKE-XRS)}$	Pulse duration, $\overline{XRS}$ wake-up signal	$t_{oscst} + 8t_{c(OSCCLK)}$		cycles

8.9.15.1.4.6 HALT Mode Switching Characteristics

over recommended operating conditions (unless otherwise noted)

PARAMETER		MIN	MAX	UNIT
$t_{d(IDLE-XCOL)}$	Delay time, IDLE instruction executed to XCLKOUT low	$32t_{c(SCO)}$	$45t_{c(SCO)}$	cycles
t_p	PLL lock-up time		1	ms
$t_{d(WAKE-HALT)}$	Delay time, PLL lock to program execution resume • Wake up from flash – Flash module in sleep state		$1125t_{c(SCO)}$	cycles
	• Wake up from SARAM		$35t_{c(SCO)}$	cycles



A. IDLE instruction is executed to put the device into HALT mode.

B. The PLL block responds to the HALT signal. SYSCLKOUT is held for the number of cycles indicated below before oscillator is turned off and the CLKIN to the core is stopped:

- 16 cycles, when DIVSEL = 00 or 01
- 32 cycles, when DIVSEL = 10
- 64 cycles, when DIVSEL = 11

This delay enables the CPU pipeline and any other pending operations to flush properly.

C. Clocks to the peripherals are turned off and the PLL is shut down. If a quartz crystal or ceramic resonator is used as the clock source, the internal oscillator is shut down as well. The device is now in HALT mode and consumes absolute minimum power. It is possible to keep the zero-pin internal oscillators (INTOSC1 and INTOSC2) and the watchdog alive in HALT mode. This is done by writing to the appropriate bits in the CLKCTL register. After the IDLE instruction is executed, a delay of five OSCCLK cycles (minimum) is needed before the wake-up signal could be asserted.

D. When the GPIOn pin (used to bring the device out of HALT) is driven low, the oscillator is turned on and the oscillator wake-up sequence is initiated. The GPIO pin should be driven high only after the oscillator has stabilized. This enables the provision of a clean clock signal during the PLL lock sequence. Because the falling edge of the GPIO pin asynchronously begins the wake-up procedure, care should be taken to maintain a low-noise environment before entering and during HALT mode.

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E. The wake-up signal fed to a GPIO pin to wake up the device must meet the minimum pulse width requirement. Furthermore, this signal must be free of glitches. If a noisy signal is fed to a GPIO pin, the wake-up behavior of the device will not be deterministic and the device may not exit low-power mode for subsequent wake-up pulses.
F. Once the oscillator has stabilized, the PLL lock sequence is initiated, which takes 1 ms.
G. When CLKIN to the core is enabled, the device will respond to the interrupt (if enabled), after a latency. The HALT mode is now exited.
H. Normal operation resumes.
I. From the time the IDLE instruction is executed to place the device into low-power mode (LPM), wakeup should not be initiated until at least four OSCCLK cycles have elapsed.

Figure 8-62. HALT Mode Wakeup Using GPIOn

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8.9.16 Universal Serial Bus (USB)

8.9.16.1 USB Electrical Data/Timing

8.9.16.1.1 USB Input Ports DP and DM Timing Requirements

		V_{CC}	MIN	MAX	UNIT
V(CM)	Differential input common mode range		0.8	2.5	V
Z(IN)	Input impedance		300		kΩ
VCRS	Crossover voltage		1.3	2.0	V
V_{IL}	Static SE input logic-low level		0.8		V
V_{IH}	Static SE input logic-high level			2.0	V
VDI	Differential input voltage			0.2	V

8.9.16.1.2 USB Output Ports DP and DM Switching Characteristics

over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	MAX	UNIT
V_{OH}	D+, D– single-ended	USB 2.0 load conditions		2.8	3.6	V
V_{OL}	D+, D– single-ended	USB 2.0 load conditions		0	0.3	V
Z(DRV)	D+, D– impedance			28	50	Ω
t_r	Rise time	Full speed, differential, C_L = 50 pF, 10%/90%, Rpu on D+		4	20	ns
t_f	Fall time	Full speed, differential, C_L = 50 pF, 10%/90%, Rpu on D+		4	20	ns

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9 Applications, Implementation, and Layout

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

9.1 TI Reference Design

The TI Reference Design Library is a robust reference design library spanning analog, embedded processor, and connectivity. Created by TI experts to help you jump start your system design, all reference designs include schematic or block diagrams, BOMs, and design files to speed your time to market. Search and download designs at the Select TI reference designs page.

Digitally Controlled Non-Isolated DC/DC Buck Converter Reference Design
This design implements a non-isolated DC/DC buck converter that is digitally controlled using a C2000 microcontroller. The main purpose of this design is to evaluate the powerSUITE Digital Power Software tools. The design consists of two separate boards: 1) Digital Power BoosterPack™ Plug-in Module and 2) C2000 F28069M LaunchPad™ Development Kit or C2000 F28377S LaunchPad Development Kit.

672W Highly Integrated Reference Design for Automotive Bidirectional 48V-12V Converter
Today's automotive power consumption is 3KW, which will increase to 10KW in the next 5 years. A 12-V battery is unable to provide that much power. The 48-12V bidirectional convertor provides a high-power requirement solution with two phases, each capable of running 28 A. This solution allows bidirectional current control of both phases using a C2000 control stick and firmware OCP and OVP. The 48-12V bidirectional converter removes the voltage conditioner need and distributes loads more evenly. The 48-V battery is used to power high-torque motors and other high-power components, such as A/C compressors and EPS, with no change to 12-V battery loads.

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10 Device and Documentation Support

10.1 Device and Development Support Tool Nomenclature

To designate the stages in the product development cycle, TI assigns prefixes to the part numbers of all TMS320™ MCU devices and support tools. Each TMS320 MCU commercial family member has one of three prefixes: TMX, TMP, or TMS (for example, **TMS**320F28069). Texas Instruments recommends two of three possible prefix designators for its support tools: TMDX and TMDS. These prefixes represent evolutionary stages of product development from engineering prototypes (with TMX for devices and TMDX for tools) to fully qualified production devices/tools (with TMS for devices and TMDS for tools).

Device development evolutionary flow:

TMX Experimental device that is not necessarily representative of the final device's electrical specifications and may not use production assembly flow.

TMP Prototype device that is not necessarily the final silicon die and may not necessarily meet final electrical specifications.

TMS Production version of the silicon die that is fully qualified.

Support tool development evolutionary flow:

TMDX Development-support product that has not yet completed Texas Instruments internal qualification testing.

TMDS Fully-qualified development-support product.

TMX and TMP devices and TMDX development-support tools are shipped against the following disclaimer:

TI device nomenclature also includes a suffix with the device family name. This suffix indicates the package type (for example, PZP) and temperature range (for example, S). Figure 10-1 provides a legend for reading the complete device name for any family member.

For device part numbers and further ordering information, see the TI website (www.ti.com) or contact your TI sales representative.

For additional description of the device nomenclature markings on the die, see the *TMS320F2806x MCUs Silicon Errata*.

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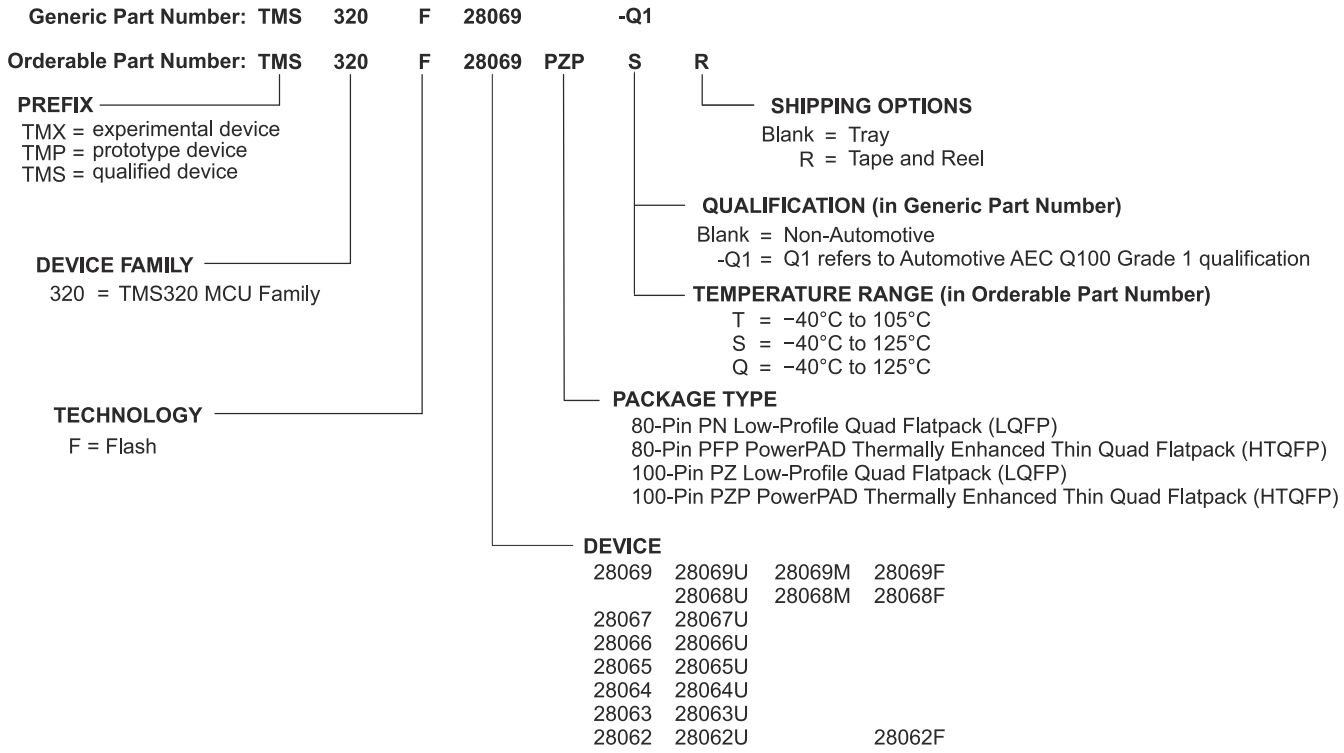

A. USB is present on TMS320F2806xU, TMS320F2806xM, and TMS320F2806xF devices.

B. TMS320F2806xM devices are InstaSPIN-MOTION-enabled MCUs. TMS320F2806xF devices are InstaSPIN-FOC-enabled MCUs. For more information, see Section 10.3 for a list of InstaSPIN Technical Reference Manuals.

C. For more information on peripheral, temperature, and package availability for a specific device, see Table 5-1.

Figure 10-1. Device Nomenclature

10.2 Tools and Software

TI offers an extensive line of development tools. Some of the tools and software to evaluate the performance of the device, generate code, and develop solutions are listed below. To view all available tools and software for C2000™ real-time control MCUs, visit the C2000 real-time control MCUs – Design & development page.

Development Tools

C2000 F28069M LaunchPad™ development kit

LAUNCHXL-F28069M is a low cost evaluation and development tool for the F2806x series as well as the InstaSPIN-FOC and InstaSPIN-MOTION enabled F2806x series in the TI MCU LaunchPad ecosystem which is compatible with various plug-on BoosterPacks. This extended version of the LaunchPad supports the connection of two BoosterPacks. The LaunchPad provides a standardized and easy to use platform to use while developing your next application.

F28069 controlCARD

The C2000 controlCARDs from Texas Instruments are ideal products for OEMs to use for initial software development and short-run builds for system prototypes, test stands, and many other projects that require easy access to high-performance controllers. The controlCARDs are complete board-level modules that use an industry-standard DIMM form factor to provide a low-profile, single-board controller solution. All of the C2000 controlCARDs use the same 100-pin connector footprint to provide the analog and digital I/Os onboard controller and are completely interchangeable. The host system must provide only a single 5-V power rail to the controlCARD for it to function fully.

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F28069 Experimenter Kit

The C2000 experimenter kits from Texas Instruments are ideal products for OEMs to use for initial device exploration and testing. The F28069 Experimenter Kit has a docking station that features onboard USB JTAG debug, access to all controlCARD signals, breadboard areas, and RS-232 and JTAG connectors. Each kit contains an F28069 controlCARD. The controlCARD is a complete board-level module that uses an industry-standard DIMM form factor to provide a low-profile, single-board controller solution. The kit is complete with Code Composer Studio IDE and USB cable.

Software Tools

C2000 Third-party search tool

TI has partnered with multiple companies to offer a wide range of solutions and services for TI C2000 devices. These companies can accelerate your path to production using C2000 devices. Download this search tool to quickly browse third-party details and find the right third-party to meet your needs.

C2000Ware for C2000 MCUs

C2000Ware for C2000™ microcontrollers is a cohesive set of development software and documentation designed to minimize software development time. From device-specific drivers and libraries to device peripheral examples, C2000Ware provides a solid foundation to begin development and evaluation of your product.

Code Composer Studio™ (CCS) Integrated Development Environment (IDE) for C2000 Microcontrollers

Code Composer Studio is an integrated development environment (IDE) that supports TI's Microcontroller and Embedded Processors portfolio. CCS comprises a suite of tools used to develop and debug embedded applications. It includes an optimizing C/C++ compiler, source code editor, project build environment, debugger, profiler, and many other features. The intuitive IDE provides a single user interface taking the user through each step of the application development flow. Familiar tools and interfaces let users get started faster than ever before. CCS combines the advantages of the Eclipse software framework with advanced embedded debug capabilities from TI resulting in a compelling feature-rich development environment for embedded developers.

Pin Mux Tool

The Pin Mux Utility is a software tool which provides a Graphical User Interface for configuring pin multiplexing settings, resolving conflicts and specifying I/O cell characteristics for TI MPUs.

UniFlash Standalone Flash Tool

UniFlash is a standalone tool used to program on-chip flash memory through a GUI, command line, or scripting interface.

Models

Various models are available for download from the product Tools & Software pages. These include I/O Buffer Information Specification (IBIS) Models and Boundary-Scan Description Language (BSDL) Models. To view all available models, visit the Models section of the Tools & Software page for each device.

Training

To help assist design engineers in taking full advantage of the C2000 microcontroller features and performance, TI has developed a variety of training resources. Utilizing the online training materials and downloadable hands-on workshops provides an easy means for gaining a complete working knowledge of the C2000 microcontroller family. These training resources have been designed to decrease the learning curve, while reducing development time, and accelerating product time to market. For more information on the various training resources, visit the C2000™ real-time control MCUs – Support & training site.

Specific TMS320F2806x hands-on training resources can be found at C2000™ MCU Device Workshops.

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10.3 Documentation Support

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Subscribe to updates* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

The current documentation that describes the processor, related peripherals, and other technical collateral is listed below.

Errata

TMS320F2806x MCUs Silicon Errata describes known advisories on silicon and provides workarounds.

InstaSPIN Technical Reference Manuals

InstaSPIN-FOC™ and InstaSPIN-MOTION™ User's Guide describes the InstaSPIN-FOC and InstaSPIN-MOTION devices.

TMS320F28069F, TMS320F28068F, TMS320F28062F InstaSPIN-FOC™ Software Technical Reference Manual describes the TMS320F28069F, TMS320F28068F, and TMS320F28062F InstaSPIN-FOC™ software.

TMS320F28069M, TMS320F28068M InstaSPIN-MOTION™ Software Technical Reference Manual describes the TMS320F28069M and TMS320F28068M InstaSPIN-MOTION™ software.

CPU User's Guides

TMS320C28x CPU and Instruction Set Reference Guide describes the central processing unit (CPU) and the assembly language instructions of the TMS320C28x fixed-point digital signal processors (DSPs). This reference guide also describes debug features available on these DSPs.

Peripheral Guides and Technical Reference Manuals

C2000 Real-Time Control Peripherals Reference Guide describes the peripheral reference guides of the 28x digital signal processors (DSPs).

TMS320x2806x Technical Reference Manual details the integration, the environment, the functional description, and the programming models for each peripheral and subsystem in the device.

Tools Guides

TMS320C28x Assembly Language Tools v20.12.0.STS User's Guide describes the assembly language tools (assembler and other tools used to develop assembly language code), assembler directives, macros, common object file format, and symbolic debugging directives for the TMS320C28x device.

TMS320C28x Optimizing C/C++ Compiler v20.12.0.STS User's Guide describes the TMS320C28x C/C++ compiler. This compiler accepts ANSI standard C/C++ source code and produces TMS320 DSP assembly language source code for the TMS320C28x device.

Application Reports

Semiconductor Packing Methodology describes the packing methodologies employed to prepare semiconductor devices for shipment to end users.

Calculating Useful Lifetimes of Embedded Processors provides a methodology for calculating the useful lifetime of TI embedded processors (EPs) under power when used in electronic systems. It is aimed at general engineers who wish to determine if the reliability of the TI EP meets the end system reliability requirement.

An Introduction to IBIS (I/O Buffer Information Specification) Modeling discusses various aspects of IBIS including its history, advantages, compatibility, model generation flow, data requirements in modeling the input/output structures and future trends.

Serial Flash Programming of C2000™ Microcontrollers discusses using a flash kernel and ROM loaders for serial programming a device.

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10.4 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

10.5 Trademarks

PowerPAD™, InstaSPIN-FOC™, InstaSPIN-MOTION™, TMS320C2000™, C2000™, FAST™, BoosterPack™, LaunchPad™, TMS320™, Code Composer Studio™, and TI E2E™ are trademarks of Texas Instruments.
SpinTAC™ is a trademark of LineStream Technologies, Inc.
I2C-bus® is a registered trademark of NXP B.V. Corporation.
All trademarks are the property of their respective owners.

10.6 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

10.7 Glossary

TI Glossary	This glossary lists and explains terms, acronyms, and definitions.

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11 Mechanical, Packaging, and Orderable Information

11.1 Packaging Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

For packages with a thermal pad, the MECHANICAL DATA figure shows a generic thermal pad without dimensions. For the actual thermal pad dimensions that are applicable to this device, see the THERMAL PAD MECHANICAL DATA figure.

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PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TMS320F28062FPFPQ	ACTIVE	HTQFP	PFP	80	96	RoHS & Green	NIPDAU	Level-3-260C-168 HR	-40 to 125	F28062FPFPQ TMS320	Samples
TMS320F28062FPNT	ACTIVE	LQFP	PN	80	119	RoHS & Green	NIPDAU	Level-3-260C-168 HR	-40 to 105	F28062FPNT TMS320	Samples
TMS320F28062FPZT	ACTIVE	LQFP	PZ	100	90	RoHS & Green	NIPDAU	Level-3-260C-168 HR	-40 to 105	F28062FPZT TMS320	Samples
TMS320F28062PFPQ	ACTIVE	HTQFP	PFP	80	96	RoHS & Green	NIPDAU	Level-3-260C-168 HR	-40 to 125	F28062PFPQ TMS320	Samples
TMS320F28062PFPQR	ACTIVE	HTQFP	PFP	80	1000	RoHS & Green	NIPDAU	Level-3-260C-168 HR	-40 to 125	F28062PFPQ TMS320	Samples
TMS320F28062PFPS	ACTIVE	HTQFP	PFP	80	96	RoHS & Green	NIPDAU	Level-3-260C-168 HR	-40 to 125	F28062PFPS TMS320	Samples
TMS320F28062PNT	ACTIVE	LQFP	PN	80	119	RoHS & Green	NIPDAU	Level-3-260C-168 HR	-40 to 105	320F28062PNT TMS	Samples
TMS320F28062PZPQ	ACTIVE	HTQFP	PZP	100	90	RoHS & Green	NIPDAU	Level-3-260C-168 HR	-40 to 125	F28062PZPQ TMS320	Samples
TMS320F28062PZPS	ACTIVE	HTQFP	PZP	100	90	RoHS & Green	NIPDAU	Level-3-260C-168 HR	-40 to 125	F28062PZPS TMS320	Samples
TMS320F28062PZT	ACTIVE	LQFP	PZ	100	90	RoHS & Green	NIPDAU	Level-3-260C-168 HR	-40 to 105	320F28062PZT TMS	Samples
TMS320F28062PZTR	ACTIVE	LQFP	PZ	100	1000	RoHS & Green	NIPDAU	Level-3-260C-168 HR	-40 to 105	320F28062PZT TMS	Samples
TMS320F28062UPNT	ACTIVE	LQFP	PN	80	119	RoHS & Green	NIPDAU	Level-3-260C-168 HR	-40 to 105	320F28062UPNT TMS	Samples
TMS320F28062UPZT	ACTIVE	LQFP	PZ	100	90	RoHS & Green	NIPDAU	Level-3-260C-168 HR	-40 to 105	F28062UPZT TMS320	Samples
TMS320F28063PNT	ACTIVE	LQFP	PN	80	119	RoHS & Green	NIPDAU	Level-3-260C-168 HR	-40 to 105	320F28063PNT TMS	Samples
TMS320F28063PZT	ACTIVE	LQFP	PZ	100	90	RoHS & Green	NIPDAU	Level-3-260C-168 HR	-40 to 105	320F28063PZT TMS	Samples
TMS320F28064PZT	ACTIVE	LQFP	PZ	100	90	RoHS & Green	NIPDAU	Level-3-260C-168 HR	-40 to 105	320F28064PZT TMS	Samples
TMS320F28065PFPS	ACTIVE	HTQFP	PFP	80	96	RoHS & Green	NIPDAU	Level-3-260C-168 HR	-40 to 125	F28065PFPS	Samples

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
										TMS320	
TMS320F28065PNT	ACTIVE	LQFP	PN	80	119	RoHS & Green	NIPDAU	Level-3-260C-168 HR	-40 to 105	F28065PNT TMS320	Samples
TMS320F28065PZPS	ACTIVE	HTQFP	PZP	100	90	RoHS & Green	NIPDAU	Level-3-260C-168 HR	-40 to 125	F28065PZPS TMS320	Samples
TMS320F28065PZT	ACTIVE	LQFP	PZ	100	90	RoHS & Green	NIPDAU	Level-3-260C-168 HR	-40 to 105	320F28065PZT TMS	Samples
TMS320F28065UPZT	ACTIVE	LQFP	PZ	100	90	RoHS & Green	NIPDAU	Level-3-260C-168 HR	-40 to 105	F28065UPZT TMS320	Samples
TMS320F28066PFPQ	ACTIVE	HTQFP	PFP	80	96	RoHS & Green	NIPDAU	Level-3-260C-168 HR	-40 to 125	F28066PFPQ TMS320	Samples
TMS320F28066PFPS	ACTIVE	HTQFP	PFP	80	96	RoHS & Green	NIPDAU	Level-3-260C-168 HR	-40 to 125	F28066PFPS TMS320	Samples
TMS320F28066PNT	ACTIVE	LQFP	PN	80	119	RoHS & Green	NIPDAU	Level-3-260C-168 HR	-40 to 105	320F28066PNT TMS	Samples
TMS320F28066PZPQ	ACTIVE	HTQFP	PZP	100	90	RoHS & Green	NIPDAU	Level-3-260C-168 HR	-40 to 125	F28066PZPQ TMS320	Samples
TMS320F28066PZPS	ACTIVE	HTQFP	PZP	100	90	RoHS & Green	NIPDAU	Level-3-260C-168 HR	-40 to 125	F28066PZPS TMS320	Samples
TMS320F28066PZT	ACTIVE	LQFP	PZ	100	90	RoHS & Green	NIPDAU	Level-3-260C-168 HR	-40 to 105	320F28066PZT TMS	Samples
TMS320F28067PFPS	ACTIVE	HTQFP	PFP	80	96	RoHS & Green	NIPDAU	Level-3-260C-168 HR	-40 to 125	F28067PFPS TMS320	Samples
TMS320F28067PNT	ACTIVE	LQFP	PN	80	119	RoHS & Green	NIPDAU	Level-3-260C-168 HR	-40 to 105	320F28067PNT TMS	Samples
TMS320F28067PZPQ	ACTIVE	HTQFP	PZP	100	90	RoHS & Green	NIPDAU	Level-3-260C-168 HR	-40 to 125	F28067PZPQ TMS320	Samples
TMS320F28067PZPS	ACTIVE	HTQFP	PZP	100	90	RoHS & Green	NIPDAU	Level-3-260C-168 HR	-40 to 125	F28067PZPS TMS320	Samples
TMS320F28067PZT	ACTIVE	LQFP	PZ	100	90	RoHS & Green	NIPDAU	Level-3-260C-168 HR	-40 to 105	320F28067PZT TMS	Samples
TMS320F28068FPNT	ACTIVE	LQFP	PN	80	119	RoHS & Green	NIPDAU	Level-3-260C-168 HR	-40 to 105	F28068FPNT TMS320	Samples
TMS320F28068FPZT	ACTIVE	LQFP	PZ	100	90	RoHS & Green	NIPDAU	Level-3-260C-168 HR	-40 to 105	F28068FPZT TMS320	Samples

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TMS320F28068MPNT	ACTIVE	LQFP	PN	80	119	RoHS & Green	NIPDAU	Level-3-260C-168 HR	-40 to 105	F28068MPNT TMS320	Samples
TMS320F28068MPZT	ACTIVE	LQFP	PZ	100	90	RoHS & Green	NIPDAU	Level-3-260C-168 HR	-40 to 105	F28068MPZT TMS320	Samples
TMS320F28069FPFPQ	ACTIVE	HTQFP	PFP	80	96	RoHS & Green	NIPDAU	Level-3-260C-168 HR	-40 to 125	F28069FPFPQ TMS320	Samples
TMS320F28069FPNT	ACTIVE	LQFP	PN	80	119	RoHS & Green	NIPDAU	Level-3-260C-168 HR	-40 to 105	F28069FPNT TMS320	Samples
TMS320F28069FPZPQ	ACTIVE	HTQFP	PZP	100	90	RoHS & Green	NIPDAU	Level-3-260C-168 HR	-40 to 125	F28069FPZPQ TMS320	Samples
TMS320F28069FPZT	ACTIVE	LQFP	PZ	100	90	RoHS & Green	NIPDAU	Level-3-260C-168 HR	-40 to 105	F28069FPZT TMS320	Samples
TMS320F28069FPZTR	ACTIVE	LQFP	PZ	100	1000	RoHS & Green	NIPDAU	Level-3-260C-168 HR	-40 to 105	F28069FPZT TMS320	Samples
TMS320F28069MPFPQ	ACTIVE	HTQFP	PFP	80	96	RoHS & Green	NIPDAU	Level-3-260C-168 HR	-40 to 125	F28069MPFPQ TMS320	Samples
TMS320F28069MPNT	ACTIVE	LQFP	PN	80	119	RoHS & Green	NIPDAU	Level-3-260C-168 HR	-40 to 105	F28069MPNT TMS320	Samples
TMS320F28069MPZPQ	ACTIVE	HTQFP	PZP	100	90	RoHS & Green	NIPDAU	Level-3-260C-168 HR	-40 to 125	F28069MPZPQ TMS320	Samples
TMS320F28069MPZT	ACTIVE	LQFP	PZ	100	90	RoHS & Green	NIPDAU	Level-3-260C-168 HR	-40 to 105	F28069MPZT TMS320	Samples
TMS320F28069PFPQ	ACTIVE	HTQFP	PFP	80	96	RoHS & Green	NIPDAU	Level-3-260C-168 HR	-40 to 125	F28069PFPQ TMS320	Samples
TMS320F28069PFPS	ACTIVE	HTQFP	PFP	80	96	RoHS & Green	NIPDAU	Level-3-260C-168 HR	-40 to 125	F28069PFPS TMS320	Samples
TMS320F28069PNT	ACTIVE	LQFP	PN	80	119	RoHS & Green	NIPDAU	Level-3-260C-168 HR	-40 to 125	320F28069PNT TMS	Samples
TMS320F28069PZA	ACTIVE	LQFP	PZ	100	90	RoHS & Green	NIPDAU	Level-3-260C-168 HR	-40 to 85	320F28069PZA TMS	Samples
TMS320F28069PZPQ	ACTIVE	HTQFP	PZP	100	90	RoHS & Green	NIPDAU	Level-3-260C-168 HR	-40 to 125	F28069PZPQ TMS320	Samples
TMS320F28069PZPS	ACTIVE	HTQFP	PZP	100	90	RoHS & Green	NIPDAU	Level-3-260C-168 HR	-40 to 125	F28069PZPS TMS320	Samples
TMS320F28069PZT	ACTIVE	LQFP	PZ	100	90	RoHS & Green	NIPDAU	Level-3-260C-168 HR	-40 to 105	320F28069PZT	Samples

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
										TMS	
TMS320F28069UPFPS	ACTIVE	HTQFP	PFP	80	96	RoHS & Green	NIPDAU	Level-3-260C-168 HR	-40 to 125	F28069UPFPS TMS320	Samples
TMS320F28069UPNT	ACTIVE	LQFP	PN	80	119	RoHS & Green	NIPDAU	Level-3-260C-168 HR	-40 to 105	F28069UPNT TMS320	Samples
TMS320F28069UPZPS	ACTIVE	HTQFP	PZP	100	90	RoHS & Green	NIPDAU	Level-3-260C-168 HR	-40 to 125	F28069UPZPS TMS320	Samples
TMS320F28069UPZT	ACTIVE	LQFP	PZ	100	90	RoHS & Green	NIPDAU	Level-3-260C-168 HR	-40 to 105	F28069UPZT TMS320	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

OTHER QUALIFIED VERSIONS OF TMS320F28062, TMS320F28062-Q1, TMS320F28062F, TMS320F28062F-Q1, TMS320F28066, TMS320F28066-Q1, TMS320F28067, TMS320F28067-Q1, TMS320F28069, TMS320F28069-Q1, TMS320F28069F, TMS320F28069F-Q1, TMS320F28069M, TMS320F28069M-Q1 :

- Catalog : TMS320F28062, TMS320F28062F, TMS320F28066, TMS320F28067, TMS320F28069, TMS320F28069F, TMS320F28069M

- Automotive : TMS320F28062-Q1, TMS320F28062F-Q1, TMS320F28066-Q1, TMS320F28067-Q1, TMS320F28069-Q1, TMS320F28069F-Q1, TMS320F28069M-Q1

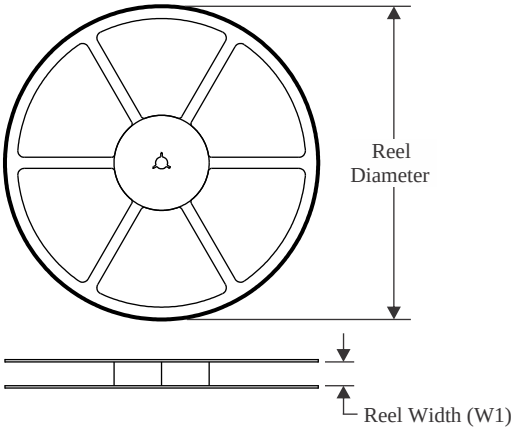
NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product

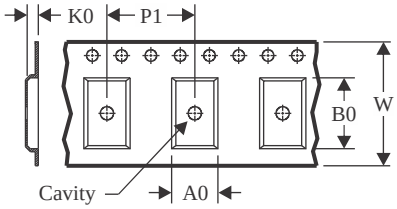
- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects

TAPE AND REEL INFORMATION

REEL DIMENSIONS

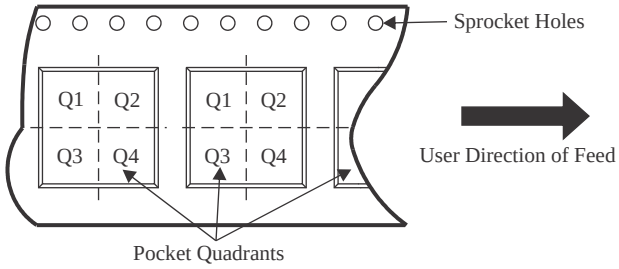


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

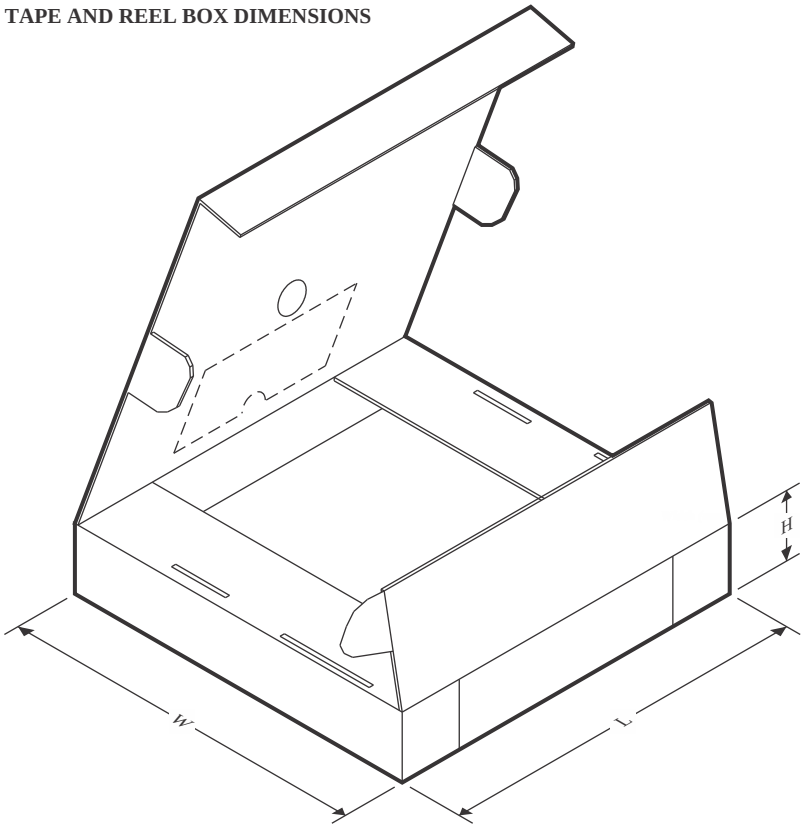
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TMS320F28062PFPQR	HTQFP	PFP	80	1000	330.0	24.4	15.0	15.0	1.5	20.0	24.0	Q2
TMS320F28069FPZTR	LQFP	PZ	100	1000	330.0	32.4	16.9	16.9	2.0	24.0	32.0	Q2

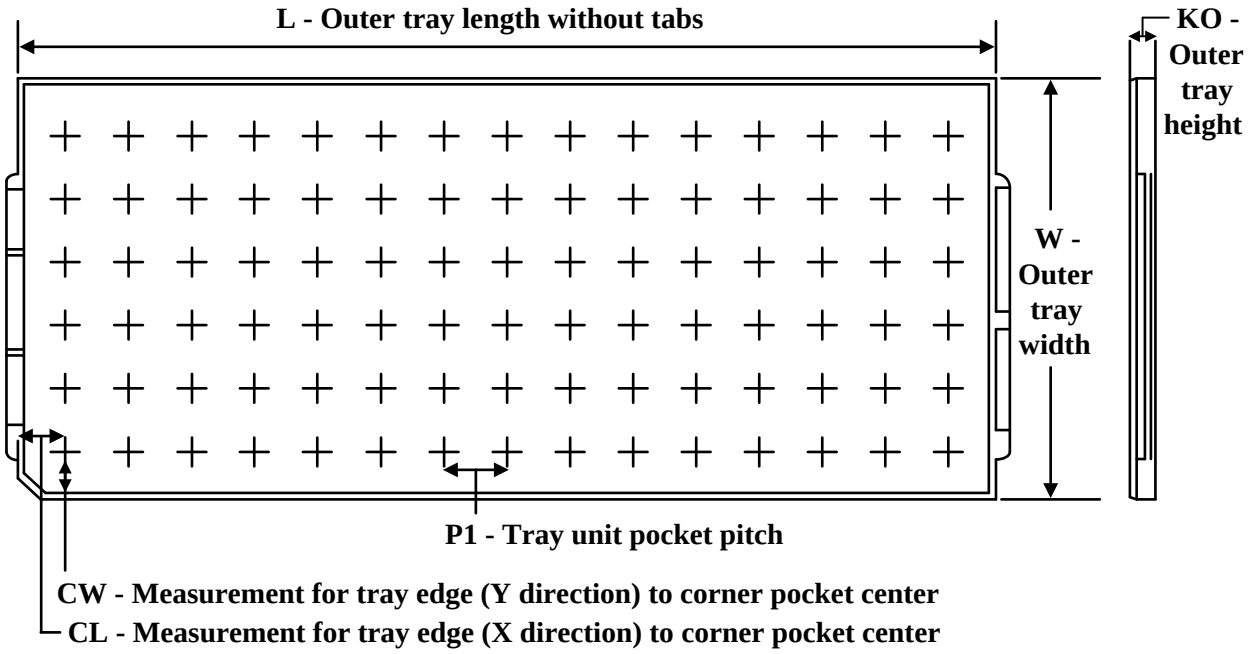
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TMS320F28062PFPQR	HTQFP	PFP	80	1000	367.0	367.0	55.0
TMS320F28069FPZTR	LQFP	PZ	100	1000	367.0	367.0	55.0

TRAY



Chamfer on Tray corner indicates Pin 1 orientation of packed units.

*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	Unit array matrix	Max temperature (°C)	L (mm)	W (mm)	K0 (µm)	P1 (mm)	CL (mm)	CW (mm)
TMS320F28062FPFPQ	PFP	HTQFP	80	96	6 x 16	150	315	135.9	7620	18.7	17.25	18.3
TMS320F28062FPNT	PN	LQFP	80	119	7 X 17	150	315	135.9	7620	17.9	14.3	13.95
TMS320F28062FPZT	PZ	LQFP	100	90	6 x 15	150	315	135.9	7620	20.3	15.4	15.4
TMS320F28062PFPQ	PFP	HTQFP	80	96	6 x 16	150	315	135.9	7620	18.7	17.25	18.3
TMS320F28062PFPS	PFP	HTQFP	80	96	6 x 16	150	315	135.9	7620	18.7	17.25	18.3
TMS320F28062PNT	PN	LQFP	80	119	7 X 17	150	315	135.9	7620	17.9	14.3	13.95
TMS320F28062PZPQ	PZP	HTQFP	100	90	6 X 15	150	315	135.9	7620	15.4	20.3	21
TMS320F28062PZPS	PZP	HTQFP	100	90	6 X 15	150	315	135.9	7620	15.4	20.3	21
TMS320F28062PZT	PZ	LQFP	100	90	6 x 15	150	315	135.9	7620	20.3	15.4	15.4
TMS320F28062UPNT	PN	LQFP	80	119	7 X 17	150	315	135.9	7620	17.9	14.3	13.95
TMS320F28062UPZT	PZ	LQFP	100	90	6 x 15	150	315	135.9	7620	20.3	15.4	15.4
TMS320F28063PNT	PN	LQFP	80	119	7 X 17	150	315	135.9	7620	17.9	14.3	13.95
TMS320F28063PZT	PZ	LQFP	100	90	6 x 15	150	315	135.9	7620	20.3	15.4	15.4
TMS320F28064PZT	PZ	LQFP	100	90	6 x 15	150	315	135.9	7620	20.3	15.4	15.4
TMS320F28065PFPS	PFP	HTQFP	80	96	6 x 16	150	315	135.9	7620	18.7	17.25	18.3
TMS320F28065PNT	PN	LQFP	80	119	7 X 17	150	315	135.9	7620	17.9	14.3	13.95
TMS320F28065PZPS	PZP	HTQFP	100	90	6 X 15	150	315	135.9	7620	15.4	20.3	21

Device	Package Name	Package Type	Pins	SPQ	Unit array matrix	Max temperature (°C)	L (mm)	W (mm)	K0 (µm)	P1 (mm)	CL (mm)	CW (mm)
TMS320F28065PZT	PZ	LQFP	100	90	6 x 15	150	315	135.9	7620	20.3	15.4	15.4
TMS320F28065UPZT	PZ	LQFP	100	90	6 x 15	150	315	135.9	7620	20.3	15.4	15.4
TMS320F28066PFPQ	PFP	HTQFP	80	96	6 x 16	150	315	135.9	7620	18.7	17.25	18.3
TMS320F28066PFPS	PFP	HTQFP	80	96	6 x 16	150	315	135.9	7620	18.7	17.25	18.3
TMS320F28066PNT	PN	LQFP	80	119	7 X 17	150	315	135.9	7620	17.9	14.3	13.95
TMS320F28066PZPQ	PZP	HTQFP	100	90	6 X 15	150	315	135.9	7620	15.4	20.3	21
TMS320F28066PZPS	PZP	HTQFP	100	90	6 X 15	150	315	135.9	7620	15.4	20.3	21
TMS320F28066PZT	PZ	LQFP	100	90	6 x 15	150	315	135.9	7620	20.3	15.4	15.4
TMS320F28067PFPS	PFP	HTQFP	80	96	6 x 16	150	315	135.9	7620	18.7	17.25	18.3
TMS320F28067PNT	PN	LQFP	80	119	7 X 17	150	315	135.9	7620	17.9	14.3	13.95
TMS320F28067PZPQ	PZP	HTQFP	100	90	6 X 15	150	315	135.9	7620	15.4	20.3	21
TMS320F28067PZPS	PZP	HTQFP	100	90	6 X 15	150	315	135.9	7620	15.4	20.3	21
TMS320F28067PZT	PZ	LQFP	100	90	6 x 15	150	315	135.9	7620	20.3	15.4	15.4
TMS320F28068FPNT	PN	LQFP	80	119	7 X 17	150	315	135.9	7620	17.9	14.3	13.95
TMS320F28068FPZT	PZ	LQFP	100	90	6 x 15	150	315	135.9	7620	20.3	15.4	15.4
TMS320F28068MPNT	PN	LQFP	80	119	7 X 17	150	315	135.9	7620	17.9	14.3	13.95
TMS320F28068MPZT	PZ	LQFP	100	90	6 x 15	150	315	135.9	7620	20.3	15.4	15.4
TMS320F28069FPFPQ	PFP	HTQFP	80	96	6 x 16	150	315	135.9	7620	18.7	17.25	18.3
TMS320F28069FPNT	PN	LQFP	80	119	7 X 17	150	315	135.9	7620	17.9	14.3	13.95
TMS320F28069FPZPQ	PZP	HTQFP	100	90	6 X 15	150	315	135.9	7620	15.4	20.3	21
TMS320F28069FPZT	PZ	LQFP	100	90	6 x 15	150	315	135.9	7620	20.3	15.4	15.4
TMS320F28069MPFPQ	PFP	HTQFP	80	96	6 x 16	150	315	135.9	7620	18.7	17.25	18.3
TMS320F28069MPNT	PN	LQFP	80	119	7 X 17	150	315	135.9	7620	17.9	14.3	13.95
TMS320F28069MPZPQ	PZP	HTQFP	100	90	6 X 15	150	315	135.9	7620	15.4	20.3	21
TMS320F28069MPZT	PZ	LQFP	100	90	6 x 15	150	315	135.9	7620	20.3	15.4	15.4
TMS320F28069PFPQ	PFP	HTQFP	80	96	6 x 16	150	315	135.9	7620	18.7	17.25	18.3
TMS320F28069PFPS	PFP	HTQFP	80	96	6 x 16	150	315	135.9	7620	18.7	17.25	18.3
TMS320F28069PNT	PN	LQFP	80	119	7 X 17	150	315	135.9	7620	17.9	14.3	13.95
TMS320F28069PZA	PZ	LQFP	100	90	6 x 15	150	315	135.9	7620	20.3	15.4	15.4
TMS320F28069PZPQ	PZP	HTQFP	100	90	6 X 15	150	315	135.9	7620	15.4	20.3	21
TMS320F28069PZPS	PZP	HTQFP	100	90	6 X 15	150	315	135.9	7620	15.4	20.3	21
TMS320F28069PZT	PZ	LQFP	100	90	6 x 15	150	315	135.9	7620	20.3	15.4	15.4
TMS320F28069UPFPS	PFP	HTQFP	80	96	6 x 16	150	315	135.9	7620	18.7	17.25	18.3
TMS320F28069UPNT	PN	LQFP	80	119	7 X 17	150	315	135.9	7620	17.9	14.3	13.95
TMS320F28069UPZPS	PZP	HTQFP	100	90	6 X 15	150	315	135.9	7620	15.4	20.3	21
TMS320F28069UPZT	PZ	LQFP	100	90	6 x 15	150	315	135.9	7620	20.3	15.4	15.4

GENERIC PACKAGE VIEW

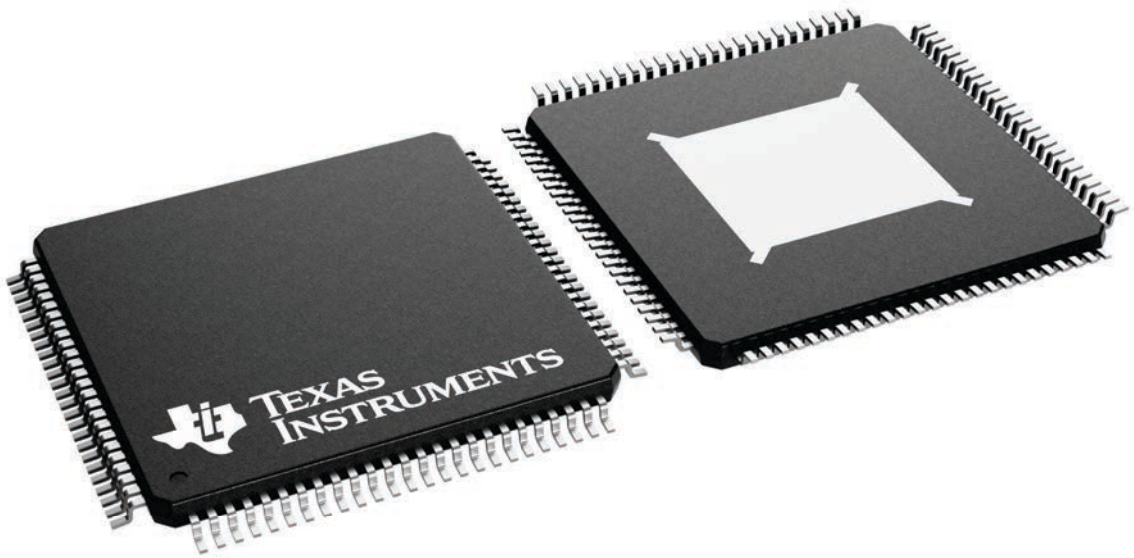
PZP 100

PowerPAD ™ TQFP - 1.2 mm max height

14 x 14 mm Pkg Body, 0.5 mm pitch
16 x 16 mm Pkg Area

PLASTIC QUAD FLATPACK

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



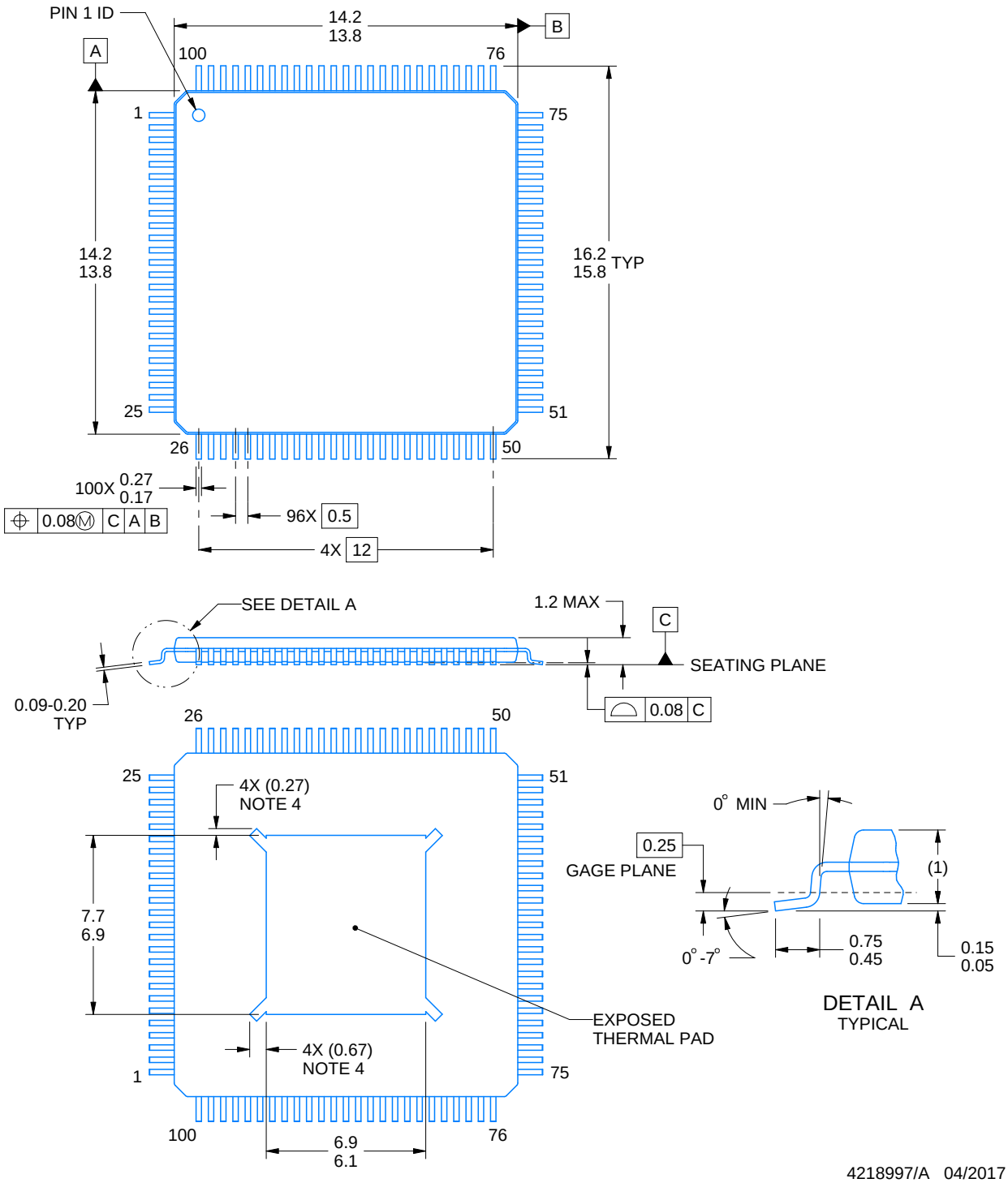
4224739/B

PACKAGE OUTLINE

PZP0100G

PowerPAD™ TQFP - 1.2 mm max height

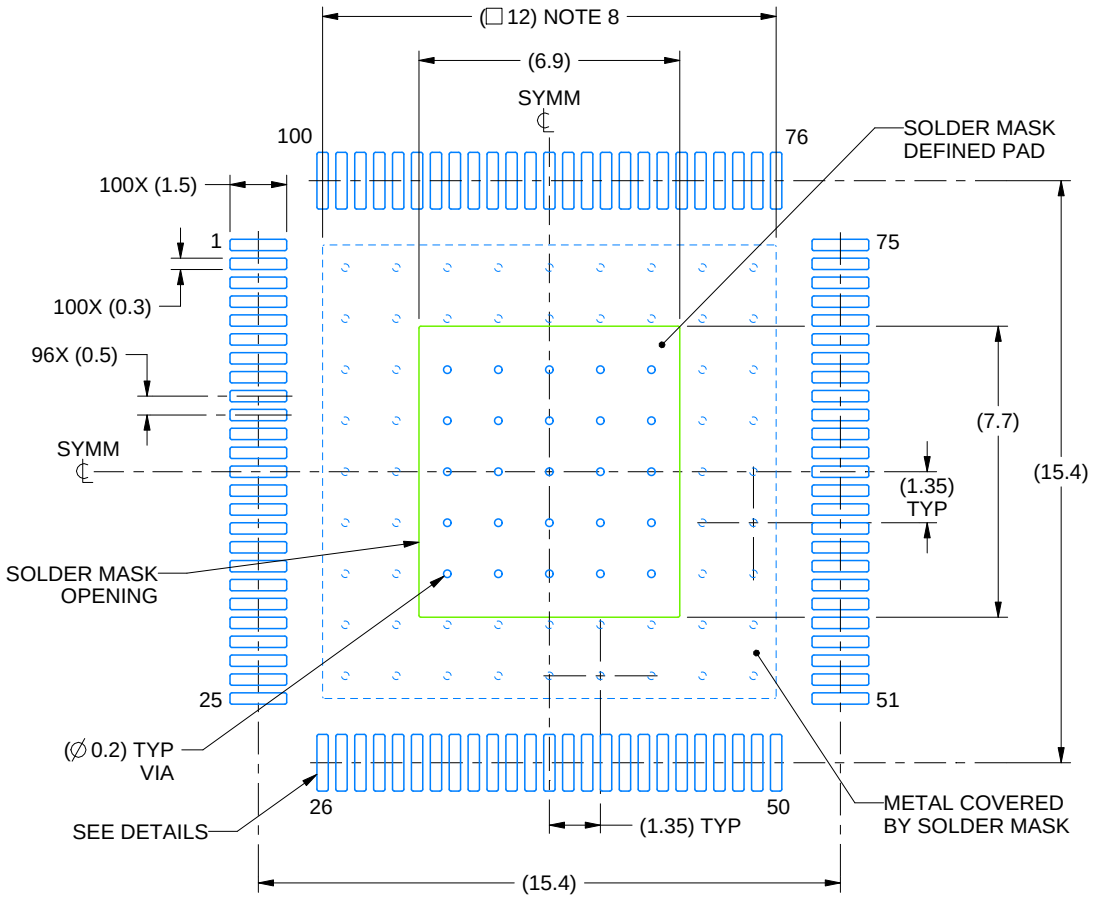
PLASTIC QUAD FLATPACK



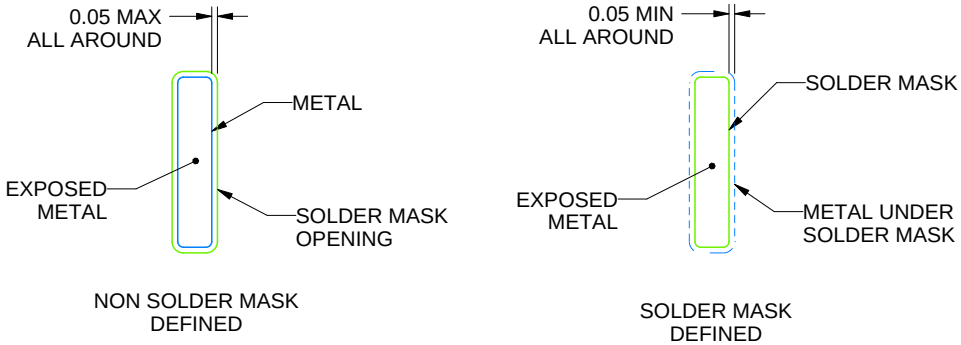
PowerPAD is a trademark of Texas Instruments.

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Reference JEDEC registration MS-026, variation ACD.
4. Strap features may not be present,



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:5X

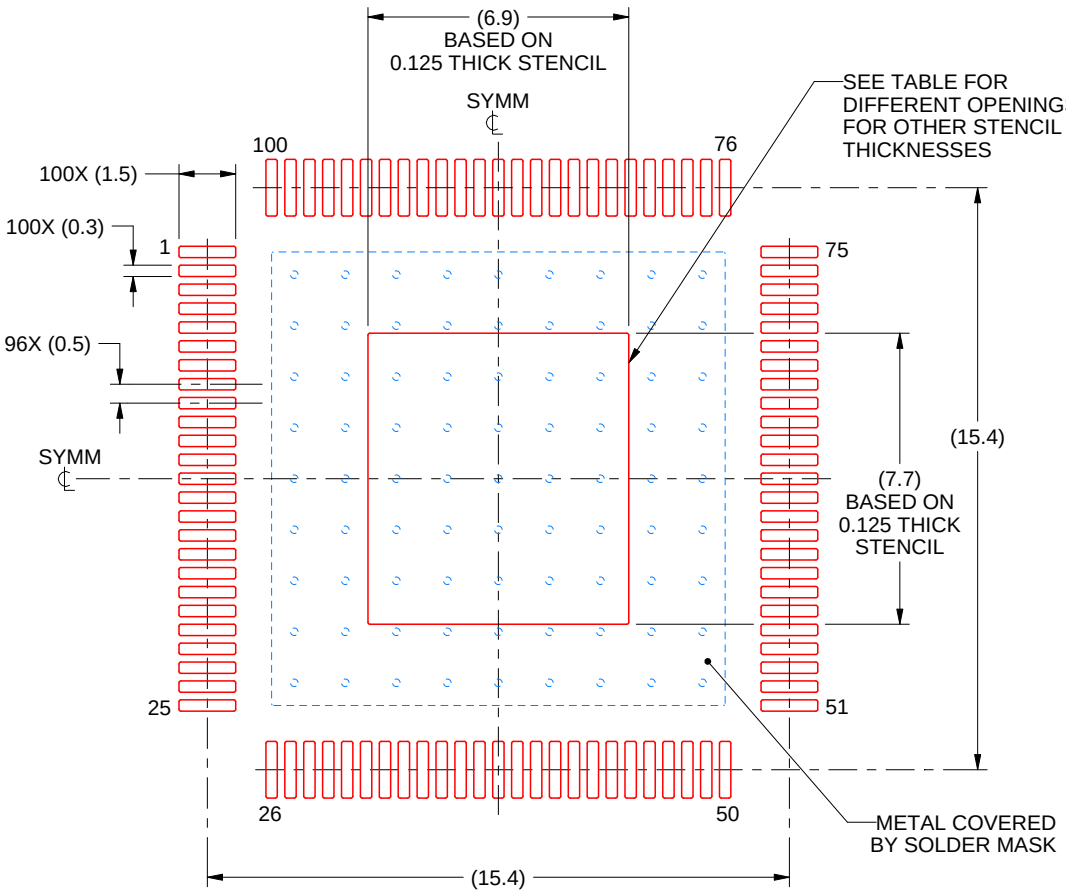


SOLDER MASK DETAILS

4218997/A 04/2017

NOTES: (continued)

5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
7. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature numbers SLMA002 (www.ti.com/lit/slma002) and SLMA004 (www.ti.com/lit/slma004).
8. Size of metal pad may vary due to creepage requirement.



SOLDER PASTE EXAMPLE
EXPOSED PAD
100% PRINTED SOLDER COVERAGE BY AREA
SCALE:5X

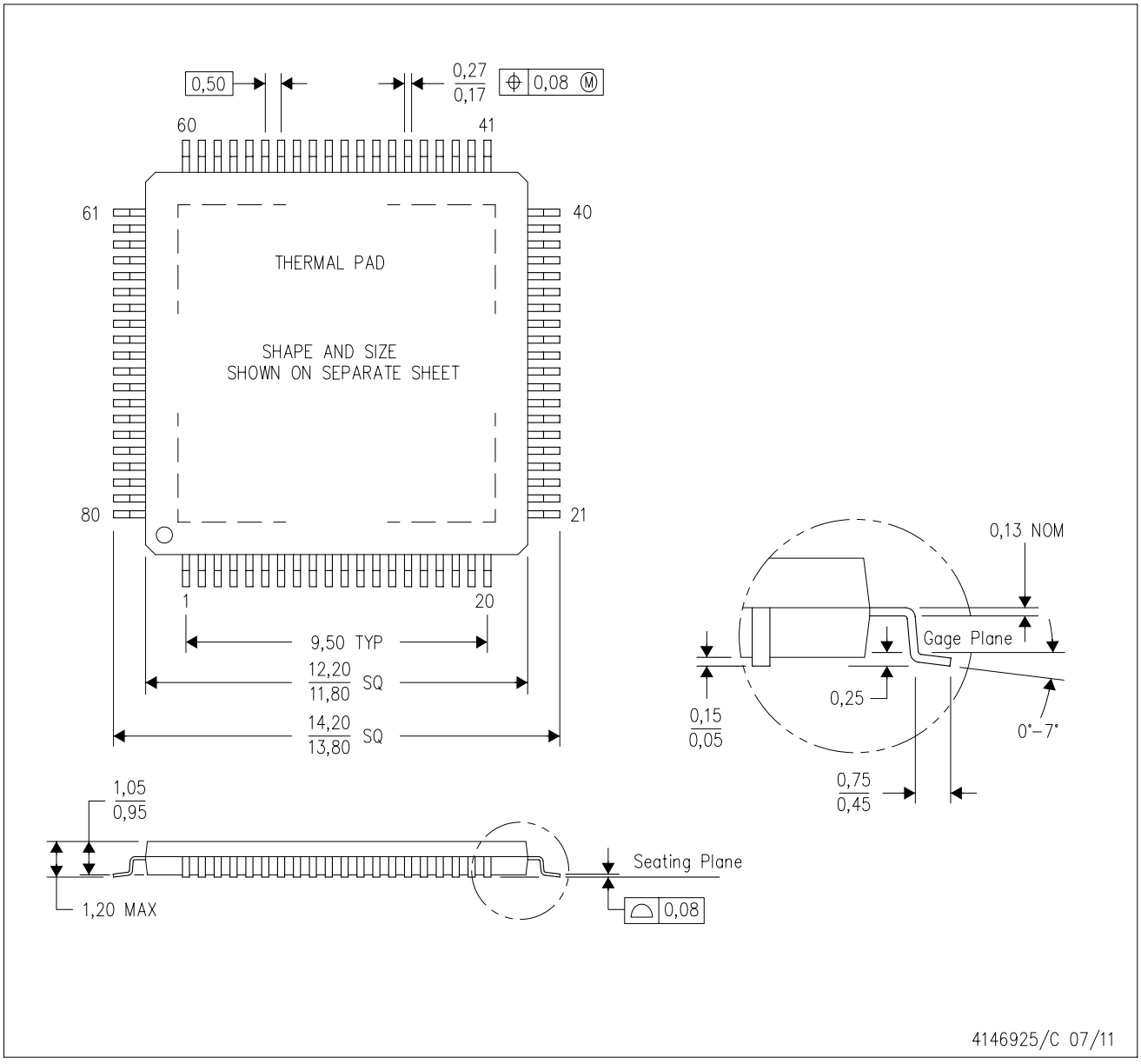
STENCIL THICKNESS	SOLDER STENCIL OPENING
0.1	7.71 X 8.61
0.125	6.9 X 7.7 (SHOWN)
0.150	6.3 X 7.03
0.175	5.83 X 6.51

4218997/A 04/2017

NOTES: (continued)

9. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
10. Board assembly site may have different recommendations for stencil design.

PFP (S–PQFP–G80) PowerPAD™ PLASTIC QUAD FLATPACK



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion
D. This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPad Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 for information regarding recommended board layout. This document is available at www.ti.com <http://www.ti.com>.
E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.
F. Falls within JEDEC MS–026

PowerPAD is a trademark of Texas Instruments.

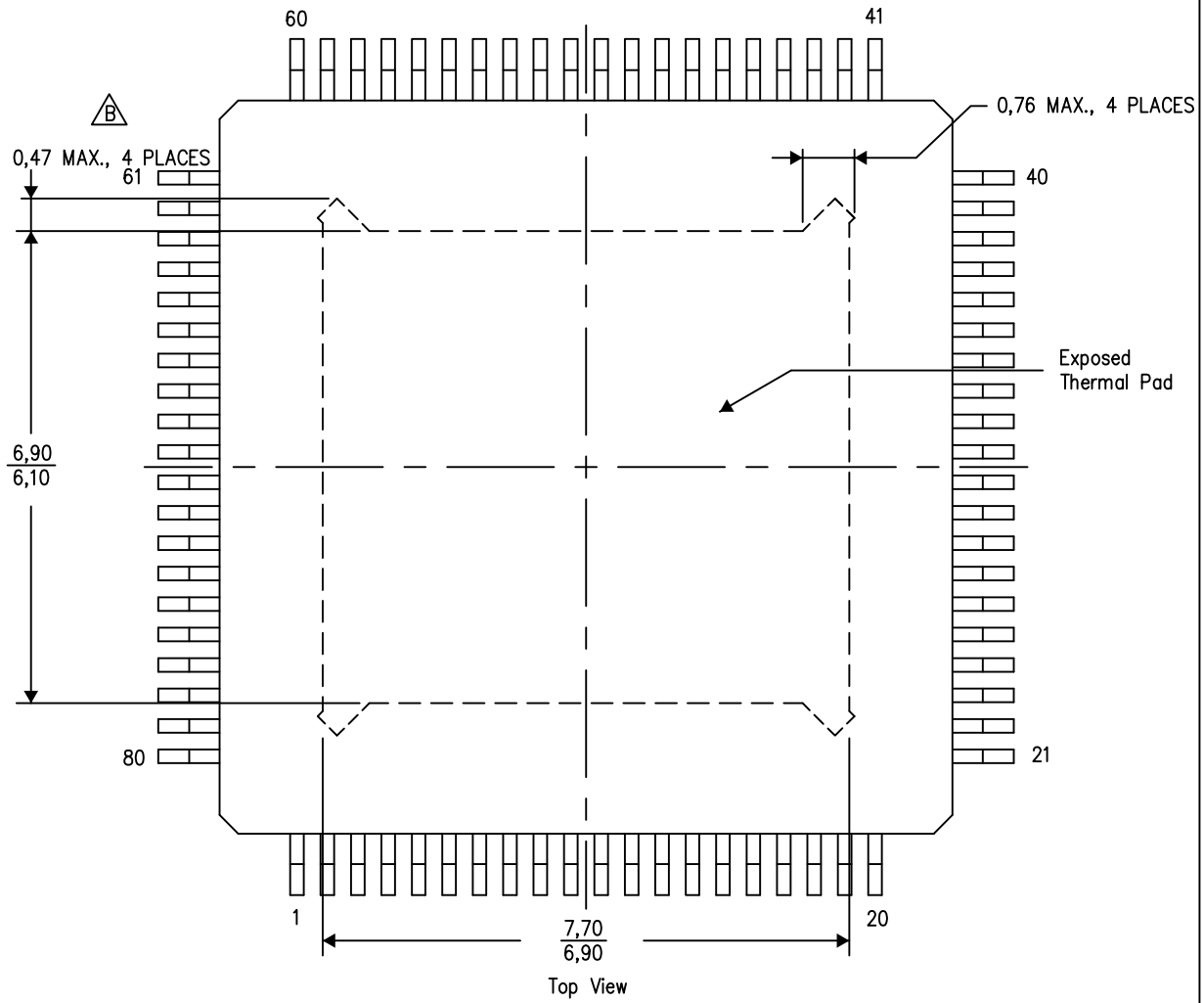
PFP (S–PQFP–G80) PowerPAD™ PLASTIC QUAD FLATPACK

THERMAL INFORMATION

This PowerPAD™ package incorporates an exposed thermal pad that is designed to be attached to a printed circuit board (PCB). The thermal pad must be soldered directly to the PCB. After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For additional information on the PowerPAD package and how to take advantage of its heat dissipating abilities, refer to Technical Brief, PowerPAD Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 and Application Brief, PowerPAD Made Easy, Texas Instruments Literature No. SLMA004. Both documents are available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



Exposed Thermal Pad Dimensions

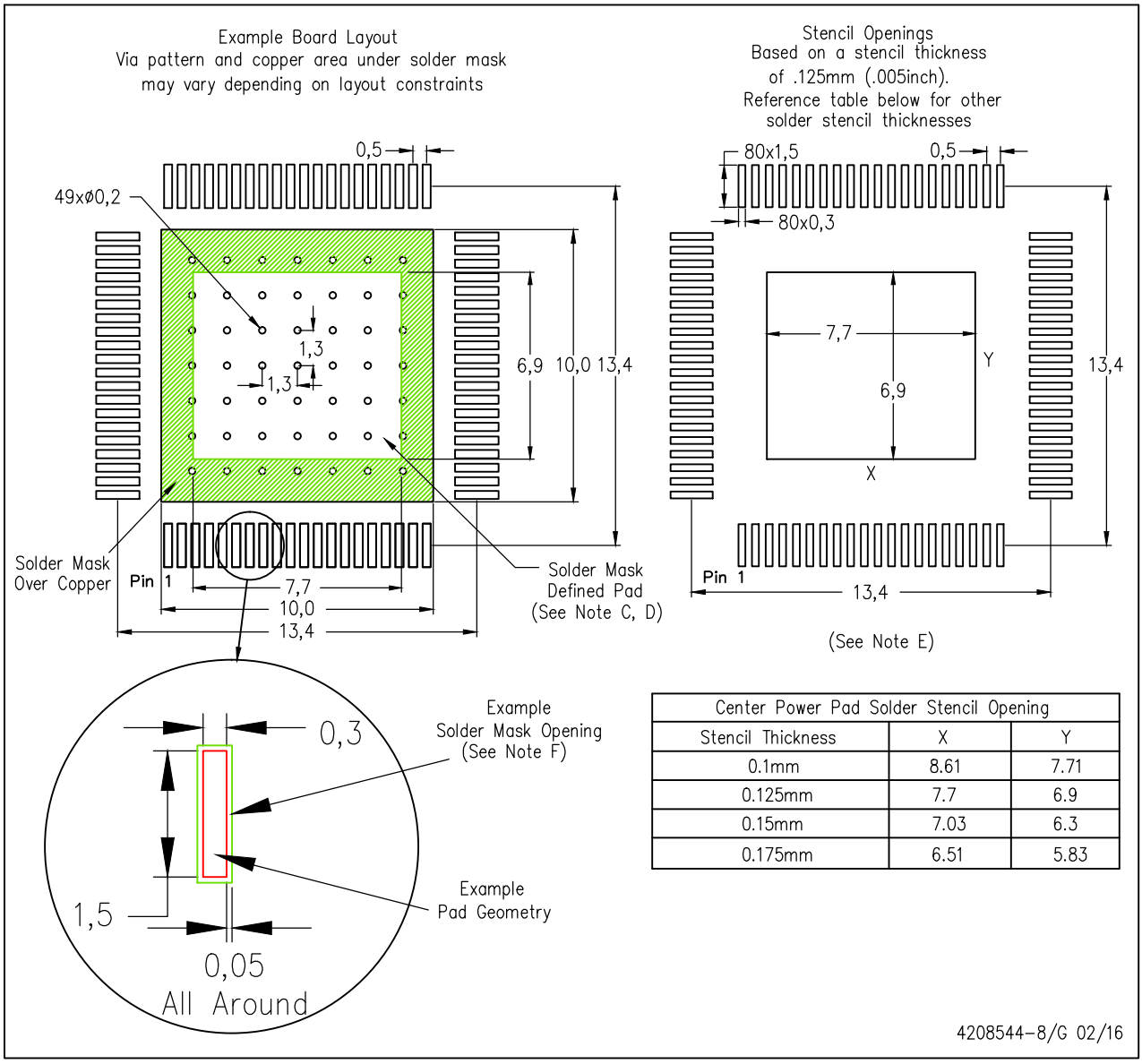
4206327–22/P 05/14

NOTE: A. All linear dimensions are in millimeters

B Tie strap features may not be present.

PowerPAD is a trademark of Texas Instruments

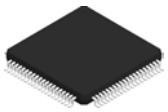
PFP (S–PQFP–G80) PowerPAD™ PLASTIC QUAD FLATPACK



Center Power Pad Solder Stencil Opening		
Stencil Thickness	X	Y
0.1mm	8.61	7.71
0.125mm	7.7	6.9
0.15mm	7.03	6.3
0.175mm	6.51	5.83

PowerPAD is a trademark of Texas Instruments.

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Customers should place a note on the circuit board fabrication drawing not to alter the center solder mask defined pad.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPad Thermally Enhanced Package, Texas Instruments Literature No. SLMA002, SLMA004, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http://www.ti.com>. Publication IPC–SM–7351 is recommended for alternate designs.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC–7525 for other stencil recommendations.
F. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

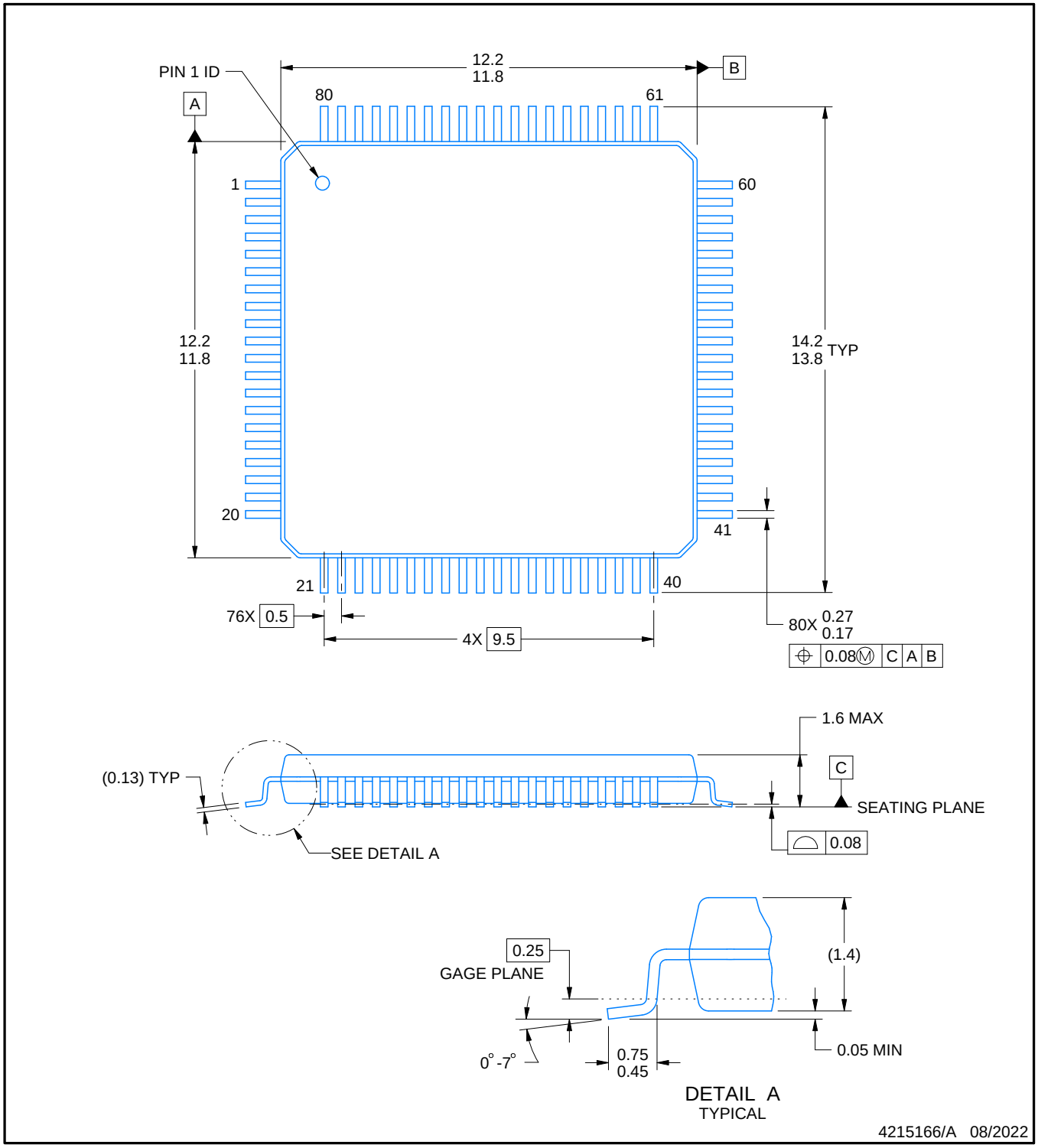


PACKAGE OUTLINE

PN0080A

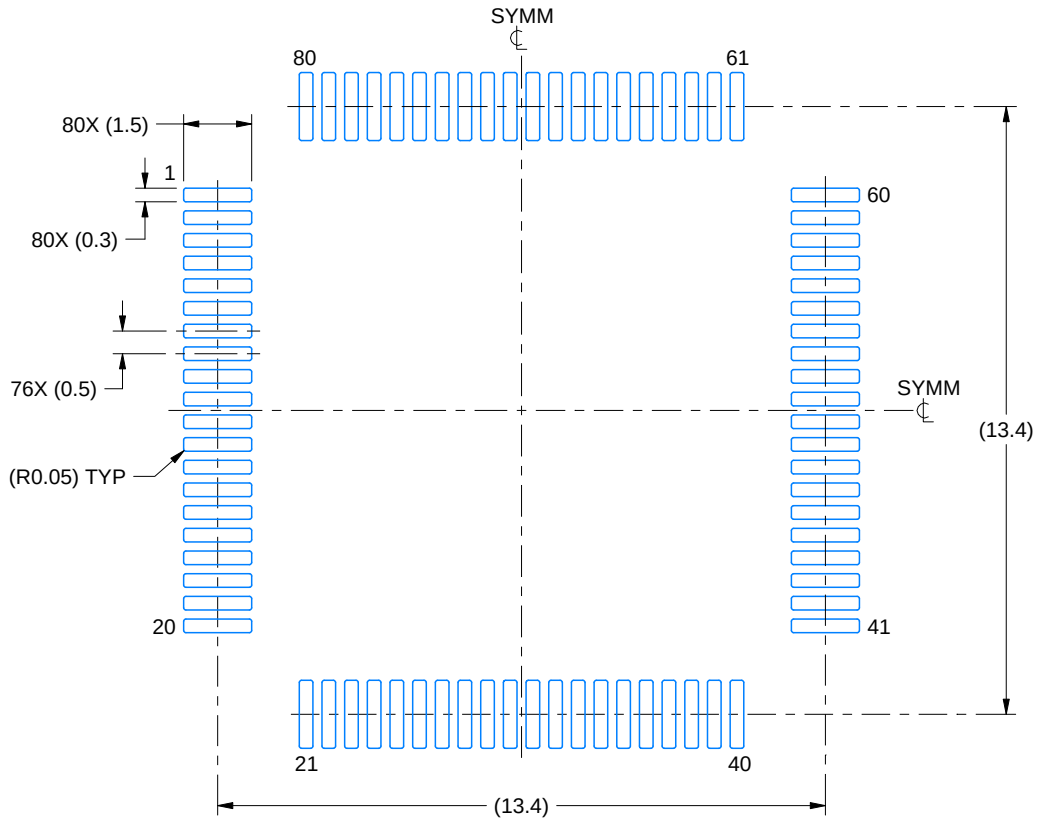
LQFP - 1.6 mm max height

PLASTIC QUAD FLATPACK

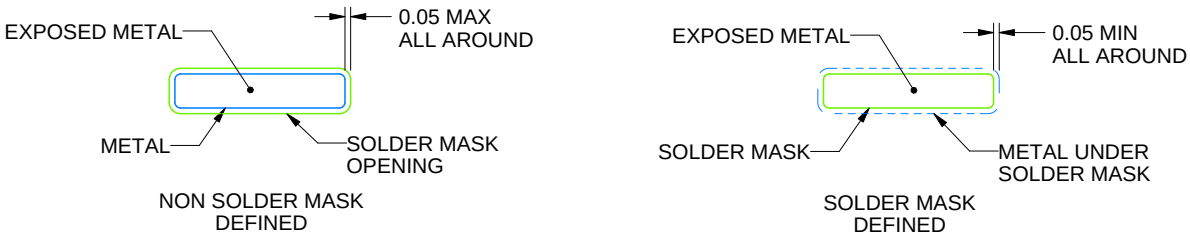


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Reference JEDEC registration MS-026.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:6X



SOLDER MASK DETAILS

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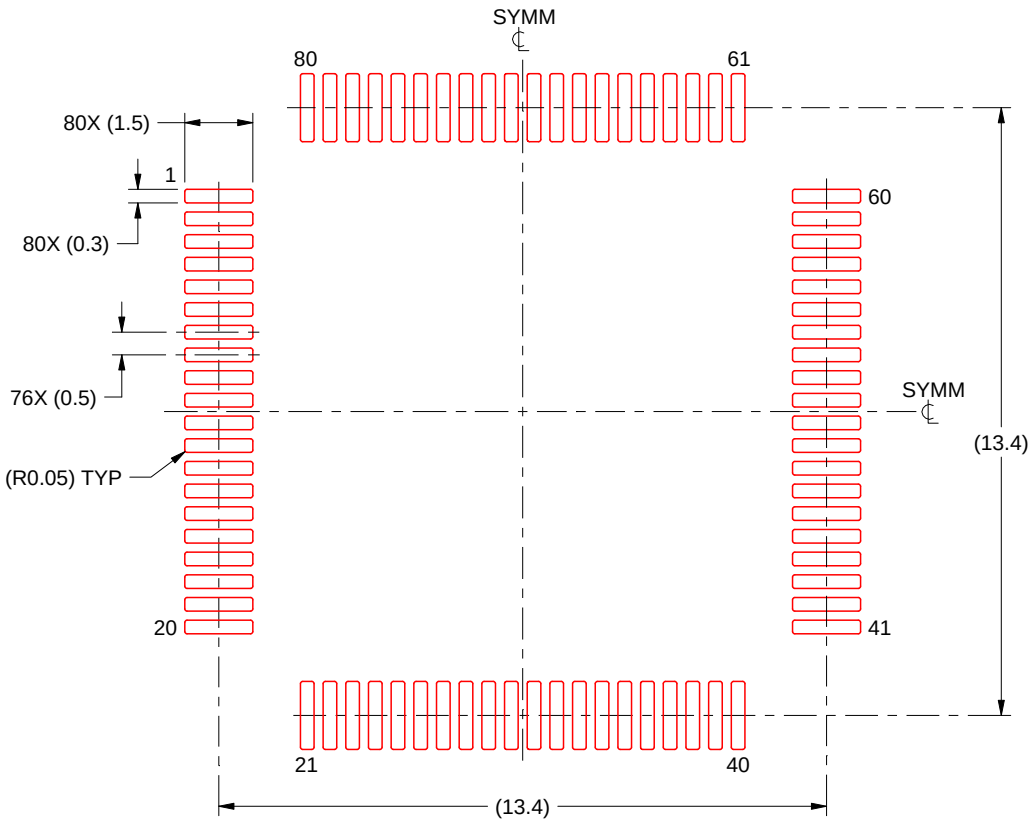
NOTES: (continued)

4. Publication IPC-7351 may have alternate designs.
5. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
6. For more information, see Texas Instruments literature number SLMA004 (www.ti.com/lit/slma004).



SOLDER PASTE EXAMPLE
BASED ON 0.1 mm THICK STENCIL
SCALE:6X

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NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

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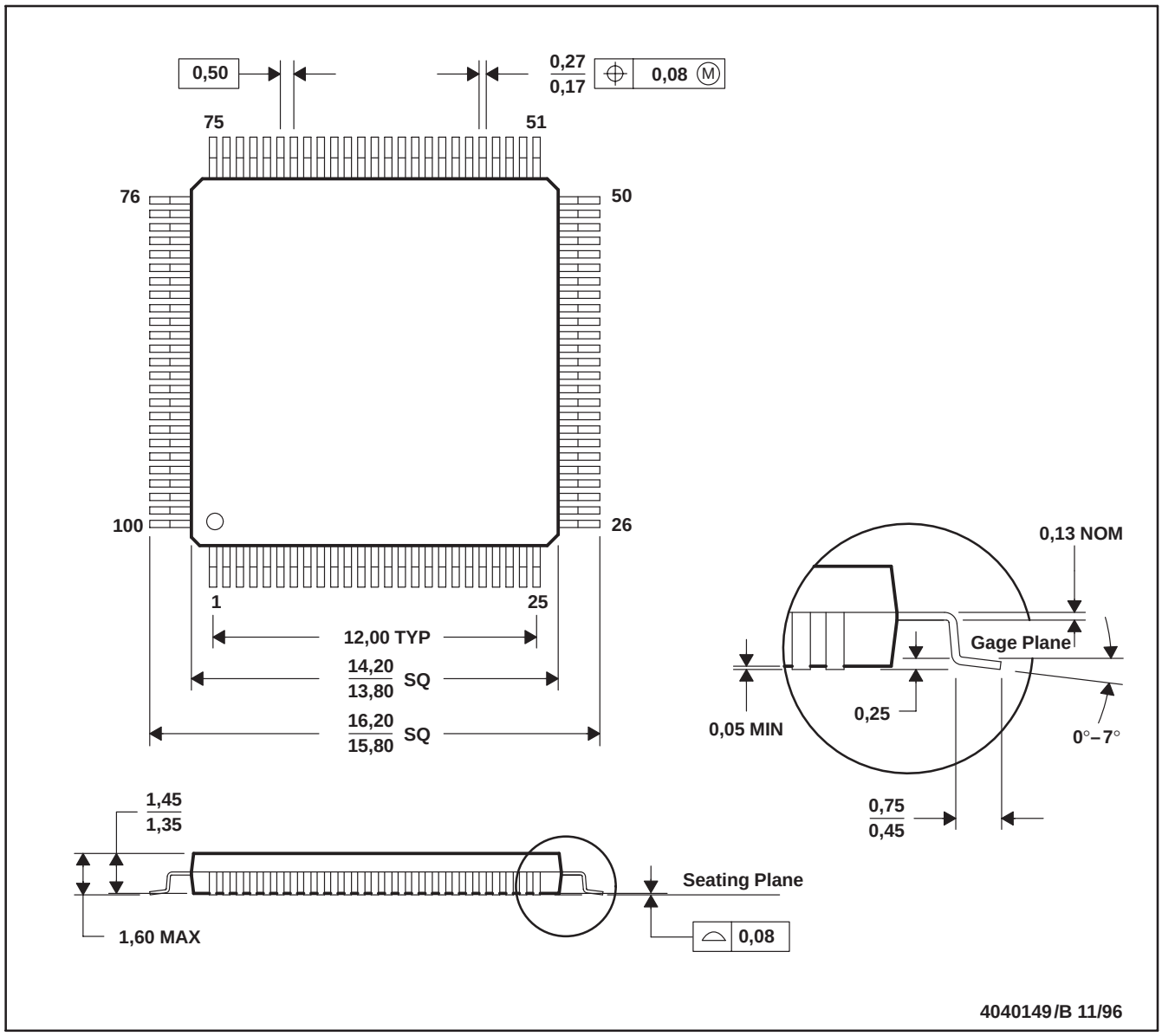
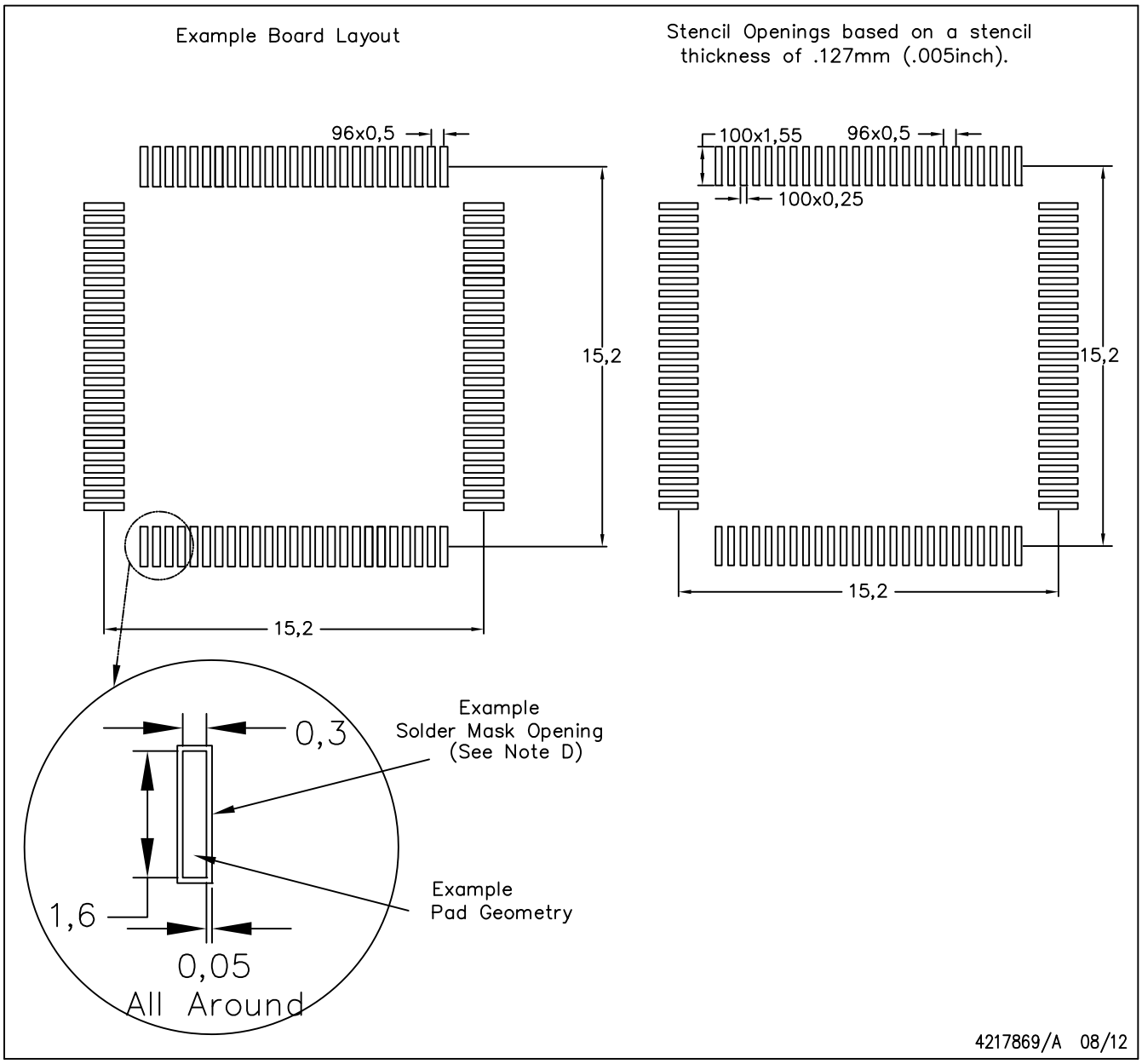
PZ (S-PQFP-G100) **PLASTIC QUAD FLATPACK**



NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS-026

PZ (S–PQFP–G100) PLASTIC QUAD FLAT PACK



NOTES:

A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC–7525 for other stencil recommendations.
D. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

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