THE DATASHEET OF

THS4521SHKQ

VERY LOW POWER, NEGATIVE RAIL INPUT, RAIL-TO-RAIL OUTPUT, FULLY DIFFERENTIAL AMPLIFIER

Check for Samples: THS4521-HT

FEATURES

- **Fully Differential Architecture**
- **Bandwidth: 40.7 MHz (210°C)**
- **Slew Rate: 353.5 V/µs (210°C)**
- **HD_2: –96 dBc at 1 kHz ($1 V_{RMS}$, R_L = 1 kΩ) (210°C)**
- **HD_3: –91.5 dBc at 1 kHz ($1 V_{RMS}$, R_L = 1 kΩ) (210°C)**
- **Input Voltage Noise: 19.95 nV/√Hz (f = 100 kHz)**
- **Open-Loop Gain: 90 dB (typ) (210°C)**
- **NRI—Negative Rail Input**
- **RRO—Rail-to-Rail Output**
- **Output Common-Mode Control (with Low Offset and Drift)**
- **Power Supply:**
  - **Voltage: 2.5 V (±1.25 V) to 3.3 V (±1.65 V)**
  - **Current: 1.4 mA/ch (3.3 V)**
- **Power-Down Capability: 10 µA (typ) (210°C)**

APPLICATIONS

- **Down-Hole Drilling**
- **High Temperature Environments**

SUPPORTS EXTREME TEMPERATURE APPLICATIONS

- **Controlled Baseline**
- **One Assembly/Test Site**
- **One Fabrication Site**
- **Available in Extreme (–55°C/210°C) Temperature Range(1)**
- **Extended Product Life Cycle**
- **Extended Product-Change Notification**
- **Product Traceability**
- **Texas Instruments high temperature products utilize highly optimized silicon (die) solutions with design and process enhancements to maximize performance over extended temperatures.**

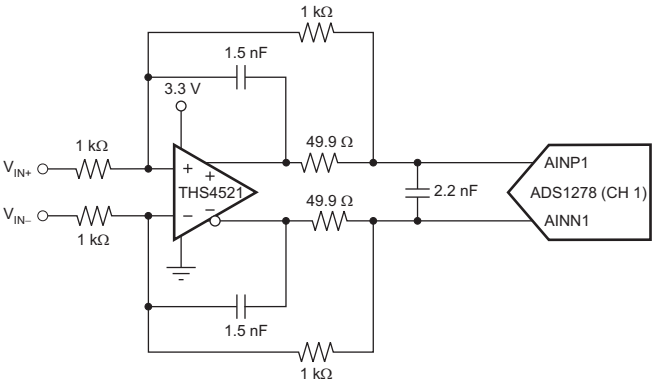
(1) Custom temperature ranges available

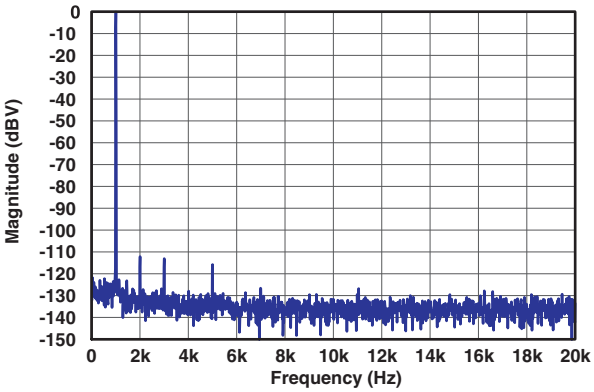
DESCRIPTION

The THS4521 is a very low-power, fully differential op amp with rail-to-rail output and an input common-mode range that includes the negative rail. This amplifier is designed for low-power data acquisition systems and high-density applications where power dissipation is a critical parameter, and provides exceptional performance in audio applications.

The THS4521 features accurate output common-mode control that allows for dc-coupling when driving analog-to-digital converters (ADCs). This control, coupled with an input common-mode range below the negative rail as well as rail-to-rail output, allows for easy interfacing between single-ended, ground-referenced signal sources. Additionally, this device is ideally suited for driving both successive-approximation register (SAR) and delta-sigma (ΔΣ) ADCs using only a single 2.5-V to 3.3-V and ground power supply.

The THS4521 is characterized for operation from –55°C to 210°C.





This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

BARE DIE INFORMATION

DIE THICKNESS	BACKSIDE FINISH	BACKSIDE POTENTIAL	BOND PAD METALLIZATION COMPOSITION	BOND PAD THICKNESS
11 mils.	Silicon with backgrind	Floating	Al-Cu (0.5%)	1380 nm

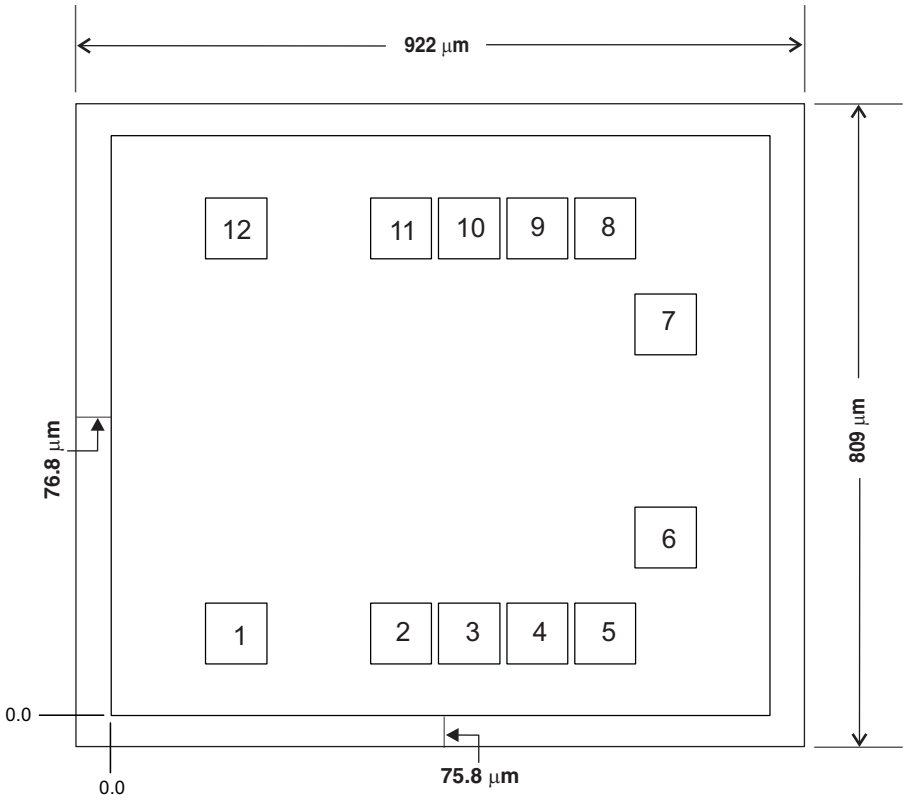


Table 1. Bond Pad Coordinates in Microns

DISCRIPTION	PAD NUMBER	X min	Y min	X max	Y max
V_{IN-}	1	80.7	3.7	165.7	88.7
V_{OCM}	2	310.6	3.7	395.6	88.7
V_{S+}	3	405.6	3.7	490.6	88.7
V_{S+}	4	500.6	3.7	585.6	88.7
V_{S+}	5	595.6	3.7	680.6	88.7
V_{OUT+}	6	679.6	137.55	764.6	222.55
V_{OUT-}	7	679.6	434.7	764.6	519.7
V_{S-}	8	595.6	568.6	680.6	653.6
V_{S-}	9	500.6	568.6	585.6	653.6
V_{S-}	10	405.6	568.6	490.6	653.6
PD	11	310.6	568.6	395.6	653.6
V_{IN+}	12	80.7	568.6	165.7	653.6

ORDERING INFORMATION(1)

T_A	PACKAGE(2)	ORDERABLE PART NUMBER	TOP-SIDE MARKING
–55°C to175°C	D	THS4521HD	THS4521
–55°C to 210°C	KGD (bare die)	THS4521SKGD1	NA
	HKJ	THS4521SHKJ	THS4521SHKJ
	HKQ	THS4521SHKQ	THS4521SHKQ

(1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI web site at www.ti.com.
(2) Package drawings, thermal data, and symbolization are available at www.ti.com/packaging.

ABSOLUTE MAXIMUM RATINGS(1)

Over operating free-air temperature range (unless otherwise noted).

			UNIT
Supply Voltage, $V_{S–}$ to V_{S+}		3.6	V
Input/Output Voltage, V_I ($V_{IN±}$, $V_{OUT±}$, V_{OCM} pins)		($V_{S–}$) – 0.7 to (V_{S+}) + 0.7V	V
Differential Input Voltage, V_{ID}		1	V
Output Current, I_O		100	mA
Input Current, I_I ($V_{IN±}$, V_{OCM} pins)		10	mA
Continuous Power Dissipation		See Thermal Characteristic Specifications	
Maximum Junction Temperature, T_J (continuous operation, long-term reliability)(2)		217	°C
Operating Free-air Temperature Range, T_A	D package	–40 to 175	°C
	KGD, HKJ, HKQ packages	–55 to 210	
Storage Temperature Range, T_{STG}		–65 to 210	°C
ESD Rating:	Human Body Model (HBM)	1300	V
	Charge Device Model (CDM)	1000	V
	Machine Model (MM)	50	V

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) Refer to Figure 1 for expected life time.

THERMAL CHARACTERISTICS FOR D PACKAGE

over operating free-air temperature range (unless otherwise noted)

PARAMETER		MIN	TYP	MAX	UNIT
θ_{JC}(1)	Junction-to-case thermal resistance			72.5	°C/W
θ_{JA}	Junction-to-ambient thermal resistance			118.5	°C/W

(1) Taken as per JESD51.

THERMAL CHARACTERISTICS FOR HKJ OR HKQ PACKAGE

over operating free-air temperature range (unless otherwise noted)

PARAMETER			MIN	TYP	MAX	UNIT
θ_{JC}	Junction-to-case thermal resistance	to ceramic side of case			5.7	°C/W
		to top of case lid (metal side of case)			13.7	

ELECTRICAL CHARACTERISTICS: $V_{S+} - V_{S-} = 3.3$ V

At V_{S+} = 3.3 V, V_{S-} = 0 V, V_{OCM} = open, V_{OUT} = 2 V_{PP} (differential), R_L = 1 kΩ differential, G = 1 V/V, single-ended input, differential output, input and output referenced to midsupply, unless otherwise noted.

PARAMETER	CONDITIONS	-55°C to 125°C			175°C			-55°C to 210°C			UNIT	TEST LEVEL(1)
		MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX		
AC PERFORMANCE												
Small-Signal Bandwidth	V_{OUT} = 100 mV_{PP}, G = 1		104.3			40.7			40.7		MHz	C
	V_{OUT} = 100 mV_{PP}, G = 2		42			12.5			12.5		MHz	C
	V_{OUT} = 100 mV_{PP}, G = 5		12.2			3.15			3.15		MHz	C
	V_{OUT} = 100 mV_{PP}, G = 10		8.1			2.2			2.2		MHz	C
Gain Bandwidth Product	V_{OUT} = 100 mV_{PP}, G = 10		81			22			22		MHz	C
Large-Signal Bandwidth	V_{OUT} = 2 V_{PP}, G = 1		84			22			22		MHz	C
Bandwidth for 0.1-dB Flatness	V_{OUT} = 2 V_{PP}, G = 1		18.1			5.4			5.4		MHz	C
Rising Slew Rate (Differential)	V_{OUT} = 2-V Step, G = 1, R_L = 200 Ω		377.5			353.5			353.5		V/µs	C
Falling Slew Rate (Differential)	V_{OUT} = 2-V Step, G = 1, R_L = 200 Ω		422.5			392.5			392.5		V/µs	C
Overshoot	V_{OUT} = 2-V Step, G = 1, R_L = 200 Ω		6.75			8.85			8.85		%	C
Undershoot	V_{OUT} = 2-V Step, G = 1, R_L = 200 Ω		7.85			11.45			11.45		%	C
Rise Time	V_{OUT} = 2-V Step, G = 1, R_L = 200 Ω		13.5			15.9			15.9		ns	C
Fall Time	V_{OUT} = 2-V Step, G = 1, R_L = 200 Ω		11.4			14.6			14.6		ns	C
Settling Time to 1%	V_{OUT} = 2-V Step, G = 1, R_L = 200 Ω		18.5			23.5			23.5		ns	C
HARMONIC DISTORTION												
2nd harmonic	f = 1 kHz, V_{OUT} = 1 V_{RMS}, G = 1(2), differential input		–115			–96			–96		dBc	C
	f = 1 MHz, V_{OUT} = 2 V_{PP}, G = 1		–77			–68.5			–68.5		dBc	C
3rd harmonic	f = 1 kHz, V_{OUT} = 1 V_{RMS}, G = 1(2), differential input		–116			–91.5			–91.5		dBc	C
	f = 1 MHz, V_{OUT} = 2 V_{PP}, G = 1		–80.5			–68.5			–68.5		dBc	C
Second-Order Intermodulation Distortion	Two-tone, f_1 = 2 kHz, f_2 = 500 Hz, V_{OUT} = 1 V_{RMS} envelope		–91.5			–79.5			–79.5		dBc	C
Third-Order Intermodulation Distortion	Two-tone, f_1 = 2 kHz, f_2 = 500 Hz, V_{OUT} = 1 V_{RMS} envelope		–95.5			–79.5			–79.5		dBc	C
Input Voltage Noise	f > 10 kHz		9.05			19.95			19.95		nV/√Hz	C
Input Current Noise	f > 100 kHz		1.8			2.45			2.45		pA/√Hz	C
Overdrive Recovery Time	Overdrive = ±0.5 V		116.5			126			126		ns	C
Output Balance Error	V_{OUT} = 100 mV, f ≤ 2 MHz (differential input)		–51.5			–45.5			–45.5		dB	C
Closed-Loop Output Impedance	f = 1 MHz (differential)		0.3								Ω	C

(1) Test levels: **(A)** 100% tested. **(B)** Limits set by characterization and simulation. **(C)** Typical value only for information.
(2) Not directly measureable; calculated using noise gain of 101.

ELECTRICAL CHARACTERISTICS: $V_{S+} - V_{S-} = 3.3$ V (continued)

At $V_{S+} = 3.3$ V, $V_{S-} = 0$ V, V_{OCM} = open, $V_{OUT} = 2\ V_{PP}$ (differential), $R_L = 1$ kΩ differential, G = 1 V/V, single-ended input, differential output, input and output referenced to midsupply, unless otherwise noted.

PARAMETER	CONDITIONS	-55°C to 125°C			175°C			-55°C to 210°C			UNIT	TEST LEVEL(1)
		MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX		
DC PERFORMANCE												
Open-Loop Voltage Gain (A_{OL})			102			81.9			90		dB	A
Input-Referred Offset Voltage			±0.1	±5		±0.13			±0.43	±11.5	mV	A
Input offset voltage drift(3)			±1	±28		±10			±2	±50	µV/°C	B
Input Bias Current			±0.75	±3.3		±0.75	±4.5		±0.78	±4.5	µA	A
Input bias current drift(3)			±3.3	±14		±4.7			±4.8	±17	nA/°C	B
Input Offset Current			±0.3	±1.7		±0.5	±3.2		±0.5	±3.5	µA	A
Input offset current drift(3)			±1.1	±8		±3.6			±1.26	±9	nA/°C	B
INPUT												
Common-Mode Input Voltage Low			–0.1	0		-0.1			–0.1	0	V	A
Common-Mode Input Voltage High		1.8	1.9			1.9		1.8	1.9		V	A
Common-Mode Rejection Ratio (CMRR)		80	105			95		74	98		dB	A
Input Resistance			154‖3.2			12.3‖46			12.3‖46		kΩ‖pF	C
OUTPUT												
Output Voltage Low			0.09	0.25		0.3			0.09	0.31	V	A
Output Voltage High		2.95	3.11			3.11		2.85	3.05		V	A
Output Current Drive (for linear operation)	R_L = 50 Ω		±35(4)			±33(4)			±33(4)		mA	C
POWER SUPPLY												
Specified Operating Voltage		2.5		3.6	2.5		3.6	2.5		3.6	V	A
Quiescent Operating Current, per channel		0.85	1	1.3	0.9	1.16	1.4	0.9	1.1	1.4	mA	A
Power-Supply Rejection Ratio (±PSRR)		66	85		62.5	74		60	80		dB	A
POWER DOWN												
Enable Voltage Threshold	Assured *on* above 2.2 V		1	2.2		1	2.2		1	2.2	V	A
Disable Voltage Threshold	Assured *off* below 0.7 V	0.7	1.6		0.7	1.6		0.7	1.6		V	A
Disable Pin Bias Current			1			1			1		µA	C
Power Down Quiescent Current			2			10			10		µA	C
Turn-On Time Delay	Time to V_{OUT} = 90% of final value, V_{IN}= 2 V, R_L = 200 Ω		86.5			99			99		ns	C
Turn-Off Time Delay	Time to V_{OUT} = 10% of original value, V_{IN}= 2 V, R_L = 200 Ω		136			145			144.5		ns	C
V_{OCM} VOLTAGE CONTROL												
Small-Signal Bandwidth			21			13			13		MHz	C

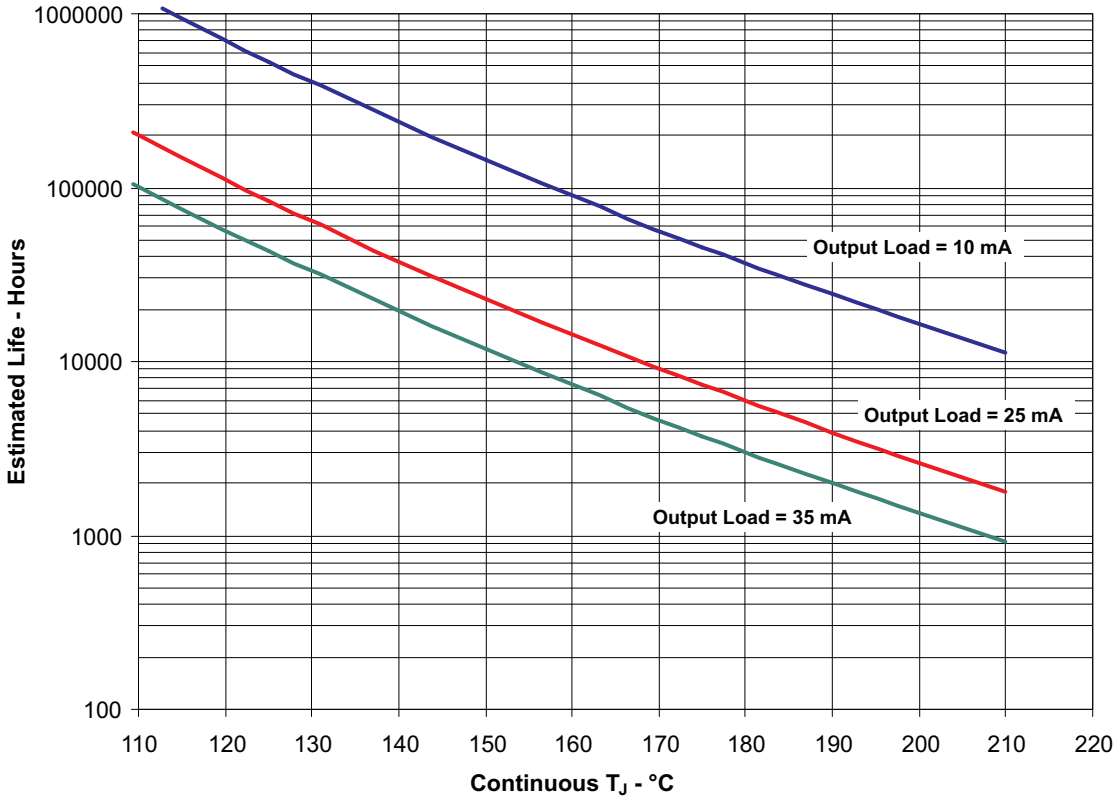
(3) Input Offset Voltage Drift, Input Bias Current Drift and Input Offset Current Drift are average values calculated by taking data at -55°C and 125°C, computing the difference and dividing by 180. High temperature drift data is an average value calculated by taking data at -55°C and 210°C, computing the difference and diving by 265.

(4) Continuous operation with high current loads at elevated temperature may affect product reliability. Refer to operating lifetime chart (Figure 1).

ELECTRICAL CHARACTERISTICS: $V_{S+} - V_{S-} = 3.3$ V (continued)

At $V_{S+} = 3.3$ V, $V_{S-} = 0$ V, V_{OCM} = open, $V_{OUT} = 2\ V_{PP}$ (differential), $R_L = 1$ kΩ differential, G = 1 V/V, single-ended input, differential output, input and output referenced to midsupply, unless otherwise noted.

PARAMETER	CONDITIONS	-55°C to 125°C			175°C			-55°C to 210°C			UNIT	TEST LEVEL(1)
		MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX		
Slew Rate			49			39			39		V/µs	C
Gain		0.97	0.99	1.02	0.97	1	1.03	0.97	1	1.03	V/V	A
Common-Mode Offset Voltage from V_{OCM} Input	Measured at V_{OUT} with V_{OCM} input driven, V_{OCM} = 1.65 V ±0.5 V		±0.2	±4		±0.7			±0.7	±10	mV	A
Input Bias Current	V_{OCM} = 1.65 V ±0.5 V		±0.9	±2.73		±0.27	±2.75		±0.91	±2.75	µA	A
V_{OCM} Voltage Range		1.01	0.8 to 2.5	2.3		0.8 to 2.5		1.09	0.8 to 2.5	2.3	V	A
Input Impedance			114‖3.6			148‖3.7			148‖3.7		kΩ‖pF	C
Default Output Common-Mode Voltage Offset from (V_{S+} – V_{S-})/2	Measured at V_{OUT} with V_{OCM} input open		±0.3	±5		±0.6	±10		±0.6	±10	mV	A



(1) See data sheet for absolute maximum and minimum recommended operating conditions.

(2) Silicon operating life design goal is 10 years at 105°C junction temperature (does not include package interconnect life).

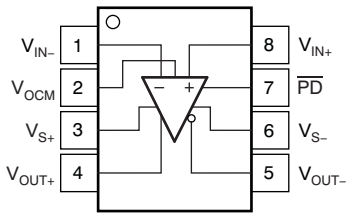
(3) The predicted operating lifetime vs. junction temperature is based on reliability modeling using electromigration as the dominant failure mechanism affecting device wearout for the specific device process and design characteristics.

(4) Device is qualified to ensure reliable operation for 1000 hours at maximum rated temperature. This includes, but is not limited to temperature bake, temperature cycle, electromigration, bond intermetallic life, and mold compound life. Such qualification testing should not be viewed as justifying use of this component beyond specified performance and environmental limits. For plastic package only.

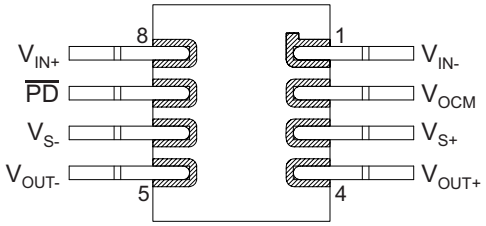
Figure 1. THS4521SHKJ/SHKQ/SKGD1 Operating Life Derating Chart

DEVICE INFORMATION

D OR HKJ PACKAGE
(TOP VIEW)



HKQ PACKAGE
(TOP VIEW)



HKQ as formed or HKJ mounted dead bug

TERMINAL FUNCTIONS

PIN NO.	NAME	DESCRIPTION
1	V_{IN-}	Inverting amplifier input
2	V_{OCM}	Common-mode voltage input
3	V_{S+}	Amplifier positive power-supply input
4	V_{OUT+}	Noninverting amplifier output
5	V_{OUT-}	Inverting amplifier output
6	V_{S-}	Amplifier negative power-supply input. Note that V_{S-} is tied together on multi-channel devices.
7	$\overline{PD}$	Power down. $\overline{PD}$ = logic low puts device into low-power mode. $\overline{PD}$ = logic high or open for normal operation.
8	V_{IN+}	Noninverting amplifier input

TYPICAL CHARACTERISTICS

Table of Graphs[(1)]: $V_{S+} - V_{S-} = 3.3$ V

TITLE	FIGURE
Small-Signal Frequency Response	Figure 2
Large-Signal Frequency Response	Figure 3
Large- and Small-Signal Pulse Response	Figure 4
Slew Rate vs V_{OUT} Step	Figure 5
Overdrive Recovery	Figure 6
10-kHz Output Spectrum on AP Analyzer	Figure 7
Harmonic Distortion vs Frequency	Figure 8
Harmonic Distortion vs Output Voltage at 1 MHz	Figure 9
Harmonic Distortion vs Gain at 1 MHz	Figure 10
Harmonic Distortion vs Load at 1 MHz	Figure 11
Harmonic Distortion vs V_{OCM} at 1 MHz	Figure 12
Two-Tone, Second- and Third-Order Intermodulation Distortion vs Frequency	Figure 13
Single-Ended Output Voltage Swing vs Load Resistance	Figure 14
Main Amplifier Differential Output Impedance vs Frequency	Figure 15
Frequency Response vs C_{LOAD} (R_{LOAD} = 1 kΩ)	Figure 16
R_O vs C_{LOAD} (R_{LOAD} = 1 kΩ)	Figure 17
Rejection Ratio vs Frequency	Figure 18
Turn-on Time	Figure 19
Turn-off Time	Figure 20
Input-Referred Voltage Noise and Current Noise Spectral Density	Figure 21
Main Amplifier Differential Open-Loop Gain and Phase	Figure 22
Output Balance Error vs Frequency	Figure 23
V_{OCM} Small-Signal Frequency Response	Figure 24
V_{OCM} Large-Signal Frequency Response	Figure 25
V_{OCM} Input Impedance vs Frequency	Figure 26

(1) Graphs are plotted for room temperature only and are given only for reference.

TYPICAL CHARACTERISTICS: $V_{S+} - V_{S-} = 3.3$ V

At V_{S+} = +3.3 V, V_{S-} = 0 V, V_{OCM} = open, V_{OUT} = 2 V_{PP} (differential), R_L = 1 kΩ differential, G = 1 V/V, single-ended input, differential output, and input and output referenced to midsupply, unless otherwise noted. Graphs are plotted for room temperature only and are given only for reference.

SMALL-SIGNAL FREQUENCY RESPONSE

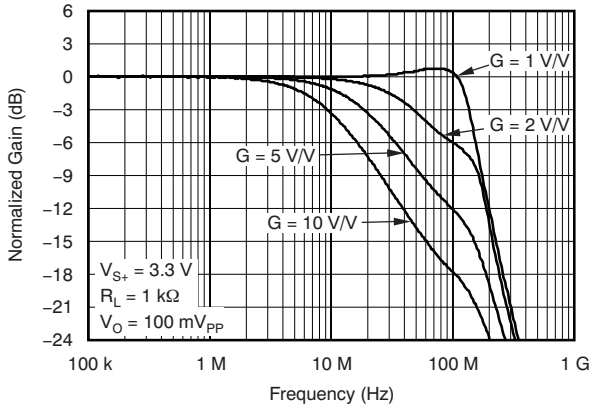


Figure 2.

LARGE-SIGNAL FREQUENCY RESPONSE

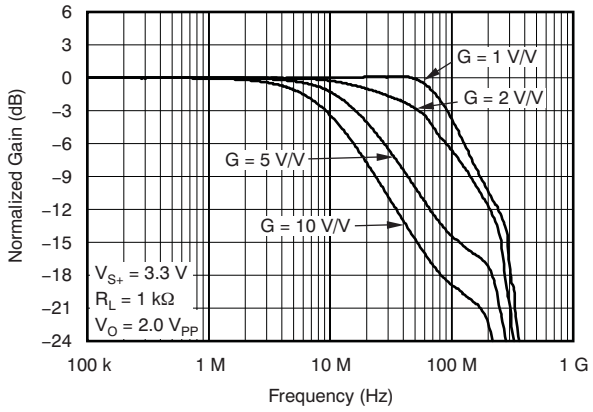


Figure 3.

LARGE- AND SMALL-SIGNAL PULSE RESPONSE

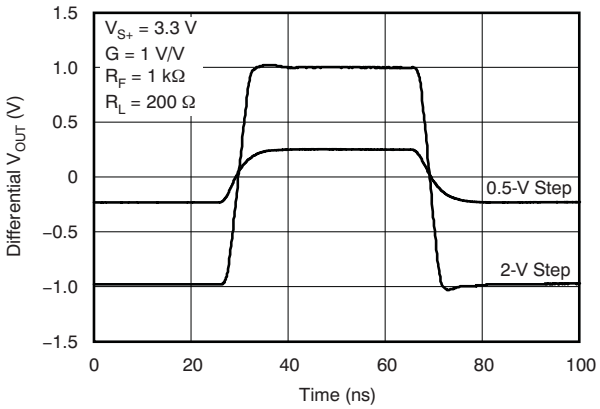


Figure 4.

SLEW RATE vs V_{OUT}

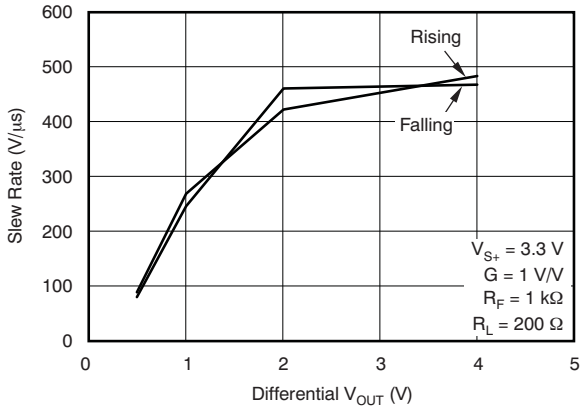


Figure 5.

OVERDRIVE RECOVERY

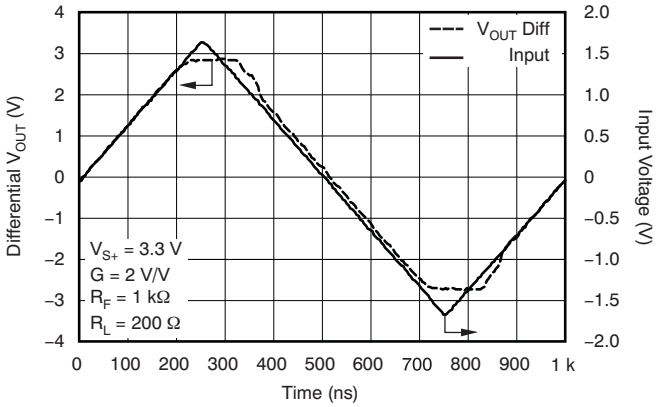


Figure 6.

10-kHz OUTPUT SPECTRUM ON AP ANALYZER

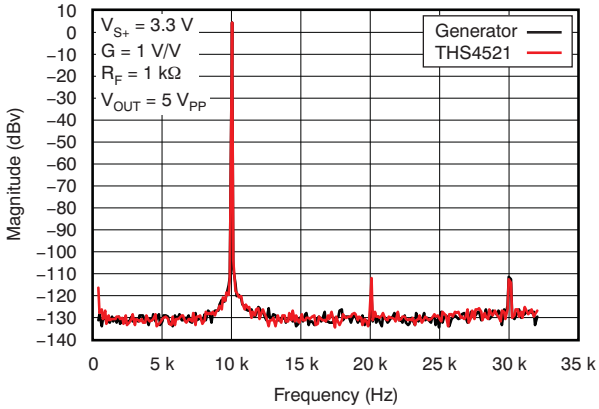


Figure 7.

TYPICAL CHARACTERISTICS: $V_{S+} - V_{S-} = 3.3$ V (continued)

At V_{S+} = +3.3 V, V_{S-} = 0 V, V_{OCM} = open, V_{OUT} = 2 V_{PP} (differential), R_L = 1 kΩ differential, G = 1 V/V, single-ended input, differential output, and input and output referenced to midsupply, unless otherwise noted. Graphs are plotted for room temperature only and are given only for reference.

HARMONIC DISTORTION vs FREQUENCY

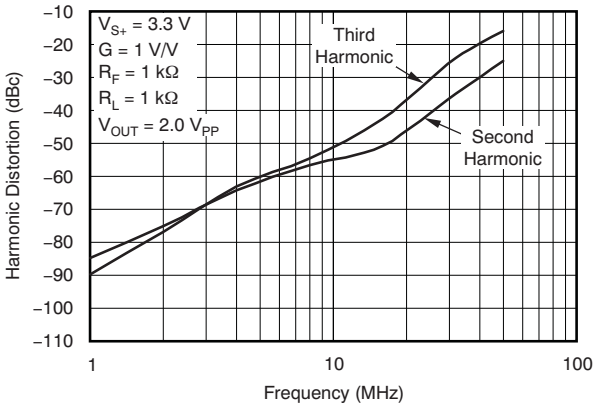


Figure 8.

HARMONIC DISTORTION vs V_{OUT} AT 1 MHZ

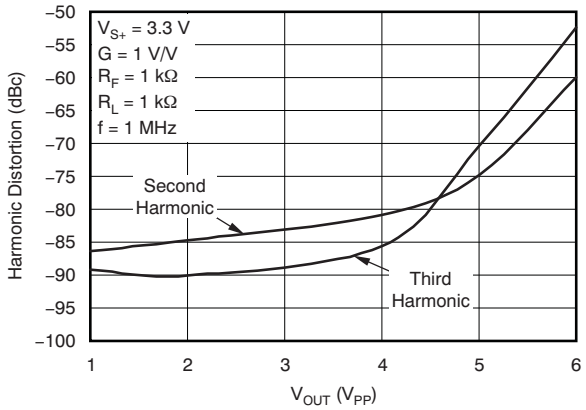


Figure 9.

HARMONIC DISTORTION vs GAIN AT 1 MHZ

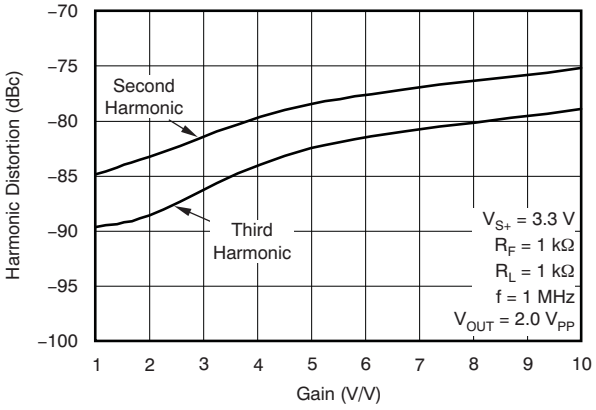


Figure 10.

HARMONIC DISTORTION vs LOAD AT 1 MHZ

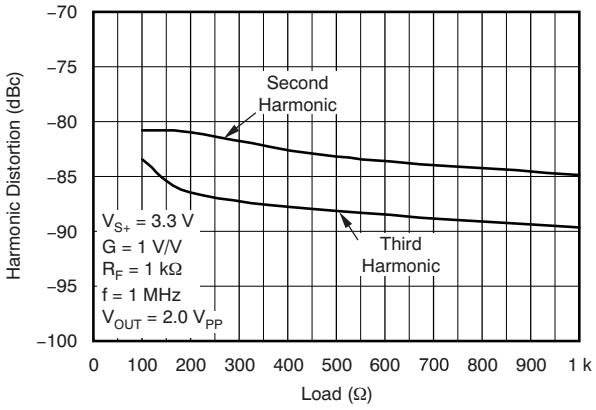


Figure 11.

TYPICAL CHARACTERISTICS: $V_{S+} - V_{S-} = 3.3$ V (continued)

At V_{S+} = +3.3 V, V_{S-} = 0 V, V_{OCM} = open, V_{OUT} = 2 V_{PP} (differential), R_L = 1 kΩ differential, G = 1 V/V, single-ended input, differential output, and input and output referenced to midsupply, unless otherwise noted. Graphs are plotted for room temperature only and are given only for reference.

HARMONIC DISTORTION vs V_{OCM} AT 1 MHZ

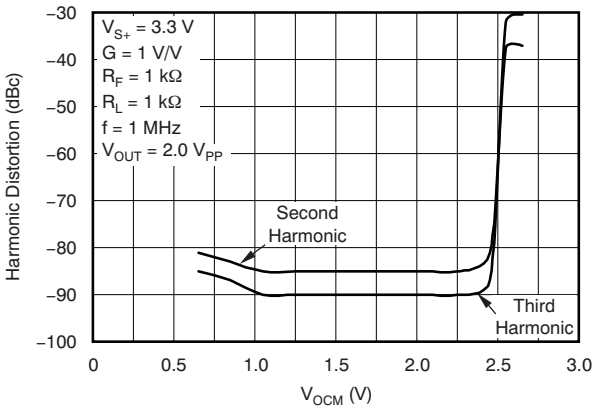


Figure 12.

TWO-TONE INTERMODULATION DISTORTION vs FREQUENCY

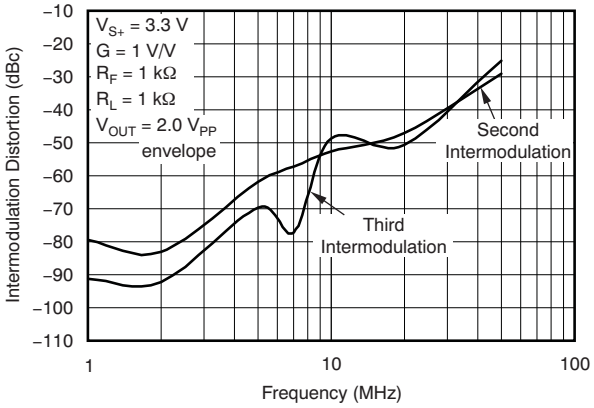


Figure 13.

SINGLE-ENDED OUTPUT VOLTAGE SWING vs LOAD RESISTANCE

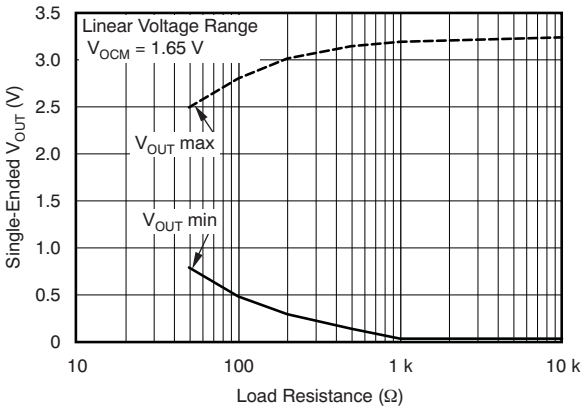


Figure 14.

MAIN AMPLIFIER DIFFERENTIAL OUTPUT IMPEDANCE vs FREQUENCY

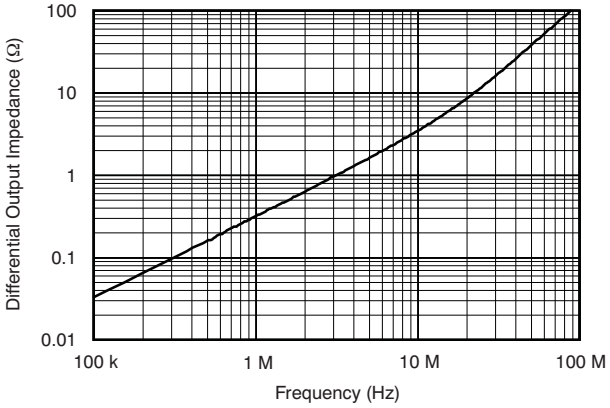


Figure 15.

TYPICAL CHARACTERISTICS: $V_{S+} - V_{S-} = 3.3$ V (continued)

At V_{S+} = +3.3 V, V_{S-} = 0 V, V_{OCM} = open, V_{OUT} = 2 V_{PP} (differential), R_L = 1 kΩ differential, G = 1 V/V, single-ended input, differential output, and input and output referenced to midsupply, unless otherwise noted. Graphs are plotted for room temperature only and are given only for reference.

FREQUENCY RESPONSE vs C_{LOAD}
R_{LOAD} = 1 kΩ

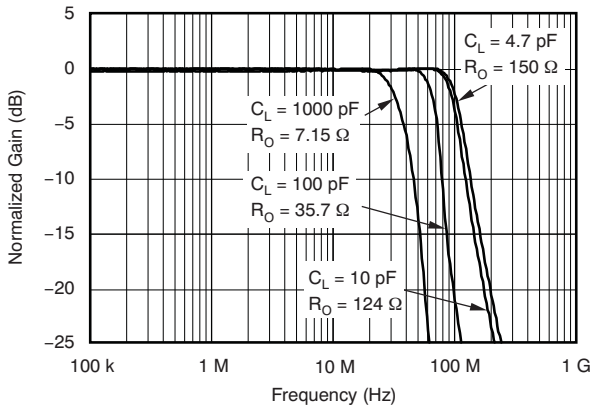


Figure 16.

R_O vs C_{LOAD}
R_{LOAD} = 1 kΩ

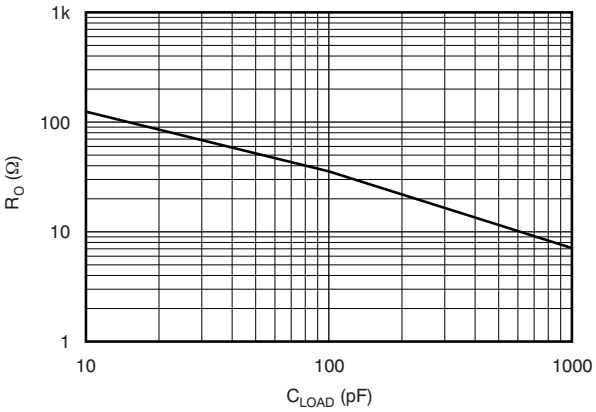


Figure 17.

REJECTION RATIO vs FREQUENCY

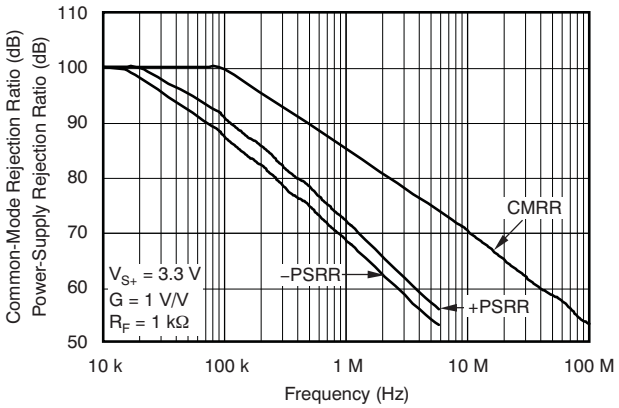


Figure 18.

TURN-ON TIME

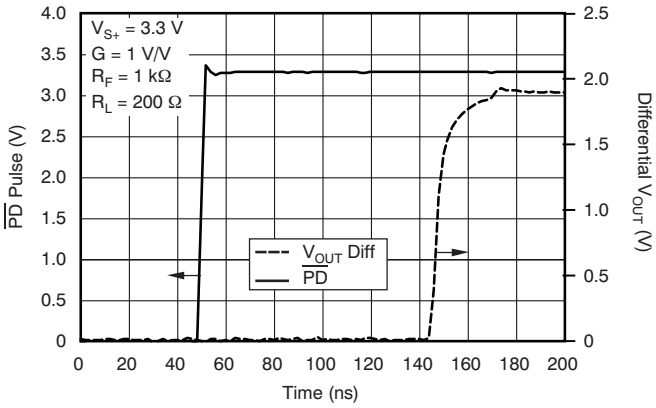


Figure 19.

TURN-OFF TIME

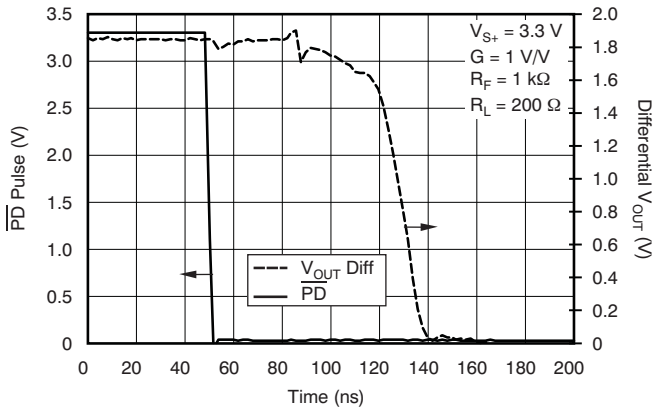


Figure 20.

INPUT-REFERRED VOLTAGE AND CURRENT NOISE SPECTRAL DENSITY

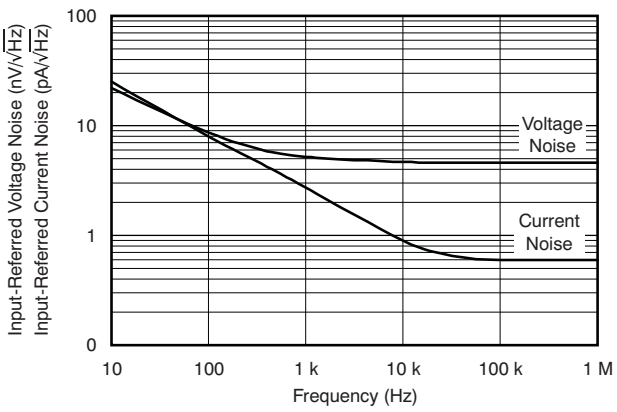


Figure 21.

TYPICAL CHARACTERISTICS: $V_{S+} - V_{S-} = 3.3$ V (continued)

At V_{S+} = +3.3 V, V_{S-} = 0 V, V_{OCM} = open, V_{OUT} = 2 V_{PP} (differential), R_L = 1 kΩ differential, G = 1 V/V, single-ended input, differential output, and input and output referenced to midsupply, unless otherwise noted. Graphs are plotted for room temperature only and are given only for reference.

MAIN AMPLIFIER
DIFFERENTIAL OPEN-LOOP GAIN AND PHASE

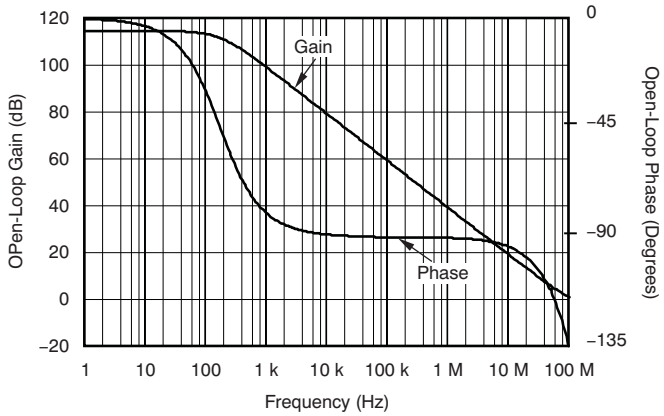


Figure 22.

OUTPUT BALANCE ERROR
vs FREQUENCY

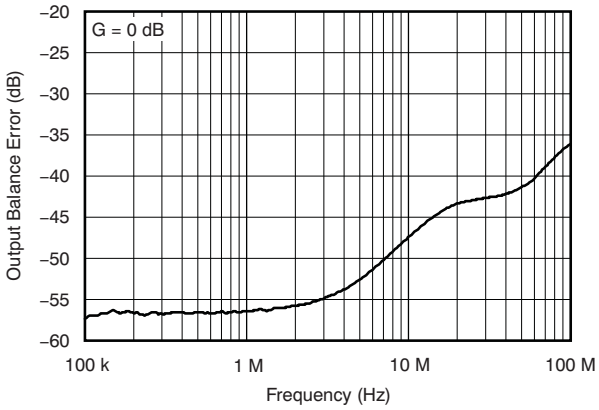


Figure 23.

V_{OCM} SMALL-SIGNAL FREQUENCY RESPONSE

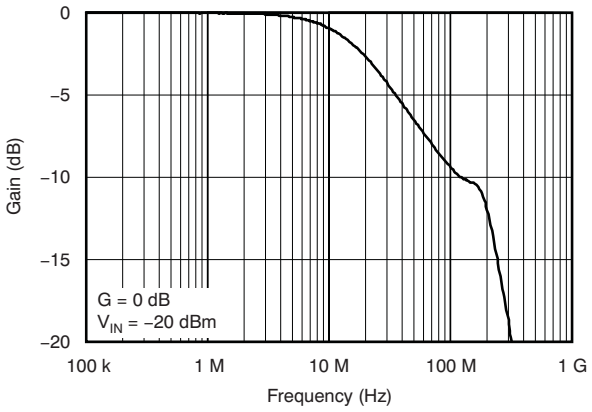


Figure 24.

V_{OCM} LARGE-SIGNAL PULSE RESPONSE

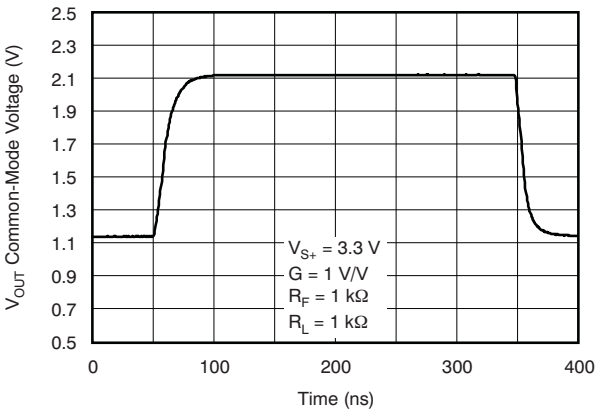


Figure 25.

V_{OCM} INPUT IMPEDANCE
vs FREQUENCY

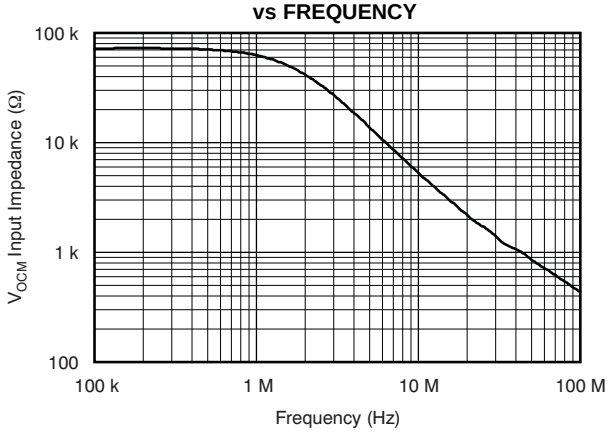


Figure 26.

TEST CIRCUITS

Overview

The THS4521 is tested with the test circuits shown in this section; all circuits are built using the available THS4521 evaluation module (EVM). For simplicity, power-supply decoupling is not shown; see the layout in the *Applications* section for recommendations. Depending on the test conditions, component values change in accordance with Table 2 and Table 3, or as otherwise noted. In some cases the signal generators used are ac-coupled and in others they dc-coupled 50-Ω sources. To balance the amplifier when ac-coupled, a 0.22-µF capacitor and 49.9-Ω resistor to ground are inserted across R_{IT} on the alternate input; when dc-coupled, only the 49.9-Ω resistor to ground is added across R_{IT}. A split power supply is used to ease the interface to common test equipment, but the amplifier can be operated in a single-supply configuration as described in the *Applications* section with no impact on performance. Also, for most of the tests, except as noted, the devices are tested with single-ended inputs and a transformer on the output to convert the differential output to single-ended because common lab test equipment has single-ended inputs and outputs. Similar or better performance can be expected with differential inputs and outputs.

As a result of the voltage divider on the output formed by the load component values, the amplifier output is attenuated. The ***Atten*** column in Table 3 shows the attenuation expected from the resistor divider. When using a transformer at the output (as shown in Figure 28), the signal sees slightly more loss because of transformer and line loss; these numbers are approximate.

Table 2. Gain Component Values for Single-Ended Input(1)

Gain	R_F	R_G	R_{IT}
1 V/V	1 kΩ	1 kΩ	52.3 Ω
2 V/V	1 kΩ	487 Ω	53.6 Ω
5 V/V	1 kΩ	187 Ω	59.0 Ω
10 V/V	1 kΩ	86.6 Ω	69.8 Ω

1. Gain setting includes 50-Ω source impedance. Components are chosen to achieve gain and 50-Ω input termination.

Table 3. Load Component Values For 1:1 Differential to Single-Ended Output Transformer(1)

R_L	R_O	R_{OT}	Atten
100 Ω	24.9 Ω	Open	6 dB
200 Ω	86.6 Ω	69.8 Ω	16.8 dB
499 Ω	237 Ω	56.2 Ω	25.5 dB
1 kΩ	487 Ω	52.3 Ω	31.8 dB

1. Total load includes 50-Ω termination by the test equipment. Components are chosen to achieve load and 50-Ω line termination through a 1:1 transformer.

Frequency Response

The circuit shown in Figure 27 is used to measure the frequency response of the circuit.

An HP network analyzer is used as the signal source and the measurement device. The output impedance of the HP network analyzer is is dc-coupled and is 50 Ω. R_{IT} and R_G are chosen to impedance-match to 50 Ω and maintain the proper gain. To balance the amplifier, a 49.9-Ω resistor to ground is inserted across R_{IT} on the alternate input.

The output is probed using a Tektronix high-impedance differential probe across the 953-Ω resistor and referred to the amplifier output by adding back the 0.42-dB because of the voltage divider on the output.

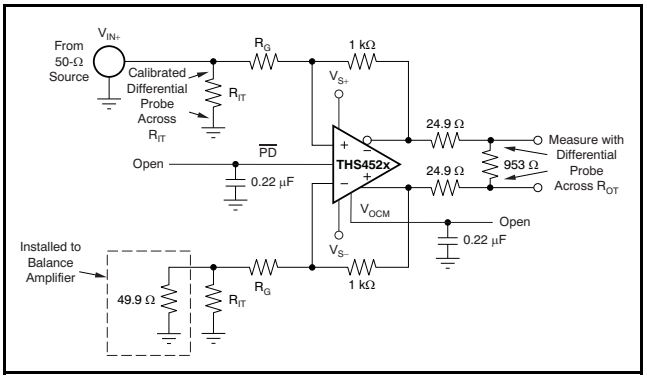


Figure 27. Frequency Response Test Circuit

Distortion

The circuit shown in Figure 28 is used to measure harmonic and intermodulation distortion of the amplifier.

An HP signal generator is used as the signal source and the output is measured with a Rhode and Schwarz spectrum analyzer. The output impedance of the HP signal generator is ac-coupled and is 50 Ω. R_{IT} and R_G are chosen to impedance match to 50 Ω and maintain the proper gain. To balance the amplifier, a 0.22-µF capacitor and 49.9-Ω resistor to ground are inserted across R_{IT} on the alternate input.

A low-pass filter is inserted in series with the input to reduce harmonics generated at the signal source. The level of the fundamental is measured and then a high-pass filter is inserted at the output to reduce the fundamental so it does not generate distortion in the input of the spectrum analyzer.

The transformer used in the output to convert the signal from differential to single-ended is an ADT1–1WT. It limits the frequency response of the circuit so that measurements cannot be made below approximately 1 MHz.

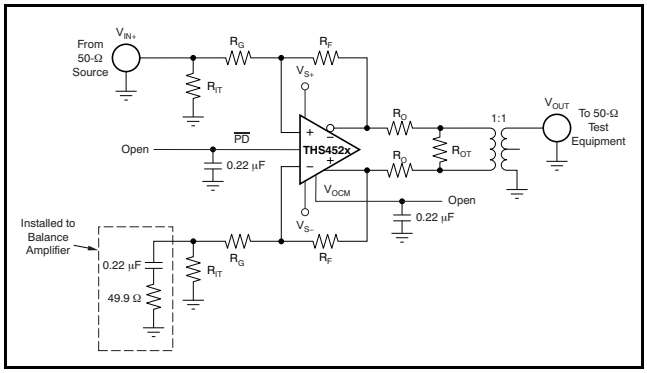


Figure 28. Distortion Test Circuit

Slew Rate, Transient Response, Settling Time, Output Impedance, Overdrive, Output Voltage, and Turn-On/Turn-Off Time

The circuit shown in Figure 29 is used to measure slew rate, transient response, settling time, output impedance, overdrive recovery, output voltage swing, and ampliifer turn-on/turn-off time. Turn-on and turn-off time are measured with the same circuit modified for 50-Ω input impedance on the $\overline{PD}$ input by replacing the 0.22-µF capacitor with a 49.9-Ω resistor. For output impedance, the signal is injected at V_{OUT} with V_{IN} open; the drop across the 2x 49.9-Ω resistors is then used to calculate the impedance seen looking into the amplifier output.

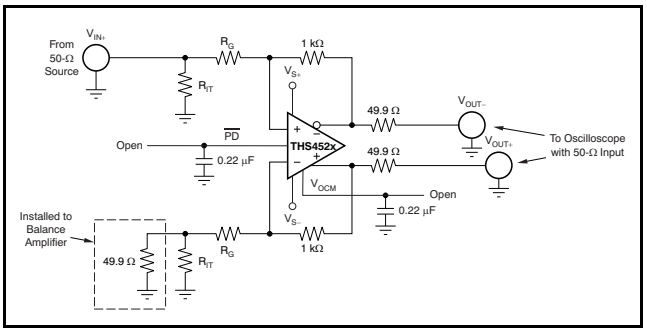


Figure 29. Slew Rate, Transient Response, Settling Time, Output Impedance, Overdrive Recovery, V_{OUT} Swing, and Turn-On/Turn-Off Test Circuit

Common-Mode and Power-Supply Rejection

The circuit shown in Figure 30 is used to measure the CMRR. The signal from the network analyzer is applied common-mode to the input. Figure 31 is used to measure the PSRR of V_{S+} and $V_{S–}$. The power supply under test is applied to the network analyzer dc offset input. For both CMRR and PSRR, the output is probed using a Tektronix high-impedance differential probe across the 953-Ω resistor and referred to the amplifier output by adding back the 0.42-dB as a result of the voltage divider on the output. For these tests, the resistors are matched for best results.

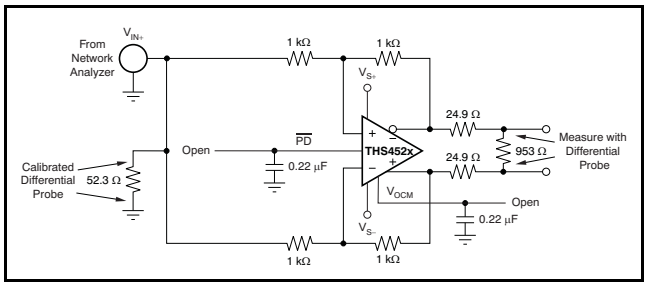


Figure 30. CMRR Test Circuit

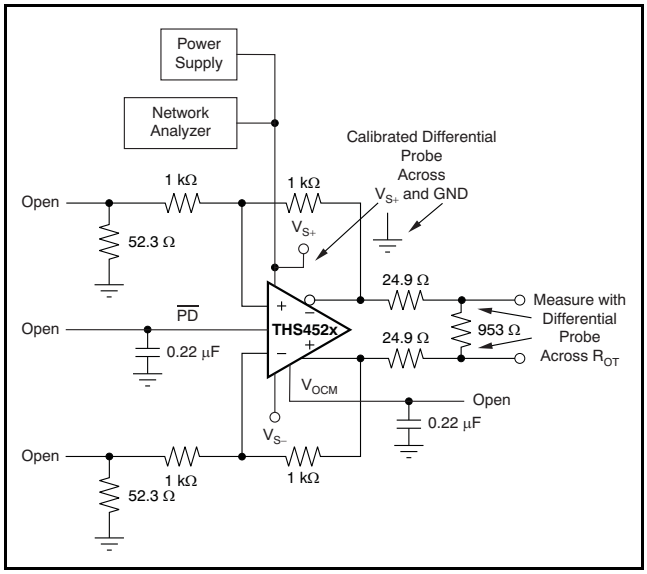


Figure 31. PSRR Test Circuit

V_{OCM} Input

The circuit illustrated in Figure 32 is used to measure the frequency response and input impedance of the V_{OCM} input. Frequency response is measured using a Tektronix high-impedance differential probe, with R_{CM} = 0 Ω at the common point of V_{OUT+} and $V_{OUT–}$, formed at the summing junction of the two matched 499-Ω resistors, with respect to ground. The input impedance is measured using a Tektronix high-impedance differential probe at the V_{OCM} input with R_{CM} = 10 kΩ and the drop across the 10-kΩ resistor is used to calculate the impedance seen looking into the amplifier V_{OCM} input.

The circuit shown in Figure 33 measures the transient response and slew rate of the V_{OCM} input. A 1-V step input is applied to the V_{OCM} input and the output is measured using a 50-Ω oscilloscope input referenced back to the amplifier output.

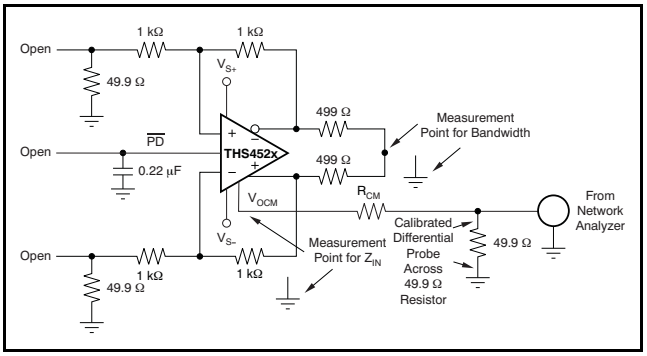


Figure 32. V_{OCM} Input Test Circuit

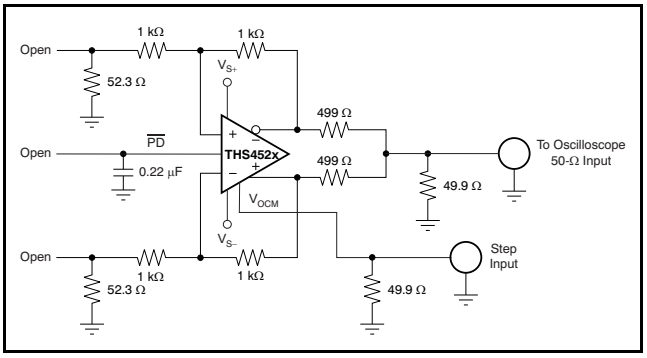


Figure 33. V_{OCM} Transient Response and Slew Rate Test Circuit

APPLICATION INFORMATION

The following circuits show application information for the THS4521. For simplicity, power-supply decoupling capacitors are not shown in these diagrams; see the *EVM and Layout Recommendations* section for suggested guidelines. For more details on the use and operation of fully differential op amps, refer to the Application Report *Fully-Differential Amplifiers* (SLOA054), available for download from the TI web site at www.ti.com.

Differential Input to Differential Output Amplifier

The THS4521 is fully-differential operational amplifiers that can be used to amplify differential input signals to differential output signals. Figure 34 shows a basic block diagram of the circuit (V_{OCM} and $\overline{PD}$ inputs not shown). The gain of the circuit is set by R_F divided by R_G.

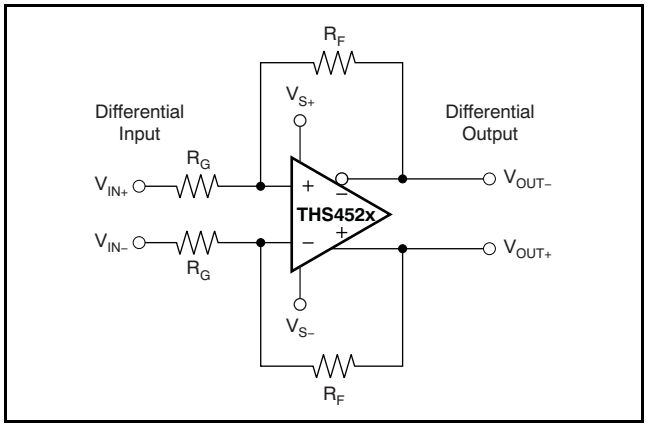


Figure 34. Differential Input to Differential Output Amplifier

Single-Ended Input to Differential Output Amplifier

The THS4521 can also amplify and convert single-ended input signals to differential output signals. Figure 35 illustrates a basic block diagram of the circuit (V_{OCM} and $\overline{PD}$ inputs not shown). The gain of the circuit is again set by R_F divided by R_G.

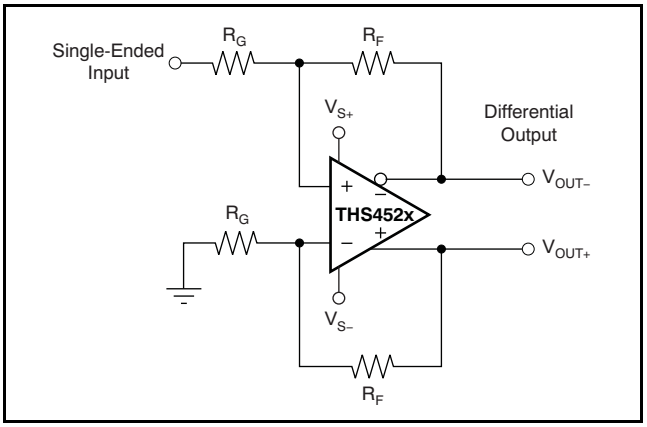


Figure 35. Single-Ended Input to Differential Output Amplifier

Input Common-Mode Voltage Range

The input common-mode voltage of a fully-differential op amp is the voltage at the **+** and **–** input pins of the device.

It is important to not violate the input common-mode voltage range (V_{ICR}) of the op amp. Assuming the op amp is in linear operation, the voltage across the input pins is only a few millivolts at most. Therefore, finding the voltage at one input pin determines the input common-mode voltage of the op amp.

Treating the negative input as a summing node, the voltage is given by Equation 1:

$$\left(V_{OUT+} \times \frac{R_G}{R_G + R_F}\right) + \left(V_{IN-} \times \frac{R_F}{R_G + R_F}\right) \quad (1)$$

To determine the V_{ICR} of the op amp, the voltage at the negative input is evaluated at the extremes of V_{OUT+}. As the gain of the op amp increases, the input common-mode voltage becomes closer and closer to the input common-mode voltage of the source.

Setting the Output Common-Mode Voltage

The output common-model voltage is set by the voltage at the V_{OCM} pin. The internal common-mode control circuit maintains the output common-mode voltage within 5-mV offset (typ) from the set voltage. If left unconnected, the common-mode set point is set to midsupply by internal circuitry, which may be overdriven from an external source.

Figure 36 represents the V_{OCM} input. The internal V_{OCM} circuit has typically 23 MHz of –3 dB bandwidth, which is required for best performance, but it is intended to be a dc bias input pin. A 0.22-µF bypass capacitor is recommended on this pin to reduce noise. The external current required to overdrive the internal resistor divider is given approximately by the formula in Equation 2:

$$I_{EXT} = \frac{2V_{OCM} - (V_{S+} - V_{S-})}{50\ k\Omega} \quad (2)$$

where:

- V_{OCM} is the voltage applied to the V_{OCM} pin

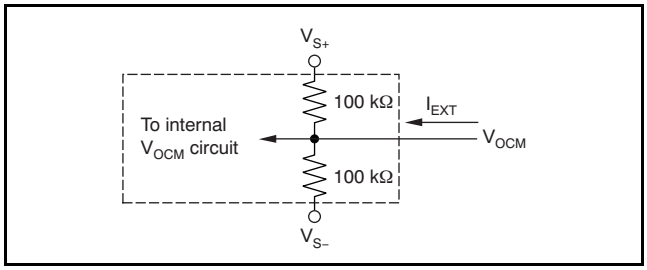


Figure 36. V_{OCM} Input Circuit

Typical Performance Variation with Supply Voltage

The THS4521 provides excellent performance across the specified power-supply range of 2.5 V to 3.3 V with only minor variations. The input and output voltage compliance ranges track with the power supply in nearly a 1:1 correlation. Other changes can be observed in slew rate, output current drive, open-loop gain, bandwidth, and distortion.

Single-Supply Operation

To facilitate testing with common lab equipment, the THS4521EVM allows for split-supply operation; most of the characterization data presented in this data sheet is measured using split-supply power inputs. The device can easily be used with a single-supply power input without degrading performance.

Figure 37 shows a dc-coupled single-supply circuit with single-ended inputs. This circuit can also be applied to differential input sources.

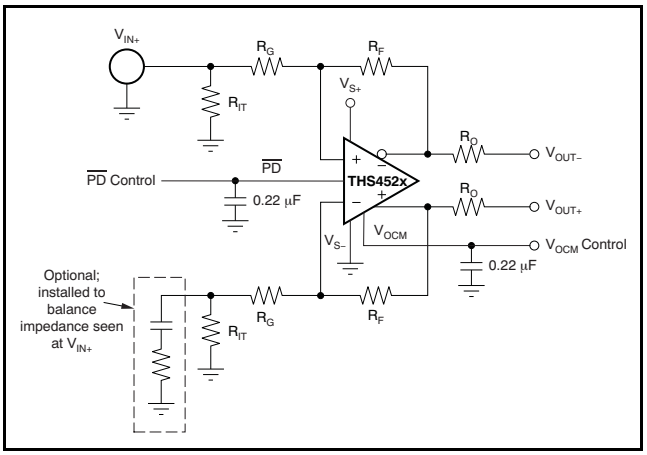


Figure 37. THS4521 DC-Coupled Single-Supply with Single-Ended Inputs

The input common-mode voltage range of the THS4521 is designed to include the negative supply voltage. In the circuit shown in Figure 37, the signal source is referenced to ground. V_{OCM} is set by an external control source or, if left unconnected, the internal circuit defaults to midsupply. Together with the input impedance of the amplifier circuit, R_{IT} provides input termination, which is also referenced to ground.

Note that R_{IT} and optional matching components are added to the alternate input to balance the impedance at signal input.

Low-Power Applications and the Effects of Resistor Values on Bandwidth

For low-power operation, it may be necessary to increase the gain setting resistors values to limit current consumption and not load the source. Using larger value resistors lowers the bandwidth of the THS4521 as a result of the interactions between the resistors, the device parasitic capacitance, and printed circuit board (PCB) parasitic capacitance.

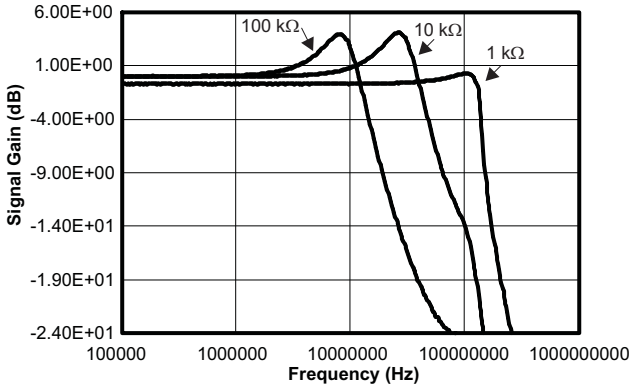


Figure 38. THS4521 Frequency Response with Various Gain Setting and Load Resistor Values

Driving Capacitive Loads

The THS4521 is designed for a nominal capacitive load of 1 pF on each output to ground. When driving capacitive loads greater than 1 pF, it is recommended to use small resistors (R_O) in series with the output, placed as close to the device as possible. Without R_O, capacitance on the output interacts with the output impedance of the amplifier and causes phase shift in the loop gain of the amplifier that reduces the phase margin. This reduction in phase margin results in frequency response peaking; overshoot, undershoot, and/or ringing when a step or square-wave signal is applied; and may lead to instability or oscillation. Inserting R_O isolates the phase shift from the loop gain path and restores the phase margin, but it also limits bandwidth.

LAYOUT RECOMMENDATIONS

It is recommended to follow the layout of the external components near to the amplifier, ground plane construction, and power routing as closely as possible. Follow these general guidelines:

1. Signal routing should be direct and as short as possible into and out of the op amp circuit.
2. The feedback path should be short and direct.
3. Ground or power planes should be removed from directly under the amplifier input and output pins.
4. An output resistor is recommended in each output lead, placed as near to the output pins as possible.
5. Two 0.1-µF power-supply decoupling capacitors should be placed as near to the power-supply pins as possible.
6. Two 10-µF power-supply decoupling capacitors should be placed within 1 inch of the device and can be shared among multple analog devices.
7. A 0.22-µF capacitor should be placed between the V_{OCM} input pin and ground near to the pin. This capacitor limits noise coupled into the pin.
8. The $\overline{PD}$ pin uses TTL logic levels; a bypass capacitor is not necessary if actively driven, but can be used for robustness in noisy environments whether driven or not.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
THS4521HD	ACTIVE	SOIC	D	8	75	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-55 to 175	T4521H	Samples
THS4521SHKJ	ACTIVE	CFP	HKJ	8	25	RoHS & Green	Call TI	N / A for Pkg Type	-55 to 210	THS4521 HKJ	Samples
THS4521SHKQ	ACTIVE	CFP	HKQ	8	25	RoHS & Green	AU	N / A for Pkg Type	-55 to 210	THS4521S HKQ	Samples
THS4521SKGD1	ACTIVE	XCEPT	KGD	0	324	RoHS & Green	Call TI	N / A for Pkg Type	-55 to 210		Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals.
TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

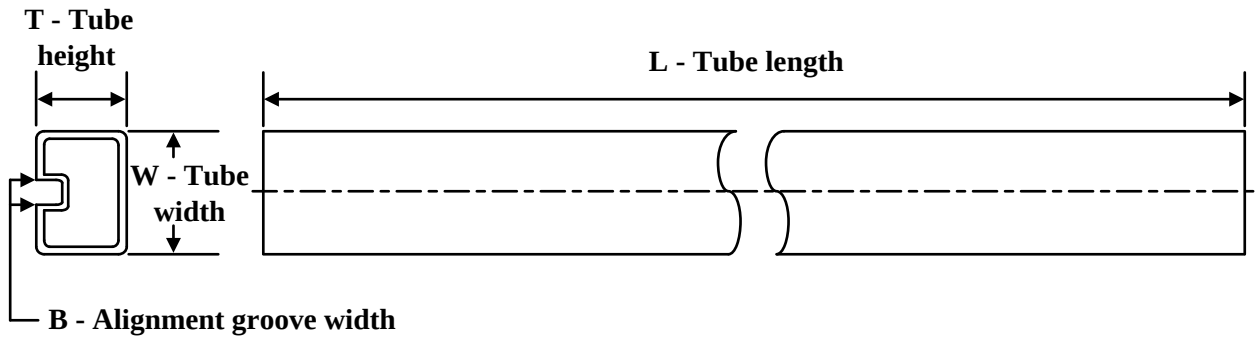
OTHER QUALIFIED VERSIONS OF THS4521-HT :

- Catalog : THS4521

NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product

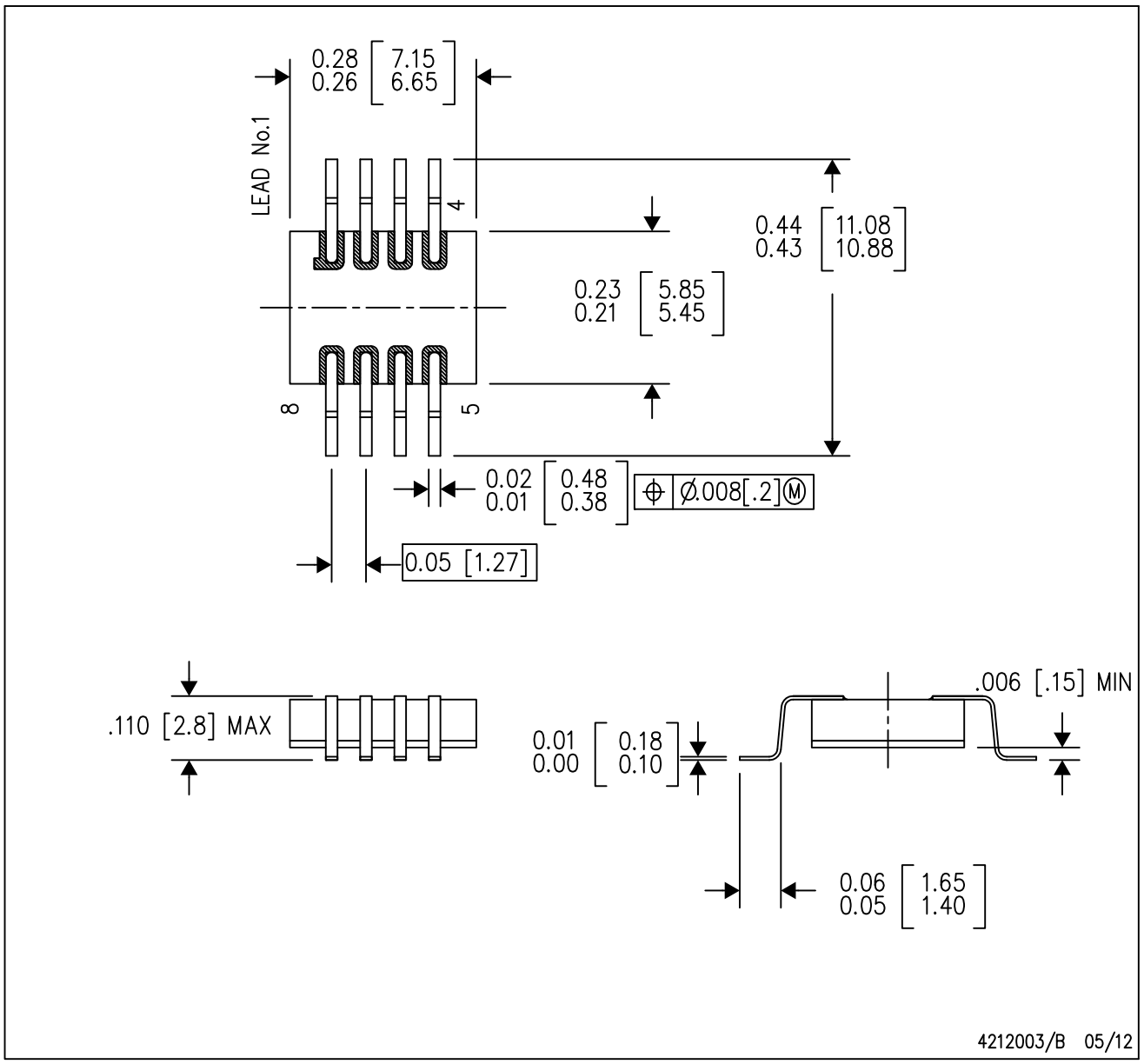
TUBE



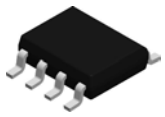
*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
THS4521HD	D	SOIC	8	75	506.6	8	3940	4.32
THS4521SHKJ	HKJ	CFP	8	25	506.98	26.16	6220	NA
THS4521SHKQ	HKQ	CFP	8	25	506.98	26.16	6220	NA

HKQ (R–CDFP–G8) CERAMIC GULL WING



NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. This package can be hermetically sealed with a metal lid.
D. The terminals will be gold plated.
E. Lid is not connected to any lead.

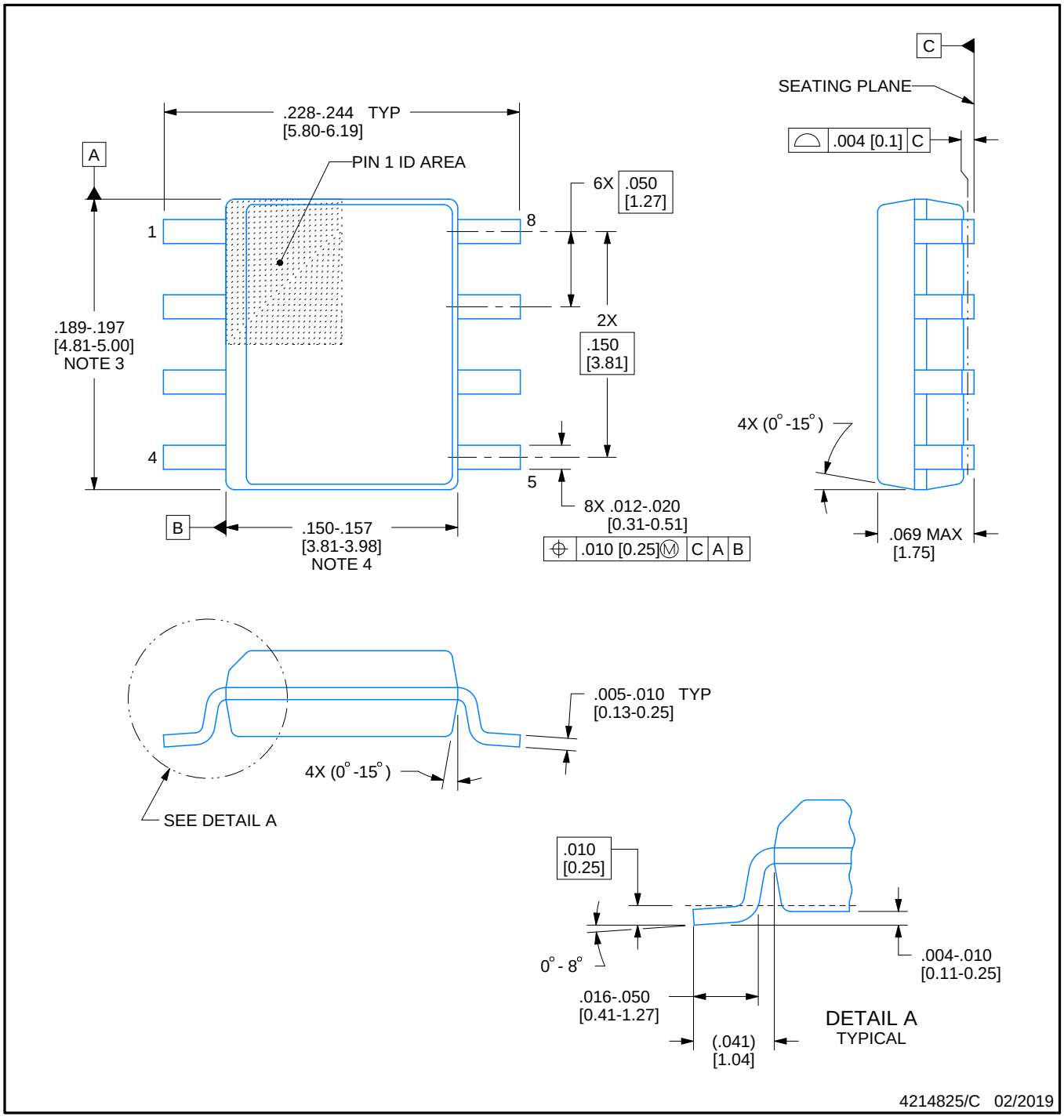


PACKAGE OUTLINE

D0008A

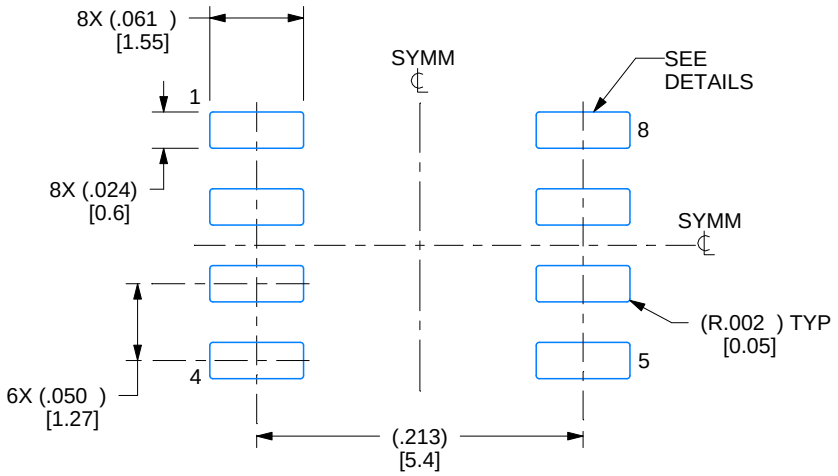
SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT

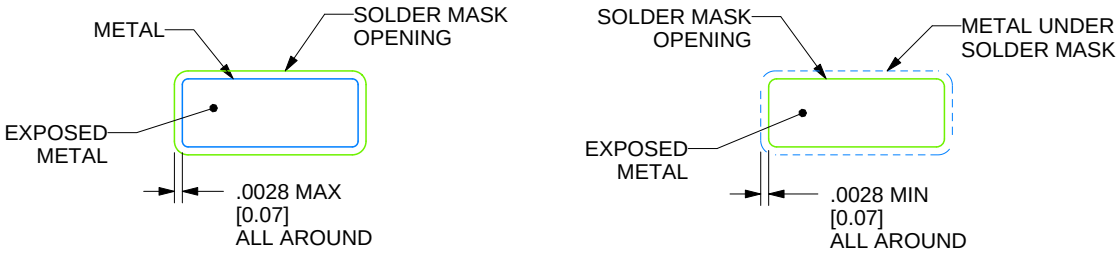


NOTES:

1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15] per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:8X



SOLDER MASK DETAILS

4214825/C 02/2019

NOTES: (continued)

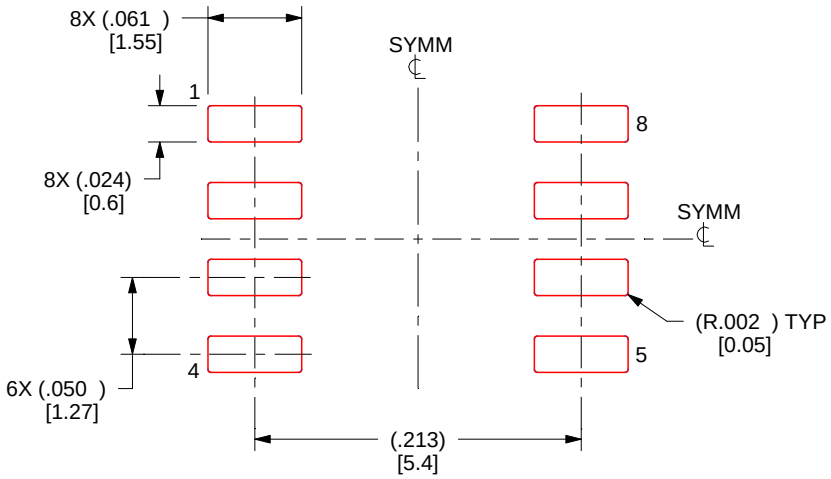
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



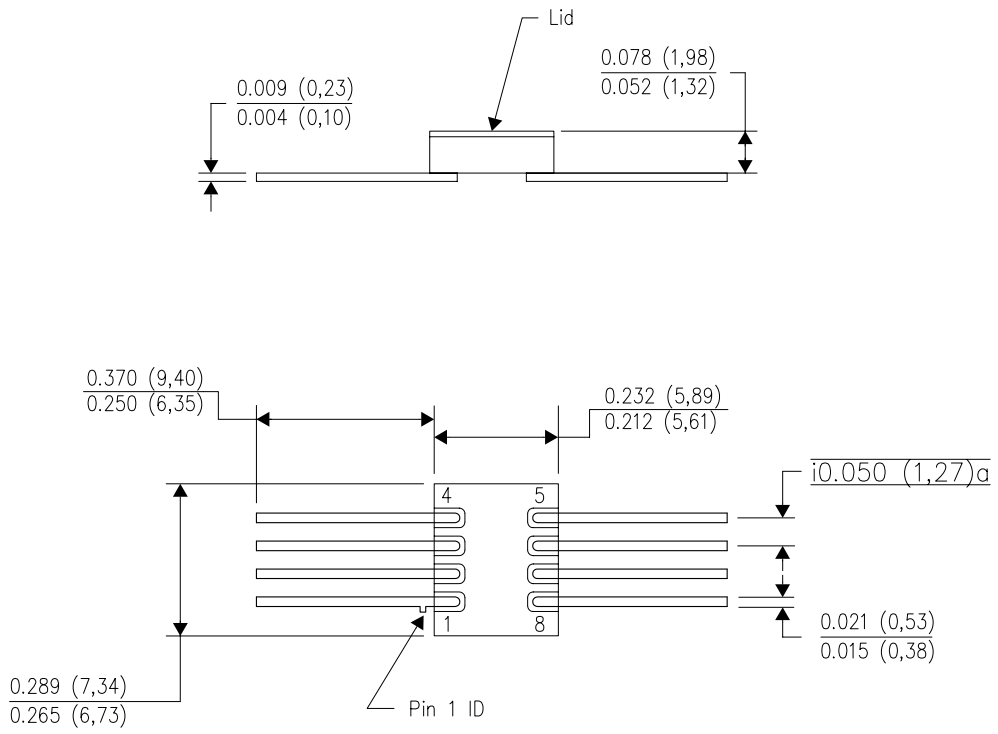
SOLDER PASTE EXAMPLE
BASED ON .005 INCH [0.125 MM] THICK STENCIL
SCALE:8X

4214825/C 02/2019

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

HKJ (R–CDFP–F8) CERAMIC DUAL FLATPACK



4209892/A 10/08

NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. This package can be hermetically sealed with a metal lid.
D. The terminals will be gold plated.

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