



**THE DATASHEET OF
TDA8037TT/C1J**



TDA8037

Low power 3V smart card interface

Rev. 1.2 — 30 June 2016

Product data sheet

1. General description

The TDA8037 is the cost efficient successor of the established integrated contact smart card reader IC TDA8035. It offers a high level of security for the card performing current limitation, short circuit detection, ESD protection as well as supply supervision. Operating in 3 V supply domain, the current consumption during the shutdown mode of the contact reader is very low. It is therefore the ideal component for a power efficient contact reader.

2. Features and benefits

2.1 Protection of the contact smart card

- Thermal and short-circuit protection on all card contacts
- V_{CC} regulation:
 - ◆ $3\text{ V} \pm 5\%$ on $2 \times 220\text{ nF}$ multilayer ceramic capacitors with low ESR
 - ◆ Current spikes of 40 nA up to 20 MHz, with controlled rise and fall times, filtered overload detection approximately 120 mA
- Automatic activation and deactivation sequences initiated by software or by hardware in the event of a short-circuit, card take-off, overheating, $V_{DD\text{host}}$, VREG and V_{DD} dropping
- Enhanced card-side ElectroStatic Discharge (ESD) protection of (> 8 kV)
- Supply supervisor for killing spikes during power on and off:
 - ◆ threshold internally fixed
 - ◆ externally by a resistor bridge (with SO28 package only)

2.2 Easy integration into your contact reader

- SW compatible to TDA8024, TDA8034 and TDA8035
- 3 V smart card supply
- Three protected half-duplex bidirectional buffered I/O lines (C4, C7 and C8)
- External clock input up to 20 MHz
- Card clock generation up to 20 MHz using pin CLKDIV with synchronous frequency changes of f_{CLKIN} , $f_{CLKIN}/2$ (with SO28 package only)
- Non-inverted control of pin RST using pin RSTIN
- Built-in debouncing on card presence contact
- Multiplexed status signal using pin OFFN
- Chip Select digital input for parallel operation of several TDA8037 ICs (with SO28 package only)



2.2.1 Other

- TSSOP16 and SO28 package
- SO28 version is footprint compatible with TDA8024T
- Compliant with ISO 7816, Cisco technology and EMV 4.3 payment systems

3. Applications

- Pay TV
- Electronic payment
- Identification
- IC card readers for banking

4. Quick reference data

Table 1. Quick reference data

$V_{DDP} = 3.3\text{ V}$; $V_{DD(INTF)} = 3.3\text{ V}$; $f_{Xtal} = 10\text{ MHz}$; $GND = 0\text{ V}$; $T_{amb} = 25\text{ °C}$; unless otherwise specified

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---|-----------------------------|--|------|-----|------|--------------------|
| Supply | | | | | | |
| V_{DD} | supply voltage | | 3 | 3.3 | 3.6 | V |
| I_{DD} | supply current | Shutdown mode; $f_{CLKIN} = \text{stopped}$ | - | 250 | 400 | μA |
| | | active mode; CLK = CLKIN; no-load | - | - | 5 | mA |
| | | active mode; CLK = CLKIN; $I_{CC} = 65\text{ mA}$ | - | - | 70 | mA |
| Supply voltage for the card: pin V_{CC} | | | | | | |
| V_{CC} | supply voltage | DC $I_{CC} < 65\text{ mA}$ | 2.85 | - | 3.15 | V |
| | | AC current spikes of 40 nA | 2.76 | - | 3.24 | V |
| $V_{ripple(p-p)}$ | peak-to-peak ripple voltage | from 20 kHz to 200 MHz | - | - | 150 | mV |
| I_{CC} | supply current | | - | - | 65 | mA |
| General | | | | | | |
| t_{deact} | deactivation time | total sequence | 35 | 90 | 250 | μs |
| P_{tot} | total power dissipation | $T_{amb} = -25\text{ °C}$ to $+85\text{ °C}$ | - | - | 0.1 | W |
| T_{amb} | ambient temperature | | -25 | - | +85 | $^{\circ}\text{C}$ |

5. Ordering information

Table 2. Ordering information

| Type number | Package | | |
|-------------|---------|--|----------|
| | Name | Description | Version |
| TDA8037TT | TSSOP16 | plastic thin shrink small outline package; 16 leads; body width 4.4 mm | SOT403-1 |
| TDA8037T | SO28 | plastic small outline package; 28 leads; body width 7.5 mm | SOT136-1 |

6. Block diagram

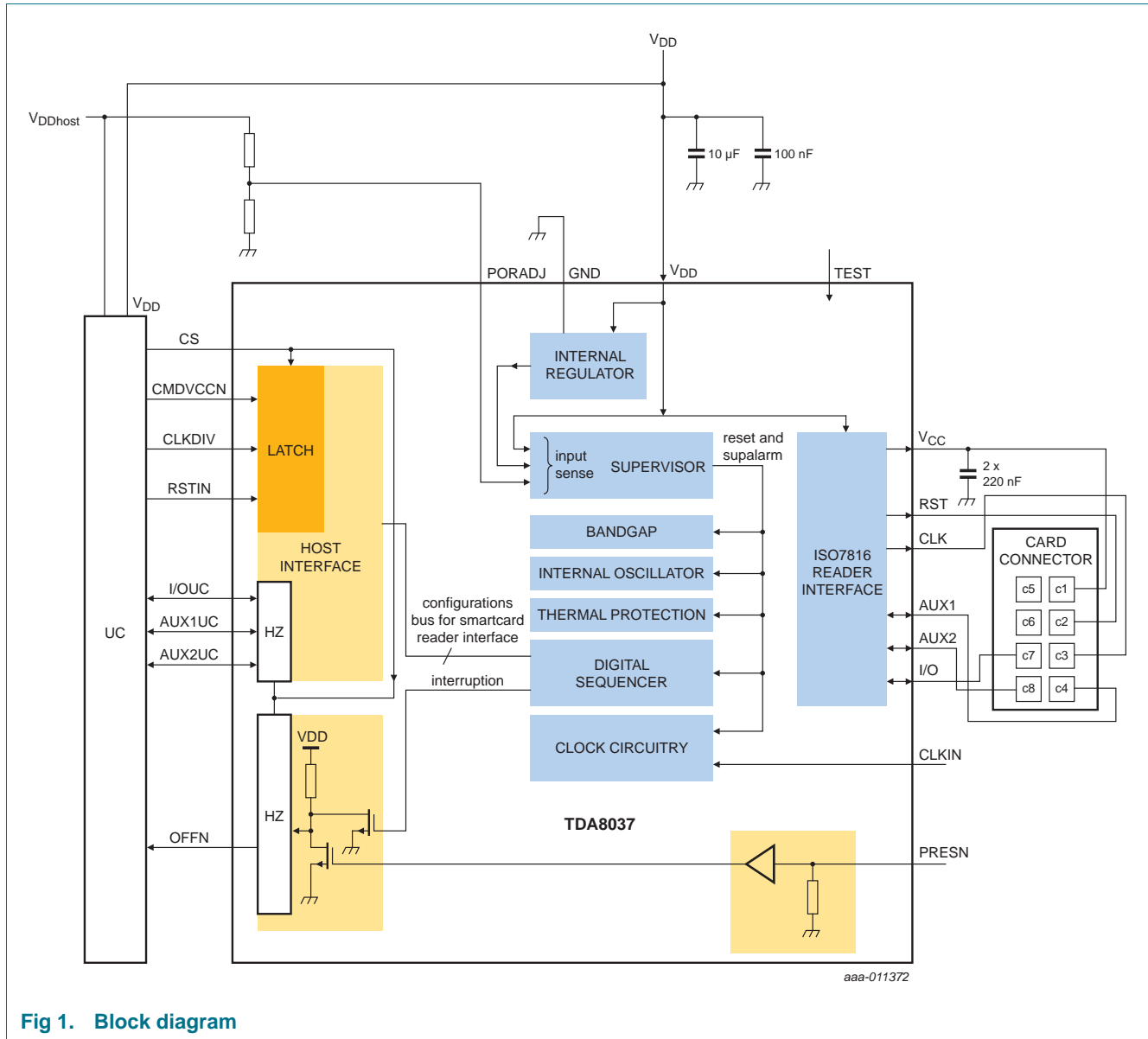
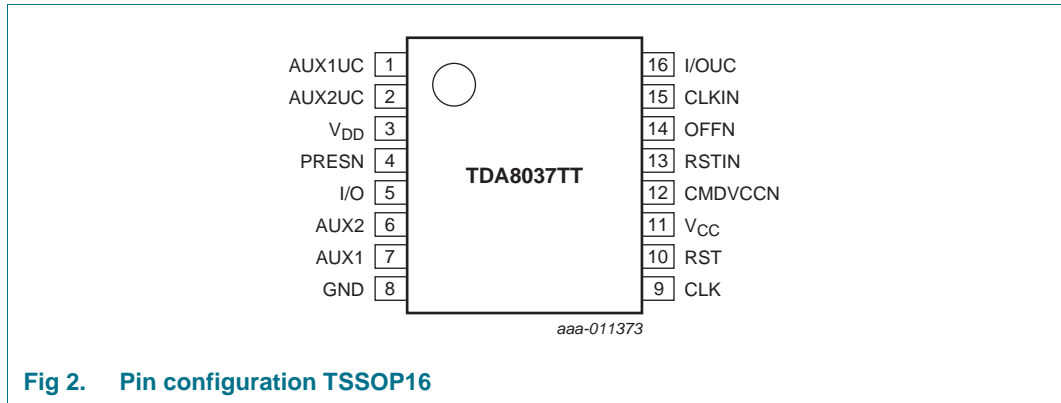


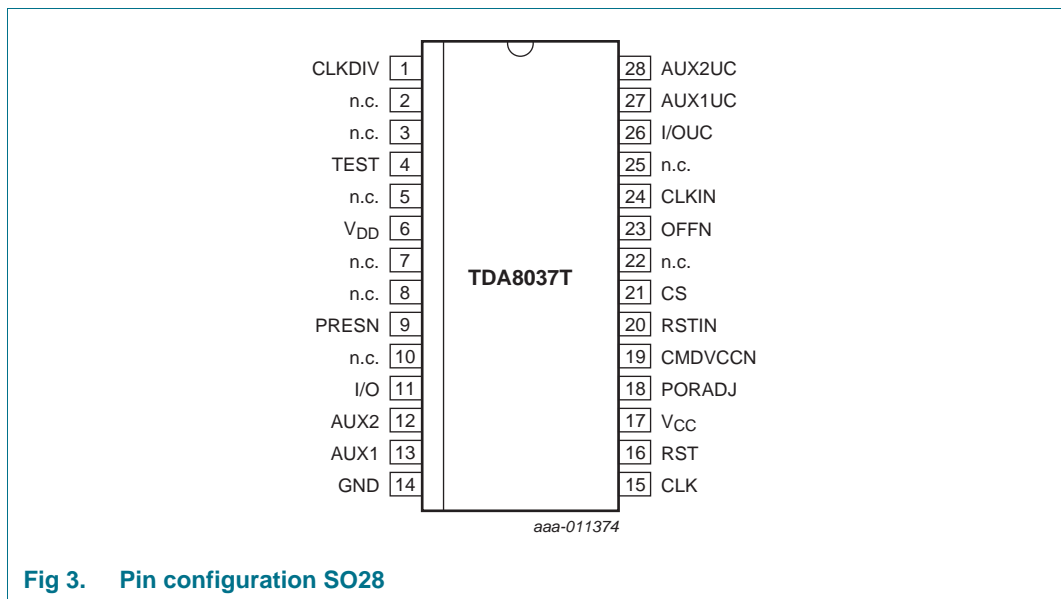
Fig 1. Block diagram

7. Pinning information

7.1 Pinning



7.2 Pinning



7.3 Pin description

Table 3. Pin description

| Symbol | Pin SO28 | Pin TSSOP16 | Supply | Type | Description |
|-----------------|----------|-------------|-----------------|--------|---|
| AUX1UC | 27 | 1 | V _{DD} | I/O | auxiliary data line to/from the host (internal 10 k pull-up resistor to V _{DD}) |
| AUX2UC | 28 | 2 | V _{DD} | I/O | auxiliary data line to/from the host (internal 10 k pull-up resistor to V _{DD}) |
| V _{DD} | 6 | 3 | V _{DD} | supply | supply voltage |
| PRESN | 9 | 4 | V _{DD} | I | card presence contact input (active LOW); if PRESN is true, then the card is considered as present. A debouncing feature of 4.05 ms typ. is built in. |
| I/O | 11 | 5 | V _{CC} | I/O | data line to/from the card (C7)(internal 10 k pull up resistor to V _{CC}) |
| AUX2 | 12 | 6 | V _{CC} | I/O | auxiliary data line to/from the card (C8) (internal 10 k pull up resistor to V _{CC}) |
| AUX1 | 13 | 7 | V _{CC} | I/O | auxiliary data line to/from the card (C4) (internal 10 k pull up resistor to V _{CC}) |
| GND | 14 | 8 | - | supply | ground |
| CLK | 15 | 9 | V _{CC} | O | clock to the card (C3) |
| RST | 16 | 10 | V _{CC} | O | card reset (C2) |
| V _{CC} | 17 | 11 | V _{CC} | O | supply for the card (C1) (decouple to GND with 2x 220 nF capacitors with ESR<100 mΩ). |
| CMDVCCN | 19 | 12 | V _{DD} | I | start activation sequence input from the host (active LOW) |
| RSTIN | 20 | 13 | V _{DD} | I | card reset input from the host (active HIGH) |
| OFFN | 23 | 14 | V _{DD} | O | NMOS interrupt to the host (active LOW) with 10 k internal pull-up resistor to V _{DD} (see fault detection) |
| CLKIN | 24 | 15 | V _{DD} | I | external clock |
| I/OUC | 26 | 16 | V _{DD} | I/O | host data I/O line (internal 10k pull-up resistor to V _{DD}) |
| CLKDIV | 1 | nc | V _{DD} | I | control for choosing CLK frequency |
| TEST | 4 | nc | V _{DD} | I | test mode |
| PORADJ | 18 | nc | V _{DD} | I | input for V _{DDhost} supervisor. PORADJ threshold can be changed with an external R bridge. |
| CS | 21 | nc | V _{DD} | I | chip select input from the host (active High) |

8. Functional description

Remark: The ISO 7816 terminology convention has been adhered to throughout this document, and it is assumed that the reader is familiar with this convention.

8.1 Power supply

Power supply voltage V_{DD} is from 3 V to 3.6 V.

All interface signals with the system controller are referenced to V_{DD} . All card contacts remain inactive during powering up or powering down.

Internal regulator V_{REG} is 1.8 V.

After powering the device, OFFN remains low until CMDVCCN is set high and PRESN is low.

During power off, OFFN falls low when V_{DD} is below the threshold voltage falling.

The frequency of the internal oscillator ($f_{osc(int)}$) used for the activation sequences is put in low frequency mode. It is to save power consumption while CMDVCCN is kept at high level (card not activated).

8.2 Voltage supervisor

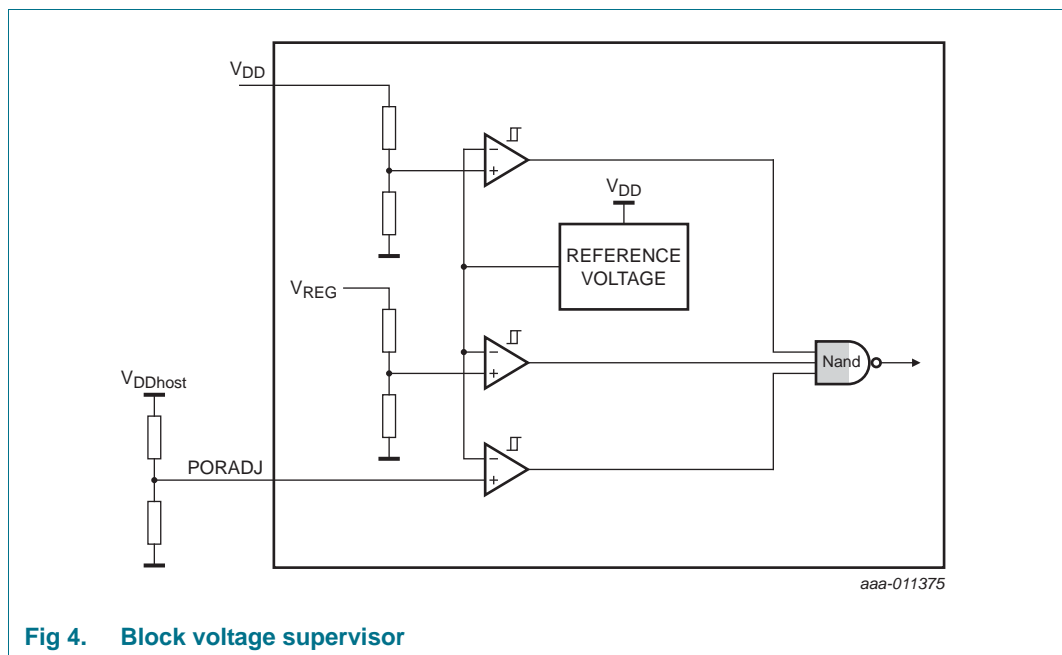


Fig 4. Block voltage supervisor

The voltage supervisor is used as a power-on reset, and also as supply drop detection during a card session. The threshold of the voltage supervisor is set internally in the IC for V_{DD} and V_{REG} . The threshold can be adjusted externally for V_{DDhost} using the PORADJ pin. As long as V_{DD} is less than $V_{th}(V_{DD}) + V_{hys}(V_{DD})$, the IC remains inactive whatever the levels on the command lines are. It lasts during t_w after V_{DD} has reached a level higher than $V_{th}(V_{DD}) + V_{hys}(V_{DD})$. The outputs of the V_{DD} , V_{REG} and V_{DDhost} supervisors, are combined and sent to a digital controller in order to reset the TDA8037. The defined reset

pulse of approximately 5.7 ms ($t_w = 2048 \times 1/(f_{osc(int_Low)})$), is used internally for maintaining the IC in an inactive mode during the supply voltage power-on (see [Figure 5](#), [Figure 6](#), [Figure 7](#), [Figure 8](#) and [Figure 9](#)). When V_{DD} falls below $V_{th}(V_{DD})$, $V_{th}(V_{REG})$ or V_{DDhost} falls below $V_{th}(V_{DDhost})$, a deactivation sequence is performed.

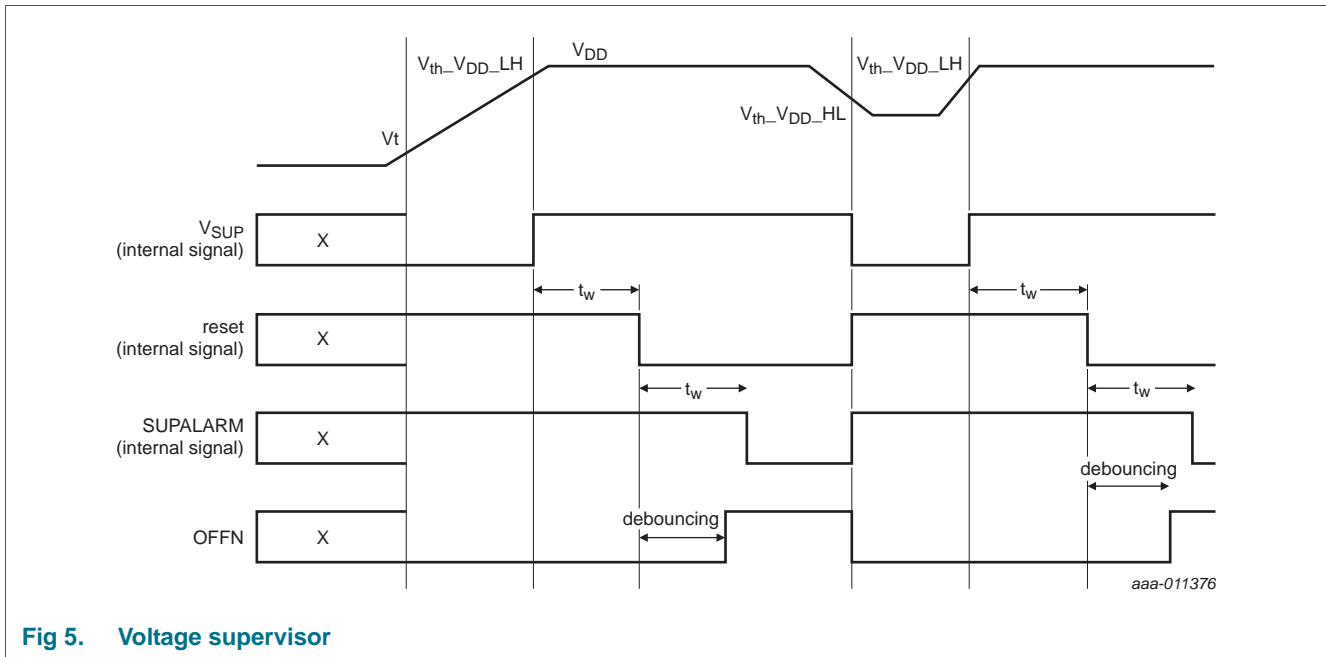


Fig 5. Voltage supervisor

8.3 Clock circuitry

To generate the card clock CLK, the TDA8037 uses an external clock provided on CLKIN pin. Apply the external clock to CLKIN before CMDVCCN falling edge signal.

The frequency is chosen as f_{CLKIN} , $f_{CLKIN}/2$ via the pins CLKDIV.

The frequency change is synchronous, which means that during transition, no pulse is shorter than 45 % of the smallest period. It ensures that the first and last clock pulse around the change has the correct width. When changing the frequency dynamically, the change is effective for only 10 periods of CLKIN after the command.

The duty cycle on pin CLK shall be between 45 % and 55 %.

Table 4. Clock configuration (SO28 only)

| CLKDIV | CLK |
|--------|---------------|
| 0 | f_{CLKIN} |
| 1 | $f_{CLKIN}/2$ |

8.4 I/O circuitry

The three data lines I/O, AUX1 and AUX2 are identical.

By pulling both lines (I/O and I/OUC) HIGH via a 10 kΩ resistor (I/O to V_{CC} and I/OUC to V_{DD}), the idle state is realized.

I/O is referenced to V_{CC} , and I/OUC to V_{DD} , thus allowing operation with $V_{CC} \neq V_{DD}$.

The first side on which a falling edge occurs becomes the master. An anti-latch circuit disables the detection of falling edges on the other line, which becomes a slave.

After a time delay $t_{d(\text{edge})}$, the logic 0 on the master side is transmitted to the slave side.

When the master side returns to logic 1, the slave side transmits the logic 1 during the time delay t_{pu} . After which, both sides return to their Idle states.

This active pull-up feature ensures fast Low to High transitions. It is able to deliver more than 1 mA up to an output voltage of $0.9 V_{CC}$ on an 80 pF load. At the end of the active pull-up pulse, the output voltage only depends on the internal pull-up resistor, and on the load current.

The current to/from the cards I/O lines, is internally limited to 15 mA.

The maximum frequency on these lines is 1.5 MHz.

8.5 CS control

The CS (Chip Select) input allows multiple devices to operate in parallel. When CS is high, the system interface signals operate as described. When CS is low, the signals CMDVCCN, RSTIN and CLKDIV are latched. I/OUC, AUX1UC and AUX2UC are set to high impedance pull-up mode and data is no longer passed to or from the smart card. The OFFN output is a 3-state output.

8.6 Shutdown mode

After power-on reset, the circuit enters the Shutdown mode if CMDVCCN input pin is set to a logic high. A minimum number of circuits are active while waiting for the microcontroller to start a session.

1. All card contacts are inactive (approximately 200 Ω to GND).
2. I/OUC, AUX1UC and AUX2UC are high impedance (10 k Ω pull-up resistor connected to V_{DD}).
3. Voltage generators are stopped.
4. Voltage supervisor is active.
5. The internal oscillator runs at its low frequency.

8.7 Activation sequence

The following sequence then occurs with external clock (see [Figure 6](#)):

$$T = 64 \times T_{oscint} \text{ (freq high)}$$

1. CMDVCCN is pulled Low (t_0)
2. The internal oscillator changes to its high frequency ($t_1 = t_0 + \sim$)
3. V_{CC} rises from 0 to selected V_{CC} value (3 V) with a controlled slope ($t_2 = t_1 + 3T/2$)
4. I/O, AUX1 and AUX2 are enabled ($t_3 = t_1 + 10T$); they were pulled LOW until this moment
5. CLK is applied to the C3 contact ($t_4 = t_3 + x$) with $200 \text{ ns} < x < 10 \times 1/f_{CLKIN}$
6. RST is enabled ($t_5 = t_1 + 13T$).

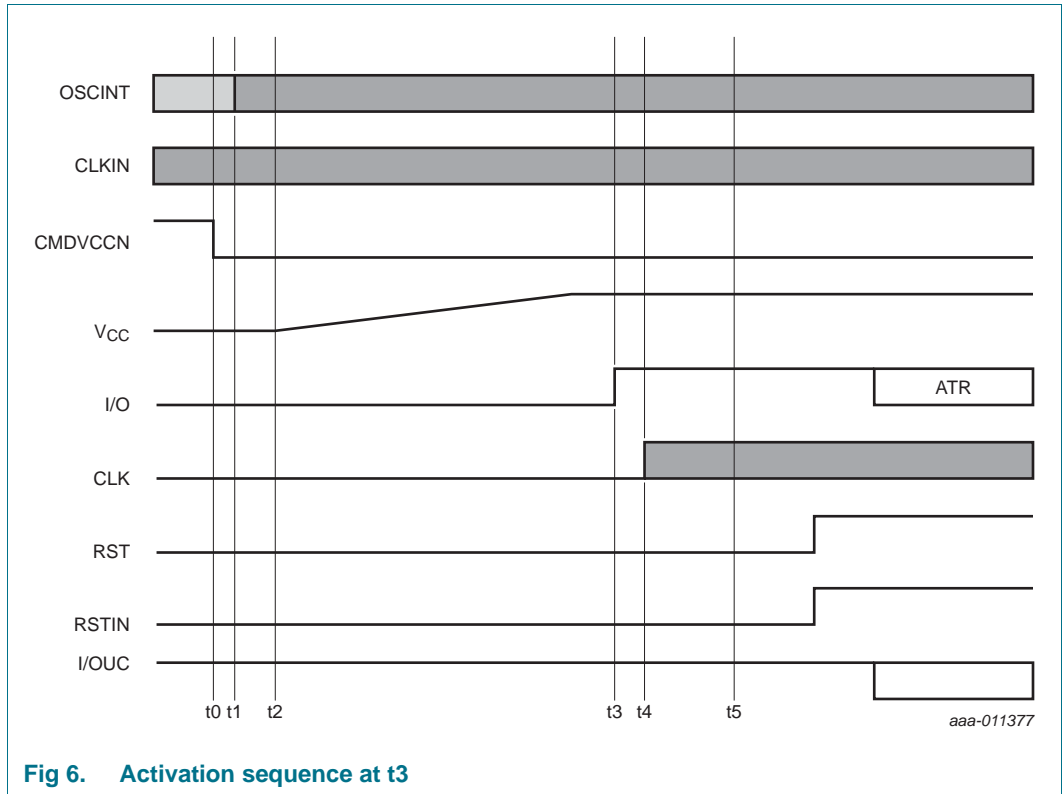


Fig 6. Activation sequence at t3

8.8 Deactivation sequence

When a session is completed, the microcontroller sets the CMDVCCN line to the HIGH state. The circuit then executes an automatic deactivation sequence by counting the sequencer back and ends in the inactive state (see [Figure 7](#)):

Note: CMDVCCN line should not be set to High state until activation sequence has not completed. Else, this deactivation command is not taken into account.

1. RST goes LOW ($t_{11} = t_{10} + 3T/64$)
2. CLK is stopped LOW ($t_{12} = t_{11} + T/2$)
3. I/O, AUX1 and AUX2 are pulled LOW ($t_{13} = t_{11} + T$)
4. V_{CC} falls to zero ($t_{14} = t_{11} + 3T/2$). The deactivation sequence is completed when V_{CC} reaches its inactive state
5. $V_{CC} < 0.4 V$ ($t_{de} = t_{11} + 3T/2 + V_{CC}$ fall time)
6. All card contacts become low-impedance to GND. I/OUC, AUX1UC and AUX2UC remain pulled up to V_{DD} via a 10 kΩ resistor.
7. The internal oscillator reverts to its lower frequency.

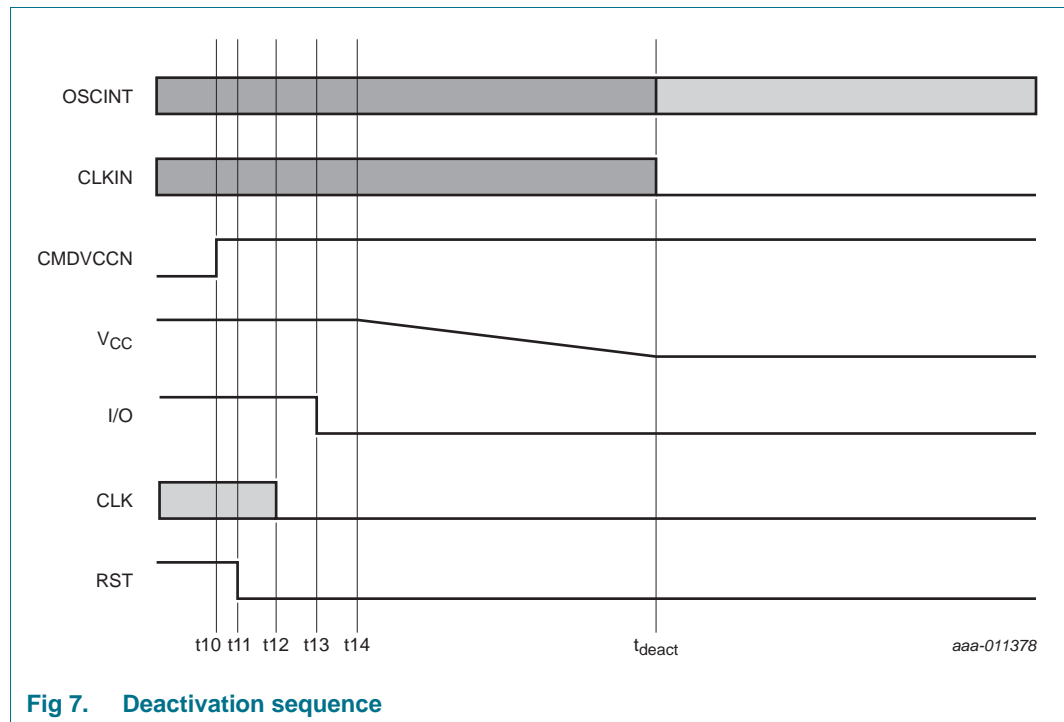


Fig 7. Deactivation sequence

8.9 V_{CC} regulator

V_{CC} buffer is able to deliver up to 65 mA continuously at $V_{CC} = 3 V$.

It has an internal overload detection at approximately 125 mA.

This detection is internally filtered, allowing the card to draw spurious current pulses up to 200 mA for some ms, without causing a deactivation. The average current value must stay below maximum.

8.10 Fault detection

The circuit monitors the following fault conditions:

- short-circuit or high current on V_{CC}
- Card removal during transaction
- V_{DD} , V_{REG} or V_{DDhost} dropping
- overheating.

There are two different cases (see [Figure 8 on page 12](#)):

1. CMDVCCN High: (outside a card session) then, if the card is not in the reader, OFFN is Low. It is High when the card is in the reader. The supply supervisor detects a supply voltage drop on V_{DD} . It generates an internal power-on reset pulse, but does not act upon OFFN. The card is not powered-up, so no short-circuit or overheating is detected.
2. CMDVCCN Low: (within a card session) then, OFFN falls Low in any of the aforementioned cases. As soon as the fault is detected, an emergency deactivation is automatically performed. When the system controller sets CMDVCCN back to High, it may sense OFFN again after complete deactivation sequence. It does it to distinguish between a hardware problem or a card extraction. If the card is still present, OFFN then returns High.

A bounce may occur on PRESN signal during card insertion or withdrawal. It depends on the type of card presence switch within the connector (normally close or normally open), and on the mechanical characteristics of the switch. To counter the bounce, a debounce feature of approximately 4.05 ms ($t_{deb} = 1280 \times 1/(f_{osc(int)_Low})$) is integrated in the device.

When the card is inserted, OFFN goes High only at the end of the debounce time (see [Figure 9 on page 12](#)).

When the card is extracted, an automatic deactivation sequence of the card is performed on the first True/False transition on PRESN, and OFFN goes Low.

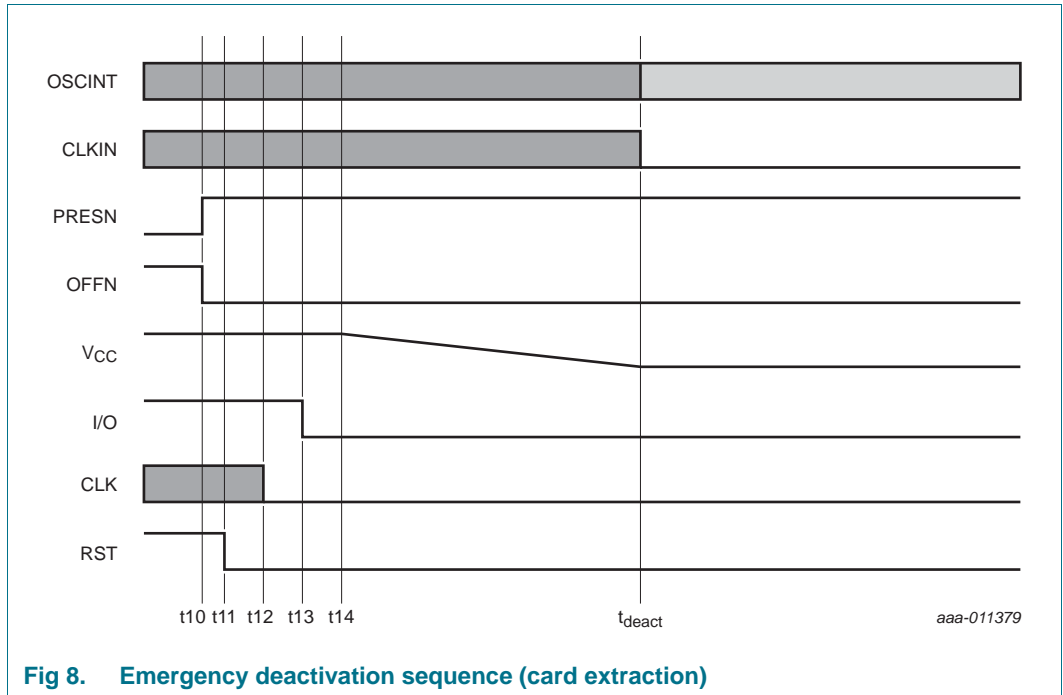


Fig 8. Emergency deactivation sequence (card extraction)

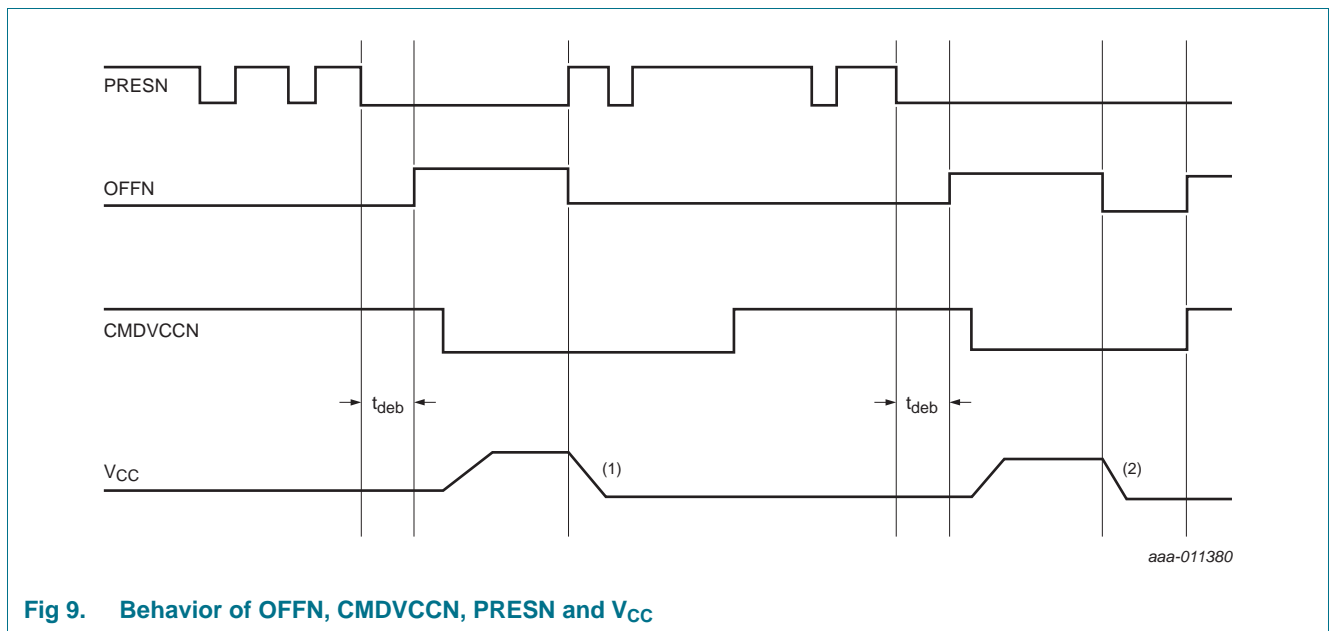


Fig 9. Behavior of OFFN, CMDVCCN, PRESN and V_{CC}

9. Limiting values

All card contacts are protected against a short-circuit with any other card contact.

Stress beyond the limiting values can damage the device permanently. The values are stress ratings only and functional operation of the device under these conditions is not implied.

Table 5. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

| Symbol | Parameter | Conditions | Min | Max | Unit |
|------------------|---------------------------------|---|------|------|------|
| V _{DD} | supply voltage | | -0.3 | +4.5 | V |
| V _{IH} | HIGH-level input voltage | CS, CLKDIV, PORADJ, PRESN, CMDVCCN, RSTIN, OFFN, CLKIN, I/OUC, AUX1UC, AUX2UC, V _{DD} | -0.3 | +4.5 | V |
| | | I/O, RST, AUX1, AUX2 and CLK | -0.3 | +4.5 | V |
| T _{amb} | ambient temperature | | -25 | +85 | °C |
| T _{stg} | storage temperature | | -55 | +150 | °C |
| T _j | junction temperature | | - | 125 | °C |
| P _{tot} | total power dissipation | T _{amb} = -25 °C to +85 °C | - | 0.1 | W |
| V _{ESD} | electrostatic discharge voltage | Human Body Model (HBM) on card pins I/O, RST, V _{CC} , AUX1, CLK, AUX2, PRESN within typical application | -8 | +8 | kV |
| | | Human Body Model (HBM) on all other pins | -2 | +2 | kV |
| | | Machine Model (MM) on all pins | -200 | +200 | V |
| | | Field Charged Device Model (FCDM) on all pins | -500 | +500 | V |

10. Thermal characteristics

Table 6. Thermal characteristics

| Symbol | Package name | Parameter | Conditions | Typ | Unit |
|----------------------|--------------|---|-------------|-----|------|
| R _{th(j-a)} | TSSOP16 | thermal resistance from junction to ambient | in free air | 160 | °C/W |
| R _{th(j-a)} | SO28 | thermal resistance from junction to ambient | in free air | 69 | °C/W |

11. Characteristics

Table 7. Characteristics of IC

$V_{DD} = 3.3\text{ V}$; Clock in = 10 MHz; GND = 0 V; $T_{amb} = 25\text{ }^{\circ}\text{C}$; unless otherwise specified

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|--|---|--|-------|-------|-------------|------------------|
| Supply voltage | | | | | | |
| V_{DD} | supply voltage | | 3 | 3.3 | 3.6 | V |
| I_{DD} | supply current | Shutdown mode; $f_{CLKIN} = \text{stopped}$ | - | 250 | 400 | μA |
| | | active mode; CLK = CLKIN; No-load | - | - | 5 | mA |
| | | active mode; CLK=CLKIN; $I_{CC} = 65\text{ mA}$ | - | - | 70 | mA |
| $V_{th(VREG)}$ | V_{REG} threshold voltage | falling | 1.20 | 1.35 | 1.5 | V |
| $V_{hys(VREG)}$ | V_{REG} hysteresis voltage | | 60 | 75 | 90 | mV |
| $V_{th(VDD)}$ | V_{DD} threshold voltage | falling | 2.45 | 2.6 | 2.75 | V |
| $V_{hys(VDD)}$ | V_{DD} hysteresis voltage | | 10 | 50 | 100 | mV |
| t_w | pulse width | | 4.87 | 6.82 | 11.3 | ms |
| $V_{th(L)(PORADJ)}$ | LOW-level threshold voltage on pin PORADJ | external resistors on PORADJ | 0.75 | 0.84 | 0.93 | V |
| $V_{hys(PORADJ)}$ | hysteresis voltage on pin PORADJ | | 20 | 75 | 130 | mV |
| I_L | leakage current | pin PORADJ | -1 | - | +1 | μA |
| V_{REG} | | | | | | |
| V_o | output voltage | | 1.62 | 1.8 | 1.98 | V |
| Card supply voltage (V_{CC})^[1] | | | | | | |
| C_{dec} | decoupling capacitance | connected on V_{CC} (220 nF + 220 nF 10 %) | 396 | - | 484 | nF |
| V_o | output voltage | inactive mode; no load | -0.1 | - | +0.1 | V |
| | | inactive mode; $I_o = 1\text{ mA}$ | -0.1 | - | +0.3 | V |
| I_o | output current | inactive mode at grounded pin V_{CC} | - | - | -1 | mA |
| V_{CC} | supply voltage | active mode; $I_{CC} < 65\text{ mA DC}$ | 2.85 | 3.05 | 3.15 | V |
| | | active mode; current pulses of 40 nA/s with $I_{CC} < 200\text{ mA}$, $t < 400\text{ ns}$; | 2.76 | - | 3.20 | V |
| $V_{ripple(p-p)}$ | peak-to-peak ripple voltage | from 20 kHz to 200 MHz | - | - | 150 | mV |
| I_{CC} | supply current | | - | - | 65 | mA |
| SR | slew rate | | 0.030 | 0.075 | 0.120 | V/ μs |
| External clock (CLKIN) | | | | | | |
| $f_{ext(CLKIN)}$ | external frequency on pin CLKIN | | 1 | - | 20 | MHz |
| δ | duty cycle | | 48 | - | 52 | % |
| V_{IL} | LOW-level input voltage | | -0.3 | - | $0.3V_{DD}$ | V |

Table 7. Characteristics of IC ...continued

$V_{DD} = 3.3\text{ V}$; Clock in = 10 MHz; GND = 0 V; $T_{amb} = 25\text{ }^{\circ}\text{C}$; unless otherwise specified

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|--|---------------------------|---|----------------|------|----------------|---------------|
| V_{IH} | HIGH-level input voltage | | $0.7V_{DD}$ | - | $V_{DD} + 0.3$ | V |
| $t_{r(i)}$ | input rise time | $f_{CLK} = f_{CLKIN} = 20\text{ MHz}$ on external clock | - | - | 4 | ns |
| | | $f_{CLK} = f_{CLKIN} = 10\text{ MHz}$ on external clock | - | - | 8 | ns |
| | | $f_{CLK} = f_{CLKIN} = 5\text{ MHz}$ on external clock | - | - | 16 | ns |
| $t_{f(i)}$ | input fall time | $f_{CLK} = f_{CLKIN} = 20\text{ MHz}$ on external clock | - | - | 4 | ns |
| | | $f_{CLK} = f_{CLKIN} = 10\text{ MHz}$ on external clock | - | - | 8 | ns |
| | | $f_{CLK} = f_{CLKIN} = 5\text{ MHz}$ on external clock | - | - | 16 | ns |
| Data lines (pins I/O, I/OUC, AUX1, AUX2, AUX1UC, AUX2UC) | | | | | | |
| t_d | delay time | falling edge on pins I/O and I/OUC or I/OUC and I/O | - | - | 200 | ns |
| $t_{w(pu)}$ | pull-up pulse width | | 200 | - | 400 | ns |
| f_{max} | maximum frequency | on data lines | - | - | 1 | MHz |
| C_i | input capacitance | on data lines | - | - | 10 | pF |
| Data lines to the card (pins I/O, AUX1, AUX2); (Integrated 10 kΩ pull-up resistor connected to V_{CC}) | | | | | | |
| V_o | output voltage | inactive mode; no load | 0 | - | 0.1 | V |
| | | inactive mode; $I_o = 1\text{ mA}$ | 0 | - | 0.3 | V |
| I_o | output current | inactive mode at grounded pin I/O | - | - | -1 | mA |
| V_{OL} | LOW-level output voltage | $I_{OL} = 1\text{ mA}$ | 0 | - | 0.3 | V |
| | | $I_{OL} \geq 15\text{ mA}$ | $V_{CC} - 0.4$ | - | V_{CC} | V |
| V_{OH} | HIGH-level output voltage | No DC load | $0.9V_{CC}$ | - | $V_{CC} + 0.1$ | V |
| | | $I_{OH} < -40\text{ }\mu\text{A}$ | $0.8V_{CC}$ | - | $V_{CC} + 0.1$ | V |
| | | $I_{OH} \geq -15\text{ mA}$ | 0 | - | 0.4 | V |
| V_{IL} | LOW-level input voltage | | -0.3 | - | +0.8 | V |
| V_{IH} | HIGH-level input voltage | | $0.6V_{CC}$ | - | V_{CC} | V |
| V_{hys} | hysteresis voltage | on I/O | 30 | 115 | 200 | mV |
| I_{IL} | LOW-level input current | on I/O; $V_{IL} = 0$ | - | - | 600 | μA |
| I_{IH} | HIGH-level input current | on I/O; $V_{IH} = V_{CC}$ | - | - | 10 | μA |
| $t_{r(i)}$ | input rise time | from $V_{IL\text{ max}}$ to $V_{IH\text{ min}}$ | - | - | 1.2 | μs |
| $t_{f(i)}$ | input fall time | from $V_{IL\text{ max}}$ to $V_{IH\text{ min}}$ | - | - | 1.2 | μs |
| $t_{r(o)}$ | output rise time | $C_L \leq 80\text{ pF}$; 10 % to 90 % from 0 to V_{CC} | - | - | 0.1 | μs |
| $t_{f(o)}$ | output fall time | $C_L \leq 80\text{ pF}$; 10 % to 90 % from 0 to V_{CC} | - | - | 0.1 | μs |
| R_{pu} | pull-up resistance | connected to V_{CC} | 8 k | 10 k | 12 k | Ω |
| I_{pu} | pull-up current | $V_{OH} = 0.9 V_{CC}$, $C = 80\text{ pF}$ | -20 | -12 | -4 | mA |

Table 7. Characteristics of IC ...continued $V_{DD} = 3.3\text{ V}$; Clock in = 10 MHz; GND = 0 V; $T_{amb} = 25\text{ }^{\circ}\text{C}$; unless otherwise specified

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|--|-------------------------------|--|----------------|-----|----------------|---------------|
| V_{high} | high voltage | instantaneous voltage level: 1 pF cross capacitance load between pin I/O and CLK | $0.7V_{CC}$ | - | $V_{CC} + 0.3$ | V |
| V_{low} | low voltage | instantaneous voltage level: 1 pF cross capacitance load between pin I/O and CLK | -0.3 | - | +0.4 | V |
| Data lines to the system; pins I/OμC, AUX1μC, AUX2μC (Integrated 10kΩ pull-up resistor to V_{DD}) | | | | | | |
| V_{OL} | LOW-level output voltage | $I_{OL} = 1\text{ mA}$ | 0 | - | 0.3 | V |
| V_{OH} | HIGH-level output voltage | No DC load | $0.9V_{DD}$ | - | $V_{DD} + 0.1$ | V |
| | | $I_{OH} \leq 40\text{ }\mu\text{A}$ | $0.75V_{DD}$ | - | $V_{DD} + 0.1$ | V |
| V_{IL} | LOW-level input voltage | | -0.3 | - | $0.3V_{DD}$ | V |
| V_{IH} | HIGH-level input voltage | | $0.7V_{DD}$ | | $V_{DD} + 0.3$ | V |
| V_{hys} | hysteresis voltage | on I/Ouc | $0.05V_{DD}$ | - | $0.25V_{DD}$ | V |
| I_{LH} | HIGH-level leakage current | $V_{IH} = V_{DD}$ | - | - | 10 | μA |
| I_{IL} | LOW-level input current | $V_{IL} = 0$ | - | - | 600 | μA |
| R_{pu} | pull-up resistance | connected to V_{DD} | 8 | 11 | 14 | k Ω |
| $t_{r(i)}$ | input rise time | from V_{IL} max to V_{IH} min | - | - | 1.2 | μs |
| $t_{f(i)}$ | input fall time | from V_{IL} max to V_{IH} min | - | - | 1.2 | μs |
| $t_{r(o)}$ | output rise time | $C_L \leq 30\text{ pF}$; 10 % to 90 % from 0 to V_{DD} | - | - | 0.1 | μs |
| $t_{f(o)}$ | output fall time | $C_L \leq 30\text{ pF}$; 10% to 90% from 0 to V_{DD} | - | - | 0.1 | μs |
| I_{pu} | pull-up current | $V_{OH} = 0.9 V_{DD}$, $C = 30\text{ pF}$ | -1 | - | - | mA |
| Internal oscillator | | | | | | |
| $f_{osc(int)}$ | internal oscillator frequency | inactive state: osc(int)_Low | 180 | 300 | 420 | kHz |
| | | active state: osc(int)_High | 1.5 | 2.5 | 3.5 | MHz |
| Reset output to the card (RST) | | | | | | |
| V_o | output voltage | inactive mode; no load | 0 | - | 0.1 | V |
| | | inactive mode; $I_o = 1\text{ mA}$ | 0 | - | 0.3 | V |
| I_o | output current | inactive mode at grounded pin RST | - | - | -1 | mA |
| t_d | delay time | between RSTIN and RST, RST enabled | - | - | 200 | ns |
| V_{OL} | LOW-level output voltage | $I_{OL} = 200\text{ }\mu\text{A}$ | 0 | - | 0.2 | V |
| | | $I_{OL} = 20\text{ mA}$ (current limit) | $V_{CC} - 0.4$ | - | V_{CC} | V |
| V_{OH} | HIGH-level output voltage | $I_{OH} = -200\text{ }\mu\text{A}$ | $0.9V_{CC}$ | - | V_{CC} | V |
| | | $I_{OH} = -20\text{ mA}$ (current limit) | 0 | - | 0.4 | V |
| t_r | rise time | $C_L = 100\text{ pF}$ | - | - | 0.1 | μs |
| t_f | fall time | $C_L = 100\text{ pF}$ | - | - | 0.1 | μs |
| V_{high} | high voltage | instantaneous voltage level: 1 pF cross capacitance load between pin RST and CLK | $0.85V_{CC}$ | - | $V_{CC} + 0.3$ | V |

Table 7. Characteristics of IC ...continued

$V_{DD} = 3.3\text{ V}$; Clock in = 10 MHz; GND = 0 V; $T_{amb} = 25\text{ }^{\circ}\text{C}$; unless otherwise specified

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|--|----------------------------|--|----------------|-----|-------------------|---------------|
| V_{low} | low voltage | instantaneous voltage level: 1 pF cross capacitance load between pin RST and CLK | -0.3 | - | +0.32 | V |
| Clock output to the card (CLK) | | | | | | |
| V_o | output voltage | inactive mode; no load | 0 | - | 0.1 | V |
| | | inactive mode; $I_o = 1\text{ mA}$ | 0 | - | 0.3 | V |
| I_o | output current | inactive mode at grounded pin CLK | - | - | -1 | mA |
| V_{OL} | LOW-level output voltage | $I_{OL} = 200\text{ }\mu\text{A}$ | 0 | - | 0.3 | V |
| | | $I_{OL} = 70\text{ mA}$ (current limit) | $V_{CC} - 0.4$ | - | V_{CC} | V |
| V_{OH} | HIGH-level output voltage | $I_{OH} = -200\text{ }\mu\text{A}$ | $0.9V_{CC}$ | - | V_{CC} | V |
| | | $I_{OH} = -70\text{ mA}$ (current limit) | 0 | - | 0.4 | V |
| t_r | rise time | $C_L = 30\text{ pF}$ [2], $f_{CLK} = 5\text{ MHz}$ | - | - | 16 | ns |
| | | $C_L = 30\text{ pF}$ [2], $f_{CLK} = 10\text{ MHz}$ | - | - | 8 | ns |
| t_f | fall time | $C_L = 30\text{ pF}$ [2], $f_{CLK} = 5\text{ MHz}$ | - | - | 16 | ns |
| | | $C_L = 30\text{ pF}$ [2], $f_{CLK} = 10\text{ MHz}$ | - | - | 8 | ns |
| f_{clk} | clock frequency on pin CLK | operational | 0 | - | 10 | MHz |
| δ | duty cycle | $C_L = 30\text{ pF}$ [2] | 45 | - | 55 | % |
| SR | slew rate | rise and fall; $C_L = 30\text{ pF}$ | 0.12 | - | - | V/ns |
| V_{high} | high voltage | instantaneous voltage level: 1 pF cross capacitance load between pin CLK and RST or CLK and I/O | $0.85V_{CC}$ | - | $V_{CC} + 0.3$ | V |
| V_{low} | low voltage | instantaneous voltage level: 1 pF cross capacitance load between pin RST and I/O | -0.3 | - | +0.50 | V |
| Control inputs (pins CS, CMDVCCN, CLKDIV, RSTIN, TEST) [3] | | | | | | |
| V_{IL} | LOW-level input voltage | | -0.3 | - | $+0.3V_{DD}$ | V |
| V_{IH} | HIGH-level input voltage | | $0.7V_{DD}$ | - | $V_{DD} + 0.3$ | V |
| V_{hys} | hysteresis voltage | on control input | $0.05V_{DD}$ | - | $0.25V_{DD}$ | V |
| I_{LL} | LOW-level leakage current | $V_{IL} = 0$ | - | - | 1 | μA |
| I_{LH} | HIGH-level leakage current | $V_{IH} = V_{DD}$ | - | - | 1 | μA |
| Card presence input (PRESN); PRESN has an integrated pull down resistor [3] | | | | | | |
| V_{IL} | LOW-level input voltage | | -0.3 | - | $0.3V_{DD(INTF)}$ | V |
| V_{IH} | HIGH-level input voltage | | $0.7V_{DD}$ | - | $V_{DD} + 0.3$ | V |
| V_{hys} | hysteresis voltage | | $0.05V_{DD}$ | - | $0.1V_{DD}$ | V |
| I_{LL} | LOW-level leakage current | $V_{IL} = 0$ | - | - | 1 | μA |
| I_{LH} | HIGH-level leakage current | $V_{IH} = V_{DD}$ | - | - | 5 | μA |

Table 7. Characteristics of IC ...continued

$V_{DD} = 3.3\text{ V}$; Clock in = 10 MHz; GND = 0 V; $T_{amb} = 25\text{ }^{\circ}\text{C}$; unless otherwise specified

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---|---------------------------|--|--------------|------|------|--------------------|
| OFFN output (pin OFFN is an NMOS drain with a 10 kΩ pull-up resistor to V_{DD}) | | | | | | |
| V_{OL} | LOW-level output voltage | $I_{OL} = 2\text{ mA}$ | 0 | - | 0.3 | V |
| V_{OH} | HIGH-level output voltage | $I_{OH} = -15\text{ }\mu\text{A}$ | $0.75V_{DD}$ | - | - | V |
| R_{pu} | pull-up resistance | | 8 | 10 | 13 | kΩ |
| Protections and limitations | | | | | | |
| T_{sd} | shutdown temperature | at die | - | 150 | - | $^{\circ}\text{C}$ |
| I_{Olim} | output current limit | on pin I/O, AUX1 and AUX2 | -15 | - | +15 | mA |
| | | on pin CLK | -70 | - | +70 | mA |
| | | on pin RST | -20 | - | +20 | mA |
| | | on pin V_{CC} | 94 | 130 | 160 | mA |
| I_{sd} | shutdown current | on pin V_{CC} | 90 | 120 | 150 | mA |
| Timing | | | | | | |
| t_{act} | activation time | see Figure 6 on page 9 | 182 | - | 554 | μs |
| t_{deact} | deactivation time | see Figure 7 on page 10 | 35 | - | 250 | μs |
| t_{act} | activation time | time of the window for sending CLK to the card with CLKIN | | | | |
| | | $t_{act(start)} = t3$; see Figure 6 on page 9 | 182 | 256 | 426 | μs |
| | | $t_{act(end)} = t5$; see Figure 6 on page 9 | 237 | 332 | 554 | μs |
| t_{deb} | debounce time | on pin PRESN | 3.04 | 4.26 | 7.11 | ms |

- [1] To meet these specifications, V_{CC} is decoupled to CGND using two ceramic multilayer capacitors of low ESR with both capacitors having a value of 220 nF.
- [2] The transition time and the duty factor definitions are shown in [Figure 10 on page 18](#); $d = t1/(t1 + t2)$
- [3] PRESN and CMDVCCN are active LOW; RSTIN is active HIGH; for CLKDIV see [Table 4](#).

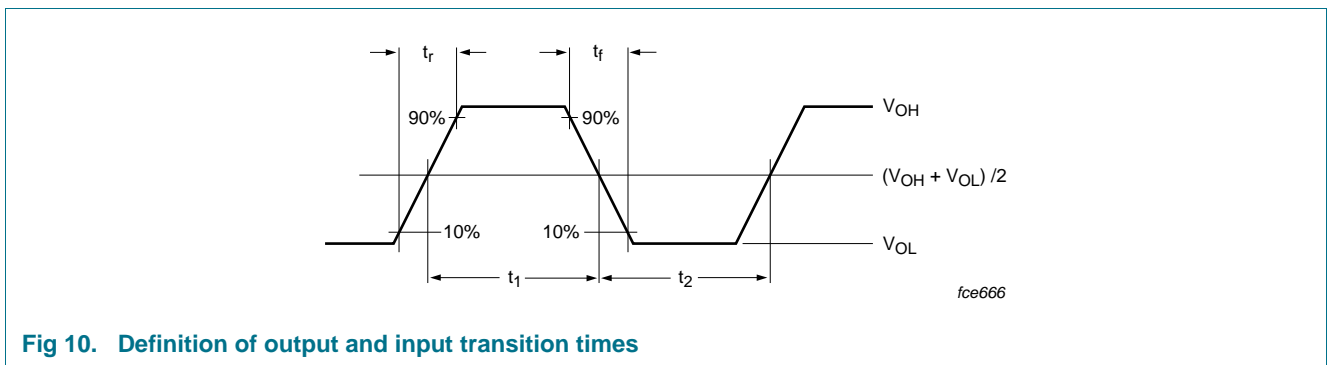


Fig 10. Definition of output and input transition times

12. Application information

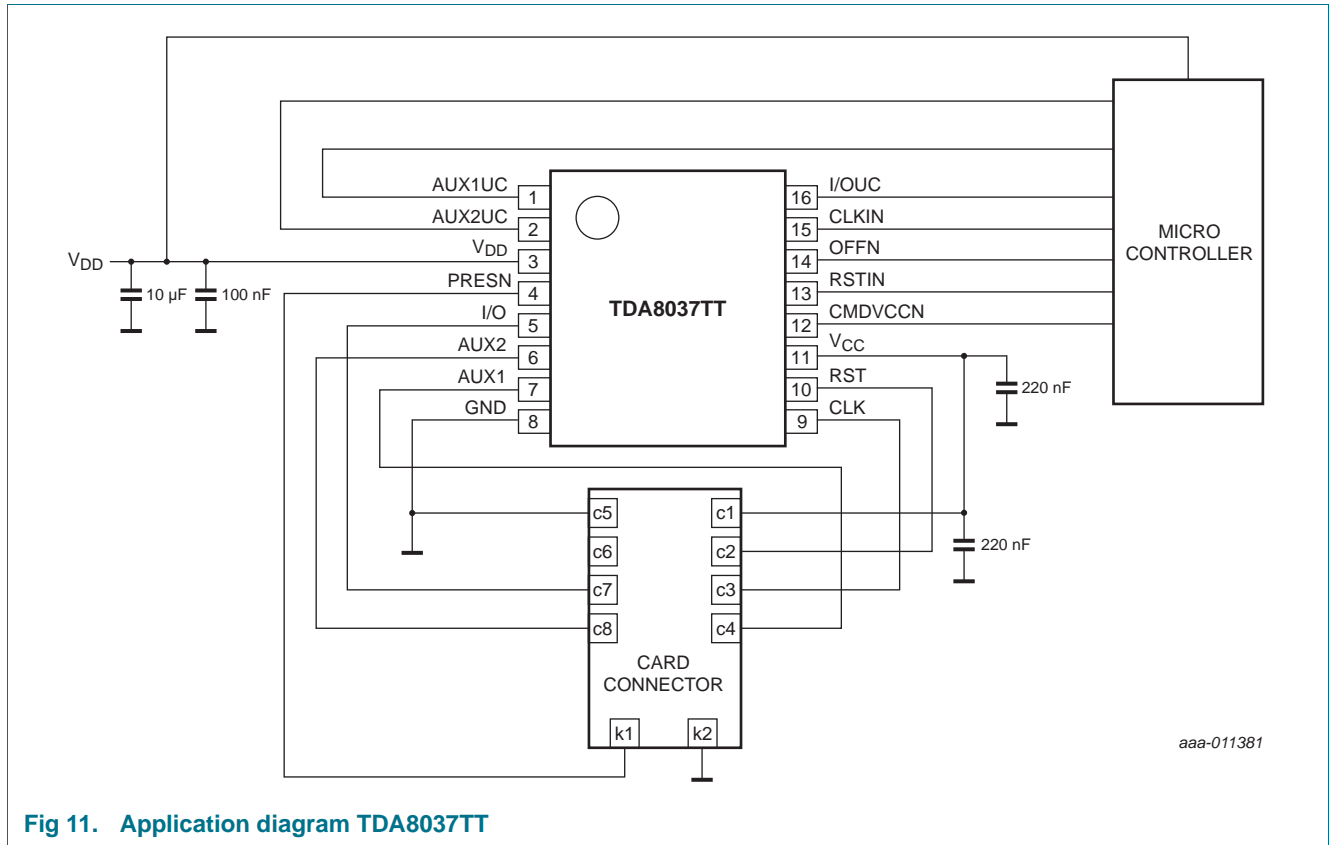
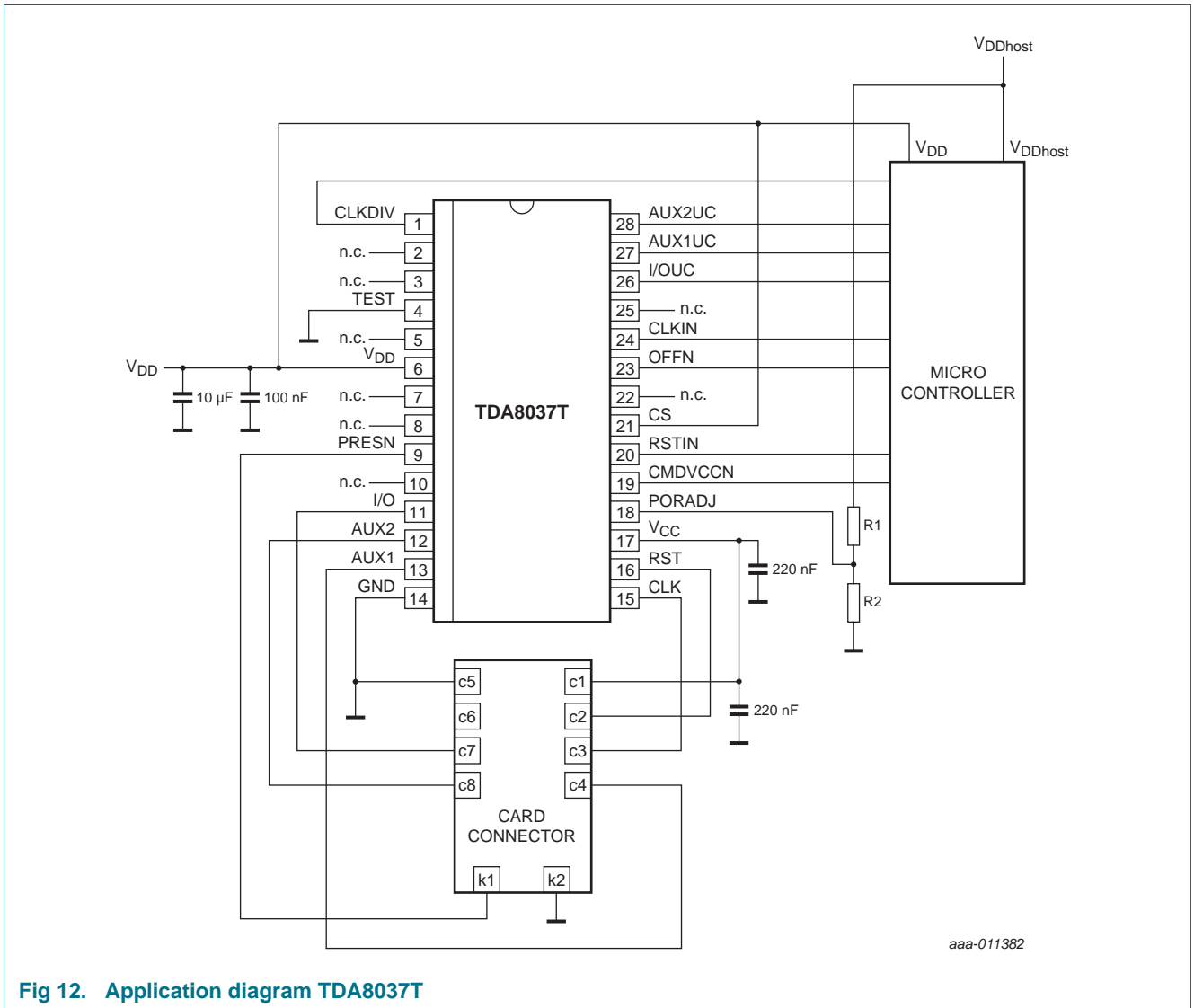


Fig 11. Application diagram TDA8037TT



aaa-011382

Fig 12. Application diagram TDA8037T

13. Package outline

SO28: plastic small outline package; 28 leads; body width 7.5 mm

SOT136-1

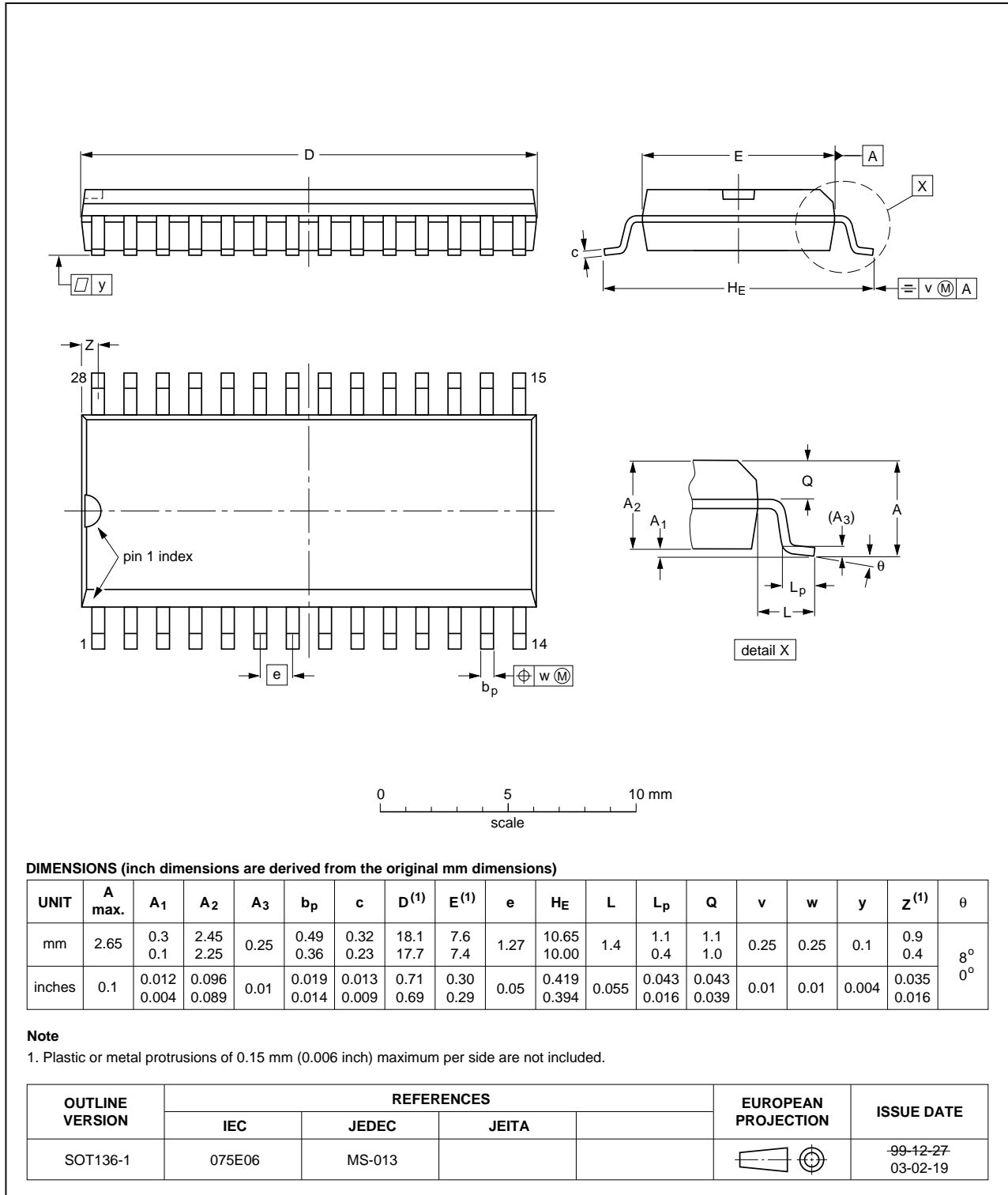


Fig 13. Package outline SOT136-1

TSSOP16: plastic thin shrink small outline package; 16 leads; body width 4.4 mm

SOT403-1

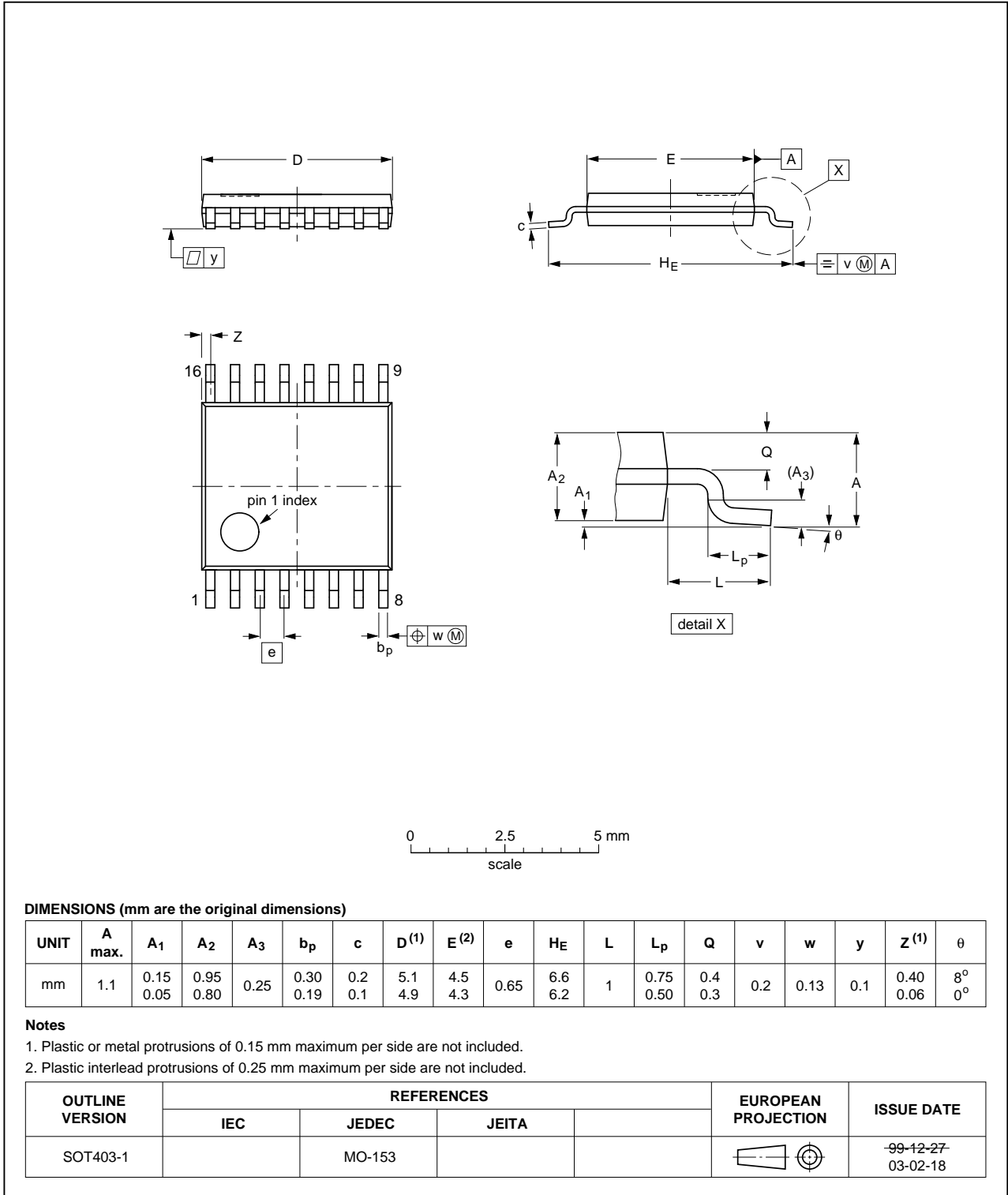


Fig 14. Package outline SOT403-1

14. Soldering of SMD packages

This text provides a very brief insight into a complex technology. A more in-depth account of soldering ICs can be found in Application Note *AN10365 "Surface mount reflow soldering description"*.

14.1 Introduction to soldering

Soldering is one of the most common methods through which packages are attached to Printed Circuit Boards (PCBs), to form electrical circuits. The soldered joint provides both the mechanical and the electrical connection. There is no single soldering method that is ideal for all IC packages. Wave soldering is often preferred when through-hole and Surface Mount Devices (SMDs) are mixed on one printed wiring board; however, it is not suitable for fine pitch SMDs. Reflow soldering is ideal for the small pitches and high densities that come with increased miniaturization.

14.2 Wave and reflow soldering

Wave soldering is a joining technology in which the joints are made by solder coming from a standing wave of liquid solder. The wave soldering process is suitable for the following:

- Through-hole components
- Leaded or leadless SMDs, which are glued to the surface of the printed circuit board

Not all SMDs can be wave soldered. Packages with solder balls, and some leadless packages which have solder lands underneath the body, cannot be wave soldered. Also, leaded SMDs with leads having a pitch smaller than ~0.6 mm cannot be wave soldered, due to an increased probability of bridging.

The reflow soldering process involves applying solder paste to a board, followed by component placement and exposure to a temperature profile. Leaded packages, packages with solder balls, and leadless packages are all reflow solderable.

Key characteristics in both wave and reflow soldering are:

- Board specifications, including the board finish, solder masks and vias
- Package footprints, including solder thieves and orientation
- The moisture sensitivity level of the packages
- Package placement
- Inspection and repair
- Lead-free soldering versus SnPb soldering

14.3 Wave soldering

Key characteristics in wave soldering are:

- Process issues, such as application of adhesive and flux, clinching of leads, board transport, the solder wave parameters, and the time during which components are exposed to the wave
- Solder bath specifications, including temperature and impurities

14.4 Reflow soldering

Key characteristics in reflow soldering are:

- Lead-free versus SnPb soldering; note that a lead-free reflow process usually leads to higher minimum peak temperatures (see [Figure 15](#)) than a SnPb process, thus reducing the process window
- Solder paste printing issues including smearing, release, and adjusting the process window for a mix of large and small components on one board
- Reflow temperature profile; this profile includes preheat, reflow (in which the board is heated to the peak temperature) and cooling down. It is imperative that the peak temperature is high enough for the solder to make reliable solder joints (a solder paste characteristic). In addition, the peak temperature must be low enough that the packages and/or boards are not damaged. The peak temperature of the package depends on package thickness and volume and is classified in accordance with [Table 8](#) and [9](#)

Table 8. SnPb eutectic process (from J-STD-020D)

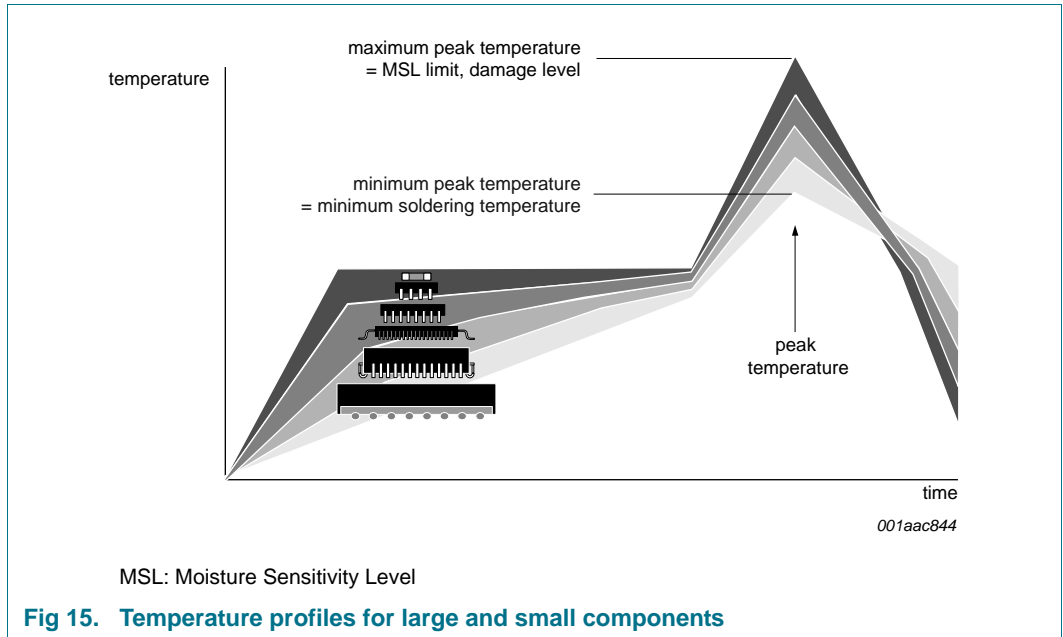
| Package thickness (mm) | Package reflow temperature (°C) | |
|------------------------|---------------------------------|-------|
| | Volume (mm ³) | |
| | < 350 | ≥ 350 |
| < 2.5 | 235 | 220 |
| ≥ 2.5 | 220 | 220 |

Table 9. Lead-free process (from J-STD-020D)

| Package thickness (mm) | Package reflow temperature (°C) | | |
|------------------------|---------------------------------|-------------|--------|
| | Volume (mm ³) | | |
| | < 350 | 350 to 2000 | > 2000 |
| < 1.6 | 260 | 260 | 260 |
| 1.6 to 2.5 | 260 | 250 | 245 |
| > 2.5 | 250 | 245 | 245 |

Moisture sensitivity precautions, as indicated on the packing, must be respected at all times.

Studies have shown that small packages reach higher temperatures during reflow soldering, see [Figure 15](#).



For further information on temperature profiles, refer to Application Note AN10365 “Surface mount reflow soldering description”.

15. Abbreviations

Table 10. Abbreviations

| Acronym | Description |
|---------|-------------------------|
| ESD | ElectroStatic Discharge |

16. Revision history

Table 11. Revision history

| Document ID | Release date | Data sheet status | Change notice | Supersedes |
|----------------|---|--------------------|---------------|---------------|
| TDA8037 v.1.2 | 20160630 | Product data sheet | | TDA8037 v.1.1 |
| Modifications: | <ul style="list-style-type: none"> EMVCo 4.3 compliance added Table 7 “Characteristics of IC”: values of “HIGH-level output voltage” and “HIGH-level input voltage” updated | | | |
| TDA8037 v.1.1 | 20141117 | Product data sheet | - | TDA8037 v.1 |
| Modifications: | <ul style="list-style-type: none"> Table 3 “Pin description”: updated | | | |
| TDA8037 v.1 | 20141007 | Product data sheet | - | - |

17. Legal information

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| Document status ^{[1][2]} | Product status ^[3] | Definition |
|-----------------------------------|-------------------------------|---|
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| Preliminary [short] data sheet | Qualification | This document contains data from the preliminary specification. |
| Product [short] data sheet | Production | This document contains the product specification. |

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

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