

TOSHIBA CMOS Digital Integrated Circuit Silicon Monolithic

TC74VHC161F, TC74VHC161FK TC74VHC163F, TC74VHC163FK

Synchronous Presetable 4-Bit Counter

TC74VHC161F/FK Binary, Asynchronous Clear

TC74VHC163F/FK Binary, Synchronous Clear

The TC74VHC 161 and 163 are advanced high speed CMOS SYNCHRONOUS PRESETTABLE 4 BIT BINARY COUNTERs fabricated with silicon gate CMOS technology.

They achieve the high speed operation similar to equivalent Bipolar Schottky TTL while maintaining the CMOS low power dissipation.

The CK input is active on the rising edge. Both \overline{LOAD} and \overline{CLR} inputs are active on low logic level.

Presetting of each IC's is synchronous to the rising edge of CK.

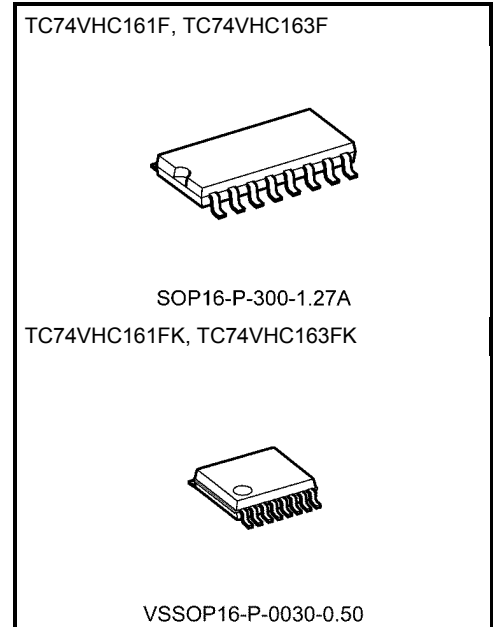
The clear function of the TC74VHC163 is synchronous to CK, while the TC74VHC161 are cleared asynchronously.

Two enable inputs (ENP and ENT) and CARRY OUTPUT are provided to enable easy cascading of counters, which facilitates easy implementation of n-bit counters without using external gates.

An input protection circuit ensures that 0 to 5.5 V can be applied to the input pins without regard to the supply voltage. This device can be used to interface 5 V to 3 V systems and two supply systems such as battery back up. This circuit prevents device destruction due to mismatched supply and input voltages.

Features

- High speed: $f_{max} = 185$ MHz (typ.) at $V_{CC} = 5$ V
- Low power dissipation: $I_{CC} = 4$ μ A (max) at $T_a = 25^\circ$ C
- High noise immunity: $V_{NIH} = V_{NIL} = 28\%$ V_{CC} (min)
- Power down protection is provided on all inputs.
- Balanced propagation delays: $t_{pLH} \approx t_{pHL}$
- Wide operating voltage range: $V_{CC} (opr) = 2$ to 5.5 V
- Low noise: $V_{OLP} = 0.8$ V (max)
- Pin and function compatible with 74ALS161/163

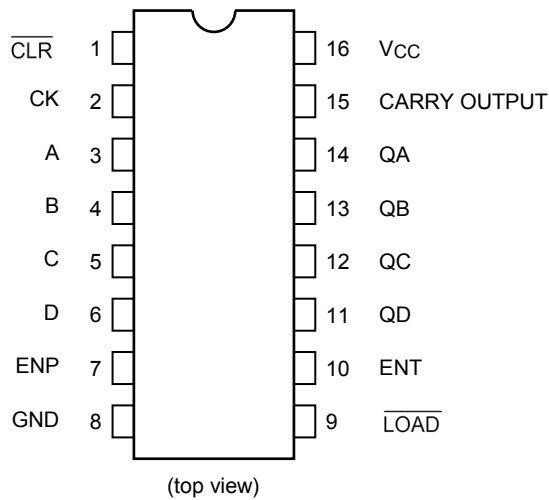


Weight

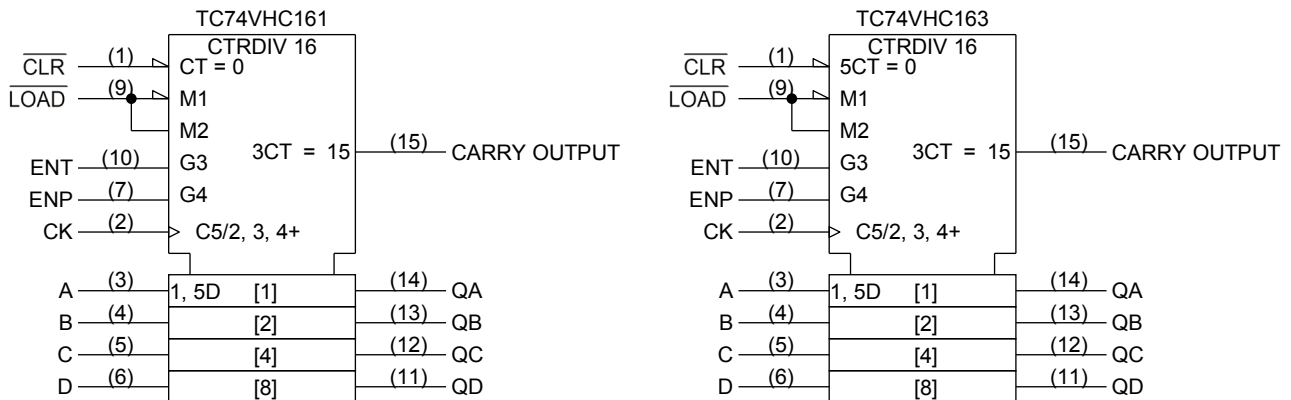
SOP16-P-300-1.27A	: 0.18 g (typ.)
VSSOP16-P-0030-0.50	: 0.02 g (typ.)

Start of commercial production
1991-11

Pin Assignment



IEC Logic Symbol



Truth Table (Note)

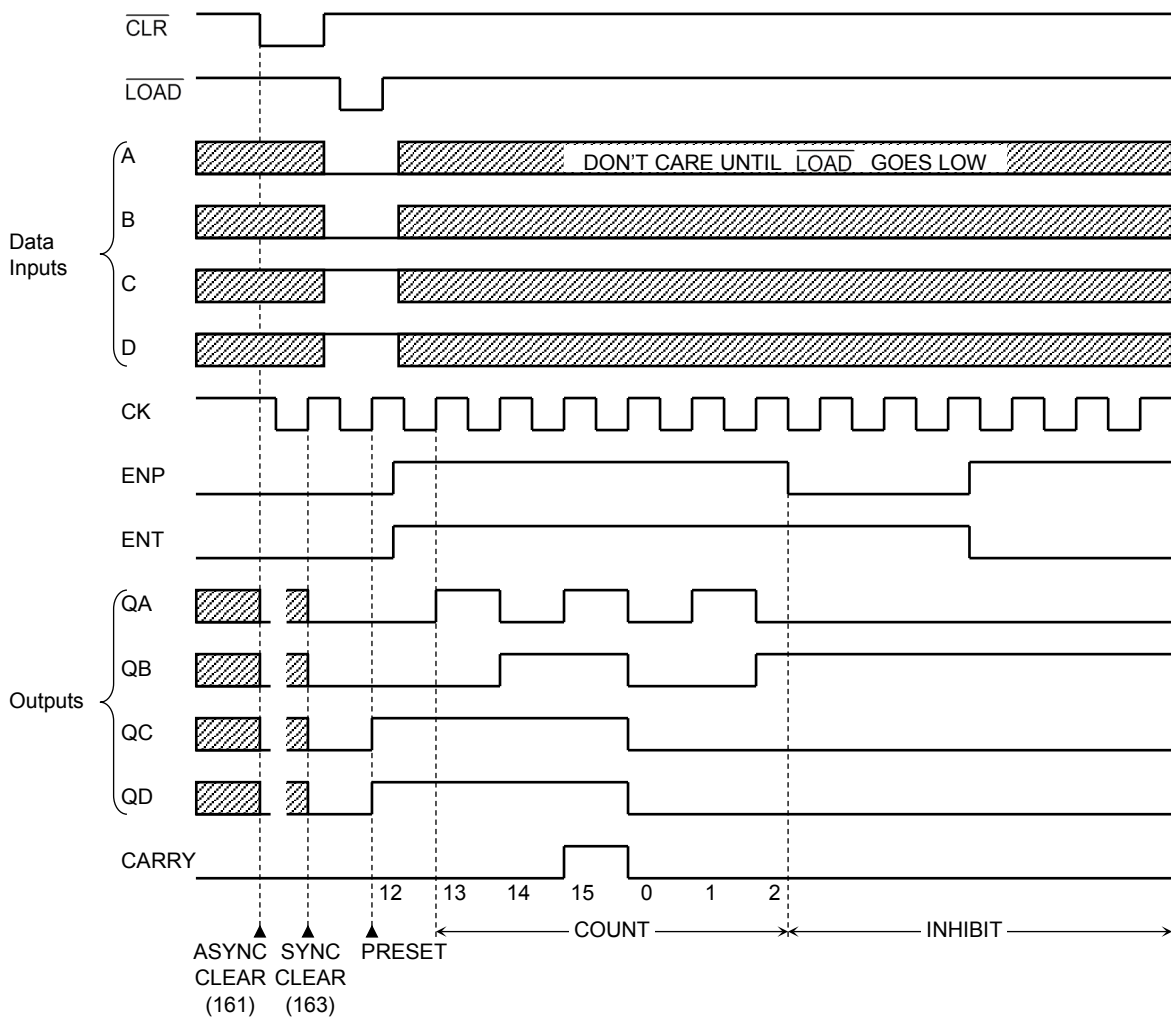
TC74VHC161					TC74VHC163					Outputs				Function
Inputs					Inputs					QA	QB	QC	QD	
CLR	LD	ENP	ENT	CK	CLR	LD	ENP	ENT	CK					
L	X	X	X	X	L	X	X	X	↑	L	L	L	L	Reset to "0"
H	L	X	X	↑	H	L	X	X	↑	A	B	C	D	Preset Data
H	H	X	L	↑	H	H	X	L	↑	No Change				No Count
H	H	L	X	↑	H	H	L	X	↑	No Change				No Count
H	H	H	H	↑	H	H	H	H	↑	Count Up				Count
H	X	X	X	↓	X	X	X	X	↓	No Change				No Count

Note: X: Don't care

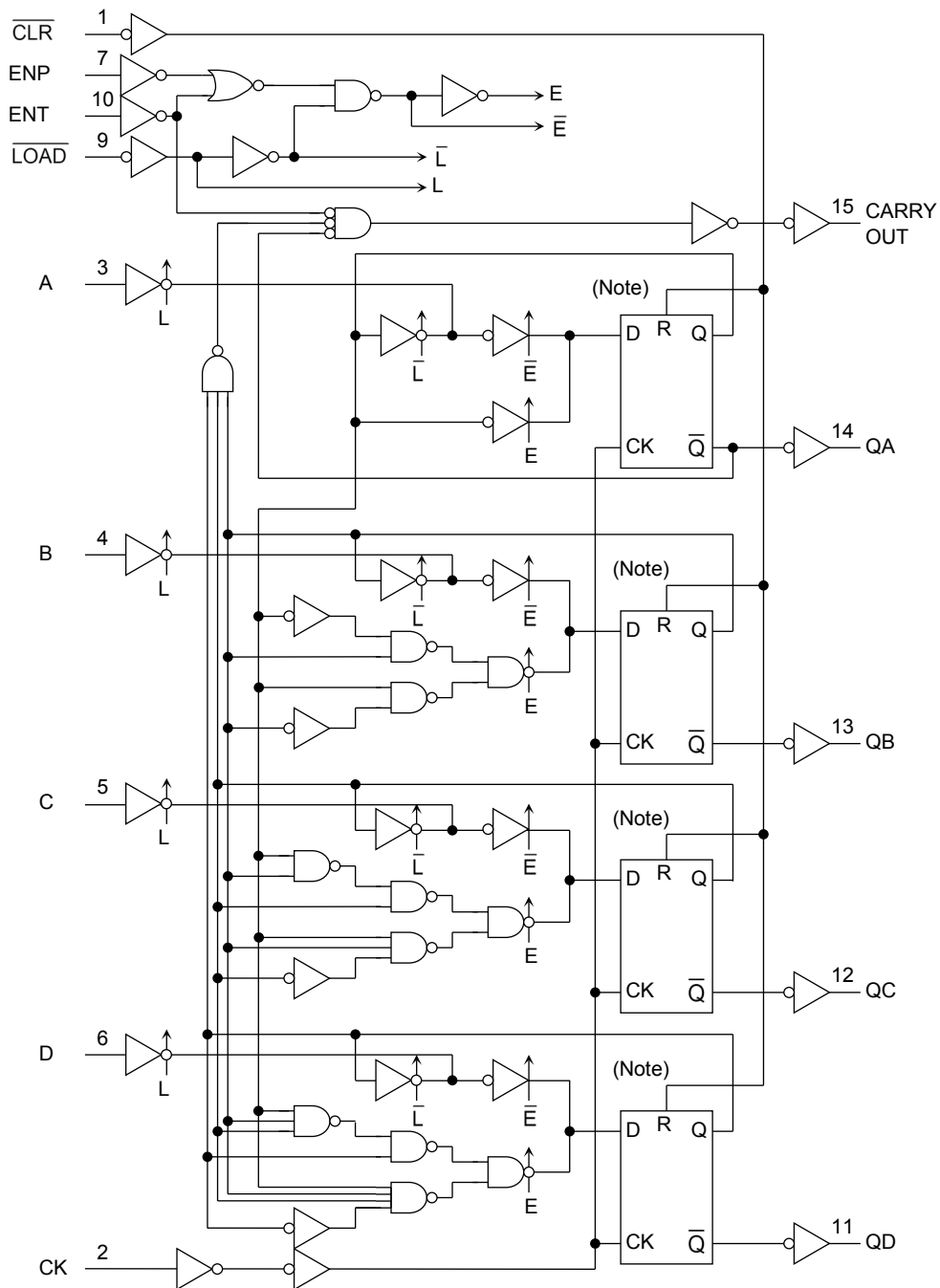
A, B, C, D: Logic level of data inputs

Carry: CARRY = ENT · QA · QB · QC · QD

Timing Chart



System Diagram



Note: Truth table of internal F/F

TC74VHC161					TC74VHC163				
D	CK	R	Q	\bar{Q}	D	CK	R	Q	\bar{Q}
X	X	H	L	H	X	\uparrow	H	L	H
L	\uparrow	L	L	H	L	\uparrow	L	L	H
H	\uparrow	L	H	L	H	\uparrow	L	H	L
X	\downarrow	L	No Change		X	\downarrow	X	No Change	

X: Don't care

Absolute Maximum Ratings (Note)

Characteristics	Symbol	Rating	Unit
Supply voltage range	V _{CC}	-0.5 to 7.0	V
DC input voltage	V _{IN}	-0.5 to 7.0	V
DC output voltage	V _{OUT}	-0.5 to V _{CC} + 0.5	V
Input diode current	I _{IK}	-20	mA
Output diode current	I _{OK}	±20	mA
DC output current	I _{OUT}	±25	mA
DC V _{CC} /ground current	I _{CC}	±50	mA
Power dissipation	P _D	180	mW
Storage temperature	T _{stg}	-65 to 150	°C

Note: Exceeding any of the absolute maximum ratings, even briefly, lead to deterioration in IC performance or even destruction.
 Using continuously under heavy loads (e.g. the application of high temperature/current/voltage and the significant change in temperature, etc.) may cause this product to decrease in the reliability significantly even if the operating conditions (i.e. operating temperature/current/voltage, etc.) are within the absolute maximum ratings and the operating ranges.
 Please design the appropriate reliability upon reviewing the Toshiba Semiconductor Reliability Handbook (“Handling Precautions”/“Derating Concept and Methods”) and individual reliability data (i.e. reliability test report and estimated failure rate, etc).

Operating Range (Note)

Characteristics	Symbol	Rating	Unit
Supply voltage	V _{CC}	2.0 to 5.5	V
Input voltage	V _{IN}	0 to 5.5	V
Output voltage	V _{OUT}	0 to V _{CC}	V
Operating temperature	T _{opr}	-40 to 85	°C
Input rise and fall time	dt/dv	0 to 100 (V _{CC} = 3.3 ± 0.3 V) 0 to 20 (V _{CC} = 5 ± 0.5 V)	ns/V

Note: The operating ranges must be maintained to ensure the normal operation of the device.
 Unused inputs must be tied to either V_{CC} or GND.

Electrical Characteristics

DC Characteristics

Characteristics	Symbol	Test Condition		Ta = 25°C			Ta = -40 to 85°C		Unit	
				VCC (V)	Min	Typ.	Max	Min		Max
High-level input voltage	V _{IH}	—		2.0 3.0 to 5.5	1.50 V _{CC} × 0.7	— —	— —	1.50 V _{CC} × 0.7	— —	V
Low-level input voltage	V _{IL}	—		2.0 3.0 to 5.5	— —	— —	0.50 V _{CC} × 0.3	— —	0.50 V _{CC} × 0.3	V
High-level output voltage	V _{OH}	V _{IN} = V _{IH} or V _{IL}	I _{OH} = -50 μA	2.0	1.9	2.0	—	1.9	—	V
				3.0	2.9	3.0	—	2.9	—	
				4.5	4.4	4.5	—	4.4	—	
Low-level output voltage	V _{OL}	V _{IN} = V _{IH} or V _{IL}	I _{OL} = 50 μA	2.0	—	0.0	0.1	—	0.1	V
				3.0	—	0.0	0.1	—	0.1	
				4.5	—	0.0	0.1	—	0.1	
Low-level output voltage	V _{OL}	V _{IN} = V _{IH} or V _{IL}	I _{OL} = 4 mA	3.0	—	—	0.36	—	0.44	V
				4.5	—	—	0.36	—	0.44	
				I _{OL} = 8 mA	4.5	—	—	0.36	—	
Input leakage current	I _{IN}	V _{IN} = 5.5 or GND		0 to 5.5	—	—	±0.1	—	±1.0	μA
Quiescent supply current	I _{CC}	V _{IN} = V _{CC} or GND		5.5	—	—	4.0	—	40.0	μA

Timing Requirements (input: $t_r = t_f = 3 \text{ ns}$)

Characteristics	Symbol	Test Condition	VCC (V)	Ta = 25°C	Ta = -40 to 85°C	Unit
				Limit	Limit	
Minimum pulse width (CK)	$t_w(L)$ $t_w(H)$	Figure 1	3.3 ± 0.3	5.0	5.0	ns
			5.0 ± 0.5	5.0	5.0	
Minimum pulse width (CLR) (Note 1)	$t_w(L)$	Figure 4	3.3 ± 0.3 5.0 ± 0.5	5.0 5.0	5.0 5.0	ns
Minimum set-up time (A, B, C, D)	t_s	Figure 2	3.3 ± 0.3	5.5	6.5	ns
			5.0 ± 0.5	4.5	4.5	
Minimum set-up time (LOAD)	t_s	Figure 2	3.3 ± 0.3	8.0	9.5	ns
			5.0 ± 0.5	5.0	6.0	
Minimum set-up time (ENT, ENP)	t_s	Figure 3	3.3 ± 0.3	7.5	9.0	ns
			5.0 ± 0.5	5.0	6.0	
Minimum set-up time (CLR) (Note 2)	t_s	Figure 5	3.3 ± 0.3	4.0	4.0	ns
			5.0 ± 0.5	3.5	3.5	
Minimum hold time	t_h	Figure 2, Figure 3	3.3 ± 0.3	1.0	1.0	ns
			5.0 ± 0.5	1.0	1.0	
Minimum hold time (CLR) (Note 2)	t_h	Figure 5	3.3 ± 0.3	1.0	1.0	ns
			5.0 ± 0.5	1.5	1.5	
Minimum removal time (CLR) (Note 1)	t_{rem}	Figure 4	3.3 ± 0.3	2.5	2.5	ns
			5.0 ± 0.5	1.5	1.5	

Note 1: For TC74VHC161 only

Note 2: For TC74VHC163 only

AC Characteristics (input: $t_r = t_f = 3 \text{ ns}$)

Characteristics	Symbol	Test Condition	Ta = 25°C			Ta = -40 to 85°C		Unit		
			VCC (V)	CL (pF)	Min	Typ.	Max		Min	Max
Propagation delay time (CK-Q)	t_{pLH} t_{pHL}	Figure 1, Figure 2	3.3 ± 0.3	15	—	8.3	12.8	1.0	15.0	ns
				50	—	10.8	16.3	1.0	18.5	
			5.0 ± 0.5	15	—	4.9	8.1	1.0	9.5	
				50	—	6.4	10.1	1.0	11.5	
Propagation delay time (CK-CARRY, count-mode)	t_{pLH} t_{pHL}	Figure 1	3.3 ± 0.3	15	—	8.7	13.6	1.0	16.0	ns
				50	—	11.2	17.1	1.0	19.5	
			5.0 ± 0.5	15	—	4.9	8.1	1.0	9.5	
				50	—	6.4	10.1	1.0	11.5	
Propagation delay time (CK-CARRY, preset-mode)	t_{pLH} t_{pHL}	Figure 2	3.3 ± 0.3	15	—	11.0	17.2	1.0	20.0	ns
				50	—	13.5	20.7	1.0	23.5	
			5.0 ± 0.5	15	—	6.2	10.3	1.0	12.0	
				50	—	7.7	12.3	1.0	14.0	
Propagation delay time (ENT-CARRY)	t_{pLH} t_{pHL}	Figure 6	3.3 ± 0.3	15	—	7.5	12.3	1.0	14.5	ns
				50	—	10.5	15.8	1.0	18.0	
			5.0 ± 0.5	15	—	4.9	8.1	1.0	9.5	
				50	—	6.4	10.1	1.0	11.5	
Propagation delay time (CLR-Q) (Note 2)	t_{pHL}	Figure 4	3.3 ± 0.3	15	—	8.9	13.6	1.0	16.0	ns
				50	—	11.2	17.1	1.0	19.5	
			5.0 ± 0.5	15	—	5.5	9.0	1.0	10.5	
				50	—	7.0	11.0	1.0	12.5	
Propagation delay time (CLR-CARRY) (Note 2)	t_{pHL}	Figure 4	3.3 ± 0.3	15	—	8.4	13.2	1.0	15.5	ns
				50	—	10.9	16.7	1.0	19.0	
			5.0 ± 0.5	15	—	5.0	8.6	1.0	10.0	
				50	—	6.5	10.6	1.0	12.0	
Maximum clock frequency	f_{max}	—	3.3 ± 0.3	15	80	130	—	70	—	MHz
				50	55	85	—	50	—	
			5.0 ± 0.5	15	135	185	—	115	—	
				50	95	125	—	85	—	
Input capacitance	C_{IN}	—	—	—	4	10	—	10	pF	
Power dissipation capacitance	C_{PD}	(Note 1)	—	—	23	—	—	—	pF	

Note 1: CPD is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load.

Average operating current can be obtained by the equation:

$$I_{CC(opr)} = CPD \cdot V_{CC} \cdot f_{IN} + I_{CC}$$

When the outputs drive a capacitive load, total current consumption is the sum of CPD, and ΔI_{CC} which is obtained from the following formula:

$$\Delta I_{CC} = f_{CK} \cdot V_{CC} \left(\frac{C_{QA}}{2} + \frac{C_{QB}}{4} + \frac{C_{QC}}{8} + \frac{C_{QD}}{16} + \frac{C_{CO}}{16} \right)$$

CQA to CQD and CCO are the capacitances at QA to QD and CARRY OUT, respectively.
fCK is the input frequency of the CK.

Note 2: For TC74VHC161 only

Switching Characteristics Test Waveform

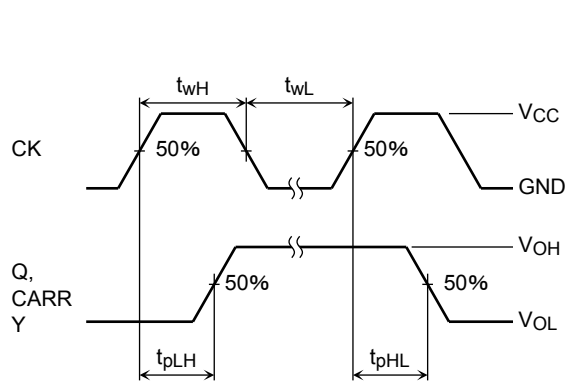


Figure 1 Count Mode

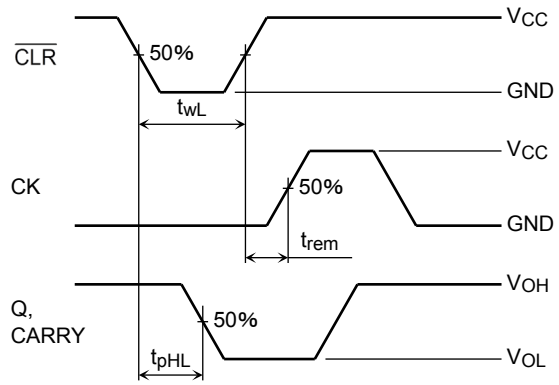


Figure 4 Clear Mode (TC74VHC161)

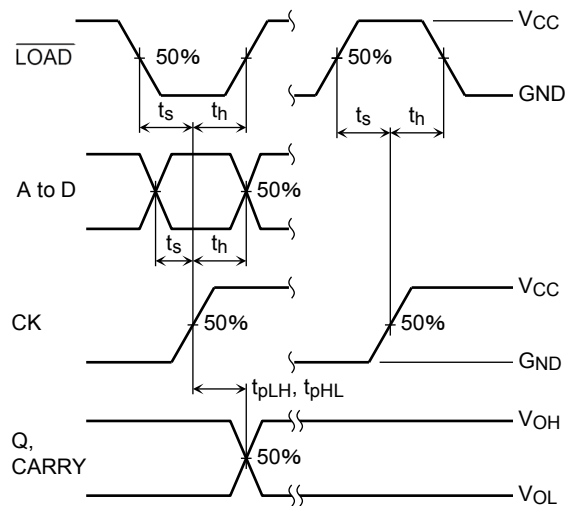


Figure 2 Preset Mode

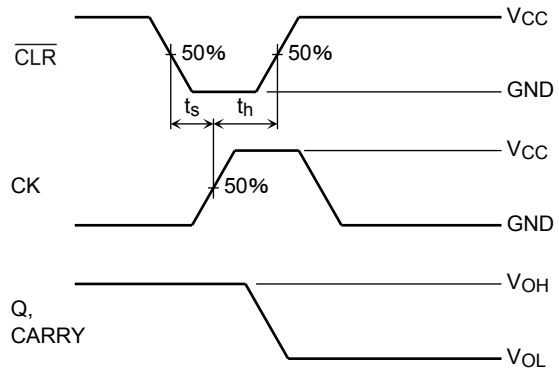


Figure 5 Clear Mode (TC74VHC163)

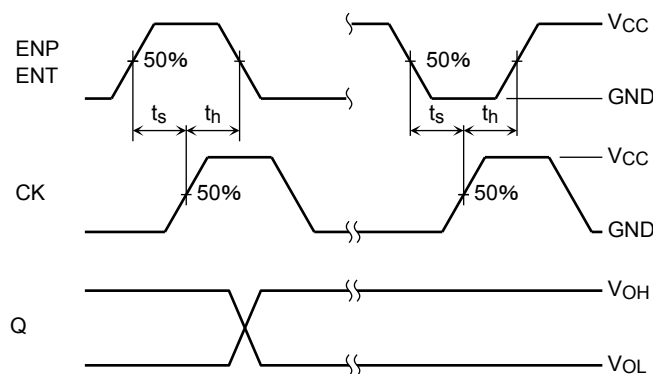


Figure 3 Count Enable Mode

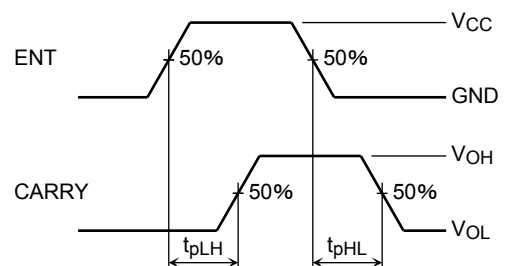
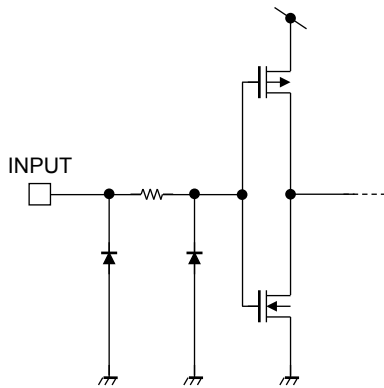


Figure 6 Cascade Mode (fix maximum count)

Noise Characteristics (input: $t_r = t_f = 3$ ns)

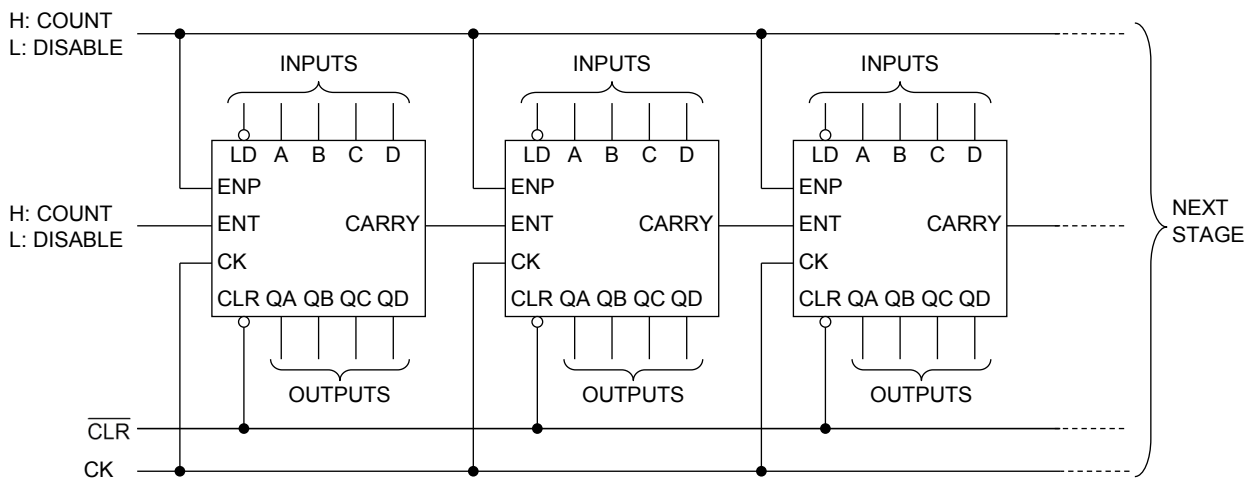
Characteristics	Symbol	Test Condition		Ta = 25°C		Unit
			VCC (V)	Typ.	Max	
Quiet output maximum dynamic V _{OL}	V _{OLP}	C _L = 50 pF	5.0	0.4	0.8	V
Quiet output minimum dynamic V _{OL}	V _{OLV}	C _L = 50 pF	5.0	-0.4	-0.8	V
Minimum high level dynamic input voltage	V _{IHD}	C _L = 50 pF	5.0	—	3.5	V
Maximum low level dynamic input voltage	V _{ILD}	C _L = 50 pF	5.0	—	1.5	V

Input Equivalent Circuit



Typical Application

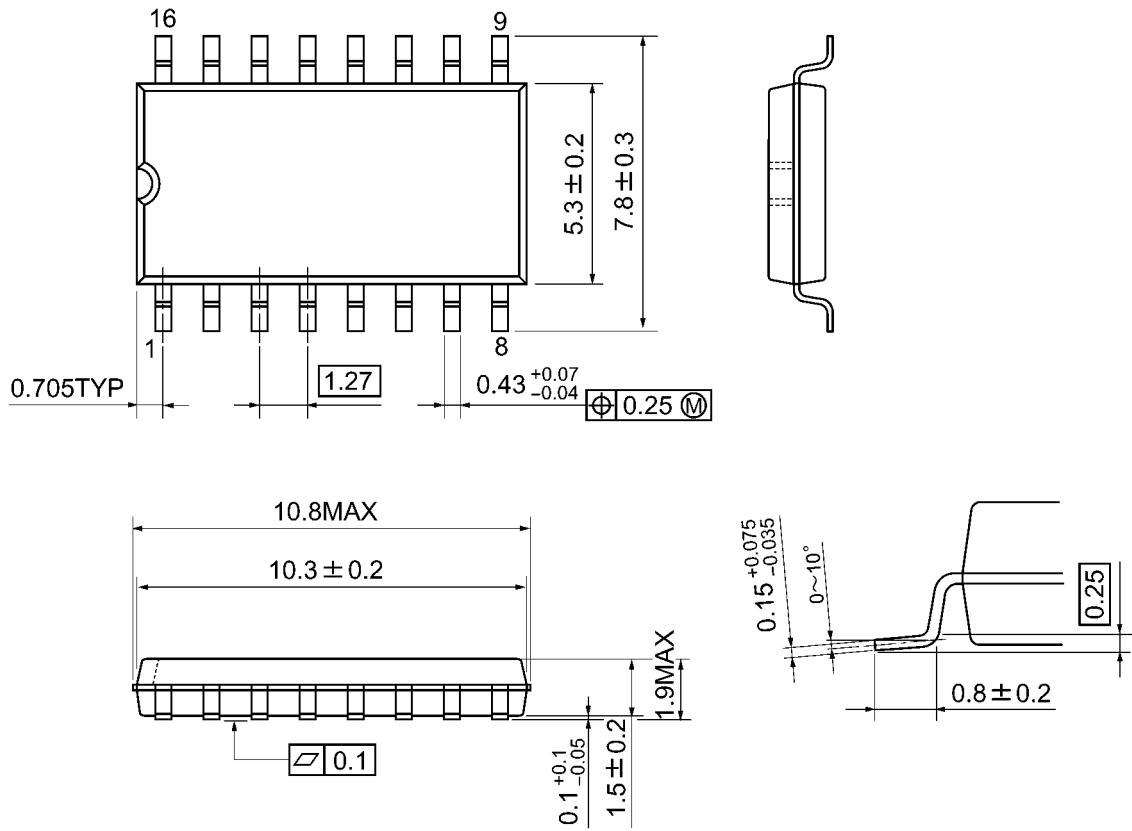
Parallel Carry N-Bit Counter



Package Dimensions

SOP16-P-300-1.27A

Unit: mm

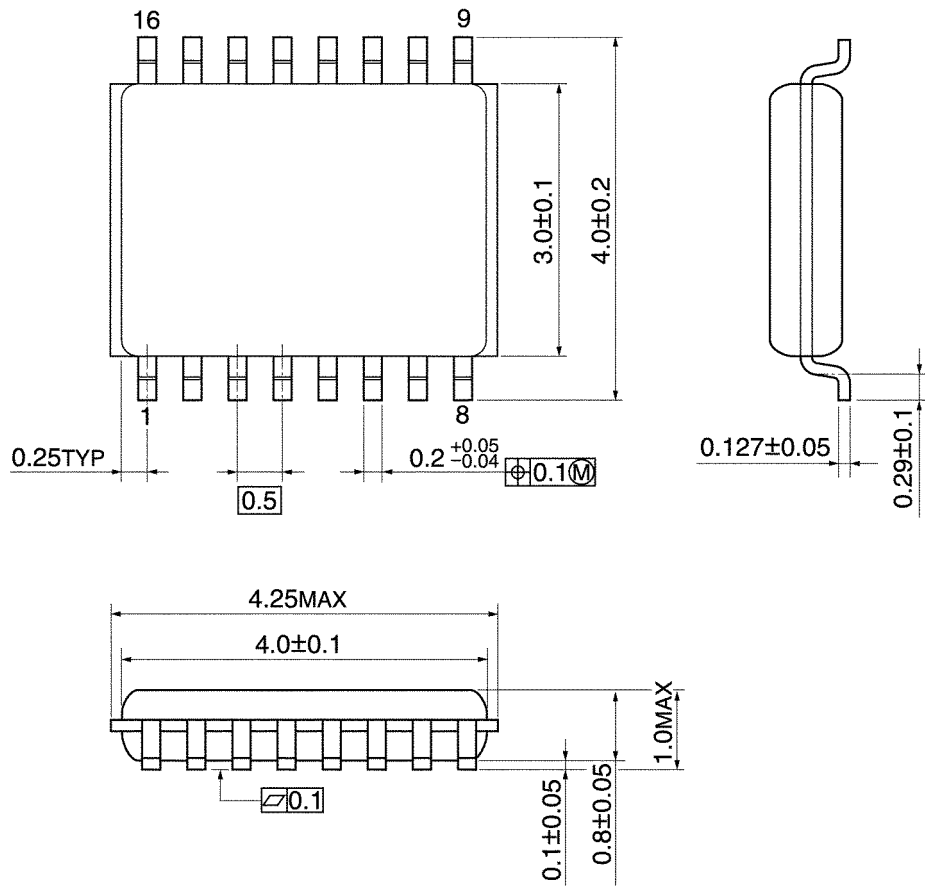


Weight: 0.18 g (typ.)

Package Dimensions

VSSOP16-P-0030-0.50

Unit: mm



Weight: 0.02 g (typ.)

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