THE DATASHEET OF

TAS5622ADDVR

TAS5622A 125-W Stereo and 250-W Stereo PurePath™ HD Digital-Input Class-D Power Stage

1 Features

- PurePath™ HD Integrated Feedback Provides:
  - 0.025% THD at 1 W into 4 Ω
  - > 65-dB PSRR (No Input Signal)
  - > 105 dB (A weighted) SNR
- Preclipping Output for Control of a Class-G Power Supply
- Reduced Heat Sink Size Due to Use of 40mΩ Output MOSFET With > 90% Efficiency at Full Output Power
- Output Power at 10%THD+N
  - 125-W and 4-Ω BTL Stereo Configuration
  - 250-W and 2-Ω PBTL Mono Configuration
- Output Power at 1%THD+N
  - 105-W and 4-Ω BTL Stereo Configuration
  - 210-W and 2-Ω PBTL Mono Configuration
- Click and Pop Free Start-up
- Error Reporting Self-Protected Design With UVP, Overtemperature, and Short-Circuit Protection
- EMI Compliant When Used With Recommended System Design
- 44-Pin HTSSOP (DDV) Package for Reduced Board Size

2 Applications

- Blu-ray™ and DVD Receivers
- High-Power Sound Bars
- Powered Subwoofer and Active Speakers
- Mini Combo Systems

3 Description

The TAS5622A device is a thermally enhanced version of the class-D power amplifier based on the TAS5612A using large MOSFETs for improved power efficiency and a novel gate drive scheme for reduced losses in idle and at low output signals leading to reduced heat sink size.

The unique preclipping output signal can be used to control a class-G power supply. This combined with the low idle loss and high power efficiency of the TAS5622A leads to industry-leading levels of efficiency ensuring a super “green” system.

The TAS5622A uses constant voltage gain. The internally matched gain resistors ensure a high Power Supply Rejection Ratio giving an output voltage only dependent on the audio input voltage and free from any power supply artifacts.

The high integration of the TAS5622A makes the amplifier easy to use; and, using TI’s reference schematics and PCB layouts leads to fast design in time. The TAS5622A is available in the space-saving, surface-mount, 44-pin HTSSOP package.

Device Information(1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
TAS5622A	HTSSOP (44)	14.00 mm × 6.10 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Typical TAS5622A Application Block Diagram

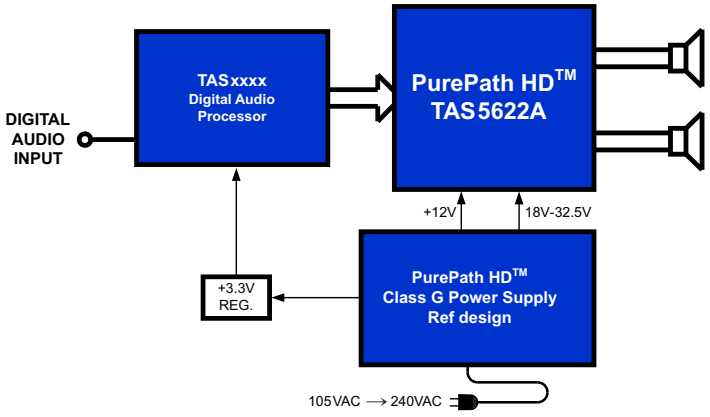


Table of Contents

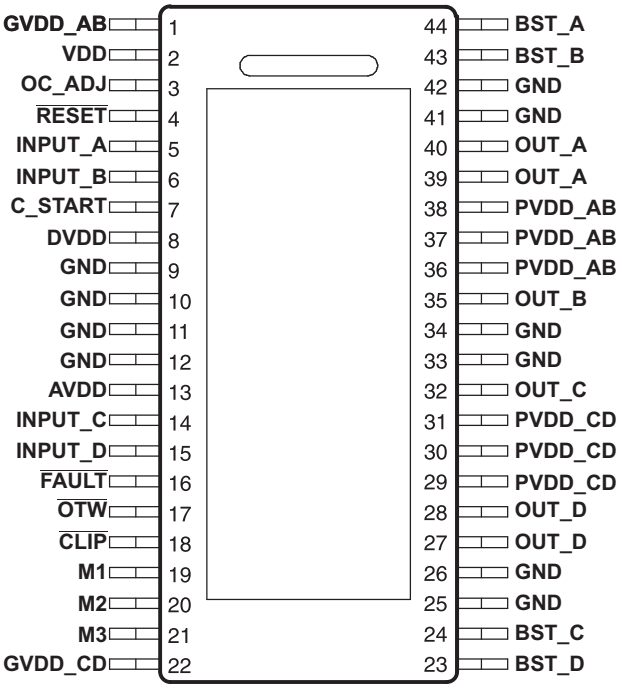
4 Revision History

Changes from Original (May 2012) to Revision A **Page**

- Added *Pin Configuration and Functions* section, *ESD Ratings* table, *Feature Description* section, *Device Functional Modes*, *Application and Implementation* section, *Power Supply Recommendations* section, *Layout* section, *Device and Documentation Support* section, and *Mechanical, Packaging, and Orderable Information* section ... 1

5 Pin Configuration and Functions

DDV Package
44-Pin HTSSOP
Top View



Pin Functions

PIN		I/O/P[1]	DESCRIPTION
NAME	NO.		
AVDD	13	P	Internal voltage regulator, analog section
BST_A	44	P	Bootstrap pin, A-side
BST_B	43	P	Bootstrap pin, B-side
BST_C	24	P	Bootstrap pin, C-side
BST_D	23	P	Bootstrap pin, D-side
$\overline{\text{CLIP}}$	18	O	Clipping warning; open drain; active low
C_START	7	O	Start-up ramp
DVDD	8	P	Internal voltage regulator, digital section
$\overline{\text{FAULT}}$	16	O	Shutdown signal, open drain; active low
GND	9, 10, 11, 12, 25, 26, 33, 34, 41, 42	P	Ground
GVDD_AB	1	P	Gate-drive voltage supply; AB-side
GVDD_CD	22	P	Gate-drive voltage supply; CD-side
INPUT_A	5	I	PWM Input signal for half-bridge A
INPUT_B	6	I	PWM Input signal for half-bridge B
INPUT_C	14	I	PWM Input signal for half-bridge C
INPUT_D	15	I	PWM Input signal for half-bridge D
M1	19	I	Mode selection 1 (LSB)
M2	20	I	Mode selection 2
M3	21	I	Mode selection 3 (MSB)
OC_ADJ	3	O	Over-Current threshold programming pin

(1) I = Input, O = Output, P = Power

Pin Functions (continued)

PIN		I/O/P[1]	DESCRIPTION
NAME	NO.		
$\overline{\text{OTW}}$	17	O	Over-temperature warning; open drain; active low
OUT_A	39, 40	O	Output, half-bridge A
OUT_B	35	O	Output, half-bridge B
OUT_C	32	O	Output, half-bridge C
OUT_D	27, 28	O	Output, half-bridge D
PVDD_AB	36, 37, 38	P	PVDD supply for half-bridge A and B
PVDD_CD	29, 30, 31	P	PVDD supply for half-bridge C and D
$\overline{\text{RESET}}$	4	I	Device reset Input; active low
VDD	2	P	Input power supply
PowerPAD™	–	P	Ground, connect to grounded heat sink

Mode Selection Pins

MODE PINS			PWM INPUT[1]	OUTPUT CONFIGURATION	INPUT A	INPUT B	INPUT C	INPUT D	MODE
M3	M2	M1							
0	0	0	2N + 1	2 x BTL	PWMa	PWMb	PWMc	PWMd	AD mode
0	0	1	1N + 1[2]	2 x BTL	PWMa	Unused	PWMc	Unused	AD mode
0	1	0	2N + 1	2 x BTL	PWMa	PWMb	PWMc	PWMd	BD mode
0	1	1	1N + 1[2]	1 x BTL + 2 x SE	PWMa	Unused	PWMc	PWMd	AD mode
1	0	0	2N + 1	1 x PBTL	PWMa	PWMb	0	0	AD mode
1	0	0	1N + 1[2]	1 x PBTL	PWMa	Unused	0	1	AD mode
1	0	0	2N + 1	1 x PBTL	PWMa	PWMb	1	0	BD mode
1	0	1	1N + 1	4 x SE[3]	PWMa	PWMb	PWMc	PWMd	AD mode

(1) The 1N and 2N naming convention is used to indicate the number of PWM lines to the power stage per channel in a specific mode.
(2) Using 1N interface in BTL and PBTL mode results in increased DC offset on the output terminals.
(3) The 4xSE mode can be used as 1xBTL + 2xSE configuration by feeding a 2N PWM signal to either INPUT_AB or INPUT_CD for improved DC offset accuracy

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range unless otherwise noted (1)

	MIN	MAX	UNIT
VDD to GND, GVDD_X(2) to GND	–0.3	13.2	V
PVDD_X(2) to GND(3), OUT_X to GND(3), BST_X to GVDD_X(2)(3)	–0.3	50	V
BST_X to GND(3)(4)	–0.3	62.5	V
DVDD to GND	–0.3	4.2	V
AVDD to GND	–0.3	8.5	V
OC_ADJ, M1, M2, M3, C_START, INPUT_X to GND	–0.3	4.2	V
$\overline{\text{RESET}}$, $\overline{\text{FAULT}}$, $\overline{\text{OTW}}$, $\overline{\text{CLIP}}$, to GND	–0.3	4.2	V
Maximum continuous sink current ($\overline{\text{FAULT}}$, $\overline{\text{OTW}}$, $\overline{\text{CLIP}}$)		9	mA
Maximum operating junction temperature, T_J	0	150	°C
Lead temperature		260	°C
Storage temperature, T_{stg}	–40	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) GVDD_X and PVDD_X represents a full bridge gate drive or power supply. GVDD_X is GVDD_AB or GVDD_CD, PVDD_X is PVDD_AB or PVDD_CD
(3) These voltages represents the DC voltage + peak AC waveform measured at the terminal of the device in all conditions.
(4) Maximum BST_X to GND voltage is the sum of maximum PVDD to GND and GVDD to GND voltages minus a diode drop.

6.2 ESD Ratings

		VALUE	UNIT
$V_{(ESD)}$ Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±2000	V
	Charged-device model (CDM), per JEDEC specification JESD22-C101(2)	±500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

				MIN	NOM	MAX	UNIT
PVDD_X	Full-bridge supply		DC supply voltage	12	32.5	34	V
GVDD_X	Supply for logic regulators and gate-drive circuitry		DC supply voltage	10.8	12	13.2	V
VDD	Digital regulator supply voltage		DC supply voltage	10.8	12	13.2	V
R_L	Load impedance	BTL	Output filter: L = 10 uH, 1 µF. Output AD modulation, switching frequency > 350 kHz.	2.5	4.0		Ω
		SE		1.5	3.0		
		PBTL		1.5	2.0		
L_{OUTPUT}	Output filter inductance		Minimum inductance at overcurrent limit, including inductor tolerance, temperature and possible inductor saturation	5			µH
F_{PWM}	PWM frame rate			352	384	500	kHz
C_{PVDD}	PVDD close decoupling capacitors			0.44	1		µF
C_START	Start-up ramp capacitor		BTL and PBTL configuration		100		nF
			SE and 1xBTL+2xSE configuration		1		µF
R_{OC}	Overcurrent programming resistor		Resistor tolerance = 5%	24		33	kΩ
$R_{OC\_LATCHED}$	Overcurrent programming resistor		Resistor tolerance = 5%	47	62	68	kΩ
T_J	Junction temperature			0		125	°C

6.4 Thermal Information

THERMAL METRIC[1]		TAS5622A DDV (HTSSOP) 44 PINS	UNIT
$R_{\theta JH}$	Junction-to-heat sink thermal resistance	1.9	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	0.6	
$R_{\theta JB}$	Junction-to-board thermal resistance	1.7	
ψ_{JT}	Junction-to-top characterization parameter	0.6	
ψ_{JB}	Junction-to-board characterization parameter	1.7	

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, SPRA953.

6.5 Electrical Characteristics

PVDD_X = 32.5 V, GVDD_X = 12 V, VDD = 12 V, T_C (Case temperature) = 75°C, f_S = 384 kHz, unless otherwise specified.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
INTERNAL VOLTAGE REGULATOR AND CURRENT CONSUMPTION						
DVDD	Voltage regulator, only used as a reference node	VDD = 12 V	3.0	3.3	3.6	V
AVDD	Voltage regulator, only used as a reference node	VDD = 12 V		7.8		V
I_{VDD}	VDD supply current	Operating, 50% duty cycle		20		mA
		Idle, reset mode		20		
I_{GVDD_X}	Gate-supply current per full-bridge	50% duty cycle		12		mA
		Reset mode		3		
I_{PVDD_X}	Full-bridge idle current	50% duty cycle without load		12		mA
		$\overline{RESET}$ low		1.7		
		VDD and GVDD_X at 0V		0.35		
OUTPUT-STAGE MOSFETs						
$R_{DS(on),\ LS}$	Drain-to-source resistance, low side (LS)	T_J = 25°C, excludes metallization resistance, GVDD = 12 V		40		mΩ
$R_{DS(on),\ HS}$	Drain-to-source resistance, high side (HS)			40		mΩ
I/O PROTECTION						
$V_{uvp,GVDD}$	Undervoltage protection limit, GVDD_X			8.5		V
$V_{uvp,GVDD,\ hyst}$ (1)				0.7		V
$V_{uvp,VDD}$	Undervoltage protection limit, VDD			8.5		V
$V_{uvp,VDD,\ hyst}$ (1)				0.7		V
$V_{uvp,PVDD}$	Undervoltage protection limit, PVDD_X			8.5		V
$V_{uvp,PVDD,hyst}$ (1)				0.7		V
OTW (1)	Overtemperature warning		115	125	135	°C
OTW_{hyst} (1)	Temperature drop needed below OTW temperature for $\overline{OTW}$ to be inactive after $\overline{OTW}$ event.			25		°C
OTE (1)	Overtemperature error		145	155	165	°C
$OTE\text{-}OTW_{differential}$ (1)	OTE-OTW differential			30		°C
OTE_{HYST} (1)	A device reset is needed to clear $\overline{FAULT}$ after an OTE event			25		°C
OLPC	Overload protection counter	f_{PWM} = 384 kHz		2.6		ms
I_{OC}	Overcurrent limit protection	Resistor – programmable, nominal peak current in 1Ω load, ROC = 24 kΩ		15		A
$I_{OC\_LATCHED}$	Overcurrent limit protection, latched	Resistor – programmable, nominal peak current in 1Ω load, ROC = 62 kΩ		15		A
I_{OCT}	Overcurrent response time	Time from application of short condition to Hi-Z of affected half bridge		150		ns
I_{PD}	Internal pulldown resistor at output of each half bridge	Connected when $\overline{RESET}$ is active to provide bootstrap charge. Not used in SE mode.		3		mA
STATIC DIGITAL SPECIFICATIONS						
V_{IH}	High level input voltage	INPUT_X, M1, M2, M3, $\overline{RESET}$	1.9			V
V_{IL}	Low level input voltage				0.8	V
LEAKAGE	Input leakage current				100	µA
OTW / SHUTDOWN (FAULT)						
R_{INT_PU}	Internal pullup resistance, $\overline{OTW}$, $\overline{CLIP}$, $\overline{FAULT}$ to DVDD		20	26	33	kΩ
V_{OH}	High level output voltage	Internal pullup resistor	3	3.3	3.6	V
V_{OL}	Low level output voltage	I_O = 4mA		200	500	mV
FANOUT	Device fanout $\overline{OTW}$, $\overline{FAULT}$, $\overline{CLIP}$	No external pullup		30		devices

(1) Specified by design.

6.6 Audio Specification Stereo (BTL)

Audio performance is recorded as a chipset consisting of a TASxxxx PWM Processor (modulation index limited to 97.7%) and a TAS5622A power stage with PCB and system configurations in accordance with recommended guidelines. Audio frequency = 1 kHz, PVDD_X = 32.5 V, GVDD_X = 12 V, R_L = 4 Ω, f_S = 384 kHz, R_{OC} = 24 kΩ, T_C = 75°C,Output Filter: L_{DEM} = 10 µH, C_{DEM} = 1 µF, unless otherwise noted.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
P_O	Power output per channel	R_L = 3 Ω, 10% THD+N		150		W
		R_L = 4 Ω, 10% THD+N		125		
		R_L = 3 Ω, 1% THD+N		140		
		R_L = 4 Ω, 1% THD+N		105		
THD+N	Total harmonic distortion + noise	1 W, 1 kHz signal		0.025%		
V_n	Output integrated noise	A-weighted, AES17 measuring filter		180		µV
V_{OS}	Output offset voltage	No signal		10	20	mV
SNR	Signal-to-noise ratio(1)	A-weighted, AES17 measuring filter		105		dB
DNR	Dynamic range	A-weighted, –60 dBFS (rel 1% THD+N)		105		dB
P_{idle}	Power dissipation due to Idle losses (IPVDD_X)	P_O = 0, channels switching(2)		0.8		W

(1) SNR is calculated relative to 1% THD-N output level.
(2) Actual system idle losses also are affected by core losses of output inductors.

6.7 Audio Specification 4 Channels (SE)

Audio performance is recorded as a chipset consisting of a TASxxxx PWM Processor (modulation index limited to 97.7%) and a TAS5622A power stage with PCB and system configurations in accordance with recommended guidelines. Audio frequency = 1 kHz, PVDD_X = 32.5 V, GVDD_X = 12 V, R_L = 4 Ω, f_S = 384 kHz, R_{OC} = 24 kΩ, T_C = 75°C,Output Filter: L_{DEM} = 10 µH, C_{DEM} = 1 µF, C_{DCB} = 470 µF, unless otherwise noted.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
P_O	Power output per channel	R_L = 3 Ω, 10% THD+N		43		W
		R_L = 3 Ω, 1% THD+N		35		
THD+N	Total harmonic distortion + noise	1 W, 1 kHz signal		0.025%		
V_n	Output integrated noise	A-weighted, AES17 measuring filter		180		µV
SNR	Signal-to-noise ratio(1)	A-weighted, AES17 measuring filter		102		dB
DNR	Dynamic range	A-weighted, –60 dBFS (rel 1% THD+N)		102		dB
P_{idle}	Power dissipation due to Idle losses (IPVDD_X)	P_O = 0, channels switching(2)		0.8		W

(1) SNR is calculated relative to 1% THD-N output level.
(2) Actual system idle losses also are affected by core losses of output inductors.

6.8 Audio Specification Mono (PBTL)

Audio performance is recorded as a chipset consisting of a TASxxxx PWM Processor (modulation index limited to 97.7%) and a TAS5622A power stage with PCB and system configurations in accordance with recommended guidelines. Audio frequency = 1 kHz, PVDD_X = 32.5 V, GVDD_X = 12 V, R_L = 4 Ω, f_S = 384 kHz, R_{OC} = 24 kΩ, T_C = 75°C, Output Filter: L_{DEM} = 10 µH, C_{DEM} = 1 µF, unless otherwise noted.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
P_O	Power output per channel	R_L = 1.5 Ω, 10%, THD+N		330		W
		R_L = 2 Ω, 10% THD+N		250		
		R_L = 4 Ω, 10% THD+N		130		
		R_L = 1.5 Ω, 1% THD+N		270		
		R_L = 2 Ω, 1% THD+N		210		
		R_L = 4 Ω, 1% THD+N		105		
THD+N	Total harmonic distortion + noise	1 W, 1 kHz signal		0.025%		
V_n	Output integrated noise	A-weighted, AES17 measuring filter		180		µV
V_{OS}	Output offset voltage	No signal		10	20	mV
SNR	Signal to noise ratio(1)	A-weighted, AES17 measuring filter		105		dB
DNR	Dynamic range	A-weighted, –60 dBFS (rel 1% THD)		105		dB
P_{idle}	Power dissipation due to idle losses (IPVDD_X)	P_O = 0, All channels switching(2)		0.8		W

(1) SNR is calculated relative to 1% THD-N output level.
(2) Actual system idle losses are affected by core losses of output inductors.

6.9 Typical Characteristics

6.9.1 Typical Characteristics, BTL Configuration

Measurement conditions are: 1 kHz, PVDD_X = 32.5 V, GVDD_X = 12 V, R_L = 4 Ω, f_S = 384 kHz, R_{OC} = 24 kΩ, T_C = 75°C, Output Filter: L_{DEM} = 10 µH, C_{DEM} = 1 µF, 20 Hz to 20 kHz BW (AES17 low pass filter), unless otherwise noted.

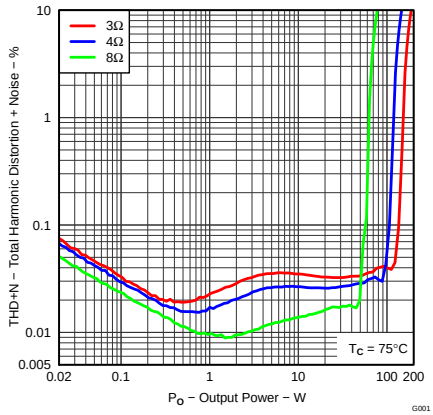


Figure 1. Total Harmonic + Noise vs Output Power, 1 kHz

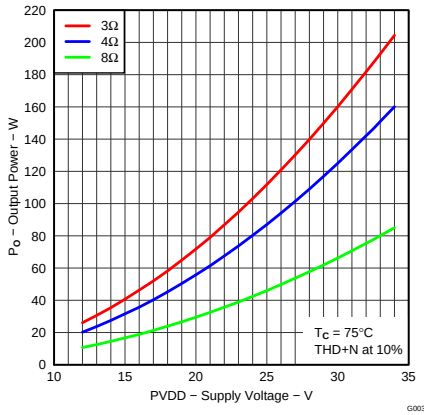


Figure 2. Output Power vs Supply Voltage vs Distortion + Noise = 10%

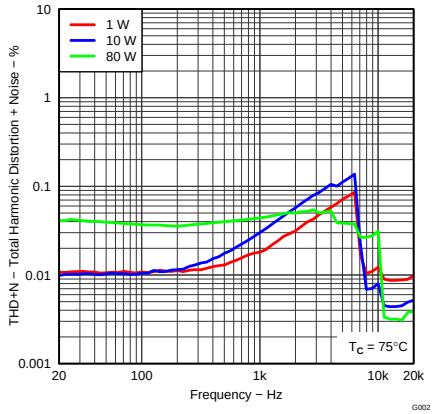


Figure 3. Total Harmonic Distortion + Noise vs Frequency, 4 Ω

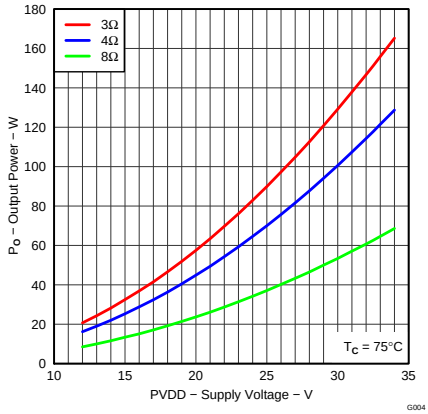


Figure 4. Output Power vs Supply Voltage, vs Distortion + Noise = 1%

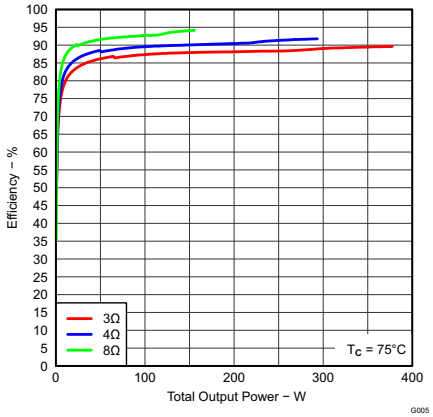


Figure 5. System Efficiency vs Output Power

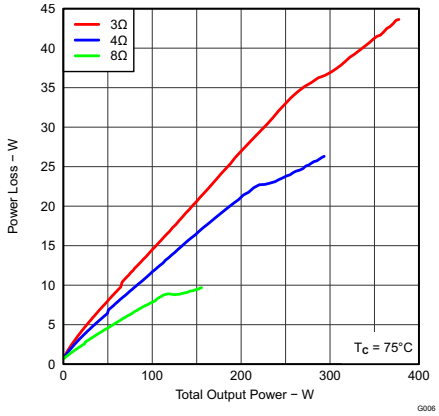


Figure 6. System Power Loss vs Output Power

Typical Characteristics, BTL Configuration (continued)

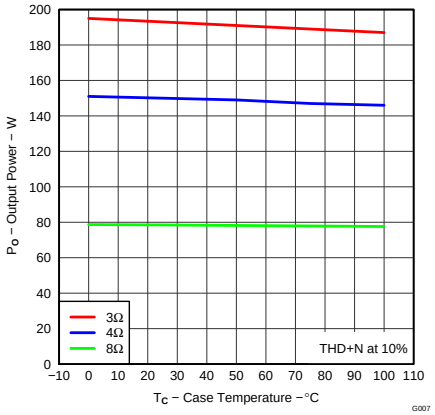


Figure 7. Output Power vs Temperature

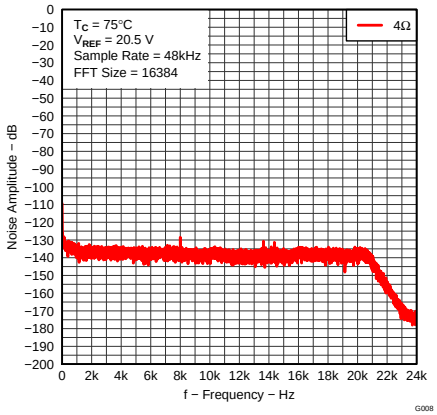


Figure 8. Noise Amplitude vs Frequency

6.9.2 Typical Characteristics, SE Configuration

Measurement conditions are: 1 kHz, PVDD_X = 32.5 V, GVDD_X = 12 V, R_L = 4 Ω, f_S = 384 kHz, R_{OC} = 24 kΩ, T_C = 75°C, Output Filter: L_{DEM} = 10 µH, C_{DEM} = 1 µF, C_{DCB} = 470 µF, 20 Hz to 20 kHz BW (AES17 low pass filter), unless otherwise noted.

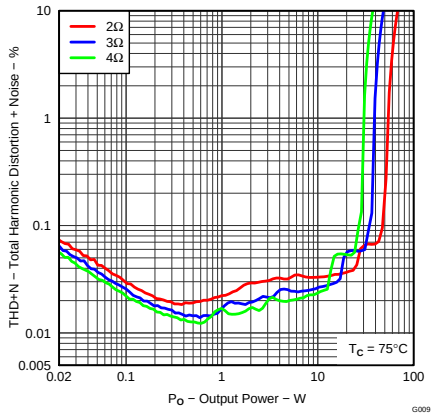


Figure 9. Total Harmonic Distortion + Noise vs Output Power

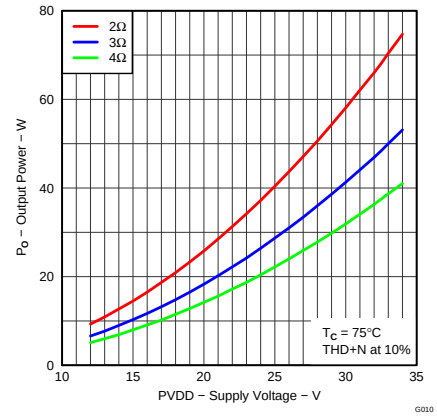


Figure 10. Output Power vs Supply Voltage

6.9.3 Typical Characteristics, PBTL Configuration

Measurement conditions are: 1 kHz, PVDD_X = 32.5 V, GVDD_X = 12 V, R_L = 4 Ω, f_S = 384 kHz, R_{OC} = 24 kΩ, T_C = 75°C, Output Filter: L_{DEM} = 10 µH, C_{DEM} = 1 µF, 20 Hz to 20 kHz BW (AES17 low pass filter), unless otherwise noted.

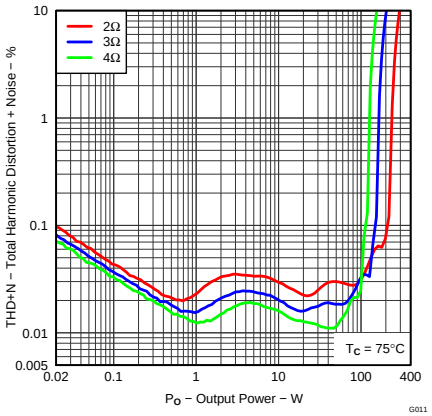


Figure 11. Total Harmonic Distortion + Noise vs Output Power

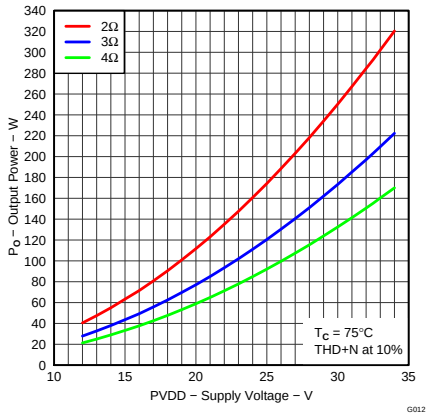


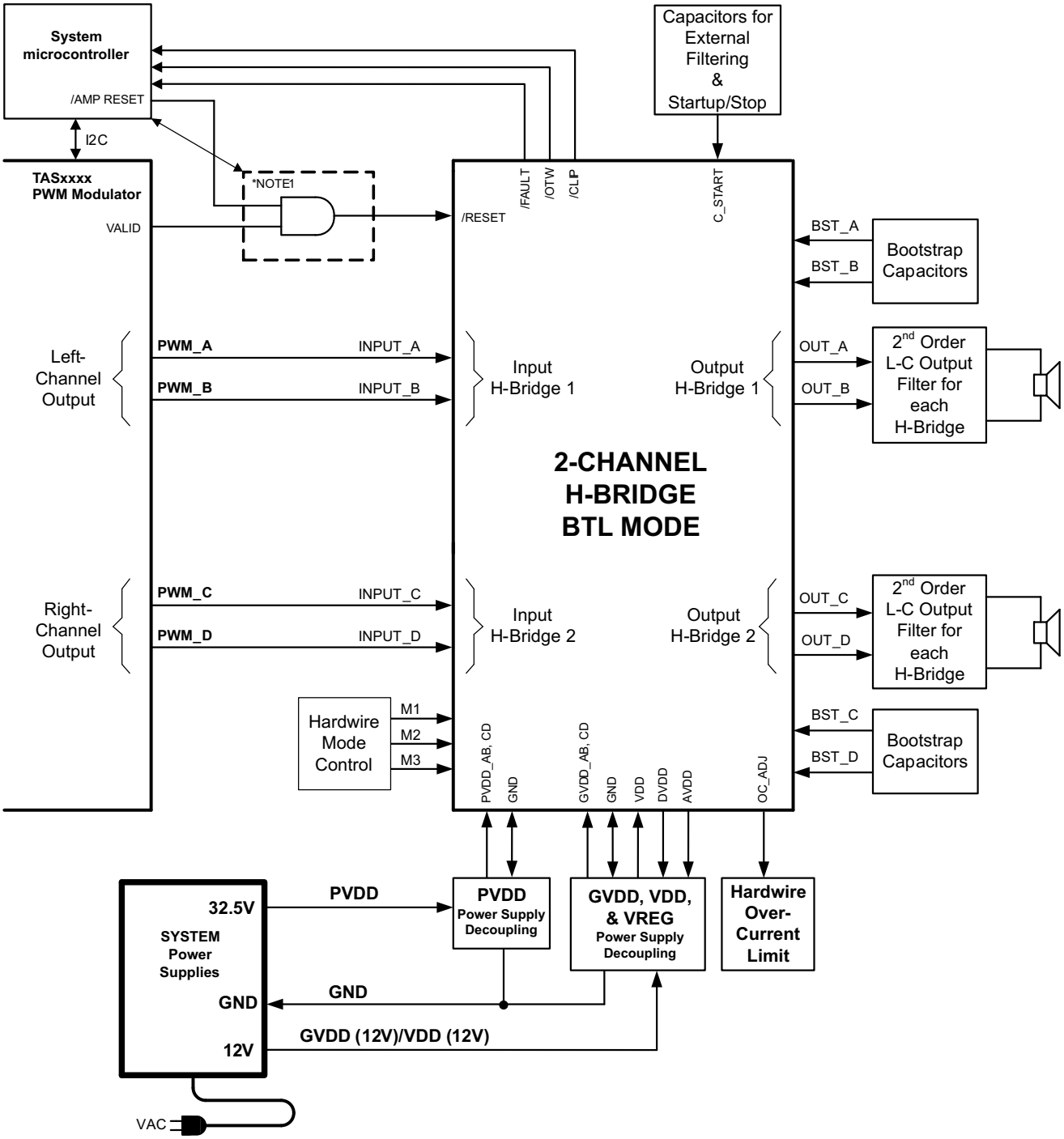
Figure 12. Output Power vs Supply Voltage

7 Detailed Description

7.1 Overview

TAS5622A is a PWM input, audio PWM (class-D) amplifier. The output of the TAS5622A can be configured for single-ended, BTL (Bridge-Tied Load) or parallel BTL (PBTL) output. It requires two rails for power supply, PVDD and 12 V (GVDD and VDD). The following block diagram shows typical connections for BTL outputs. Detailed schematic can be viewed in *TAS5622A EVM User's Guide* (SLAU376).

7.2 Functional Block Diagrams



(1) Logic AND is inside or outside the microprocessor.

Figure 13. Typical System Block Diagram

Functional Block Diagrams (continued)

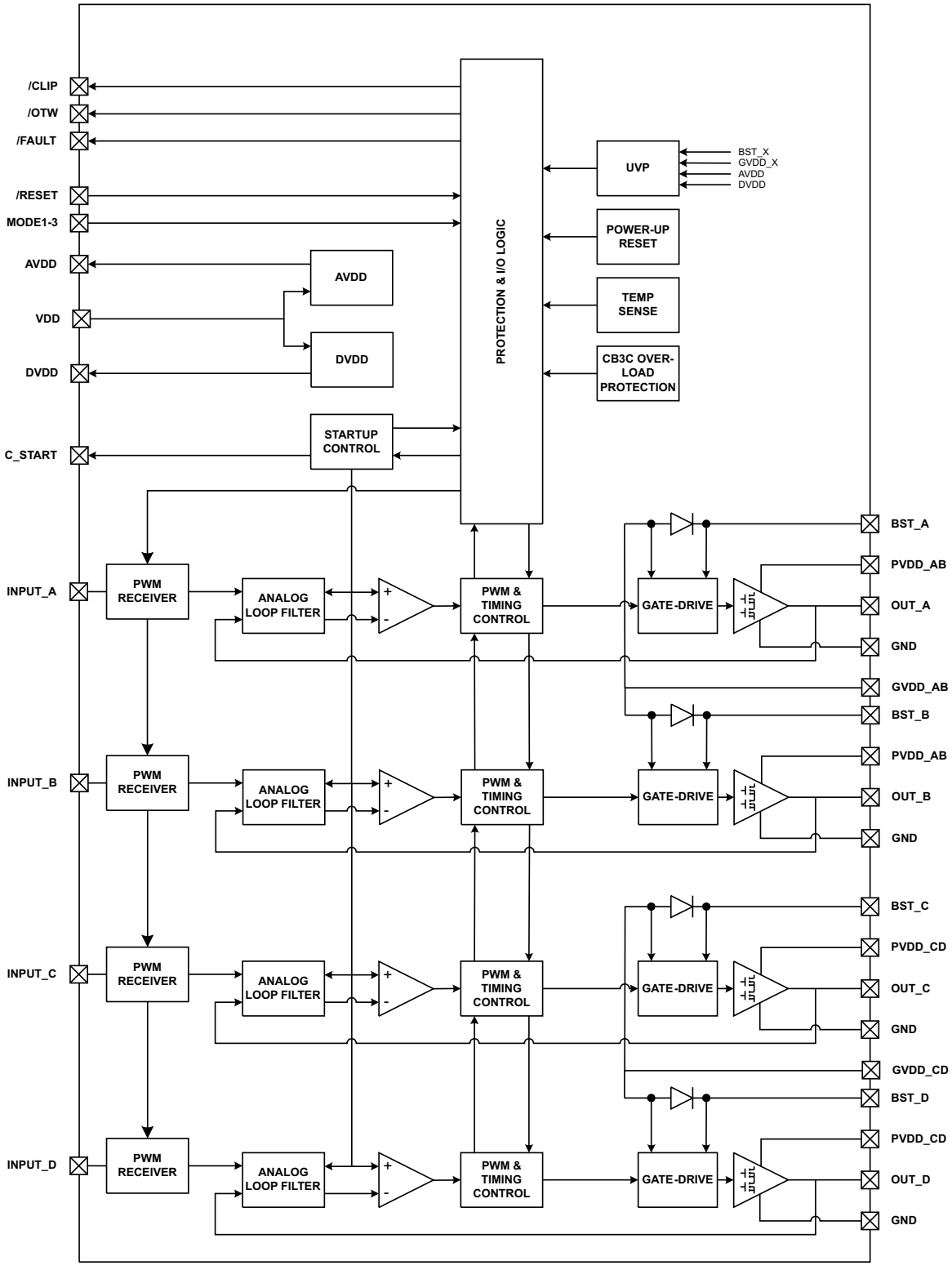


Figure 14. Functional Block Diagram

7.3 Feature Description

7.3.1 System Power-Up and Power-Down Sequence

7.3.1.1 Powering Up

The TAS5622A does not require a power-up sequence. The outputs of the H-bridges remain in a high-impedance state until the gate-drive supply voltage (GVDD_X) and VDD voltage are above the undervoltage protection (UVP) voltage threshold (see *Electrical Characteristics*). Although not specifically required, it is recommended to hold RESET in a low state while powering up the device. This allows an internal circuit to charge the external bootstrap capacitors by enabling a weak pulldown of the half-bridge output.

7.3.1.2 Powering Down

The TAS5622A does not require a power-down sequence. The device remains fully operational as long as the gate-drive supply (GVDD_X) voltage and VDD voltage are above the undervoltage protection (UVP) voltage threshold (see *Electrical Characteristics*). Although not specifically required, it is a good practice to hold RESET low during power down, thus preventing audible artifacts including pops or clicks.

7.3.2 Start-up and Shutdown Ramp Sequence

The integrated start-up and stop sequence ensures a click and pop free startup and shutdown sequence of the amplifier. The start-up sequence uses a voltage ramp with a duration set by the CSTART capacitor. The sequence uses the input PWM signals to generate output PWM signals, hence input idle PWM should be present during both start-up and shut down ramping sequences.

VDD, GVDD_X and PVDD_X power supplies must be turned on and with settled outputs before starting the start-up ramp by setting RESET high.

During start-up and shutdown ramp the input PWM signals should be in muted condition with the PWM processor noise shaper activity turned off (50% duty cycle).

The duration of the start-up and shutdown ramp is 100 ms + X ms, where X is the CSTART capacitor value in nF.

It is recommended to use 100nF CSTART in BTL and PBTL mode and 1 µF in SE mode configuration. This results in ramp times of 200 ms and 1.1s respectively. The longer ramp time in SE configuration allows charge and discharge of the output AC coupling capacitor without audible artifacts.

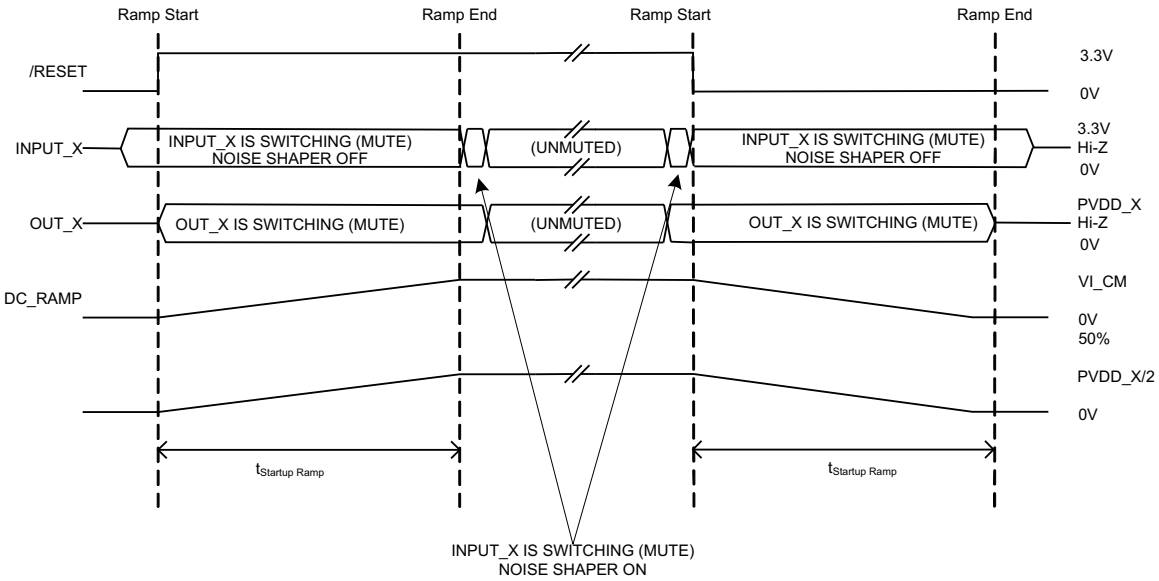


Figure 15. Start-up/Shutdown Ramp

Feature Description (continued)

7.3.3 Unused Output Channels

If all available output channels are not used, it is recommended to disable switching of unused output nodes to reduce power consumption. Furthermore by disabling unused output channels the cost of unused output LC demodulation filters can be avoided.

Disabling a channel is done by leave the bootstrap capacitor (BST) unstuffed and connecting the respective input to GND. The unused output pin(s) can be left floating. Please note that the PVDD decoupling capacitors still need to be mounted.

Table 1. Unused Output Channels

Operating Mode	PWM Input	Output Configuration	Unused Channel	INPUT_A	INPUT_B	INPUT_C	INPUT_D	Unstuffed Component
000	2N + 1	2 x BTL	AB CD	GND PWMa	GND PWMb	PWMc GND	PWMd GND	BST_A & BST_B capacitor BST_C & BST_D capacitor
001	1N + 1							
010	2N + 1							
101	1N + 1	4 x SE	A	GND	PWMb	PWMc	PWMd	BST_A capacitor
			B	PWMa	GND	PWMc	PWMd	BST_B capacitor
			C	PWMa	PWMb	GND	PWMd	BST_C capacitor
			D	PWMa	PWMb	PWMc	GND	BST_D capacitor

7.3.4 Device Protection System

The TAS5622A contains advanced protection circuitry carefully designed to facilitate system integration and ease of use, as well as to safeguard the device from permanent failure due to a wide range of fault conditions such as short circuits, overload, overtemperature, and undervoltage. The TAS5622A responds to a fault by immediately setting the power stage in a high-impedance (Hi-Z) state and asserting the $\overline{\text{FAULT}}$ pin low. In situations other than overload and overtemperature error (OTE), the device automatically recovers when the fault condition has been removed, that is, the supply voltage has increased.

The device will function on errors, as shown in the following table.

Table 2. Device Protection

BTL Mode		PBTL Mode		SE Mode	
Channel Fault	Turns Off	Channel Fault	Turns Off	Channel Fault	Turns Off
A	A+B	A	A+B+C+D	A	A+B
B		B		B	
C	C+D	C		C	C+D
D		D		D	

Bootstrap UVP does not shutdown according to the table, it shuts down the respective high-side FET.

7.3.5 Pin-to-Pin Short Circuit Protection (PPSC)

The PPSC detection system protects the device from permanent damage if a power output pin (OUT_X) is shorted to GND or PVDD_X. For comparison, the OC protection system detects an overcurrent after the demodulation filter where PPSC detects shorts directly at the pin before the filter. PPSC detection is performed at start-up, that is, when VDD is supplied, consequently a short to either GND or PVDD_X after system start-up will not activate the PPSC detection system. When PPSC detection is activated by a short on the output, all half bridges are kept in a Hi-Z state until the short is removed, the device then continues the start-up sequence and starts switching. The detection is controlled globally by a two step sequence. The first step ensures that there are no shorts from OUT_X to GND, the second step tests that there are no shorts from OUT_X to PVDD_X. The total duration of this process is roughly proportional to the capacitance of the output LC filter. The typical duration is <15 ms/µF. While the PPSC detection is in progress, $\overline{\text{FAULT}}$ is kept low, and the device will not react to changes applied to the $\overline{\text{RESET}}$ pins. If no shorts are present the PPSC detection passes, and $\overline{\text{FAULT}}$ is released. A device reset will not start a new PPSC detection. PPSC detection is enabled in BTL and PBTL output configurations, the detection is not performed in SE mode. To make sure not to trip the PPSC detection system it is recommended not to insert resistive load to GND or PVDD_X.

7.3.6 Overtemperature Protection

The TAS5622A has a two-level temperature-protection system that asserts an active-low warning signal ($\overline{\text{OTW}}$) when the device junction temperature exceeds 125°C (typical). If the device junction temperature exceeds 155°C (typical) the device is put into thermal shutdown, resulting in all half-bridge outputs being set in the high-impedance (Hi-Z) state and $\overline{\text{FAULT}}$ being asserted low. OTE is latched in this case. To clear the OTE latch, $\overline{\text{RESET}}$ must be asserted. Thereafter, the device resumes normal operation.

7.3.7 Overtemperature Warning, $\overline{\text{OTW}}$

The over temperature warning $\overline{\text{OTW}}$ asserts when the junction temperature has exceeded recommended operating temperature. Operation at junction temperatures above $\overline{\text{OTW}}$ threshold is exceeding recommended operation conditions and is strongly advised to avoid.

If $\overline{\text{OTW}}$ asserts, action should be taken to reduce power dissipation to allow junction temperature to decrease until it gets below the $\overline{\text{OTW}}$ hysteresis threshold. This action can be decreasing audio volume or turning on a system cooling fan.

7.3.8 Undervoltage Protection (UVP) and Power-On Reset (POR)

The UVP and POR circuits of the TAS5622A fully protect the device in any power-up/down and brownout situation. While powering up, the POR circuit resets the overload circuit (OLP) and ensures that all circuits are fully operational when the GVDD_X and VDD supply voltages reach stated in the *Electrical Characteristics* table. Although GVDD_X and VDD are independently monitored, a supply voltage drop below the UVP threshold on any VDD or GVDD_X pin results in all half-bridge outputs immediately being set in the high-impedance (Hi-Z) state and $\overline{\text{FAULT}}$ being asserted low. The device automatically resumes operation when all supply voltages have increased above the UVP threshold.

7.3.9 Error Reporting

Note that asserting $\overline{\text{RESET}}$ low forces the $\overline{\text{FAULT}}$ signal high, independent of faults being present. TI recommends monitoring the $\overline{\text{OTW}}$ signal using the system micro controller and responding to an overtemperature warning signal by, for example, turning down the volume to prevent further heating of the device resulting in device shutdown (OTE).

To reduce external component count, an internal pullup resistor to 3.3 V is provided on both $\overline{\text{FAULT}}$, $\overline{\text{CLIP}}$, and $\overline{\text{OTW}}$ outputs. See *Electrical Characteristics* for actual values.

The $\overline{\text{FAULT}}$, $\overline{\text{OTW}}$, pins are active-low, open-drain outputs. Their function is for protection-mode signaling to a PWM controller or other system-control device.

Any fault resulting in device shutdown is signaled by the $\overline{\text{FAULT}}$ pin going low. Likewise, $\overline{\text{OTW}}$ goes low when the device junction temperature exceeds 125°C (see the following table).

Table 3. Error Reporting

$\overline{\text{FAULT}}$	$\overline{\text{OTW}}$	DESCRIPTION
0	0	Overtemperature (OTE) or overload (OLP) or undervoltage (UVP)
0	1	Overload (OLP) or undervoltage (UVP)
1	0	Junction temperature higher than 125°C (overtemperature warning)
1	1	Junction temperature lower than 125°C and no OLP or UVP faults (normal operation)

7.3.10 Fault Handling

If a fault situation occurs while in operation, the device will act accordingly to the fault being a global or a channel fault. A global fault is a chip-wide fault situation and will cause all PWM activity of the device to be shut down, and will assert $\overline{\text{FAULT}}$ low. A global fault is a latching fault and clearing $\overline{\text{FAULT}}$ and restart operation requires resetting the device by toggling $\overline{\text{RESET}}$. Toggling $\overline{\text{RESET}}$ should never be allowed with excessive system temperature, so it is advised to monitor $\overline{\text{RESET}}$ by a system microcontroller and only allow releasing $\overline{\text{RESET}}$

(RESET high) if the OTW signal is cleared (high). A channel fault will result in shutdown of the PWM activity of the affected channel(s). Note that asserting RESET low forces the FAULT signal high, independent of faults being present. TI recommends monitoring the OTW signal using the system micro controller and responding to an over temperature warning signal by, for example, turning down the volume to prevent further heating of the device resulting in device shutdown (OTE).

Table 4. Fault Handling

Fault/Event	Fault/Event Description	Global or Channel	Reporting Method	Latched/Self Clearing	Action needed to Clear	Output FETs
PVDD_X UVP	Voltage Fault	Global	FAULT Pin	Self Clearing	Increase affected supply voltage	Hi-Z
VDD UVP						
GVDD_X UVP						
AVDD UVP						
POR (DVDD UVP)	Power On Reset	Global	FAULT Pin	Self Clearing	Allow DVDD to rise	H-Z
BST UVP	Voltage Fault	Channel (half bridge)	None	Self Clearing	Allow BST capacitor to recharge (lowside on, VDD 12V)	HighSide Off
OTW	Thermal Warning	Global	OTW Pin	Self Clearing	Cool below lower OTW threshold	Normal operation
OTE (OTSD)	Thermal Shutdown	Global	FAULT Pin	Latched	Toggle RESET	Hi-Z
OLP (CBC >2.6ms)	OC shutdown	Channel	FAULT Pin	Latched	Toggle RESET	Hi-Z
Latched OC (ROC >47k)	OC shutdown	Channel	FAULT Pin	Latched	Toggle RESET	Hi-Z
CBC (24k<ROC<33k)	OC Limiting	Channel	None	Self Clearing	reduce signal level or remove short	Flip state, cycle by cycle at fs/2
Stuck at Fault(1) (1 to 3 channels)	No PWM	Channel	None	Self Clearing	resume PWM	Hi-Z
Stuck at Fault(1) (All channels)	No PWM	Global	None	Self Clearing	resume PWM	Hi-Z

(1) Stuck at Fault occurs when input PWM drops below minimum PWM frame rate given in *Recommended Operating Conditions*

7.3.11 Device Reset

When RESET is asserted low, all power-stage FETs in the four half-bridges are forced into a high-impedance (Hi-Z) state.

In BTL modes, to accommodate bootstrap charging prior to switching start, asserting the reset input low enables weak pulldown of the half-bridge outputs. In the SE mode, the output is forced into a high impedance state when asserting the reset input low. Asserting reset input low removes any fault information to be signaled on the FAULT output, that is, FAULT is forced high. A rising-edge transition on reset input allows the device to resume operation after an overload fault. To ensure thermal reliability, the rising edge of RESET must occur no sooner than 4 ms after the falling edge of FAULT.

7.4 Device Functional Modes

There are three main output modes that the user can configure the device as per application requirement. In addition there are two PWM modulation modes, AD and BD.

AD modulation can have single-ended (SE) or differential analog inputs. AD modulation can also be configured to have SE, BTL, BTL+SE, or PBTL outputs. BD modulation requires differential analog inputs.

BD modulation can only be configured in BTL or PTBL mode.

8 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

The following sections discuss in detail three typical audio PWM (class-D) configurations:

- Differential input, stereo BTL outputs
- Differential input, mono PBTL output
- Single-ended inputs, quad single-ended outputs.

8.2 Typical Applications

8.2.1 Typical BTL Application

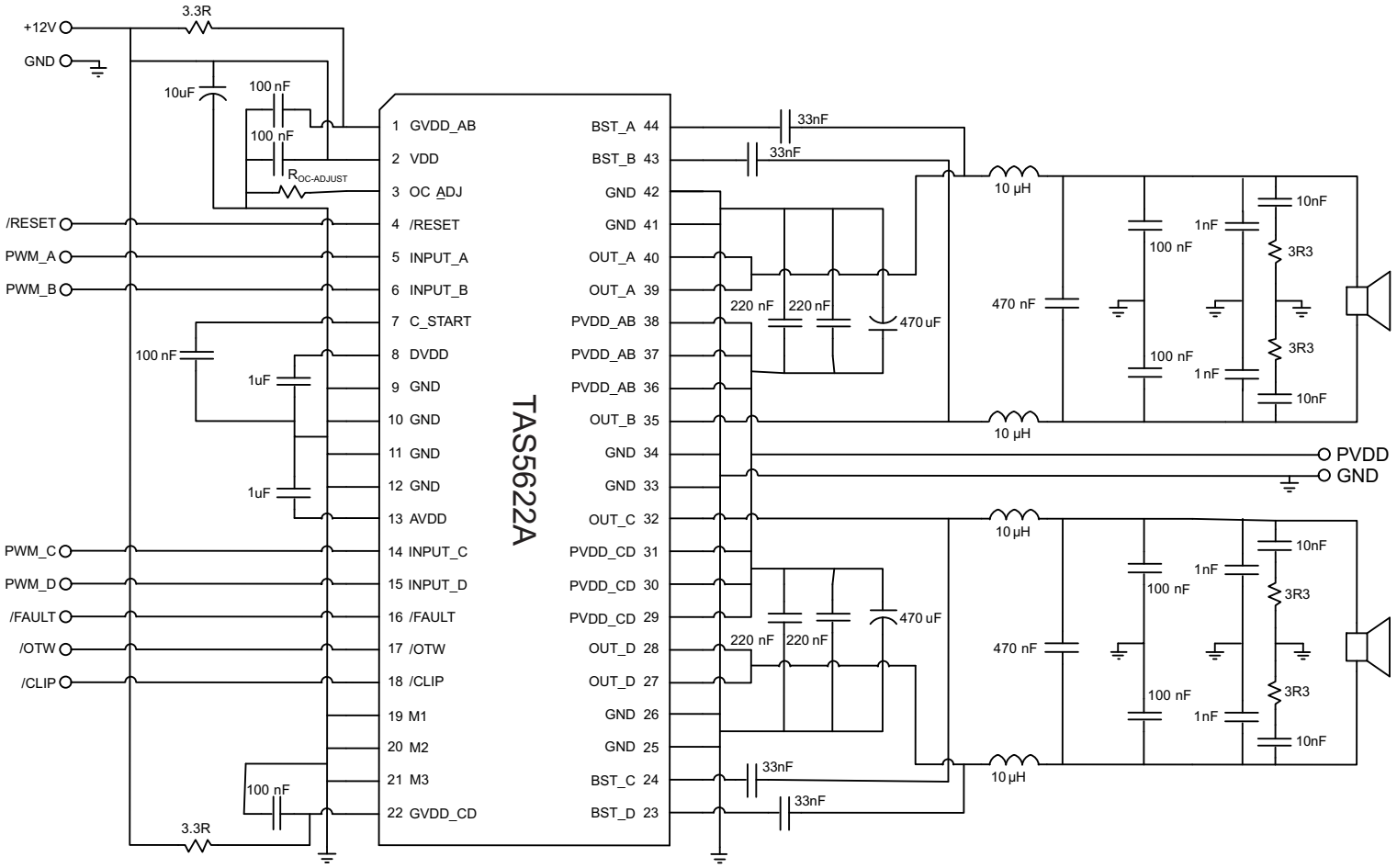


Figure 16. Typical Differential (2N) BTL Application With AD Modulation Filters

8.2.1.1 Design Requirements

See Figure 16 for application schematic. In this application, differential PWM inputs are used with AD modulation from the PWM modulator (that is, TAS5558). AD modulation scheme is defined as PWM(+) is opposite polarity from PWM(-).

8.2.1.2 Detailed Design Procedure

- Pin 1 - GVDD_AB is the gate drive voltage for half-bridges A and B. It needs a 3.3-Ω isolation resistor and a 0.1-µF decoupling capacitor.
- Pin 2 - VDD is the supply for internal voltage regulators AVDD and DVDD. It needs a 10-µF bulk capacitor and a 0.1-µF decoupling capacitor.
- Pin 3 - Roc adjust is the overcurrent programming resistor. Depending on the application, this resistor can be between 24 kΩ to 68 kΩ.
- Pin 4 - RESET pin when asserted, it keeps outputs high Z and no PWM switching. This pin can be controlled by a microprocessor.
- Pins 5 and 6 - These are PWM (+) and PWM (–) pins with signals provided by a PWM modulator such as TAS5558. These are PWM differential pair.
- Pin 7 - Start-up ramp capacitor should be 0.1 µF for BTL configuration.
- Pin 8 - Digital output supply pin is connected to 1-µF decoupling capacitor.
- Pins 9-12 - Ground pins are connected to board ground.
- Pin 13 - Analog output supply pin is connected to 1-µF decoupling capacitor.
- Pins 14 and 15 - These are PWM (+) and PWM (–) pins with signals provided by a PWM modulator such as TAS5558. These are PWM differential pair.
- Pin 16 - Fault pin can be monitored by a microcontroller through GPIO pin. System can decide to assert reset or shutdown.
- Pin 17 - Overtemperature warning pin can be monitored by a micro-controller through a GPIO pin. System can decide to turn on fan or lower output power.
- Pin 18 - Output clip indicator can be monitored by a microcontroller through a GPIO pin. System can decide to lower the volume.
- Pins 19-21 - Mode pins set the input and output configurations. For this configuration M1-M3 are grounded. These mode pins must be hardware configured, such as, not through GPIO pins from a microcontroller.
- Pin 22 - GVDD_CD is the gate drive voltage for half-bridges C and D. This pin needs a 3.3-Ω isolation resistor and a 0.1-µF decoupling capacitor.
- Pins 23, 24, 43, 44 - Bootstrap pins for half-bridges A, B, C, and D. Connect 33 nF from this pin to corresponding output pins.
- Pins 25, 26, 33, 34, 41, 42 - These ground pins should be used to ground decoupling capacitors from PVDD_X.
- Pins 27, 28, 32, 35, 39, 40 - Output pins from half-bridges A, B, C, and D. Connect appropriate bootstrap capacitors and differential LC filter as shown in Figure 16.
- Pins 29, 30, 31, 36, 37, 38 - Power supply pins to half-bridges A, B, C, and D. A and B form a full-bridge and C and D form another full-bridge. A 470-µF bulk capacitor is recommended for each full-bridge power pins. Two 0.22-µF decoupling capacitors are placed on each full-bridge power pins. See Figure 16 for details.

8.2.1.3 Application Curves

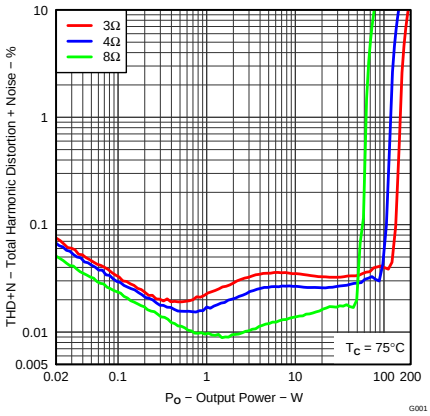


Figure 17. Total Harmonic + Noise vs Output Power, 1 kHz

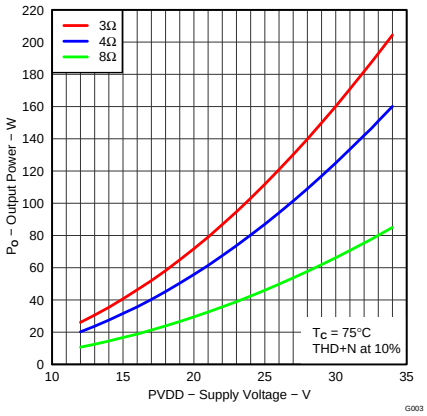


Figure 18. Output Power vs Supply Voltage vs Distortion + Noise = 10%

8.2.2 Typical SE Configuration

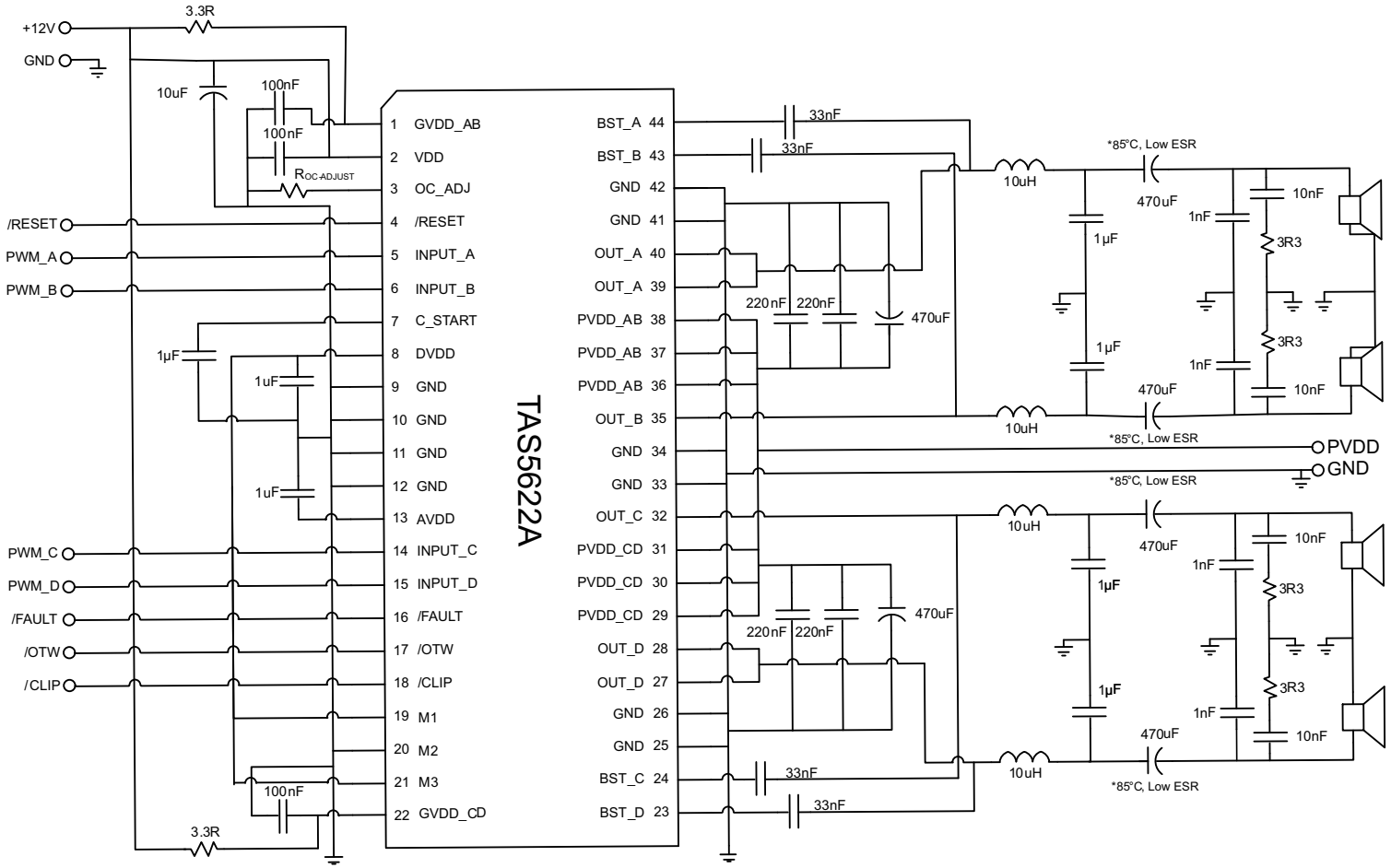


Figure 19. Typical (1N) SE Application

8.2.2.1 Design Requirements

See Figure 19 for application schematic. In this application, four single-ended PWM inputs are used with AD modulation from the PWM modulator such as the TAS5558. AD modulation scheme is defined as PWM(+) is opposite polarity from PWM(-). The single-ended (SE) output configuration is often used to drive 4 independent channels in one TAS5622A device.

8.2.2.2 Detailed Design Procedure

- Pin 1 - GVDD_AB is the gate drive voltage for half-bridges A and B. It needs a 3.3-Ω isolation resistor and a 0.1-µF decoupling capacitor.
- Pin 2 - VDD is the supply for internal voltage regulators AVDD and DVDD. It needs a 10-µF bulk capacitor and a 0.1-µF decoupling capacitor.
- Pin 3 - Roc adjust is the overcurrent programming resistor. Depending on the application, this resistor can be between 24 kΩ to 68 kΩ.
- Pin 4 - RESET pin when asserted, it keeps outputs high Z and no PWM switching. This pin can be controlled by a microprocessor.
- Pins 5 and 6 - These are PWM (+) and PWM (–) pins with signals provided by a PWM modulator such as TAS5558. These are PWM differential pair.
- Pin 7 - Start up ramp capacitor should be 1 µF for SE configuration.
- Pin 8 - Digital output supply pin is connected to 1-µF decoupling capacitor.
- Pins 9-12 - Ground pins are connected to board ground.
- Pin 13 - Analog output supply pin is connected to 1-µF decoupling capacitor.
- Pins 14 and 15 - These are PWM (+) and PWM (–) pins with signals provided by a PWM modulator such as TAS5558. These are PWM differential pair.
- Pin 16 - Fault pin can be monitored by a microcontroller through GPIO pin. System can decide to assert reset or shutdown.
- Pin 17 - Overtemperature warning pin can be monitored by a micro-controller through a GPIO pin. System can decide to turn on fan or lower output power.
- Pin 18 - Output clip indicator can be monitored by a microcontroller through a GPIO pin. System can decide to lower the volume.
- Pins 19-21 - Mode pins set the input and output configurations. For this configuration M1-M3 are grounded. These mode pins must be hardware configured, such as, not through GPIO pins from a microcontroller.
- Pin 22 - GVDD_CD is the gate drive voltage for half-bridges C and D. This pin needs a 3.3-Ω isolation resistor and a 0.1-µF decoupling capacitor.
- Pins 23, 24, 43, 44 - Bootstrap pins for half-bridges A, B, C, and D. Connect 33 nF from this pin to corresponding output pins.
- Pins 25, 26, 33, 34, 41, 42 - These ground pins should be used to ground decoupling capacitors from PVDD_X.
- Pins 27, 28, 32, 35, 39, 40 - Output pins from half-bridges A, B, C, and D. Connect appropriate bootstrap capacitors and differential LC filter as shown in Figure 19.
- Pins 29, 30, 31, 36, 37, 38 - Power supply pins to half-bridges A, B, C, and D. A and B form a full-bridge and C and D form another full-bridge. A 470-µF bulk capacitor is recommended for each full-bridge power pins. Two 0.22-µF decoupling capacitors are placed on each full-bridge power pins. See Figure 19 for details.

8.2.2.3 Application Curves

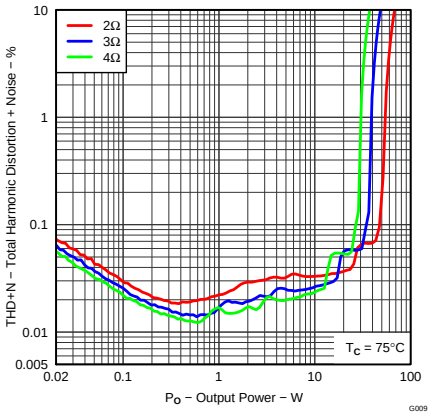


Figure 20. Total Harmonic Distortion + Noise vs Output Power

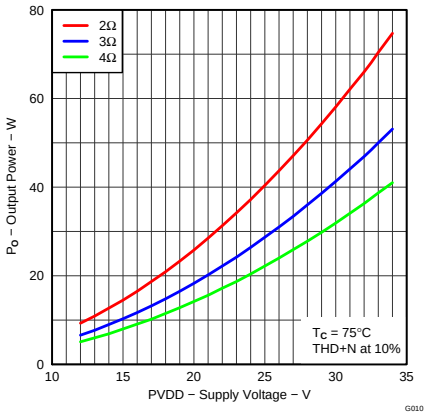


Figure 21. Output Power vs Supply Voltage

8.2.3 Typical PBTL Configuration

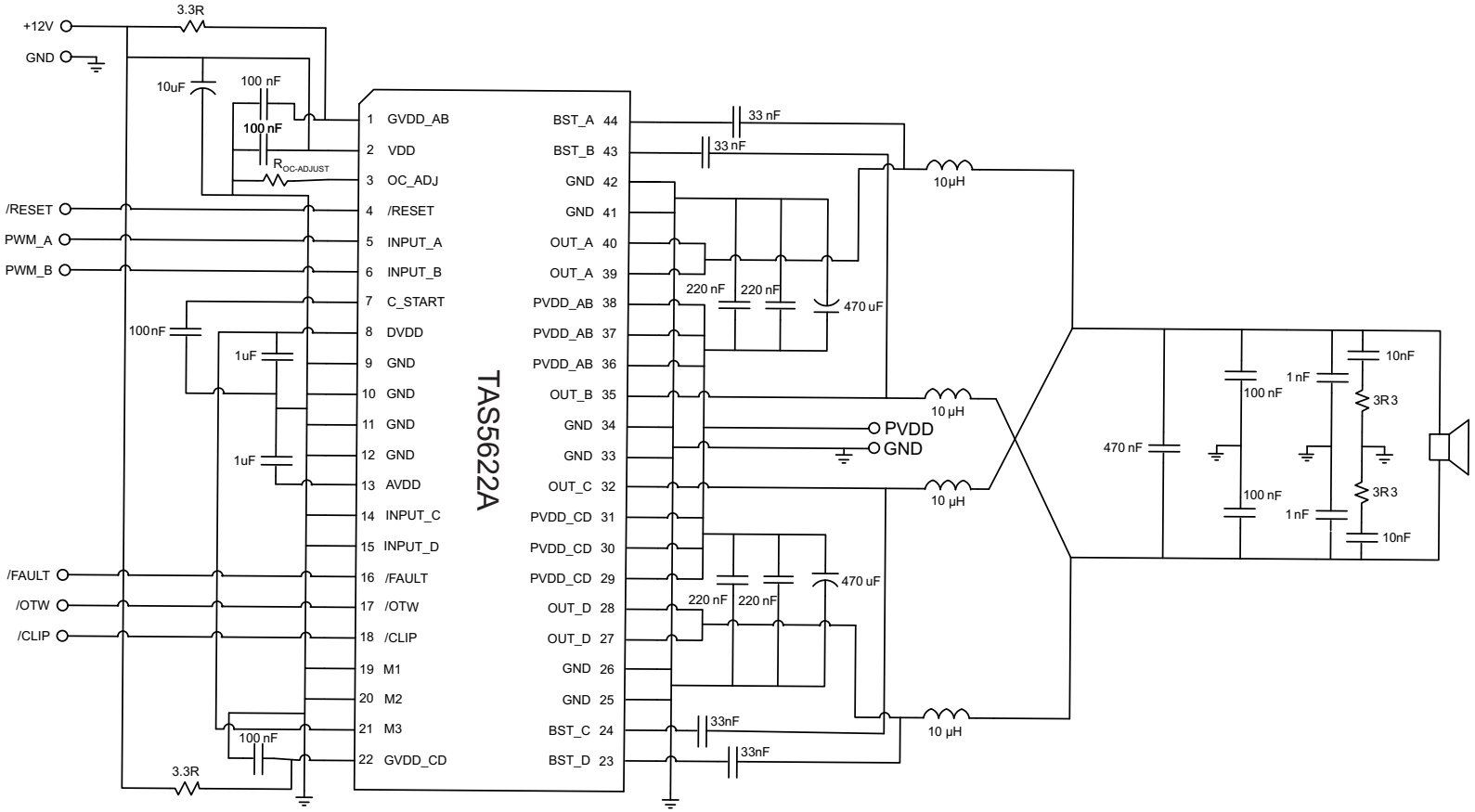


Figure 22. Typical Differential (2N) PBTL Application With AD Modulation Filter

8.2.3.1 Design Requirements

See Figure 22 for application schematic. In this application, one differential PWM input is used with AD modulation from the PWM modulator such as the TAS5558. AD modulation scheme is defined as PWM(+) is opposite polarity from PWM(-). The output PBTL configuration is often used to drive lower impedance load such as a subwoofer.

8.2.3.2 Detailed Design Procedure

- Pin 1 - GVDD_AB is the gate drive voltage for half-bridges A and B. This pin needs a 3.3-Ω isolation resistor and a 0.1-µF decoupling capacitor.
- Pin 2 - VDD is the supply for internal voltage regulators AVDD and DVDD. This pin needs a 10-µF bulk capacitor and a 0.1-µF decoupling capacitor.
- Pin 3 - Roc adjust is the overcurrent programming resistor. Depending on the application, this resistor can be between 24 kΩ to 68 kΩ.
- Pin 4 - RESET pin when asserted, it keeps outputs high Z and no PWM switching. This pin can be controlled by a microprocessor.
- Pins 5 and 6 - These are PWM (+) and PWM (–) pins with signals provided by a PWM modulator such as TAS5558. These are PWM differential pair.
- Pin 7 - Start up ramp capacitor should be 0.1 µF for PBTL configuration.
- Pin 8 - Digital output supply pin is connected to 1-µF decoupling capacitor.
- Pins 9-12 - Ground pins are connected to board ground.
- Pin 13 - Analog output supply pin is connected to 1-µF decoupling capacitor.
- Pins 14 and 15 - These are PWM (+) and PWM (–) pins with signals provided by a PWM modulator such as TAS5558. These are PWM differential pair.
- Pin 16 - Fault pin can be monitored by a microcontroller through GPIO pin. System can decide to assert reset or shutdown.
- Pin 17 - Overtemperature warning pin can be monitored by a microcontroller through a GPIO pin. System can decide to turn on fan or lower output power.
- Pin 18 - Output clip indicator can be monitored by a microcontroller through a GPIO pin. System can decide to lower the volume.
- Pins 19-21 - Mode pins set the input and output configurations. For this configuration M1-M3 are grounded. These mode pins must be hardware configured, such as, not through GPIO pins from a micro-controller.
- Pin 22 - GVDD_CD is the gate drive voltage for half-bridges C and D. This pin needs a 3.3-Ω isolation resistor and a 0.1-µF decoupling capacitor.
- Pins 23, 24, 43, 44 - Bootstrap pins for half-bridges A, B, C, and D. Connect 33 nF from this pin to corresponding output pins.
- Pins 25, 26, 33, 34, 41, 42 - These ground pins should be used to ground decoupling capacitors from PVDD_X.
- Pins 27, 28, 32, 35, 39, 40 - Output pins from half-bridges A, B, C, and D. Connect appropriate bootstrap capacitors and differential LC filter as shown in Figure 22.
- Pins 29, 30, 31, 36, 37, 38 - Power supply pins to half-bridges A, B, C, and D. A and B form a full-bridge and C and D form another full-bridge. A 470-µF bulk capacitor is recommended for each full-bridge power pins. Two 0.22-µF decoupling capacitors are placed on each full-bridge power pins. See Figure 22 for details.

8.2.3.3 Application Curves

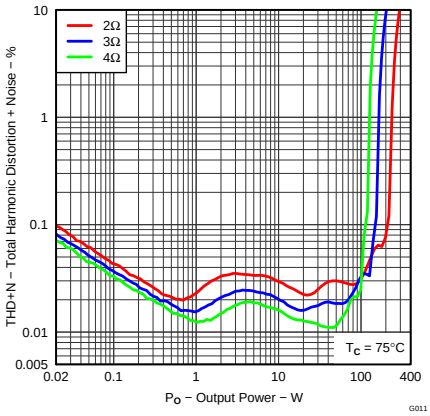


Figure 23. Total Harmonic Distortion + Noise vs Output Power

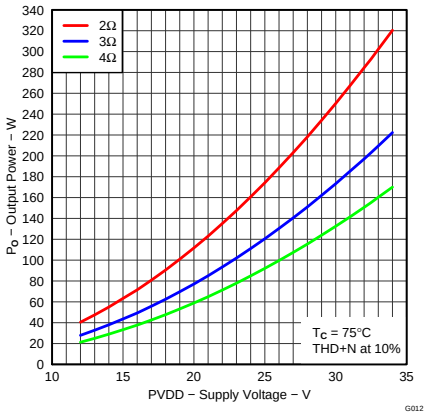


Figure 24. Output Power vs Supply Voltage

9 Power Supply Recommendations

To facilitate system design, the TAS5622A needs only a 12-V supply in addition to the (typical) 32.5-V power-stage supply. An internal voltage regulator provides suitable voltage levels for the digital and low-voltage analog circuitry. Additionally, all circuitry requiring a floating voltage supply, that is, the high-side gate drive, is accommodated by built-in bootstrap circuitry requiring only an external capacitor for each half-bridge.

To provide outstanding electrical and acoustical characteristics, the PWM signal path including gate drive and output stage is designed as identical, independent half-bridges. For this reason, each half-bridge has separate bootstrap pins (BST_X) and each full-bridge has separate power stage supply (PVDD_X) and gate supply (GVDD_X) pins. Although supplied from the same 12-V source, it is highly recommended to separate GVDD_AB, GVDD_CD, and VDD on the printed-circuit board (PCB) by RC filters (see application diagram for details). These RC filters provide the recommended high-frequency isolation. Special attention should be paid to placing all decoupling capacitors as close to their associated pins as possible. In general, inductance between the power supply pins and decoupling capacitors must be avoided. (See reference board documentation for additional information.)

Special attention should be paid to the power-stage power supply; this includes component selection, PCB placement, and routing. As indicated, each full-bridge has independent power-stage supply pins (PVDD_X). For optimal electrical performance, EMI compliance, and system reliability, it is important that each PVDD_X connection is decoupled with minimum 2x 220 nF ceramic capacitors placed as close as possible to each supply pin. It is recommended to follow the PCB layout of the TAS5622A reference design. For additional information on recommended power supply and required components, see the application diagrams in this data sheet.

The 12-V supply should be from a low-noise, low-output-impedance voltage regulator. Likewise, the 32.5-V power-stage supply is assumed to have low output impedance and low noise. The power-supply sequence is not critical as facilitated by the internal power-on-reset circuit. Moreover, the TAS5622A is fully protected against erroneous power-stage turn on due to parasitic gate charging when power supplies are applied. Thus, voltage-supply ramp rates (dV/dt) are noncritical within the specified range (see the *Recommended Operating Conditions* table of this data sheet).

9.1 Boot Strap Supply

For a properly functioning bootstrap circuit, a small ceramic capacitor must be connected from each bootstrap pin (BST_X) to the power-stage output pin (OUT_X). When the power-stage output is low, the bootstrap capacitor is charged through an internal diode connected between the gate-drive power-supply pin (GVDD_X) and the bootstrap pin. When the power-stage output is high, the bootstrap capacitor potential is shifted above the output potential and thus provides a suitable voltage supply for the high-side gate driver. In an application with PWM switching frequencies in the range from 300 kHz to 400 kHz, it is recommended to use 33-nF ceramic capacitors, size 0603 or 0805, for the bootstrap supply. These 33-nF capacitors ensure sufficient energy storage, even during minimal PWM duty cycles, to keep the high-side power stage FET (LDMOS) fully turned on during the remaining part of the PWM cycle.

10 Layout

10.1 Layout Guidelines

A rising-edge transition on reset input allows the device to execute the start-up sequence and starts switching.

Apply audio only according to the timing information for start-up and shutdown sequence. That will start and stop the amplifier without audible artifacts in the output transducers.

The $\overline{\text{CLIP}}$ signal indicates that the output is approaching clipping (when output PWM starts skipping pulses due to loop filter saturation). The signal can be used to initiate an audio volume decrease or to adjust the power supply rail.

The device inverts the audio signal from input to output.

The DVDD and AVDD pins are not recommended to be used as a voltage source for external circuitry.

Layout Guidelines (continued)

10.1.1 PCB Material Recommendation

FR-4 Glass Epoxy material with 1 oz. (35 µm) is recommended for use with the TAS5622A. The use of this material can provide for higher power output, improved thermal performance, and better EMI margin (due to lower PCB trace inductance.

10.1.2 PVDD Capacitor Recommendation

The large capacitors used in conjunction with each full-bridge, are referred to as the PVDD Capacitors. These capacitors should be selected for proper voltage margin and adequate capacitance to support the power requirements. In practice, with a well designed system power supply, 1000 µF, 50 V should support most applications. The PVDD capacitors should be low ESR type because they are used in a circuit associated with high-speed switching.

10.1.3 Decoupling Capacitor Recommendation

To design an amplifier that has robust performance, passes regulatory requirements, and exhibits good audio performance, good quality decoupling capacitors should be used. In practice, X5R or better should be used in this application.

The voltage of the decoupling capacitors should be selected in accordance with good design practices. Temperature, ripple current, and voltage overshoot must be considered. This fact is particularly true in the selection of the close decoupling capacitor that is placed on the power supply to each half-bridge. It must withstand the voltage overshoot of the PWM switching, the heat generated by the amplifier during high power output, and the ripple current created by high power output. A minimum voltage rating of 50V is required for use with a 32.5 V power supply.

See the TAS5624ADDVEVM User's Guide for more details including layout and Bill-of-Materials.

10.1.4 Circuit Component Requirements

A number of circuit components are critical to performance and reliability. They include LC filter inductors and capacitors, decoupling capacitors and the heatsink. The best detailed reference for these is the TAS5622A EVM BOM in the User's Guide, which includes components that meet all the following requirements.

- High frequency decoupling capacitors: small high frequency decoupling capacitors are placed next to the IC to control switching spikes and keep high frequency currents in a tight loop to achieve best performance and reliability and EMC. They must be high quality ceramic parts with material like X7R or X5R and voltage ratings at least 30% greater than PVDD, to minimize loss of capacitance caused by applied DC voltage. (Capacitors made of materials like Y5V or Z5U should never be used in decoupling circuits or audio circuits because their capacitance falls dramatically with applied DC and AC voltage, often to 20% of rated value or less.)
- Bulk decoupling capacitors: large bulk decoupling capacitors are placed as close as possible to the IC to stabilize the power supply at lower frequencies. They must be high quality aluminum parts with low ESR and ESL and voltage ratings at least 25% more than PVDD to handle power supply ripple currents and voltages.
- LC filter inductors: to maintain high efficiency, short circuit protection and low distortion, LC filter inductors must be linear to at least the OCP limit and must have low DC resistance and core losses. For SCP, minimum working inductance, including all variations of tolerance, temperature and current level, must be 5µH. Inductance variation of more than 1% over the output current range can cause increased distortion.
- LC filter capacitors: to maintain low distortion and reliable operation, LC filter capacitors must be linear to twice the peak output voltage. For reliability, capacitors must be rated to handle the audio current generated in them by the maximum expected audio output voltage at the highest audio frequency.
- Heatsink: The heatsink must be fabricated with the PowerPAD™ contact area spaced 1.0mm +/-0.01mm above mounting areas that contact the PCB surface. It must be supported mechanically at each end of the IC. This mounting ensures the correct pressure to provide good mechanical, thermal and electrical contact with TAS5622A PowerPAD™. The PowerPAD™ contact area must be bare and must be interfaced to the PowerPAD™ with a thin layer (about 1mil) of a thermal compound with high thermal conductivity.

Layout Guidelines (continued)

10.1.5 Printed Circuit Board Requirements

PCB layout, audio performance, EMC and reliability are linked closely together, and solid grounding improves results in all these areas. The circuit produces high, fast-switching currents, and care must be taken to control current flow and minimize voltage spikes and ground bounce at IC ground pins. Critical components must be placed for best performance and PCB traces must be sized for the high audio currents that the IC circuit produces.

Grounding: ground planes must be used to provide the lowest impedance and inductance for power and audio signal currents between the IC and its decoupling capacitors, LC filters and power supply connection. The area directly under the IC should be treated as central ground area for the device, and all IC grounds must be connected directly to that area. A matrix of vias must be used to connect that area to the ground plane. Ground planes can be interrupted by radial traces (traces pointing away from the IC), but they must never be interrupted by circular traces, which disconnect copper outside the circular trace from copper between it and the IC. Top and bottom areas that do not contain any power or signal traces should be flooded and connected with vias to the ground plane.

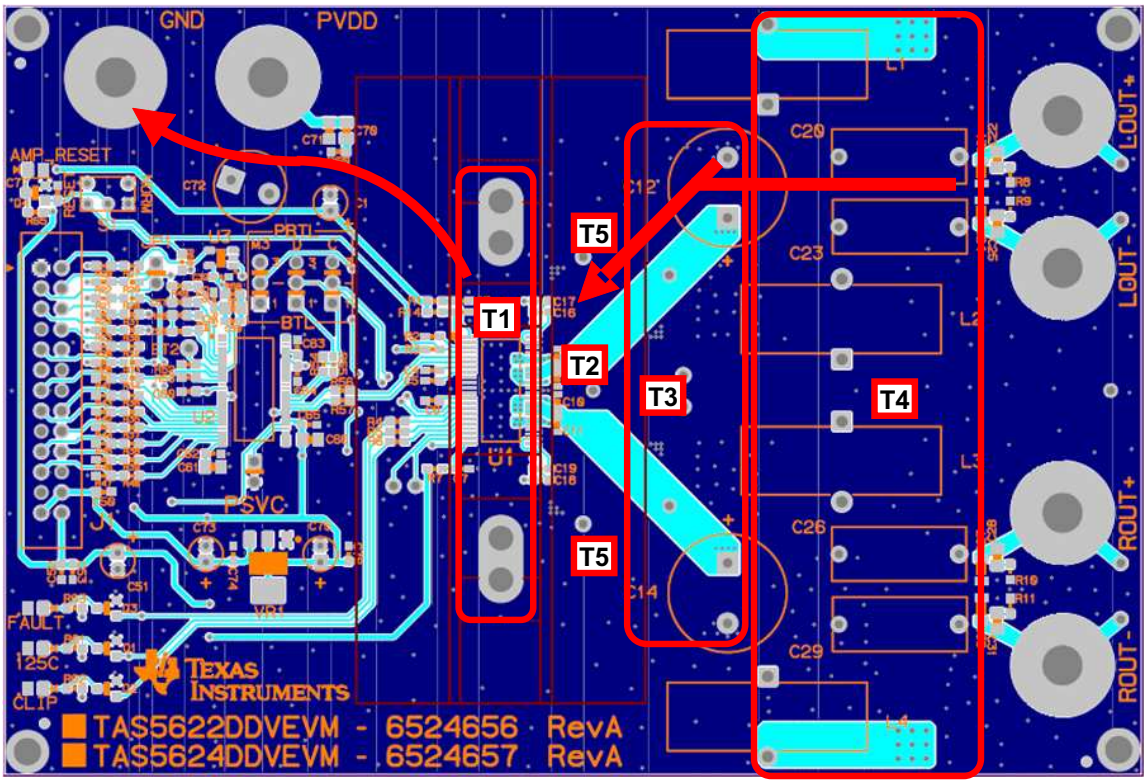
Decoupling capacitors: high frequency decoupling capacitors must be located within 2mm of the IC and connected directly to PVDD and GND pins with solid traces. Vias must not be used to complete these connections, but several vias must be used at each capacitor location to connect top ground directly to the ground plane. Placement of bulk decoupling capacitors is less critical, but they still must be placed as close as possible to the IC with strong ground return paths. Typically the heatsink sets the distance.

LC filters: LC filters must be placed as close as possible to the IC after the decoupling capacitors. The capacitors must have strong ground returns to the IC through top and bottom grounds for effective operation.

PCB copper must be at least 1 ounce thickness. PVDD and output traces must be wide enough to carry expected average currents without excessive temperature rise. PWM input traces must be kept short and close together on the input side of the IC and must be shielded with ground flood to avoid interference from high power switching signals.

The heatsink must be grounded well to the PCB near the IC, and a thin layer of highly conductive thermal compound (about 1mil) must be used to connect the heatsink to the PowerPAD™.

10.2 Layout Example



Note T1: Bottom and top layer ground plane areas are used to provide strong ground connections. The area under the IC must be treated as central ground, with IC grounds connected there and a strong via matrix connecting the area to bottom ground plane. The ground path from the IC to the power supply ground through top and bottom layers must be strong to provide very low impedance to high power and audio currents.

Note T2: Low impedance X7R or X5R ceramic high frequency decoupling capacitors must be placed within 2mm of PVDD and GND pins and connected directly to them and to top ground plane to provide good decoupling of high frequency currents for best performance and reliability. Their DC voltage rating must be 2 times PVDD.

Note T3: Low impedance electrolytic bulk decoupling capacitors must be placed as close as possible to the IC. Typically the heat sink sets the distance. Wide PVDD traces are routed on the top layer with direct connections to the pins, without going through vias.

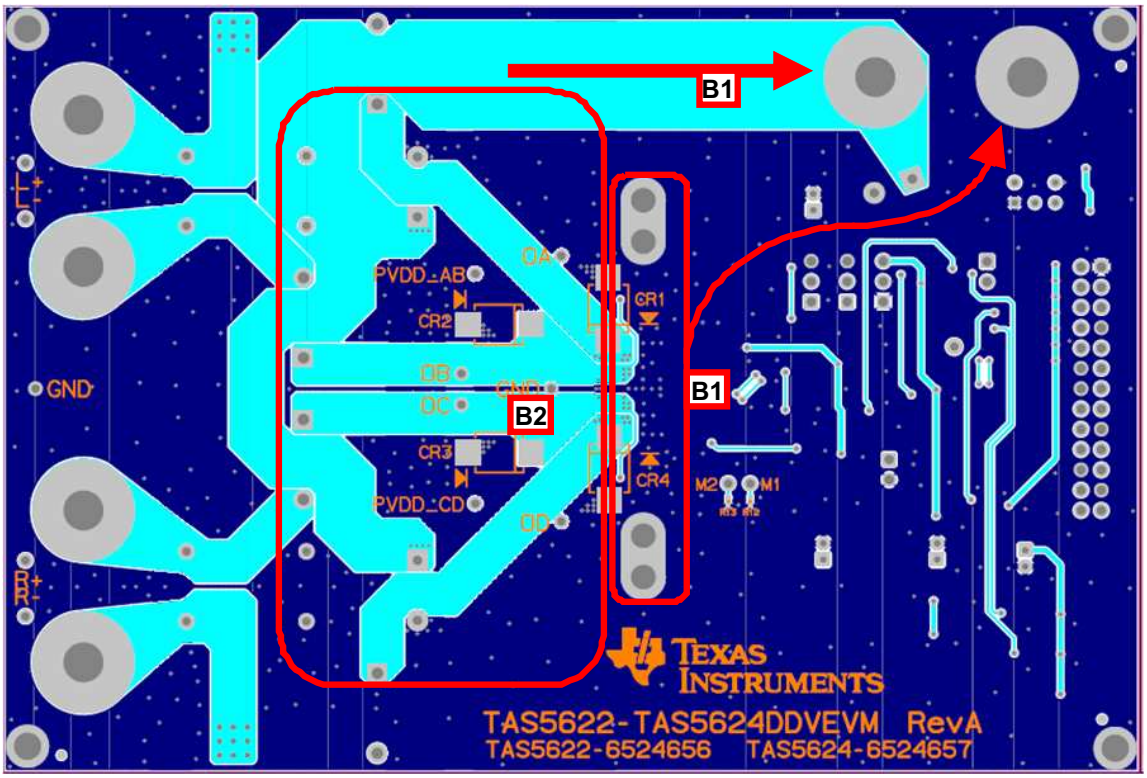
Note T4: LC filter inductors and capacitors must be placed as close as possible to the IC after decoupling capacitors. Inductors must have low DC resistance and switching losses and must be linear to at least the OCP (over current protection) limit. Capacitors must be linear to at least twice the maximum output voltage and must be capable of conducting currents generated by the maximum expected high frequency output.

Note T5: Bulk decoupling capacitors and LC filter capacitors must have strong ground return paths through ground plane to the central ground area under the IC.

Note T6: The heat sink must have a good thermal and electrical connection to PCB ground and to the IC PowerPAD™. It must be connected to the PowerPAD™ through a thin layer, about 1 mil, of highly conductive thermal compound.

Figure 25. Printed Circuit Board - Top Layer

Layout Example (continued)



Note B1: A wide PVDD bus and a wide ground path must be used to provide very low impedance to high power and audio currents to the power supply. Top and bottom ground planes must be connected with vias at many points to reinforce the ground connections.

Note B2: Wide output traces can be routed on the bottom layer and connected to output pins with strong via arrays.

Figure 26. Printed Circuit Board - Bottom Layer

11 Device and Documentation Support

11.1 Trademarks

PurePath, PowerPAD are trademarks of Texas Instruments.
Blu-ray is a trademark of Blu-ray Disk Association (BDA).
All other trademarks are the property of their respective owners.

11.2 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

11.3 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TAS5622ADDV	ACTIVE	HTSSOP	DDV	44	35	RoHS & Green	NIPDAU	Level-3-260C-168 HR	-40 to 125	TAS5622A	Samples
TAS5622ADDVR	ACTIVE	HTSSOP	DDV	44	2000	RoHS & Green	NIPDAU	Level-3-260C-168 HR	-40 to 125	TAS5622A	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

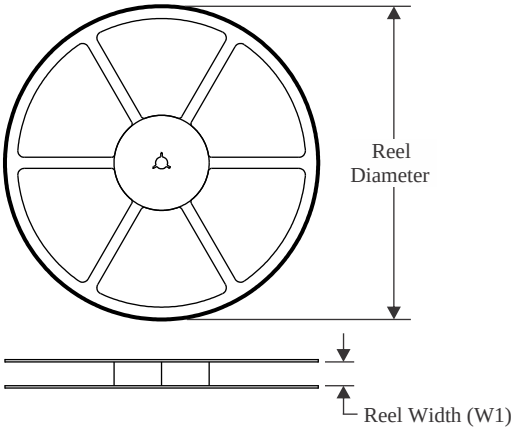
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

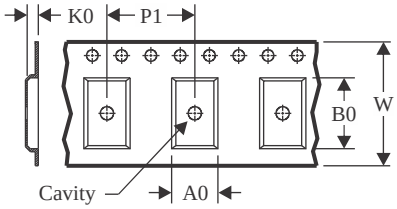
(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

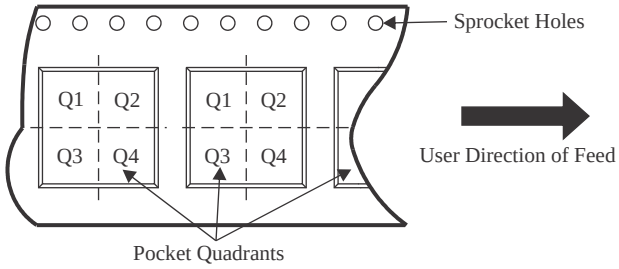


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

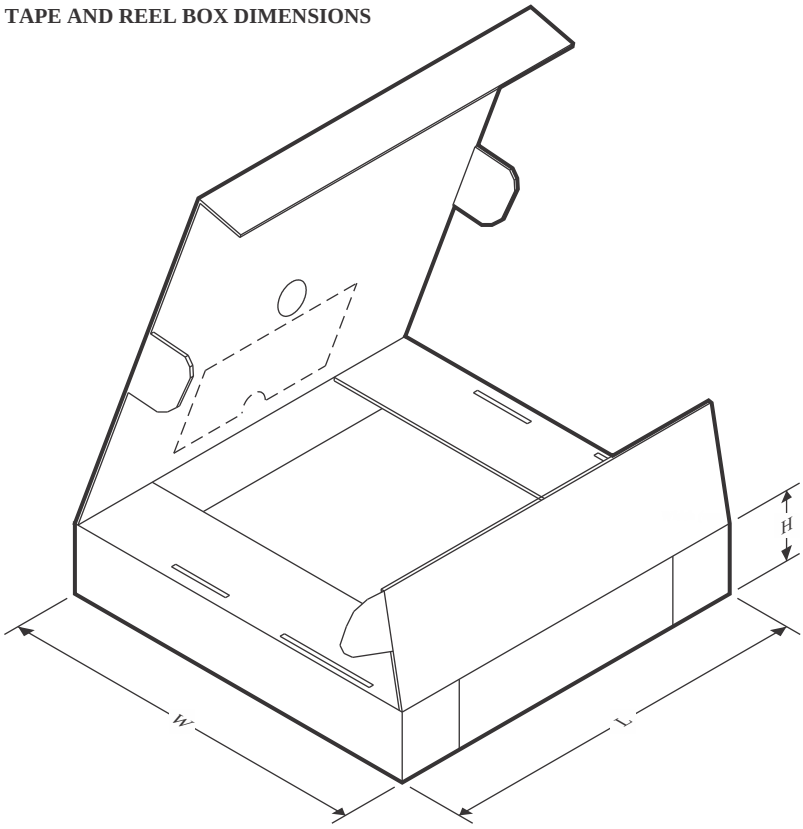
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TAS5622ADDVR	HTSSOP	DDV	44	2000	330.0	24.4	8.6	15.6	1.8	12.0	24.0	Q1

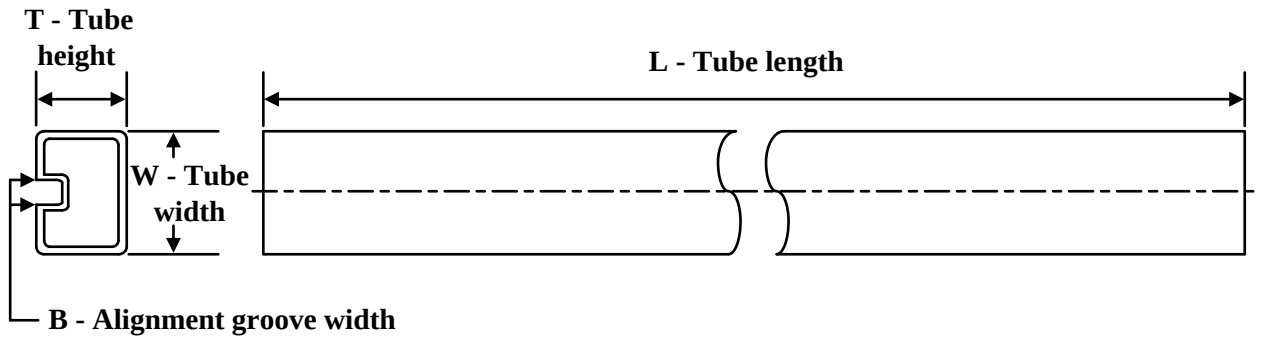
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TAS5622ADDVR	HTSSOP	DDV	44	2000	350.0	350.0	43.0

TUBE

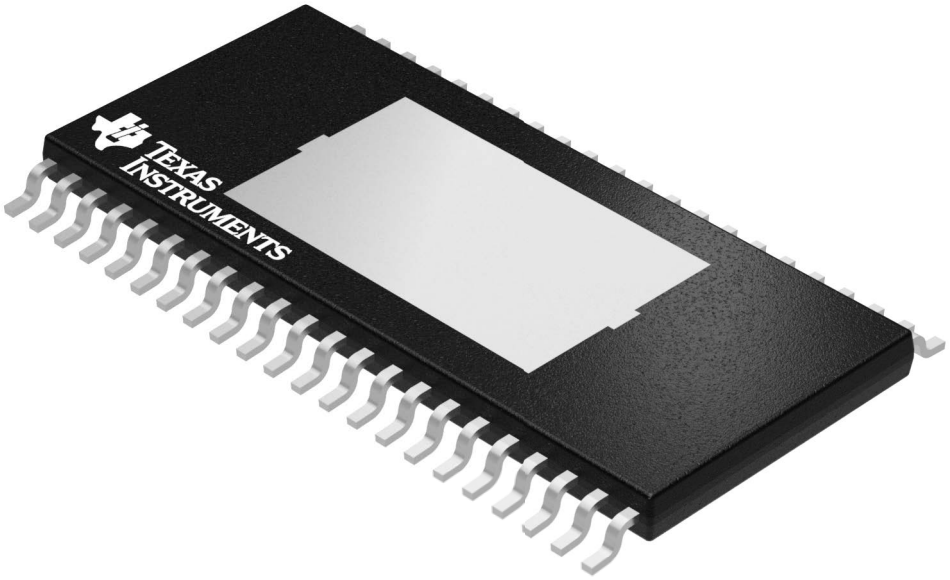


*All dimensions are nominal

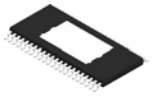
Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
TAS5622ADDV	DDV	HTSSOP	44	35	530	11.89	3600	4.9

DDV 44 PowerPAD™ TSSOP - 1.2 mm max height

PLASTIC SMALL OUTLINE



Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

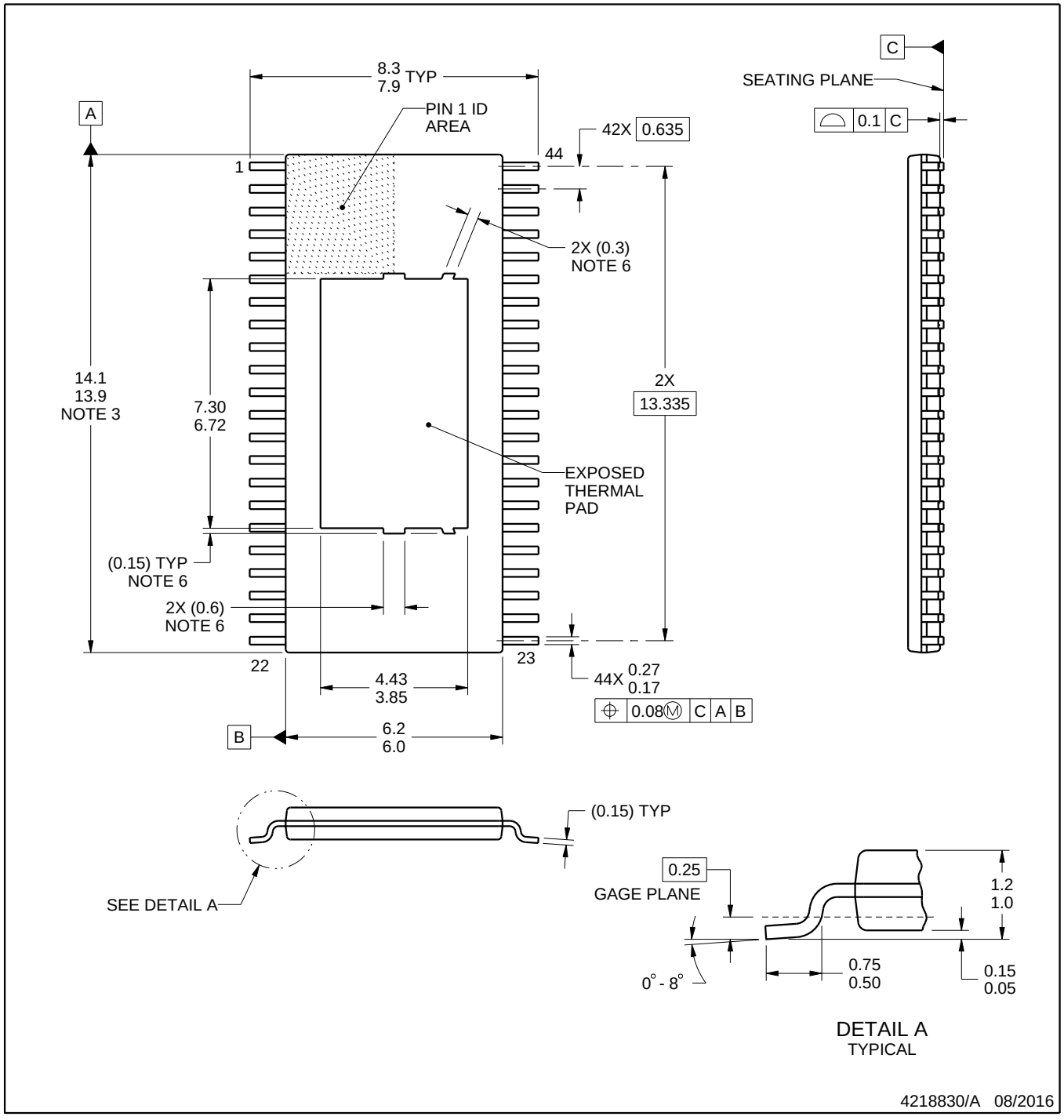


PACKAGE OUTLINE

DDV0044D

PowerPAD™ TSSOP - 1.2 mm max height

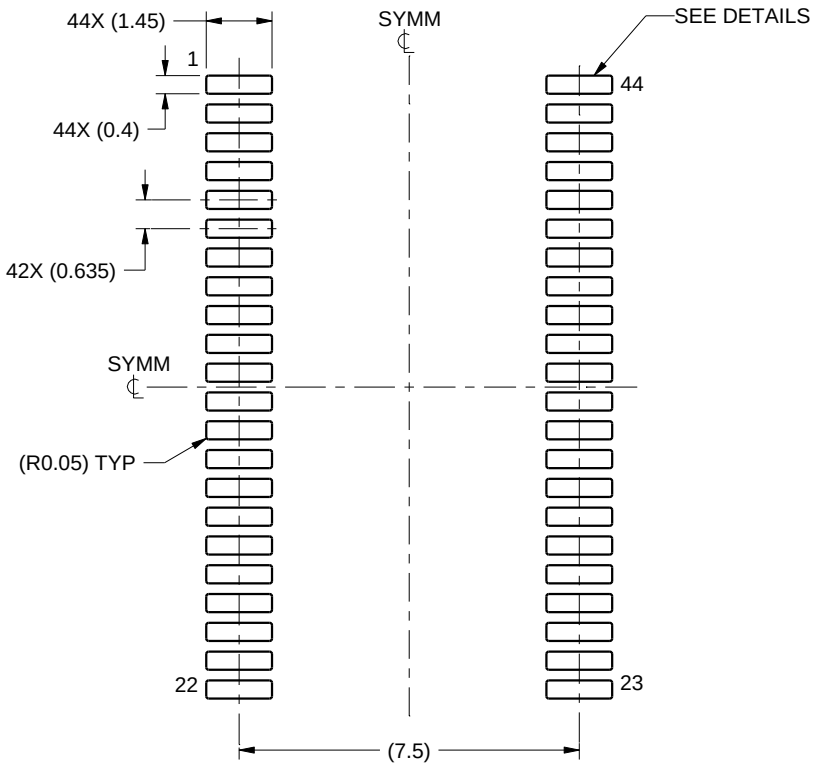
PLASTIC SMALL OUTLINE



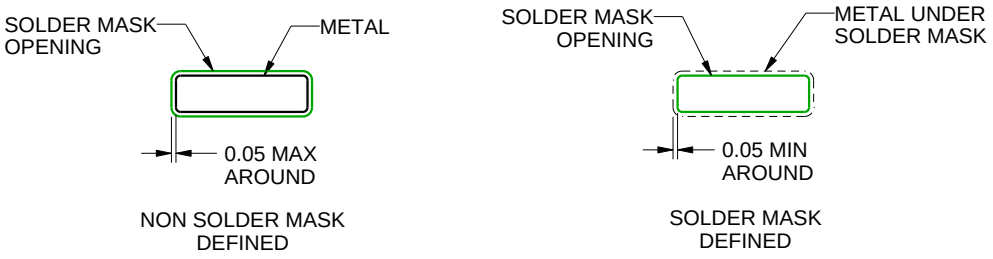
PowerPAD is a trademark of Texas Instruments.

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. Reference JEDEC registration MO-153.
5. The exposed thermal pad is designed to be attached to an external heatsink.
6. Features may differ or may not be present.



LAND PATTERN EXAMPLE
SCALE:6X

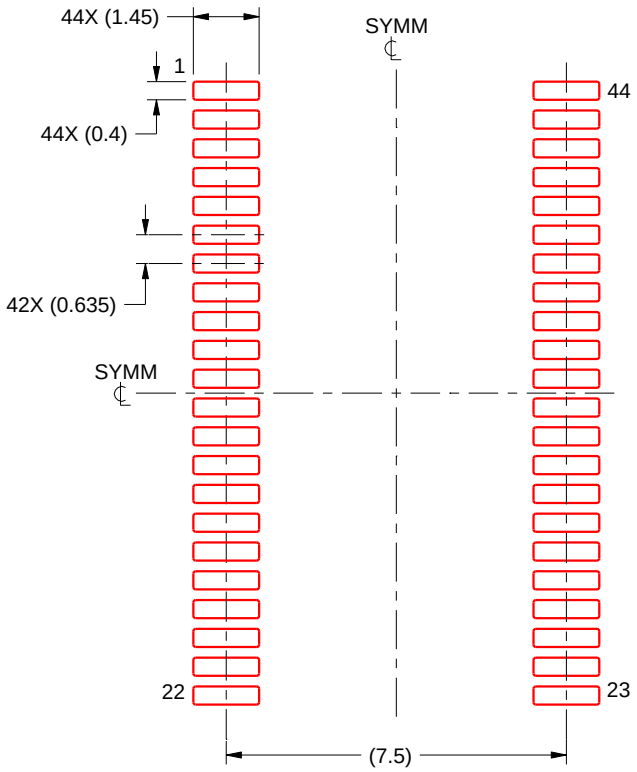


SOLDER MASK DETAILS
NOT TO SCALE

4218830/A 08/2016

NOTES: (continued)

7. Publication IPC-7351 may have alternate designs.
8. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 MM THICK STENCIL
SCALE :6X

4218830/A 08/2016

NOTES: (continued)

9. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
10. Board assembly site may have different recommendations for stencil design.

IMPORTANT NOTICE AND DISCLAIMER

TI PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATA SHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES “AS IS” AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, regulatory or other requirements.

These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you will fully indemnify TI and its representatives against, any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

TI’s products are provided subject to TI’s Terms of Sale or other applicable terms available either on ti.com or provided in conjunction with such TI products. TI’s provision of these resources does not expand or otherwise alter TI’s applicable warranties or warranty disclaimers for TI products.

TI objects to and rejects any additional or different terms you may have proposed.

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265

Looking for pricing, stock, or lifecycle information?

Click below to explore more details on WIN SOURCE:

- View TAS5622ADDVR on WIN SOURCE
- Texas Instruments Information

Optimize Your Supply Chain with WIN SOURCE Solutions

- Global Sourcing Solution
- Obsolete Management
- Cost Control Management
- Shortage Management
- Alternative Solution
- Excess Inventory Management