



**THE DATASHEET OF
SP332ET-L/TR**



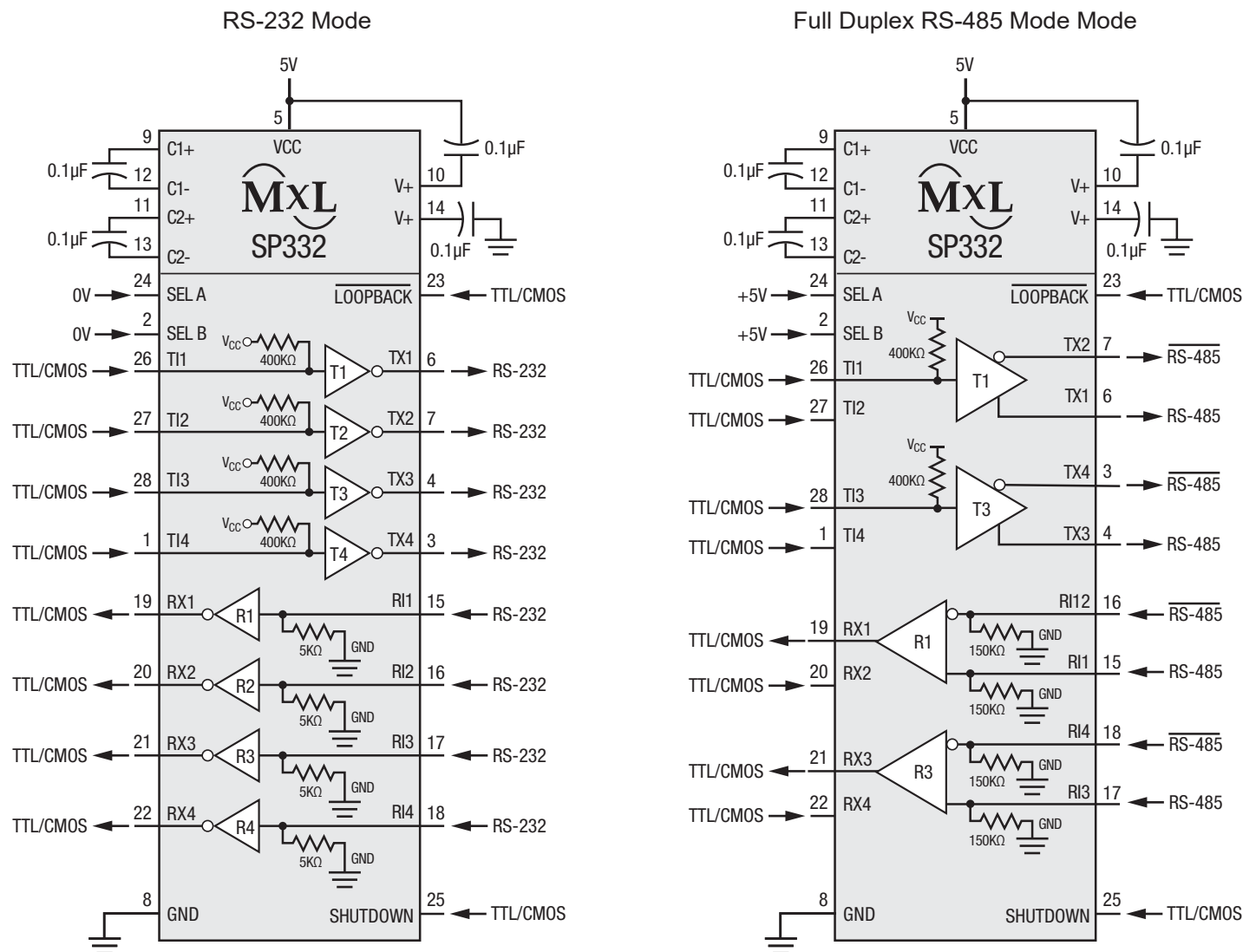
Description

The **SP332** is a monolithic device that contains both RS-232 and RS-485 line drivers and receivers. The configuration of the SP332 can be changed at any time by changing the logic state of two control pins. The device also includes a loop back function which internally connects driver outputs to receiver inputs for a chip self test. An MaxLinear-patented charge pump allows 5V-only operation.

FEATURES

- 5V only single supply operation
- Software programmable RS-232 or RS-485 selection
- 4 drivers, 4 receivers RS-232
- 2 drivers, 2 receivers RS-485
- Loop back function for self test
- 28-pin WSOIC package

Ordering Information - [Back Page](#)

Typical Applications Circuit


Absolute Maximum Ratings

These are stress ratings only and functional operation of the device at these ratings or any other above those indicated in the operation sections to the specifications below is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

| | | | |
|------------------------|------------------------------|-------------------------------|----------------|
| V_{CC} | 7V | Storage Temperature | -65°C to 150°C |
| Input Voltages | | Power Dissipation | |
| Logic..... | -0.5V to ($V_{CC} + 0.5V$) | 28-pin WSOIC | 1000mW |
| Drivers | -0.5V to ($V_{CC} + 0.5V$) | Power Derating, θ_{JA} | |
| Receivers..... | $\pm 30V @ \leq 100mA$ | 28-pin WSOIC | 40°C/W |
| Driver Outputs | $\pm 15V$ | | |
| Maximum Data Rate..... | 8Mbps ⁽¹⁾ | | |

Electrical Characteristics

Limits are specified at $T_A = 25^\circ C$ and $V_{CC} = 5.0V$ unless otherwise noted.

| Parameters | Min. | Typ. | Max. | Units | Conditions |
|--|------|------|----------|---------|--|
| RS-485 Driver DC Characteristics | | | | | |
| Differential output voltage | | | V_{CC} | Volts | Unloaded; $R = \infty\Omega$; See Figure 1 |
| Differential output voltage | 2.0 | | 5.0 | Volts | With load; $R = 50\Omega$ (RS-422); See Figure 1 |
| Differential output voltage | 1.5 | | 5.0 | Volts | With load; $R = 27\Omega$ (RS-485); See Figure 1 |
| Change in magnitude of driver differential output voltage for complementary states | | | 0.2 | Volts | $R = 27\Omega$ or $R = 50\Omega$; See Figure 1 |
| Driver common-mode output voltage | | | 3 | Volts | $R = 27\Omega$ or $R = 50\Omega$; See Figure 1 |
| Input high voltage | 2.0 | | | Volts | Applies to transmitter inputs, SEL A, SEL B, SD and \overline{LB} |
| Input low voltage | | | 0.8 | Volts | Applies to transmitter inputs, SEL A, SEL B, SD and \overline{LB} |
| Input current | | | ± 10 | μA | Applies to transmitter inputs, SEL A, SEL B, SD and \overline{LB} |
| Pull-up current | | 1.5 | | μA | |
| Pull-down current | | 3.0 | | μA | |
| Driver short circuit current $V_{OUT} = HIGH$ | 35 | | 250 | mA | $-7V \leq V_O \leq 10V$ |
| Driver short circuit current $V_{OUT} = LOW$ | 35 | | 250 | mA | $-7V \leq V_O \leq 10V$ |
| RS-485 Driver AC Characteristics | | | | | |
| Driver data rate | 10 | | | Mbps | |
| Driver data rate | | | 8 | Mbps | $T_A = 85^\circ C^{(1)}$ |
| Driver input to output t_{PLH} | | 70 | 180 | ns | $R_{DIFF} = 54\Omega$, $C_{L1} = C_{L2} = 100pF$; see Figures 3 and 5 |
| Driver input to output t_{PHL} | | 70 | 180 | ns | $R_{DIFF} = 54\Omega$, $C_{L1} = C_{L2} = 100pF$; see Figures 3 and 5 |
| Driver skew | | 5 | 10 | ns | From output to output; see Figures 3 and 5 |
| Driver rise or fall time | 3 | 15 | 40 | ns | From 10% to 90%; $R_{DIFF} = 54\Omega$, $C_{L1} = C_{L2} = 100pF$; see Figures 3 and 5 |

Electrical Characteristics (Continued)

Limits are specified at $T_A = 25^\circ\text{C}$ and $V_{CC} = 5.0\text{V}$ unless otherwise noted.

| Parameters | Min. | Typ. | Max. | Units | Conditions |
|---|-------|------|-----------|------------------|--|
| RS-485 Receiver DC Characteristics | | | | | |
| Differential input threshold | -0.2 | | 0.2 | Volts | $-7\text{V} \leq V_{CM} \leq 12\text{V}$ |
| Input hysteresis | | 70 | | mV | $V_{CM} = 0\text{V}$ |
| Output voltage HIGH | 3.5 | | | Volts | $I_O = -4\text{mA}$, $V_{ID} = 200\text{mV}$ |
| Output voltage LOW | | | 0.4 | Volts | $I_O = 4\text{mA}$, $V_{ID} = -200\text{mV}$ |
| Input resistance | 12 | 15 | | k Ω | $-7\text{V} \leq V_{CM} \leq 12\text{V}$ |
| Input current (A, B); $V_{IN} = 12\text{V}$ | | | 1.5 | mA | $V_{IN} = 12\text{V}$, A is the non-inverting receiver input. B is the inverting receiver input |
| Input current (A, B); $V_{IN} = -7\text{V}$ | | | -0.8 | mA | $V_{IN} = -7\text{V}$ |
| Short circuit current | | | 85 | mA | $0\text{V} \leq V_{CM} \leq V_{CC}$ |
| RS-485 Receiver AC Characteristics | | | | | |
| Receiver data rate | 10 | | | Mbps | |
| Receiver data rate | | | 8 | Mbps | $T_A = 85^\circ\text{C}^{(1)}$ |
| Receiver input to output t_{PLH} | | 130 | 250 | ns | $R_{DIFF} = 54\Omega$, $C_{L1} = C_{L2} = 100\text{pF}$; Figures 3 and 6 |
| Receiver input to output t_{PHL} | | 130 | 250 | ns | $R_{DIFF} = 54\Omega$, $C_{L1} = C_{L2} = 100\text{pF}$; Figures 3 and 6 |
| Differential receiver skew $ t_{PHL} - t_{PLH} $ | | 13 | | ns | $R_{DIFF} = 54\Omega$, $C_{L1} = C_{L2} = 100\text{pF}$; Figures 3 and 6 |
| RS-232 Driver DC Characteristics | | | | | |
| TTL input level V_{IL} | | | 0.8 | Volts | Applies to transmitter inputs, SEL A, SEL B, SD and $\overline{\text{LB}}$ |
| TTL input level V_{IH} | 2.0 | | | Volts | Applies to transmitter inputs, SEL A, SEL B, SD and $\overline{\text{LB}}$ |
| High level voltage output | 5.0 | | 15.0 | Volts | $R_L = 3\text{k}\Omega$ to GND |
| Low level voltage output | -15.0 | | -5.0 | Volts | $R_L = 3\text{k}\Omega$ to GND |
| Open circuit output | | | ± 15 | Volts | $R_L = \infty$ |
| Short circuit current | | | ± 100 | mA | $V_{OUT} = 0\text{V}$ |
| Power off impedance | 300 | | | Ω | $V_{CC} = 0\text{V}$; $V_{OUT} = \pm 2\text{V}$ |
| RS-232 Driver AC Characteristics | | | | | |
| Transmission rate | 120 | | | kbps | |
| Transition time | | | 1.56 | μs | Rise/fall time, 3V to -3V; -3V to 3V, $R_L = 3\text{k}\Omega$, $C_L = 2500\text{pF}$ |
| Propagation delay; t_{PHL} | | 2 | 4 | μs | $R_L = 3\text{k}\Omega$, $C_L = 2500\text{pF}$, from 1.5V of T_{IN} to 50% of V_{OUT} |
| Propagation delay; t_{PLH} | | 2 | 4 | μs | $R_L = 3\text{k}\Omega$, $C_L = 2500\text{pF}$, from 1.5V of T_{IN} to 50% of V_{OUT} |
| Slew rate | | 10 | 30 | V/ μs | $R_L = 3\text{k}\Omega$, $C_L = 50\text{pF}$; From 3V to -3V or -3V to 3V |

Electrical Characteristics (Continued)

Limits are specified at $T_A = 25^\circ\text{C}$ and $V_{CC} = 5.0\text{V}$ unless otherwise noted.

| Parameters | Min. | Typ. | Max. | Units | Conditions |
|---|------|------|------|---------------|---|
| RS-232 Receiver DC Characteristics | | | | | |
| TTL output level; V_{OL} | | | 0.4 | Volts | $I_{SINK} = 4\text{mA}$ |
| TTL output level; V_{OH} | 3.5 | | | Volts | $I_{SOURCE} = -4\text{mA}$ |
| Input high threshold | | 2.1 | 3.0 | Volts | |
| Input low threshold | 0.8 | 1.6 | | Volts | |
| Input voltage range | -15 | | 15 | Volts | |
| Input impedance | 3 | 5 | 7 | $k\Omega$ | $V_{IN} = \pm 15\text{V}$ |
| Hysteresis | 0.2 | 0.5 | 1.0 | Volts | $V_{CC} = 5\text{V}$ |
| RS-232 Receiver AC Characteristics | | | | | |
| Transmission rate | 120 | | | kbps | |
| Transition time | | 50 | | ns | Rise/fall time, 10% to 90% |
| Propagation delay t_{PHL} | | 100 | 300 | ns | From 50% of V_{IN} to 1.5V of R_{OUT} |
| Propagation delay t_{PLH} | | 100 | 200 | ns | |
| Power Requirements | | | | | |
| No load supply current | | 19 | 25 | mA | No load; $V_{CC} = 5.0\text{V}$; $T_A = 25^\circ\text{C}$ |
| Full load supply current | | 90 | 120 | mA | RS-232 drivers $R_L = 3k\Omega$ to GND, DC input RS-485 drivers $R_L = 54\Omega$ from A to B; DC input |
| Shutdown supply current | | 5 | 50 | μA | $T_A = 25^\circ\text{C}$, $V_{CC} = 5.0\text{V}$ |

NOTE

- Exceeding the maximum data rate may damage the device.

Test Circuits

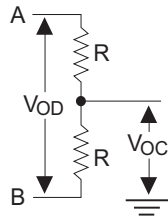


Figure 1: RS-485 Driver DC Test Load Circuit

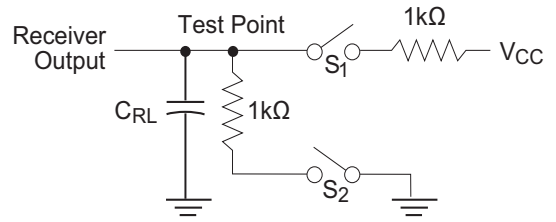


Figure 2: Receiver Timing Test Load Circuit

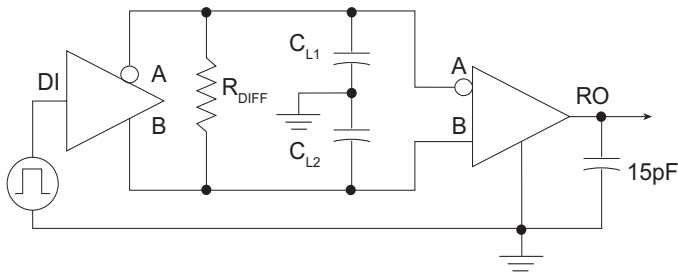


Figure 3: RS-485 Driver/Receiver Timing Test Circuit

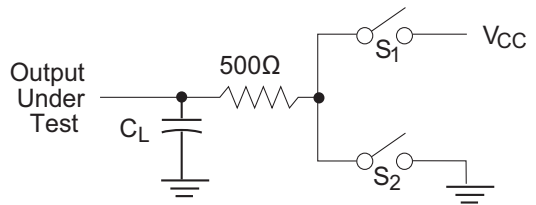


Figure 4: RS-485 Driver Timing Test Load #2 Circuit

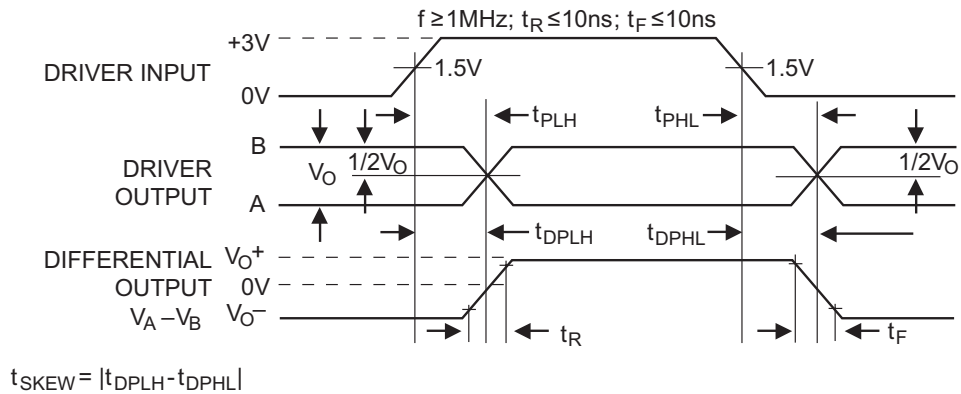


Figure 5: RS-485 Driver Propagation Delays

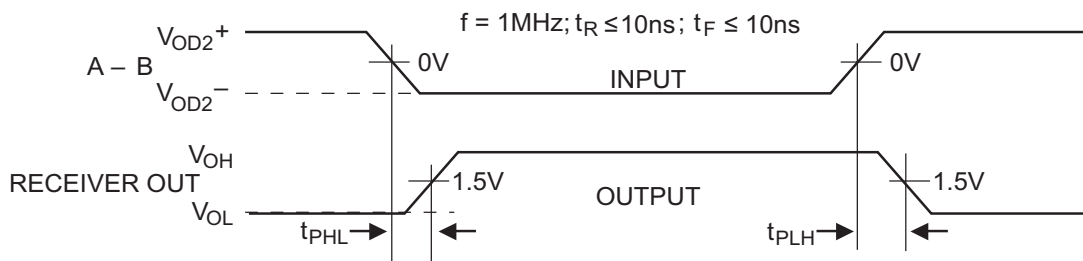
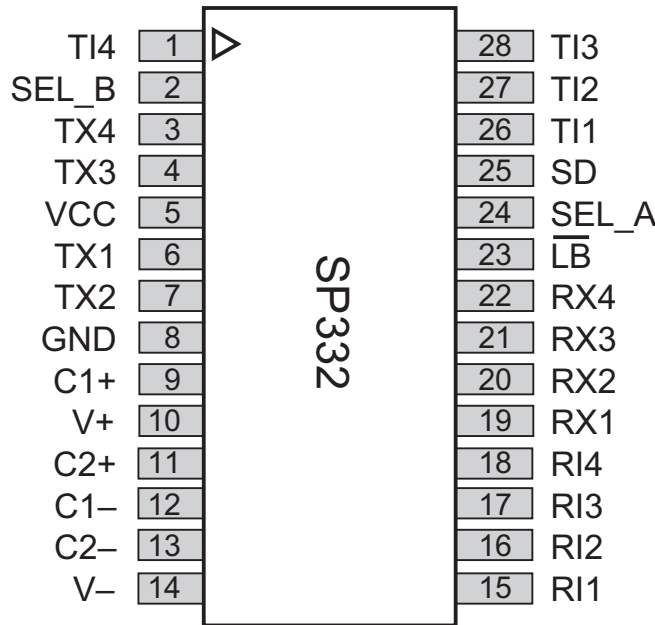


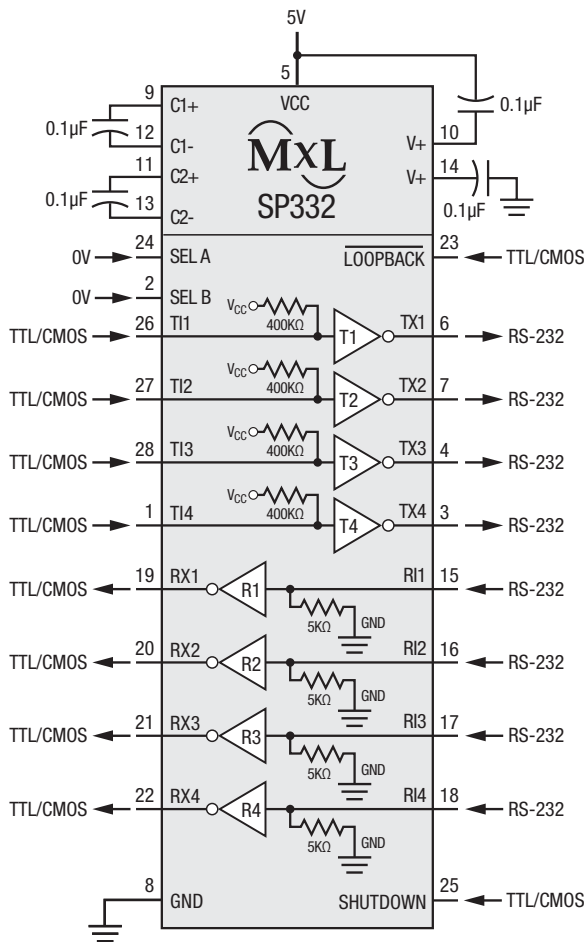
Figure 6: RS-485 Receiver Propagation Delays

Pin Configuration

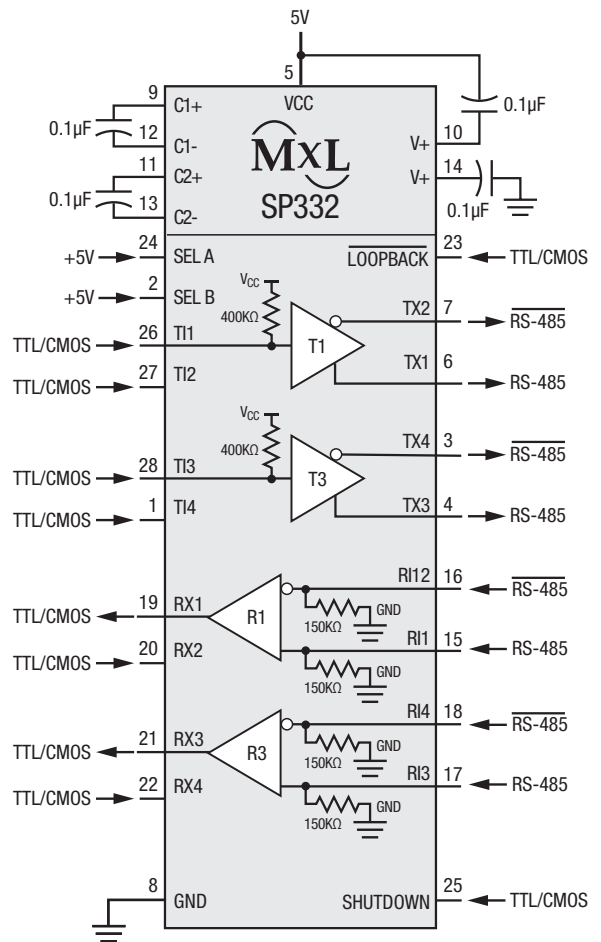


Typical Applications Circuits

RS-232 Mode



Full Duplex RS-485 Mode Mode



SP332 Control Logic Configuration

| | | | | |
|------------------------|---|---|---|---|
| SEL A | 0 | 0 | 1 | 1 |
| SEL B | 0 | 1 | 0 | 1 |
| $\overline{\text{LB}}$ | 1 | 1 | 1 | 1 |
| SD | 0 | 0 | 0 | 0 |
| | | | | |
| SEL A | 0 | 0 | 1 | 1 |
| SEL B | 0 | 1 | 0 | 1 |
| $\overline{\text{LB}}$ | 0 | 0 | 0 | 0 |
| SD | 0 | 0 | 0 | 0 |
| | | | | |

Receiver Inputs are inactive in Loopback Mode ($\overline{\text{LOOPBACK}} = 0$)

Driver Outputs are Tri-stated in Loopback Mode ($\overline{\text{LOOPBACK}} = 0$)

Unused Outputs are Tri-stated

Functional Description

The SP332 is single chip device that can be configured via software for either RS-232, RS-485 or both interface modes at any time. The SP332 is made up of three basic circuit elements, single-ended drivers and receivers, differential drivers and receivers and charge pump.

Differential Driver/Receiver

RS-485, RS-422 Drivers

The differential drivers and receivers comply with the RS-485 and RS-422 standards. The driver circuits are able to drive a minimum of 1.5V when terminated with a 54 Ω resistor across the two outputs. The typical propagation delay from driver input to output is 60ns. The driver outputs are current limited to less than 250mA, and can tolerate shorts to ground, or to any voltage within a 10V to -7V range with no damage.

RS-485, RS-422 Receivers

The differential receivers of the SP332 comply with the RS-485 and RS-422 standards. The input to the receiver is equipped with a common mode range of 12V to -7V. The input threshold over this range is a minimum of ± 200 mV. The differential receivers can receive data up to 10Mbps. The typical propagation delay from the receiver input to output is 90ns.

Single Ended Driver / Receiver

RS-232 (V.28) Drivers

The single-ended drivers and receivers comply with the RS-232 and V.28 standards. The drivers are inverting transmitters which accept either TTL or CMOS inputs and output the RS-232 signals with an inverted sense relative to the input logic levels. Typically, the RS-232 driver output voltage swing is ± 9 V with no load and is guaranteed to be greater than ± 5 V under full load. The drivers rely on the V+ and V- voltages generated by the on-chip charge pump to maintain proper RS-232 output levels. With worst case load conditions of 3k Ω and 2500pF, the four RS-232 drivers can still maintain ± 5 V output levels. The drivers can operate up to 120kbps; the propagation delay from input to output is typically 2 μ s.

RS-232 (V.28) Receivers

The RS-232 receivers convert RS-232 input signals to inverted TTL signals. Each of the four receivers features 500mV of hysteresis margin to minimize the affects of noisy transmission lines. The inputs also have a 5k Ω resistor to ground, in an open circuit situation the input of the receiver will be forced low, committing the output to a logic high state. The input resistance will maintain 3k Ω to

7k Ω over a ± 15 V range. The maximum operating voltage range for the receiver is ± 30 V, under these conditions the input current to the receiver must be limited to less than 100mA. Due to the on-chip ESD protection circuitry, the receiver inputs will be clamped to ± 15 V levels. The RS-232 receivers can operate up to 120kbps.

Charge-Pump

The charge pump is a MaxLinear-patented design (U.S. 5,306,954) and uses a unique approach compared to older less efficient designs. The charge pump still requires four external capacitors, but uses a four-phase voltage shifting technique to attain symmetrical 10V power supplies. Figure 7(a) shows the waveform found on the positive side of capacitor C₂, and Figure 7(b) shows the negative side of capacitor C₂. There is a free-running oscillator that controls the four phases of the voltage shifting. A description of each phase follows.

Phase 1 — V_{SS} charge storage

During this phase of the clock cycle, the positive side of capacitors C₁ and C₂ are initially charged to 5V. C₁⁺ is then switched to ground and charge on C₁⁻ is transferred to C₂⁻. Since C₂⁺ is connected to 5V, the voltage potential across capacitor C₂ is now 10V.

Phase 2 — V_{SS} transfer

Phase two of the clock connects the negative terminal of C₂ to the V_{SS} storage capacitor and the positive terminal of C₂ to ground, and transfers the generated -10V to C₃. Simultaneously, the positive side of capacitor C₁ is switched to 5V and the negative side is connected to ground.

Phase 3 — V_{DD} charge storage

The third phase of the clock is identical to the first phase — the charge transferred in C₁ produces -5V in the negative terminal of C₁, which is applied to the negative side of capacitor C₂. Since C₂⁺ is at +5V, the voltage potential across C₂ is 10V.

Phase 4 — V_{DD} transfer

The fourth phase of the clock connects the negative terminal of C₂ to ground and transfers the generated 10V across C₂ to C₄, the V_{DD} storage capacitor. Again, simultaneously with this, the positive side of capacitor C₁ is switched to 5V and the negative

side is connected to ground, and the cycle begins again.

Since both V^+ and V^- are separately generated from V_{CC} in a no-load condition, V^+ and V^- will be symmetrical. Older charge pump approaches that generate V^- from V^+ will show a decrease in the

magnitude of V^- compared to V^+ due to the inherent inefficiencies in the design.

The clock rate for the charge pump typically operates at 15kHz. The external capacitors must be 0.1 μ F with a 16V breakdown rating.

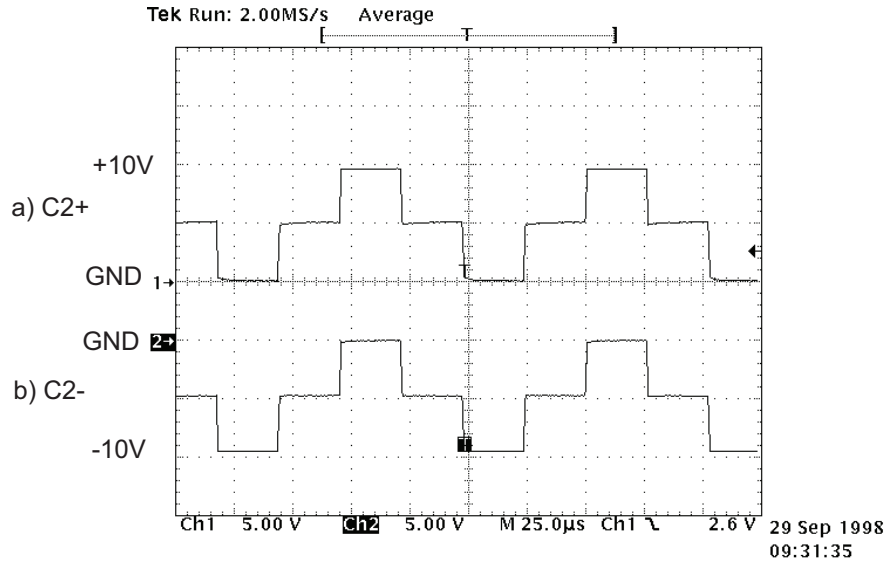


Figure 7: Charge Pump Waveforms

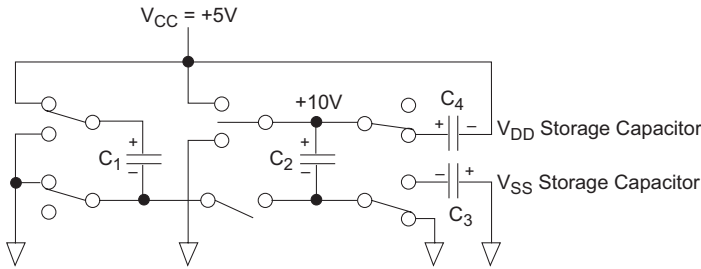


Figure 8: Charge Pump Phase 1

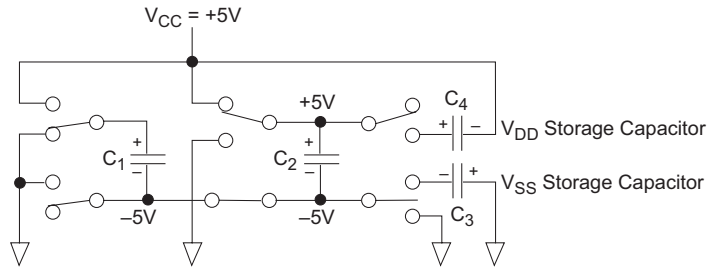


Figure 9: Charge Pump Phase 3

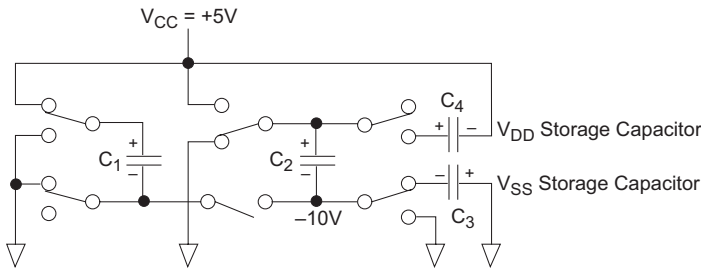


Figure 10: Charge Pump Phase 2

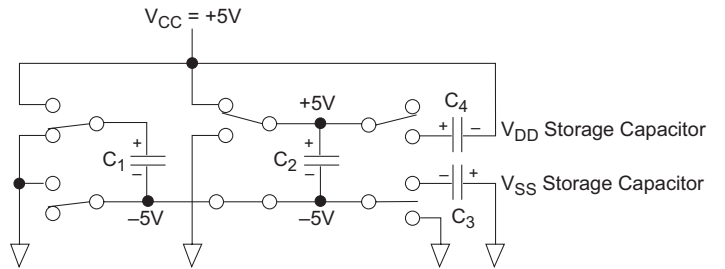
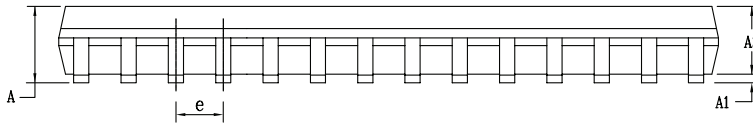
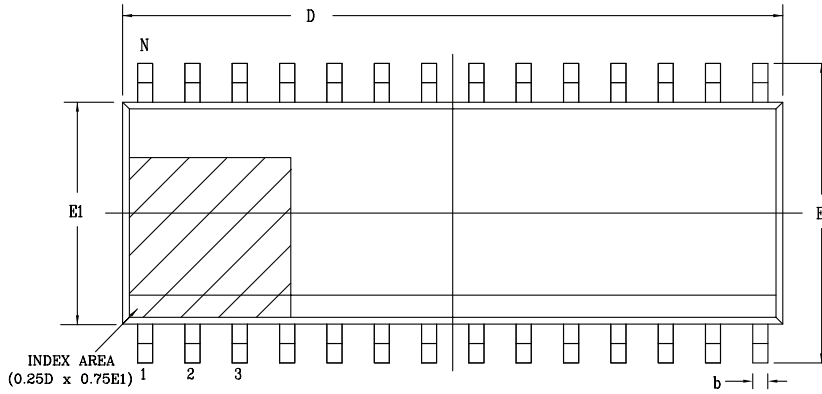


Figure 11: Charge Pump Phase 4

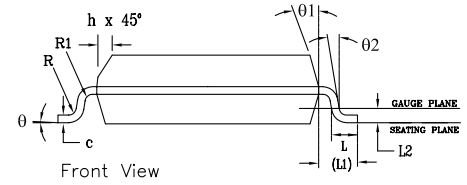
Package Description

WSOIC28

Top View



Side View



Front View

| PACKAGE OUTLINE SOIC .300" BODY JEDEC MS-013 VARIATION AE | | | | | | |
|--|---|-----|------|---|-----|-------|
| SYMBOLS | COMMON DIMENSIONS IN MM (Control Unit) | | | COMMON DIMENSIONS IN MM (Reference Unit) | | |
| | MIN | NOM | MAX | MIN | NOM | MAX |
| A | 2.35 | — | 2.65 | 0.093 | — | 0.104 |
| A1 | 0.10 | — | 0.30 | 0.004 | — | 0.012 |
| A2 | 2.05 | — | 2.55 | 0.081 | — | 0.100 |
| b | 0.31 | — | 0.51 | 0.012 | — | 0.020 |
| c | 0.20 | — | 0.33 | 0.008 | — | 0.013 |
| E | 10.30 BSC | | | 0.406 BSC | | |
| E1 | 7.50 BSC | | | 0.295 BSC | | |
| e | 1.27 BSC | | | 0.050 BSC | | |
| h | 0.25 | — | 0.75 | 0.010 | — | 0.030 |
| L | 0.40 | — | 1.27 | 0.016 | — | 0.050 |
| L1 | 1.40 REF | | | 0.055 REF | | |
| L2 | 0.25 BSC | | | 0.010 BSC | | |
| R | 0.07 | — | — | 0.003 | — | — |
| R1 | 0.07 | — | — | 0.003 | — | — |
| θ | 0° | — | 8° | 0° | — | 8° |
| $\theta1$ | 5° | — | 15° | 5° | — | 15° |
| $\theta2$ | 0° | — | — | 0° | — | — |
| D | 17.90 BSC | | | 0.705 BSC | | |
| N | 28 | | | 28 | | |

Drawing No: POD-00000106

Revision: A

Ordering Information⁽¹⁾

| Part Number | Operating Temperature Range | Lead-Free | Package | Packaging Method |
|-----------------------------|-----------------------------|--------------------|--------------|------------------|
| SP332CT-L | 0°C to 70°C | Yes ⁽²⁾ | 28-pin WSOIC | Tube |
| SP332CT-L/TR ⁽³⁾ | | | | Reel |
| SP332ET-L | -40°C to 85°C | | | Tube |
| SP332ET-L/TR | | | | Reel |

NOTE:

1. Refer to www.exar.com/SP332 for most up-to-date Ordering Information.
2. Visit www.exar.com for additional information on Environmental Rating.
3. NRND - Not recommended for new designs.

Revision History

| Revision | Date | Description |
|----------|-------|---|
| 9617RO | - | Legacy Sipex Datasheet |
| 01/26/10 | 1.0.0 | Convert to Exar Format. Add Revision History table. Change revision to 1.0.0. Add Note 1 and change maximum RS-485 data rate at +85C. Update ABS Max Rating table. |
| 10/16/17 | 1.0.1 | Remove GND from Differential Output Voltage min (page 2). Update to MaxLinear logo. Update format and ordering information table. Theory of Operation section moved to after SP332 Control Logic Configuration section, and renamed Functional Description. |



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