



# SNx5C3243 3-V To 5.5-V Multichannel RS-232 Compatible Line Driver and Receiver

## 1 Features

- Operates With 3-V to 5.5-V  $V_{CC}$  Supply
- Always-Active Noninverting Receiver Output (ROUT2B)
- Low Standby Current: 1  $\mu$ A Typical
- External Capacitors:  $4 \times 0.1 \mu$ F
- Accepts 5-V Logic Input With 3.3-V Supply
- Inter-Operable With SN65C3238, SN75C3238
- Supports Operation From 250 kbit/s to 1 Mbit/s
- RS-232 Bus-Pin ESD Protection Exceeds  $\pm 15$  kV Using Human-Body Model (HBM)

## 2 Applications

- [Battery-powered systems](#)
- [Personal electronics](#)
- [Notebooks](#)
- [Laptops](#)
- [Palmtop PCs](#)
- [Hand-held equipment](#)

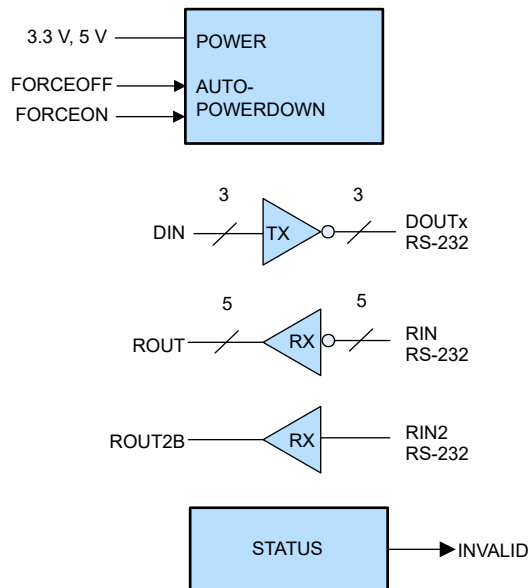
## 3 Description

The SN65C3243 and SN75C3243 consist of three line drivers, five line receivers, and a dual charge-pump circuit with  $\pm 15$ -kV ESD protection pin to pin (serial-port connection pins, including GND). This device provides the electrical interface between an asynchronous communication controller and the serial-port connector. The charge pump and four small external capacitors allow operation from a single 3-V to 5.5-V supply. In addition, this device includes an always-active noninverting output (ROUT2B), which allows applications using the ring indicator to transmit data while the device is powered down. The device operates at data signaling rates up to 1 Mbit/s and an increased slew-rate range of 24 V/ $\mu$ s to 150 V/ $\mu$ s.

### Package Information

PART NUMBER	PACKAGE <sup>(1)</sup>	BODY SIZE (NOM)
SN65C3243	SSOP (DB)	10.2 mm x 5.30 mm
	SOIC (DW)	17.9 mm x 7.50 mm
SN75C3243	TSSOP (PW)	9.70 mm x 4.40 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.



**Simplified Circuit**



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## 4 Revision History

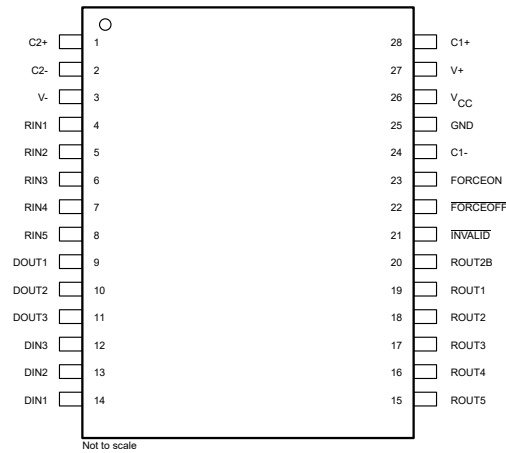
NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

### Changes from Revision H (September 2008) to Revision I (October 2022)

Page

- Added the *Device Information* table, *Pin Configuration and Functions* section, *ESD Ratings* table, *Thermal Information* table, *Detailed Description* section, *Device and Documentation Support*, and *Mechanical, Packaging, and Orderable Information* sections..... 1
- Changed the  $I_{CC}$  Supply current auto-powerdown disabled MAX value from 1 mA to 1.2 mA in the *Electrical Characteristics* ..... 5

## 5 Pin Configuration and Functions



**Figure 5-1. DB, DW, or PW Package, 28 Pin (SSOP, SOIC, TSSOP)  
(Top View)**

**Table 5-1. Pin Functions**

PIN		TYPE	DESCRIPTION
NO.	NAME		
1	C2+	—	Positive terminal of the voltage-doubler charge-pump capacitor
2	C2-	—	Negative terminal of the voltage-doubler charge-pump capacitor
3	V-		Negative charge pump output voltage
4	RIN1	I	RS-232 receiver inputs
5	RIN2		
6	RIN3		
7	RIN4		
8	RIN5		
9	DOUT1	O	RS-232 driver outputs
10	DOUT2		
11	DOUT3		
12	DIN3	I	Driver inputs
13	DIN2		
14	DIN1		
15	ROUT5	O	Receiver outputs
16	ROUT4		
17	ROUT3		
18	ROUT2		
19	ROUT1		
20	ROUT2B	—	Always-active noninverting receiver output;
21	INVALID	O	Invalid Output Pin
22	FORCEOFF	I	Auto Powerdown Control input (Refer to Truth Table)
23	FORCEON	I	Auto Powerdown Control input (Refer to Truth Table)
24	C1-	—	Negative terminal of the voltage-doubler charge-pump capacitor
25	GND	—	Ground
26	V <sub>CC</sub>	—	3-V to 5.5-V supply voltage
27	V+	—	Positive charge pump output voltage
28	C1+	—	Positive terminal of the voltage-doubler charge-pump capacitor

## 6 Specifications

### 6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted) <sup>(1)</sup>

		MIN	MAX	UNIT	
V <sub>CC</sub>	Supply voltage range <sup>(2)</sup>	-0.3	6	V	
V+	Positive-output supply voltage range <sup>(2)</sup>	-0.3	7	V	
V-	Negative-output supply voltage range <sup>(2)</sup>	0.3	-7	V	
V+ – V-	Supply voltage difference <sup>(2)</sup>		13	V	
V <sub>I</sub>	Input voltage range	Driver ( FORCEOFF, FORCEON)	-0.3	6	V
		Receiver	-25	25	
V <sub>O</sub>	Output voltage range	Driver	-13.2	13.2	V
T <sub>J</sub>	Operating virtual junction temperature		150	°C	
T <sub>stg</sub>	Storage temperature range	-65	150	°C	

- (1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) All voltages are with respect to network GND.

### 6.2 ESD Ratings

		VALUE	UNIT	
V <sub>(ESD)</sub>	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001 on RS-232 bus pins DOUT1/2/3, RIN1/2/3/4/5 <sup>(1)</sup>	±15	kV

- (1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process. .

### 6.3 Recommended Operating Conditions

see [Figure 7-6](#) <sup>(1)</sup>

		MIN	NOM	MAX	UNIT	
Supply voltage		V <sub>CC</sub> = 3.3 V	3	3.3	3.6	V
		V <sub>CC</sub> = 5 V	4.5	5	5.5	
V <sub>IH</sub>	Driver and control high-level input voltage	DIN, FORCEOFF, FORCEON	V <sub>CC</sub> = 3.3 V	2		V
			V <sub>CC</sub> = 5 V	2.4		
V <sub>IL</sub>	Driver and control low-level input voltage	DIN, FORCEOFF, FORCEON		0.8	V	
V <sub>I</sub>	Driver and control input voltage	DIN, FORCEOFF, FORCEON	0	5.5	V	
V <sub>I</sub>	Receiver input voltage		-25	25	V	
T <sub>A</sub>	Operating free-air temperature	SN65C3243	-40	85	°C	
		SN75C3243	0	70		

- (1) Test conditions are C1–C4 = 0.1 μF at V<sub>CC</sub> = 3.3 V ± 0.3 V; C1 = 0.047 μF, C2–C4 = 0.33 μF at V<sub>CC</sub> = 5 V ± 0.5 V.

## 6.4 Thermal Information

THERMAL METRIC <sup>(1)</sup>		DB (SSOP)	DW (SOIC)	PW (TSSOP)	UNIT
		28 PINS	28 PINS	28 PINS	
R <sub>θJA</sub>	Junction-to-ambient thermal resistance	76.1	59.0	70.3	°C/W
R <sub>θJC(top)</sub>	Junction-to-case (top) thermal resistance	35.8	28.8	21.0	°C/W
R <sub>θJB</sub>	Junction-to-board thermal resistance	37.4	30.3	29.2	°C/W
ψ <sub>JT</sub>	Junction-to-top characterization parameter	7.4	7.8	1.3	°C/W
ψ <sub>JB</sub>	Junction-to-board characterization parameter	37.0	30.0	28.8	°C/W
R <sub>θJC(bot)</sub>	Junction-to-case (bottom) thermal resistance	N/A	N/A	N/A	°C/W

(1) For more information about traditional and new thermal metrics, see the [Semiconductor and IC Package Thermal Metrics](#) application report.

## 6.5 Electrical Characteristics

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see [Figure 7-6](#))<sup>(2)</sup>

PARAMETER		TEST CONDITIONS	MIN	TYP <sup>(1)</sup>	MAX	UNIT
I <sub>I</sub>	Input leakage current	FORCEOFF, FORCEON		±0.01	±1	μA
I <sub>CC</sub>	Supply current	Auto-powerdown disabled	No load, FORCEOFF and FORCEON = V <sub>CC</sub> For DB and PW package	0.3	1.2	mA
		Auto-powerdown disabled	No load, FORCEOFF and FORCEON = V <sub>CC</sub> For DW package	0.3	1	mA
		Powered off	No load, FORCEOFF = GND	1	10	μA
		Auto-powerdown enabled	No load, FORCEOFF = V <sub>CC</sub> , FORCEON = GND, All RIN are open or grounded, All DIN are grounded	1	10	

(1) All typical values are at V<sub>CC</sub> = 3.3 V or V<sub>CC</sub> = 5 V, and T<sub>A</sub> = 25°C.

(2) Test conditions are C1–C4 = 0.1 μF at V<sub>CC</sub> = 3.3 V ± 0.3 V; C1 = 0.047 μF, C2–C4 = 0.33 μF at V<sub>CC</sub> = 5 V ± 0.5 V.

## 6.6 Electrical Characteristics, Driver Section

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see [Figure 7-6](#))

PARAMETER	TEST CONDITIONS <sup>(3)</sup>	MIN	TYP <sup>(1)</sup>	MAX	UNIT	
V <sub>OH</sub>	High-level output voltage	All DOUT at R <sub>L</sub> = 3 kΩ to GND	5	5.4	V	
V <sub>OL</sub>	Low-level output voltage	All DOUT at R <sub>L</sub> = 3 kΩ to GND	–5	–5.4	V	
V <sub>O</sub>	Output voltage (mouse driveability)	DIN1 = DIN2 = GND, DIN3 = V <sub>CC</sub> , 3-kΩ to GND at DOUT3, DOUT1 = DOUT2 = 2.5 mA	±5		V	
I <sub>IH</sub>	High-level input current	V <sub>I</sub> = V <sub>CC</sub>	±0.01	±1	μA	
I <sub>IL</sub>	Low-level input current	V <sub>I</sub> = GND	±0.01	±1	μA	
I <sub>OS</sub>	Short-circuit output current <sup>(2)</sup>	V <sub>CC</sub> = 3.6 V, V <sub>O</sub> = 0 V	±35	±60	mA	
		V <sub>CC</sub> = 5.5 V, V <sub>O</sub> = 0 V	±35	±90		
r <sub>o</sub>	Output resistance	V <sub>CC</sub> , V+, and V– = 0 V, V <sub>O</sub> = ±2 V	300	10M	Ω	
I <sub>off</sub>	Output leakage current	FORCEOFF = GND	V <sub>O</sub> = ±12 V, V <sub>CC</sub> = 3 V to 3.6 V		±25	μA
			V <sub>O</sub> = ±10 V, V <sub>CC</sub> = 4.5 V to 5.5 V		±25	

(1) All typical values are at V<sub>CC</sub> = 3.3 V or V<sub>CC</sub> = 5 V, and T<sub>A</sub> = 25°C.

(2) Short-circuit durations should be controlled to prevent exceeding the device absolute power dissipation ratings, and not more than one output should be shorted at a time.

(3) Test conditions are C1–C4 = 0.1 μF at V<sub>CC</sub> = 3.3 V ± 0.3 V; C1 = 0.047 μF, C2–C4 = 0.33 μF at V<sub>CC</sub> = 5 V ± 0.5 V.

## 6.7 Electrical Characteristics, Receiver Section

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see [Figure 7-6](#))

PARAMETER		TEST CONDITIONS <sup>(2)</sup>	MIN	TYP <sup>(1)</sup>	MAX	UNIT
V <sub>OH</sub>	High-level output voltage	I <sub>OH</sub> = -1 mA	V <sub>CC</sub> - 0.6	V <sub>CC</sub> - 0.1		V
V <sub>OL</sub>	Low-level output voltage	I <sub>OL</sub> = 1.6 mA			0.4	V
V <sub>IT+</sub>	Positive-going input threshold voltage	V <sub>CC</sub> = 3.3 V		1.6	2.4	V
		V <sub>CC</sub> = 5 V		1.9	2.4	
V <sub>IT-</sub>	Negative-going input threshold voltage	V <sub>CC</sub> = 3.3 V	0.6	1.1		V
		V <sub>CC</sub> = 5 V	0.8	1.4		
V <sub>hys</sub>	Input hysteresis (V <sub>IT+</sub> - V <sub>IT-</sub> )			0.5		V
I <sub>off</sub>	Output leakage current (except ROUT2B)	FORCEOFF = 0 V		±0.05	±10	μA
r <sub>i</sub>	Input resistance	V <sub>I</sub> = ±3 V to ±25 V	3	5	7	kΩ

(1) All typical values are at V<sub>CC</sub> = 3.3 V or V<sub>CC</sub> = 5 V, and T<sub>A</sub> = 25°C.

(2) Test conditions are C1–C4 = 0.1 μF at V<sub>CC</sub> = 3.3 V ± 0.3 V; C1 = 0.047 μF, C2–C4 = 0.33 μF at V<sub>CC</sub> = 5 V ± 0.5 V.

## 6.8 Electrical Characteristics, Auto-Powerdown Section

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see [Figure 7-5](#))

PARAMETER		TEST CONDITIONS	MIN	MAX	UNIT
V <sub>T+(valid)</sub>	Receiver input threshold for INVALID high-level output voltage	FORCEON = GND, FORCEOFF = V <sub>CC</sub>		2.7	V
V <sub>T-(valid)</sub>	Receiver input threshold for INVALID high-level output voltage	FORCEON = GND, FORCEOFF = V <sub>CC</sub>	-2.7		V
V <sub>T(invalid)</sub>	Receiver input threshold for INVALID low-level output voltage	FORCEON = GND, FORCEOFF = V <sub>CC</sub>	-0.3	0.3	V
V <sub>OH</sub>	INVALID high-level output voltage	I <sub>OH</sub> = -1 mA, FORCEON = GND, FORCEOFF = V <sub>CC</sub>	V <sub>CC</sub> - 0.6		V
V <sub>OL</sub>	INVALID low-level output voltage	I <sub>OL</sub> = 1.6 mA, FORCEON = GND, FORCEOFF = V <sub>CC</sub>		0.4	V

## 6.9 Switching Characteristics: Driver

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see [Figure 7-6](#))

PARAMETER		TEST CONDITIONS <sup>(3)</sup>		MIN	TYP <sup>(1)</sup>	MAX	UNIT	
Maximum data rate (see <a href="#">Figure 7-1</a> )	R <sub>L</sub> = 3 kΩ, One DOUT switching	C <sub>L</sub> = 1000 pF		250		kbit/s		
		C <sub>L</sub> = 250 pF,	V <sub>CC</sub> = 3 V to 4.5 V	1000				
		C <sub>L</sub> = 1000 pF,	V <sub>CC</sub> = 4.5 V to 5.5 V	1000				
t <sub>sk(p)</sub>	Pulse skew <sup>(2)</sup>	C <sub>L</sub> = 150 pF to 2500 pF,	R <sub>L</sub> = 3 kΩ to 7 kΩ,	See <a href="#">Figure 7-2</a>		25	ns	
SR(tr)	Slew rate, transition region (see <a href="#">Figure 7-1</a> )	C <sub>L</sub> = 150 pF to 1000 pF,	R <sub>L</sub> = 3 kΩ to 7 kΩ,	V <sub>CC</sub> = 3.3 V		18	150	V/μs

- (1) All typical values are at V<sub>CC</sub> = 3.3 V or V<sub>CC</sub> = 5 V, and T<sub>A</sub> = 25°C.
- (2) Pulse skew is defined as |t<sub>PLH</sub> – t<sub>PHL</sub>| of each channel of the same device.
- (3) Test conditions are C1–C4 = 0.1 μF at V<sub>CC</sub> = 3.3 V ± 0.3 V; C1 = 0.047 μF, C2–C4 = 0.33 μF at V<sub>CC</sub> = 5 V ± 0.5 V.

## 6.10 Switching Characteristics: Receiver

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS <sup>(3)</sup>		TYP <sup>(1)</sup>	UNIT
t <sub>PLH</sub>	Propagation delay time, low- to high-level output	C <sub>L</sub> = 150 pF, See <a href="#">Figure 7-3</a>		150	ns
t <sub>PHL</sub>	Propagation delay time, high- to low-level output	C <sub>L</sub> = 150 pF, See <a href="#">Figure 7-3</a>		150	ns
t <sub>en</sub>	Output enable time	C <sub>L</sub> = 150 pF, R <sub>L</sub> = 3 kΩ, See <a href="#">Figure 7-4</a>		200	ns
t <sub>dis</sub>	Output disable time	C <sub>L</sub> = 150 pF, R <sub>L</sub> = 3 kΩ, See <a href="#">Figure 7-4</a>		200	ns
t <sub>sk(p)</sub>	Pulse skew <sup>(2)</sup>	See <a href="#">Figure 7-3</a>		50	ns

- (1) All typical values are at V<sub>CC</sub> = 3.3 V or V<sub>CC</sub> = 5 V, and T<sub>A</sub> = 25°C.
- (2) Pulse skew is defined as |t<sub>PLH</sub> – t<sub>PHL</sub>| of each channel of the same device.
- (3) Test conditions are C1–C4 = 0.1 μF at V<sub>CC</sub> = 3.3 V ± 0.3 V; C1 = 0.047 μF, C2–C4 = 0.33 μF at V<sub>CC</sub> = 5 V ± 0.5 V.

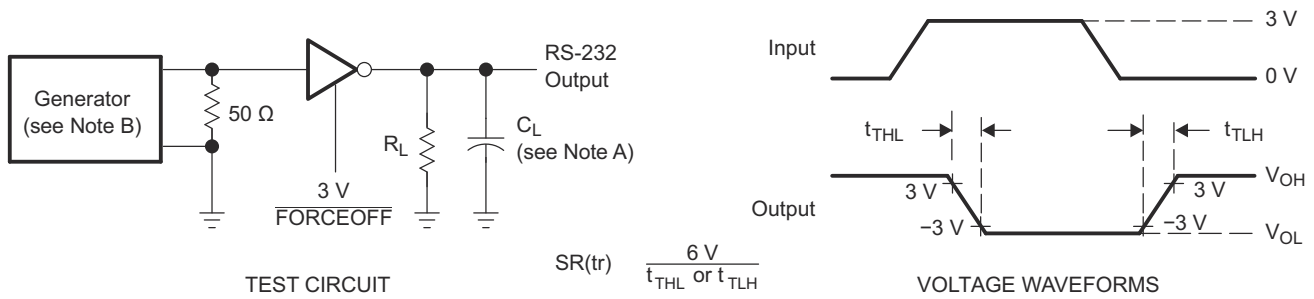
## 6.11 Switching Characteristics: Auto-Powerdown

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see [Figure 7-5](#))

PARAMETER		TYP <sup>(1)</sup>	UNIT
t <sub>valid</sub>	Propagation delay time, low- to high-level output	1	μs
t <sub>invalid</sub>	Propagation delay time, high- to low-level output	30	μs
t <sub>en</sub>	Supply enable time	100	μs

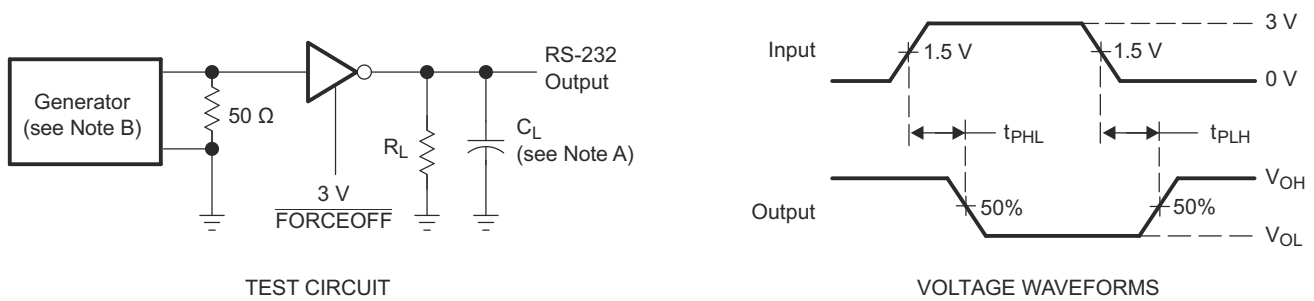
- (1) All typical values are at V<sub>CC</sub> = 3.3 V or V<sub>CC</sub> = 5 V, and T<sub>A</sub> = 25°C.

## 7 Parameter Measurement Information



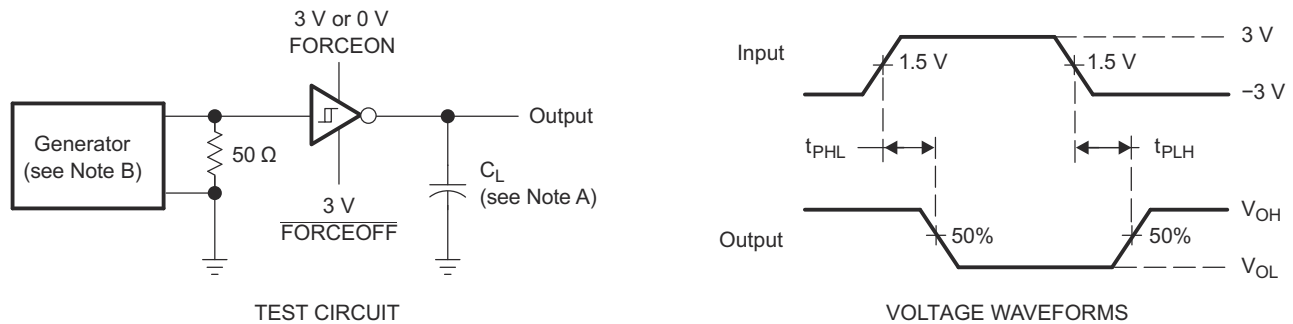
- A.  $C_L$  includes probe and jig capacitance.
- B. The pulse generator has the following characteristics: PRR = 1 Mbits,  $Z_0 = 50 \Omega$ , 50% duty cycle,  $t_r \leq 10 \text{ ns}$ ,  $t_f \leq 10 \text{ ns}$ .

**Figure 7-1. Driver Slew Rate**



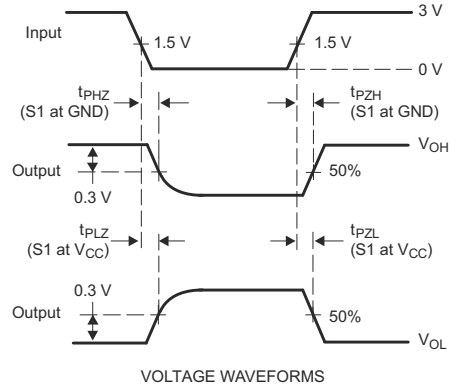
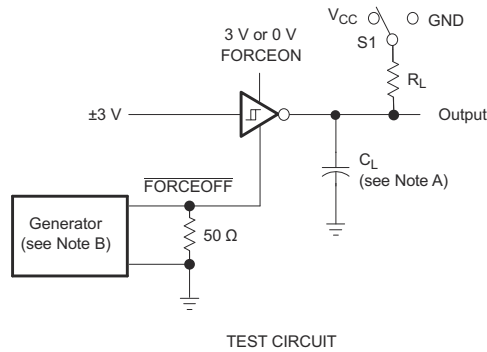
- A.  $C_L$  includes probe and jig capacitance.
- B. The pulse generator has the following characteristics: PRR = 1 Mbits,  $Z_0 = 50 \Omega$ , 50% duty cycle,  $t_r \leq 10 \text{ ns}$ ,  $t_f \leq 10 \text{ ns}$ .

**Figure 7-2. Driver Pulse Skew**



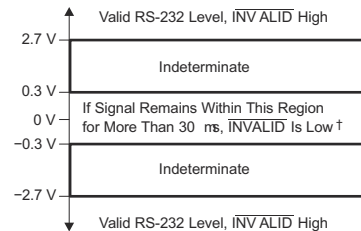
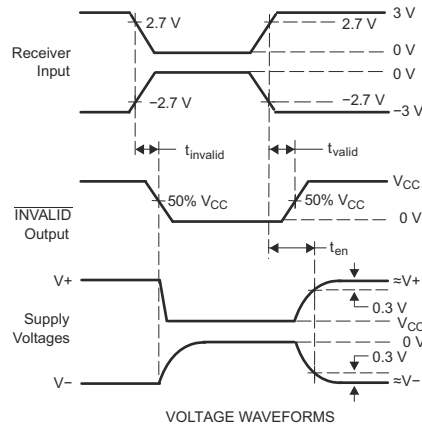
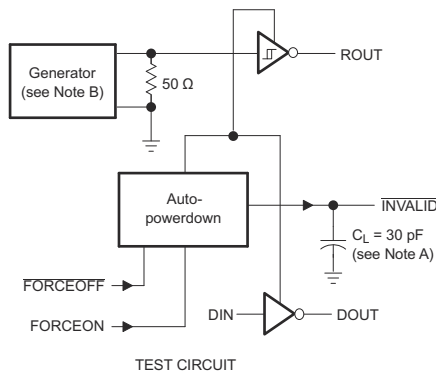
- A.  $C_L$  includes probe and jig capacitance.
- B. The pulse generator has the following characteristics:  $Z_0 = 50 \Omega$ , 50% duty cycle,  $t_r \leq 10 \text{ ns}$ ,  $t_f \leq 10 \text{ ns}$ .

**Figure 7-3. Receiver Propagation Delay Times**



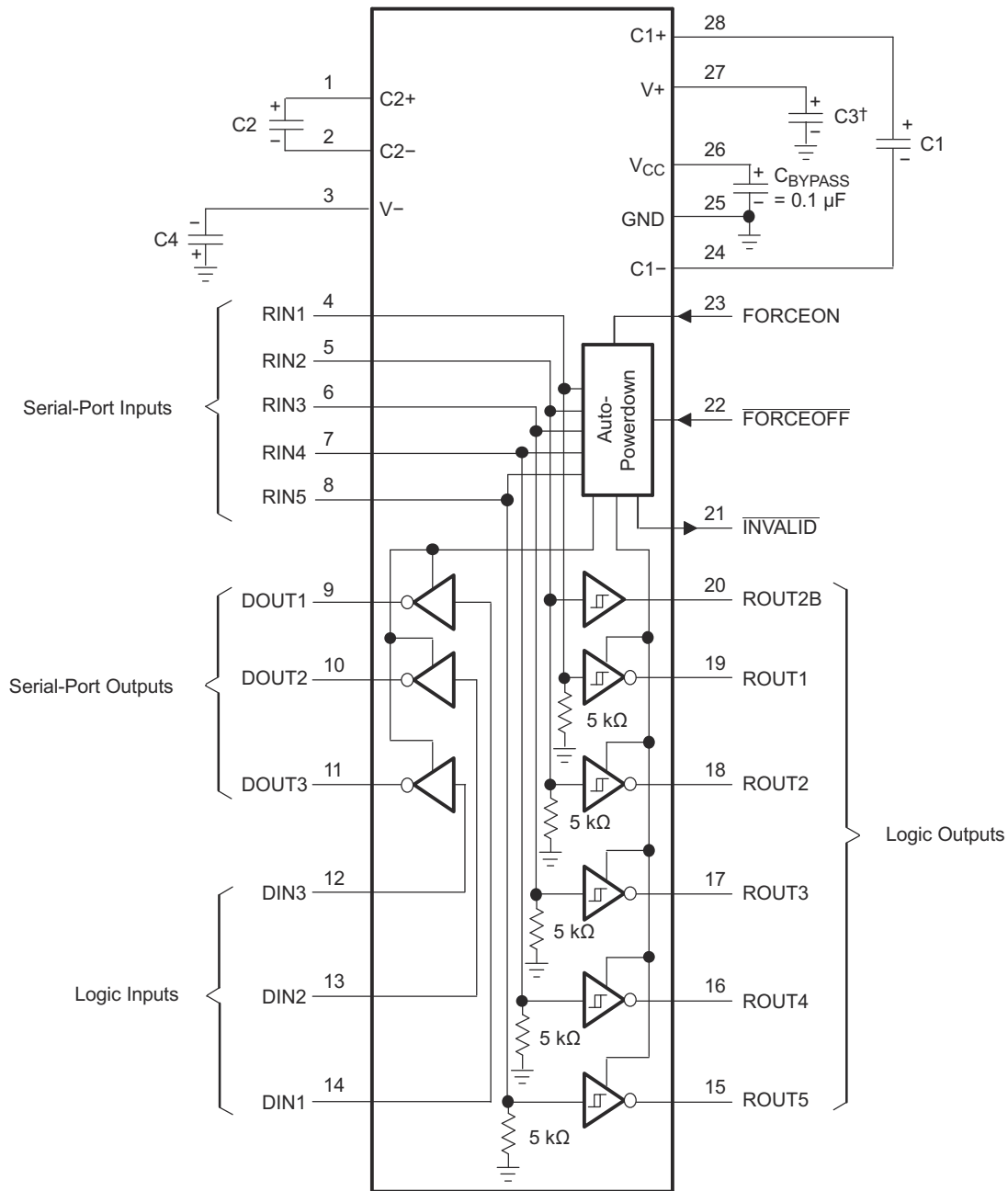
- A.  $C_L$  includes probe and jig capacitance.
- B. The pulse generator has the following characteristics:  $Z_O = 50 \Omega$ , 50% duty cycle,  $t_r \leq 10 \text{ ns}$ ,  $t_f \leq 10 \text{ ns}$ .
- C.  $t_{PLZ}$  and  $t_{PHZ}$  are the same as  $t_{dis}$ .
- D.  $t_{PZL}$  and  $t_{PZH}$  are the same as  $t_{en}$ .

Figure 7-4. Receiver Enable and Disable Times



- A.  $C_L$  includes probe and jig capacitance.
- B. The pulse generator has the following characteristics: PRR = 5 Mbits,  $Z_O = 50 \Omega$ , 50% duty cycle,  $t_r \leq 10 \text{ ns}$ ,  $t_f \leq 10 \text{ ns}$ .

Figure 7-5. INVALID Propagation Delay Times and Supply Enabling Time



† C3 can be connected to V<sub>CC</sub> or GND.

A. Resistor values shown are nominal.

**Figure 7-6. Typical Operating Circuit and Capacitor Values**

**Table 7-1. V<sub>CC</sub> vs Capacitor Values**

V <sub>CC</sub>	C1	C2, C3, and C4
3.3 V ± 0.3 V	0.1 μF	0.1 μF
5 V ± 0.5 V	0.047 μF	0.33 μF
3 V to 5.5 V	0.1 μF	0.47 μF

## 8 Detailed Description

### 8.1 Overview

Flexible control options for power management are available when the serial port is inactive. The auto-powerdown feature functions when FORCEON is low and FORCEOFF is high. During this mode of operation, if the device does not sense a valid RS-232 signal, the driver outputs are disabled. If FORCEOFF is set low, both drivers and receivers (except ROUT2B) are shut off, and the supply current is reduced to 1  $\mu$ A. Disconnecting the serial port or turning off the peripheral drivers causes the auto-powerdown condition to occur.

Auto-powerdown can be disabled when FORCEON and FORCEOFF are high and should be done when driving a serial mouse. With auto-powerdown enabled, the device is activated automatically when a valid signal is applied to any receiver input. The INVALID output is used to notify the user if an RS-232 signal is present at any receiver input. INVALID is high (valid data) if any receiver input voltage is greater than 2.7 V or less than -2.7 V or has been between -0.3 V and 0.3 V for less than 30  $\mu$ s. INVALID is low (invalid data) if all receiver input voltages are between -0.3 V and 0.3 V for more than 30  $\mu$ s. Refer to Figure 7-5 for receiver input levels.

### 8.2 Device Functional Modes

#### 8.2.1 Function Tables

Each Driver, DIN<sup>(1)</sup>

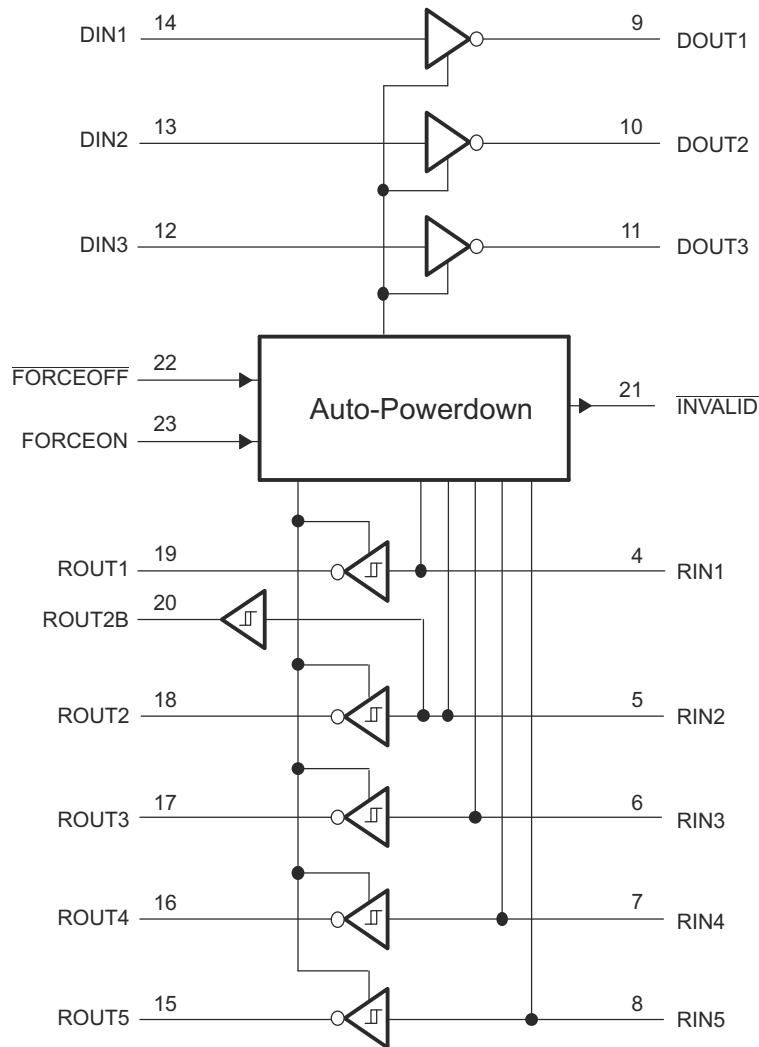
INPUTS				OUTPUT DOUT	DRIVER STATUS
DIN	FORCEON	FORCEOFF	VALID RIN RS-232 LEVEL		
X	X	L	X	Z	Powered off
L	H	H	X	H	Normal operation with auto-powerdown disabled
H	H	H	X	L	
L	L	H	Yes	H	Normal operation with auto-powerdown enabled
H	L	H	Yes	L	
L	L	H	No	Z	Powered off by auto-powerdown feature
H	L	H	No	Z	

(1) H = high level, L = low level, X = irrelevant, Z = high impedance

Each Receiver, RIN<sup>(1)</sup>

INPUTS				OUTPUTS			RECEIVER STATUS
RIN2	RIN1, RIN3–RIN5	FORCEOFF	VALID RIN RS-232 LEVEL	ROUT2B	ROUT2	ROUT1, ROUT3–5	
L	X	L	X	L	Z	Z	Powered off while ROUT2B is active
H	X	L	X	H	Z	Z	
L	L	H	YES	L	H	H	Normal operation with auto-powerdown disabled/enabled
L	H	H	YES	L	L	L	
H	L	H	YES	H	H	H	
H	H	H	YES	H	L	L	
Open	Open	H	YES	L	H	H	

(1) H = high level, L = low level, X = irrelevant, Z = high impedance (off), Open = input disconnected or connected driver off



**Figure 8-1. Logic Diagram (Positive Logic)**

## 9 Device and Documentation Support

### 9.1 Device Support

### 9.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on [ti.com](http://ti.com). Click on *Subscribe to updates* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

### 9.3 Support Resources

[TI E2E™ support forums](#) are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's [Terms of Use](#).

### 9.4 Trademarks

TI E2E™ is a trademark of Texas Instruments.  
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### 9.5 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

### 9.6 Glossary

[TI Glossary](#) This glossary lists and explains terms, acronyms, and definitions.

## 10 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

## PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
SN65C3243DBR	ACTIVE	SSOP	DB	28	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	65C3243	<a href="#">Samples</a>
SN65C3243DW	ACTIVE	SOIC	DW	28	20	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	65C3243	<a href="#">Samples</a>
SN65C3243DWR	ACTIVE	SOIC	DW	28	1000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	65C3243	<a href="#">Samples</a>
SN65C3243PWR	ACTIVE	TSSOP	PW	28	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	CB3243	<a href="#">Samples</a>
SN75C3243DBR	ACTIVE	SSOP	DB	28	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	75C3243	<a href="#">Samples</a>
SN75C3243DW	ACTIVE	SOIC	DW	28	20	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	75C3243	<a href="#">Samples</a>
SN75C3243DWR	ACTIVE	SOIC	DW	28	1000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	75C3243	<a href="#">Samples</a>
SN75C3243PWR	ACTIVE	TSSOP	PW	28	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	CA3243	<a href="#">Samples</a>

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSELETE:** TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

<sup>(6)</sup> Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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**TAPE AND REEL INFORMATION**

**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**

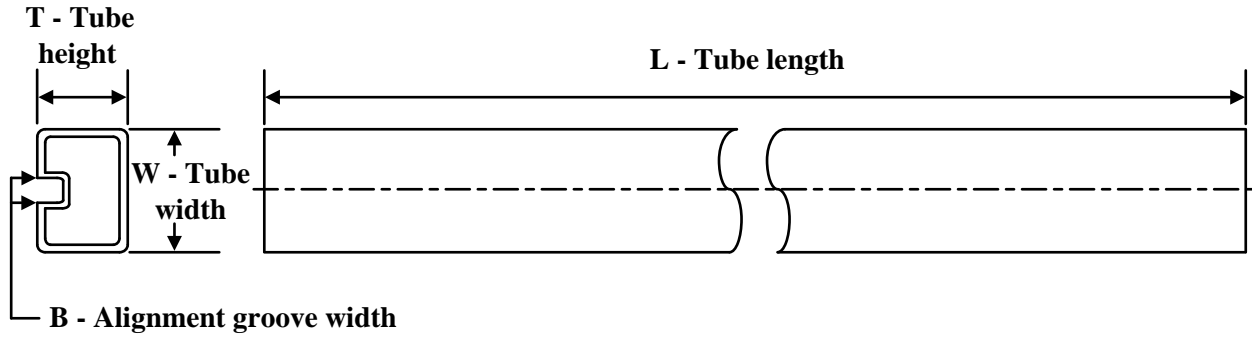

\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN65C3243DBR	SSOP	DB	28	2000	330.0	16.4	8.2	10.5	2.5	12.0	16.0	Q1
SN65C3243DWR	SOIC	DW	28	1000	330.0	32.4	11.35	18.67	3.1	16.0	32.0	Q1
SN65C3243PWR	TSSOP	PW	28	2000	330.0	16.4	6.9	10.2	1.8	12.0	16.0	Q1
SN75C3243DBR	SSOP	DB	28	2000	330.0	16.4	8.2	10.5	2.5	12.0	16.0	Q1
SN75C3243DWR	SOIC	DW	28	1000	330.0	32.4	11.35	18.67	3.1	16.0	32.0	Q1
SN75C3243PWR	TSSOP	PW	28	2000	330.0	16.4	6.9	10.2	1.8	12.0	16.0	Q1

**TAPE AND REEL BOX DIMENSIONS**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN65C3243DBR	SSOP	DB	28	2000	356.0	356.0	35.0
SN65C3243DWR	SOIC	DW	28	1000	350.0	350.0	66.0
SN65C3243PWR	TSSOP	PW	28	2000	356.0	356.0	35.0
SN75C3243DBR	SSOP	DB	28	2000	356.0	356.0	35.0
SN75C3243DWR	SOIC	DW	28	1000	350.0	350.0	66.0
SN75C3243PWR	TSSOP	PW	28	2000	356.0	356.0	35.0

**TUBE**


\*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (μm)	B (mm)
SN65C3243DW	DW	SOIC	28	20	506.98	12.7	4826	6.6
SN75C3243DW	DW	SOIC	28	20	506.98	12.7	4826	6.6

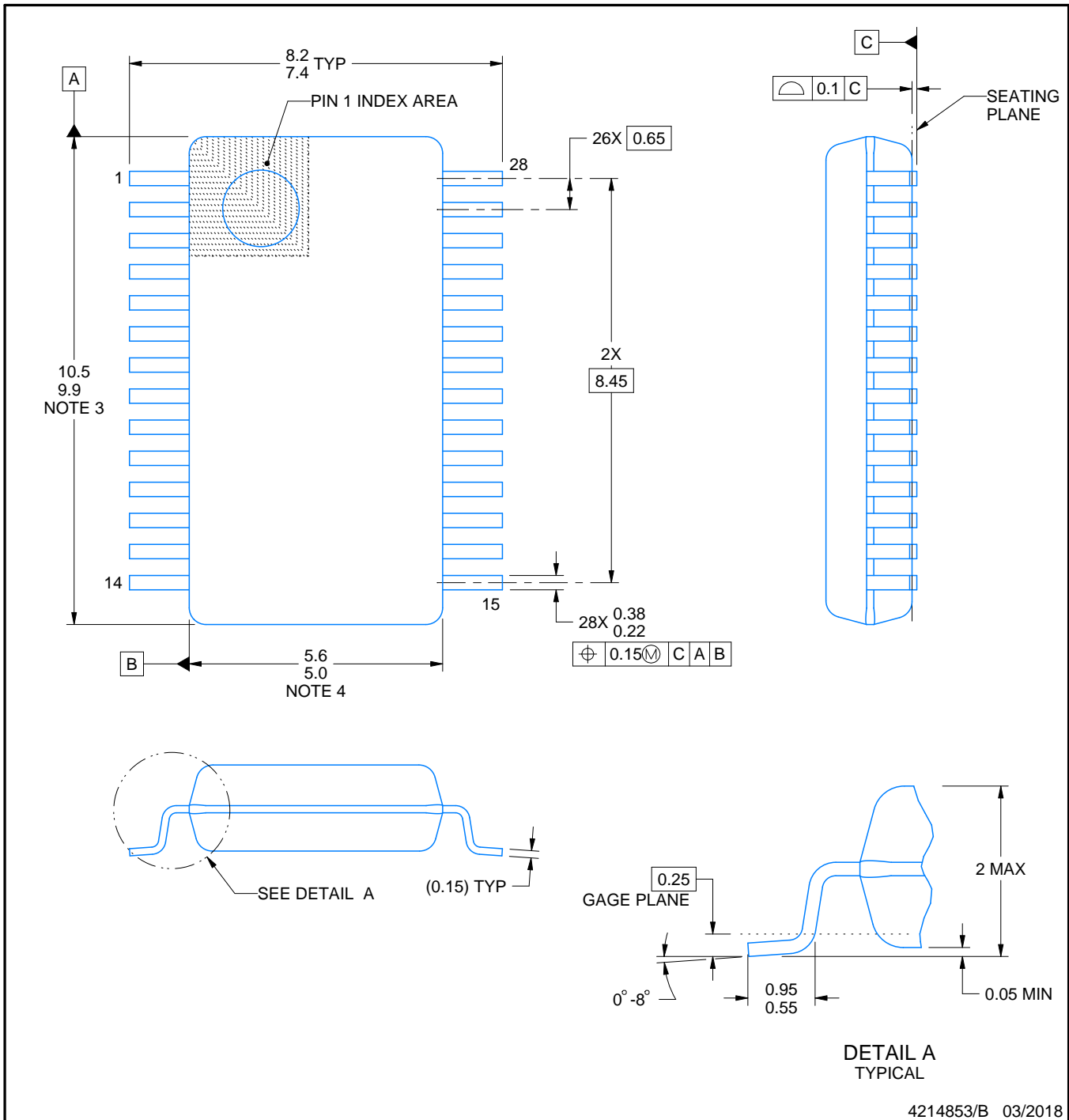
# DB0028A



# PACKAGE OUTLINE

## SSOP - 2 mm max height

SMALL OUTLINE PACKAGE



4214853/B 03/2018

### NOTES:

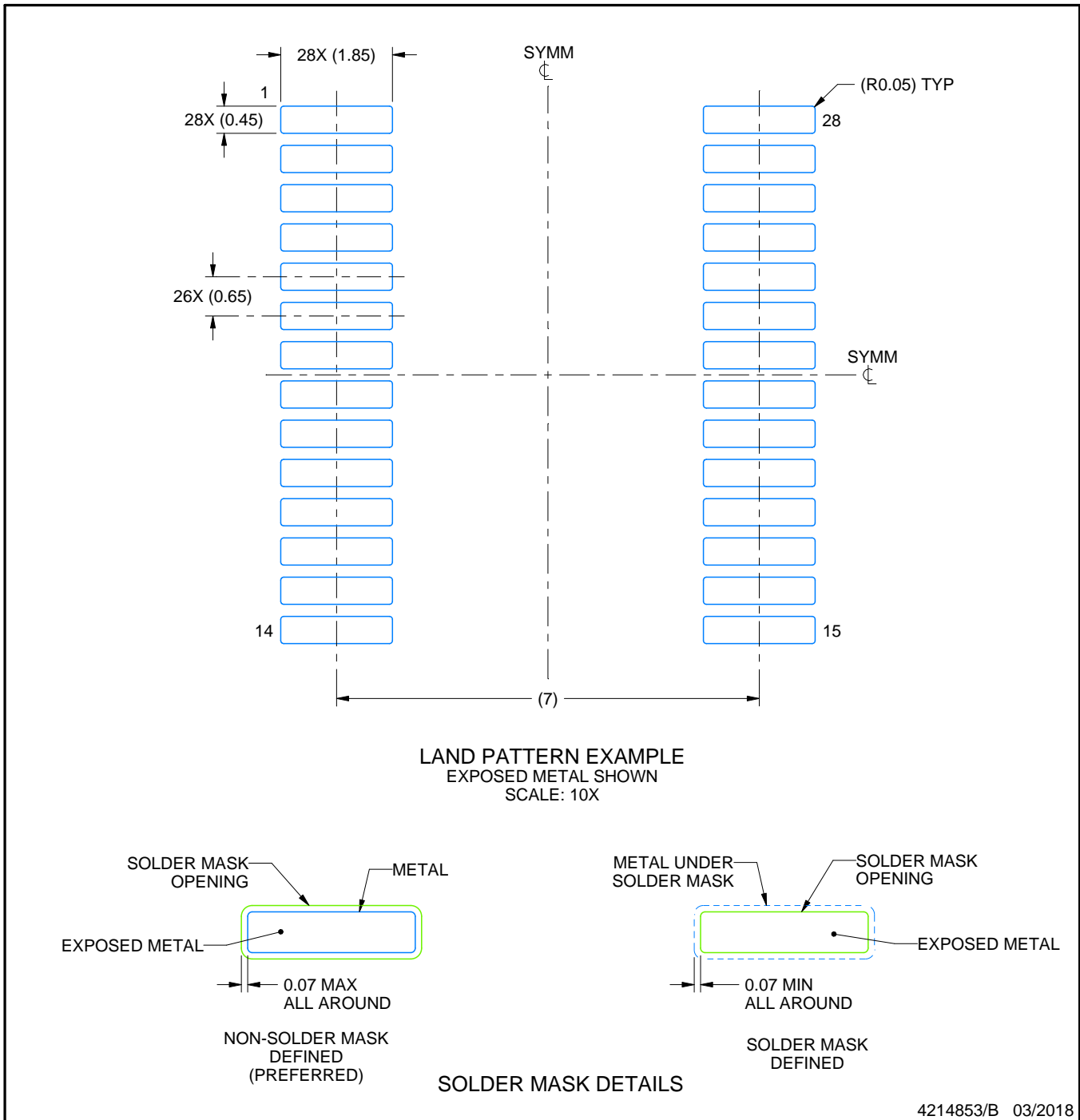
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-150.

# EXAMPLE BOARD LAYOUT

DB0028A

SSOP - 2 mm max height

SMALL OUTLINE PACKAGE



NOTES: (continued)

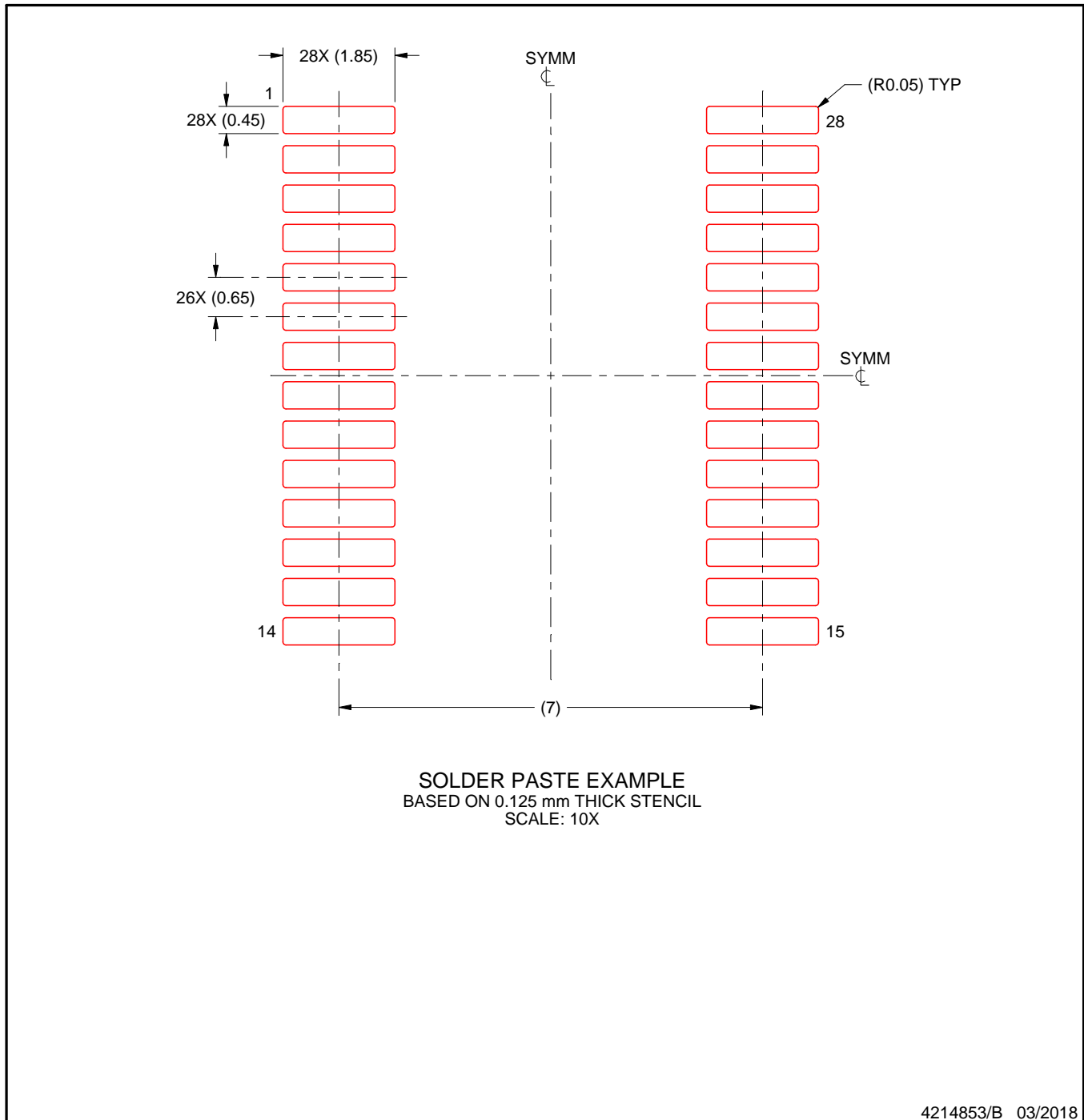
- 6. Publication IPC-7351 may have alternate designs.
- 7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

# EXAMPLE STENCIL DESIGN

DB0028A

SSOP - 2 mm max height

SMALL OUTLINE PACKAGE



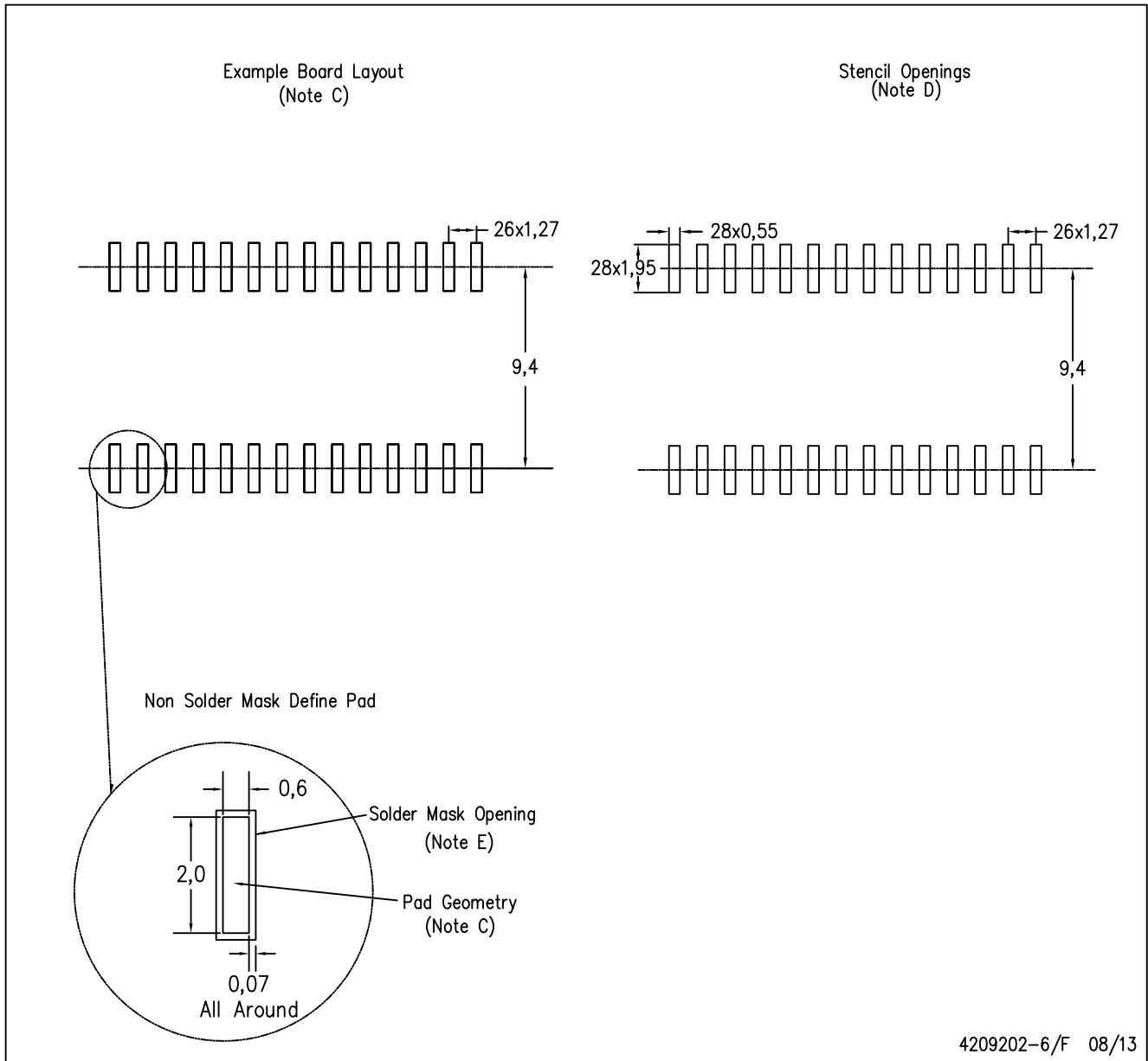
NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.



DW (R-PDSO-G28)

PLASTIC SMALL OUTLINE



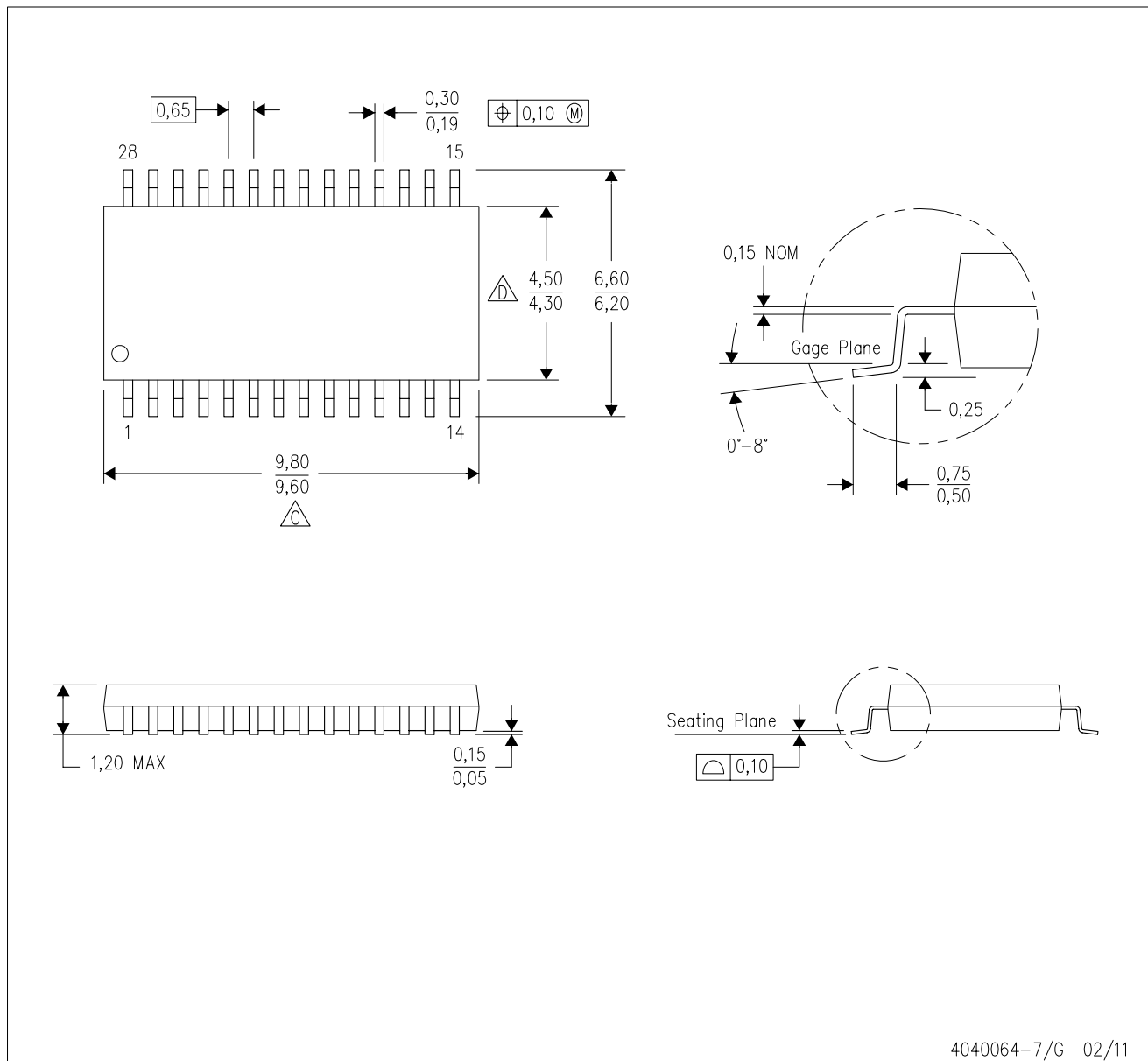
4209202-6/F 08/13

- NOTES:
- A. All linear dimensions are in millimeters.
  - B. This drawing is subject to change without notice.
  - C. Refer to IPC7351 for alternate board design.
  - D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525
  - E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.



# MECHANICAL DATA

PW (R-PDSO-G28)

PLASTIC SMALL OUTLINE

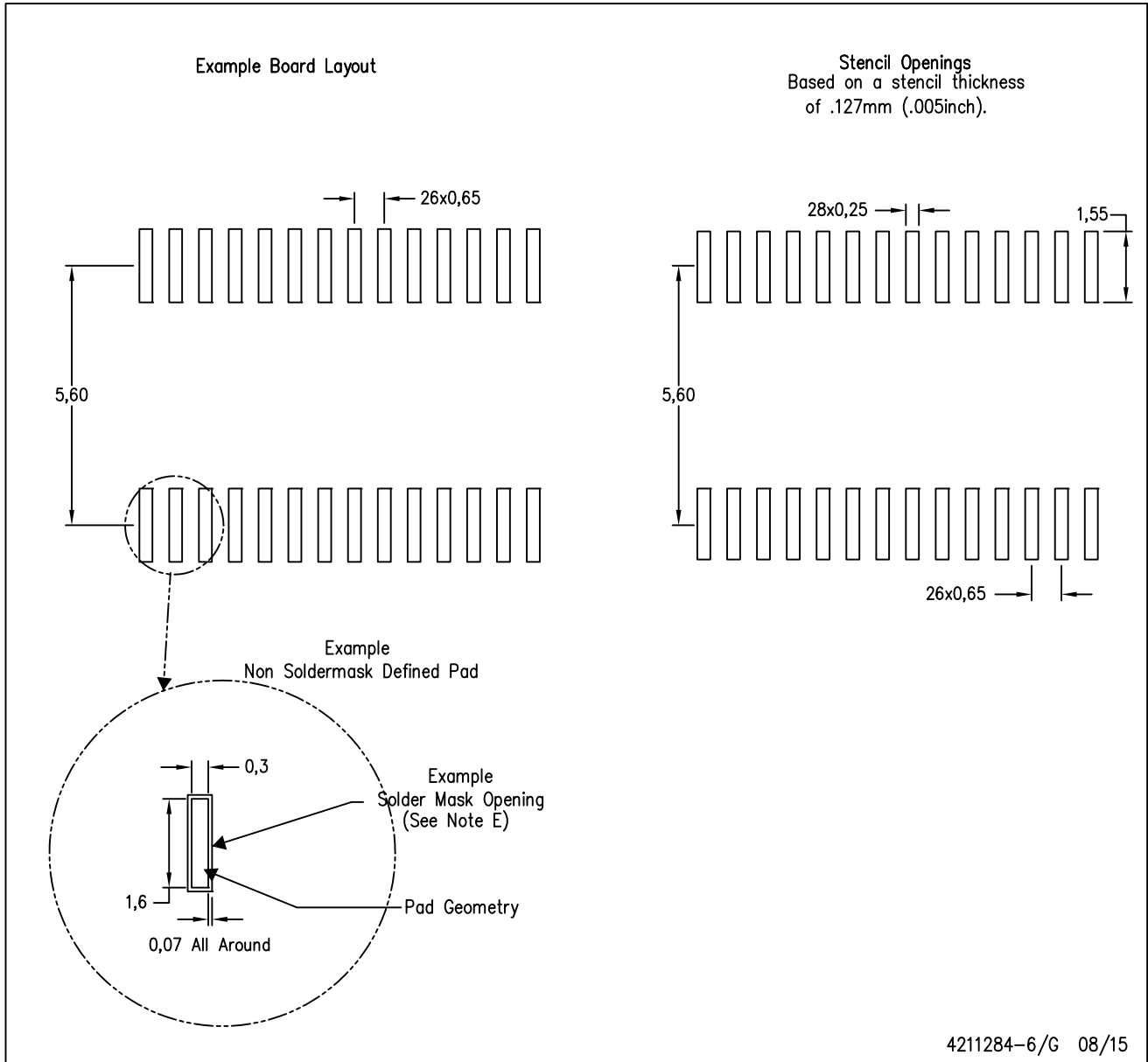


4040064-7/G 02/11

- NOTES:
- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
  - B. This drawing is subject to change without notice.
  -  Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0,15 each side.
  -  Body width does not include interlead flash. Interlead flash shall not exceed 0,25 each side.
  - E. Falls within JEDEC MO-153

PW (R-PDSO-G28)

PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in millimeters.
  - B. This drawing is subject to change without notice.
  - C. Publication IPC-7351 is recommended for alternate design.
  - D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
  - E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

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