



**THE DATASHEET OF
SN74LVC1G99DCURG4**



Ultra-Configurable Multiple-Function Gate With 3-State Output

Check for Samples: [SN74LVC1G99](#)

FEATURES

- Available in Texas Instruments NanoFree™ Package
- Supports 5-V V_{CC} Operation
- Inputs Accept Voltages to 5.5 V
- Supports Down Translation to V_{CC}
- Max t_{pd} of 6.7 ns at 3.3 V
- Low Power Consumption, 10- μ A Max I_{CC}
- ± 24 -mA Output Drive at 3.3 V
- Offers Nine Different Logic Functions in a Single Package
- I_{off} Supports Live Insertion, Partial-Power-Down Mode, and Back-Drive Protection
- Input Hysteresis Allows for Slow Input Transition Time and Better Noise Immunity at Input
- Latch-Up Performance Exceeds 100 mA Per JESD 78, Class II
- ESD Protection Exceeds JESD 22
 - 2000-V Human-Body Model (A114-A)
 - 200-V Machine Model (A115-A)
 - 1000-V Charged-Device Model (C101)

DESCRIPTION

The SN74LVC1G99 device is operational from 1.65 V to 5.5 V.

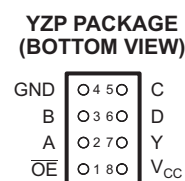
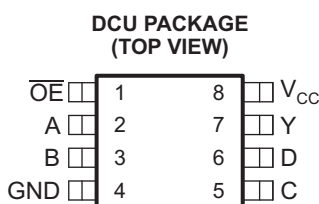
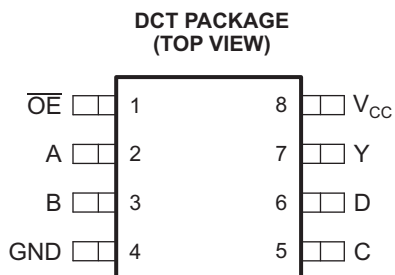
The SN74LVC1G99 device features configurable multiple functions with a 3-state output. The output is disabled when the output-enable (\overline{OE}) input is high. When \overline{OE} is low, the output state is determined by 16 patterns of 4-bit input. The user can choose logic functions, such as MUX, AND, OR, NAND, NOR, XOR, XNOR, inverter, and buffer. All inputs can be connected to V_{CC} or GND.

This device functions as an independent inverter, but because of Schmitt action, it has different input threshold levels for positive-going (V_{T+}) and negative-going (V_{T-}) signals.

To ensure the high-impedance state during power up or power down, \overline{OE} should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

This device is fully specified for partial-power-down applications using I_{off} . The I_{off} circuitry disables the outputs, preventing damaging current backflow through the device when it is powered down.

NanoFree™ package technologies are a major breakthrough in IC packaging concepts, using the die as the package.



See mechanical drawings for dimensions.



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

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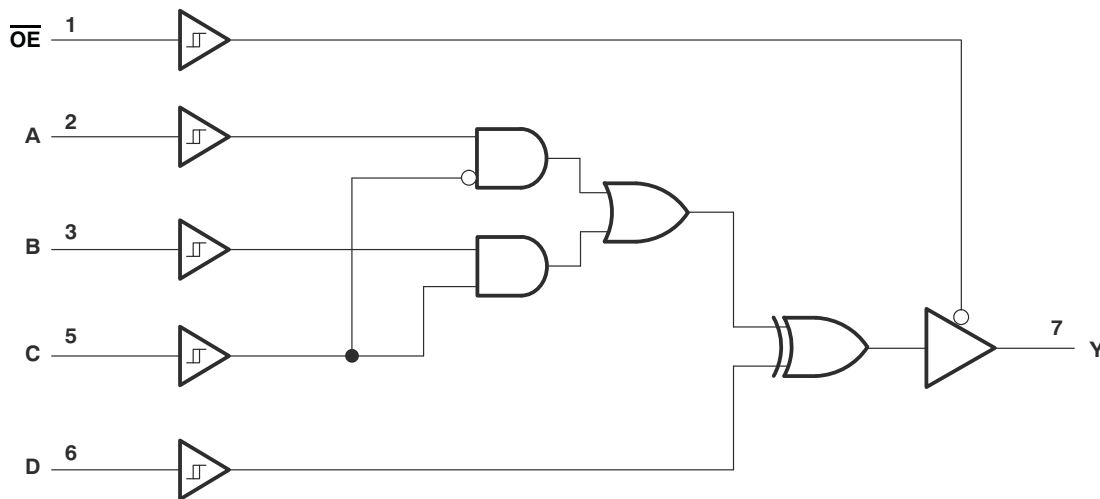


These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

Function Table

INPUTS						OUTPUT
\overline{OE}	D	C	B	A	Y	
L	L	L	L	L	L	
L	L	L	L	H	H	
L	L	L	H	L	L	
L	L	L	H	H	H	
L	L	H	L	L	L	
L	L	H	L	H	L	
L	L	H	H	L	H	
L	L	H	H	H	H	
L	H	L	L	L	H	
L	H	L	L	H	L	
L	H	L	H	L	H	
L	H	L	H	H	L	
L	H	H	L	L	H	
L	H	H	L	H	H	
L	H	H	H	L	L	
L	H	H	H	H	L	
H	H or L	H or L	H or L	H or L	Z	

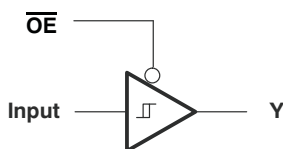
Logic Diagram (Positive Logic)



Function Selection Table

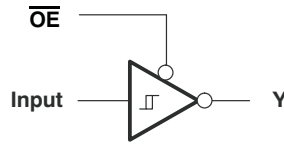
PRIMARY FUNCTION	COMPLEMENTARY FUNCTION	PAGE
3-state buffer		3
3-state inverter		3
3-state 2-in-1 data selector MUX		4
3-state 2-in-1 data selector MUX, inverted out		4
3-state 2-input AND	3-state 2-input NOR, both inputs inverted	5
3-state 2-input AND, one input inverted	3-state 2-input NOR, one input inverted	5
3-state 2-input AND, both inputs inverted	3-state 2-input NOR	5
3-state 2-input NAND	3-state 2-input OR, both inputs inverted	6
3-state 2-input NAND, one input inverted	3-state 2-input OR, one input inverted	6
3-state 2-input NAND, both inputs inverted	3-state 2-input OR	6
3-state 2-input XOR		7
3-state 2-input XNOR	3-state 2-input XOR, one input inverted	7

3-State Buffer Functions Available



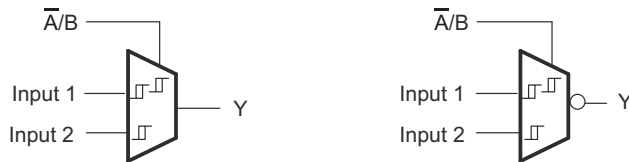
FUNCTION	\overline{OE}	A	B	C	D
3-state buffer	L	Input	H or L	L	L
		H or L	Input	H	L
		L	H	Input	L
		H	L	Input	H
		H	H or L	L	Input
		H or L	L	H	Input
		L	L	H or L	Input

3-State Inverter Functions Available



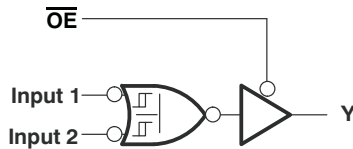
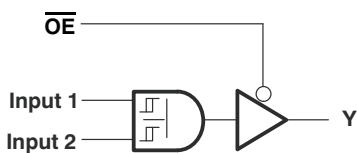
FUNCTION	\overline{OE}	A	B	C	D
3-state buffer	L	Input	H or L	L	H
		X	Input	H	H
		L	H	Input	H
		H	L	Input	L
		H	H or L	L	Input
		H or L	H	H	Input
		H	H	H or L	Input

3-State MUX Functions Available

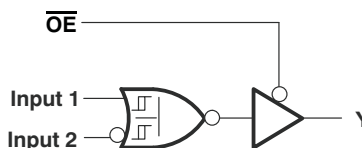
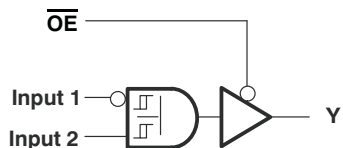


FUNCTION	\overline{OE}	A	B	C	D
3-state 2-to-1, data selector MUX	L	Input 1	Input 2	$\overline{\text{Input 1}}$ or Input 2	L
3-state 2-to-1, data selector MUX		Input 2	Input 1	$\overline{\text{Input 2}}$ or Input 1	L
3-state 2-to-1, data selector MUX, inverted out		Input 1	Input 2	$\overline{\text{Input 1}}$ or Input 2	H
3-state 2-to-1, data selector MUX, inverted out		Input 2	Input 1	$\overline{\text{Input 2}}$ or Input 1	H

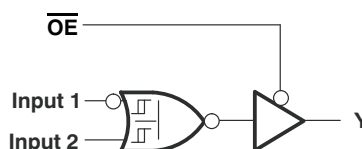
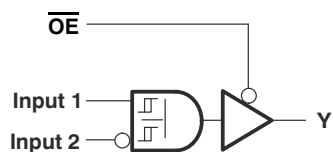
3-State AND/NOR/OR Functions Available



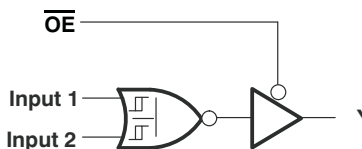
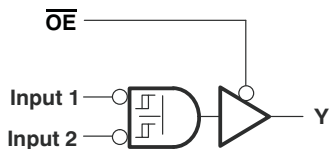
NO. OF INPUTS	AND/NAND FUNCTION	OR/NOR FUNCTION	\overline{OE}	A	B	C	D
2	3-state AND	3-state NOR	L	L	Input 1	Input 2	L
2	3-state AND	3-state NOR		L	Input 2	Input 1	L



NO. OF INPUTS	AND/NAND FUNCTION	OR/NOR FUNCTION	\overline{OE}	A	B	C	D
2	3-state AND	3-state NOR	L	Input 2	L	Input 1	L
2	3-state AND	3-state NOR		H	Input 1	Input 2	H

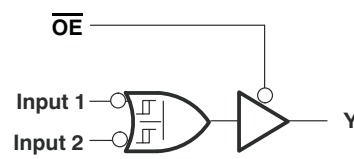
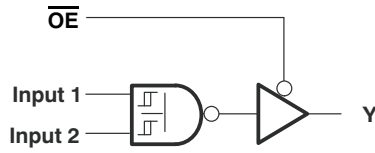


NO. OF INPUTS	AND/NAND FUNCTION	OR/NOR FUNCTION	\overline{OE}	A	B	C	D
2	3-state AND	3-state NOR	L	Input 1	L	Input 2	L
2	3-state AND	3-state NOR		H	Input 2	Input 1	H

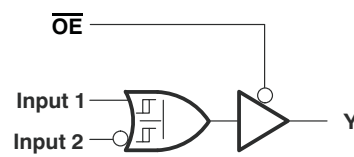
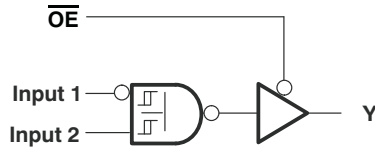


NO. OF INPUTS	AND/NAND FUNCTION	OR/NOR FUNCTION	\overline{OE}	A	B	C	D
2	3-state AND, both inverted inputs	3-state NOR	L	Input 1	H	Input 2	H
2	3-state AND, both inverted inputs	3-state NOR		Input 2	H	Input 1	H

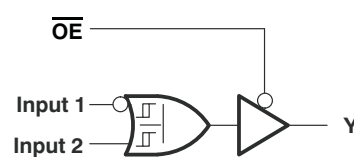
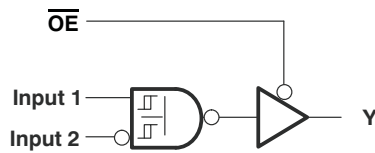
3-State NAND/OR Functions Available



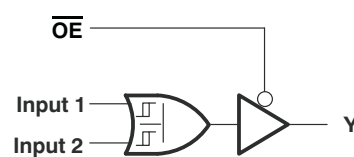
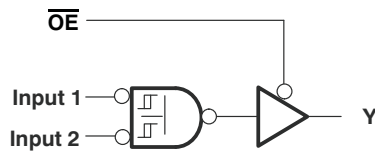
NO. OF INPUTS	AND/NAND FUNCTION	OR/NOR FUNCTION	\overline{OE}	A	B	C	D
2	3-state NAND	3-state OR	L	L	Input 1	Input 2	H
2	3-state NAND	3-state OR		L	Input 2	Input 1	H



NO. OF INPUTS	AND/NAND FUNCTION	OR/NOR FUNCTION	\overline{OE}	A	B	C	D
2	3-state NAND	3-state OR	L	Input 2	L	Input 1	H
2	3-state NAND	3-state OR		H	Input 1	Input 2	L

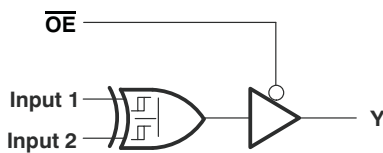


NO. OF INPUTS	AND/NAND FUNCTION	OR/NOR FUNCTION	\overline{OE}	A	B	C	D
2	3-state NAND	3-state OR	L	Input 1	L	Input 2	H
2	3-state NAND	3-state OR		H	Input 2	Input 1	L

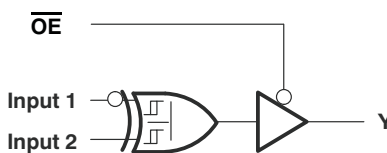


NO. OF INPUTS	AND/NAND FUNCTION	OR/NOR FUNCTION	\overline{OE}	A	B	C	D
2	3-state NAND	3-state OR	L	Input 1	H	Input 2	L
2	3-state NAND	3-state OR		Input 2	H	Input 1	L

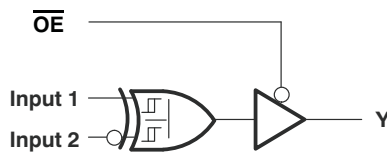
3-State XOR/XNOR Functions Available



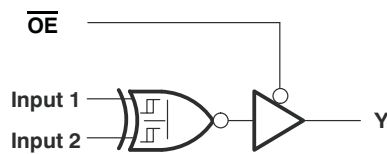
FUNCTION	\overline{OE}	A	B	C	D
3-state XOR	L	Input 1	H or L	L	Input 2
		Input 2	H or L	L	Input 1
		H or L	Input 1	H	Input 2
		H or L	Input 2	H	Input 1
		L	H	Input 1	Input 2
		L	H	Input 2	Input 1



FUNCTION	\overline{OE}	A	B	C	D
3-state XOR	L	H	L	Input 1	Input 2



FUNCTION	\overline{OE}	A	B	C	D
3-state XOR	L	H	L	Input 1	Input 2



FUNCTION	\overline{OE}	A	B	C	D
3-state XNOR	L	H	L	Input 1	Input 2
3-state XNOR		H	L	Input 2	Input 1

Absolute Maximum Ratings⁽¹⁾

over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT
V _{CC}	Supply voltage range	-0.5	6.5	V
V _I	Input voltage range ⁽²⁾	-0.5	6.5	V
V _O	Voltage range applied to any output in the high-impedance or power-off state ⁽²⁾	-0.5	6.5	V
V _O	Voltage range applied to any output in the high or low state ⁽²⁾⁽³⁾	-0.5	V _{CC} + 0.5	V
I _{IK}	Input clamp current	V _I < 0	-50	mA
I _{OK}	Output clamp current	V _O < 0	-50	mA
I _O	Continuous output current		±50	mA
	Continuous current through V _{CC} or GND		±100	mA
θ _{JA}	Package thermal impedance ⁽⁴⁾	DCT package	220	°C/W
		DCU package	227	
		YZP package	102	
T _{stg}	Storage temperature range	-65	150	°C

- (1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) The input and output negative voltage ratings may be exceeded if the input and output current ratings are observed.
- (3) The value of V_{CC} is provided in the recommended operating conditions table.
- (4) The package thermal impedance is calculated in accordance with JESD 51-7.

Recommended Operating Conditions⁽¹⁾

		MIN	MAX	UNIT	
V _{CC}	Supply voltage	Operating	1.65	5.5	V
		Data retention only	1.5		
V _I	Input voltage	0	5.5	V	
V _O	Output voltage	0	V _{CC}	V	
I _{OH}	High-level output current	V _{CC} = 1.65 V		-4	mA
		V _{CC} = 2.3 V		-8	
		V _{CC} = 3 V		-16	
		V _{CC} = 4.5 V		-24	
I _{OL}	Low-level output current	V _{CC} = 1.65 V		4	mA
		V _{CC} = 2.3 V		8	
		V _{CC} = 3 V		16	
		V _{CC} = 4.5 V		24	
Δt/Δv	Input transition rise or fall rate	V _{CC} = 1.8 V ± 0.15 V, 2.5 V ± 0.2 V		20	ns/V
		V _{CC} = 3.3 V ± 0.3 V		10	
		V _{CC} = 5 V ± 0.5 V		5	

- (1) All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number [SCBA004](#).

Electrical Characteristics

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V _{CC}	–40°C to 85°C			–40°C to 125°C			UNIT
			MIN	TYP ⁽¹⁾	MAX	MIN	TYP ⁽¹⁾	MAX	
V _{T+} Positive-going input threshold voltage		1.65 V	0.79		1.26	0.79		1.26	V
		2.3 V	1.11		1.66	1.11		1.66	
		3 V	1.5		1.97	1.5		1.97	
		4.5 V	2.16		2.84	2.16		2.84	
		5.5 V	2.61		3.43	2.61		3.43	
V _{T–} Negative-going input threshold voltage		1.65 V	0.39		0.72	0.39		0.72	V
		2.3 V	0.58		0.97	0.58		0.97	
		3 V	0.84		1.24	0.84		1.24	
		4.5 V	1.41		1.89	1.41		1.89	
		5.5 V	1.87		2.39	1.87		2.39	
ΔV _T Hysteresis (V _{T+} – V _{T–})		1.65 V	0.37		0.72	0.37		0.72	V
		2.3 V	0.48		0.87	0.48		0.87	
		3 V	0.56		0.97	0.56		0.97	
		4.5 V	0.71		1.14	0.71		1.14	
		5.5 V	0.71		1.21	0.71		1.21	
V _{OH}	I _{OH} = –100 μA	1.65 V to 5.5 V	V _{CC} – 0.1		V _{CC} – 0.1				V
	I _{OH} = –4 mA	1.65 V	1.2		1.2				
	I _{OH} = –8 mA	2.3 V	1.9		1.9				
	I _{OH} = –16 mA	3 V	2.4		2.4				
	I _{OH} = –24 mA		2.3		2.3				
	I _{OH} = –32 mA	4.5 V	3.8		3.8				
V _{OL}	I _{OL} = 100 μA	1.65 V to 5.5 V		0.1		0.1		V	
	I _{OL} = 4 mA	1.65 V		0.45		0.45			
	I _{OL} = 8 mA	2.3 V		0.3		0.3			
	I _{OL} = 16 mA	3 V		0.4		0.4			
	I _{OL} = 24 mA			0.55		0.55			
	I _{OL} = 32 mA	4.5 V		0.55		0.55			
I _I	V _I = 5.5 V or GND	0 V to 5.5 V		±5		±5	μA		
I _{off}	V _I or V _O = 5.5 V	0 V		±10		±10	μA		
I _{OZ}	V _O = V _{CC} or GND	1.65 V to 5.5 V		±10		±10	μA		
I _{CC}	V _I = 5.5 V or GND, I _O = 0	1.65 V to 5.5 V		10		10	μA		
ΔI _{CC}	One input at V _{CC} – 0.6 V, Other inputs at V _{CC} or GND	3 V to 5.5 V		500		500	μA		
C _i	V _I = V _{CC} or GND	3.3 V		3.5		3.5	pF		
C _o	V _O = V _{CC} or GND	3.3 V		6		6	pF		

 (1) T_A = 25°C

Switching Characteristics

over recommended operating free-air temperature range, $C_L = 15$ pF (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	SN74LVC1G99 –40°C to 85°C								UNIT
			$V_{CC} = 1.8$ V ± 0.15 V		$V_{CC} = 2.5$ V ± 0.2 V		$V_{CC} = 3.3$ V ± 0.3 V		$V_{CC} = 5$ V ± 0.5 V		
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
t_{pd}	A	Y	4.5	30.1	2.5	11.3	1.8	7.5	1.3	4.8	ns
	B		4.4	28.3	2.4	10.8	1.8	7.2	1.3	4.7	
	C		4.4	29.1	2.4	11.7	1.9	7.6	1.3	5	
	D		4.3	25.1	2.4	10.2	1.7	6.7	1.3	4.5	
t_{en}	\overline{OE}	Y	3.4	24.7	2.1	10	1.3	5.8	1	3.8	ns
t_{dis}	\overline{OE}	Y	4	15.5	2.7	7.5	3.5	7	2	5.5	ns

Switching Characteristics

over recommended operating free-air temperature range, $C_L = 30$ pF or 50 pF (unless otherwise noted) (see Figure 2)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	SN74LVC1G99 –40°C to 85°C								UNIT
			$V_{CC} = 1.8$ V ± 0.15 V		$V_{CC} = 2.5$ V ± 0.2 V		$V_{CC} = 3.3$ V ± 0.3 V		$V_{CC} = 5$ V ± 0.5 V		
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
t_{pd}	A	Y	4.6	30.8	2.6	11.7	2.4	8.4	1.8	5.5	ns
	B		4.6	28.9	2.6	11.3	2.3	8.2	1.8	5.4	
	C		4.4	29.8	2.5	12.3	2.5	8.6	1.8	5.7	
	D		4.3	25.7	2.5	10.7	2.4	7.6	1.6	5.2	
t_{en}	\overline{OE}	Y	4.2	25.2	2.4	11.3	2	7	1.7	4.7	ns
t_{dis}	\overline{OE}	Y	3.7	15	2	5.8	2.1	5.6	1	4.5	ns

Switching Characteristics

over recommended operating free-air temperature range (unless otherwise noted) (see Figure 2)

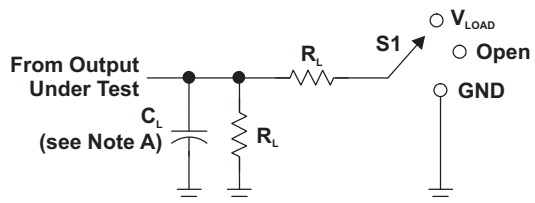
PARAMETER	FROM (INPUT)	TO (OUTPUT)	SN74LVC1G99 –40°C to 125°C								UNIT
			$V_{CC} = 1.8$ V ± 0.15 V		$V_{CC} = 2.5$ V ± 0.2 V		$V_{CC} = 3.3$ V ± 0.3 V		$V_{CC} = 5$ V ± 0.5 V		
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
t_{pd}	A	Y	4.6	32.8	2.6	13.7	2.4	10.4	1.8	6.9	ns
	B		4.6	30.9	2.6	13.3	2.3	10.2	1.8	6.8	
	C		4.4	31.8	2.4	14.3	2.5	10.6	1.8	7.2	
	D		4.3	27.7	2.5	12.7	2.4	9.5	1.6	6.5	
t_{en}	\overline{OE}	Y	4.2	27.2	2.4	13.3	2.0	9.0	1.7	6.0	ns
t_{dis}	\overline{OE}	Y	3.7	17.0	2.0	7.3	2.1	7.4	1.0	5.6	ns

Operating Characteristics

$T_A = 25^\circ\text{C}$

PARAMETER	TEST CONDITIONS	$V_{CC} = 1.8$ V	$V_{CC} = 2.5$ V	$V_{CC} = 3.3$ V	$V_{CC} = 5$ V	UNIT
		TYP	TYP	TYP	TYP	
C_{pd} Power dissipation capacitance	$f = 10$ MHz	19	20	22	27	pF

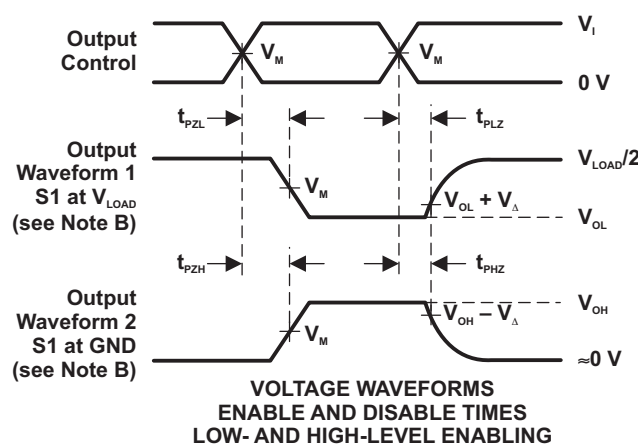
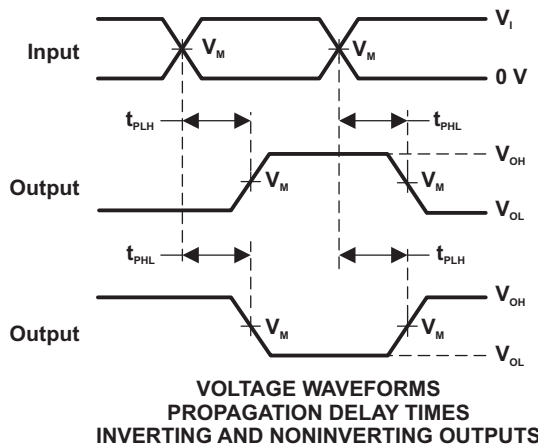
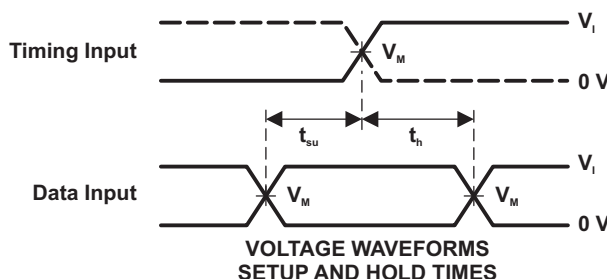
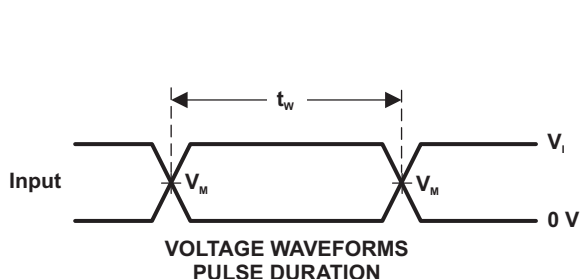
Parameter Measurement Information



LOAD CIRCUIT

TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	V_{LOAD}
t_{PHZ}/t_{PZH}	GND

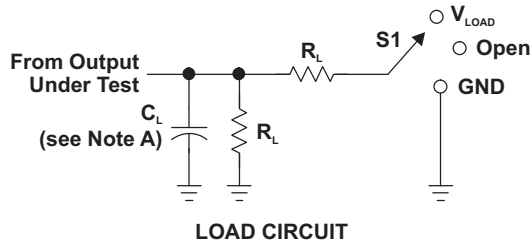
V_{CC}	INPUTS		V_M	V_{LOAD}	C_L	R_L	V_{Δ}
	V_I	t/t_i					
$1.8 V \pm 0.15 V$	V_{CC}	$\leq 2 ns$	$V_{CC}/2$	$2 \times V_{CC}$	15 pF	1 M Ω	0.15 V
$2.5 V \pm 0.2 V$	V_{CC}	$\leq 2 ns$	$V_{CC}/2$	$2 \times V_{CC}$	15 pF	1 M Ω	0.15 V
$3.3 V \pm 0.3 V$	3 V	$\leq 2.5 ns$	1.5 V	6 V	15 pF	1 M Ω	0.3 V
$5 V \pm 0.5 V$	V_{CC}	$\leq 2.5 ns$	$V_{CC}/2$	$2 \times V_{CC}$	15 pF	1 M Ω	0.3 V



- NOTES: A. C_L includes probe and jig capacitance.
 B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
 C. All input pulses are supplied by generators having the following characteristics: PRR \leq 10 MHz, $Z_o = 50 \Omega$.
 D. The outputs are measured one at a time, with one transition per measurement.
 E. t_{PLZ} and t_{PHZ} are the same as t_{dis} .
 F. t_{PZL} and t_{PZH} are the same as t_{en} .
 G. t_{PLH} and t_{PHL} are the same as t_{pd} .
 H. All parameters and waveforms are not applicable to all devices.

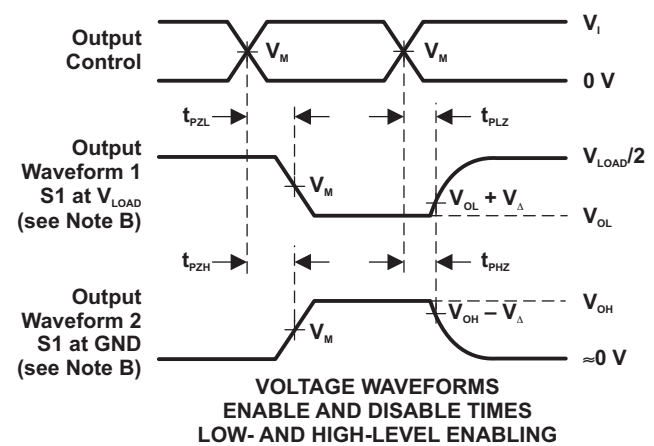
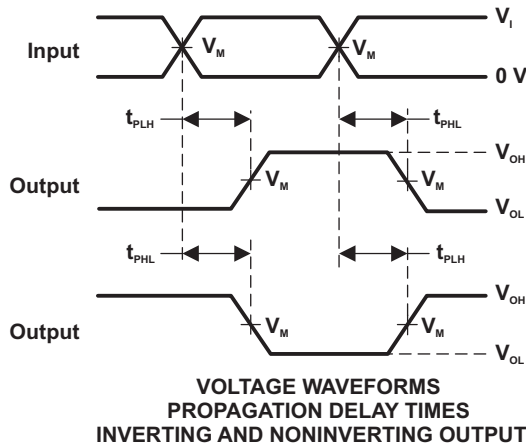
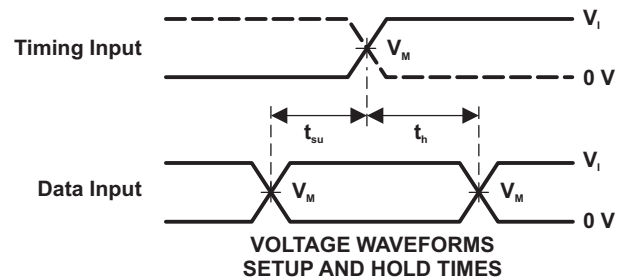
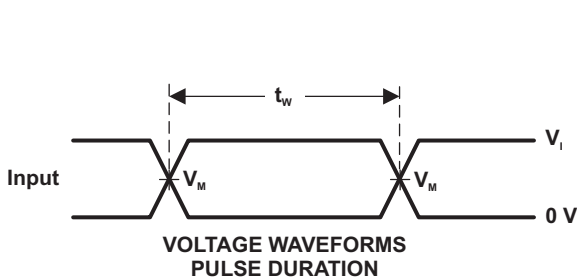
Figure 1. Load Circuit and Voltage Waveforms

Parameter Measurement Information (continued)



TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	V_{LOAD}
t_{PHZ}/t_{PZH}	GND

V_{CC}	INPUTS		V_M	V_{LOAD}	C_L	R_L	V_{Δ}
	V_I	t_r/t_f					
$1.8\text{ V} \pm 0.15\text{ V}$	V_{CC}	$\leq 2\text{ ns}$	$V_{CC}/2$	$2 \times V_{CC}$	30 pF	1 k Ω	0.15 V
$2.5\text{ V} \pm 0.2\text{ V}$	V_{CC}	$\leq 2\text{ ns}$	$V_{CC}/2$	$2 \times V_{CC}$	30 pF	500 Ω	0.15 V
$3.3\text{ V} \pm 0.3\text{ V}$	3 V	$\leq 2.5\text{ ns}$	1.5 V	6 V	50 pF	500 Ω	0.3 V
$5\text{ V} \pm 0.5\text{ V}$	V_{CC}	$\leq 2.5\text{ ns}$	$V_{CC}/2$	$2 \times V_{CC}$	50 pF	500 Ω	0.3 V



- NOTES: A. C_L includes probe and jig capacitance.
 B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
 C. All input pulses are supplied by generators having the following characteristics: PRR \leq 10 MHz, $Z_o = 50\ \Omega$.
 D. The outputs are measured one at a time, with one transition per measurement.
 E. t_{PLZ} and t_{PHZ} are the same as t_{dis} .
 F. t_{PZL} and t_{PZH} are the same as t_{on} .
 G. t_{PLH} and t_{PHL} are the same as t_{pd} .
 H. All parameters and waveforms are not applicable to all devices.

Figure 2. Load Circuit and Voltage Waveforms

REVISION HISTORY

Changes from Revision E (October 2007) to Revision F **Page**

- Changed document template from TIMS format to DocZone format. 1
 - Changed 3-State Mux graphic to fix labeling error. 4
-

Changes from Revision F (April 2011) to Revision G **Page**

- Updated document to new TI data sheet format. 1
 - Updated Features. 1
 - Added ESD warning. 2
 - Updated operating temperature range. 8
-

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
SN74LVC1G99DCTR	ACTIVE	SM8	DCT	8	3000	RoHS & Green	NIPDAU SN	Level-1-260C-UNLIM	-40 to 125	(2WF5, C99) (R, Z)	Samples
SN74LVC1G99DCTRG4	ACTIVE	SM8	DCT	8	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	(2WF5, C99) (R, Z)	Samples
SN74LVC1G99DCTT	ACTIVE	SM8	DCT	8	250	RoHS & Green	NIPDAU SN	Level-1-260C-UNLIM	-40 to 125	(2WF5, C99) (R, Z)	Samples
SN74LVC1G99DCUR	ACTIVE	VSSOP	DCU	8	3000	RoHS & Green	NIPDAU SN	Level-1-260C-UNLIM	-40 to 125	(C99J, C99Q, C99R)	Samples
SN74LVC1G99DCURG4	ACTIVE	VSSOP	DCU	8	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	C99R	Samples
SN74LVC1G99DCUT	ACTIVE	VSSOP	DCU	8	250	RoHS & Green	NIPDAU SN	Level-1-260C-UNLIM	-40 to 125	(C99J, C99Q, C99R)	Samples
SN74LVC1G99YZPR	ACTIVE	DSBGA	YZP	8	3000	RoHS & Green	SNAGCU	Level-1-260C-UNLIM	-40 to 125	DEN	Samples

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

⁽⁶⁾ Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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OTHER QUALIFIED VERSIONS OF SN74LVC1G99 :

- Automotive : [SN74LVC1G99-Q1](#)

NOTE: Qualified Version Definitions:

- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects

TAPE AND REEL INFORMATION

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE

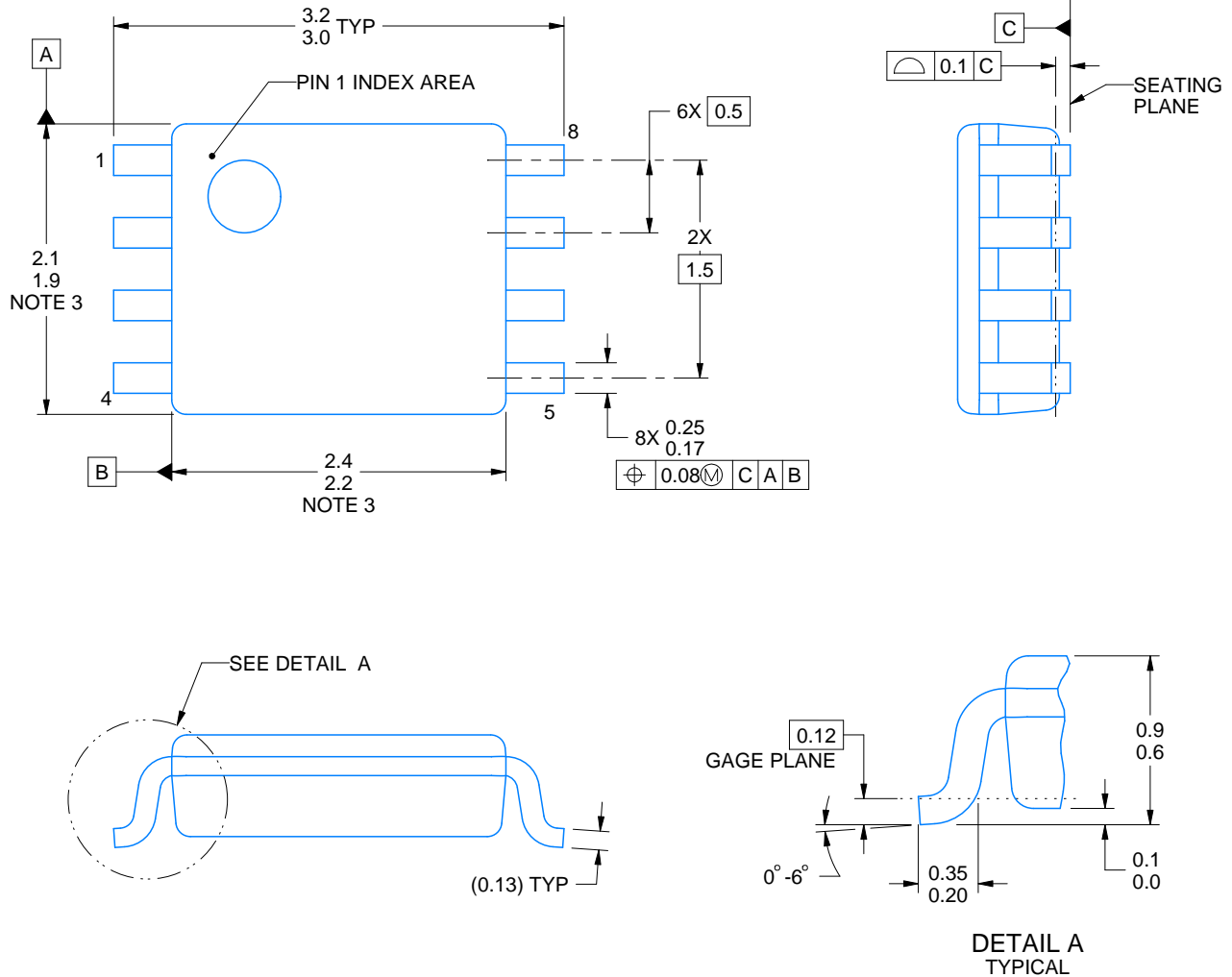

*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74LVC1G99DCTR	SM8	DCT	8	3000	180.0	12.4	3.15	4.35	1.55	4.0	12.0	Q3
SN74LVC1G99DCTR	SM8	DCT	8	3000	180.0	13.0	3.35	4.5	1.55	4.0	12.0	Q3
SN74LVC1G99DCTT	SM8	DCT	8	250	180.0	13.0	3.35	4.5	1.55	4.0	12.0	Q3
SN74LVC1G99DCTT	SM8	DCT	8	250	180.0	12.4	3.15	4.35	1.55	4.0	12.0	Q3
SN74LVC1G99DCUR	VSSOP	DCU	8	3000	178.0	9.0	2.25	3.35	1.05	4.0	8.0	Q3
SN74LVC1G99DCURG4	VSSOP	DCU	8	3000	180.0	8.4	2.25	3.35	1.05	4.0	8.0	Q3
SN74LVC1G99DCUT	VSSOP	DCU	8	250	178.0	9.5	2.25	3.35	1.05	4.0	8.0	Q3
SN74LVC1G99DCUT	VSSOP	DCU	8	250	178.0	9.0	2.25	3.35	1.05	4.0	8.0	Q3
SN74LVC1G99YZPR	DSBGA	YZP	8	3000	178.0	9.2	1.02	2.02	0.63	4.0	8.0	Q1

TAPE AND REEL BOX DIMENSIONS


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74LVC1G99DCTR	SM8	DCT	8	3000	190.0	190.0	30.0
SN74LVC1G99DCTR	SM8	DCT	8	3000	182.0	182.0	20.0
SN74LVC1G99DCTT	SM8	DCT	8	250	182.0	182.0	20.0
SN74LVC1G99DCTT	SM8	DCT	8	250	190.0	190.0	30.0
SN74LVC1G99DCUR	VSSOP	DCU	8	3000	180.0	180.0	18.0
SN74LVC1G99DCURG4	VSSOP	DCU	8	3000	183.0	183.0	20.0
SN74LVC1G99DCUT	VSSOP	DCU	8	250	202.0	201.0	28.0
SN74LVC1G99DCUT	VSSOP	DCU	8	250	180.0	180.0	18.0
SN74LVC1G99YZPR	DSBGA	YZP	8	3000	220.0	220.0	35.0



4225266/A 09/2014

NOTES:

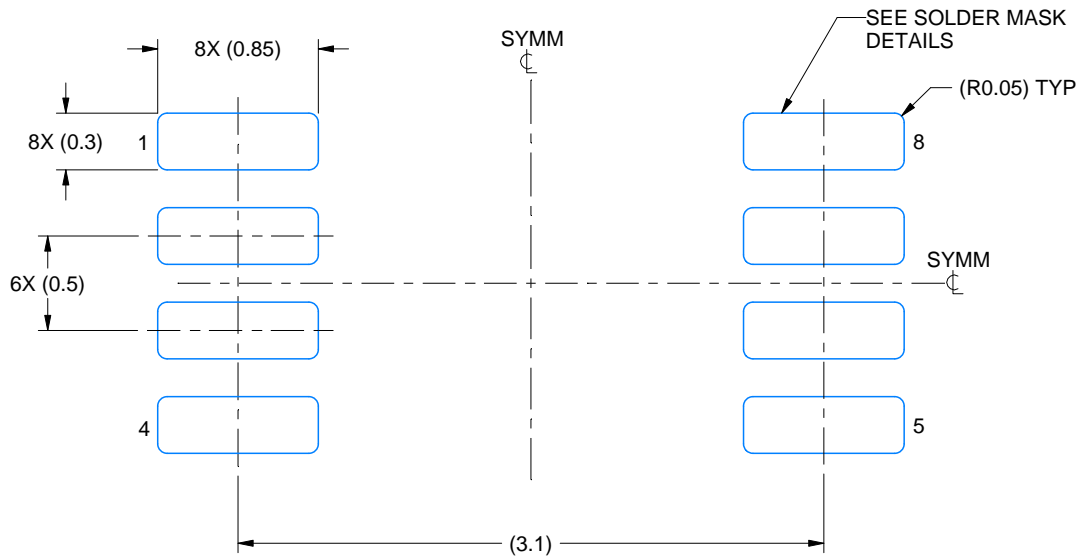
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. Reference JEDEC registration MO-187 variation CA.

EXAMPLE BOARD LAYOUT

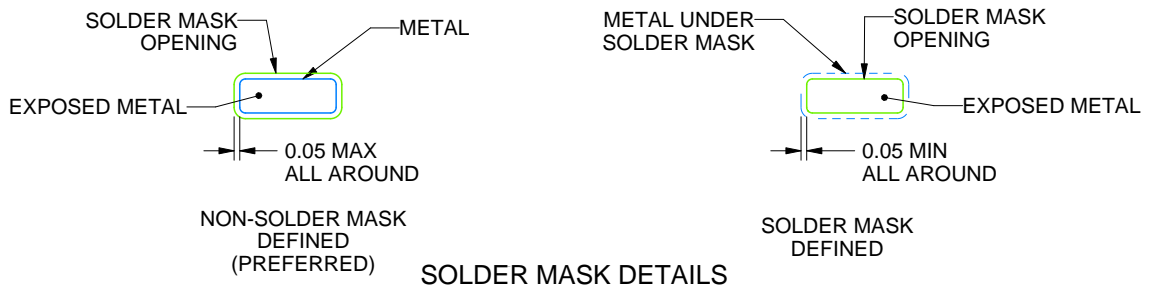
DCU0008A

VSSOP - 0.9 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 25X



4225266/A 09/2014

NOTES: (continued)

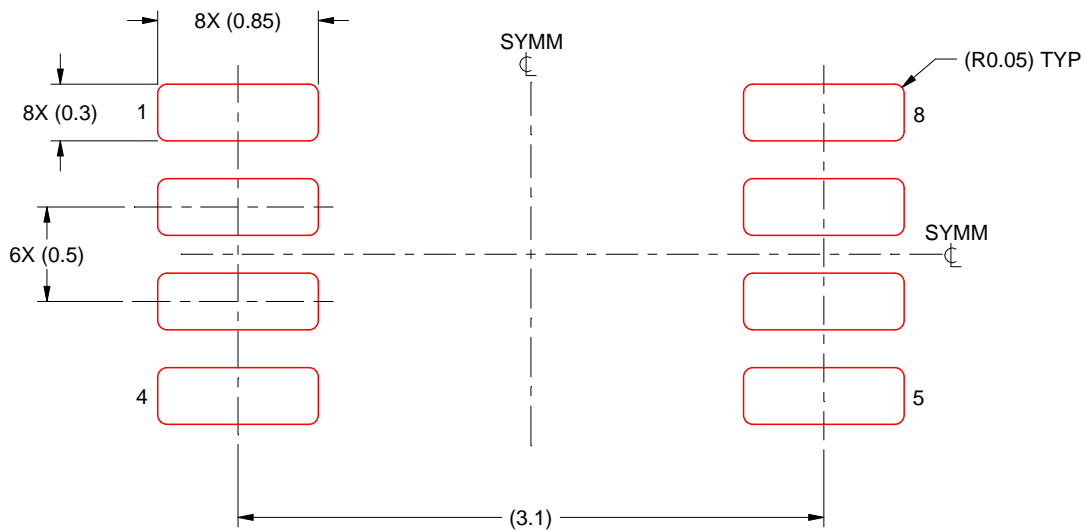
- 5. Publication IPC-7351 may have alternate designs.
- 6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

DCU0008A

VSSOP - 0.9 mm max height

SMALL OUTLINE PACKAGE

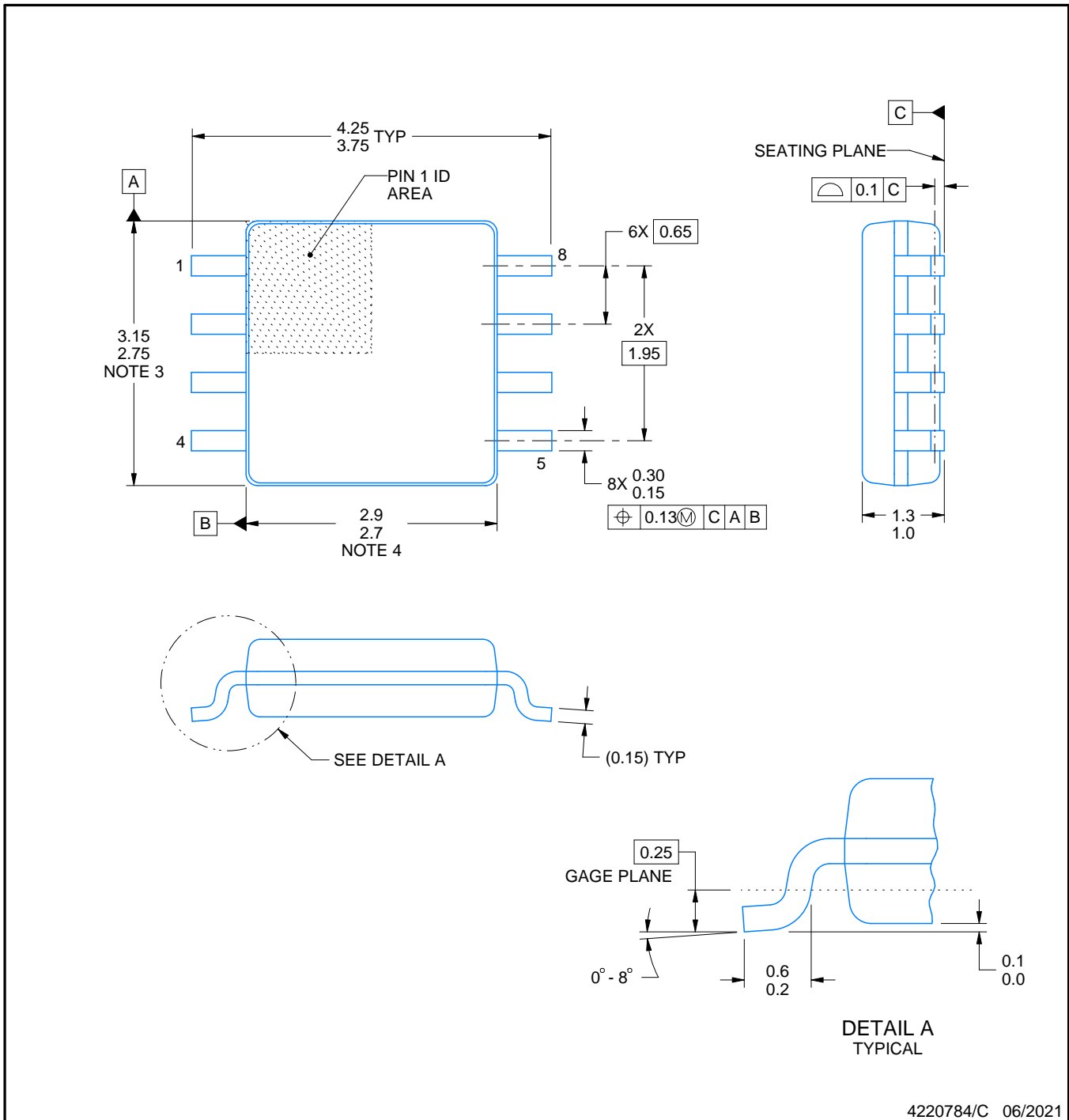
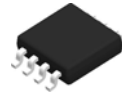


SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 25X

4225266/A 09/2014

NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.



4220784/C 06/2021

NOTES:

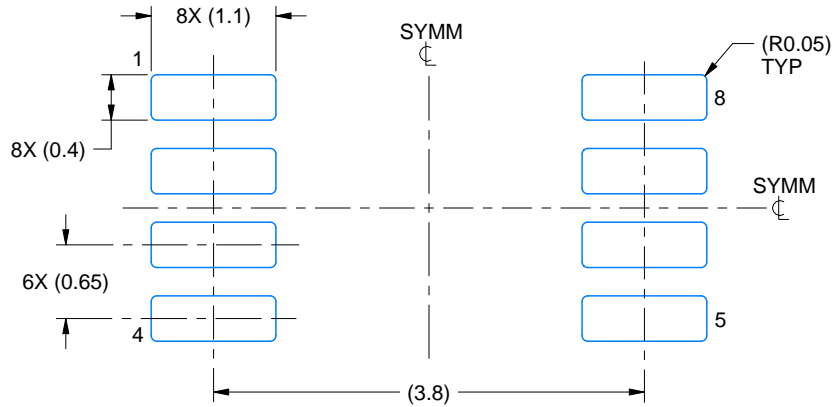
- All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
- This drawing is subject to change without notice.
- This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
- This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.

EXAMPLE BOARD LAYOUT

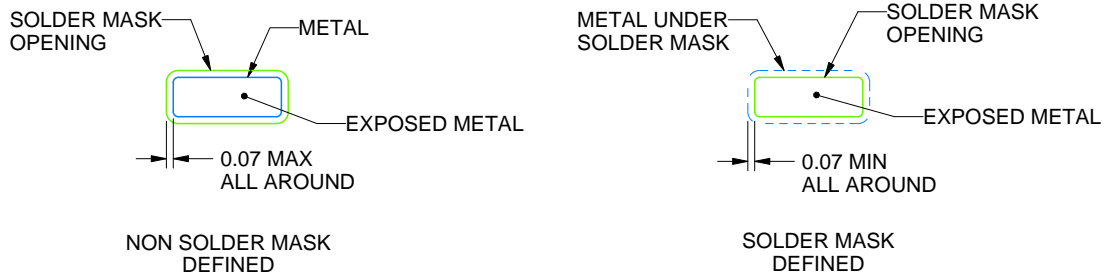
DCT0008A

SSOP - 1.3 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:15X



SOLDER MASK DETAILS

4220784/C 06/2021

NOTES: (continued)

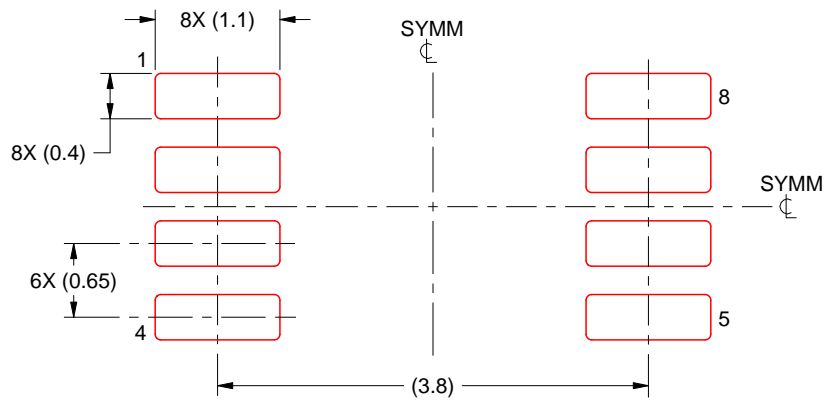
- 5. Publication IPC-7351 may have alternate designs.
- 6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

DCT0008A

SSOP - 1.3 mm max height

SMALL OUTLINE PACKAGE



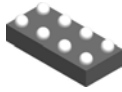
SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:15X

4220784/C 06/2021

NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

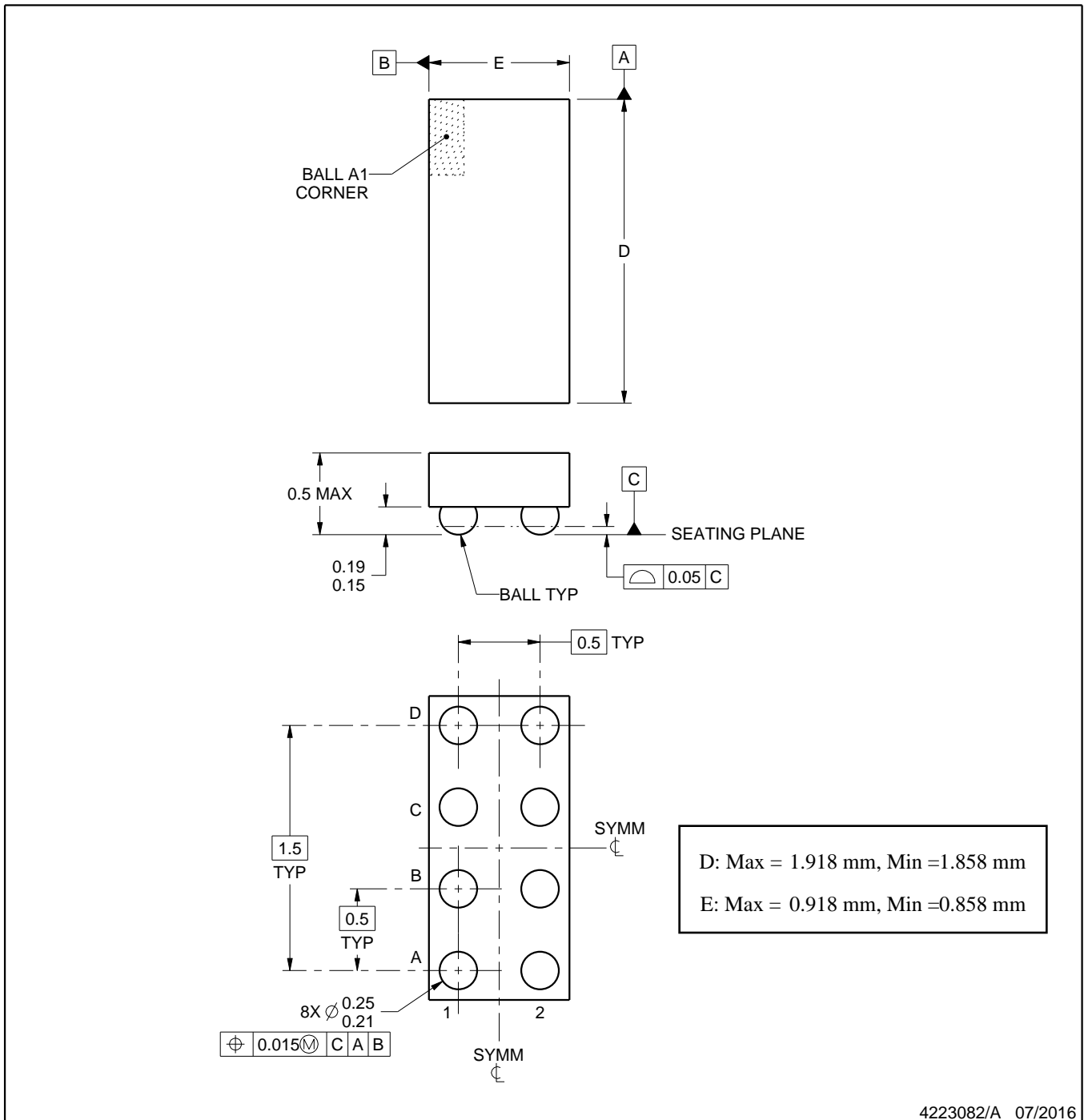
YZP0008



PACKAGE OUTLINE

DSBGA - 0.5 mm max height

DIE SIZE BALL GRID ARRAY



NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.

EXAMPLE BOARD LAYOUT

YZP0008

DSBGA - 0.5 mm max height

DIE SIZE BALL GRID ARRAY



LAND PATTERN EXAMPLE
SCALE:40X



SOLDER MASK DETAILS
NOT TO SCALE

4223082/A 07/2016

NOTES: (continued)

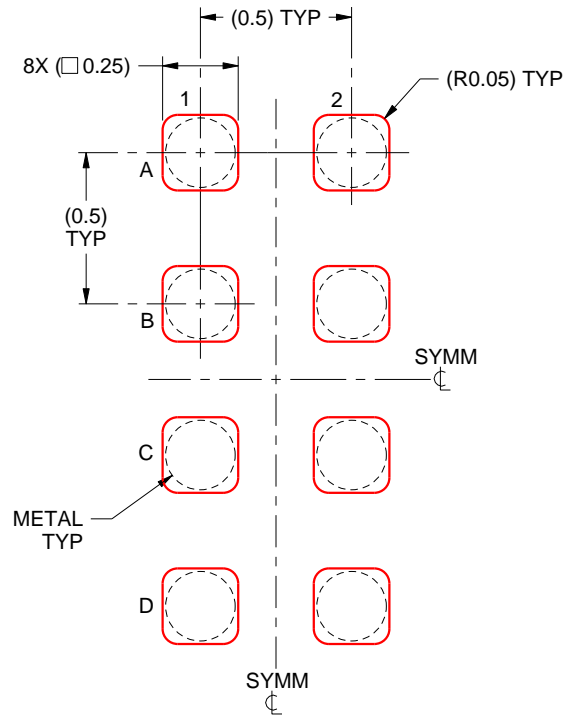
3. Final dimensions may vary due to manufacturing tolerance considerations and also routing constraints. For more information, see Texas Instruments literature number SNVA009 (www.ti.com/lit/snva009).

EXAMPLE STENCIL DESIGN

YZP0008

DSBGA - 0.5 mm max height

DIE SIZE BALL GRID ARRAY



SOLDER PASTE EXAMPLE
BASED ON 0.1 mm THICK STENCIL
SCALE:40X

4223082/A 07/2016

NOTES: (continued)

4. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release.

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