



# THE DATASHEET OF SN65HVS882PWPR



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## INDUSTRIAL 8-DIGITAL-INPUT SERIALIZER

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### FEATURES

- **Eight Inputs**
  - **High Input Voltage – up to 34 V**
  - **Selectable Debounce Filters – 0 ms to 3 ms**
  - **Flexible Input Current Limit – 0.2 mA to 5.2 mA**
  - **Field Pins Protected to 15-kV HBM ESD**
- **Output Drivers for External Status LEDs**
- **Cascadable in Multiples of Eight Inputs**
- **SPI-Compatible Interface**
- **Regulated 5-V Output for External Isolator**
- **Over-Temperature Indicator**

### APPLICATIONS

- **Sensor Inputs for Industrial Automation and Process Control**
- **High Channel Count Digital Input Modules for PC and PLC Systems**
- **Decentralized I/O Modules**
- **Motion Control Systems**

### DESCRIPTION

The SN65HVS882 is an eight channel, digital-input serializer for high-channel density digital input modules in industrial automation. In combination with galvanic isolators the device completes the interface between the high voltage signals on the field-side and the low-voltage signals on the controller side. Input signals are current-limited and then validated by internal debounce filters.

With the addition of a few external components, the input switching characteristics can be configured in accordance with IEC61131-2 for Type 1, 2, and 3 sensor switches.

Upon the application of load and clock signals, input data is latched in parallel into the shift register and afterwards clocked out serially.

Cascading of multiple devices is possible by connecting the serial output of the leading device with the serial input of the following device, enabling the design of high-channel count input modules. Multiple devices can be cascaded through a single serial port, reducing both the isolation channels and controller inputs required.

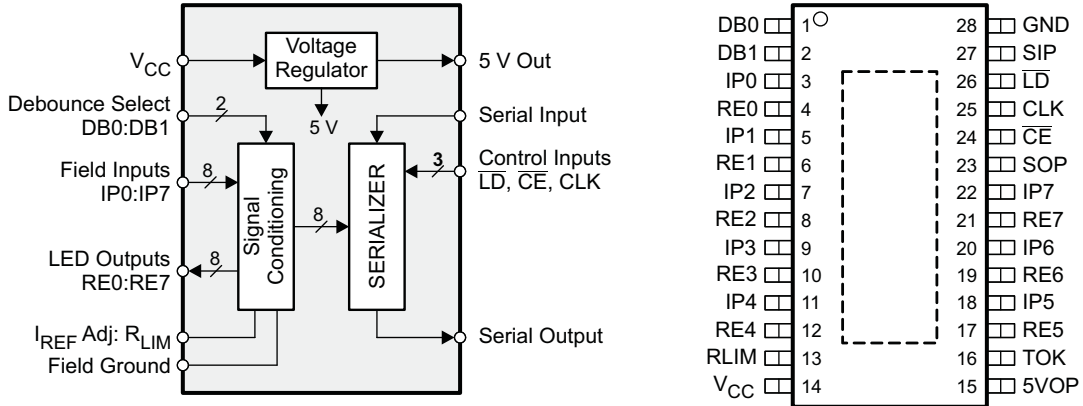
Input status can be visually indicated via constant current LED outputs. The current limit on the inputs is set by a single external precision resistor. An integrated voltage regulator provides a 5-V output to supply low-power isolators. An on-chip temperature sensor provides diagnostic information for graceful shutdown and system safety.

The SN65HVS882 is available in a 28-pin PWP PowerPAD™ package, allowing for efficient heat dissipation. The device is characterized for operation at temperatures from -40°C to 125°C.

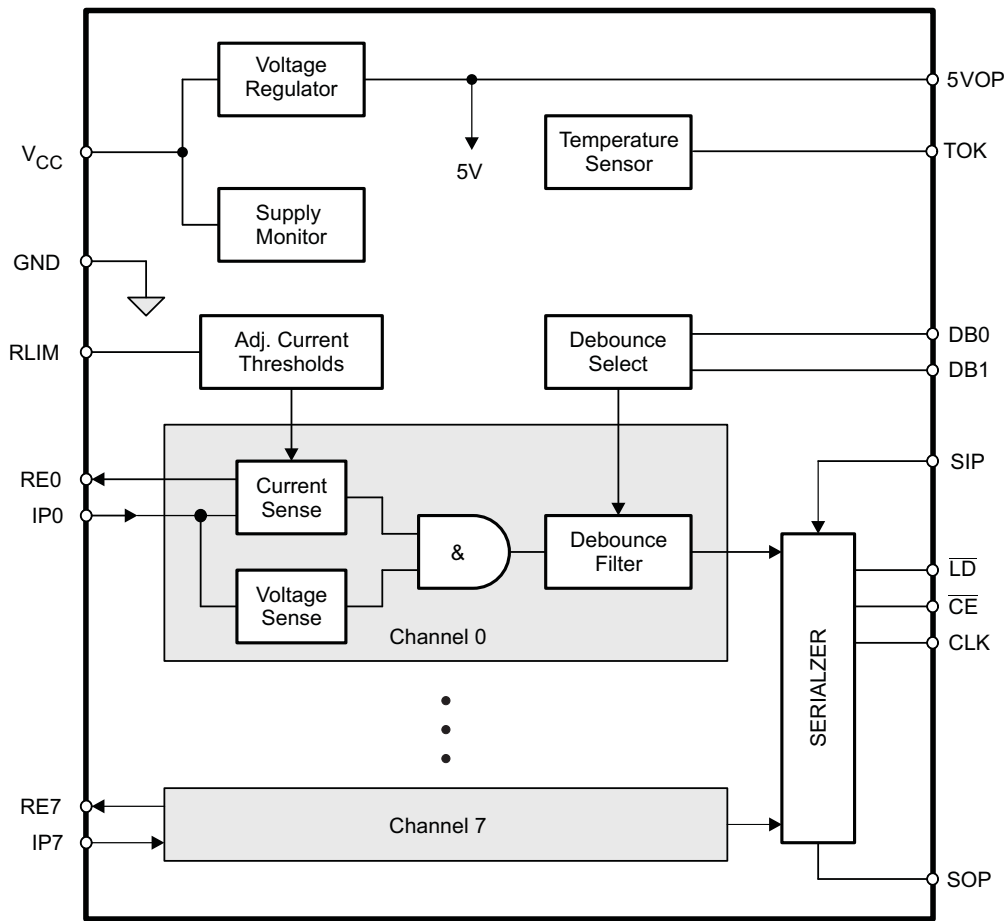


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PowerPAD is a trademark of Texas Instruments.



FUNCTIONAL BLOCK DIAGRAM



**TERMINAL FUNCTIONS**

TERMINAL		DESCRIPTION
PIN NO.	NAME	
1, 2	DB0, DB1	Debounce select inputs
3, 5, 7, 9, 11, 18, 20, 22	IPx	Input channel x
4, 6, 8, 10, 12, 17, 19, 21	REx	Return path x (LED drive)
13	RLIM	Current limiting resistor
14	V <sub>CC</sub>	Field supply voltage
15	5VOP	5-V output to supply low power isolators
16	TOK	Temperature okay
23	SOP	Serial data output
24	$\overline{\text{CE}}$	Clock enable input
25	CLK	Serial clock input
26	$\overline{\text{LD}}$	Load pulse input
27	SIP	Serial data input
28	GND	Field ground

**ABSOLUTE MAXIMUM RATINGS<sup>(1)</sup>**

over operating free-air temperature range (unless otherwise noted)

			VALUE	UNIT	
V <sub>CC</sub>	Field power input		–0.3 to 36	V	
V <sub>IPx</sub>	Field digital inputs	IPx	–0.3 to 36	V	
V <sub>ID</sub>	Voltage at any logic input	DB0, DB1, CLK, SIP, $\overline{CE}$ , $\overline{LD}$	–0.5 to 6	V	
I <sub>O</sub>	Output current	TOK, SOP	±8	mA	
V <sub>ESD</sub>	Electrostatic discharge	Human-Body Model <sup>(2)</sup>	All pins	±4	kV
			IPx, V <sub>CC</sub>	±15	
		Charged-Device Model <sup>(3)</sup>	All pins	±1	kV
			Machine Model <sup>(4)</sup>	All pins	±100
P <sub>TOT</sub>	Continuous total power dissipation	See <i>Thermal Characteristics</i>			
T <sub>J</sub>	Junction temperature		170	°C	

(1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

(2) JEDEC Standard 22, Method A114-A.

(3) JEDEC Standard 22, Method C101

(4) JEDEC Standard 22, Method A115-A

**THERMAL CHARACTERISTICS**

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
θ <sub>JA</sub>	Junction-to-air thermal resistance	High-K JEDEC thermal resistance model		35		°C/W
θ <sub>JB</sub>	Junction-to-board thermal resistance			15		°C/W
θ <sub>JC</sub>	Junction-to-case thermal resistance			4.27		°C/W
P <sub>D</sub>	Device power dissipation	I <sub>CC</sub> and I <sub>IP-LIM</sub> = worst case with R <sub>LIM</sub> = 25 kΩ, I <sub>LOAD</sub> = 50 mA on 5VOP, RE0-RE7 = GND, f <sub>IP</sub> = 100 MHz	IP0-IP7 = V <sub>CC</sub> = 34 V			mW
			IP0-IP7 = V <sub>CC</sub> = 30 V		2600	
			IP0-IP7 = V <sub>CC</sub> = 24 V			
			IP0-IP7 = V <sub>CC</sub> = 12 V			

**RECOMMENDED OPERATING CONDITIONS**

			MIN	TYP	MAX	UNIT
V <sub>CC</sub>	Field supply voltage		10		34	V
V <sub>IPL</sub>	Field input low-state input voltage		0		4	V
V <sub>IPH</sub>	Field input high-state input voltage		5.5		34	V
V <sub>IL</sub>	Logic low-state input voltage		0		0.8	V
V <sub>IH</sub>	Logic high-state input voltage		2.0		5.5	V
R <sub>LIM</sub>	Current limiter resistor		17	25	500	kΩ
f <sub>IP</sub> <sup>(1)</sup>	Input data rate (each field input)		0		1	Mbps
T <sub>A</sub>	Free-air temperature, see <i>Thermal Characteristics</i>	V <sub>CC</sub> ≤ 34 V	–40		85	°C
		V <sub>CC</sub> ≤ 27 V	–40		105	
		V <sub>CC</sub> ≤ 18 V	–40		125	
T <sub>J</sub>	Junction temperature				150	°C

(1) Maximum data rate corresponds to 0 ms debounce time, (DB0 = open, DB1 = GND), and R<sub>IN</sub> = 0 Ω

## ELECTRICAL CHARACTERISTICS

Over full-range of recommended operating conditions, unless otherwise noted

PARAMETER		TERMINAL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
<b>FIELD INPUTS</b>							
$V_{TH-(IP)}$	Low-level input threshold voltage	IP0–IP7	$R_{LIM} = 25\text{ k}\Omega$	4.0	4.3		V
$V_{TH+(IP)}$	High-level input threshold voltage			5.2	5.5		
$V_{HYS(IP)}$	Input hysteresis			0.9			
$V_{TH-(IN)}$	Low-level input threshold voltage	Measured at field side of $R_{IN}$	18 V < $V_{CC}$ < 30 V, $R_{IN} = 1.2\text{ k}\Omega \pm 5\%$ , $R_{LIM} = 25\text{ k}\Omega$ , $T_A \leq 85\text{ }^\circ\text{C}$	6	8.4		V
$V_{TH+(IN)}$	High-level input threshold voltage			9.4	10		
$V_{HYS(IN)}$	Input hysteresis			1			
$R_{IP}$	Input resistance	IP0–IP7	3 V < $V_{IPx}$ < 6 V, $R_{LIM} = 25\text{ k}\Omega$	0.2	0.63	1.1	k $\Omega$
$I_{IP-LIM}$	Input current limit	IP0–IP7	$R_{LIM} = 25\text{ k}\Omega$	3.15	3.6	4	mA
$t_{DB}$	Debounce times of input channels	IP0–IP7	DB0 = open, DB1 = GND	0			ms
			DB0 = GND, DB1 = open	1			
			DB0 = DB1 = open	3			
$I_{RE-on}$	RE on-state current	RE0–RE7	$R_{LIM} = 25\text{ k}\Omega$ , $RE_x = \text{GND}$	2.8	3.15	3.5	mA
<b>FIELD SUPPLY</b>							
$ICC(V_{CC})$	Supply current, no load	$V_{CC}$	IP0 to IP7 = $V_{CC}$ , 5VOP = open, $RE_x = \text{GND}$ , All logic inputs open			8.7	mA
<b>5V REGULATED OUTPUT</b>							
$V_{O(5V)}$	Linear regulator output voltage	5VOP	10V < $V_{CC}$ < 34V, no load	4.5	5	5.5	V
			10V < $V_{CC}$ < 34V, $I_L = 5\text{ mA}$	4.5	5	5.5	
			10V < $V_{CC}$ < 34V, $I_L = 20\text{ mA}$ , $T_A \leq 105\text{ }^\circ\text{C}$	4.5	5	5.5	
			10V < $V_{CC}$ < 34V, $I_L = 50\text{ mA}$ , $T_A \leq 85\text{ }^\circ\text{C}$	4.5	5	5.5	
$I_{LIM(5V)}$	Linear regulator output current limit			115			mA
$\Delta V_5/\Delta V_{CC}$	Linear regulation	5VOP, $V_{CC}$	10V < $V_{CC}$ < 34V, $I_L = 5\text{ mA}$ ,	2			mV/V
<b>LOGIC INPUT AND OUTPUTS</b>							
$V_{OL}$	Logic low-level output voltage	SOP, TOK	$I_{OL} = 20\text{ }\mu\text{A}$	0.4			V
$V_{OH}$	Logic high-level output voltage			4			V
$I_{IL}$	Logic input leakage current	DB0, DB1, SIP, $\overline{LD}$ , $\overline{CE}$ , CLK		–50	50		$\mu\text{A}$
$T_{OVER}$	Over-temperature indication, internal	TOK		150			$^\circ\text{C}$
$T_{SHDN}$	Shutdown temperature, internal			170			$^\circ\text{C}$

## TIMING REQUIREMENTS

over operating free-air temperature range (unless otherwise noted)

PARAMETER			MIN	TYP	MAX	UNIT
$t_{W1}$	CLK pulse duration	See <a href="#">Figure 5</a>	4			ns
$t_{W2}$	$\overline{LD}$ pulse duration	See <a href="#">Figure 3</a>	6			ns
$t_{SU1}$	SIP to CLK setup time	See <a href="#">Figure 6</a>	4			ns
$t_{H1}$	SIP to CLK hold time	See <a href="#">Figure 6</a>	2			ns
$t_{SU2}$	Falling edge to rising edge ( $\overline{CE}$ to CLK) setup time	See <a href="#">Figure 7</a>	4			ns
$t_{REC}$	$\overline{LD}$ to CLK recovery time	See <a href="#">Figure 4</a>	2			ns
$f_{CLK}$	Clock pulse frequency	See <a href="#">Figure 5</a>	DC		100	MHz

## SWITCHING CHARACTERISTICS

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$t_{PLH1}$ , $t_{PHL1}$	CLK to SOP	$C_L = 15$ pF, see <a href="#">Figure 5</a>			10	ns
$t_{PLH2}$ , $t_{PHL2}$	$\overline{LD}$ to SOP	$C_L = 15$ pF, see <a href="#">Figure 3</a>			14	ns
$t_r$ , $t_f$	Rise and fall times	$C_L = 15$ pF, see <a href="#">Figure 5</a>			5	ns

INPUT CHARACTERISTICS

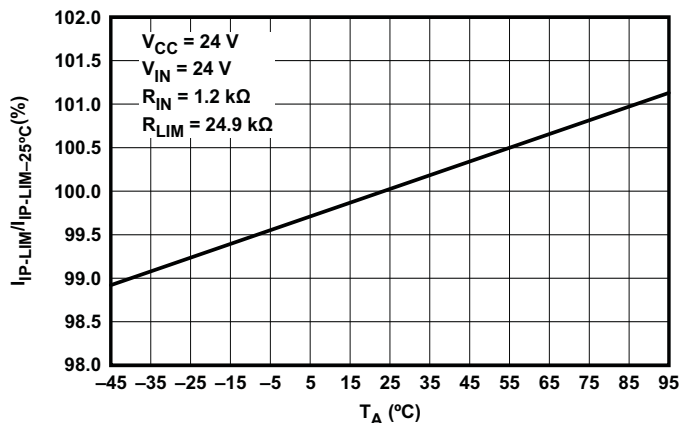


Figure 1. Typical Current Limiter Variation vs Free-Air Temperature

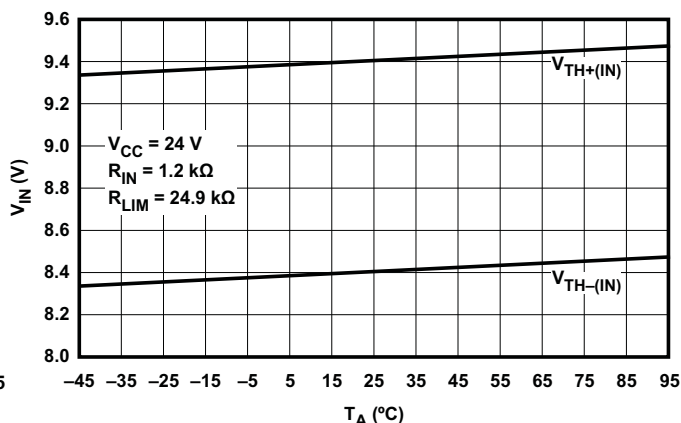


Figure 2. Typical Limiter Input Threshold Voltage Variation vs Free-Air Temperature

PARAMETER MEASUREMENT INFORMATION

Waveforms

For the complete serial interface timing, refer to [Figure 19](#).

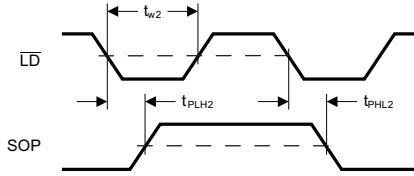


Figure 3. Parallel – Load Mode

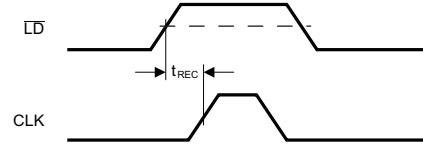


Figure 4. Serial – Shift Mode

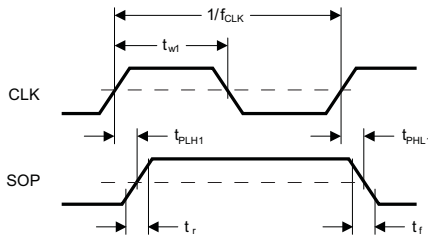


Figure 5. Serial – Shift Mode

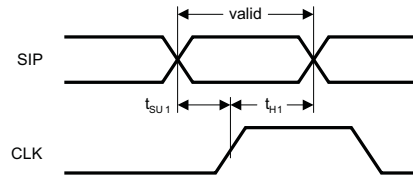


Figure 6. Serial – Shift Mode

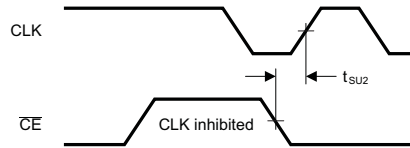


Figure 7. Serial – Shift Clock Inhibit Mode

VOLTAGE REGULATOR PERFORMANCE CHARACTERISTICS

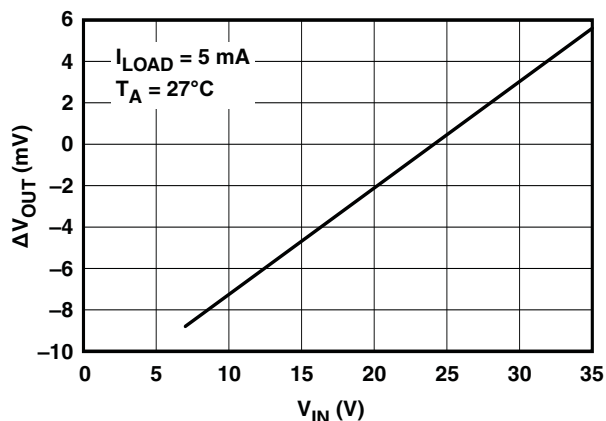


Figure 8. Line Regulation

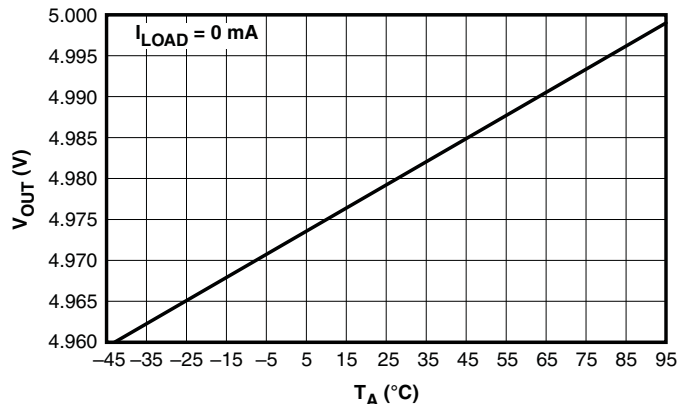


Figure 9. Output Voltage vs Free-Air Temperature

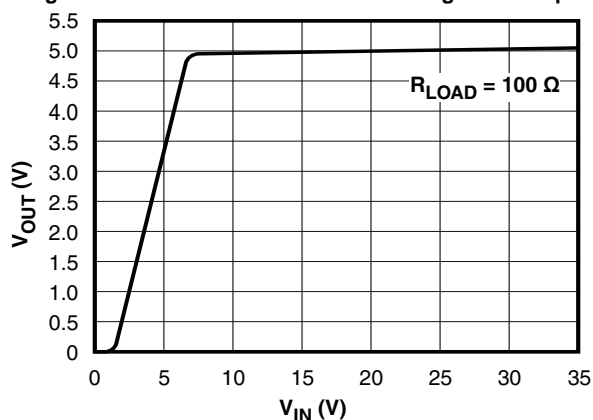


Figure 10. Output Voltage vs Input Voltage

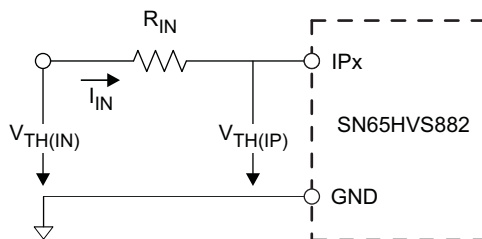
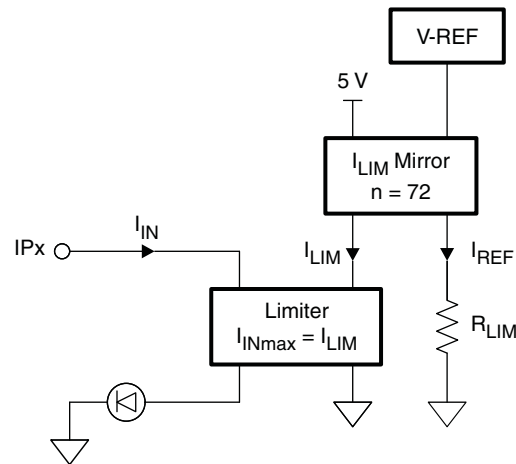


Figure 11. On/Off Threshold Voltage Measurements

## DEVICE INFORMATION

### Digital Inputs



**Figure 12. Digital Input Stage**

Each digital input operates as a controlled current sink limiting the input current to a maximum value of  $I_{LIM}$ . The current limit is derived from the reference current via  $I_{LIM} = n \times I_{REF}$ , and  $I_{REF}$  is determined by  $I_{REF} = V_{REF}/R_{LIM}$ . Thus, changing the current limit requires the change of  $R_{LIM}$  to a different value via:  $R_{LIM} = n \times V_{REF}/I_{LIM}$ .

While the device is specified for a current limit of 3.6 mA, (via  $R_{LIM} = 25 \text{ k}\Omega$ ), it is easy to lower the current limit to further reduce the power consumption. For example, for a current limit of 2.5 mA simply calculate:

$$R_{LIM} = \frac{90}{I_{LIM}} = \frac{90}{2.5 \text{ mA}} = 36 \text{ k}\Omega$$

### Debounce Filter

The HVS882 applies a simple analog/digital filtering technique to remove unintended signal transitions due to contact bounce or other mechanical effects. Any new input (either low or high) must be present for the duration of the selected debounce time to be latched into the shift register as a valid state.

The logic signal levels at the control inputs, DB0 and DB1 of the internal Debounce-Select logic determine the different debounce times listed in the following truth table.

**Table 1. Debounce Times**

DB1	DB0	FUNCTION
Open	Open	3 ms delay
Open	GND	1 ms delay
GND	Open	0 ms delay (filter bypassed)
GND	GND	Reserved

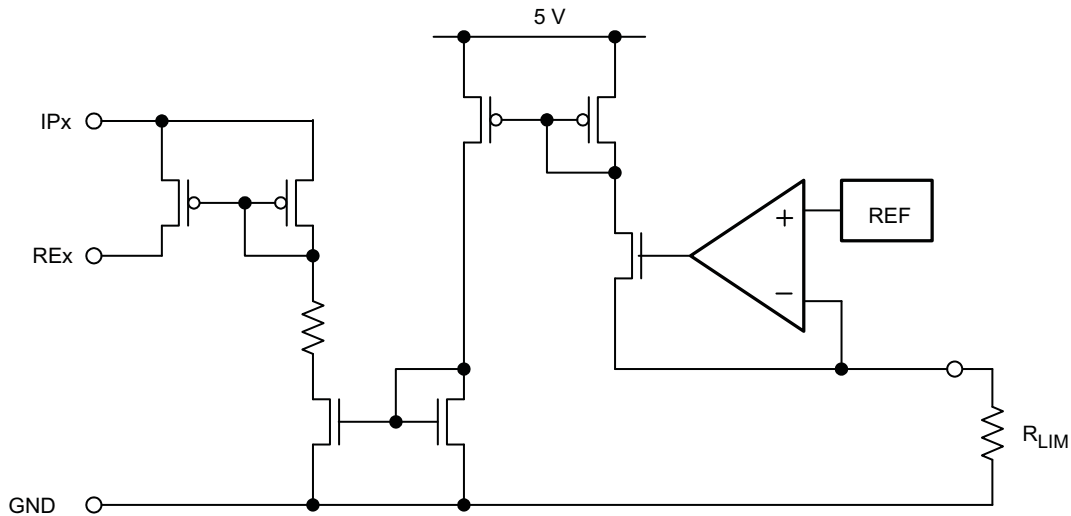


Figure 13. Equivalent Input Diagram

### Shift Register

The conversion from parallel input to serial output data is performed by an eight-channel serial-in parallel-out shift register. Parallel-in access is provided by the internal inputs, PIP0–PIP7, that are enabled by a low level at the load input (LD). When clocked, the latched input data shift towards the serial output (SOP). The shift register also provides a clock-enable function.

Clocking is accomplished by a low-to-high transition of the clock (CLK) input while  $\overline{LD}$  is held high and the clock enable ( $\overline{CE}$ ) input is held low. Parallel loading is inhibited when  $\overline{LD}$  is held high. The parallel inputs to the register are enabled while  $\overline{LD}$  is low independently of the levels of the CLK,  $\overline{CE}$ , or serial (SIP) inputs.

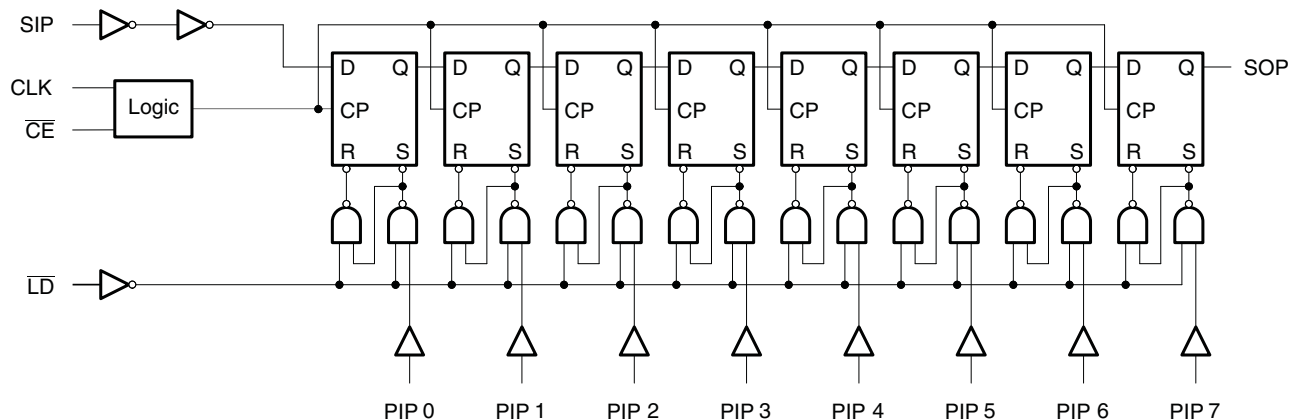


Figure 14. Shift Register Logic Structure

**Table 2. Function Table**

INPUTS			FUNCTION
$\overline{\text{LD}}$	CLK	$\overline{\text{CE}}$	
L	X	X	Parallel load
H	X	H	No change
H	↑	L	Shift <sup>(1)</sup>

(1) Shift = content of each internal register shifts towards serial outputs. Data at SIP is shifted into first register.

## Voltage Regulator

The on-chip linear voltage regulator provides a 5-V supply to the internal and external circuitry, such as digital isolators, with an output drive capability of 50 mA and a typical current limit of 115 mA. The regulator accepts input voltages from 30 V down to 10 V. Because the regulator output is intended to supply external digital isolator circuits proper output voltage decoupling is required. For best results connect a 1- $\mu\text{F}$  and a 0.1- $\mu\text{F}$  ceramic capacitor as close as possible to the 5VOP output. For longer traces between the SN65HVS882 and isolators of the ISO72xx family use additional 0.1- $\mu\text{F}$  and 10-pF capacitors next to the isolator supply pins. Make sure, however, that the total load capacitance does not exceed 4.7  $\mu\text{F}$ .

For good stability the voltage regulator requires a minimum load current,  $I_{L\text{-MIN}}$ . Ensure that under any operating condition the ratio of the minimum load current in mA to the total load capacitance in  $\mu\text{F}$  is larger than 1:

$$\frac{I_{L\text{-MIN}}}{C_L} > \frac{1 \text{ mA}}{1 \mu\text{F}}$$

## Temperature Sensor

An on-chip temperature sensor monitors the device temperature and signals a fault condition if the internal temperature reaches 150°C. If the internal temperature exceeds this trip point, the TOK output switches to an active low state. If the internal temperature continues to rise, passing a second trip point at 170°C, all device outputs are put in a high-impedance state.

A special condition occurs, however, when the chip temperature exceeds the second temperature trip point due to an output short. Then the output buffer becomes three-state, thus separating the buffer from the external circuitry. An internal 100-k $\Omega$  pull-down resistor, connecting the TOK pin to ground, is used as a *cooling down* resistor, which continues to provide a logic low level to the external circuitry.

### APPLICATION INFORMATION

#### System-Level EMC

The SN65HVS882 is designed to operate reliably in harsh industrial environments. At a system level, the device is tested according to several international electromagnetic compatibility (EMC) standards. In addition to the device internal ESD structures, external protection circuitry, as shown in Figure 15, can be used to absorb as much energy from burst- and surge-transients as possible.

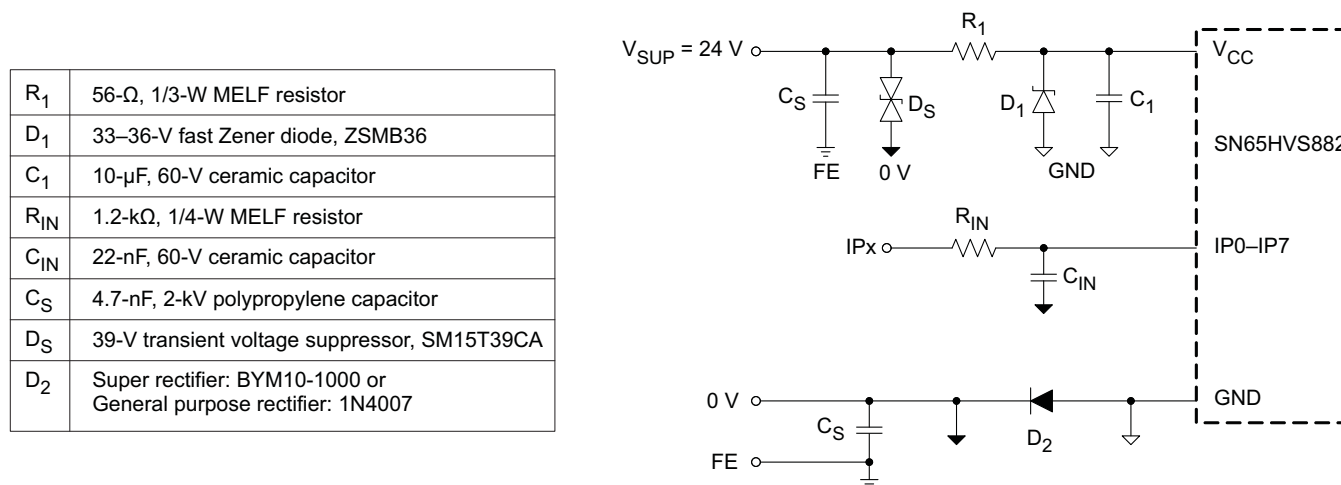


Figure 15. Typical EMC Protection Circuitry for Supply and Signal Inputs

#### Input Channel Switching for IEC61131-2 PLC Applications

The input stage of the SN65HVS882 is designed so that with a 24-V supply on V<sub>CC</sub> and an input resistor R<sub>IN</sub> = 1.2 kΩ, the trip point for signaling an ON-condition is at 9.4 V at 3.6 mA. This trip point satisfies the switching requirements of IEC61131-2 type-1 and type-3 switches.

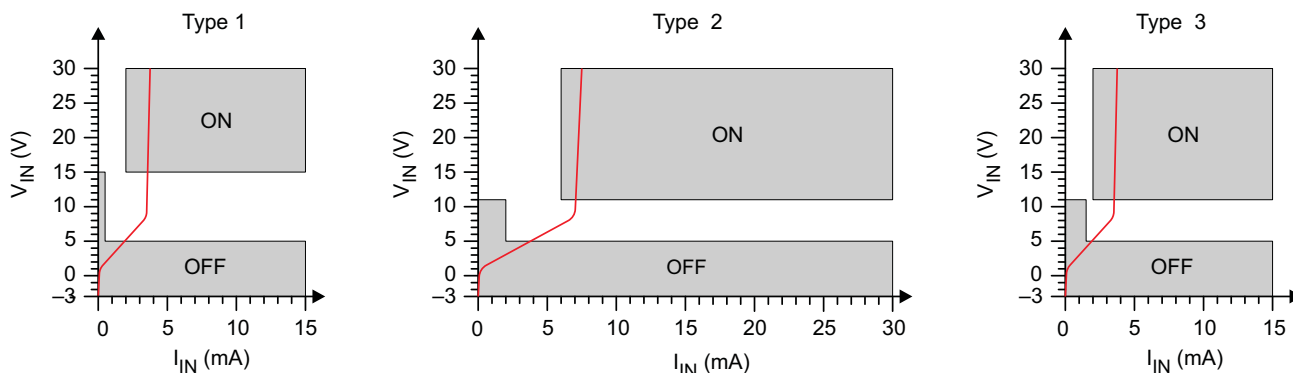


Figure 16. Switching Characteristics for IEC1131-2 Type 1, 2, and 3 Proximity Switches

For a type-2 switch application two inputs are connected in parallel. The current limiters then add to a total maximum current of 7.2 mA. While the return-path (RE-pin), of one input might be used to drive an indicator LED, the RE-pin of the other input channel should be connected to ground (GND).

Paralleling input channels reduces the number of available input channels from an octal Type 1 or Type 3 input to a quad Type 2 input device. Note, that in this configuration output data of an input channel is represented by two shift register bits.

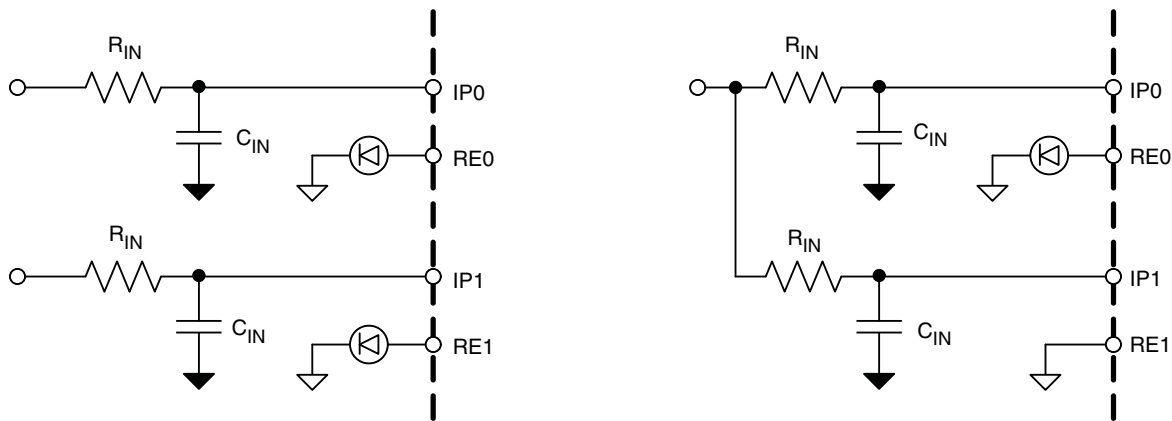


Figure 17. Paralleling Two Type 1 or Type 3 Inputs Into One Type 2 Input

### Digital Interface Timing

The digital interface of the SN65HVS882 is SPI compatible and interfaces, isolated or non-isolated, to a wide variety of standard microcontrollers.

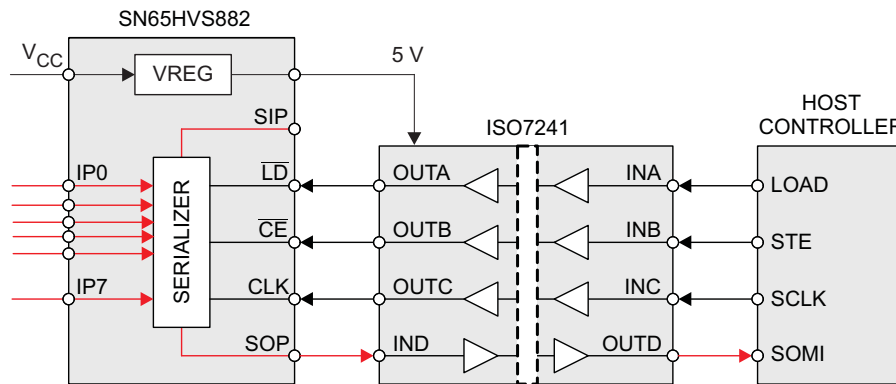


Figure 18. Simple Isolation of the Shift Register Interface

Upon a low-level at the load input,  $\overline{LD}$ , the information of the field inputs, IP0 to IP7 is latched into the shift register. Taking  $\overline{LD}$  high again blocks the parallel inputs of the shift register from the field inputs. A low-level at the clock-enable input,  $\overline{CE}$ , enables the clock signal, CLK, to serially shift the data to the serial output, SOP. Data is clocked at the rising edge of CLK. Thus after eight consecutive clock cycles all field input data have been clocked out of the shift register and the information of the serial input, SIP, appears at the serial output, SOP.

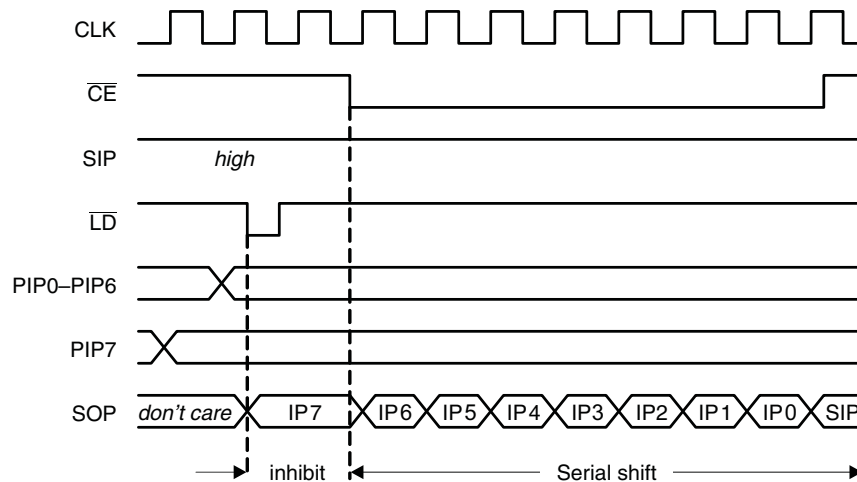


Figure 19. Interface Timing for Parallel-Load and Serial-Shift Operation of the Shift Register

### Cascading for High Channel Count Input Modules

Designing high-channel count modules requires cascading multiple SN65HVS882 devices. Simply connect the serial output (SOP) of a leading device with the serial input (SIP) of a following device without changing the processor interface.

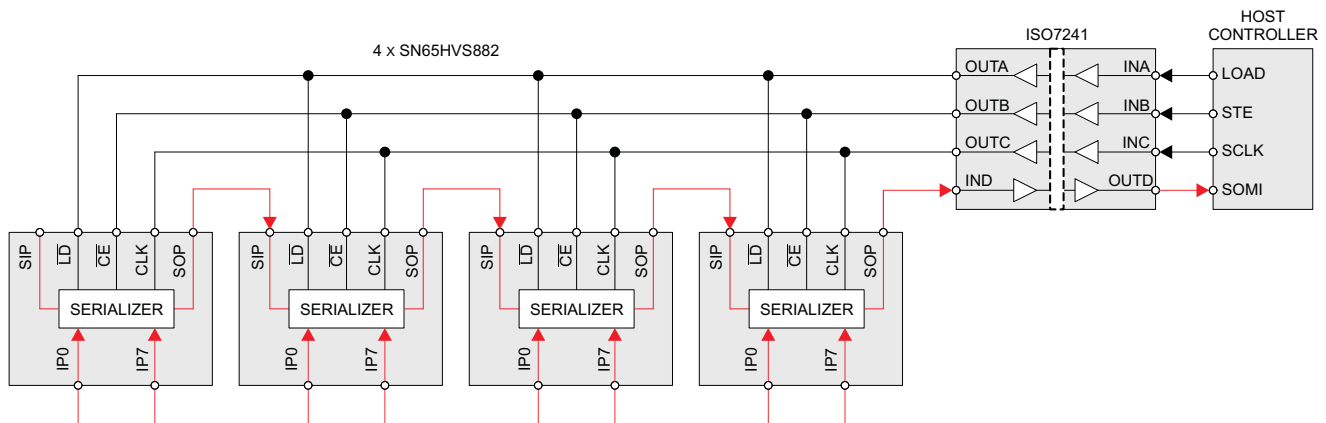


Figure 20. Cascading Four SN65HVS882 for a 32-Channel Input Module

### Typical Digital Input Module Application

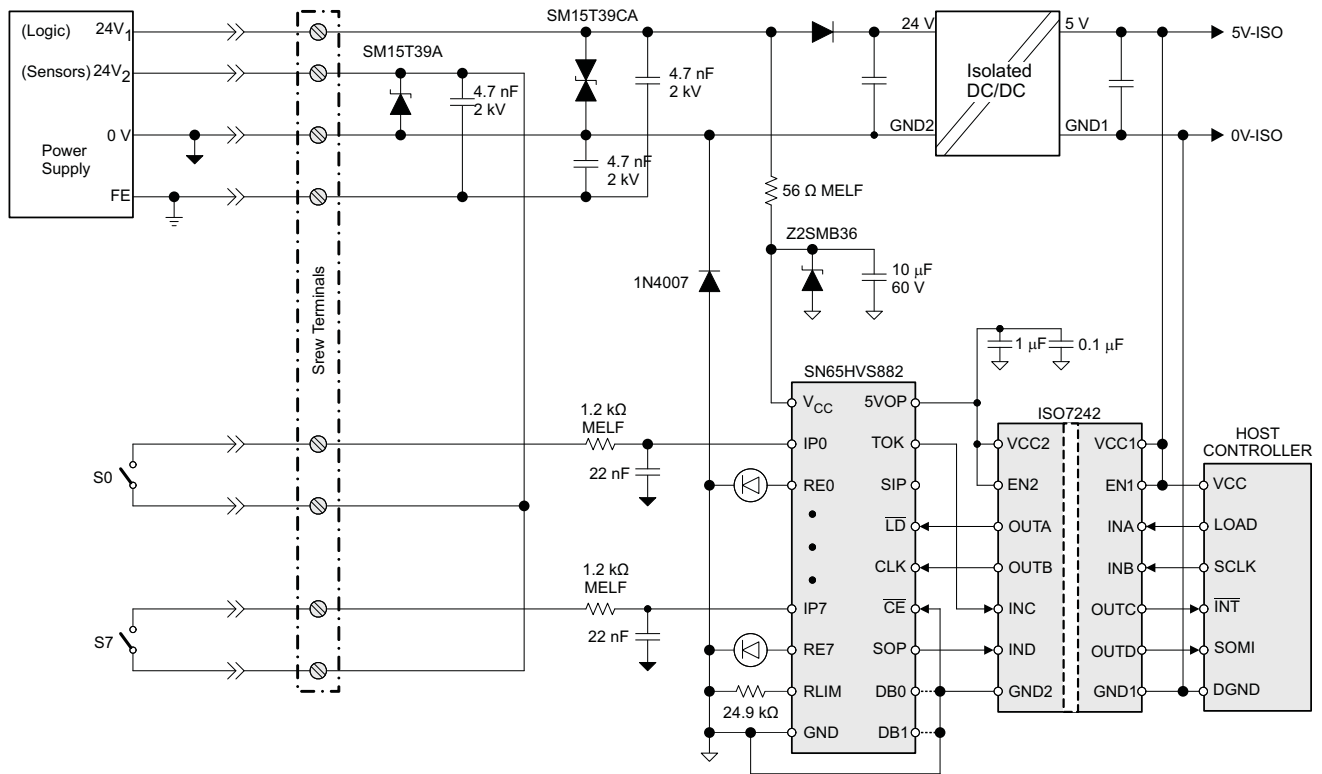


Figure 21. Typical Digital Input Module Application

**PACKAGING INFORMATION**

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
SN65HVS882PWPR	ACTIVE	HTSSOP	PWP	28	2000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	HVS882	<a href="#">Samples</a>
SN65HVS882PWPRG4	ACTIVE	HTSSOP	PWP	28	2000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	HVS882	<a href="#">Samples</a>

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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**TAPE AND REEL INFORMATION**

**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN65HVS882PWPR	HTSSOP	PWP	28	2000	330.0	16.4	6.9	10.2	1.8	12.0	16.0	Q1

**TAPE AND REEL BOX DIMENSIONS**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN65HVS882PWPR	HTSSOP	PWP	28	2000	350.0	350.0	43.0

## GENERIC PACKAGE VIEW

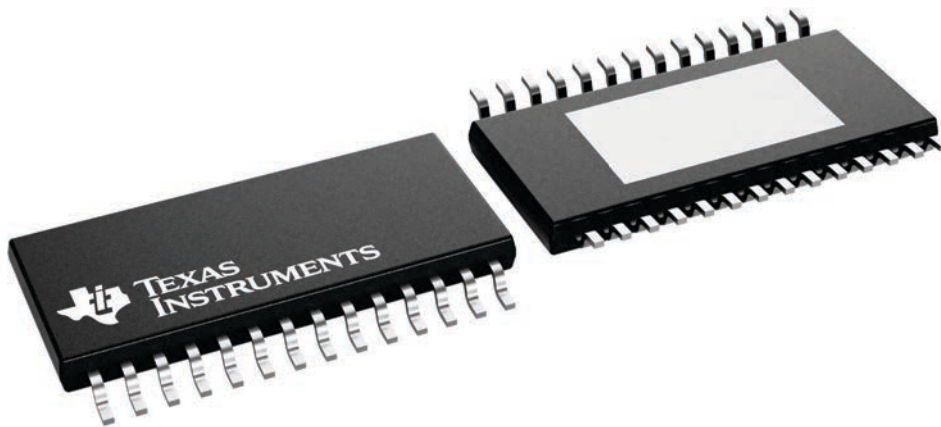
**PWP 28**

**PowerPAD™ TSSOP - 1.2 mm max height**

4.4 x 9.7, 0.65 mm pitch

SMALL OUTLINE PACKAGE

This image is a representation of the package family, actual package may vary.  
Refer to the product data sheet for package details.

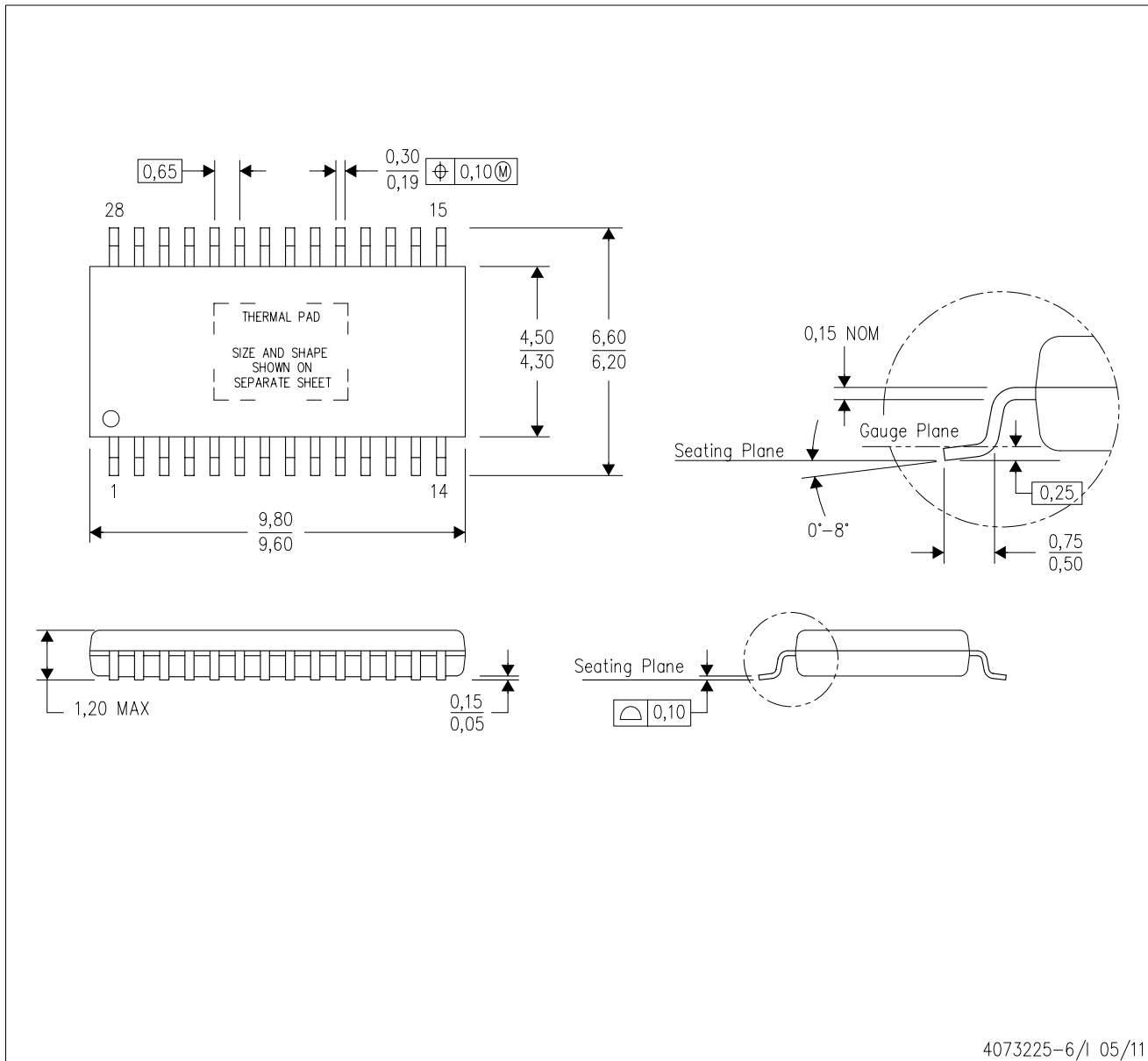


4224765/B

# MECHANICAL DATA

PWP (R-PDSO-G28)

PowerPAD™ PLASTIC SMALL OUTLINE



- NOTES:
- All linear dimensions are in millimeters.
  - This drawing is subject to change without notice.
  - Body dimensions do not include mold flash or protrusions. Mold flash and protrusion shall not exceed 0.15 per side.
  - This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPad Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 for information regarding recommended board layout. This document is available at [www.ti.com](http://www.ti.com) <<http://www.ti.com>>.
  - See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.
  - Falls within JEDEC MO-153

PowerPAD is a trademark of Texas Instruments.

# THERMAL PAD MECHANICAL DATA

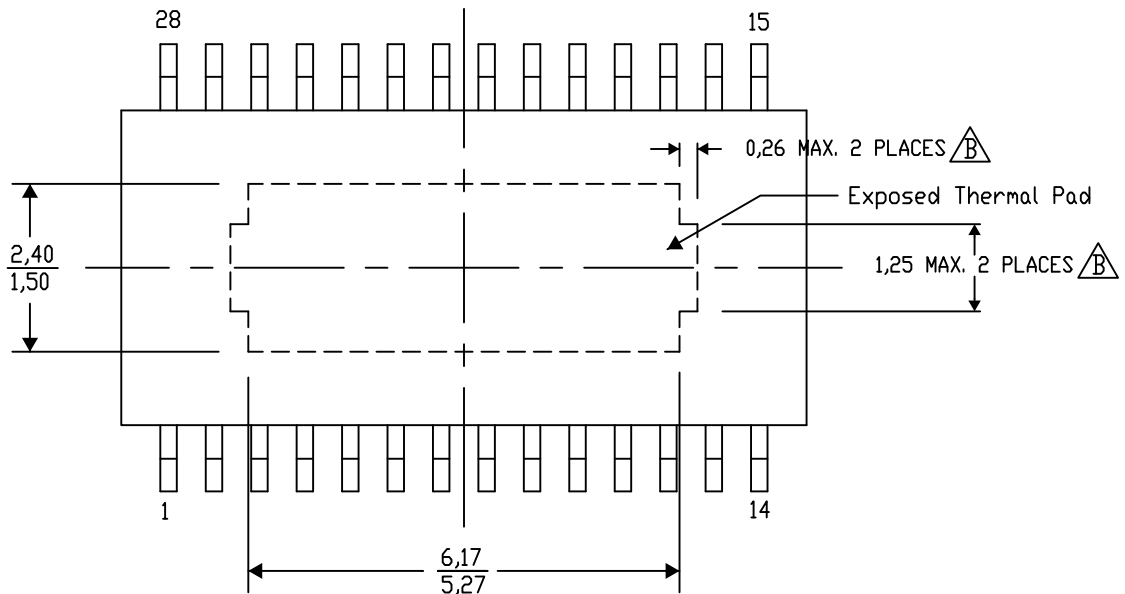
## PWP (R-PDSO-G28) PowerPAD™ SMALL PLASTIC OUTLINE

### THERMAL INFORMATION

This PowerPAD™ package incorporates an exposed thermal pad that is designed to be attached to a printed circuit board (PCB). The thermal pad must be soldered directly to the PCB. After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For additional information on the PowerPAD package and how to take advantage of its heat dissipating abilities, refer to Technical Brief, PowerPAD Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 and Application Brief, PowerPAD Made Easy, Texas Instruments Literature No. SLMA004. Both documents are available at [www.ti.com](http://www.ti.com).

The exposed thermal pad dimensions for this package are shown in the following illustration.



Top View

Exposed Thermal Pad Dimensions

4206332-33/AO 01/16

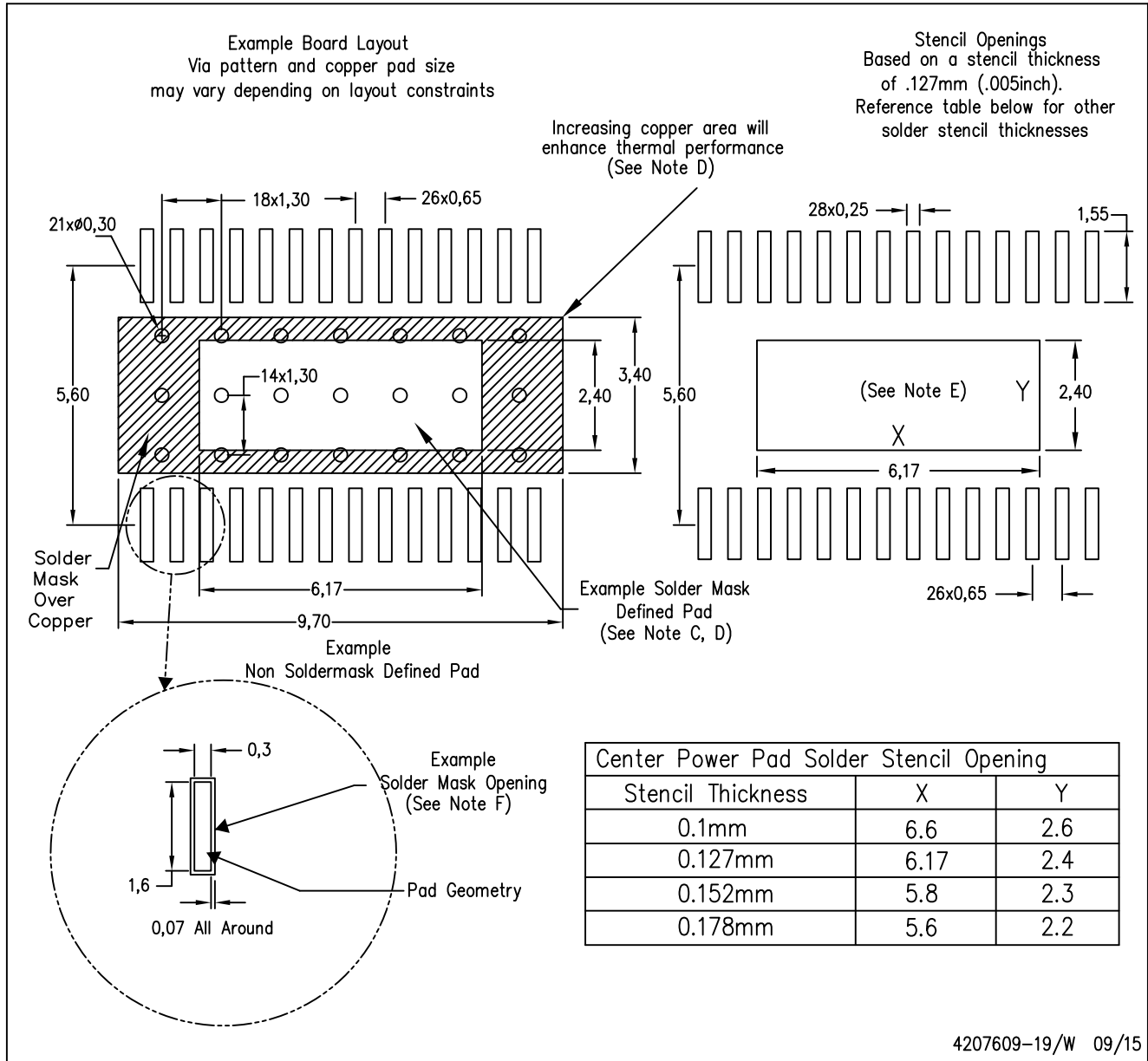
NOTE: A. All linear dimensions are in millimeters

$\triangle B$ . Exposed tie strap features may not be present.

PowerPAD is a trademark of Texas Instruments

PWP (R-PDSO-G28)

PowerPAD™ PLASTIC SMALL OUTLINE



- NOTES:
- All linear dimensions are in millimeters.
  - This drawing is subject to change without notice.
  - Customers should place a note on the circuit board fabrication drawing not to alter the center solder mask defined pad.
  - This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPad Thermally Enhanced Package, Texas Instruments Literature No. SLMA002, SLMA004, and also the Product Data Sheets.
  - For specific thermal information, via requirements, and recommended board layout. These documents are available at [www.ti.com](http://www.ti.com) <<http://www.ti.com>>. Publication IPC-7351 is recommended for alternate designs. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC-7525 for other stencil
  - Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

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