



**THE DATASHEET OF
SI53302-B-GM**





Si5330x Data Sheet

Ultra-Low Additive Jitter Fanout Clock Buffers with up to 10 Universal Outputs from Any-Format Input and Wide Frequency Range from 1 MHz to 725 MHz

The Si5330x family of Universal/Any-format fanout buffers is ideal for clock distribution (1 MHz minimum) and redundant clocking applications. These devices feature typical ultra-low jitter characteristics of 50 fs and operate over a wide frequency range. Built-in LDOs deliver high PSRR performance and reduce the need for external components, simplifying low-jitter clock distribution in noisy environments.

The Si5330x family is available in multiple configurations, with some versions offering a selectable input clock using a 2:1 input mux. Other features include independent (synchronous) output enable, glitchless switching, LOS monitor of input clocks, output clock division, and built-in format translation. These buffers can be paired with the Si534x clocks and jitter attenuators, the Si5332 clocks, and the Si5xx oscillators to deliver end-to-end clock tree performance.

KEY FEATURES

- Ultra-low additive jitter: 50 fs rms
- Built-in LDOs for high PSRR performance
- Up to 10 outputs
- Any-format Inputs (LVPECL, Low-power LVPECL, LVDS, CML, HCSSL, LVCMOS)
- Wide frequency range
- Output Enable option
- Multiple configuration options
 - Dual Bank option
 - 2:1 Input Mux operation
- Synchronous output enable
- Loss of signal (LOS) monitors for loss of input clock
- Output clock division: /1, /2, /4
- RoHS compliant, Pb-free
- Temperature range: -40 to +85 °C

1. Ordering Guide

Table 1.1. Product Family Overview

| Part Number | Description | Input MUX | Input | Output | Glitch-less Switch ¹ | LOS Output | OE Option | Synchronous OE ¹ | Clk Divider Option |
|--------------|---|-----------|-------|-----------------|---------------------------------|------------|------------|-----------------------------|--------------------|
| Si53301-B-GM | 6 output universal buffer with 2:1 input mux | Yes | 2 | 6 Diff / 12 SE | Yes | Yes | Per Bank | Yes | Per Bank |
| Si53302-B-GM | 10 output universal buffer with 2:1 input mux | Yes | 2 | 10 Diff / 20 SE | Yes | Yes | Per Bank | Yes | Per Bank |
| Si53303-B-GM | Dual 1:5 universal buffer | No | 2 | 5 Diff / 10 SE | No | No | Per Bank | Yes | Per Bank |
| Si53304-B-GM | 6 output universal buffer with 2:1 input mux | Yes | 2 | 6 Diff / 12 SE | Yes | No | Individual | Yes | No |
| Si53305-B-GM | 10 output universal buffer with 2:1 input mux | Yes | 2 | 10 Diff / 20 SE | Yes | No | Individual | Yes | No |
| Si53306-B-GM | 4 output universal buffer, single input | No | 1 | 4 Diff / 8 SE | No | No | Single | Yes | No |
| Si53307-B-GM | 2 output universal buffer with 2:1 input mux | Yes | 2 | 2 Diff / 4 SE | Yes | No | Single | Yes | No |
| Si53308-B-GM | Dual 1:3 universal buffer | No | 2 | 3 Diff / 6 SE | No | Yes | Per Bank | Yes | Per Bank |

Note:

- The synchronous features (Glitch-less switching and Synchronous OE) of the Si533xx family require a minimum input clock frequency of 1 MHz. If the selected input clock stops, pauses, or is gapped such that the 1 MHz minimum is not met for any time interval, then the output clock(s) will be disabled (turned off). Once the paused input clock restarts, the output clock may NOT start up immediately. Output start-up (turning back on) may be delayed for several input clock cycles until the internal synchronizer determines the input clock is once again valid.
- Click on the part number above to see a block diagram for each corresponding part number.

Table 1.2. Si5330x Ordering Guide

| Part Number | Package | Pb-Free, ROHS-6 | Temperature |
|---------------------------|------------------|-----------------|--------------|
| Si53301-B-GM ¹ | 32-QFN | Yes | -40 to 85 °C |
| Si53302-B-GM ¹ | 44-QFN | Yes | -40 to 85 °C |
| Si53303-B-GM ¹ | 44-QFN | Yes | -40 to 85 °C |
| Si53304-B-GM ¹ | 32-QFN | Yes | -40 to 85 °C |
| Si53305-B-GM ¹ | 44-QFN | Yes | -40 to 85 °C |
| Si53306-B-GM ¹ | 16-QFN | Yes | -40 to 85 °C |
| Si53307-B-GM ¹ | 16-QFN | Yes | -40 to 85 °C |
| Si53308-B-GM ¹ | 32-QFN | Yes | -40 to 85 °C |
| Si53301/4-EVB | Evaluation Board | — | — |

Note:

- Add an "R" at the end of the OPN to denote tape and reel ordering options.

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2. Functional Description

The Si5330x family of low-jitter, low-skew, universal/any-format buffers accepts most common differential or LVCMOS input signals. These devices are available in multiple configurations customized for the end application (refer to [1. Ordering Guide](#) for more details on configurations).

2.1 Universal, Any-Format Input Termination

The universal input stage enables simple interfacing to a wide variety of clock formats, including LVPECL, low-power LVPECL, LVCMOS, LVDS, HCSL, and CML. The simplified tables below summarize the various ac- and dc-coupling options supported by the device. For the best high-speed performance, the use of differential formats is recommended. For both single-ended and differential input clocks, the fastest possible slew rate is recommended since low slew rates can increase the noise floor and degrade jitter performance. Though not required, a minimum slew rate of 0.75 V/ns is recommended for differential formats and 1.0 V/ns for single-ended formats. See [AN766: Understanding and Optimizing Clock Buffer's Additive Jitter Performance](#) for more information.

Table 2.1. AC-Coupled Clock Input Options

| Clock Format | 1.8 V | 2.5/3.3 V |
|-------------------------|-------|-----------|
| LVPECL/Low-power LVPECL | N/A | Yes |
| LVCMOS | No | Yes |
| LVDS | Yes | Yes |
| HCSL | No | Yes |
| CML | Yes | Yes |

Table 2.2. DC-Coupled Clock Input Options

| Clock Format | 1.8 V | 2.5/3.3 V |
|-------------------------|-------|-----------|
| LVPECL/Low-power LVPECL | N/A | Yes |
| LVCMOS | No | Yes |
| LVDS | No | Yes |
| HCSL | No | Yes |
| CML | No | No |

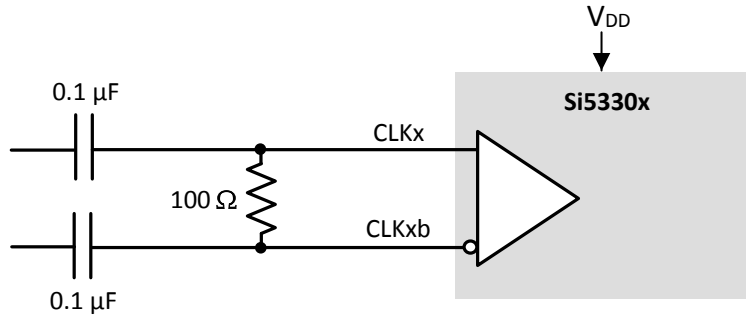
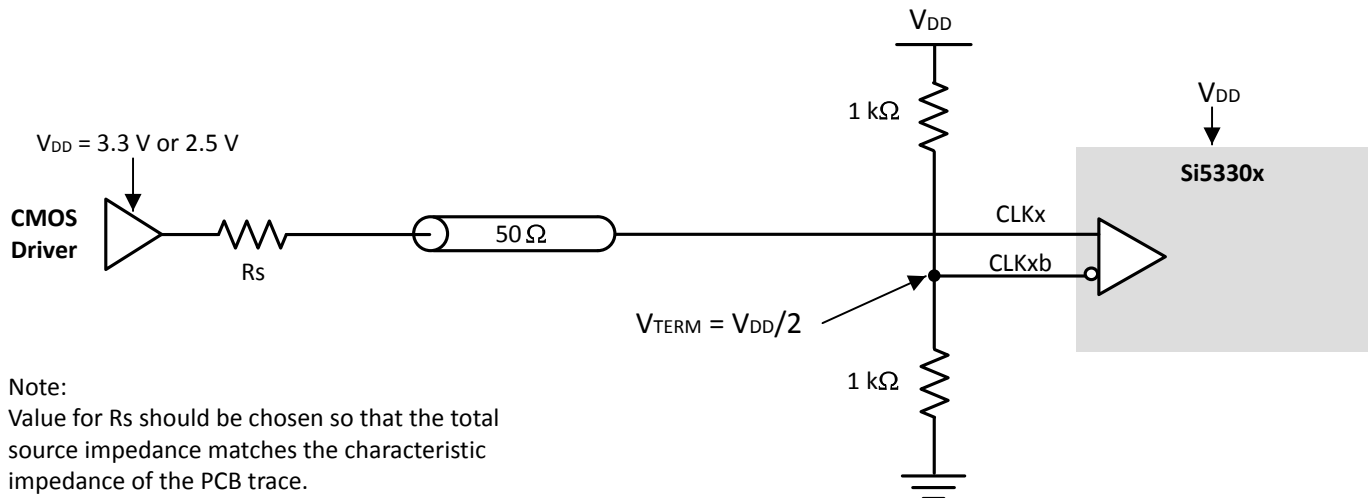
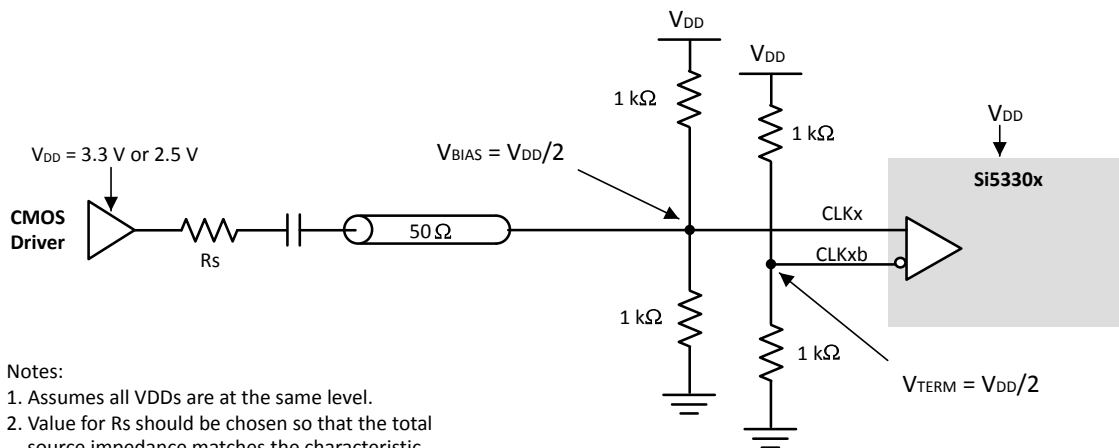


Figure 2.1. Differential (HCSL, LVPECL, Low-Power LVPECL, LVDS, CML) AC-Coupled Input Termination



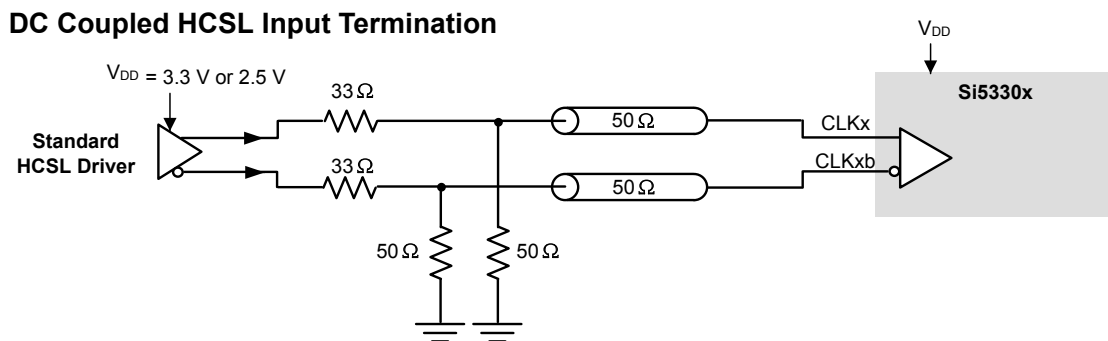
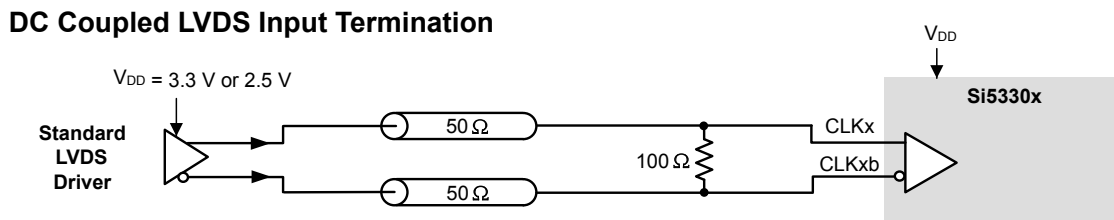
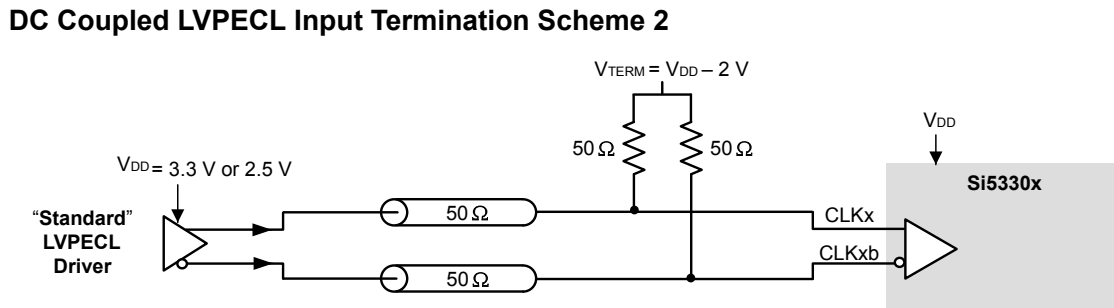
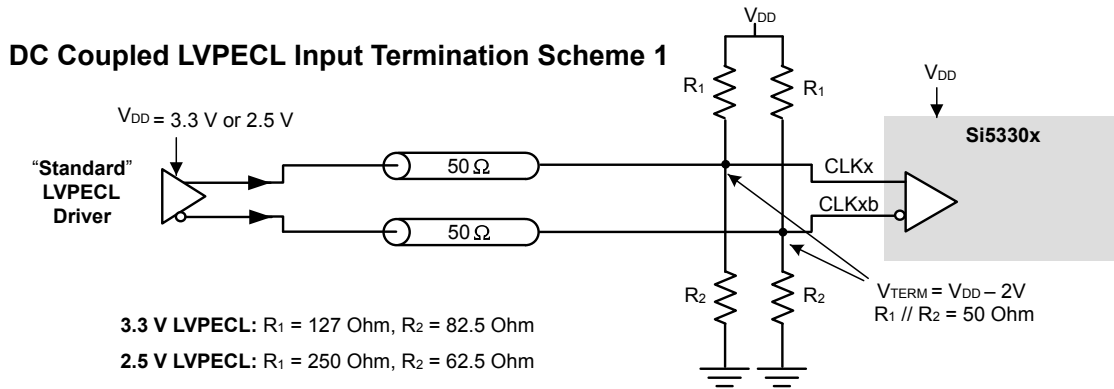
Note:
Value for R_s should be chosen so that the total source impedance matches the characteristic impedance of the PCB trace.

Figure 2.2. DC-Coupled, Single-Ended (LVCMOS) Input Termination



Notes:
1. Assumes all VDDs are at the same level.
2. Value for R_s should be chosen so that the total source impedance matches the characteristic impedance of the PCB trace.

Figure 2.3. AC-Coupled, Single-Ended (LVCMOS) Input Termination



Note: 33 Ohm series termination is optional depending on the location of the receiver.

Figure 2.4. Differential DC-Coupled Input Terminations

Table 2.3. AC/DC-Coupled Clock Input Requirements for Glitchless, Non-Continuous Clocks^{1, 2, 3}

| Clock Input Type | Input Clock Driver Stop State | | |
|------------------|-------------------------------|------|--------|
| | Low | High | High-Z |
| DC-Coupled | Yes | Yes | No |
| AC-Coupled | Yes | No | No |

Note:

1. "Non-continuous clocks" means any clock that can be stopped, disabled, or gapped.
2. "Yes" means this configuration is supported.
3. "No" indicates that the configuration is not supported. Operating under a "No" condition can result in erroneous clock outputs and/or erroneous LOS indications. Operating the device in unsupported configurations is not recommended.

2.2 Internal Input Bias Resistors

Internal bias resistors ensure a differential output low condition in the event that the clock inputs are not connected. The clock input should not be actively driven when power is not applied to the device. The non-inverting input is biased with a 18.75 k Ω pull-down to GND and a 75 k Ω pull-up to V_{DD}. The inverting input is biased with a 75 k Ω pull-up to V_{DD}.

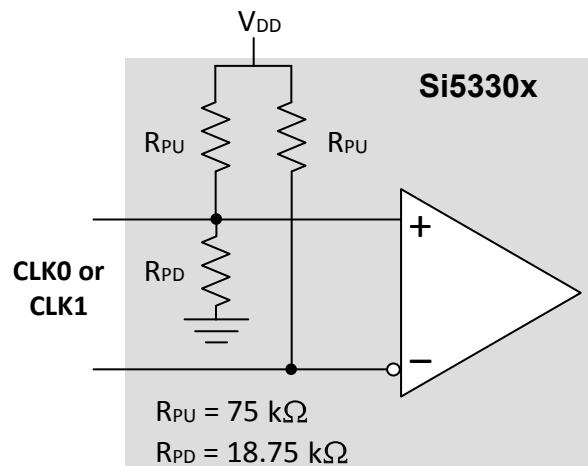


Figure 2.5. Internal Input Bias Resistors

2.3 Voltage Reference (V_{REF})

The V_{REF} pin can be used to bias the input receiver, as shown in the figure below, when a single-ended input clock (such as LVCMOS) is used. Note that $V_{REF} = V_{DD}/2$ and should be compatible with the V_{cm} rating of the single-ended input clock driving the CLK0 or CLK1 inputs. To optimize jitter and duty cycle performance, use the circuit in [Figure 2.3 AC-Coupled, Single-Ended \(LVCMOS\) Input Termination on page 6](#). V_{REF} pin should be left floating when differential clocks are used.

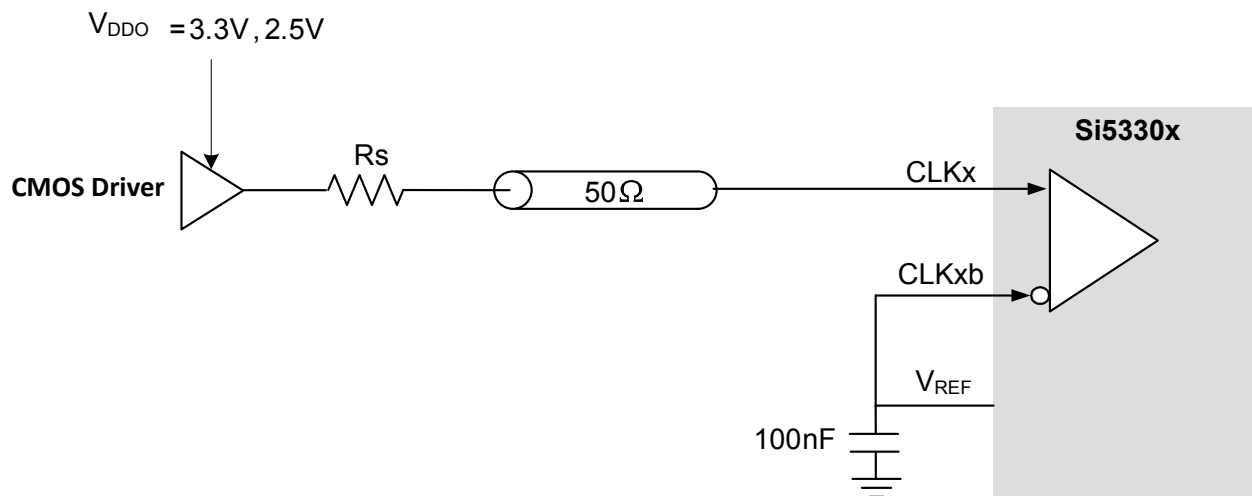


Figure 2.6. Using Voltage Reference with Single-Ended Input Clock

2.4 Universal, Any-Format Output Buffer

The highly flexible output drivers support a wide range of clock signal formats, including LVPECL, low power LVPECL, LVDS, CML, HCSL, and LVCMOS. SFOUTx[1] and SFOUTx[0] are 3-level inputs that can be pinstrapped to select the Bank A and Bank B clock signal formats independently. This feature enables the device to be used for format/level translation in addition to clock distribution, minimizing the number of unique buffer part numbers required in a typical application and simplifying design reuse. For EMI reduction applications, four LVCMOS drive strength options are available for each V_{DDO} setting.

Table 2.4. Output Signal Format Selection

| SFOUTx[1] | SFOUTx[0] | VDDOX = 3.3 V | VDDOX = 2.5 V | VDDOX = 1.8 V |
|-------------------|-------------------|---------------------|---------------------|---------------------|
| Open ¹ | Open ¹ | LVPECL | LVPECL | N/A |
| 0 | 0 | LVDS | LVDS | LVDS |
| 0 | 1 | LVCMOS, 24 mA drive | LVCMOS, 18 mA drive | LVCMOS, 12 mA drive |
| 1 | 0 | LVCMOS, 18 mA drive | LVCMOS, 12 mA drive | LVCMOS, 9 mA drive |
| 1 | 1 | LVCMOS, 12 mA drive | LVCMOS, 9 mA drive | LVCMOS, 6 mA drive |
| Open ¹ | 0 | LVCMOS, 6 mA drive | LVCMOS, 4 mA drive | LVCMOS, 2 mA drive |
| Open ¹ | 1 | LVPECL Low power | LVPECL Low power | N/A |
| 0 | Open ¹ | CML | CML | CML |
| 1 | Open ¹ | HCSL | HCSL | N/A |

Note:

1. SFOUTx[1:0] are 3-level input pins. Tie low for “0” setting. Tie high for “1” setting. When left open, the pin is internally biased to $V_{DD}/2$.

2.5 Input Mux (Si53301/02/04/05/07 Only)

The Si53301/02/04/05/07 provide two clock inputs for applications that need to select between one of two clock sources. The CLK_SEL pin selects the active clock input and has an internal pulldown resistor. The following table summarizes the input and output clock based on the input mux pin settings.

Table 2.5. Input Mux Logic

| CLK_SEL | CLK0 | CLK1 | Q ¹ | Q _b |
|---------|------|------|----------------|----------------|
| L | L | X | L | H |
| L | H | X | H | L |
| H | X | L | L | H |
| H | X | H | H | L |

Note:

1. On the next negative transition of CLK0 or CLK1.

2.6 Glitchless Clock Input Switching

The Si53301/2/4/5/7 feature glitchless switching between two valid input clocks. The following figure illustrates that switching between input clocks does not generate runt pulses or glitches at the output.

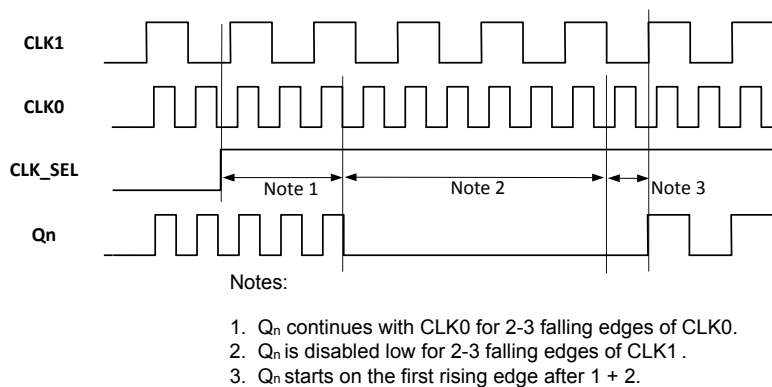


Figure 2.7. Glitchless Input Clock Switch

The Si53301/2/4/5/7 support glitchless switching between clock inputs with a frequency variance up to 10x. When a switchover to a new clock is made, the output will disable low after two or three clock cycles of the previously selected input clock. The outputs will remain low for up to three clock cycles of the newly-selected clock, after which the outputs will start from the newly-selected input. If a switchover to an absent clock is made, the output will glitchlessly stop low and wait for edges of the newly-selected clock. A switchover from an absent clock to a live clock will also be glitchless. Note that the CLK_SEL input should not be toggled faster than 1/250th the frequency of the slower input clock.

2.7 Synchronous Output Enable

The Si5330x features a synchronous output enable (disable) feature. The output enable pin is sampled and synchronized to the falling edge of the input clock. This feature prevents runt pulses from being generated when the outputs are enabled or disabled.

When OE is low, Q is held low and Q_b is held high for differential output formats. For LVCMOS output format options, both Q and Q_b are held low when OE is set low. The output enable pin has an internal pull-up that enables the outputs when left unconnected. See [Table 3.10 AC Characteristics on page 23](#) for output enable and output disable times.

2.8 Loss of Signal (LOS) Indicator

Si53301/2/8 feature a Loss of Signal (LOS) indicator. The LOS0 and LOS1 indicators are used to check for the presence of input clocks CLK0 and CLK1. The LOS0 and LOS1 pins must be checked prior to selecting the clock input or should be polled to check for the presence of the currently selected input clock. In the event that an input clock is not present, the associated LOSx pin will assume a logic high (LOSx = 1) state. When a clock is present at the associated input clock pin, the LOSx pin will assume a logic low (LOSx = 0) state.

2.9 Flexible Output Divider

The Si53301/02/03/08 provide optional clock division in addition to clock distribution. The divider setting for each bank of output clocks is selected via 3-level control pins as shown in the table below. Leaving the DIVx pins open will force a divider value of 1, which is the default mode of operation.

Table 2.6. Divider Selection

| DIVx ¹ | Divider Value |
|-------------------|---------------|
| Open | ÷1 (default) |
| 0 | ÷2 |
| 1 | ÷4 |

Notes:

1. DIVx are 3-level input pins. Tie low for “0” setting. Tie high for “1” setting. When left open, the pin is internally biased to $V_{DD}/2$.

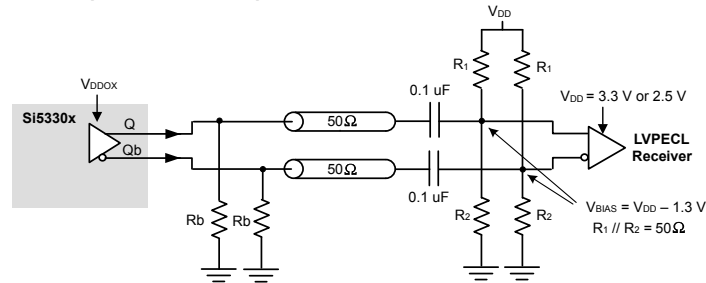
2.10 Power Supply (V_{DD} and V_{DDOX})

The device includes separate core (V_{DD}) and output driver supplies (V_{DDOX}). This feature allows the core to operate at a lower voltage than V_{DDO} , reducing current consumption in mixed supply applications. The core V_{DD} supports 3.3, 2.5, or 1.8 V. Control signals, such as CLK_SEL, DIV, and OE, are in the VDD domain. Each output bank has its own V_{DDOX} supply, supporting 3.3, 2.5, or 1.8 V.

2.11 Output Clock Termination Options

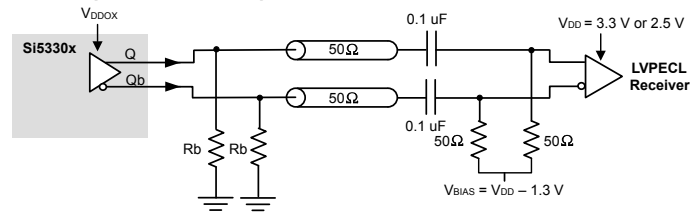
The recommended output clock termination options for ac and dc are shown below. Unused outputs should be left unconnected.

AC-Coupled LVPECL Output Termination Scheme 1



3.3 V LVPECL: $R_1 = 82.5 \Omega$; $R_2 = 127 \Omega$; $R_b = 120 \Omega$
2.5 V LVPECL: $R_1 = 62.5 \Omega$; $R_2 = 250 \Omega$; $R_b = 90 \Omega$

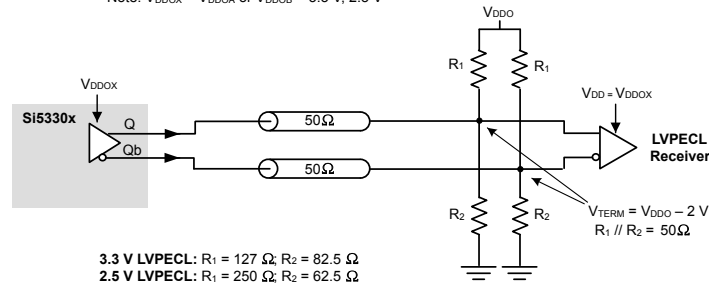
AC-Coupled LVPECL Output Termination Scheme 2



3.3 V LVPECL: $R_b = 120 \Omega$
2.5 V LVPECL: $R_b = 90 \Omega$

DC-Coupled LVPECL Output Termination Scheme 1

Note: $V_{DD0x} = V_{DD0A}$ or $V_{DD0B} = 3.3 \text{ V}, 2.5 \text{ V}$



3.3 V LVPECL: $R_1 = 127 \Omega$; $R_2 = 82.5 \Omega$
2.5 V LVPECL: $R_1 = 250 \Omega$; $R_2 = 62.5 \Omega$

DC-Coupled LVPECL Output Termination Scheme 2

Note: $V_{DD0x} = V_{DD0A}$ or $V_{DD0B} = 3.3 \text{ V}, 2.5 \text{ V}$

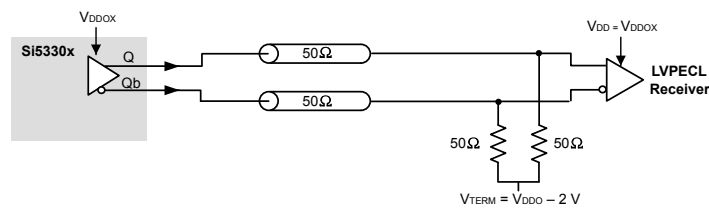


Figure 2.8. LVPECL AC and DC Output Terminations

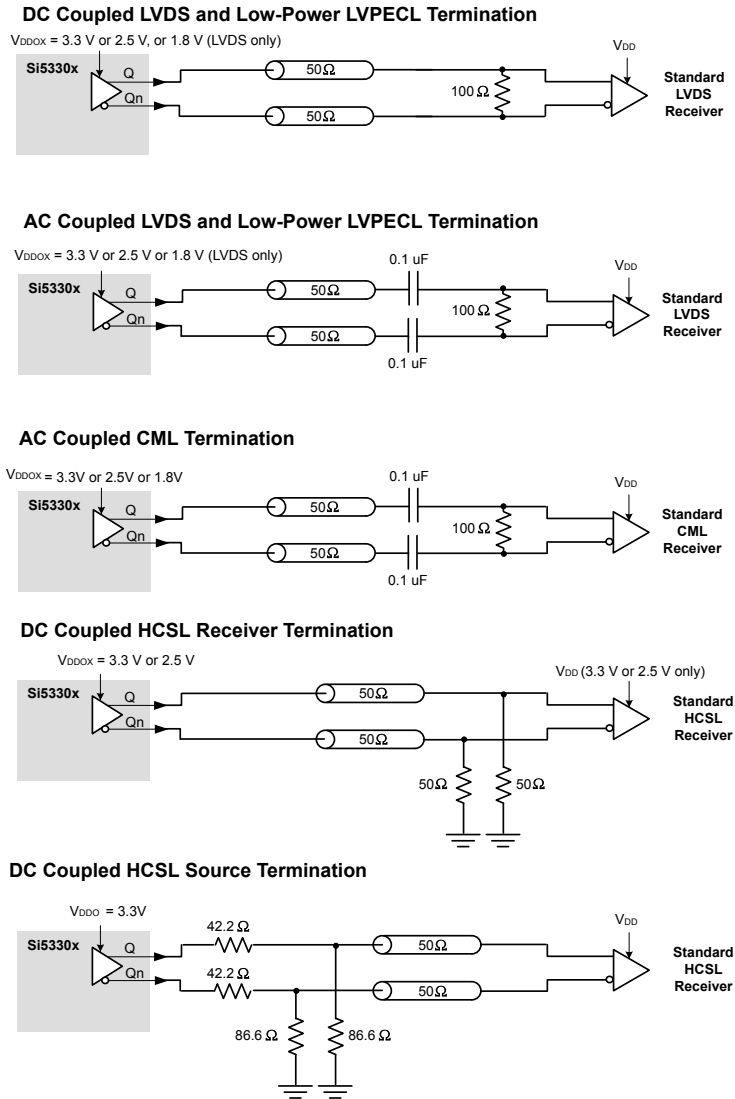


Figure 2.9. LVDS, CML, HCSSL, and Low-Power LVPECL Output Terminations

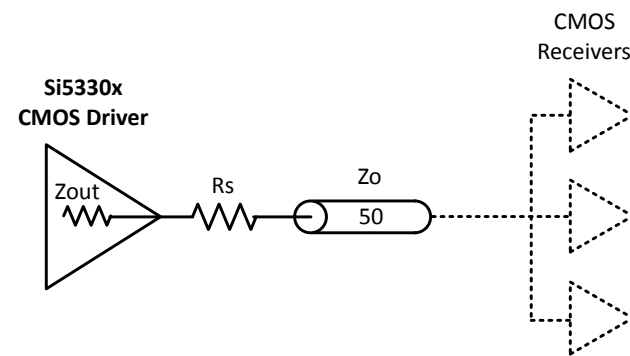


Figure 2.10. LVCMOS Output Termination

Table 2.7. Recommended LVCMOS R_S Series Termination

| SFOUTX[1] | SFOUTX[0] | R_S (Ω) | | |
|-----------|-----------|--------------------|-------|-------|
| | | 3.3 V | 2.5 V | 1.8 V |
| 0 | 1 | 33 | 33 | 33 |

| SFOUTX[1] | SFOUTX[0] | R_S (Ω) | | |
|-----------|-----------|--------------------|----|----|
| 1 | 0 | 33 | 33 | 33 |
| 1 | 1 | 33 | 33 | 0 |
| Open | 0 | 0 | 0 | 0 |

2.12 LVCMOS Output Termination to Support 1.5 V and 1.2 V

LVCMOS clock outputs are natively supported at 1.8, 2.5, and 3.3 V. However, 1.2 V and 1.5 V LVCMOS clock outputs can be supported via a simple resistor divider network that will translate the buffer's 1.8 V output to a lower voltage as shown in the following figure.

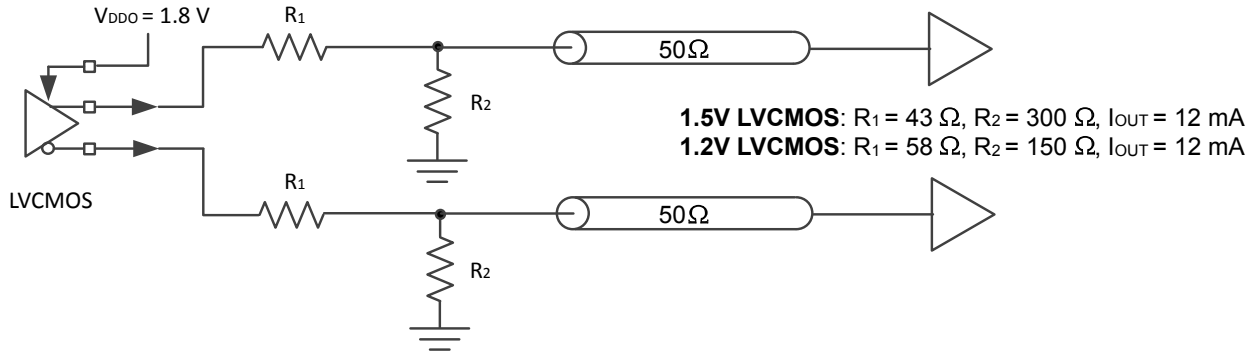


Figure 2.11. 1.5 V and 1.2 V LVCMOS Low-Voltage Output Termination

2.13 AC Timing Waveforms

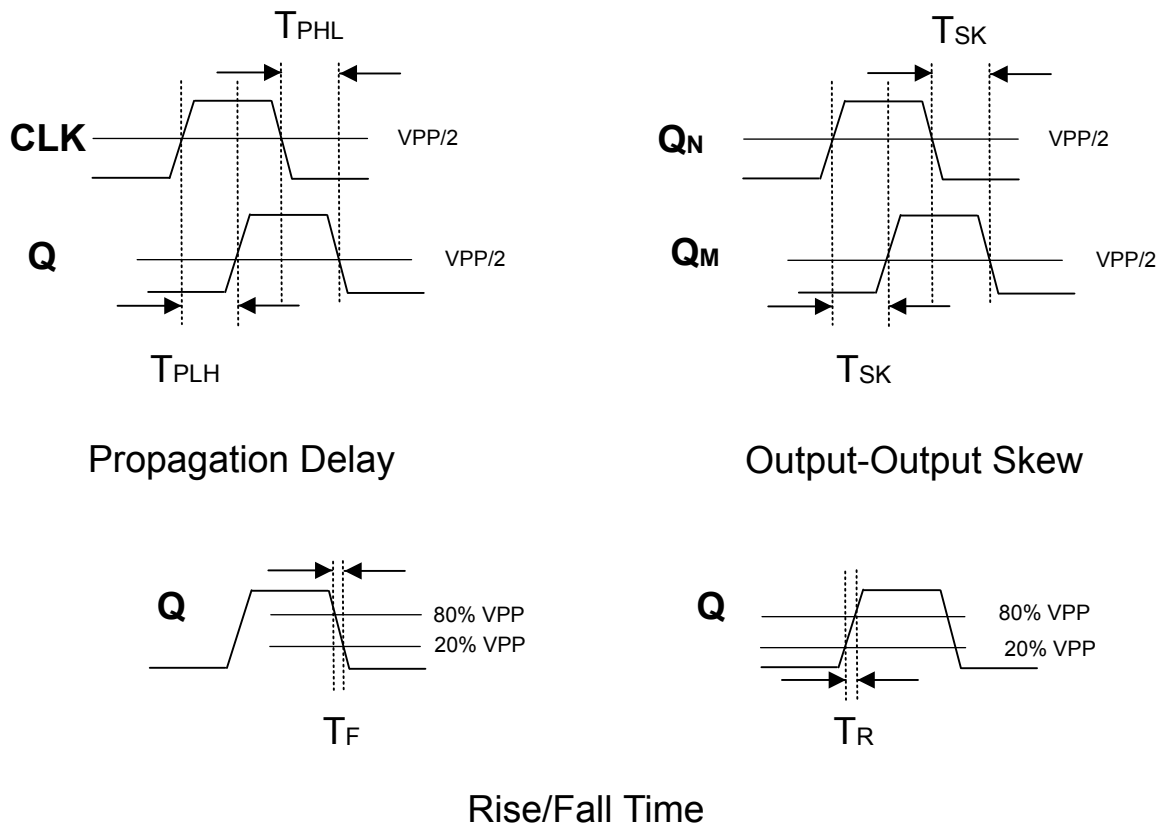


Figure 2.12. AC-Coupled Timing Waveforms

2.14 Typical Phase Noise Performance (Differential Input Clock)

Each of the phase noise plots superimposes Source Jitter, Total SE Jitter, and Total Diff Jitter on the same diagram.

- **Source Jitter**—Reference clock phase noise (measured Single-ended to PNA).
- **Total Jitter (SE)**—Combined source and clock buffer phase noise measured as a single-ended output to the phase noise analyzer and integrated from 12 kHz to 20 MHz.
- **Total Jitter (Diff)**—Combined source and clock buffer phase noise measured as a differential output to the phase noise analyzer and integrated from 12 kHz to 20 MHz. The differential measurement as shown in each figure is made using a balun. For more information, see 3. Electrical Specifications.

Note: To calculate the total RMS phase jitter when adding a buffer to your clock tree, use the root-sum-square (RSS).

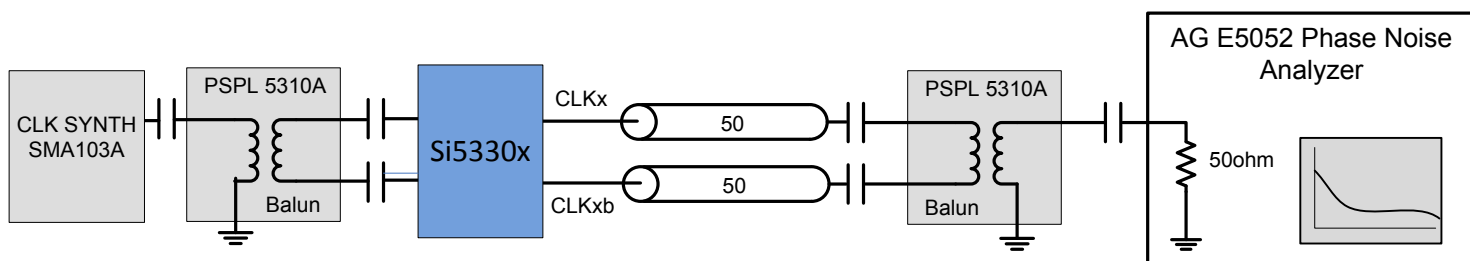
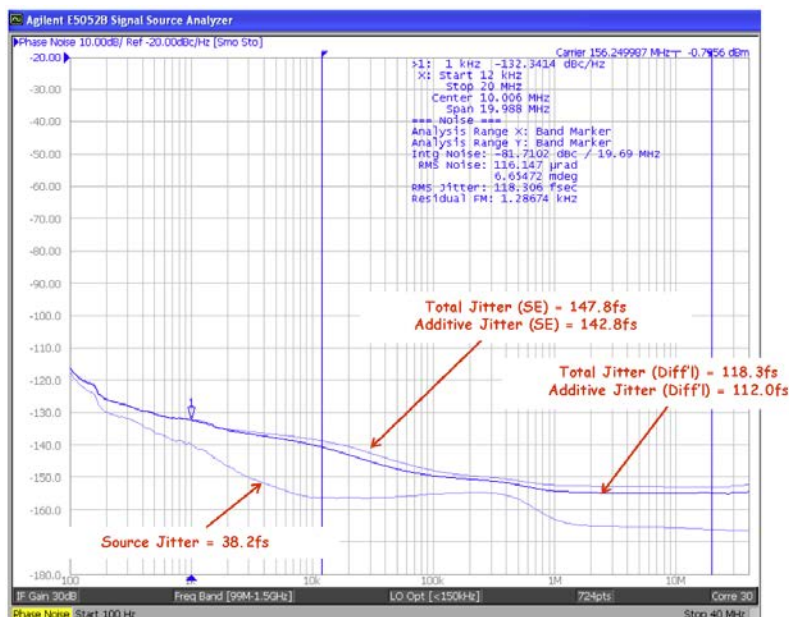
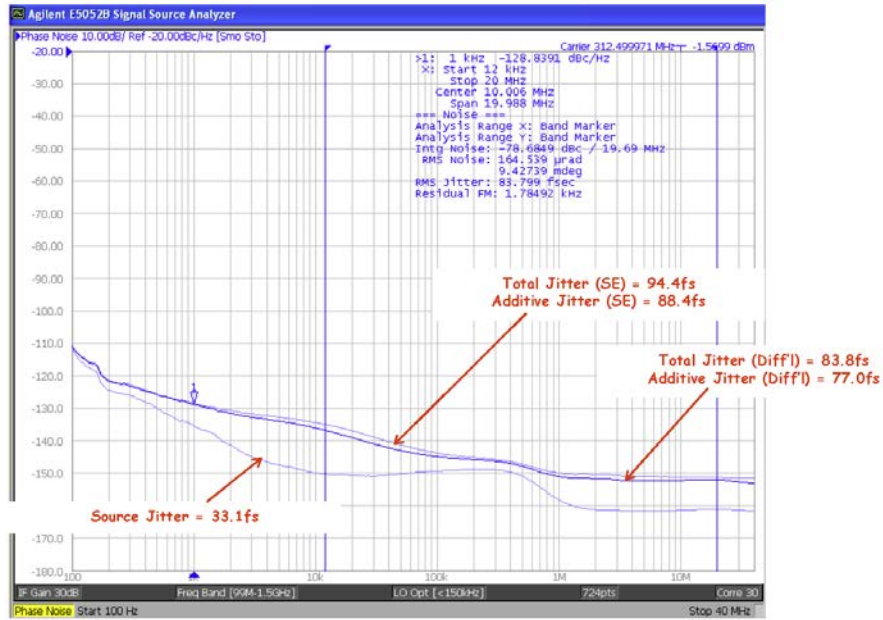


Figure 2.13. Differential Measurement Method Using a Balun



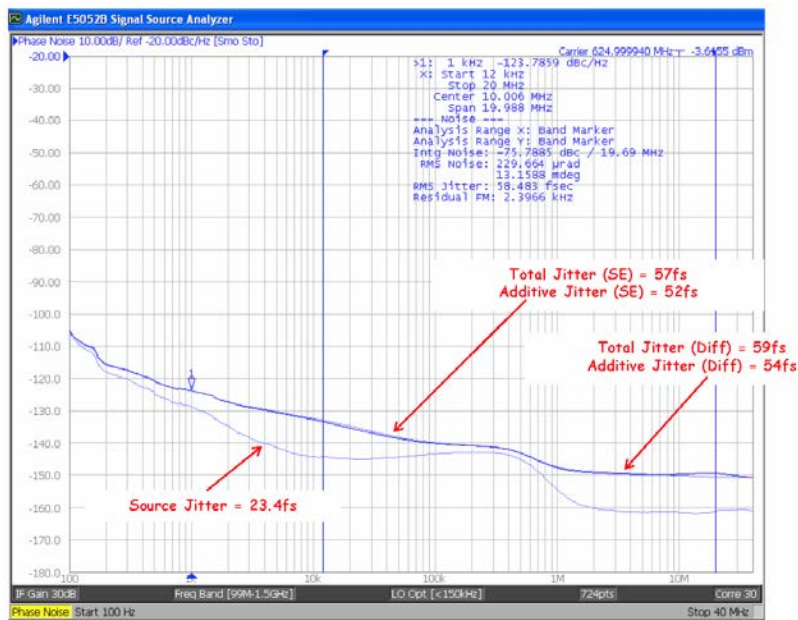
| Frequency (MHz) | Differential Input Slew Rate (V/ns) | Source Jitter (fs) | Total Jitter (SE) (fs) | Additive Jitter (SE) (fs) | Total Jitter (Differential) (fs) | Additive Jitter (Differential) (fs) |
|-----------------|-------------------------------------|--------------------|------------------------|---------------------------|----------------------------------|-------------------------------------|
| 156.25 | 1.0 | 38.2 | 147.8 | 142.8 | 118.3 | 112.0 |

Figure 2.14. Total Jitter Differential Input (156.25 MHz)



| Frequency (MHz) | Differential Input Slew Rate (V/ns) | Source Jitter (fs) | Total Jitter (SE) (fs) | Additive Jitter (SE) (fs) | Total Jitter (Differential) (fs) | Additive Jitter (Differential) (fs) |
|-----------------|-------------------------------------|--------------------|------------------------|---------------------------|----------------------------------|-------------------------------------|
| 312.5 | 1.0 | 33.10 | 94.39 | 88.39 | 83.80 | 76.99 |

Figure 2.15. Total Jitter Differential Input (312.5 MHz)



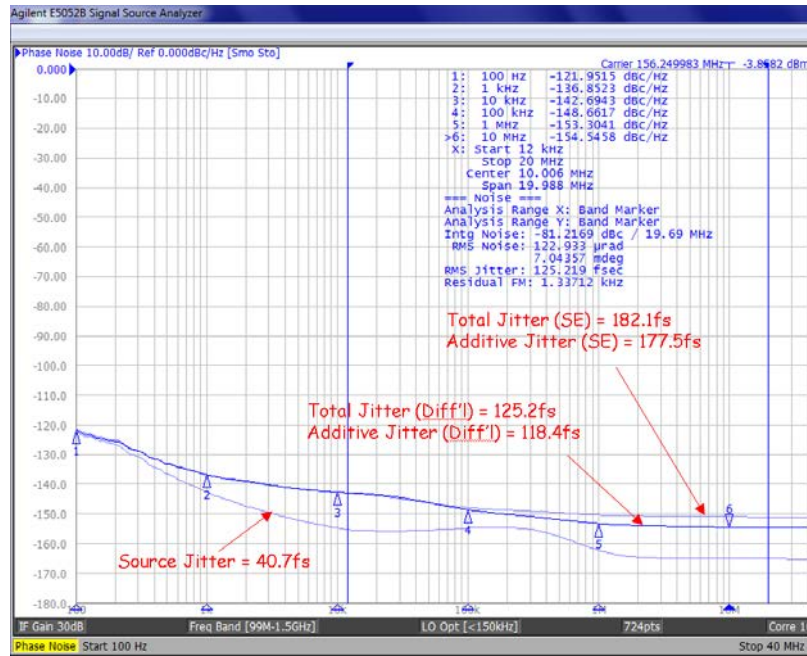
| Frequency (MHz) | Differential Input Slew Rate (V/ns) | Source Jitter (fs) | Total Jitter (SE) (fs) | Additive Jitter (SE) (fs) | Total Jitter (Differential) (fs) | Additive Jitter (Differential) (fs) |
|-----------------|-------------------------------------|--------------------|------------------------|---------------------------|----------------------------------|-------------------------------------|
| 625 | 1.0 | 23 | 57 | 52 | 59 | 54 |

Figure 2.16. Total Jitter Differential Input (625 MHz)

2.15 Typical Phase Noise Performance (Single-Ended Input Clock)

For single-ended phase noise measurements, the phase noise analyzer was connected directly without the use of a balun.

The following figure shows three phase noise plots superimposed on the same diagram.



| Frequency (MHz) | Single-Ended Input Slew Rate (V/ns) | Source Jitter (fs) | Total Jitter (SE) (fs) | Additive Jitter (SE) (fs) | Total Jitter (Differential) (fs) | Additive Jitter (Differential) (fs) |
|-----------------|-------------------------------------|--------------------|------------------------|---------------------------|----------------------------------|-------------------------------------|
| 156.25 | 1.0 | 40.74 | 182.12 | 177.51 | 125.22 | 118.41 |

Figure 2.17. Total Jitter Single-Ended Input (156.25 MHz)

2.16 Input Mux Noise Isolation

The input clock mux is designed to minimize crosstalk between CLK0 and CLK1. This improves phase jitter performance when clocks are present at both the CLK0 and CLK1 inputs. The following figure shows a measurement of the input mux's noise isolation.

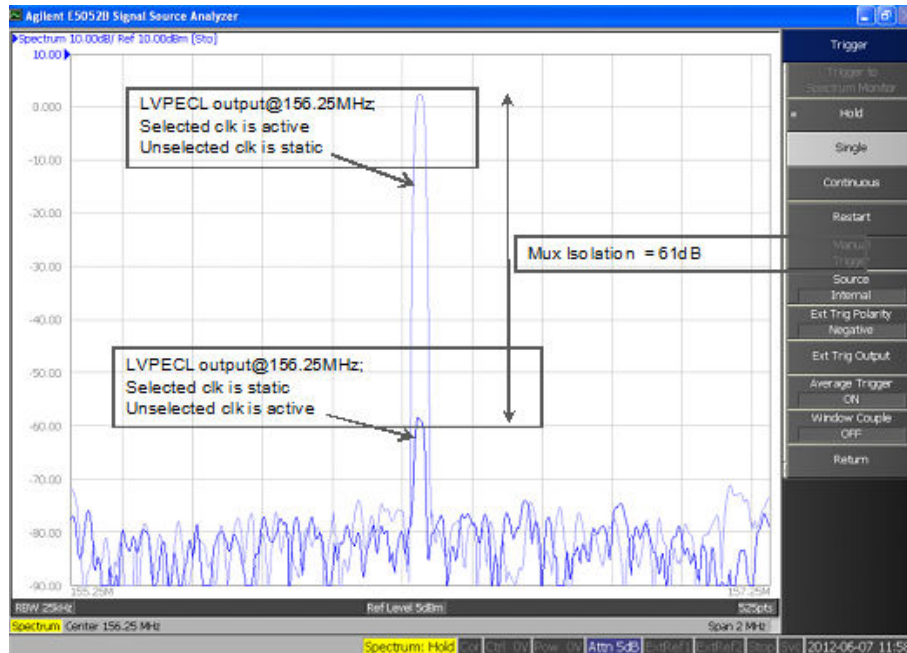


Figure 2.18. Input Mux Noise Isolation (Differential Input Clock, 44-QFN Package)

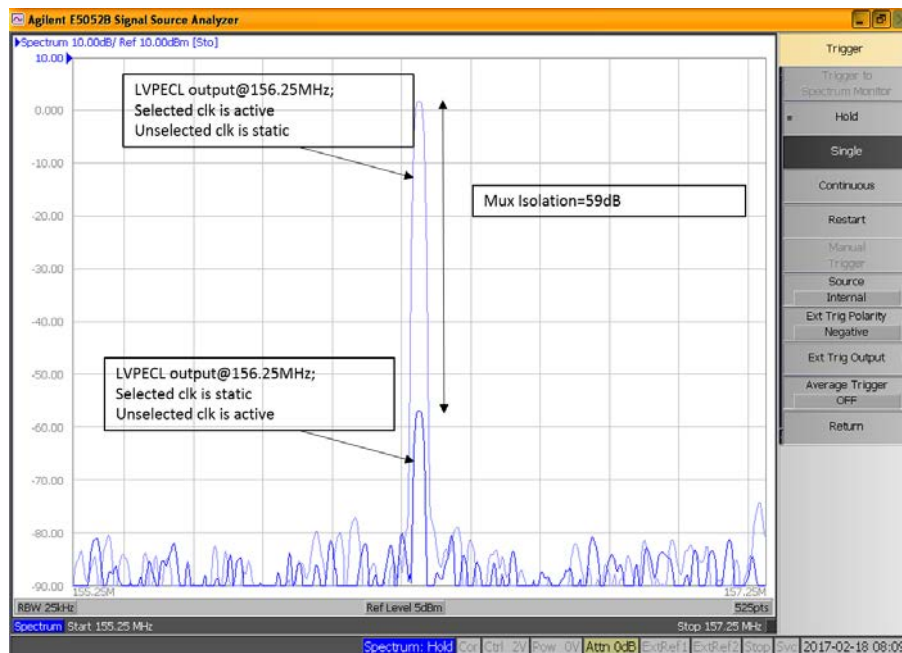


Figure 2.19. Input Mux Noise Isolation (Single-Ended Input Clock, 44-QFN Package)

2.17 Power Supply Noise Rejection

The device supports on-chip supply voltage regulation to reject power supply noise and simplify low-jitter operation in real-world environments. This feature enables robust operation alongside FPGAs, ASICs and SoCs and may reduce board-level filtering requirements. See [AN491: Power Supply Rejection for Low-Jitter Clocks](#) for more information.

3. Electrical Specifications

Table 3.1. Recommended Operating Conditions

| Parameter | Symbol | Test Condition | Min | Typ | Max | Unit |
|-----------------------------------|----------|-----------------------------------|------|-----|------|------|
| Ambient Operating Temperature | T_A | | -40 | — | 85 | °C |
| Supply Voltage Range ¹ | V_{DD} | LVDS, CML | 1.71 | 1.8 | 1.89 | V |
| | | | 2.38 | 2.5 | 2.63 | V |
| | | | 2.97 | 3.3 | 3.63 | V |
| | | LVPECL, low power LVPECL, LVC MOS | 2.38 | 2.5 | 2.63 | V |
| | | | 2.97 | 3.3 | 3.63 | V |
| | | | 2.97 | 3.3 | 3.63 | V |

| Parameter | Symbol | Test Condition | Min | Typ | Max | Unit |
|---|------------|-----------------------------------|------|-----|------|------|
| Output Buffer Supply Voltage ¹ | V_{DDOX} | LVDS, CML, LVC MOS | 1.71 | 1.8 | 1.89 | V |
| | | | 2.38 | 2.5 | 2.63 | V |
| | | | 2.97 | 3.3 | 3.63 | V |
| | | LVPECL, low power LVPECL, LVC MOS | 2.38 | 2.5 | 2.63 | V |
| | | | 2.97 | 3.3 | 3.63 | V |
| | | | 2.97 | 3.3 | 3.63 | V |

Note:

1. Core supply V_{DD} and output buffer supplies V_{DDOX} are independent. LVC MOS clock input is not supported for $V_{DD} = 1.8$ V but is supported for LVC MOS clock output for $V_{DDOX} = 1.8$ V. LVC MOS outputs at 1.5 V and 1.2 V can be supported via a simple resistor divider network.
2. See [2.12 LVC MOS Output Termination to Support 1.5 V and 1.2 V](#).

Table 3.2. Input Clock Specifications

($V_{DD} = 1.8$ V \pm 5%, 2.5 V \pm 5%, or 3.3 V \pm 10%, $T_A = -40$ to 85 °C)

| Parameter | Symbol | Test Condition | Min | Typ | Max | Unit |
|---|----------|--|---------------------|-----|---------------------|------|
| Differential Input Common Mode Voltage | V_{CM} | $V_{DD} = 2.5$ V \pm 5%, 3.3 V \pm 10% | 0.05 | — | — | V |
| Differential Input Swing (peak-to-peak) | V_{IN} | | 0.2 | — | 2.2 | V |
| LVC MOS Input High Voltage | V_{IH} | $V_{DD} = 2.5$ V \pm 5%, 3.3 V \pm 10% | $V_{DD} \times 0.7$ | — | — | V |
| LVC MOS Input Low Voltage | V_{IL} | $V_{DD} = 2.5$ V \pm 5%, 3.3 V \pm 10% | — | — | $V_{DD} \times 0.3$ | V |
| Input Capacitance | C_{IN} | CLK0 and CLK1 pins with respect to GND | — | 5 | — | pF |

Table 3.3. DC Common Characteristics

 $(V_{DD} = 1.8 V \pm 5\%, 2.5 V \pm 5\%, \text{ or } 3.3 V \pm 10\%, T_A = -40 \text{ to } 85 \text{ } ^\circ\text{C})$

| Parameter | Symbol | Test Condition | Min | Typ | Max | Unit |
|---|------------|---|----------------------|---------------------|----------------------|------------|
| Supply Current | I_{DD} | | — | 65 | 100 | mA |
| Output Buffer Supply Current (Per Clock Output) @ 100 MHz (differential) @ 200MHz (CMOS) | I_{DDOX} | LVPECL (3.3 V) Si53301/2/3/4/5/6/8 | — | 35 | — | mA |
| | | LVPECL (3.3 V) Si53307 | — | 40 | — | mA |
| | | Low Power LVPECL (3.3 V) Si53301/2/4/5/6/7/8 | — | 35 | — | mA |
| | | Low Power LVPECL (3.3 V) Si53303 | — | 30 | — | mA |
| | | LVDS (3.3 V) | — | 20 | — | mA |
| | | CML (3.3V), Si53301/4/8 | — | 35 | — | mA |
| | | CML (3.3V), Si53302/3/5 | — | 30 | — | mA |
| | | CML (3.3V), Si53306 | — | 40 | — | mA |
| | | CML (3.3V), Si53307 | — | 60 | — | mA |
| | | HCSL, 100 MHz, 2 pF load (3.3 V) | — | 35 | — | mA |
| | | CMOS (1.8 V, SFOUT = Open/0), per output, $C_L = 5 \text{ pF}$, 200 MHz | — | 5 | — | mA |
| | | CMOS (2.5 V, SFOUT = Open/0), per output, $C_L = 5 \text{ pF}$, 200 MHz | — | 8 | — | mA |
| | | CMOS (3.3 V, SFOUT = 0/1), per output, $C_L = 5 \text{ pF}$, 200 MHz Si53306/7 | — | 20 | — | mA |
| | | CMOS (3.3 V, SFOUT = 0/1), per output, $C_L = 5 \text{ pF}$, 200 MHz Si53301/2/3/4/5/8 | — | 15 | — | mA |
| Voltage Reference | V_{REF} | V_{REF} pin, $I_{REF} = \pm 500 \mu\text{A}$ | — | $V_{DD}/2$ | — | V |
| Input High Voltage | V_{IH} | SFOUTx, DIVx, CLK_SEL, OEx Si53303 | $0.85 \times V_{DD}$ | — | — | V |
| | | SFOUTx, DIVx, CLK_SEL, OEx Si53301/2/4/5/6/7/8 | $0.8 \times V_{DD}$ | — | — | V |
| Input Mid Voltage | V_{IM} | SFOUTx, DIVx 3-level input pins | $0.45 \times V_{DD}$ | $0.5 \times V_{DD}$ | $0.55 \times V_{DD}$ | V |
| Input Low Voltage | V_{IL} | SFOUTx, DIVx, CLK_SEL, OEx Si53301/2/4/5/6/7/8 | — | — | $0.2 \times V_{DD}$ | V |
| | | SFOUTx, DIVx, CLK_SEL, OEx Si53303 | — | — | $0.15 \times V_{DD}$ | V |
| Output Voltage High (LOSx) | V_{OH} | $I_{DD} = -1 \text{ mA}$ | $0.8 \times V_{DD}$ | — | — | V |
| Output Voltage Low (LOSx) | V_{OL} | $I_{DD} = 1 \text{ mA}$ | — | — | $0.2 \times V_{DD}$ | V |
| Internal Pull-down Resistor | R_{DOWN} | CLK_SEL, DIVx, SFOUTx, | — | 25 | — | k Ω |

| Parameter | Symbol | Test Condition | Min | Typ | Max | Unit |
|---------------------------|----------|-------------------|-----|-----|-----|------------|
| Internal Pull-up Resistor | R_{UP} | OEx, DIVx, SFOUTx | — | 25 | — | k Ω |

Table 3.4. Output Characteristics (LVPECL) $(V_{DDOX} = 2.5\text{ V} \pm 5\%$, or $3.3\text{ V} \pm 10\%$, $T_A = -40$ to $85\text{ }^\circ\text{C}$)

| Parameter | Symbol | Test Condition | Min | Typ | Max | Unit |
|-------------------------------|-----------|----------------|--------------------|------|--------------------|------|
| Output DC Common Mode Voltage | V_{COM} | | $V_{DDOX} - 1.595$ | — | $V_{DDOX} - 1.245$ | V |
| Single-Ended Output Swing | V_{SE} | | 0.55 | 0.80 | 1.050 | V |

Note:

1. Unused outputs can be left floating. Do not short unused outputs to ground.

Table 3.5. Output Characteristics (Low Power LVPECL) $(V_{DDOX} = 2.5\text{ V} \pm 5\%$, or $3.3\text{ V} \pm 10\%$, $T_A = -40$ to $85\text{ }^\circ\text{C}$)

| Parameter | Symbol | Test Condition | Min | Typ | Max | Unit |
|-------------------------------|-----------|--------------------------------------|--------------------|------|--------------------|------|
| Output DC Common Mode Voltage | V_{COM} | $R_L = 100\ \Omega$ across Qn and Qn | $V_{DDOX} - 1.895$ | | $V_{DDOX} - 1.275$ | V |
| Single-Ended Output Swing | V_{SE} | $R_L = 100\ \Omega$ across Qn and Qn | 0.25 | 0.60 | 0.85 | V |

Table 3.6. Output Characteristics (CML) $(V_{DDOX} = 1.8\text{ V} \pm 5\%$, $2.5\text{ V} \pm 5\%$, or $3.3\text{ V} \pm 10\%$, $T_A = -40$ to $85\text{ }^\circ\text{C}$)

| Parameter | Symbol | Test Condition | Min | Typ | Max | Unit |
|---------------------------|----------|---|-----|-----|-----|------|
| Single-Ended Output Swing | V_{SE} | Terminated as shown in Figure 2.9 LVDS, CML, HCSL, and Low-Power LVPECL Output Terminations on page 13 (CML termination). | 300 | 400 | 550 | mV |

Table 3.7. Output Characteristics (LVDS) $(V_{DDOX} = 1.8\text{ V} \pm 5\%, 2.5\text{ V} \pm 5\%, \text{ or } 3.3\text{ V} \pm 10\%, T_A = -40 \text{ to } 85\text{ }^\circ\text{C})$

| Parameter | Symbol | Test Condition | Min | Typ | Max | Unit |
|---|------------|--|------|------|------|------|
| Single-Ended Output Swing | V_{SE} | $R_L = 100\ \Omega$ across Q_N and Q_N Si53301/2/4/5/6/7/8 | 247 | — | 490 | mV |
| | | $R_L = 100\ \Omega$ across Q_N and Q_N Si53303 | 247 | — | 454 | mV |
| Output Common Mode Voltage ($V_{DDO} = 2.5\text{ V}$ or 3.3V) | V_{COM1} | $V_{DDOX} = 2.38$ to 2.63 V , 2.97 to 3.63 V , $R_L = 100\ \Omega$ across Q_N and Q_N | 1.10 | 1.25 | 1.35 | V |
| Output Common Mode Voltage ($V_{DDO} = 1.8\text{ V}$) | V_{COM2} | $V_{DDOX} = 1.71$ to 1.89 V , $R_L = 100\ \Omega$ across Q_N and Q_N Si53301/2/4/5/6/7/8 | 0.85 | 0.97 | 1.25 | V |
| | | $V_{DDOX} = 1.71$ to 1.89 V , $R_L = 100\ \Omega$ across Q_N and Q_N Si53303 | 0.85 | 0.97 | 1.1 | V |

Table 3.8. Output Characteristics (LVCMOS) $(V_{DDOX} = 1.8\text{ V} \pm 5\%, 2.5\text{ V} \pm 5\%, \text{ or } 3.3\text{ V} \pm 10\%, T_A = -40 \text{ to } 85\text{ }^\circ\text{C})$

| Parameter | Symbol | Test Condition | Min | Typ | Max | Unit |
|---------------------|----------|---------------------|------------------------|-----|------------------------|------|
| Output Voltage High | V_{OH} | Si53301/2/4/5/6/7/8 | $0.75 \times V_{DDOX}$ | — | — | V |
| | | Si53303 | $0.8 \times V_{DDOX}$ | — | — | V |
| Output Voltage Low | V_{OL} | Si53301/2/4/5/6/7/8 | — | — | $0.25 \times V_{DDOX}$ | V |
| | | Si53303 | — | — | $0.2 \times V_{DDOX}$ | V |

Note:

- I_{OH} and I_{OL} per the Output Signal Format Table for specific V_{DDOX} and SFOUTx settings.

Table 3.9. Output Characteristics (HCSL) $(V_{DDOX} = 2.5\text{ V} \pm 5\% \text{ or } 3.3\text{ V} \pm 10\%, T_A = -40 \text{ to } 85\text{ }^\circ\text{C})$

| Parameter | Symbol | Test Condition | Min | Typ | Max | Unit |
|---------------------------|----------|--|------|-----|-----|------|
| Output Voltage High | V_{OH} | $R_L = 50\ \Omega$ to GND Si53301/2/3/4/5/6/8 | 550 | 700 | 900 | mV |
| | | $R_L = 50\ \Omega$ to GND Si53307 | 550 | 700 | 850 | mV |
| Output Voltage Low | V_{OL} | $R_L = 50\ \Omega$ to GND | -150 | 0 | 150 | mV |
| Single-Ended Output Swing | V_{SE} | $R_L = 50\ \Omega$ to GND | 550 | 700 | 850 | mV |
| Crossing Voltage | V_C | $R_L = 50\ \Omega$ to GND | 250 | 350 | 550 | mV |

Table 3.10. AC Characteristics

 $(V_{DD} = V_{DDOX} = 1.8\text{ V} \pm 5\%, 2.5\text{ V} \pm 5\%, \text{ or } 3.3\text{ V} \pm 10\%, T_A = -40\text{ to } 85\text{ }^\circ\text{C})$

| Parameter | Symbol | Test Condition | Min | Typ | Max | Unit |
|--|--------------------|---|------|----------------|------|---------------|
| LOSx Clear Time | T_{LOSCLR} | F < 100 MHz | — | $T_{PER} + 15$ | — | ns |
| | | F > 100 MHz | — | 25 | — | ns |
| LOSx Activation Time | T_{LOSACT} | | — | 15 | — | μs |
| Frequency | F | LVPECL, low power LVPECL, LVDS, CML, HCSL ¹ | 1 | — | 725 | MHz |
| | | LVC MOS | 1 | — | 200 | MHz |
| Duty Cycle ⁶ | D_C | 200 MHz, 20/80% $T_R/T_F < 10\%$ of period (LVC MOS) (12 mA drive) | 40 | 50 | 60 | % |
| | | 80% $T_R/T_F < 10\%$ of period (Differential) | 48 | 50 | 52 | % |
| Minimum Input Clock Slew Rate ⁵ | SR | Required to meet prop delay and additive jitter specifications (20–80%) | 0.75 | — | — | V/ns |
| Output Rise/Fall Time | T_R/T_F | LVDS, 20/80% | — | — | 325 | ps |
| | | LVPECL, 20/80% | — | — | 350 | ps |
| | | HCSL ¹ , 20/80% | — | — | 280 | ps |
| | | CML, 20/80% | — | — | 350 | ps |
| | | Low-Power LVPECL, 20/80% | — | — | 350 | ps |
| | | LVC MOS 200 MHz, 20/80%, 2 pF load | — | — | 750 | ps |
| Minimum Input Pulse Width | T_W | | 500 | — | — | ps |
| Propagation Delay | T_{PLH}, T_{PHL} | LVC MOS (12 mA drive with no load) | 1250 | 2000 | 2750 | ps |
| | | LVPECL Si53301/2/3/4/5/8 | 600 | 800 | 1000 | ps |
| | | LVPECL Si53306/7 | 675 | 875 | 1075 | ps |
| | | LVDS Si53301/2/3/4/5/8 | 600 | 800 | 1000 | ps |
| | | LVDS Si53306/7 | 675 | 875 | 1075 | ps |
| Output Enable Time Si53301/2/4/5/8 | T_{EN} | F = 1 MHz | — | 2500 | — | ns |
| | | F = 100 MHz | — | 30 | — | ns |
| | | F = 725 MHz | — | 5 | — | ns |
| Output Enable Time Si53303 | T_{EN} | F = 1 MHz | — | 2000 | — | ns |
| | | F = 100 MHz | — | 60 | — | ns |
| | | F = 725 MHz | — | 50 | — | ns |

| Parameter | Symbol | Test Condition | Min | Typ | Max | Unit |
|--|-----------|--|-----|------|-----|------|
| Output Enable Time Si53306/7 | T_{EN} | F = 1 MHz | — | 1570 | — | ns |
| | | F = 100 MHz | — | 20 | — | ns |
| | | F = 725 MHz | — | 5 | — | ns |
| Output Disable Time Si53301/2/4/5/8 | T_{DIS} | F = 1 MHz | — | 2000 | — | ns |
| | | F = 100 MHz | — | 30 | — | ns |
| | | F = 725 MHz | — | 5 | — | ns |
| Output Disable Time Si53303 | T_{DIS} | F = 1 MHz | — | 2000 | — | ns |
| | | F = 100 MHz | — | 25 | — | ns |
| | | F = 725 MHz | — | 15 | — | ns |
| Output Disable Time Si53306/7 | T_{DIS} | F = 1 MHz | — | 2000 | — | ns |
| | | F = 100 MHz | — | 35 | — | ns |
| | | F = 725 MHz | — | 5 | — | ns |
| Output to Output Skew ² | T_{SK} | LVC MOS (12 mA drive to no load) ⁷ | — | 50 | 120 | ps |
| | | LVPECL | — | 35 | 75 | ps |
| | | LVDS | — | 35 | 85 | ps |
| Part to Part Skew ³ | T_{PS} | Differential | — | — | 150 | ps |
| Power Supply Noise Rejection ⁴ (Si53305/2) | PSNR | 10 kHz sinusoidal noise | — | -63 | — | dBc |
| | | 100 kHz sinusoidal noise | — | -62 | — | dBc |
| | | 500 kHz sinusoidal noise | — | -58 | — | dBc |
| | | 10 MHz sinusoidal noise | — | -55 | — | dBc |
| Power Supply Noise Rejection ⁴ (Si53308/4/1) | PSNR | 10 kHz sinusoidal noise | — | -65 | — | dBc |
| | | 100 kHz sinusoidal noise | — | -63 | — | dBc |
| | | 500 kHz sinusoidal noise | — | -60 | — | dBc |
| | | 10 MHz sinusoidal noise | — | -55 | — | dBc |
| Power Supply Noise Rejection ⁴ (Si53307/6) | PSNR | 10 kHz sinusoidal noise | — | -72 | — | dBc |
| | | 100 kHz sinusoidal noise | — | -70 | — | dBc |
| | | 500 kHz sinusoidal noise | — | -67 | — | dBc |
| | | 10 MHz sinusoidal noise | — | -62 | — | dBc |
| Power Supply Noise Rejection ⁴ (Si53303) | PSNR | 10 kHz sinusoidal noise | — | -90 | — | dBc |
| | | 100 kHz sinusoidal noise | — | -90 | — | dBc |
| | | 500 kHz sinusoidal noise | — | -80 | — | dBc |
| | | 10 MHz sinusoidal noise | — | -70 | — | dBc |

| Parameter | Symbol | Test Condition | Min | Typ | Max | Unit |
|--|--------|----------------|-----|-----|-----|------|
| Notes: | | | | | | |
| 1. HCSL measurements were made with receiver termination and applies for 2.5 V and 3.3 V only. See Figure 2.9 LVDS, CML, HCSL, and Low-Power LVPECL Output Terminations on page 13 . | | | | | | |
| 2. Output to Output skew specified for outputs with an identical configuration. | | | | | | |
| 3. Defined as skew between any output on different devices operating at the same supply voltage, temperature, and equal load condition. Using the same type of inputs on each device, the outputs are measured at the differential cross points. | | | | | | |
| 4. Measured for 156.25 MHz carrier frequency. Sine-wave noise added to V_{DDOX} (3.3 V = 100 mV _{PP}) and noise spur amplitude measured. See "AN491: Power Supply Rejection for Low-Jitter Clocks" for further details. | | | | | | |
| 5. TBD | | | | | | |
| 6. 50% input duty cycle. | | | | | | |
| 7. LVCMOS outputs are in phase. | | | | | | |

Table 3.11. Additive Jitter, Differential Clock Input

| V_{DD} | Input ^{1,2} | Output | Additive Jitter (fs rms, 12 kHz to 20 MHz) ³ | | | | |
|----------|----------------------|--------------|--|---|--------------|-----|-----|
| | Freq (MHz) | Clock Format | Amplitude V_{IN} (Single-Ended, Peak-to-Peak) | Differential 20%-80% Slew Rate (V/ns) | Clock Format | Typ | Max |
| 3.3 | 725 | Differential | 0.15 | 0.637 | LVPECL | 45 | 65 |
| 3.3 | 725 | Differential | 0.15 | 0.637 | LVDS | 50 | 65 |
| 3.3 | 156.25 | Differential | 0.5 | 0.458 | LVPECL | 160 | 185 |
| 3.3 | 156.25 | Differential | 0.5 | 0.458 | LVDS | 150 | 200 |
| 2.5 | 725 | Differential | 0.15 | 0.637 | LVPECL | 45 | 65 |
| 2.5 | 725 | Differential | 0.15 | 0.637 | LVDS | 50 | 65 |
| 2.5 | 156.25 | Differential | 0.5 | 0.458 | LVPECL | 145 | 185 |
| 2.5 | 156.25 | Differential | 0.5 | 0.458 | LVDS | 145 | 195 |

Notes:

- For best additive jitter results, use the fastest slew rate possible. See "AN766: Understanding and Optimizing Clock Buffer's Additive Jitter Performance" for more information.
- AC-coupled differential inputs.
- Measured differentially using a balun at the phase noise analyzer input. See [Figure 2.13 Differential Measurement Method Using a Balun on page 15](#).

Table 3.12. Additive Jitter, Single-Ended Clock Input

| V _{DD} | Input ^{1,2} | Output | Additive Jitter (fs rms, 12 kHz to 20 MHz) ³ | | | | |
|-----------------|----------------------|--------------|---|--------------------------------|----------------------|-----|-----|
| | Freq (MHz) | Clock Format | Amplitude V _{IN} (single-ended, peak to peak) | SE 20%-80% Slew Rate (V/ns) | Clock Format | Typ | Max |
| 3.3 | 200 | Single-ended | 1.70 | 1 | LVC MOS ⁴ | 120 | 160 |
| 3.3 | 156.25 | Single-ended | 2.18 | 1 | LVPECL | 160 | 185 |
| 3.3 | 156.25 | Single-ended | 2.18 | 1 | LVDS | 150 | 200 |
| 3.3 | 156.25 | Single-ended | 2.18 | 1 | LVC MOS ⁴ | 130 | 180 |
| 2.5 | 200 | Single-ended | 1.70 | 1 | LVC MOS ⁵ | 120 | 160 |
| 2.5 | 156.25 | Single-ended | 2.18 | 1 | LVPECL | 145 | 185 |
| 2.5 | 156.25 | Single-ended | 2.18 | 1 | LVDS | 145 | 195 |
| 2.5 | 156.25 | Single-ended | 2.18 | 1 | LVC MOS ⁵ | 140 | 180 |

Notes:

1. For best additive jitter results, use the fastest slew rate possible. See "AN766: Understanding and Optimizing Clock Buffer's Additive Jitter Performance" for more information.
2. DC-coupled single-ended inputs.
3. Measured single-ended at the phase noise analyzer input. See [Figure 2.17 Total Jitter Single-Ended Input \(156.25 MHz\) on page 17](#).
4. Drive Strength: 12 mA, 3.3 V (SFOUT = 11). LVC MOS jitter is measured single-ended.
5. Drive Strength: 9 mA, 2.5 V (SFOUT = 11). LVC MOS jitter is measured single-ended.

Table 3.13. Thermal Conditions

| Package | Parameter | Symbol | Test Condition | Value | Unit |
|---------------------------|---|---------------|----------------|-------|------|
| 3 x 3 mm QFN ¹ | Thermal Resistance, Junction to Ambient | θ_{JA} | Still air | 60 | °C/W |
| | Thermal Resistance, Junction to Case | θ_{JC} | Still air | 10.8 | °C/W |
| | Thermal Resistance, Junction to Board | θ_{JB} | Still air | 34.1 | °C/W |
| 5 x 5 mm QFN ² | Thermal Resistance, Junction to Ambient | θ_{JA} | Still air | 50.3 | °C/W |
| | Thermal Resistance, Junction to Case | θ_{JC} | Still air | 10.3 | °C/W |
| | Thermal Resistance, Junction to Board | θ_{JB} | Still air | 30.9 | °C/W |
| 7 x 7 mm QFN ³ | Thermal Resistance, Junction to Ambient | θ_{JA} | Still air | 46.2 | °C/W |
| | Thermal Resistance, Junction to Case | θ_{JC} | Still air | 27.1 | °C/W |
| | Thermal Resistance, Junction to Board | θ_{JB} | Still air | 28 | °C/W |

Note:

1. Based on a 2-layer, PCB with Dimension 3"x4.5". PCB Thickness of 1.6mm. PCB Center Land with 4 Via to backside, 75% Cu coverage.
2. Based on PCB with dimension 3" x 4.5", PCB Thickness of 1.6 mm. PCB Center Land with 4 Via to top plane.
3. Based on 2-layer PCB with dimension 3" x 4.5", PCB Thickness of 1.6 mm. PCB Center Land with 16 Via to back side with 75% Cu coverage.

Table 3.14. Absolute Maximum Ratings

| Parameter | Symbol | Test Condition | Min | Typ | Max | Unit |
|-----------------------------------|------------|--|------|-----|----------------|------|
| Storage Temperature | T_S | | -55 | — | 150 | °C |
| Supply Voltage | V_{DD} | | -0.5 | — | 3.8 | V |
| Input Voltage | V_{IN} | | -0.5 | — | $V_{DD} + 0.3$ | V |
| Output Voltage | V_{OUT} | | — | — | $V_{DD} + 0.3$ | V |
| ESD Sensitivity | HBM | HBM, 100 pF, 1.5 k Ω | — | — | 2000 | V |
| ESD Sensitivity | CDM | | — | — | 500 | V |
| Peak Soldering Reflow Temperature | T_{PEAK} | Pb-Free; Solder reflow profile per JEDEC J-STD-020 | — | — | 260 | °C |
| Maximum Junction Temperature | T_J | | — | — | 125 | °C |

Note:

1. Stresses beyond those listed in this table may cause permanent damage to the device. Functional operation specification compliance is not implied at these conditions. Exposure to maximum rating conditions for extended periods may affect device reliability.

4. Detailed Block Diagrams

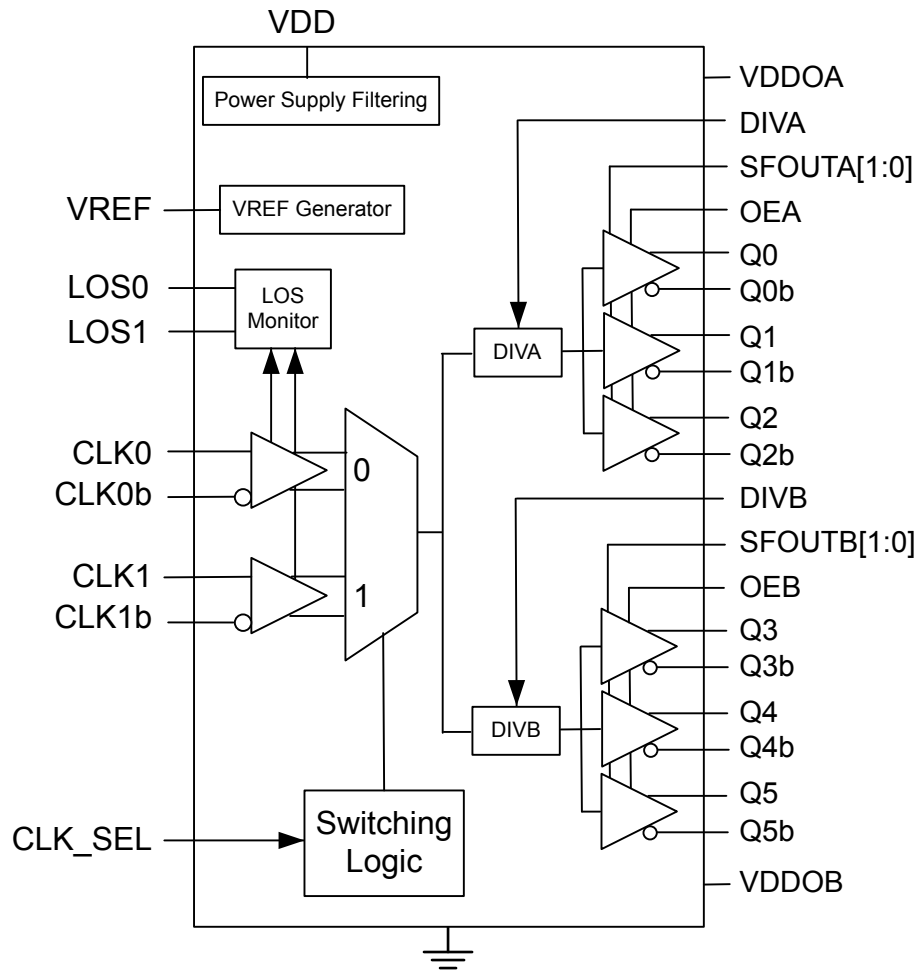


Figure 4.1. Si53301 Block Diagram

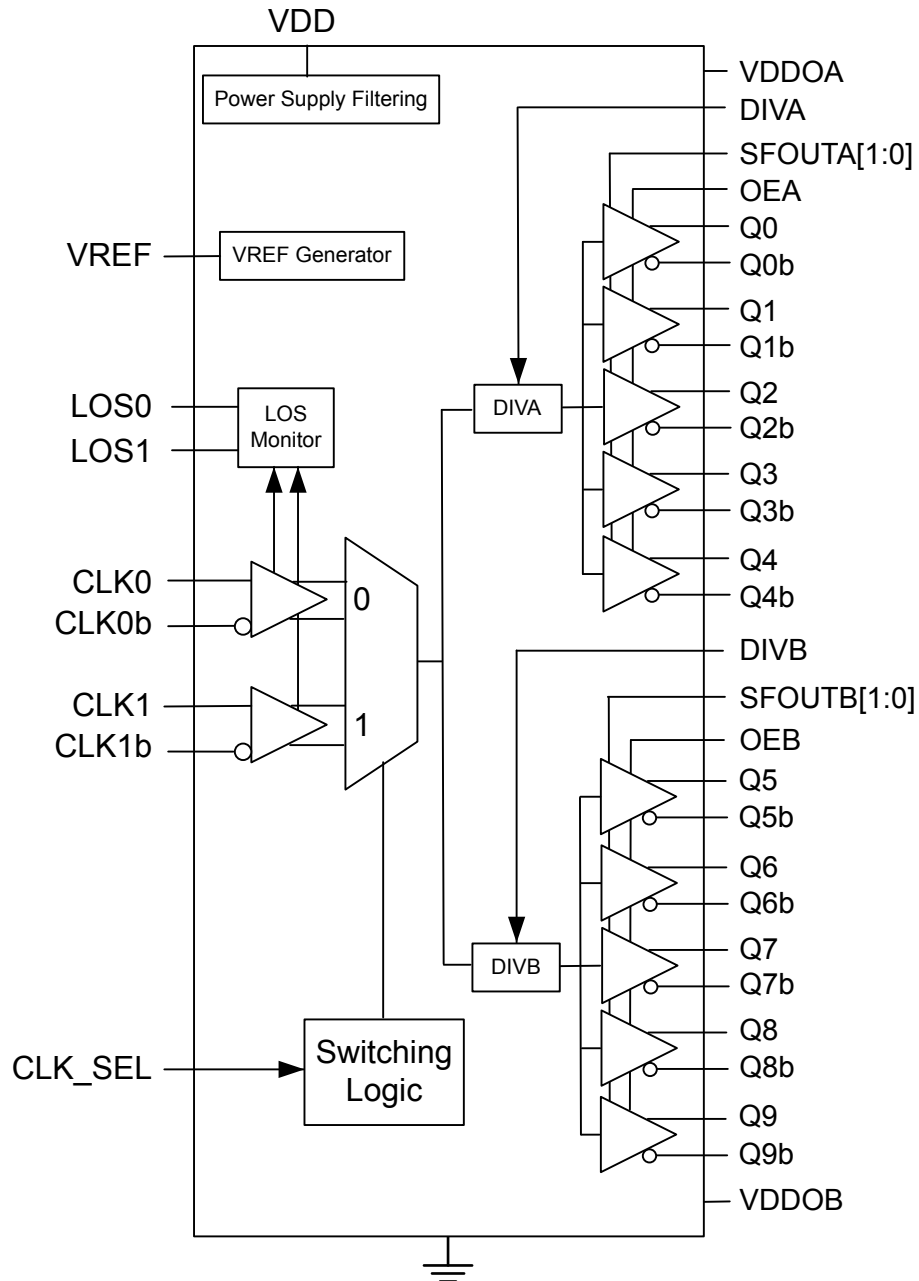


Figure 4.2. Si53302 Block Diagram

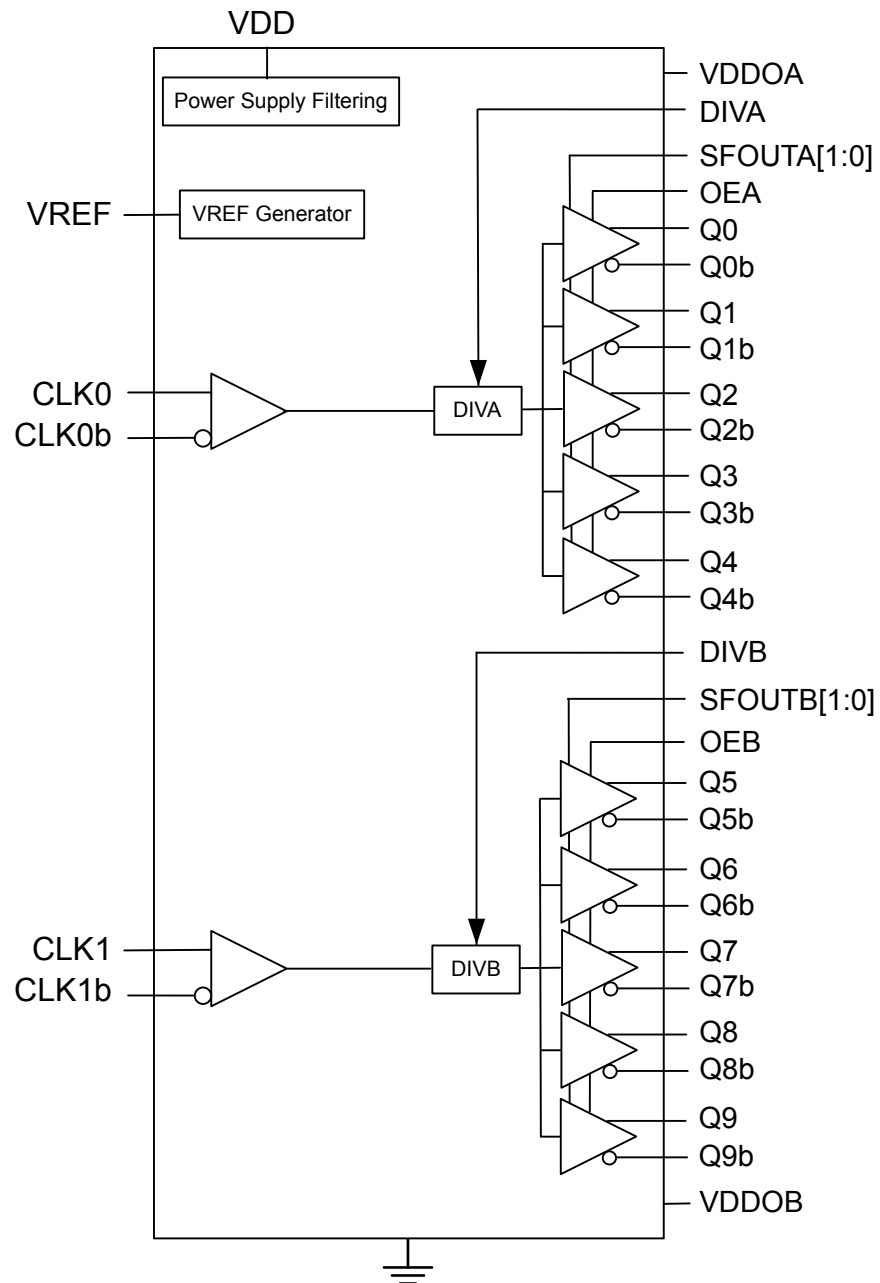


Figure 4.3. Si53303 Block Diagram

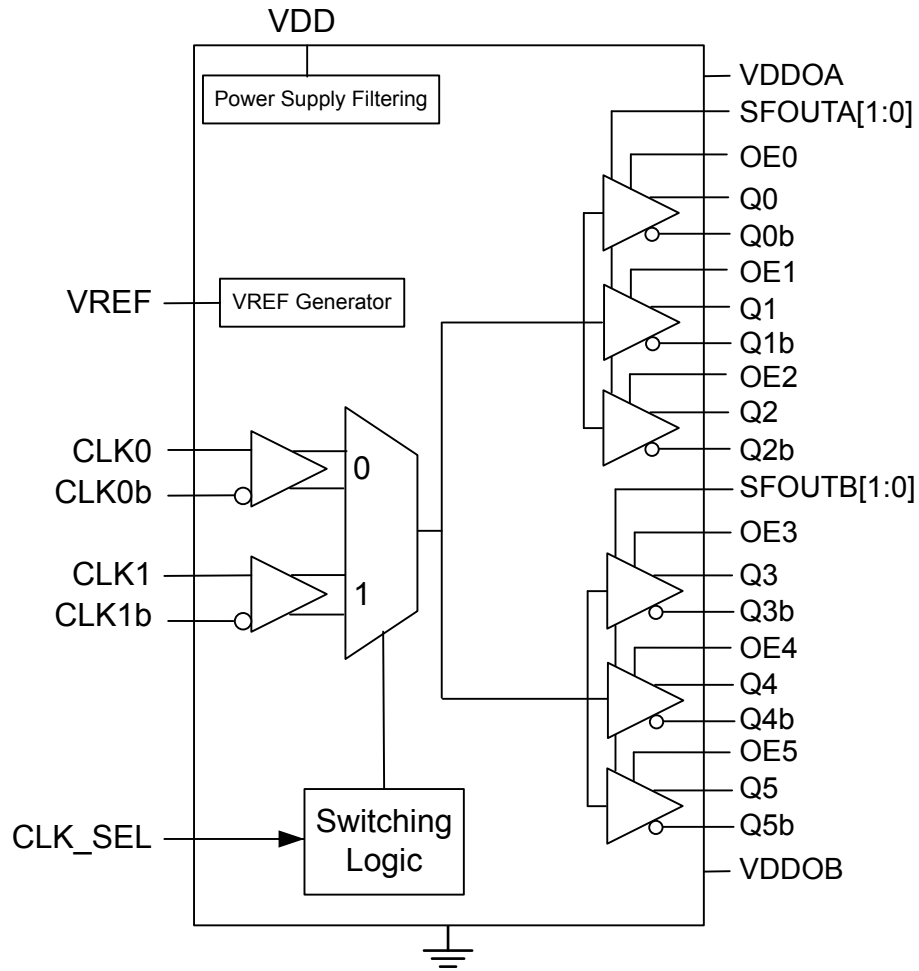


Figure 4.4. Si53304 Block Diagram

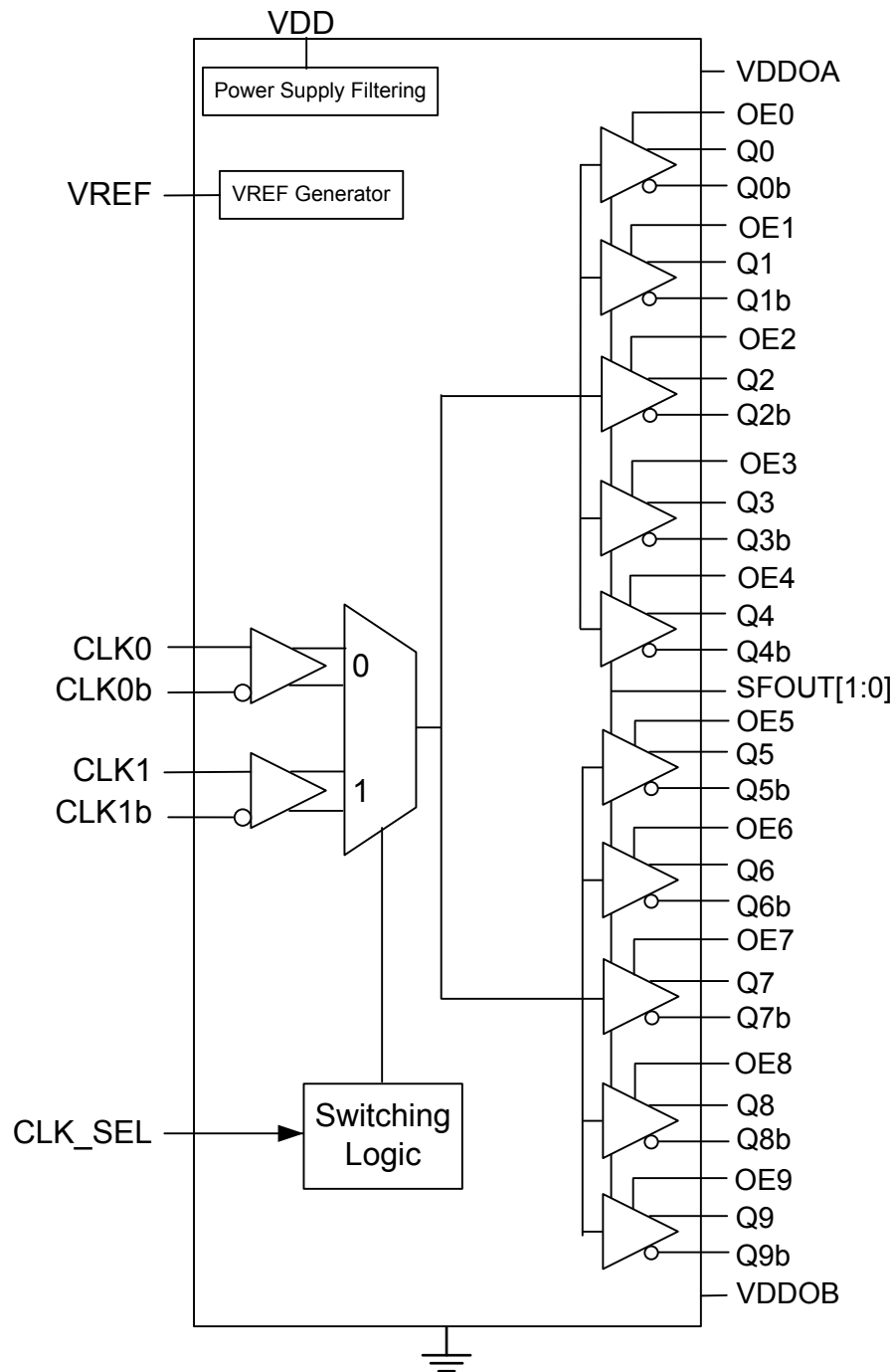


Figure 4.5. Si53305 Block Diagram

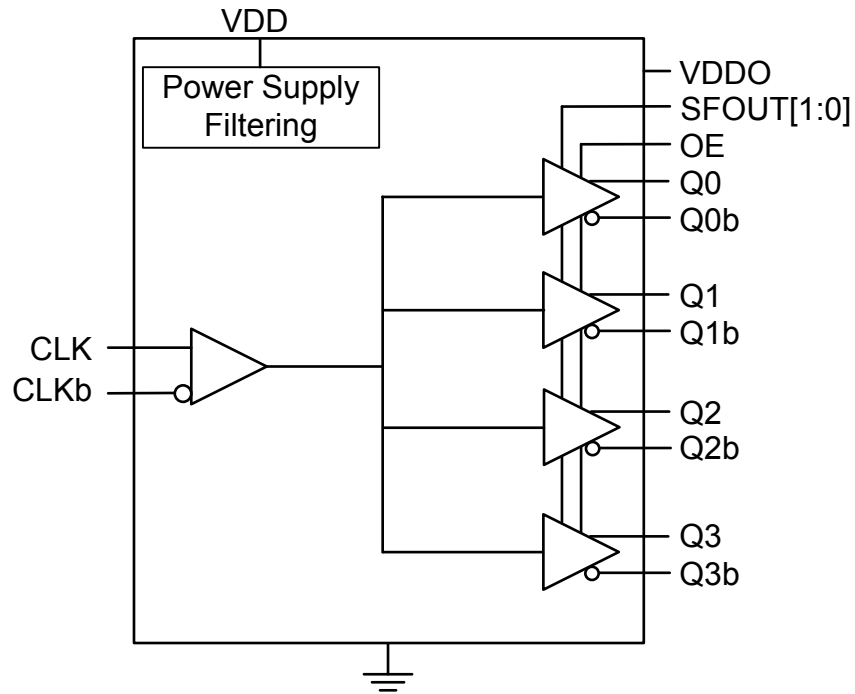


Figure 4.6. Si53306 Block Diagram

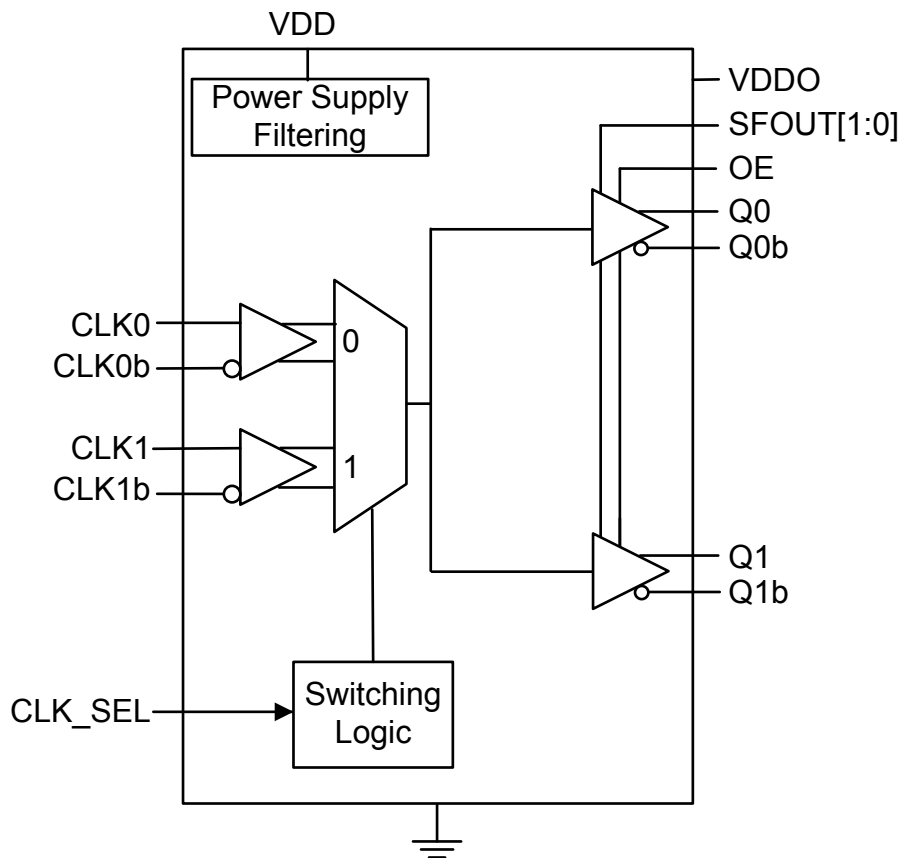


Figure 4.7. Si53307 Block Diagram

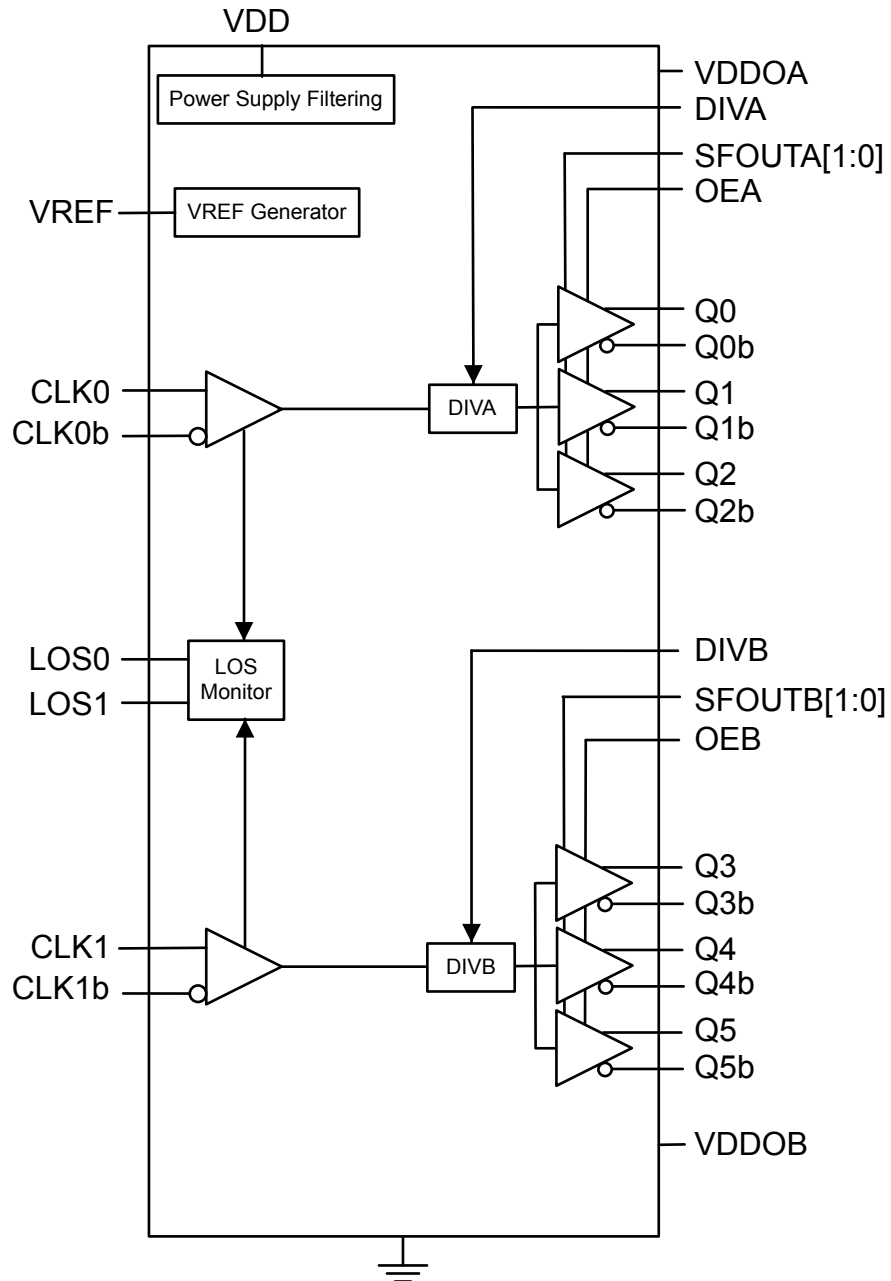


Figure 4.8. Si53308 Block Diagram

5. Pin Descriptions

5.1 Si53301 Pin Descriptions

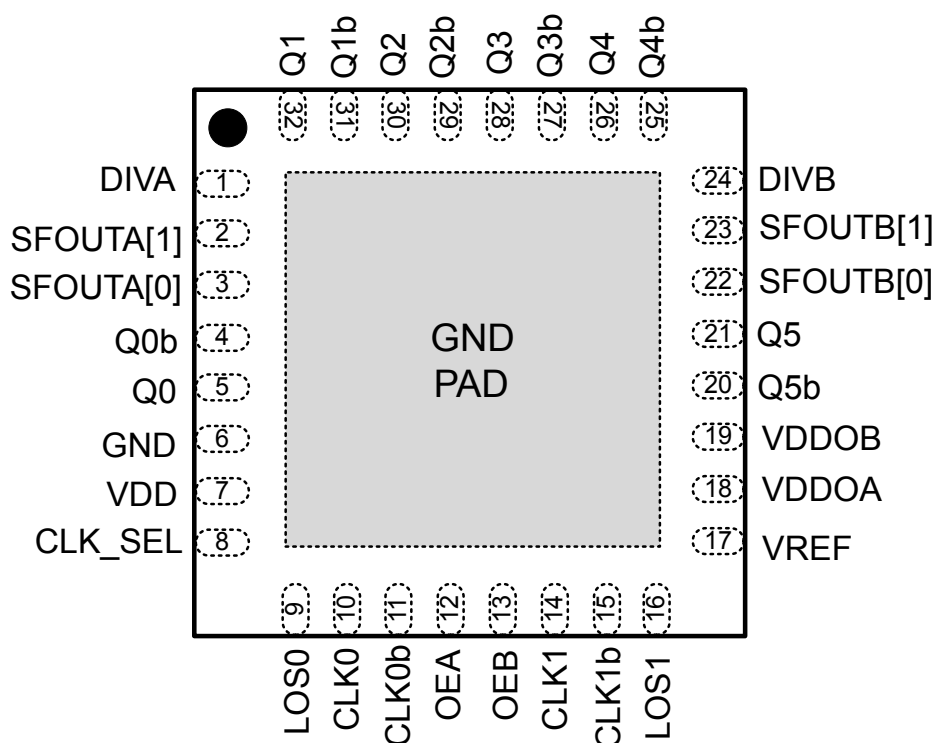


Table 5.1. Si53301 -QFN Pin Descriptions

| Pin | Name | Type ¹ | Description |
|-----|-----------|-------------------|--|
| 1 | DIVA | I | Output divider control pin for Bank A Three-level input control. Internally biased at $V_{DD}/2$. Can be left floating or tied to ground or V_{DD} . |
| 2 | SFOUTA[1] | I | Output signal format control pin for Bank A Three-level input control. Internally biased at $V_{DD}/2$. Can be left floating or tied to ground or V_{DD} . |
| 3 | SFOUTA[0] | I | Output signal format control pin for Bank A Three-level input control. Internally biased at $V_{DD}/2$. Can be left floating or tied to ground or V_{DD} . |
| 4 | Q0b | O | Output clock 0 (complement) |
| 5 | Q0 | O | Output clock 0 |
| 6 | GND | GND | Ground |
| 7 | VDD | P | Core voltage supply. Bypass with 1.0 μF capacitor placed as close to the VDD pin as possible. |

| Pin | Name | Type ¹ | Description |
|-----|-----------|-------------------|--|
| 8 | CLK_SEL | I | Mux input select pin Clock inputs are switched without the introduction of glitches. When CLK_SEL is high, CLK1 is selected. When CLK_SEL is low, CLK0 is selected. CLK_SEL contains an internal pull-down resistor. |
| 9 | LOS0 | O | The LOS0 status pin indicates whether a clock is present at the CLK0 input. CLK0 input clock present LOS0 = 0 CLK0 input clock not present LOS0 = 1 |
| 10 | CLK0 | I | Input clock 0 |
| 11 | CLK0b | I | Input clock 0 (complement) When the CLK0 is driven by a single-end input, connect CLK0b to $V_{DD}/2$. |
| 12 | OEA | I | Output enable—Bank A (Outputs Q0 to Q2). When OE = high, the Bank A outputs are enabled. When OE = low, Q is held low, and Qb is held high for differential formats. For LVCMOS, both Q and Qb are held low when OE is set low. OEA contains an internal pull-up resistor. |
| 13 | OEB | I | Output enable—Bank B (Outputs Q3 to Q5) When OE = high, the Bank B outputs are enabled. When OE = low, Q is held low, and Qb is held high for differential formats. For LVCMOS, both Q and Qb are held low when OE is set low. OEB contains an internal pull-up resistor. |
| 14 | CLK1 | I | Input clock 1 |
| 15 | CLK1b | I | Input clock 1 (complement) When the CLK1 is driven by a single-end input, connect CLK1b to $V_{DD}/2$. |
| 16 | LOS1 | O | The LOS1 status pin indicates whether a clock is present at the CLK1 input: CLK1 input clock present LOS1 = 0 CLK1 input clock not present LOS1 = 1 |
| 17 | VREF | O | Reference voltage output. |
| 18 | VDDOA | P | Output voltage supply—Bank A (Outputs: Q0 to Q2) Bypass with 1.0 μ F capacitor and place as close to the VDDOA pin as possible. |
| 19 | VDDOB | P | Output voltage supply—Bank B (Outputs: Q3 to Q5) Bypass with 1.0 μ F capacitor and place as close to the VDDOB pin as possible. |
| 20 | Q5b | O | Output clock 5 (complement) |
| 21 | Q5 | O | Output clock 5 |
| 22 | SFOUTB[0] | I | Output signal format control pin for Bank B. Three-level input control. Internally biased at $V_{DD}/2$. Can be left floating or tied to ground or V_{DD} . |

| Pin | Name | Type ¹ | Description |
|---------|-----------|-------------------|---|
| 23 | SFOUTB[1] | I | Output signal format control pin for Bank B. Three-level input control. Internally biased at $V_{DD}/2$. Can be left floating or tied to ground or V_{DD} . |
| 24 | DIVB | I | Output divider configuration bit for Bank B. Three-level input control. Internally biased at $V_{DD}/2$. Can be left floating or tied to ground or V_{DD} . |
| 25 | Q4b | O | Output clock 4 (complement) |
| 26 | Q4 | O | Output clock 4 |
| 27 | Q3b | O | Output clock 3 (complement) |
| 28 | Q3 | O | Output clock 3 |
| 29 | Q2b | O | Output clock 2 (complement) |
| 30 | Q2 | O | Output clock 2 |
| 31 | Q1b | O | Output clock 1 (complement) |
| 32 | Q1 | O | Output clock 1 |
| GND Pad | GND | GND | Power supply ground and thermal relief. |

Note:

1. Pin types are: I = input, O = output, P = power, GND = ground.

5.2 Si53302 Pin Descriptions

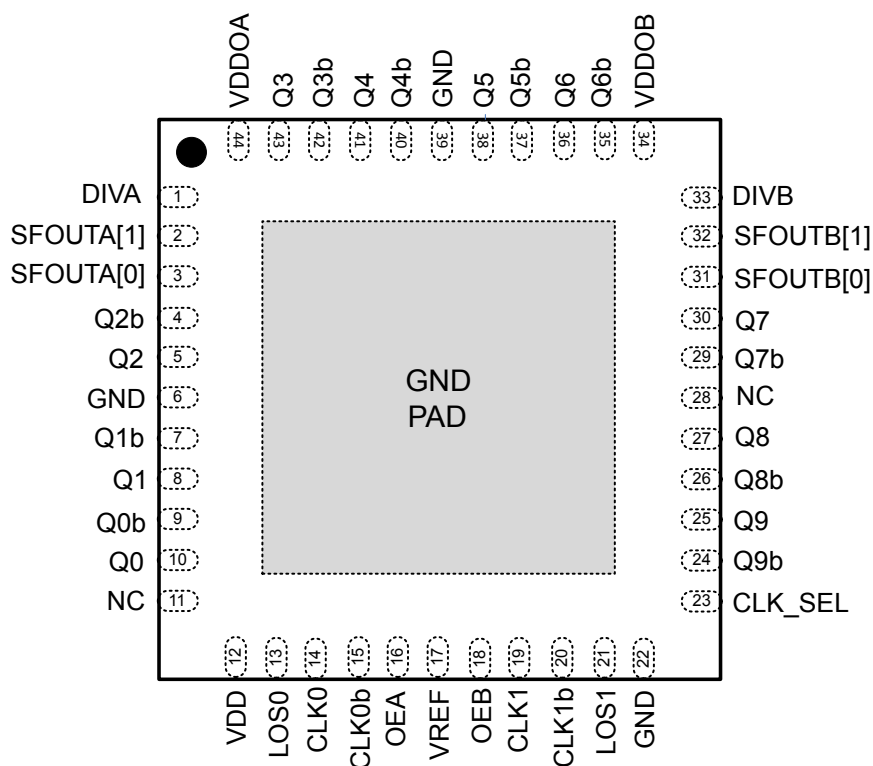


Table 5.2. Si53302 44-QFN Pin Descriptions

| Pin # | Name | Type ¹ | Description |
|-------|-----------|-------------------|---|
| 1 | DIVA | I | Output divider control pin for Bank A. Three-level input control. Internally biased at $V_{DD}/2$. Can be left floating or tied to ground or V_{DD} . |
| 2 | SFOUTA[1] | I | Output signal format control pin for Bank A. Three-level input control. Internally biased at $V_{DD}/2$. Can be left floating or tied to ground or V_{DD} . |
| 3 | SFOUTA[0] | I | Output signal format control pin for Bank A. Three-level input control. Internally biased at $V_{DD}/2$. Can be left floating or tied to ground or V_{DD} . |
| 4 | Q2b | O | Output clock 2 (complement). |
| 5 | Q2 | O | Output clock 2. |
| 6 | GND | GND | Ground. |
| 7 | Q1b | O | Output clock 1 (complement). |
| 8 | Q1 | O | Output clock 1. |
| 9 | Q0b | O | Output clock 0 (complement). |
| 10 | Q0 | O | Output clock 0. |
| 11 | NC | | No connect. Do not connect this pin to anything. |

| Pin # | Name | Type ¹ | Description |
|-------|---------|-------------------|---|
| 12 | VDD | P | Core voltage supply. Bypass with a 1.0 μ F capacitor placed as close to the pin as possible. |
| 13 | LOS0 | O | The LOS0 status pin indicates whether a clock is present at the CLK0 input: CLK0 input clock present LOS0 = 0 CLK0 input clock not present LOS0 = 1 |
| 14 | CLK0 | I | Input clock 0. |
| 15 | CLK0b | I | Input clock 0 (complement). When the CLK0 is driven by a single-end LVCMOS input, connect CLK0b to $V_{DD}/2$. |
| 16 | OEA | I | Output enable—Bank A. When OEA = high, the Bank A outputs are enabled. When OEA = low, Q is held low and Qb is held high for differential formats. For LVCMOS, both Q and Qb are held low when OEA is set low. OEA contains an internal pull-up resistor. |
| 17 | VREF | O | Reference voltage output. See section 2.3 Voltage Reference (V_{REF}) for details. |
| 18 | OEB | I | Output enable—Bank B. When OEB = high, the Bank B outputs are enabled. When OEB = low, Q is held low and Qb is held high for differential formats. For LVCMOS, both Q and Qb are held low when OEB is set low. OEB contains an internal pull-up resistor. |
| 19 | CLK1 | I | Input clock 1. |
| 20 | CLK1b | I | Input clock 1 (complement). When the CLK1 is driven by a single-end LVCMOS input, connect CLK1b to $V_{DD}/2$. |
| 21 | LOS1 | O | The LOS1 status pin indicates whether a clock is present at the CLK1 input: CLK1 input clock present LOS1 = 0 CLK1 input clock not present LOS1 = 1 |
| 22 | GND | GND | Ground. |
| 23 | CLK_SEL | I | MUX input select pin (LVCMOS). When CLK_SEL is high, CLK1 is selected. When CLK_SEL is low, CLK0 is selected. CLK_SEL contains an internal pull-down resistor. |
| 24 | Q9b | O | Output clock 9 (complement). |
| 25 | Q9 | O | Output clock 9. |
| 26 | Q8b | O | Output clock 8 (complement). |
| 27 | Q8 | O | Output clock 8. |
| 28 | NC | | No connect. |

| Pin # | Name | Type ¹ | Description |
|---------|-----------|-------------------|---|
| 29 | Q7b | O | Output clock 7 (complement). |
| 30 | Q7 | O | Output clock 7. |
| 31 | SFOUTB[0] | I | Output signal format control pin for Bank B. Three-level input control. Internally biased at $V_{DD}/2$. Can be left floating or tied to ground or V_{DD} . |
| 32 | SFOUTB[1] | I | Output signal format control pin for Bank B. Three-level input control. Internally biased at $V_{DD}/2$. Can be left floating or tied to ground or V_{DD} . |
| 33 | DIVB | I | Output divider configuration bit for Bank B. Three-level input control. Internally biased at $V_{DD}/2$. Can be left floating or tied to ground or V_{DD} . |
| 34 | VDDOB | P | Output Clock Voltage Supply—Bank B (Outputs: Q5 to Q9). Bypass with a 1.0 μ F capacitor placed as close to the pin as possible. |
| 35 | Q6b | O | Output clock 6 (complement). |
| 36 | Q6 | O | Output clock 6. |
| 37 | Q5b | O | Output clock 5 (complement). |
| 38 | Q5 | O | Output clock 5. |
| 39 | GND | GND | Ground. |
| 40 | Q4b | O | Output clock 4 (complement). |
| 41 | Q4 | O | Output clock 4. |
| 42 | Q3b | O | Output clock 3 (complement). |
| 43 | Q3 | O | Output clock 3. |
| 44 | VDDOA | P | Output Voltage Supply—Bank A (Outputs: Q0 to Q4). Bypass with a 1.0 μ F capacitor placed as close to the pin as possible. |
| GND Pad | GND | GND | Ground Pad. Power supply ground and thermal relief. |

Note:

1. Pin types are: I = input, O = output, P = power, GND = ground.

5.3 Si53303 Pin Descriptions

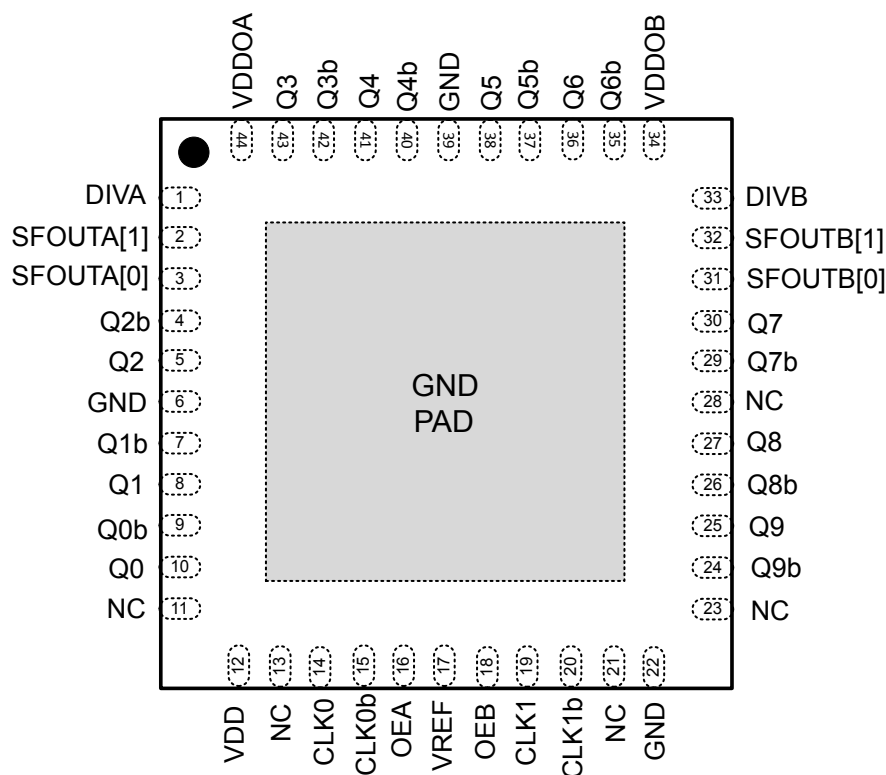


Table 5.3. Si53303 44-QFN Pin Descriptions

| Pin # | Name | Type ¹ | Description |
|-------|-----------|-------------------|---|
| 1 | DIVA | I | Output divider control pin for Bank A Three-level input control. Internally biased at VDD/2. Can be left floating or tied to ground or V _{DD} . |
| 2 | SFOUTA[1] | I | Output signal format control pin for Bank A Three-level input control. Internally biased at VDD/2. Can be left floating or tied to ground or V _{DD} . |
| 3 | SFOUTA[0] | I | Output signal format control pin for Bank A Three-level input control. Internally biased at VDD/2. Can be left floating or tied to ground or V _{DD} . |
| 4 | Q2b | O | Output clock 2 (complement) |
| 5 | Q2 | O | Output clock 2 |
| 6 | GND | GND | Ground |
| 7 | Q1b | O | Output clock 1 (complement) |
| 8 | Q1 | O | Output clock 1 |
| 9 | Q0b | O | Output clock 0 (complement) |
| 10 | Q0 | O | Output clock 0 |
| 11 | NC | | No connect. Do not connect this pin to anything. |

| Pin # | Name | Type ¹ | Description |
|-------|-----------|-------------------|--|
| 12 | VDD | P | Core voltage supply Bypass with 1.0 μ F capacitor placed as close to the VDD pin as possible |
| 13 | NC | | No connect |
| 14 | CLK0 | I | Input clock 0 |
| 15 | CLK0b | I | Input clock 0 (complement) When the CLK0 is driven by a single-end LVCMOS input, connect CLK0b to $V_{DD}/2$. |
| 16 | OEA | I | Output enable—Bank A When OE = high, the Bank A outputs are enabled When OE = low, Q is held low and Qb is held high for differential formats For LVCMOS, both Q and Qb are held low when OE is set low OEA contains an internal pull-up resistor |
| 17 | VREF | O | Reference voltage output. See section 2.3 Voltage Reference (V_{REF}) for details. |
| 18 | OEB | I | Output enable—Bank B When OE = high, the Bank B outputs are enabled When OE = low, Q is held low and Qb is held high for differential formats For LVCMOS, both Q and Qb are held low when OE is set low OEB contains an internal pull-up resistor. |
| 19 | CLK1 | I | Input clock 1 |
| 20 | CLK1b | I | Input clock 1 (complement) When the CLK1 is driven by a single-end LVCMOS input, connect CLK1b to $V_{DD}/2$. |
| 21 | NC | | No connect |
| 22 | GND | GND | Ground |
| 23 | NC | | No connect |
| 24 | Q9b | O | Output clock 9 (complement) |
| 25 | Q9 | O | Output clock 9 |
| 26 | Q8b | O | Output clock 8 (complement) |
| 27 | Q8 | O | Output clock 8 |
| 28 | NC | | No connect |
| 29 | Q7b | O | Output clock 7 (complement) |
| 30 | Q7 | O | Output clock 7 |
| 31 | SFOUTB[0] | I | Output signal format control pin for Bank B Three-level input control. Internally biased at $V_{DD}/2$. Can be left floating or tied to ground or V_{DD} . |
| 32 | SFOUTB[1] | I | Output signal format control pin for Bank B Three-level input control. Internally biased at $V_{DD}/2$. Can be left floating or tied to ground or V_{DD} . |

| Pin # | Name | Type ¹ | Description |
|---------|-------|-------------------|--|
| 33 | DIVB | I | Output divider configuration bit for Bank B Three-level input control. Internally biased at $V_{DD}/2$. Can be left floating or tied to ground or V_{DD} . |
| 34 | VDDOB | P | Output Clock Voltage Supply—Bank B (Outputs: Q5 to Q9) Bypass with 1.0 μ F capacitor and place close to the VDDOB pin as possible. |
| 35 | Q6b | O | Output clock 6 (complement) |
| 36 | Q6 | O | Output clock 6 |
| 37 | Q5b | O | Output clock 5 (complement) |
| 38 | Q5 | O | Output clock 5. |
| 39 | GND | GND | Ground. |
| 40 | Q4b | O | Output clock 4 (complement) |
| 41 | Q4 | O | Output clock 4. |
| 42 | Q3b | O | Output clock 3 (complement) |
| 43 | Q3 | O | Output clock 3 |
| 44 | VDDOA | P | Output Voltage Supply—Bank A (Outputs: Q0 to Q4) Bypass with 1.0 μ F capacitor and place close to the VDDOA pin as possible. |
| GND Pad | GND | GND | Ground Pad Power supply ground and thermal relief. |

Note:

1. Pin types are: I = input, O = output, P = power, GND = ground.

5.4 Si53304 Pin Descriptions

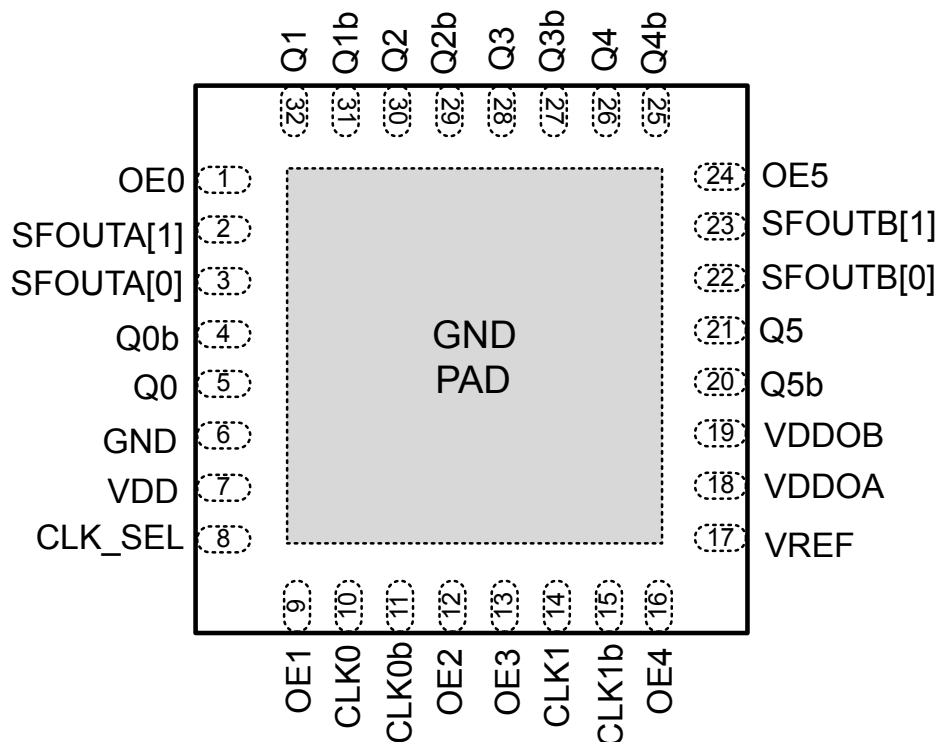


Table 5.4. Si53304 32-QFN Pin Descriptions

| Pin | Name | Type ¹ | Description |
|-----|-----------|-------------------|---|
| 1 | OE0 | I | Output enable—Output 0 When OE = high, Q0 is enabled. When OE = low, Q is held low and Qb is held high for differential formats. For LVCMOS, both Q and Qb are held low when OE is set low. This pin contains an internal pull-up resistor. |
| 2 | SFOUTA[1] | I | Output signal format control pin for Bank A Three level input control. Internally biased at $V_{DD}/2$. Can be left floating or tied to ground or V_{DD} . |
| 3 | SFOUTA[0] | I | Output signal format control pin for Bank A Three level input control. Internally biased at $V_{DD}/2$. Can be left floating or tied to ground or V_{DD} . |
| 4 | Q0b | O | Output clock 0 (complement) |
| 5 | Q0 | O | Output clock 0 |
| 6 | GND | GND | Ground |
| 7 | VDD | P | Core voltage supply Bypass with 1.0 μ F capacitor and place as close to the V_{DD} pin as possible. |

| Pin | Name | Type ¹ | Description |
|-----|---------|-------------------|---|
| 8 | CLK_SEL | I | Mux input select pin (LVCMOS) When CLK_SEL is high, CLK1 is selected. When CLK_SEL is low, CLK0 is selected. CLK_SEL contains an internal pull-down resistor. |
| 9 | OE1 | I | Output enable—Output 1 When OE = high, Q1 is enabled. When OE = low, Q is held low and Qb is held high for differential formats. For LVCMOS, both Q and Qb are held low when OE is set low. This pin contains an internal pull-up resistor. |
| 10 | CLK0 | I | Input clock 0 |
| 11 | CLK0b | I | Input clock 0 (complement) When the CLK0 is driven by a single-end input, connect CLK0b to $V_{DD}/2$. |
| 12 | OE2 | I | Output enable—Output 2 When OE = high, Q2 is enabled. When OE = low, Q is held low and Qb is held high for differential formats. For LVCMOS, both Q and Qb are held low when OE is set low. OE2 contains an internal pull-up resistor. |
| 13 | OE3 | I | Output enable—Output 3 When OE = high, Q3 is enabled. When OE = low, Q is held low and Qb is held high for differential formats. For LVCMOS, both Q and Qb are held low when OE is set low. OE3 contains an internal pull-up resistor. |
| 14 | CLK1 | I | Input clock 1 |
| 15 | CLK1b | I | Input clock 1 (complement) When the CLK1 is driven by a single-end input, connect CLK1b to $V_{DD}/2$. |
| 16 | OE4 | I | Output enable—Output 4 When OE = high, Q4 is enabled. When OE = low, Q is held low and Qb is held high for differential formats. For LVCMOS, both Q and Qb are held low when OE is set low. This pin contains an internal pull-up resistor. |
| 17 | VREF | O | See 2.3 Voltage Reference (V_{REF}) for details. |
| 18 | VDDOA | P | Output voltage supply—Bank A (Outputs: Q0 to Q2) Bypass with 1.0 μ F capacitor and place as close to the VDDOA pin as possible. |
| 19 | VDDOB | P | Output voltage supply—Bank B (Outputs: Q3 to Q5) Bypass with 1.0 μ F capacitor and place as close to the VDDOB pin as possible. |
| 20 | Q5b | O | Output clock 5 (complement) |

| Pin | Name | Type ¹ | Description |
|---------|-----------|-------------------|---|
| 21 | Q5 | O | Output clock 5 |
| 22 | SFOUTB[0] | I | Output signal format control pin for Bank B Three level input control. Internally biased at $V_{DD}/2$. Can be left floating or tied to ground or V_{DD} . |
| 23 | SFOUTB[1] | I | Output signal format control pin for Bank B Three level input control. Internally biased at $V_{DD}/2$. Can be left floating or tied to ground or V_{DD} . |
| 24 | OE5 | I | Output enable—Output 5 When OE = high, Q5 is enabled. When OE = low, Q is held low and Qb is held high for differential formats. For LVCMOS, both Q and Qb are held low when OE is set low. This pin contains an internal pull-up resistor. |
| 25 | Q4b | O | Output clock 4 (complement) |
| 26 | Q4 | O | Output clock 4 |
| 27 | Q3b | O | Output clock 3 (complement) |
| 28 | Q3 | O | Output clock 3 |
| 29 | Q2b | O | Output clock 2 (complement) |
| 30 | Q2 | O | Output clock 2 |
| 31 | Q1b | O | Output clock 1 (complement) |
| 32 | Q1 | O | Output clock 1 |
| GND Pad | GND | GND | Ground Pad Power supply ground and thermal relief. |

Note:

1. Pin types are: I = input, O = output, P = power, GND = ground.

5.5 Si53305 Pin Descriptions

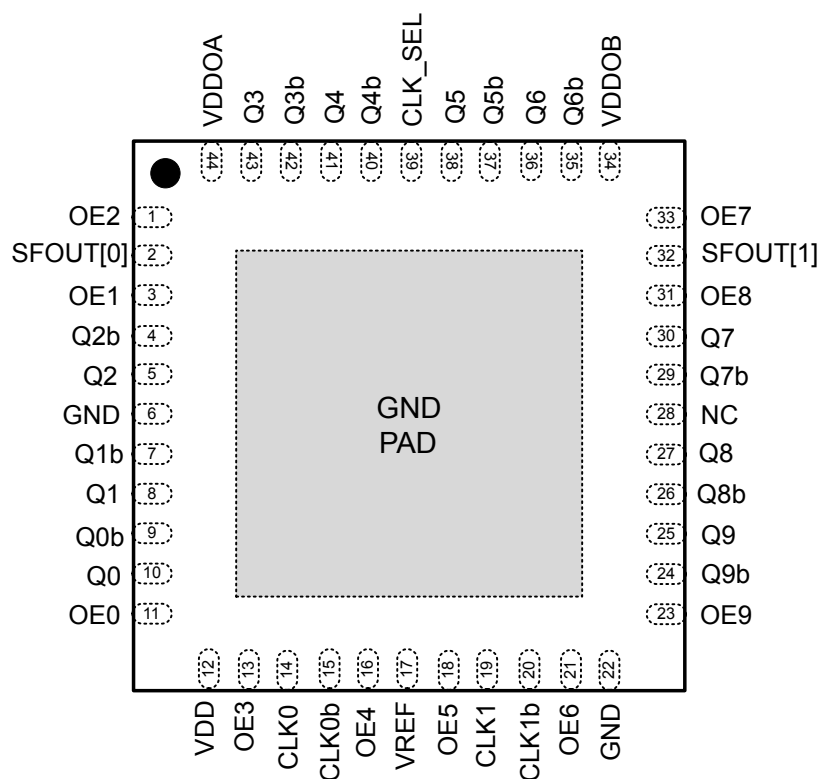


Table 5.5. Si53305 44-QFN Pin Descriptions

| Pin # | Name | Type ¹ | Description |
|-------|----------|-------------------|---|
| 1 | OE2 | I | Output enable—Output 2 When OE = high, Q2 is enabled. When OE = low, Q is held low, and Qb is held high for differential formats. For LVCMOS, both Q and Qb are held low when OE is set low. OE2 contains an internal pull-up resistor. |
| 2 | SFOUT[0] | I | Output signal format control pin [0] Three-level input control. Internally biased at $V_{DD}/2$. Can be left floating or tied to ground or V_{DD} . |
| 3 | OE1 | I | Output enable—Output 1 When OE = high, Q1 is enabled. When OE = low, Q is held low, and Qb is held high for differential formats. For LVCMOS, both Q and Qb are held low when OE is set low. OE1 contains an internal pull-up resistor. |
| 4 | Q2b | O | Output clock 2 (complement) |
| 5 | Q2 | O | Output clock 2 |
| 6 | GND | GND | Ground |
| 7 | Q1b | O | Output clock 1 (complement) |

| Pin # | Name | Type ¹ | Description |
|-------|-------|-------------------|---|
| 8 | Q1 | O | Output clock 1 |
| 9 | Q0b | O | Output clock 0 (complement) |
| 10 | Q0 | O | Output clock 0 |
| 11 | OE0 | I | Output enable—Output 0 When OE = high, Q0 is enabled. When OE = low, Q is held low, and Qb is held high for differential formats. For LVCMOS, both Q and Qb are held low when OE is set low. OE0 contains an internal pull-up resistor. |
| 12 | VDD | P | Core voltage supply Bypass with 1.0 μ F capacitor and place close to the VDD pin as possible |
| 13 | OE3 | I | Output Enable 3 When OE = high, Q3 is enabled. When OE = low, Q is held low, and Qb is held high for differential formats. For LVCMOS, both Q and Qb are held low when OE is set low. OE3 contains an internal pull-up resistor. |
| 14 | CLK0 | I | Input clock 0 |
| 15 | CLK0b | I | Input clock 0 (complement) When CLK0 is driven by a single-ended input, connect CLK0b to $V_{DD}/2$. |
| 16 | OE4 | I | Output Enable 4 When OE = high, Q4 is enabled. When OE = low, Q is held low, and Qb is held high for differential formats. For LVCMOS, both Q and Qb are held low when OE is set low. OE4 contains an internal pull-up resistor. |
| 17 | VREF | O | Reference voltage output. See 2.3 Voltage Reference (V_{REF}) for details. |
| 18 | OE5 | I | Output Enable 5 When OE = high, Q5 is enabled. When OE = low, Q is held low, and Qb is held high for differential formats. For LVCMOS, both Q and Qb are held low when OE is set low. OE5 contains an internal pull-up resistor. |
| 19 | CLK1 | I | Input clock 1 |
| 20 | CLK1b | I | Input clock 1 (complement) When CLK1 is driven by a single-ended input, connect CLK1b to $V_{DD}/2$. |

| Pin # | Name | Type ¹ | Description |
|-------|----------|-------------------|--|
| 21 | OE6 | I | Output Enable 6 When OE = high, Q6 is enabled. When OE = low, Q is held low, and Qb is held high for differential formats. For LVCMOS, both Q and Qb are held low when OE is set low. OE6 contains an internal pull-up resistor. |
| 22 | GND | GND | Ground |
| 23 | OE9 | I | Output Enable 9 When OE = high, Q9 is enabled. When OE = low, Q is held low, and Qb is held high for differential formats. For LVCMOS, both Q and Qb are held low when OE is set low. OE9 contains an internal pull-up resistor. |
| 24 | Q9b | O | Output clock 9 (complement) |
| 25 | Q9 | O | Output clock 9 |
| 26 | Q8b | O | Output clock 8 (complement) |
| 27 | Q8 | O | Output clock 8 |
| 28 | NC | | No Connect |
| 29 | Q7b | O | Output clock 7 (complement) |
| 30 | Q7 | O | Output clock 7 |
| 31 | OE8 | I | Output Enable 8 When OE = high, Q8 is enabled. When OE = low, Q is held low, and Qb is held high for differential formats. For LVCMOS, both Q and Qb are held low when OE is set low. OE8 contains an internal pull-up resistor. |
| 32 | SFOUT[1] | I | Output signal format control pin [1] Three-level input control. Internally biased at $V_{DD}/2$. Can be left floating or tied to ground or V_{DD} . |
| 33 | OE7 | I | Output Enable 7 When OE = high, Q7 is enabled. When OE = low, Q is held low, and Qb is held high for differential formats. For LVCMOS, both Q and Qb are held low when OE is set low. OE7 contains an internal pull-up resistor. |
| 34 | VDDOB | P | Output voltage supply—Bank B (Outputs Q5 through Q9) Bypass with 1.0 μ F capacitor and place as close to VDDOB pin as possible. |
| 35 | Q6b | O | Output clock 6 (complement) |
| 36 | Q6 | O | Output clock 6 |
| 37 | Q5b | O | Output clock 5 (complement) |
| 38 | Q5 | O | Output clock 5 |

| Pin # | Name | Type ¹ | Description |
|---------|---------|-------------------|---|
| 39 | CLK_SEL | I | MUX input select pin (LVCMOS) When CLK_SEL is high, CLK1 is selected When CLK_SEL is low, CLK0 is selected CLK_SEL contains an internal pull-down resistor |
| 40 | Q4b | O | Output clock 4 (complement) |
| 41 | Q4 | O | Output clock 4 |
| 42 | Q3b | O | Output clock 3 (complement) |
| 43 | Q3 | O | Output clock 3 |
| 44 | VDDOA | P | Output voltage supply—Bank A (Outputs Q0 to Q4) Bypass with 1.0 μ F capacitor and place as close to VDDOA pin as possible. |
| GND Pad | GND | GND | Ground Pad Power supply ground and thermal relief |

Note:

1. Pin types are: I = input, O = output, P = power, GND = ground.

5.6 Si53306 Pin Descriptions

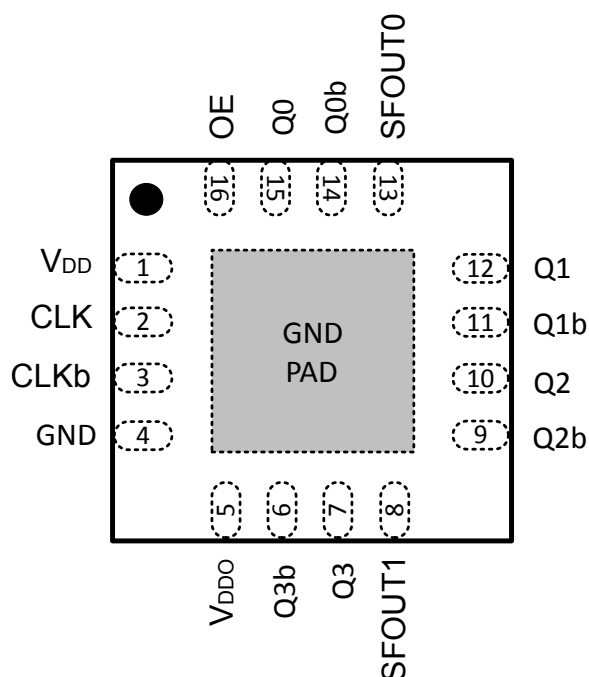


Table 5.6. Si53306 16-QFN Pin Descriptions

| Pin | Name | Type ¹ | Description |
|-----|--------|-------------------|--|
| 1 | VDD | P | Core voltage supply. Bypass with 1.0 μ F capacitor and place as close to the VDD pin as possible. |
| 2 | CLK | I | Input clock. |
| 3 | CLKb | I | Input clock (complement). When the CLK is driven by a single-ended input, connect CLKb to VDD/2. |
| 4 | GND | GND | Ground. |
| 5 | VDDO | P | Output voltage supply— All outputs (Q0 to Q3). Bypass with 1.0 μ F capacitor and place as close to the VDDO pin as possible. |
| 6 | Q3b | O | Output clock 3 (complement). |
| 7 | Q3 | O | Output clock 3. |
| 8 | SFOUT1 | I | Output signal format control pin 1. Three-level input control. Internally biased at VDD/2. Can be left floating or tied to ground or VDD. |
| 9 | Q2b | O | Output clock 2 (complement). |
| 10 | Q2 | O | Output clock 2. |
| 11 | Q1b | O | Output clock 1 (complement). |
| 12 | Q1 | O | Output clock 1. |

| Pin | Name | Type ¹ | Description |
|---------|--------|-------------------|--|
| 13 | SFOUT0 | I | Output signal format control pin 0. Three-level input control. Internally biased at VDD/2. Can be left floating or tied to ground or VDD. |
| 14 | Q0b | O | Output clock 0 (complement). |
| 15 | Q0 | O | Output clock 0. |
| 16 | OE | I | Output enable. When OE = high, all outputs are enabled. When OE = low, Q is held low, and Qb is held high for differential formats. For LVCMOS, both Q and Qb are held low when OE is set low. OE contains an internal pull-up resistor. |
| GND Pad | GND | GND | Ground. |

Note:

1. Pin types are: I = input, O = output, P = power, GND = ground.

5.7 Si53307 Pin Descriptions

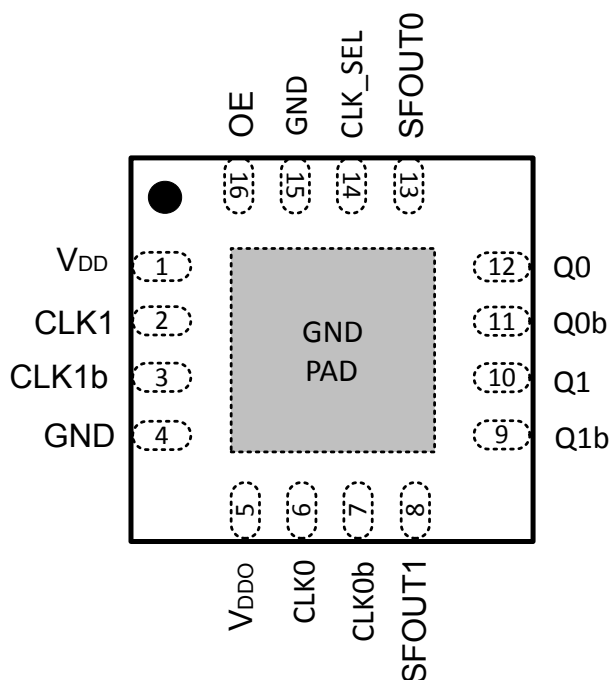


Table 5.7. Si53307 16-QFN Pin Descriptions

| Pin | Name | Type ¹ | Description |
|-----|--------|-------------------|--|
| 1 | VDD | P | Core voltage supply. Bypass with 1.0 μ F capacitor and place as close to the VDD pin as possible. |
| 2 | CLK1 | I | Input clock 1. |
| 3 | CLK1b | I | Input clock 1 (complement). When CLK1 is driven by a single-ended input, connect CLK1b to VDD/2. |
| 4 | GND | GND | Ground. |
| 5 | VDDO | P | Output clock supply voltage. Bypass with 1.0 μ F capacitor and place as close to the VDDO pin as possible. |
| 6 | CLK0 | I | Input clock 0. |
| 7 | CLK0b | I | Input clock 0 (complement). When CLK0 is driven by a single-ended input, connect CLK0b to VDD/2. |
| 8 | SFOUT1 | I | Output signal format control pin 1. Three-level input control. Internally biased at VDD/2. Can be left floating or tied to ground or VDD. |
| 9 | Q1b | O | Output clock 1 (complement). |
| 10 | Q1 | O | Output clock 1. |
| 11 | Q0b | O | Output clock 0 (complement). |
| 12 | Q0 | O | Output clock 0. |

| Pin | Name | Type ¹ | Description |
|---|---------|-------------------|--|
| 13 | SFOUT0 | I | Output signal format control pin 0. Three-level input control. Internally biased at VDD/2. Can be left floating or tied to ground or VDD. |
| 14 | CLK_SEL | I | Mux input select pin: When CLK_SEL is high, CLK1 is selected. When CLK_SEL is low, CLK0 is selected. CLK_SEL contains an internal pull-down resistor. |
| 15 | GND | GND | Ground. |
| 16 | OE | I | Output enable. When OE = high, all outputs are enabled. When OE = low, Q is held low, and Qb is held high for differential formats. For LVCMOS, both Q and Qb are held low when OE is set low. OE contains an internal pull-up resistor. |
| GND Pad | GND | GND | Ground. |
| Note: 1. Pin types are: I = input, O = output, P = power, GND = ground. | | | |

5.8 Si53308 Pin Descriptions

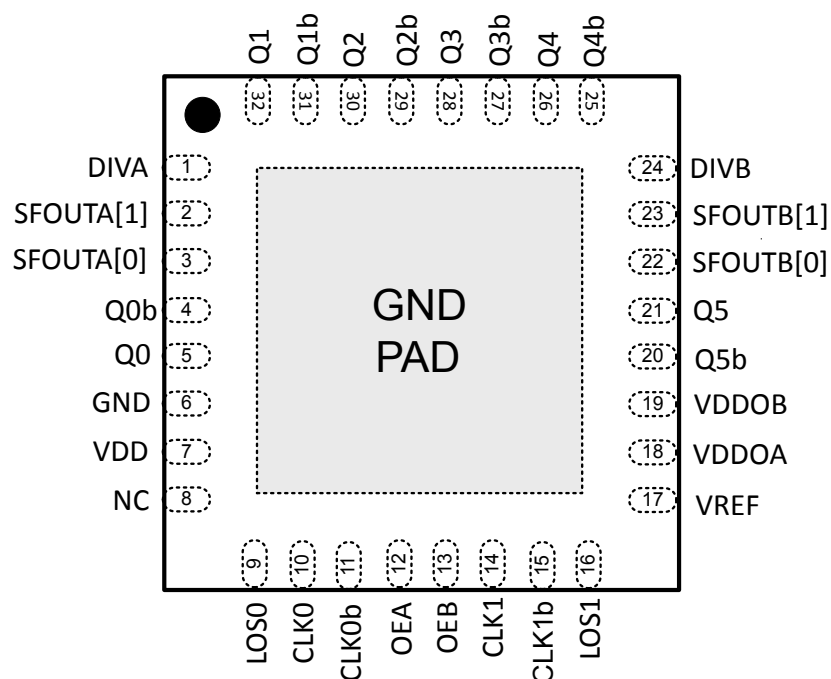


Table 5.8. Si53308 32-QFN Pin Descriptions

| Pin | Name | Type ¹ | Description |
|-----|-----------|-------------------|---|
| 1 | DIVA | I | Output divider control pin for Bank A. Three-level input control. Internally biased at VDD/2. Can be left floating or tied to ground or VDD. |
| 2 | SFOUTA[1] | I | Output signal format control pin 1 for Bank A. Three-level input control. Internally biased at VDD/2. Can be left floating or tied to ground or VDD. |
| 3 | SFOUTA[0] | I | Output signal format control pin 0 for Bank A. Three-level input control. Internally biased at VDD/2. Can be left floating or tied to ground or VDD. |
| 4 | Q0b | O | Output clock 0 (complement). |
| 5 | Q0 | O | Output clock 0. |
| 6 | GND | GND | Ground. |
| 7 | VDD | P | Core voltage supply. Bypass with 1.0 μ F capacitor and place close to the VDD pin as possible. |
| 8 | NC | | No connect. |
| 9 | LOS0 | O | The LOS0 status pin indicates whether a clock is present (LOS0 = 0) or not present (LOS0 = 1) at the CLK0 input. |
| 10 | CLK0 | I | Input clock 0. |
| 11 | CLK0b | I | Input clock 0 (complement). When CLK0 is driven by a single-ended input, connect CLK0b to VDD/2. |

| Pin | Name | Type ¹ | Description |
|-----|-----------|-------------------|--|
| 12 | OEA | I | Output enable—Bank A. When OE = high, the Bank A outputs are enabled. When OE = low, Q is held low and Qb is held high for differential formats. For LVCMOS, both Q and Qb are held low when OE is set low. OEA contains an internal pull-up resistor. |
| 13 | OEB | I | Output enable—Bank B. When OE = high, the Bank B outputs are enabled. When OE = low, Q is held low and Qb is held high for differential formats. For LVCMOS, both Q and Qb are held low when OE is set low. OEB contains an internal pull-up resistor. |
| 14 | CLK1 | I | Input clock 1. |
| 15 | CLK1b | I | Input clock 1 (complement). When CLK1 is driven by a single-ended input, connect CLK1b to VDD/2. |
| 16 | LOS1 | O | The LOS1 status pin indicates whether a clock is present (LOS1 = 0) or not present (LOS1 = 1) at the CLK1 input. |
| 17 | VREF | O | Reference voltage. |
| 18 | VDDOA | P | Output Clock Voltage Supply—Bank A (Outputs: Q0 to Q2). Bypass with 1.0 μ F capacitor and place as close to the VDDOA pin as possible. |
| 19 | VDDOB | P | Output Clock Voltage Supply—Bank B (Outputs: Q3 to Q5). Bypass with 1.0 μ F capacitor and place as close to the VDDOB pin as possible. |
| 20 | Q5b | O | Output clock 5 (complement). |
| 21 | Q5 | O | Output clock 5. |
| 22 | SFOUTB[0] | I | Output signal format control pin 0 for Bank B. Three-level input control. Internally biased at VDD/2. Can be left floating or tied to ground or VDD. |
| 23 | SFOUTB[1] | I | Output signal format control pin 1 or Bank B. Three-level input control. Internally biased at VDD/2. Can be left floating or tied to ground or VDD. |
| 24 | DIVB | I | Output divider control pin for Bank B. Three-level input control. Internally biased at VDD/2. Can be left floating or tied to ground or VDD. |
| 25 | Q4b | O | Output clock 4 (complement). |
| 26 | Q4 | O | Output clock 4. |
| 27 | Q3b | O | Output clock 3 (complement). |
| 28 | Q3 | O | Output clock 3. |
| 29 | Q2b | O | Output clock 2 (complement). |

| Pin | Name | Type ¹ | Description |
|---------|------|-------------------|--|
| 30 | Q2 | O | Output clock 2. |
| 31 | Q1b | O | Output clock 1 (complement). |
| 32 | Q1 | O | Output clock 1. |
| GND Pad | GND | GND | Ground Pad. Power supply ground and thermal relief. |

Note:

1. Pin types are: I = input, O = output, P = power, GND = ground.

6. Package Outlines

6.1 16-QFN Package Diagram

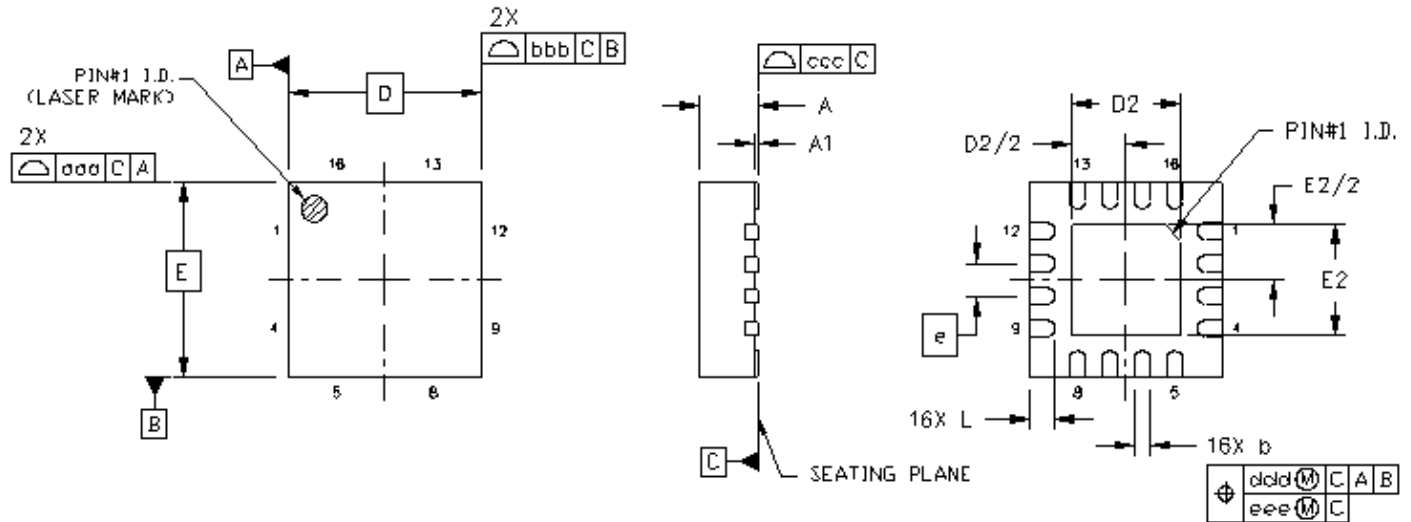


Figure 6.1. 3x3 mm 16-QFN Package Diagram Dimensions

Table 6.1. Package Diagram Dimensions

| Dimension | Min | Nom | Max |
|-----------|----------|------|------|
| A | 0.80 | 0.85 | 0.90 |
| A1 | 0.00 | 0.02 | 0.05 |
| b | 0.18 | 0.25 | 0.30 |
| D | 3.00 BSC | | |
| D2 | 1.70 | 1.80 | 1.90 |
| e | 0.50 BSC | | |
| E | 3.00 BSC | | |
| E2 | 1.70 | 1.80 | 1.90 |
| L | 0.30 | 0.40 | 0.50 |
| aaa | — | — | 0.10 |
| bbb | — | — | 0.10 |
| ccc | — | — | 0.08 |
| ddd | — | — | 0.10 |
| eee | — | — | 0.05 |

Notes:

1. All dimensions shown are in millimeters (mm) unless otherwise noted.
2. Dimensioning and Tolerancing per ANSI Y14.5M-1994.

6.2 32-QFN Package Diagram

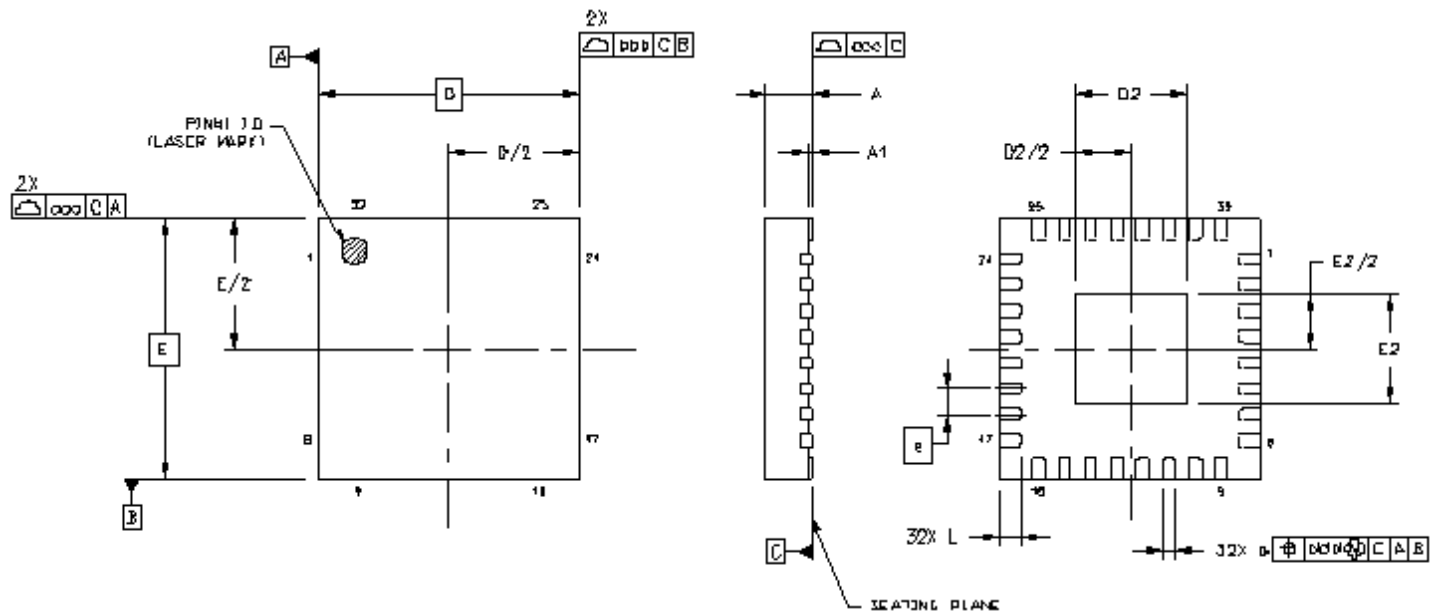


Figure 6.2. 5x5 mm 32-QFN Package Diagram Dimensions

Table 6.2. Package Diagram Dimensions

| Dimension | Min | Nom | Max |
|-----------|----------|------|------|
| A | 0.80 | 0.85 | 1.00 |
| A1 | 0.00 | 0.02 | 0.05 |
| b | 0.18 | 0.25 | 0.30 |
| c | 0.20 | 0.25 | 0.30 |
| D | 5.00 BSC | | |
| D2 | 2.00 | 2.15 | 2.30 |
| e | 0.50 BSC | | |
| E | 5.00 BSC | | |
| E2 | 2.00 | 2.15 | 2.30 |
| L | 0.30 | 0.40 | 0.50 |
| aaa | 0.10 | | |
| bbb | 0.10 | | |
| ccc | 0.08 | | |
| ddd | 0.10 | | |

Notes:

1. All dimensions shown are in millimeters (mm) unless otherwise noted.
2. Dimensioning and Tolerancing per ANSI Y14.5M-1994.
3. This drawing conforms to the JEDEC Solid State Outline MO-220.

6.3 44-QFN Package Diagram

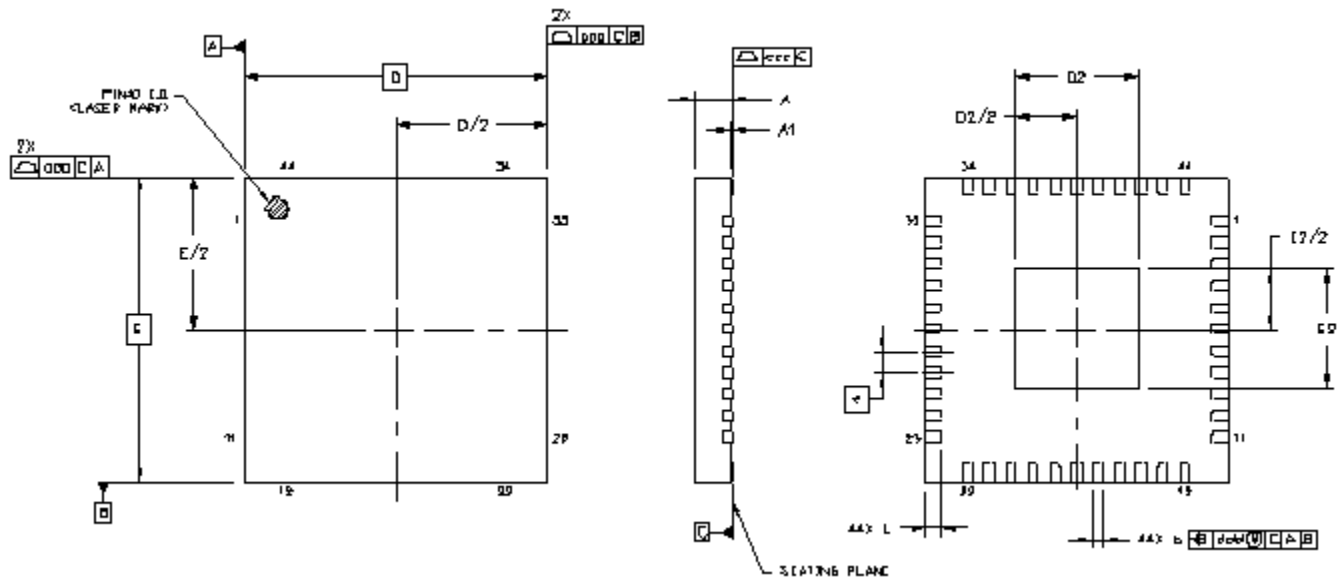


Figure 6.3. 7x7 mm 44-QFN Package Diagram Dimensions

Table 6.3. Package Diagram Dimensions

| Dimension | Min | Nom | Max |
|-----------|----------|------|------|
| A | 0.80 | 0.85 | 0.90 |
| A1 | 0.00 | 0.02 | 0.05 |
| b | 0.18 | 0.25 | 0.30 |
| D | 7.00 BSC | | |
| D2 | 2.65 | 2.80 | 2.95 |
| e | 0.50 BSC | | |
| E | 7.00 BSC | | |
| E2 | 2.65 | 2.80 | 2.95 |
| L | 0.30 | 0.40 | 0.50 |
| aaa | — | — | 0.10 |
| bbb | — | — | 0.10 |
| ccc | — | — | 0.08 |
| ddd | — | — | 0.10 |

Notes:

1. All dimensions shown are in millimeters (mm) unless otherwise noted.
2. Dimensioning and Tolerancing per ANSI Y14.5M-1994.
3. This drawing conforms to the JEDEC Solid State Outline MO-220.
4. Recommended card reflow profile is per the JEDEC/IPC J-STD-020 specification for Small Body Components.

7. Land Patterns

7.1 16-QFN Land Pattern

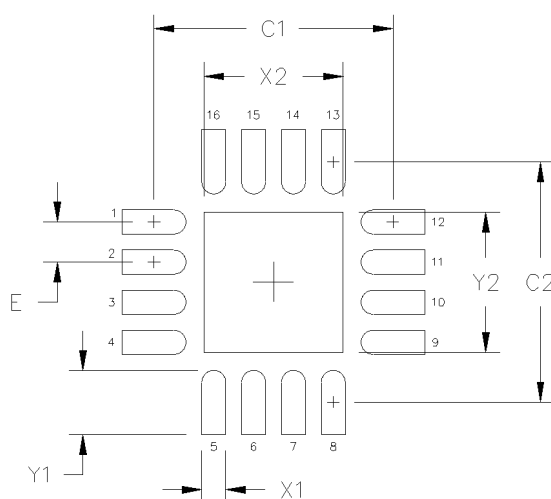


Figure 7.1. 3x3 mm 16-QFN Land Pattern

Table 7.1. PCB Land Pattern

| Dimension | mm |
|-----------|------|
| C1 | 3.00 |
| C2 | 3.00 |
| E | 0.50 |
| X1 | 0.30 |
| Y1 | 0.80 |
| X2 | 1.80 |
| Y2 | 1.80 |

Notes:

General

- All dimensions shown are in millimeters (mm).
- This Land Pattern Design is based on the IPC-7351 guidelines.
- All dimensions shown are at Maximum Material Condition (MMC). Least Material Condition (LMC) is calculated based on a Fabrication Allowance of 0.05 mm.

Solder Mask Design

- All metal pads are to be non-solder mask defined (NSMD). Clearance between the solder mask and the metal pad is to be 60µm minimum, all the way around the pad.

Stencil Design

- A stainless steel, laser-cut and electro-polished stencil with trapezoidal walls should be used to assure good solder paste release.
- The stencil thickness should be 0.125 mm (5 mils).
- The ratio of stencil aperture to land pad size should be 1:1 for all perimeter pads.
- A 2 x 2 array of 0.65 mm square openings on a 0.90 mm pitch should be used for the center ground pad.

Card Assembly

- A No-Clean, Type-3 solder paste is recommended.
- The recommended card reflow profile is per the JEDEC/IPC J-STD-020 specification for Small Body Components.

7.2 32-QFN Land Pattern

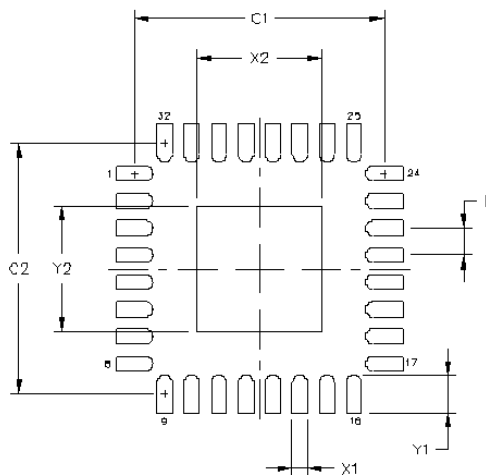


Figure 7.2. 5x5 mm 32-QFN Land Pattern

Table 7.2. PCB Land Pattern

| Dimension | Min | Max |
|-----------|----------|------|
| C1 | 4.52 | 4.62 |
| C2 | 4.52 | 4.62 |
| E | 0.50 BSC | |
| X1 | 0.20 | 0.30 |
| X2 | 2.20 | 2.30 |
| Y1 | 0.59 | 0.69 |
| Y2 | 2.20 | 2.30 |

Notes:**General**

1. All dimensions shown are in millimeters (mm) unless otherwise noted.
2. This Land Pattern Design is based on the IPC-7351 guidelines.

Solder Mask Design

1. All metal pads are to be non-solder mask defined (NSMD). Clearance between the solder mask and the metal pad is to be 60 μm minimum, all the way around the pad.

Stencil Design

1. A stainless steel, laser-cut and electro-polished stencil with trapezoidal walls should be used to assure good solder paste release.
2. The stencil thickness should be 0.125 mm (5 mils).
3. The ratio of stencil aperture to land pad size should be 1:1 for all perimeter pads.
4. A 2x2 array of 0.75 mm square openings on 1.15 mm pitch should be used for the center ground pad.

Card Assembly

1. A No-Clean, Type-3 solder paste is recommended.
2. The recommended card reflow profile is per the JEDEC/IPC J-STD-020 specification for Small Body Components.

7.3 44-QFN Land Pattern

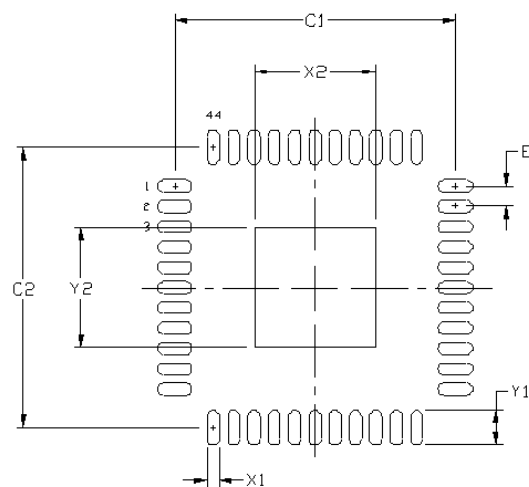


Figure 7.3. 7x7 mm 44-QFN Land Pattern

Table 7.3. PCB Land Pattern

| Dimension | Min | Max |
|-----------|----------|------|
| C1 | 6.80 | 6.90 |
| C2 | 6.80 | 6.90 |
| E | 0.50 BSC | |
| X1 | 0.20 | 0.30 |
| X2 | 2.85 | 2.95 |
| Y1 | 0.75 | 0.85 |
| Y2 | 2.85 | 2.95 |

Notes:**General**

1. All dimensions shown are in millimeters (mm) unless otherwise noted.
2. This Land Pattern Design is based on the IPC-7351 guidelines.

Solder Mask Design

1. All metal pads are to be non-solder mask defined (NSMD). Clearance between the solder mask and the metal pad is to be 60 μm minimum, all the way around the pad.

Stencil Design

1. A stainless steel, laser-cut and electro-polished stencil with trapezoidal walls should be used to assure good solder paste release.
2. The stencil thickness should be 0.125 mm (5 mils).
3. The ratio of stencil aperture to land pad size should be 1:1 for all perimeter pads.
4. A 2x2 array of 1.0 mm square openings on 1.45 mm pitch should be used for the center ground pad.

Card Assembly

1. A No-Clean, Type-3 solder paste is recommended.
2. The recommended card reflow profile is per the JEDEC/IPC J-STD-020 specification for Small Body Components.

8. Top Markings

8.1 Si53301/04/08 Top Markings

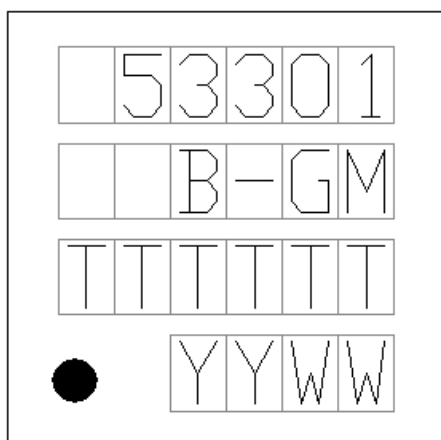


Figure 8.1. Si53301 Top Marking

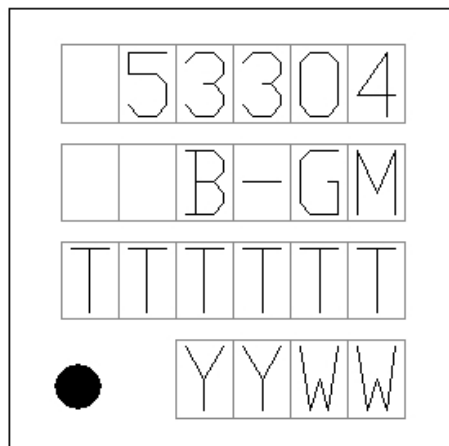


Figure 8.2. Si53304 Top Marking

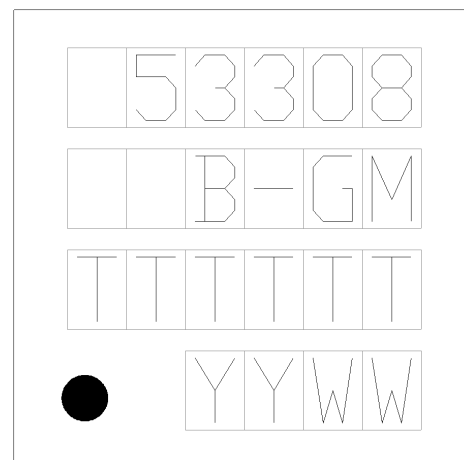


Figure 8.3. Si53308 Top Marking

Table 8.1. Si53301/04/08 32-QFN Top Marking Explanation

| | | |
|------------------------|--|--|
| Mark Method: | Laser | |
| Font Size: | 2.0 Point (28 mils) Center-Justified | |
| Line 1 Marking: | Device Part Number | 53301 for Si53301-B-GM 53304 for Si53304-B-GM 53308 for Si53308-B-GM |
| Line 2 Marking: | Device Revision/Type | B-GM |
| Line 3 Marking: | TTTTTT = Mfg Code | Manufacturing Code |
| Line 4 Marking | Circle = 0.5 mm Diameter Lower-Left Justified | Pin 1 Identifier |
| | YY = Year WW = Work Week | Assigned by Assembly Supplier. Corresponds to the year and work week of the mold date. |

8.2 Si53302/03/05 Top Markings



Figure 8.4. Si53302 Top Marking

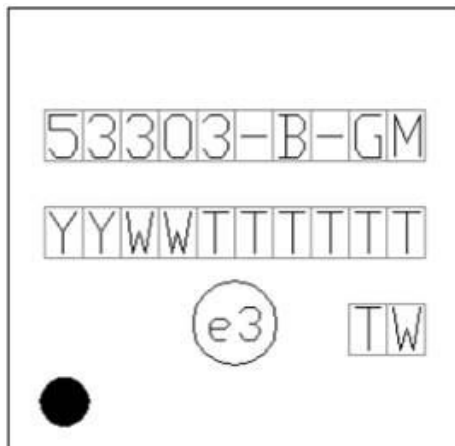


Figure 8.5. Si53303 Top Marking



Figure 8.6. Si53305 Top Marking

Table 8.2. Si53302/03/05 44-QFN Top Marking Explanation

| | | |
|------------------------|--|--|
| Mark Method: | Laser | |
| Font Size: | 1.9 Point (26 mils) Right-Justified | |
| Line 1 Marking: | Device Part Number | 53302 for Si53302-B-GM 53303 for Si53303-B-GM 53305 for Si53305-B-GM |
| Line 2 Marking: | YY = Year WW=Work Week | Assigned by Assembly Supplier. Corresponds to the year and work week of the mold date. |
| | TTTTTT = Mfg Code | Manufacturing Code from the Assembly Purchase Order form. |
| Line 3 Marking: | Circle=1.3 mm Diameter Center-Justified | "e3" Pb-Free Symbol |
| | Country of Origin ISO Code Abbreviation | TW |
| Line 4 Marking | Circle = 0.75 mm Diameter Filled | Pin 1 Identification |

8.3 Si53306/07 Top Markings

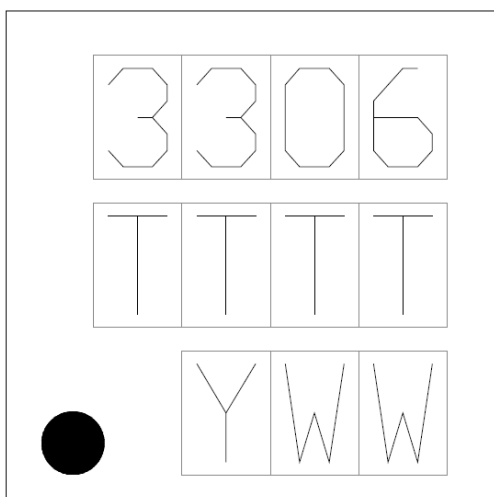


Figure 8.7. Si53306 Top Marking

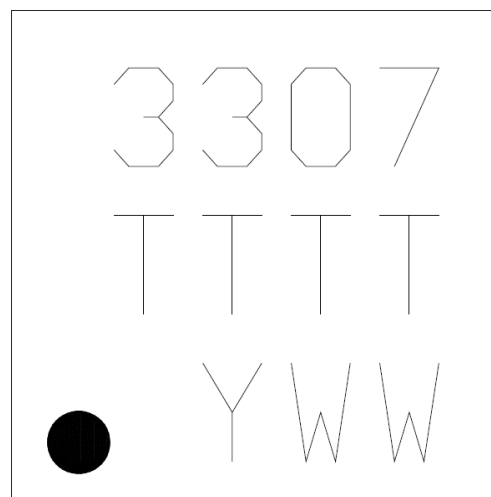


Figure 8.8. Si53307 Top Marking

Table 8.3. Si53306/07 Top Marking Explanation

| | | |
|------------------------|---|---|
| Mark Method: | Laser | |
| Font Size: | 0.635 mm (25 mils) Right-Justified | |
| Line 1 Marking: | Device Part Number | 3306 for Si53306-B-GM 3307 for Si53307-B-GM |
| Line 2 Marking: | TTTT = Mfg Code | Manufacturing Code from the Assembly Purchase Order form. |
| | YY = Year WW=Work Week | Assigned by Assembly Supplier. Corresponds to the year and work week of the mold date. |
| Line 3 Marking: | Circle=0.5 mm Diameter (Bottom-Left Justified) | Pin 1 Identifier |
| | YWW = Date Code | Corresponds to the last digit of the current year (Y) and the workweek (WW) of the mold date. |

9. Revision History

Revision 1.0

April, 2019

Initial release.



ClockBuilder Pro

One-click access to Timing tools, documentation, software, source code libraries & more. Available for Windows and iOS (CBGo only).

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