THE DATASHEET OF

SI4322-A0-FTR

Si4322 Universal ISM Band FSK Receiver

Si4322

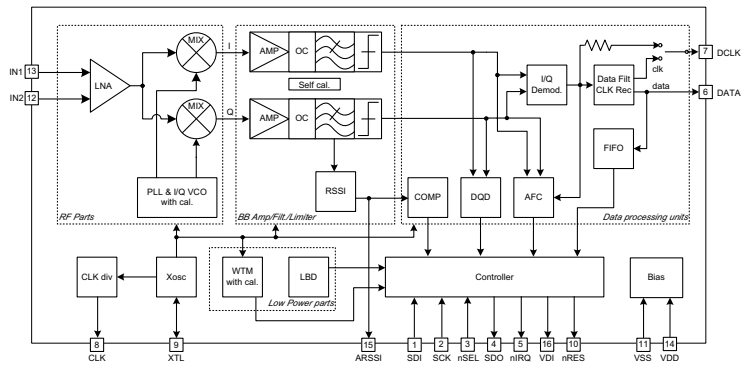
DESCRIPTION

Silicon Labs's Si4322 is a single chip, low power, multi-channel FSK receiver designed for use in applications requiring FCC or ETSI conformance for unlicensed use in the 868 and 915 MHz bands. Used in conjunction with Silicon Labs' FSK transmitters, the Si4322 is a flexible, low cost, and highly integrated solution that does not require production alignments. All required RF functions are integrated. Only an external crystal and bypass filtering is needed for operation.

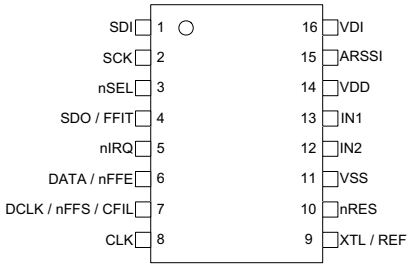
The Si4322 has a completely integrated PLL for easy RF design, and its rapid settling time allows for fast frequency hopping, bypassing multipath fading, and interference to achieve robust wireless links. The PLL's high resolution allows the usage of multiple channels in any of the bands. The baseband bandwidth (BW) is programmable to accommodate various deviation, data rate, and crystal tolerance requirements. The receiver employs the Zero-IF approach with I/Q demodulation, therefore no external components (except crystal and decoupling) are needed in a typical application. The Si4322 is a complete analog RF and baseband receiver including a multi-band PLL synthesizer with an LNA, I/Q down converter mixers, baseband filters and amplifiers, and I/Q demodulator.

The chip dramatically reduces the load on the microcontroller with integrated digital data processing: data filtering, clock recovery, data pattern recognition and integrated FIFO. The automatic frequency control (AFC) feature allows using a low accuracy (low cost) crystal. To minimize the system cost, the chip can provide a clock signal for the microcontroller, avoiding the need for two crystals.

FUNCTIONAL BLOCK DIAGRAM



PIN ASSIGNMENT



This document refers to Si4322-IC Rev A0.
See www.silabs.com/integration for any applicable errata. See back page for ordering information.

FEATURES

- Fully integrated (low BOM, easy design-in)
- No alignment required in production
- Fast settling, programmable, high-resolution PLL
- Fast frequency hopping capability
- High bit rate (up to 115.2 kbps in digital mode and 256 kbps in analog mode)
- Direct differential antenna input
- Programmable baseband bandwidth (134 to 400 kHz)
- Analog and digital RSSI outputs
- Automatic frequency control (AFC)
- Data quality detection (DQD)
- Internal data filtering and clock recovery
- RX pattern recognition
- SPI compatible serial control interface
- Clock and reset signals for microcontroller
- 48 bit RX data FIFO
- Standard 10 MHz crystal reference
- Wake-up timer
- Low battery detector
- 2.2 to 3.8 V supply voltage
- Low power consumption
- Low standby current (typ. 0.3 µA)

TYPICAL APPLICATIONS

- Remote control
- Home security and alarm
- Wireless keyboard/mouse and other PC peripherals
- Toy control
- Remote keyless entry
- Tire pressure monitoring
- Telemetry
- Personal/patient data logging
- Remote automatic meter reading

DETAILED DESCRIPTION

General

The Si4322 FSK receiver is the counterpart of the Silicon Labs' FSK transmitter. It covers the unlicensed frequency bands at 868 and 915 MHz. The device facilitates compliance with FCC and ETSI requirements.

The programmable PLL synthesizer determines the operating frequency, while preserving accuracy based on the on-chip crystal-controlled reference oscillator. The PLL's high resolution allows for the use of multiple channels in any of the bands.

The receiver employs the Zero-IF approach with I/Q demodulation, allowing the use of a minimal number of external components in a typical application. The Si4322 consists of a fully integrated multi-band PLL synthesizer, an LNA with switchable gain, I/Q down converter mixers, baseband filters and amplifiers, and an I/Q demodulator followed by a data filter.

LNA

The LNA has 250 Ohm input impedance, which works well with the recommended antennas. (See Application Notes available from www.silabs.com/integration.)

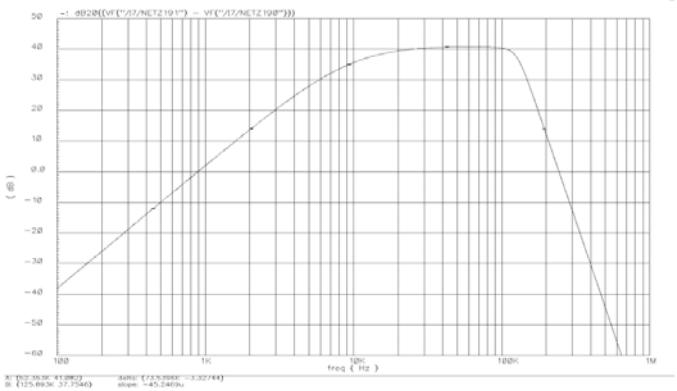
If the RF input of the chip is connected to 50 Ohm devices, an external matching circuit is required to provide the correct matching and to minimize the noise figure of the receiver.

The LNA gain (and linearity) can be selected (0, –6, –12, –18 dB relative to the highest gain) according to RF signal strength. This is useful in an environment with strong interferers.

Baseband Filters

The receiver bandwidth is selectable by programming the bandwidth (BW) of the baseband filters. This allows setting up the receiver according to the characteristics of the signal to be received.

An appropriate bandwidth can be selected to accommodate various FSK deviation, data rate, and crystal tolerance requirements. The filter structure is a 7-th order Butterworth low-pass with 40 dB suppression at 2*BW frequency. Offset cancellation is accomplished by using a high-pass filter with a cut-off frequency below 15 kHz.



Data Filtering and Clock Recovery

The output data filtering can be completed by an external capacitor or by using digital filtering according to the final application.

Analog operation: The filter is an RC type low-pass filter and a Schmitt-trigger (St). The resistor (10k) and the St is integrated on the chip. An (external) capacitor can be chosen according to the actual bit-rate. In this mode the receiver can handle up to 256 kbps data rate.

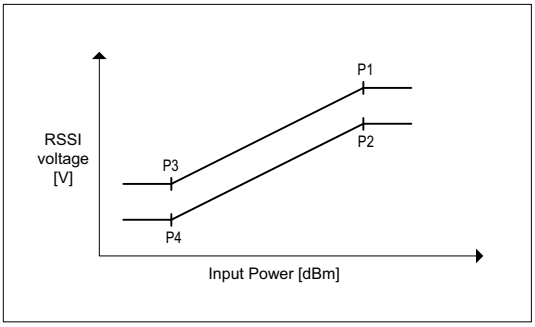
Digital operation: The data filter is a digital realization of an analog RC filter followed by a comparator with hysteresis. In this mode there is a clock recovery circuit (CR), which can provide synchronized clock to the data. With this clock the received data can fill the RX Data FIFO. The CR has three operation modes: fast, slow, and automatic. In slow mode, its noise immunity is very high, but it has slower settling time and requires more accurate data timing than in fast mode. In automatic mode the CR automatically changes between fast and slow modes. The CR starts in fast mode, then automatically switches to slow mode after locking.

(Only the data filter and the clock recovery use the bit-rate clock. Therefore, in analog mode, there is no need for setting the correct bit-rate.)

Data Validity Blocks

RSSI

A digital RSSI output is provided to monitor the input signal level. It goes high if the received signal strength exceeds a given preprogrammed level. An analog RSSI signal is also available. The RSSI settling time depends on the filter capacitor used.



Voltage on ARRSI pin vs. Input RF power

P1	-65 dBm	1300 mV
P2	-65 dBm	1000 mV
P3	-100 dBm	600 mV
P4	-100 dBm	300 mV

DQD

The Data Quality Detector monitors the I/Q output of the baseband amplifier chain by counting the consecutive correct 0->1, 1->0 transitions. The DQD output indicates the quality of the signal to be demodulated. Using this method it is possible to "forecast" the probability of BER degradation. The programmable DQD parameter defines the threshold for signaling the good/bad data quality by the digital one-bit DQD output. In cases when the deviation is close to the bitrate, there should be four transitions during a single one bit period in the I/Q signals. As the bitrate decreases in comparison to the deviation, more and more transitions will happen during a bitperiod.

AFC

By using an integrated Automatic Frequency Control (AFC) feature, the receiver can synchronize its local oscillator to the received signal, allowing the use of:

- inexpensive, low accuracy crystals
- narrower receiver bandwidth (i.e. increased sensitivity)
- higher data rate

Crystal Oscillator and Microcontroller Clock Output

The chip has a single-pin crystal oscillator circuit, which provides a 10 MHz reference signal for the PLL. To reduce external parts and simplify design, the crystal load capacitor is internal and programmable. Guidelines for selecting the appropriate crystal can be found later in this datasheet. The receiver can supply the clock signal for the microcontroller, so accurate timing is possible without the need for a second crystal. In normal operation it is divided from the reference 10 MHz. During sleep mode a low frequency (typical 32 kHz) output clock signal can be switched on.

When the microcontroller turns the crystal oscillator off by clearing the appropriate bit using the *Configuration Setting Command,* the chip provides a programmable number (default is 128) of further clock pulses (“clock tail”) for the microcontroller to let it go to idle or sleep mode.

Low Battery Voltage Detector

The low battery detector circuit monitors periodically (typ. 8 ms) the supply voltage and generates an interrupt if it falls below a programmable threshold level.

Wake-Up Timer

The wake-up timer has very low current consumption (4 µA max) and can be programmed from 1 ms to several hours.

It calibrates itself to the crystal oscillator at every startup and then at every 30 seconds with an accuracy of ±0.5%. When the crystal oscillator is switched off, the calibration circuit switches it back on only long enough for a quick calibration (a few milliseconds) to facilitate accurate wake-up timing. The periodic autocalibration feature can be turned off.

Event Handling

In order to minimize current consumption, the receiver supports the sleep mode. Active mode can be initiated by setting the *ex* or *en* bits (in the *Configuration Setting* or *Receiver Setting Command*).

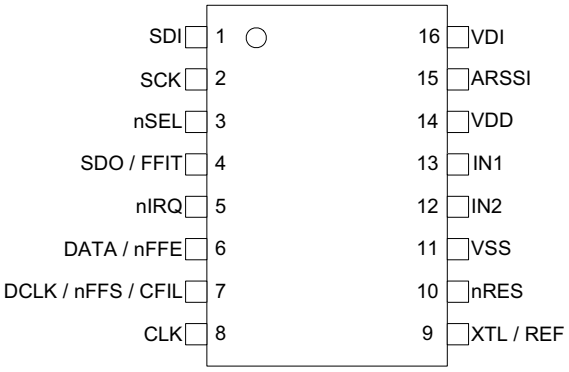
Si4322 generates an interrupt signal on several events (wake-up timer timeout, low supply voltage detection, on-chip FIFO filled up). This signal can be used to wake up the microcontroller, effectively reducing the period the microcontroller has to be active. The cause of the interrupt can be read out from the receiver by the microcontroller through the SDO pin.

Interface and Controller

An SPI compatible serial interface lets the user select the frequency band, center frequency of the synthesizer, and the bandwidth of the baseband signal path. Division ratio for the microcontroller clock, wake-up timer period, and low supply voltage detector threshold are also programmable. Any of these auxiliary functions can be disabled when not needed. All parameters are set to default after power-on; the programmed values are retained during sleep mode. The interface supports the read-out of a status register, providing detailed information about the status of the receiver and the received data. It is also possible to store the received data bits into the 48 bit RX FIFO register and read them out in a buffered mode. FIFO mode can be enabled through the SPI compatible interface by setting the *fe* bit to 1 in the *Output and FIFO Mode Command.* During FIFO read the crystal oscillator must be ON.

PIN DEFINITIONS

Pin type key: D=digital, A=analog, S=supply, I=input, O=output, IO=input/output



Pin	Name	Function	Type	Description
1	SDI	SDI	DI	Data input of serial control interface
2	SCK	SCK	DI	Clock input of serial control interface
3	nSEL	nSEL	DI	Chip select input of serial control interface (active low)
4	SDO / FFIT	SDO	DO	Serial data out for Status Read Command. Tristate with bushold cell if nSEL= H
		FFIT	DO	FIFO IT (active low)
5	nIRQ	nIRQ	DO	Interrupt request output (active low)
6	DATA / nFFS	DATA	DO	Received data output (FIFO not used)
		nFFS	DI	FIFO select input
7	DCLK	DCLK	DO	Received data clock output (digital filter used, FIFO not used)
		FFIT	DO	FIFO IT (active high) FIFO empty function can be achieved when FIFO IT level is set to1
		CFIL	AIO	External data filter capacitor connection (analog filter used)
8	CLK	CLK	DO	Clock output for the microcontroller
9	XTL / REF	XTL	AIO	Crystal connection (other terminal of crystal to VSS)
		REF	DI	External reference input
10	nRES	nRES	DO	Reset output (active low)
11	VSS	VSS	S	Negative supply voltage
12	IN2	IN2	AI	RF differential signal input
13	IN1	IN1	AI	RF differential signal input
14	VDD	VDD	S	Positive supply voltage
15	ARSSI	ARSSI	AO	Analog RSSI output
16	VDI	VDI	DO	Valid Data Indicator output

GENERAL DEVICE SPECIFICATION

All voltages are referenced to V_{ss}, the potential on the ground reference pin VSS.

Absolute Maximum Ratings (non-operating)

Symbol	Parameter	Min	Max	Units
V_{dd}	Positive supply voltage	-0.5	6.0	V
V_{in}	Voltage on any pin	-0.5	V_{dd}+0.5	V
I_{in}	Input current into any pin except VDD and VSS	-25	25	mA
ESD	Electrostatic discharge with human body model		1000	V
T_{st}	Storage temperature	-55	125	°C
T_{ld}	Lead temperature (soldering, max 10 s)		260	°C

Recommended Operating Range

ELECTRICAL SPECIFICATION

(Min/max values are valid over the whole recommended operating range, typ conditions: T_{op} = 27 °C; V_{dd} = 2.7 V)

DC Characteristics

Symbol	Parameter
T_{op}	Ambient operating temperature

Symbol	Parameter	Conditions/Notes	Min	Typ	Max	Units
I_{dd}	Supply current	868 MHz band 915 MHz band		10.5 12	12.5 14	mA
I_{pd}	Standby current	all blocks disabled		1		µA
I_{lb}	Low battery voltage detector and wake-up timer current				5	µA
I_x	Idle current	crystal oscillator is ON		0.5		mA
V_{lb}	Low battery detection threshold	programmable in 0.1 V steps	2.0		3.5	V
V_{lba}	Low battery detection accuracy			± 0.05		V
V_{POR}	V_{dd} threshold required to generate a POR			1.5		V
$V_{POR,hyst}$	POR hysteresis	larger glithches on the V_{dd} generate a POR even above the threshold V_{POR}			0.6	V
SR_{Vdd}	V_{dd} slew rate	for proper POR generation	0.1			V/ms
V_{il}	Digital input low level				0.3*V_{dd}	V
V_{ih}	Digital input high level		0.7*V_{dd}			V
I_{il}	Digital input current	V_{il} = 0 V	-1		1	µA
I_{ih}	Digital input current	V_{ih} = V_{dd}, V_{dd} = 3.8 V	-1		1	µA
V_{ol}	Digital output low level	I_{ol} = 2 mA			0.4	V
V_{oh}	Digital output high level	I_{oh} = -2 mA	V_{dd}-0.4			V

AC Characteristics

Symbol	Parameter	Conditions/Notes	Min	Typ	Max	Units
f_{LO}	Receiver frequency	868 MHz band, 20 kHz resolution 915 MHz band, 20 kHz resolution	801.92 881.92		878.06 958.06	MHz
BW	Receiver bandwidth	mode 1 mode 2 mode 3 mode 4 mode 5	120 180 240 300 360	134 200 270 350 400	150 225 300 375 450	kHz
BR	FSK bit rate	with internal digital filters			115.2	kbps
BRA	FSK bit rate	with analog filter			256	kbps
P_{min}	Receiver sensitivity	BER 10^{-3}, BW = 134 kHz, BR = 9.6 kbps		-104		dBm
AFC_{range}	AFC locking range	δf_{FSK}: FSK deviation in the received signal		$0.8*\delta f_{FSK}$		
$IIP3_{inh}$	Input IP3	in band interferers		-21		dBm
$IIP3_{outh}$	Input IP3	out of band interferers $f\text{-}f_{LO} > 4MHz$		-18		dBm
CCR	Co-channel rejection	BER = 10^{-2} with continuous wave interferer in the channel		-4		dB
BR_{1MHz}	Blocking ratio	BER = 10^{-2} with continuous wave interferer, BW = 134 kHz, BR = 9.6 kbps, δf_{FSK} = 80 kHz, interferer offset 1 MHz		46		dB
BR_{2MHz}	Blocking ratio	same as above, interferer offset 2 MHz		49		dB
BR_{5MHz}	Blocking ratio	same as above, interferer offset 5 MHz		55		dB
BR_{10MHz}	Blocking ratio	same as above, interferer offset 10 MHz		67		dB
P_{max}	Maximum input power	LNA: high gain	0			dBm
Rin	RF input impedance real part (differential) (Note 1)	LNA gain (0, -12dB) LNA gain (-6, -18dB)		250 500		Ohm
Cin	RF input capacitance			1		pF
RS_a	RSSI accuracy			+/-5		dB
RS_r	RSSI range			46		dB
C_{ARSSI}	Filter capacitance for ARSSI		1			nF
RS_{step}	RSSI programmable level steps			6		dB
RS_{resp}	DRSSI response time	until the RSSI output goes high after the input signal exceeds the pre-programmed limit, C_{ARRSI} = 5nF		500		µs

Note 1: See matching circuit parameters and antenna design guide for information, and Application Notes available from http://www.silabs.com.

AC Characteristics (continued)

Symbol	Parameter	Conditions/Notes	Min	Typ	Max	Units
f_{ref}	PLL reference frequency	(Note 2)	9	10	11	MHz
f_{res}	PLL frequency resolution			20		kHz
t_{lock}	PLL lock time	Frequency error < 1kHz after 1 MHz step		30		µs
$t_{st1, P}$	PLL startup time	Initial calibration after power-up with running crystal oscillator			500	µs
$t_{st2, P}$	PLL startup time	Recalibration after receiver chain enable with running crystal oscillator			60	µs
C_{xl}	Crystal load capacitance, see crystal selection guide	Programmable in 0.5 pF steps, tolerance +/- 10%	8.5		16	pF
t_{POR}	Internal POR pulse width (Note 3)	After V_{dd} has reached 90% of final value		50	100	ms
t_{sx}	Crystal oscillator startup time	Crystal ESR < 100 Ω			5	ms
t_{PBt}	Wake-up timer clock period	Calibrated every 30 seconds (Note 4)	0.995	1	1.005	ms
$t_{wake-up}$	Programmable wake-up time		1		$8.4*10^6$	ms
$C_{in, D}$	Digital input capacitance				2	pF
$t_{r, f}$	Digital output rise/fall time	15 pF pure capacitive load			10	ns
$t_{r, f, ckout}$	Clock output rise/fall time	10 pF pure capacitive load			15	ns
$f_{ckout, slow}$	Slow clock frequency	Tolerance +/- 1 kHz		32		kHz

Note 2: Using other than a 10 MHz crystal is not recommended because the crystal referred timing and frequency parameters will change accordingly.

Note 3: During this period, commands are not accepted by the chip.

Note 4: Autocalibration can be turned off.

CONTROL INTERFACE

Commands to the receiver are sent serially. Data bits on pin SDI are shifted into the device upon the rising edge of the clock on pin SCK whenever the chip select pin nSEL is low. When the nSEL signal is high, it initializes the serial interface. The number of bits sent is an integer multiple of 8. All commands consist of a command code, followed by a varying number of parameter or data bits. All data are sent MSB first (e.g. bit 15 for a 16-bit command). Bits having no influence (don't care) are indicated with X. The Power On Reset (POR) circuit sets default values in all control registers.

The receiver will generate an interrupt request (IRQ) for the microcontroller on the following events:

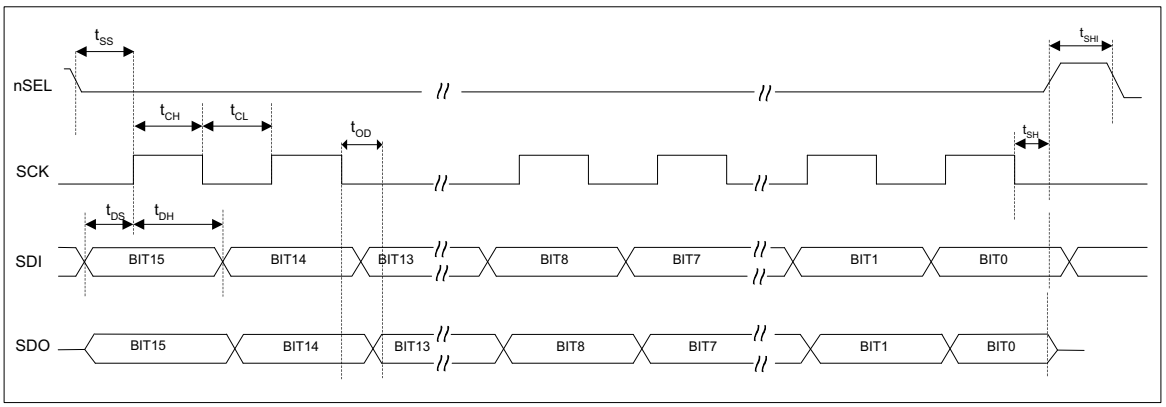
- Supply voltage below the preprogrammed value is detected (LBD)
- Wake-up timer timeout (WK-UP)
- FIFO received the preprogrammed amount of bits (FFIT)
- FIFO overflow (FFOV)

FFIT and FFOV are applicable only when the FIFO is enabled. To find out why the nIRQ was issued, the status bits should be read out.

Timing Specification

Symbol	Parameter	Minimum value [ns]
t_{CH}	Clock high time	25
t_{CL}	Clock low time	25
t_{SS}	Select setup time (nSEL falling edge to SCK rising edge)	10
t_{SH}	Select hold time (SCK falling edge to nSEL rising edge)	10
t_{SHI}	Select high time	25
t_{DS}	Data setup time (SDI transition to SCK rising edge)	5
t_{DH}	Data hold time (SCK rising edge to SDI transition)	5
t_{OD}	Data delay time	10

Timing Diagram



Control Commands

Control Word	Related Parameters/Functions
Configuration Setting Command	frequency band, crystal oscillator load capacitance, baseband filter bandwidth, etc.
Frequency Setting Command	frequency of the local oscillator
Receiver Setting Command	VDI source, LNA gain, RSSI threshold
Wake-up Timer Command	wake-up time period
Extended Wake-up Timer Command	wake-up time period finer adjustment
Low Battery Detector and Clock Divider Command	LBD voltage and microcontroller clock division ratio
AFC Control Command	AFC parameters
Data Rate Command	bit rate
Data Filter Command	data filter type, clock recovery parameters, POR level selection, autosleep mode
Output and FIFO Command	FIFO IT level, FIFO start control, FIFO enable and FIFO fill enable
Extended Features Command	low frequency output clock, wake-up timer extra functions, long FIFO extra funcions
Status Read Command	receiver status read

Note: In the following tables the POR column shows the default values of the command registers after power-on.

Configuration Setting Command

bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	POR
	1	0	0	1	bs	eb	et	ex	x3	x2	x1	x0	i2	i1	i0	dc	938Ah

bs	Frequency Band [MHz]
0	868
1	915

i2	i1	i0	Baseband Bandwidth [kHz]
0	0	0	reserved
0	0	1	400
0	1	0	340
0	1	1	270
1	0	0	200
1	0	1	134
1	1	0	reserved
1	1	1	reserved

x3	x2	x1	x0	Crystal Load Capacitance [pF]
0	0	0	0	8.5
0	0	0	1	9.0
0	0	1	0	9.5
0	0	1	1	10.0
.....				....
1	1	1	0	15.5
1	1	1	1	16.0

Bits *eb* and *et* control the operation of the low battery detector and wake-up timer, respectively. They are enabled when the corresponding bit is set.

If *ex* is set the crystal is active during non-active mode.
When *dc* bit is set it disables the clock output

Frequency Setting Command

bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	POR
	1	0	1	0	f11	f10	f9	f8	f7	f6	f5	f4	f3	f2	f1	f0	AD57h

The 12-bit *Frequency Setting Command <f11 : f0>* has the value F. The value F should be in the range of 96 and 3903. When F is out of range, the previous value is kept. The synthesizer center frequency f_0 can be calculated as:

$f_0 = 8 * 10\ MHz * (C + F/4000)$

The constant C is determined by the selected band as:

Band [MHz]	C
868	10
915	11

Receiver Setting Command

bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	POR
	1	1	0	0	0	0	0	0	d1	d0	g1	g0	r2	r1	r0	en	C080h

Bit 7-6 <*d1:d0*>: Select the VDI (valid data indicator) signal:

d1	d0	VDI output
0	0	Digital RSSI Out (DRSSI)
0	1	Data Quality Detector Output (DQD)
1	0	Clock recovery lock
1	1	Always

Bit 5-4 <*g1:g0*>: Set the LNA gain:

g1	g0	G_{LNA} (dB relative to max. G)
0	0	0
0	1	-6
1	0	-12
1	1	-18

Bit 3-1 <*r2:r0*>: Control the threshold of the RSSI detector:

r2	r1	r0	RSSIsetth [dBm]
0	0	0	-103
0	0	1	-97
0	1	0	-91
0	1	1	-85
1	0	0	-79
1	0	1	-73
1	1	0	-67
1	1	1	-61

The RSSI threshold depends on the LNA gain, the real RSSI threshold can be calculated:

$$RSSI_{th} = RSSI_{setth} + G_{LNA}$$

Bit 0 <*en*>: Enables the whole receiver chain and crystal ocsillator when set. Enable/disable of the wake-up timer and the low battery detector are not affected by this setting.

Wake-Up Timer Command

bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	POR
	1	1	1	0	r3	r2	r1	r0	m7	m6	m5	m4	m3	m2	m1	m0	E196h

The wake-up time period can be calculated by M <*m13* : *m0*> , R <*r3* : *r0*> and D <*d1* : *d0*>:

$$T_{wake\text{-}up} = M * 2^{R\text{-}D} \text{ ms}$$

Note: The wake-up timer generates interrupts continuously at the programmed interval while the *et* bit is set.

Extended Wake-Up Timer Command

bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	POR
	1	1	0	0	0	0	1	1	d1	d0	m13	m12	m11	m10	m9	m8	C300h

These bits can be used for further fine adjustment of the wake-up timer. The explanation of the bits can be found above.

Low Battery Detector and Microcontroller Clock Divider Command

bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	POR
	1	1	0	0	0	0	1	0	d2	d1	d0	elfc	t3	t2	t1	t0	C213h

The 4-bit value T of *t3-t0* determines the threshold voltage of the threshold voltage V_{lb} of the detector:

$$V_{lb} = 2.0 \text{ V} + T * 0.1 \text{ V}$$

Bit 4 <*elfc*>: Enables low frequency (32 kHz) microcontroller output clock during sleep mode.

Clock divider configuration (valid only if the crystal oscillator is on):

d2	d1	d0	Clock Output Frequency [MHz]
0	0	0	1
0	0	1	1.25
0	1	0	1.66
0	1	1	2
1	0	0	2.5
1	0	1	3.33
1	1	0	5
1	1	1	10

AFC Command

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	POR
	1	1	0	0	0	1	1	0	a1	a0	rl1	rl0	st	fi	oe	en	C687h

Bit 0 <*en*>*:* Enables the calculation of the offset frequency by the AFC circuit (it allows the addition of the content of the output register to the frequency control word of the PLL).

Bit 1 <*oe*>: Enables the output (frequency offset) register

Bit 2 <*fi*>: Switches the circuit to high accuracy (fine) mode. In this case the processing time is about four times longer, but the measurement uncertainty is less than half.

Bit 3 <*st*>*:* Strobe edge. When *st* goes to high, the actual latest calculated frequency error is stored into the output registers of the AFC block.

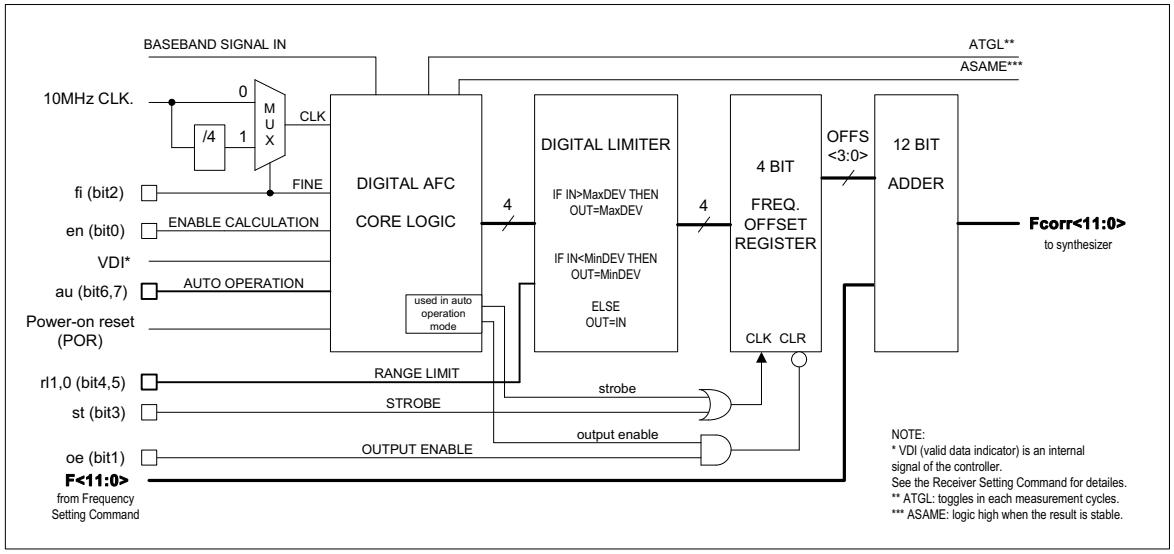
Bit 5-4 <*rl1:rl0*>: Limit the value of the frequency offset register to the following values:

rl1	rl0	Max dev [fres]
0	0	No restriction
0	1	± 4
1	0	± 2
1	1	± 1

fres:
868MHz band: 20 kHz
915MHz band: 20 kHz

Bit 7-6 <*a1:a0*>: Automatic operation mode selector:

a1	a0	
0	0	Auto mode off (Strobe is controlled by uC)
0	1	Runs only once after each power-up
1	0	Keep the f_{offset} only during receiving (VDI=high).
1	1	Keep the f_{offset} value



In automatic operation mode (no strobe signal is needed from the microcontroller to update the output offset register), the AFC circuit is automatically enabled when VDI indicates a potential incoming signal during the whole measurement cycle and the circuit measures the same result in two subsequent cycles.

There are three operation modes, example from the possible application:

1, (*a1*=0, *a0*=1) The circuit measures the frequency offset only once after power up. This way, the extended TX/RX maximum distance can be achieved. In the final application when the user is inserted the battery the circuit measures and compensate the frequency offset caused by the crystal tolerances. This method enables to use cheaper quartz in the application and provide quite good protection against locking in an interferer.

2a, (*a1*=1, *a0*=0) The circuit measures automatically the frequency offset during an initial low data rate pattern – easier to receive – (i.e 00110011) of the package and change the receiving frequency according that. The further part of the package can be received by the corrected frequency settings.

2b, (*a1*=1, *a0*=0) The transmitter must transmit the first part of the packet with a step higher deviation and later it is possible to reduce it.

In both cases (*2a* and *2b*) when the VDI indicates poor receiving conditions (VDI goes low) the output register is automatically cleared. It is suggested to use when one receiver receives signal from more than one transmitter.

3, (*a1*=1, *a0*=1) It is similar to the *2a* and *2b* modes, but 3 is suggested to use when a receiver operates with only one transmitter. After a complete measuring cycle, the measured value is held independently of the sate of VDI signal.

Data Filter Command

bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	POR
	1	1	0	0	0	1	0	0	al	ml	dsfi	sf	ewi	f2	f1	f0	C462h

Bit 7 <*al*>: Clock recovery (CR) auto lock control if set.
It means that the CR start in fast mode after locking it automatically switches to slow mode.

Bit 6 <*ml*>: Clock recovery lock control
1: fast mode, fast attack and fast release - 0: slow mode, slow attack and slow release
Using the slower one requires more accurate bit timing (see *Data Rate Command*).

Bit 5 <*dsfi*>: Disables autosleep on FIFO interrupt if set to 1.

Bit 4 <*sf*>: Selects the type of the data filter:

sf	Filter Type
0	Digital
1	Analog RC filter

Digital: this is a digital realization of an analog RC filter followed by a comparator with hysteresis. The time constant is automatically adjusted to the bit rate defined by the *Data Rate Command*.

Analog RC filter: the demodulator output is fed to the DCK pin over a 10 kOhm resistor. The filter characteristic is set by the external capacitor connected to this pin and VSS. (Suggested value for 9600 bps is 1.8 nF).

Bit 3 <*ewi*>: Enables the automatic wake-up on any interrupt event.

Bit 2-0 <*f0:f2*>: DQD threshold parameter.

Note: To let the DQD report "good signal quality" the threshold parameter should be less than 4 in the case when the bitrate is close to the deviation. At higher deviation/bitrate settings higher threshold parameter can report "good signal quality" as well.

Data Rate Command

bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	POR
	1	1	0	0	1	0	0	0	cs	r6	r5	r4	r3	r2	r1	r0	C813h

The expected bit rate of the received data stream is determined by the 7-bit value R (bits *r6* to *r0*) and the 1 bit *cs*.

BR = 10 MHz / 29 / (R+1) / (*1* + *cs**7)

In the receiver set R according the next function:

R= (10 MHz / 29 /(*1* + *cs**7)/ BR) – 1

Apart from setting custom values, the standard bit rates from 600 bps to 115.2 kbps can be approximated with small error.

Data rate accuracy requirements:

Clock recovery in slow mode: $\Delta BR/BR < 1/(29*N_{bit})$ Clock recovery in fast mode: $\Delta BR/BR < 3/(29*N_{bit})$

BR is the bit rate set in the receiver and ΔBR is bit rate difference between the transmitter and the receiver. N_{bit} is the maximal number of consecutive ones or zeros in the data stream. It is recommended for long data packets to include enough 1/0 and 0/1 transitions, and be careful to use the same division ratio in the receiver and in the transmitter.

ΔBR is a theoretical limit for the clock recovery circuit. Clock recovery will not work above this limit. The clock recovery circuit will always operate below this limit independently from process, temperature, or Vdd condition.

e.g. Supposing a maximum length of consecutive zeros or ones in the data stream is less than 5 bits, the necessary relative accuracy is 0.68% in slow mode and 2.1% in fast mode.

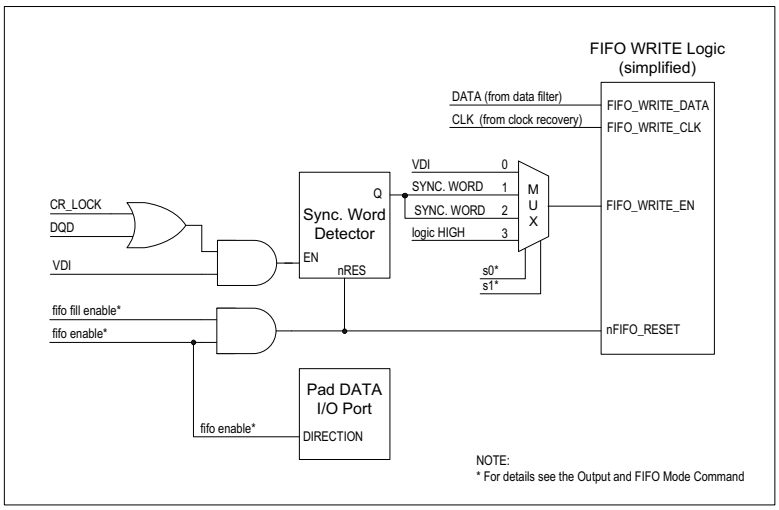
Output and FIFO Mode Command

bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	POR
	1	1	0	0	1	1	1	0	f3	f2	f1	f0	s1	s0	ff	fe	CE87h

Bit 7-4 <*f3* : *f0*>: FIFO IT level. The FIFO generates IT when number of the received data bits reaches this level.

Bit 3-2 <s*1* : s*0*>: Select the input of the FIFO fill start condition:

s1	s0	
0	0	VDI
0	1	Sync. Word
1	0	Sync. Word
1	1	Always



Note: VDI (Valid Data Indicator) see further details in *Receiver Control Word*, Synchron word in microcontroller mode is 2DD4h.

Bit 1 <*ff*>: Enables FIFO fill after synchron word reception. FIFO fill stops when this bit is cleared.

Bit 0 <*fe*>: Enables the 48 bit deep FIFO mode. To clear the counter of the FIFO, it has to be set to zero.

Note: To restart the synchron word reception, bit 1 should be cleared and set.

This action will initialize the FIFO and clear its content.

Bit 0 modifies the function of DATA pin and DCLK pin. The DATA pin will become input (nFFS) if *fe* is set to 1. If the chip is used in FIFO mode, do not allow this to be a floating input.

Extended Features Command:

bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	POR
	1	0	1	1	0	0	0	0	exlp	ctls	0	dcal	bw1	bw0	f5	f4	B0CAh

Bit 7 <*exlp*>: Enables low power mode for the crystal oscillator.

Bit 6 <*ctls*>: Clock tail selection bit. Setting this bit selects 512 bit long clock tail instead of the default 128 bit length.

Bit 4 <*dcal*>: Disables the wake-up timer autocalibration.

Bit 3-2 <*bw1:bw0*>: Select the bandwidth of the PLL.

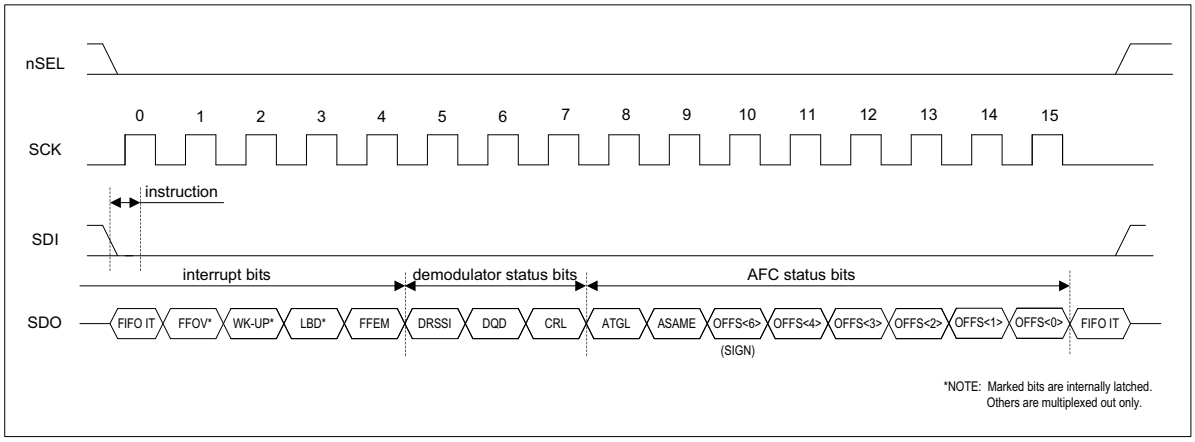
bw1	bw0	PLL bandwidth
0	0	15 kHz
0	1	30 kHz
1	0	60 kHz
1	1	120 kHz

Bit 1-0 <*f5:f4*>: Upper two bits for selecting the 48 bit FIFO IT level together with the *f3-f0* bits in the Output and FIFO Mode Command.

Status Read Command

The read command starts with a zero, whereas all other control commands start with a one. Therefore, after receiving the first bit of the control command the Si4322 identifies it as a read command. So as the first bit of the command is received, the receiver starts to clock out the status bits on the SDO output as follows:

Status Register Read Sequence with FIFO Read Example



Note: The FIFO IT bit behaves like a status bit, but generates nIRQ pulse if active. To check whether there is a sufficient amount of data in the FIFO, the SDO output can be tested. In extreme speed critical applications, it can be useful to read only the first four bits (*FIFO IT - LBD*) to clear the FFOV, WK-UP, and LBD bits. During the FIFO access the f_{SCK} cannot be higher than $f_{ref}/4$, where f_{ref} is the crystal oscillator frequency. If the FIFO is read in this mode the nFFS input must be connected to logic high level.

Definitions of the bits in the above timing diagram:

FFIT	The number of data bits in the FIFO has reached the preprogrammed limit
FFOV	FIFO overflow
WK-UP	Wake-up timer overflow
LBD	Low battery detect, the power supply voltage is below the preprogrammed limit
FFEM	FIFO is empty
DRSSI	The strength of the incoming signal is above the preprogrammed limit
DQD	Data Quality Detector detected a good quality signal
CRL	Clock recovery lock
ATGL	Toggling in each AFC cycle
ASAME	AFC measured twice the same result
OFFS(6)	MSB of the measured frequency offset (sign of the offset value)
OFFS(4) -OFFS(0)	Offset value to be added to the value of the selected center frequency

FIFO Buffered Data Read

In this operating mode, incoming data are clocked into a 48 bit FIFO buffer. The receiver starts to fill up the FIFO when the Valid Data Indicator (VDI) bit and/or the synchron word recognition circuit indicates potentially real incoming data. This prevents the FIFO from being filled with noise and overloading the external microcontroller.

For further details see the *Receiver Setting Command* and the *Output and FIFO Command*.

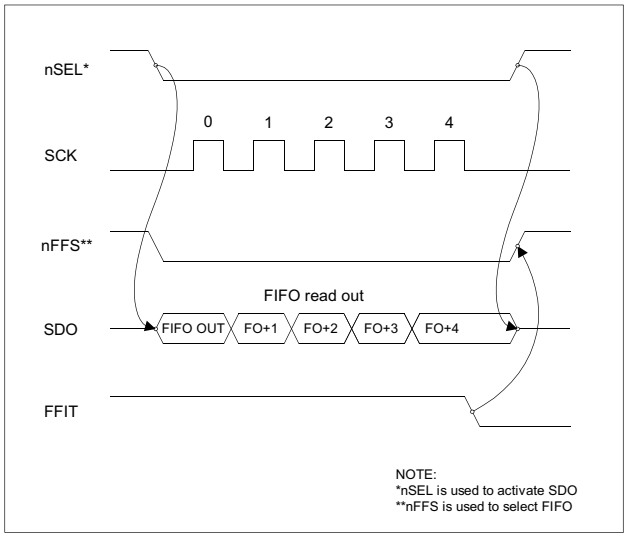
Polling Mode:

The nFFS signal selects the buffer directly and its content could be clocked out through pin SDO by SCK. Set the FIFO IT level to 1. In this case, as long as FFIT indicates received bits in the FIFO, the controller may continue to take the bits away. When FFIT goes low, no more bits need to be taken. An SPI read command is also available.

Interrupt Controlled Mode:

The user can define the FIFO level (the number of received bits) which will generate the nFFIT when exceeded. The status bits report the changed FIFO status in this case.

FIFO Read Example with FFIT Polling:



During FIFO access the f_{SCK} cannot be higher than f_{ref} /4, where f_{ref} is the crystal oscillator frequency.

Power Saving Modes

The different operating modes of the chip depend on the following control bits:

Operating Mode	eb or et *(Configuration Setting Comand)*	en *(Receiver Setting Command*	ex *(Configuration Setting Command)*
Active	X	1	1
Idle	X	0	1
Sleep	1	0	0
Standby	0	0	0

Dual Clock Output

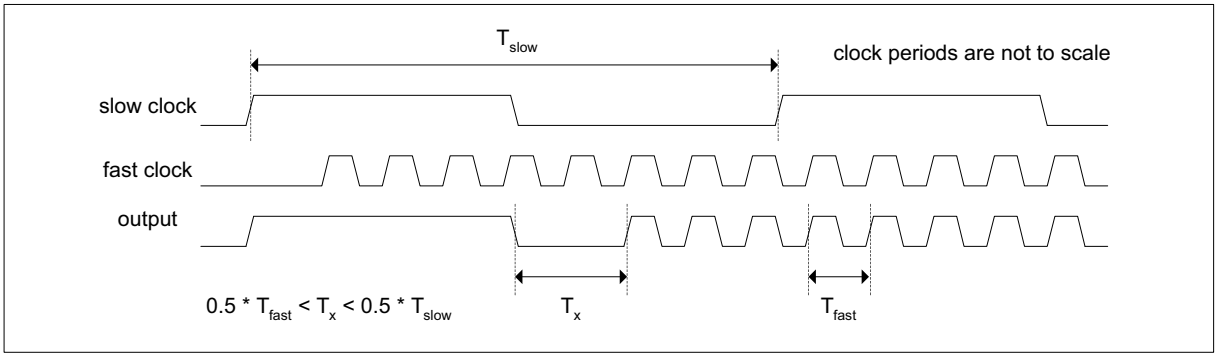
When the chip is switched into idle mode, the 10 MHz crystal oscillator starts. After oscillation ramp-up a 1 MHz clock signal is available on the CLK pin. This (fast) clock frequency can be reprogrammed during operation with the *Low Battery and Microcontroller Clock Divider Command* (page11). During startup and in sleep or standby mode (crystal oscillator disabled), the CLK output is pulled to logic low.

On the same pin a low frequency clock signal can be obtained if the *elfc* bit is set in the *Low Battery and Microcontroller Clock Divider Command*. The clock frequency is 32 kHz which is derived from the low-power RC oscillator of the wake-up timer. In order to use this slow clock the wake-up timer should be enabled by setting the *et* bit in the *Configuration Setting Command* (page 9) even if the wake-up timer itself is not used.

Slow clock feature can be enabled by entering into sleep mode (page 17). Driving the output will increase the sleep mode supply current. Actual worst-case value can be determined when the exact load and min/max operating conditions are defined. After power-on reset the chip goes into sleep mode and the slow frequency clock appears on the CLK pin.

Switching back into fast clock mode can be done by setting the *ex* or *en* bits in the approriate commands. It is important to leave bit *dc* in the *Configuration Setting Command* at its default state (0) otherwise there will be no clock signal on the CLK pin.

Switching between the fast and slow clock modes is glitch-free in a sense that either state of the clock lasts for at least a half cycle of the fast clock. During switching the clock can be logic low once for an intermediate period i.e. for any time between the half cycle of the fast and the slow clock.



The clock switching synchronization circuit detects the falling edges of the clocks. One consequence is a latency of 0 to $T_{slow} + T_{fast}$ from the occurrence of a clock change request (entering into sleep mode or interrupt) until the beginning of the intermediate length (T_x) half cycle. The other is that both clocks should be up and running for the change to occur. Changing from fast to slow clock, it is automatically ensured by entering into the sleep mode in the appropriate way provided that the wake-up timer is continouosly enabled. As the crystal oscillator is normally stopped while the slow clock is used, when changing back to fast clock the crystal oscillator startup time has to pass first before the above mentioned latency period starts. The startup condition is detected internally, so no software timing is necessary.

Wake-Up Timer Calibration

By default the wake-up timer is calibrated each time it is enabled by setting the *et* bit in the *Configuration Setting Command*. After timeout the timer restarts automatically and can be stopped by resetting the *et* bit. If the timer is programmed to run for longer periods, at app. every 30 seconds it performs additional self-calibration.

This feature can be disabled to avoid sudden changes in the actual wake-up time period. A suitable software algorithm can then compensate for the gradual shift caused by temperature change.

Bit *dcal* in the *Extended Features Command* (page 15) controls the automatic calibration feature. It is reset to 0 at power-on and the automatic calibration is enabled. This is necessary to compensate for process tolerances. After one calibration cycle further (re)calibration can be disabled by setting this bit to 1.

RX-TX ALIGNMENT PROCEDURES

RX-TX frequency offset can be caused only by the differences in the actual reference frequency. To minimize these errors it is suggested to use the same crystal type and the same PCB layout for the crystal placement on the RX and TX PCBs.

To verify the possible RX-TX offset it is suggested to measure the CLK output of both chips with a high level of accuracy. Do not measure the output at the XTL pin since the measurement process itself will change the reference frequency. Since the carrier frequencies are derived from the reference frequency, having identical reference frequencies and nominal frequency settings at the TX and RX side there should be no offset if the CLK signals have identical frequencies.

It is possible to monitor the actual RX-TX offset using the AFC status report included in the status byte of the receiver. By reading out the status byte from the receiver the actual measured offset frequency will be reported. In order to get accurate values the AFC has to be disabled during the read by clearing the "en" bit in the AFC Control Command (bit 0).

CRYSTAL SELECTION GUIDELINES

The crystal oscillator of the Si4322 requires a 10 MHz parallel mode crystal. The circuit contains an integrated load capacitor in order to minimize the external component count. The internal load capacitance value is programmable from 8.5 pF to 16 pF in 0.5 pF steps. With appropriate PCB layout, the total load capacitance value can be 10 pF to 20 pF so a variety of crystal types can be used.

When the total load capacitance is not more than 20 pF and a worst case 7 pF shunt capacitance (C_0) value is expected for the crystal, the oscillator is able to start up with any crystal having less than 300 ohms ESR (equivalent series loss resistance). However, lower C_0 and ESR values guarantee faster oscillator startup.

The crystal frequency is used as the reference of the PLL, which generates the local oscillator frequency (f_{LO}). Therefore f_{LO} is directly proportional to the crystal frequency. The accuracy requirements for production tolerance, temperature drift and aging can thus be determined from the maximum allowable local oscillator frequency error.

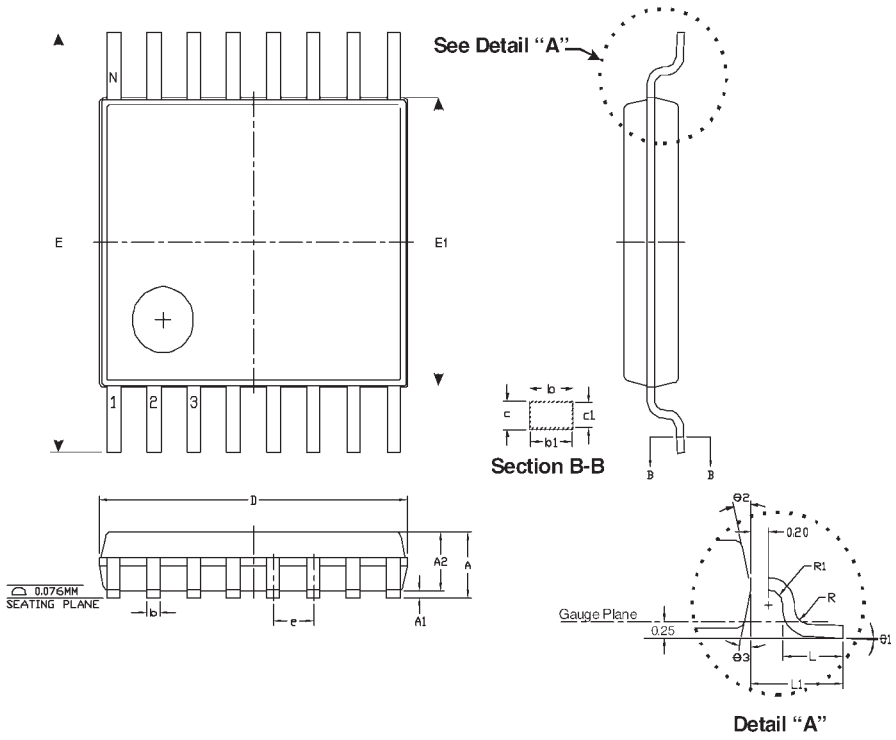
Whenever a low frequency error is essential for the application, it is possible to “pull” the crystal to the accurate frequency by changing the load capacitor value. The widest pulling range can be achieved if the nominal required load capacitance of the crystal is in the “midrange”, for example 16 pF. The “pull-ability” of the crystal is defined by its motional capacitance and C_0.

The on chip AFC is capable to correct TX/RX carrier offsets as much as 80% of the deviation of the received FSK modulated signal.

Note: There may be other requirements for the TX carrier accuracy with regards to the requirements as defined by standards and/or channel separations.

PACKAGE INFORMATION

16-pin TSSOP



Symbol	Dimensions in mm			Dimensions in Inches		
	Min.	Nom.	Max.	Min.	Nom.	Max.
A			1,20			0,047
A1	0,05		0,15	0,002		0,006
A2	0,80	0,90	1,05	0,031	0,035	0,041
b	0,19		0,30	0,007		0,012
b1	0,19	0,22	0,25	0,007	0,009	0,010
c	0,09		0,20	0,004		0,008
c1	0,09		0,16	0,004		0,006
D	4,90	5,00	5,10	0,193	0,197	0,201
e		0.65 BSC.			0.026 BSC.	
E		6.40 BSC.			0.252 BSC.	
E1	4,30	4,40	4,50	0,169	0,173	0,177
L	0,50	0,60	0,75	0,020	0,024	0,030
L1		1.00 REF.			0.39 REF.	
R	0,09			0,004		
R1	0,09			0,004		
θ1	0		8	0		8
θ2		12 REF.			12 REF.	
θ3		12 REF.			12 REF.	

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ORDERING INFORMATION

Si4322 Universal ISM Band FSK Receiver

DESCRIPTION	ORDERING NUMBER
Si4322 16-pin TSSOP	Si4322-IC CC16 Rev A0
die	see Silicon Labs

Demo Boards and Development Kits

DESCRIPTION	ORDERING NUMBER
ISM Chipset Development Kit	IA ISM – DK3

Related Resources

DESCRIPTION	ORDERING NUMBER
Antenna Selection Guide	IA ISM – AN1
Antenna Development Guide	IA ISM – AN2
Si4222 Universal ISM Band FSK Transmitter	see http://www.silabs.com/integration for details

Note: Volume orders must include chip revision to be accepted.

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