



**THE DATASHEET OF
SGA-5263**

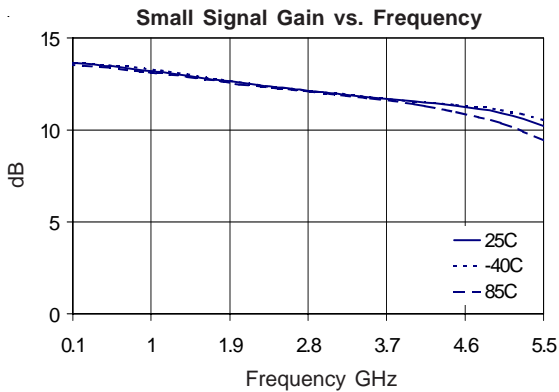




Product Description

The SGA-5263 is a high performance SiGe HBT MMIC Amplifier. A Darlington configuration featuring 1 micron emitters provides high F_T and excellent thermal performance. The heterojunction increases breakdown voltage and minimizes leakage current between junctions. Cancellation of emitter junction non-linearities results in higher suppression of intermodulation products. Only 2 DC-blocking capacitors, a bias resistor and an optional RF choke are required for operation.

The matte tin finish on Sirenza's lead-free package utilizes a post annealing process to mitigate tin whisker formation and is RoHS compliant per EU Directive 2002/95. This package is also manufactured with green molding compounds that contain no antimony trioxide nor halogenated fire retardants.



SGA-5263

SGA-5263Z



DC-4500 MHz, Silicon Germanium Cascadeable Gain Block



Product Features

- Now available in Lead Free, RoHS Compliant, & Green Packaging
- DC-4500 MHz Operation
- Single Voltage Supply
- Low Current Draw: 60mA at 3.4V typ.
- High Output Intercept: 29 dBm typ. at 1950MHz

Applications

- Oscillator Amplifiers
- Broadband Gain Blocks
- IF/RF Buffer Amplifiers

Symbol	Parameters: Test Conditions: $Z_0 = 50 \text{ Ohms}$, $I_D = 60 \text{ mA}$, $T = 25^\circ\text{C}$		Units	Min.	Typ.	Max.
P_{1dB}	Output Power at 1dB Compression	f = 850 MHz f = 1950 MHz f = 2400 MHz	dBm dBm dBm		16.3 15.0 14.0	
IP_3	Third Order Intercept Point Power out per tone = -10 dBm	f = 850 MHz f = 1950 MHz f = 2400 MHz	dBm dBm dBm		32.5 29.3 27.3	
S_{21}	Small Signal Gain	f = 850 MHz f = 1950 MHz f = 2400 MHz	dB dB dB		13.3 12.6 12.3	
Bandwidth	S_{11} , S_{22} : Minimum 10db Return Loss (typ.)		MHz		4500	
S_{11}	Input VSWR	f = 1950 MHz	-		1.2:1	
S_{22}	Output VSWR	f = 1950 MHz	-		1.4:1	
S_{12}	Reverse Isolation	f = 850 MHz f = 1950 MHz f = 2400 MHz	dB dB dB		18.3 19.2 19.5	
NF	Noise Figure	f = 1950 MHz	dB		4.0	
V_D	Device Operating Voltage		V		3.4	
I_D	Device Operating Current		mA	54	60	66
$R_{th, j-l}$	Thermal Resistance (junction - lead)		$^\circ\text{C/W}$		255	

The information provided herein is believed to be reliable at press time. Sirenza Microdevices assumes no responsibility for inaccuracies or omissions. Sirenza Microdevices assumes no responsibility for the use of this information, and all such information shall be entirely at the user's own risk. Prices and specifications are subject to change without notice. No patent rights or licenses to any of the circuits described herein are implied or granted to any third party. Sirenza Microdevices does not authorize or warrant any Sirenza Microdevices product for use in life-support devices and/or systems. Copyright 2001 Sirenza Microdevices, Inc.. All worldwide rights reserved.

Parameter	Typical 25°C	Unit	Test Condition ($I_D = 60\text{mA}$, unless otherwise noted)
100 MHz Gain Output IP3 Output P1dB Input Return Loss Reverse Isolation Noise Figure	13.6 33.6 16.1 26.0 17.7 3.9	dB dBm dBm dB dB dB	Tone spacing = 1 MHz, Pout per tone = -10dBm $Z_s = 50\text{ Ohms}$
500 MHz Gain Output IP3 Output P1dB Input Return Loss Reverse Isolation Noise Figure	13.5 33.0 16.4 23.5 18.0 3.9	dB dBm dBm dB dB dB	Tone spacing = 1 MHz, Pout per tone = -10dBm $Z_s = 50\text{ Ohms}$
850 MHz Gain Output IP3 Output P1dB Input Return Loss Reverse Isolation Noise Figure	13.3 32.5 16.3 21.4 18.3 4.0	dB dBm dBm dB dB dB	Tone spacing = 1 MHz, Pout per tone = -10dBm $Z_s = 50\text{ Ohms}$
1950 MHz Gain Output IP3 Output P1dB Input Return Loss Reverse Isolation Noise Figure	12.6 29.3 15.0 20.2 19.2 4.0	dB dBm dBm dB dB dB	Tone spacing = 1 MHz, Pout per tone = -10dBm $Z_s = 50\text{ Ohms}$
2400 MHz Gain Output IP3 Output P1dB Input Return Loss Reverse Isolation	12.3 27.3 14.0 23.0 19.5	dB dBm dBm dB dB	Tone spacing = 1 MHz, Pout per tone = -10dBm
3500 MHz Gain Output IP3 Output P1dB Input Return Loss Reverse Isolation	11.8 23.1 11.6 24.6 19.6	dB dBm dBm dB dB	Tone spacing = 1 MHz, Pout per tone = -10dBm

Absolute Maximum Ratings

Parameter	Absolute Limit
Max. Device Current (I_D)	120 mA
Max. Device Voltage (V_D)	6 V
Max. RF Input Power	+16 dBm
Max. Junction Temp. (T_J)	+150°C
Operating Temp. Range (T_L)	-40°C to +85°C
Max. Storage Temp.	+150°C

Operation of this device beyond any one of these limits may cause permanent damage. For reliable continuous operation, the device voltage and current must not exceed the maximum operating values specified in the table on page one.

Bias Conditions should also satisfy the following expression:

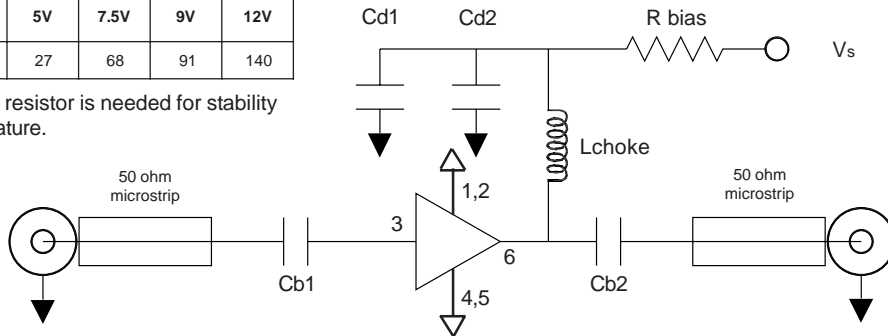
$$I_D V_D < (T_J - T_L) / R_{TH} \text{ j-1}$$

Pin #	Function	Description	Device Schematic
1	GND	Connection to ground. For best performance use via holes (as close to ground leads as possible) to reduce lead inductance.	
2	GND	Same as Pin 1	
3	RF IN	RF input pin. This pin requires the use of an external DC blocking capacitor chosen for the frequency of operation.	
4	GND	Same as Pin 1	
5	GND	Same as Pin 1	
6	RF OUT	RF output and bias pin. Bias should be supplied to this pin through an external series resistor and RF choke inductor. Because DC biasing is present on this pin, a DC blocking capacitor should be used in most applications (see application schematic). The supply side of this bias network should be well bypassed.	

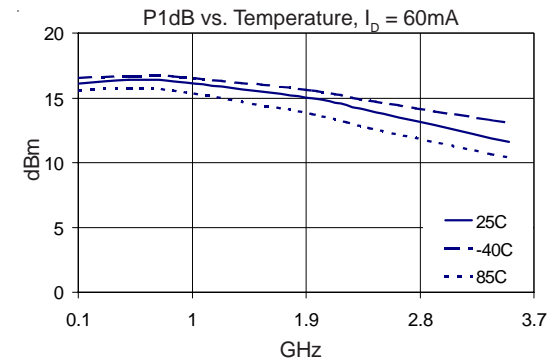
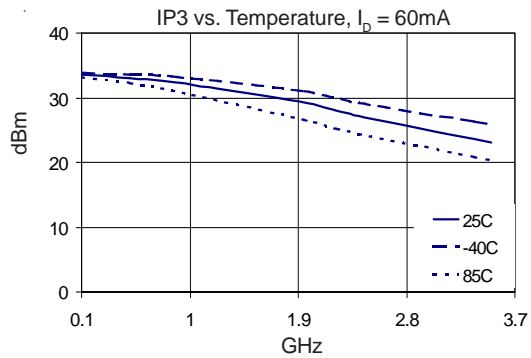
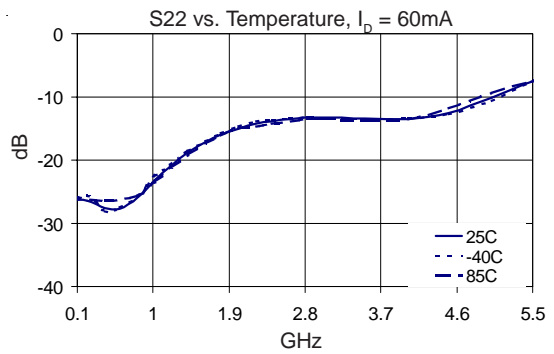
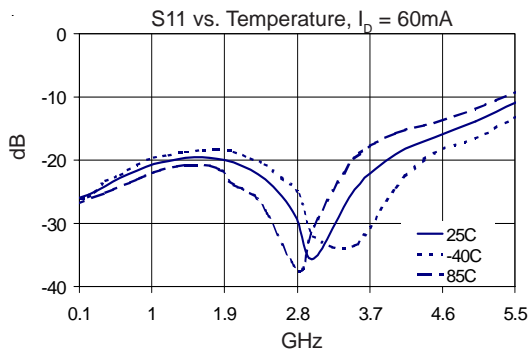
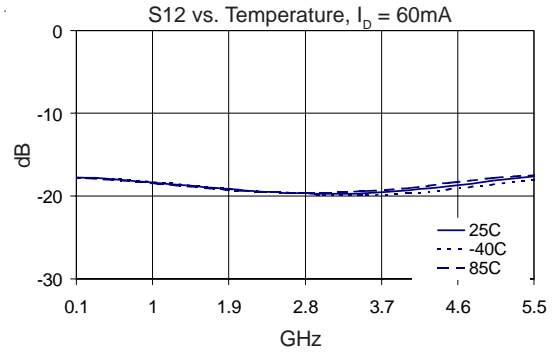
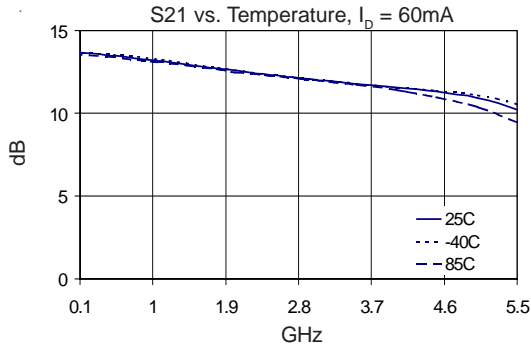
Application Schematic

Recommended Bias Resistor Values				
Supply Voltage(Vs)	5V	7.5V	9V	12V
Rbias (Ohms)	27	68	91	140

Note: A bias resistor is needed for stability over temperature.

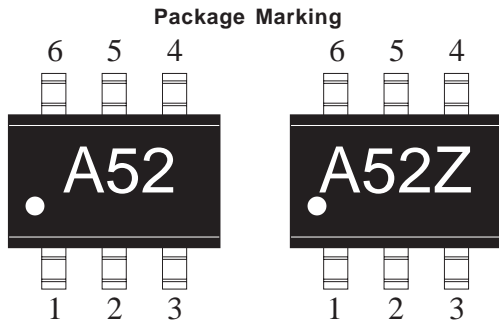


Reference Designator	Function	500 MHz	850 MHz	1950 MHz	2400 MHz
Cb1	DC Blocking	220 pF	100 pF	68 pF	56 pF
Cb2	DC Blocking	220 pF	100 pF	68 pF	56 pF
Cd1	Decoupling	1 uF	1 uF	1 uF	1 uF
Cd2	Decoupling	100 pF	68 pF	22 pF	22 pF
Lchoke	AC Blocking	68 nH	33 nH	22 nH	18 nH





Caution: ESD sensitive
Appropriate precautions in handling, packaging and testing devices must be observed.



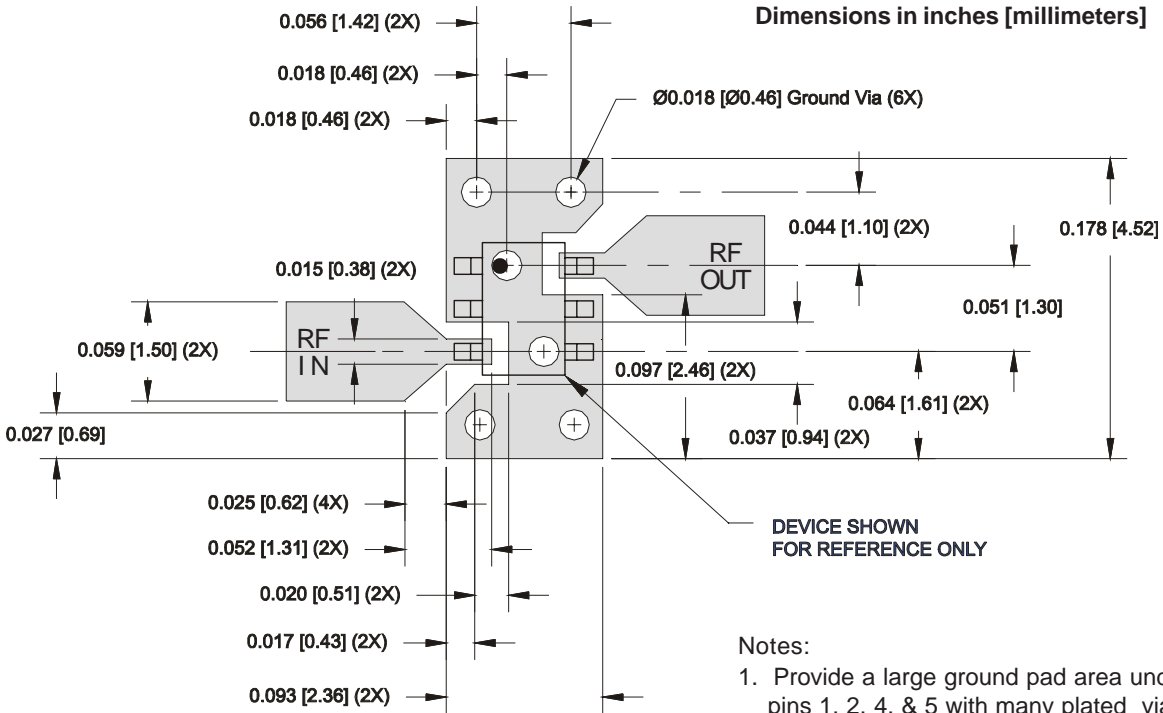
Part Number Ordering Information

Part Number	Reel Size	Devices/Reel
SGA-5263	7"	3000
SGA-5263Z	7"	3000

Note: Pin 1 is on lower left when you can read package marking

SOT-363 PCB Pad Layout

Dimensions in inches [millimeters]





Notes:

1. Provide a large ground pad area under device pins 1, 2, 4, & 5 with many plated via holes as shown.
2. Dimensions given for 50 Ohm RF I/O lines are for 31 mil thick Getek. Scale accordingly for different board thicknesses and dielectric constants.
3. We recommend 1 or 2 ounce copper. Measurements for this data sheet were made on a 31 mil thick Getek with 1 ounce copper on both sides.

Looking for pricing, stock, or lifecycle information?

Click below to explore more details on WIN SOURCE:

-  [View SGA-5263 on WIN SOURCE](#)
-  [RF Micro Devices Information](#)

Optimize Your Supply Chain with WIN SOURCE Solutions

-  Global Sourcing Solution
-  Obsolete Management
-  Cost Control Management
-  Shortage Management
-  Alternative Solution
-  Excess Inventory Management