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April 1st, 2010
Renesas Electronics Corporation

Issued by: Renesas Electronics Corporation (<http://www.renesas.com>)

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1. Overview

1.1 Features

The R8C/2A Group and R8C/2B Group of single-chip MCUs incorporates the R8C/Tiny Series CPU core, employing sophisticated instructions for a high level of efficiency. With 1 Mbyte of address space, and it is capable of executing instructions at high speed. In addition, the CPU core boasts a multiplier for high-speed operation processing.

Power consumption is low, and the supported operating modes allow additional power control. These MCUs also use an anti-noise configuration to reduce emissions of electromagnetic noise and are designed to withstand EMI.

Integration of many peripheral functions, including multifunction timer and serial interface, reduces the number of system components.

Furthermore, the R8C/2B Group has on-chip data flash (1 KB × 2 blocks).

The difference between the R8C/2A Group and R8C/2B Group is only the presence or absence of data flash. Their peripheral functions are the same.

1.1.1 Applications

Electronic household appliances, office equipment, audio equipment, consumer equipment, etc.

1.1.2 Specifications

Tables 1.1 and 1.2 outlines the Specifications for R8C/2A Group and Tables 1.3 and 1.4 outlines the Specifications for R8C/2B Group.

Table 1.1 Specifications for R8C/2A Group (1)

| Item | Function | Specification |
|--------------------------------|---------------------------|---|
| CPU | Central processing unit | R8C/Tiny series core <ul style="list-style-type: none"> • Number of fundamental instructions: 89 • Minimum instruction execution time: <ul style="list-style-type: none"> 50 ns ($f(XIN) = 20$ MHz, $VCC = 3.0$ to 5.5 V) 100 ns ($f(XIN) = 10$ MHz, $VCC = 2.7$ to 5.5 V) 200 ns ($f(XIN) = 5$ MHz, $VCC = 2.2$ to 5.5 V) • Multiplier: 16 bits \times 16 bits \rightarrow 32 bits • Multiply-accumulate instruction: 16 bits \times 16 bits + 32 bits \rightarrow 32 bits • Operation mode: Single-chip mode (address space: 1 Mbyte) |
| Memory | ROM, RAM | Refer to Table 1.5 Product List for R8C/2A Group . |
| Power Supply Voltage Detection | Voltage detection circuit | <ul style="list-style-type: none"> • Power-on reset • Voltage detection 2 |
| I/O Ports | Programmable I/O ports | <ul style="list-style-type: none"> • Input-only: 2 pins • CMOS I/O ports: 55, selectable pull-up resistor • High current drive ports: 8 |
| Clock | Clock generation circuits | 3 circuits: XIN clock oscillation circuit (with on-chip feedback resistor), On-chip oscillator (high-speed, low-speed) (high-speed on-chip oscillator has a frequency adjustment function), XCIN clock oscillation circuit (32 kHz) <ul style="list-style-type: none"> • Oscillation stop detection: XIN clock oscillation stop detection function • Frequency divider circuit: Dividing selectable 1, 2, 4, 8, and 16 • Low power consumption modes: <ul style="list-style-type: none"> Standard operating mode (high-speed clock, low-speed clock, high-speed on-chip oscillator, low-speed on-chip oscillator), wait mode, stop mode |
| | | Real-time clock (timer RE) |
| Interrupts | | <ul style="list-style-type: none"> • External: 5 sources, Internal: 23 sources, Software: 4 sources • Priority levels: 7 levels |
| Watchdog Timer | | 15 bits \times 1 (with prescaler), reset start selectable |
| Timer | Timer RA | 8 bits \times 1 (with 8-bit prescaler) Timer mode (period timer), pulse output mode (output level inverted every period), event counter mode, pulse width measurement mode, pulse period measurement mode |
| | Timer RB | 8 bits \times 1 (with 8-bit prescaler) Timer mode (period timer), programmable waveform generation mode (PWM output), programmable one-shot generation mode, programmable wait one-shot generation mode |
| | Timer RC | 16 bits \times 1 (with 4 capture/compare registers) Timer mode (input capture function, output compare function), PWM mode (output 3 pins), PWM2 mode (PWM output pin) |
| | Timer RD | 16 bits \times 2 (with 4 capture/compare registers) Timer mode (input capture function, output compare function), PWM mode (output 6 pins), reset synchronous PWM mode (output three-phase waveforms (6 pins), sawtooth wave modulation), complementary PWM mode (output three-phase waveforms (6 pins), triangular wave modulation), PWM3 mode (PWM output 2 pins with fixed period) |
| | Timer RE | 8 bits \times 1 Real-time clock mode (count seconds, minutes, hours, days of week), output compare mode |
| | Timer RF | 16 bits \times 1 (with capture/compare register pin and compare register pin) Input capture mode, output compare mode |

Table 1.2 Specifications for R8C/2A Group (2)

| Item | Function | Specification |
|---|---------------------|---|
| Serial Interface | UART0, UART1, UART2 | Clock synchronous serial I/O/UART x 3 |
| Clock Synchronous Serial I/O with Chip Select (SSU) | | 1 (shared with I ² C-bus) |
| I ² C bus ⁽¹⁾ | | 1 (shared with SSU) |
| LIN Module | | Hardware LIN: 1 (timer RA, UART0) |
| A/D Converter | | 10-bit resolution x 12 channels, includes sample and hold function |
| D/A Converter | | 8-bit resolution x 2 circuits |
| Flash Memory | | <ul style="list-style-type: none"> • Programming and erasure voltage: VCC = 2.7 to 5.5 V • Programming and erasure endurance: 100 times • Program security: ROM code protect, ID code check • Debug functions: On-chip debug, on-board flash rewrite function |
| Operating Frequency/Supply Voltage | | f(XIN) = 20 MHz (VCC = 3.0 to 5.5 V) f(XIN) = 10 MHz (VCC = 2.7 to 5.5 V) f(XIN) = 5 MHz (VCC = 2.2 to 5.5 V) |
| Current consumption | | 12 mA (VCC = 5.0 V, f(XIN) = 20 MHz) 5.5 mA (VCC = 3.0 V, f(XIN) = 10 MHz) 2.1 μ A (VCC = 3.0 V, wait mode (f(XCIN) = 32 kHz)) 0.65 μ A (VCC = 3.0 V, stop mode) |
| Operating Ambient Temperature | | -20 to 85°C (N version) -40 to 85°C (D version) ⁽²⁾ -20 to 105°C (Y version) ⁽³⁾ |
| Package | | 64-pin LQFP <ul style="list-style-type: none"> • Package code: PLQP0064KB-A (previous code: 64P6Q-A) • Package code: PLQP0064GA-A (previous code: 64P6U-A) 64-pin FLGA <ul style="list-style-type: none"> • Package code: PTLG0064JA-A (previous code: 64F0G) |

NOTES:

1. I²C bus is a trademark of Koninklijke Philips Electronics N. V.
2. Specify the D version if D version functions are to be used.
3. Please contact Renesas Technology sales offices for the Y version.

Table 1.3 Specifications for R8C/2B Group (1)

| Item | Function | Specification |
|--------------------------------|---------------------------|---|
| CPU | Central processing unit | R8C/Tiny series core <ul style="list-style-type: none"> • Number of fundamental instructions: 89 • Minimum instruction execution time: <ul style="list-style-type: none"> 50 ns ($f(XIN) = 20$ MHz, $VCC = 3.0$ to 5.5 V) 100 ns ($f(XIN) = 10$ MHz, $VCC = 2.7$ to 5.5 V) 200 ns ($f(XIN) = 5$ MHz, $VCC = 2.2$ to 5.5 V) • Multiplier: 16 bits \times 16 bits \rightarrow 32 bits • Multiply-accumulate instruction: 16 bits \times 16 bits + 32 bits \rightarrow 32 bits • Operation mode: Single-chip mode (address space: 1 Mbyte) |
| Memory | ROM, RAM | Refer to Table 1.6 Product List for R8C/2B Group . |
| Power Supply Voltage Detection | Voltage detection circuit | <ul style="list-style-type: none"> • Power-on reset • Voltage detection 2 |
| I/O Ports | Programmable I/O ports | <ul style="list-style-type: none"> • Input-only: 2 pins • CMOS I/O ports: 55, selectable pull-up resistor • High current drive ports: 8 |
| Clock | Clock generation circuits | <p>3 circuits: XIN clock oscillation circuit (with on-chip feedback resistor), On-chip oscillator (high-speed, low-speed) (high-speed on-chip oscillator has a frequency adjustment function), XCIN clock oscillation circuit (32 kHz)</p> <ul style="list-style-type: none"> • Oscillation stop detection: XIN clock oscillation stop detection function • Frequency divider circuit: Dividing selectable 1, 2, 4, 8, and 16 • Low power consumption modes: <ul style="list-style-type: none"> Standard operating mode (high-speed clock, low-speed clock, high-speed on-chip oscillator, low-speed on-chip oscillator), wait mode, stop mode <p>Real-time clock (timer RE)</p> |
| Interrupts | | <ul style="list-style-type: none"> • External: 5 sources, Internal: 23 sources, Software: 4 sources • Priority levels: 7 levels |
| Watchdog Timer | | 15 bits \times 1 (with prescaler), reset start selectable |
| Timer | Timer RA | 8 bits \times 1 (with 8-bit prescaler) Timer mode (period timer), pulse output mode (output level inverted every period), event counter mode, pulse width measurement mode, pulse period measurement mode |
| | Timer RB | 8 bits \times 1 (with 8-bit prescaler) Timer mode (period timer), programmable waveform generation mode (PWM output), programmable one-shot generation mode, programmable wait one-shot generation mode |
| | Timer RC | 16 bits \times 1 (with 4 capture/compare registers) Timer mode (input capture function, output compare function), PWM mode (output 3 pins), PWM2 mode (PWM output pin) |
| | Timer RD | 16 bits \times 2 (with 4 capture/compare registers) Timer mode (input capture function, output compare function), PWM mode (output 6 pins), reset synchronous PWM mode (output three-phase waveforms (6 pins), sawtooth wave modulation), complementary PWM mode (output three-phase waveforms (6 pins), triangular wave modulation), PWM3 mode (PWM output 2 pins with fixed period) |
| | Timer RE | 8 bits \times 1 Real-time clock mode (count seconds, minutes, hours, days of week), output compare mode |
| | Timer RF | 16 bits \times 1 (with capture/compare register pin and compare register pin) Input capture mode, output compare mode |

Table 1.4 Specifications for R8C/2B Group (2)

| Item | Function | Specification |
|---|---------------------|---|
| Serial Interface | UART0, UART1, UART2 | Clock synchronous serial I/O/UART x 3 |
| Clock Synchronous Serial I/O with Chip Select (SSU) | | 1 (shared with I ² C-bus) |
| I ² C bus ⁽¹⁾ | | 1 (shared with SSU) |
| LIN Module | | Hardware LIN: 1 (timer RA, UART0) |
| A/D Converter | | 10-bit resolution x 12 channels, includes sample and hold function |
| D/A Converter | | 8-bit resolution x 2 circuits |
| Flash Memory | | <ul style="list-style-type: none"> • Programming and erasure voltage: VCC = 2.7 to 5.5 V • Programming and erasure endurance: 10,000 times (data flash) 1,000 times (program ROM) • Program security: ROM code protect, ID code check • Debug functions: On-chip debug, on-board flash rewrite function |
| Operating Frequency/Supply Voltage | | f(XIN) = 20 MHz (VCC = 3.0 to 5.5 V) f(XIN) = 10 MHz (VCC = 2.7 to 5.5 V) f(XIN) = 5 MHz (VCC = 2.2 to 5.5 V) |
| Current consumption | | 12 mA (VCC = 5.0 V, f(XIN) = 20 MHz) 5.5 mA (VCC = 3.0 V, f(XIN) = 10 MHz) 2.1 μ A (VCC = 3.0 V, wait mode (f(XCIN) = 32 kHz)) 0.65 μ A (VCC = 3.0 V, stop mode) |
| Operating Ambient Temperature | | -20 to 85°C (N version) -40 to 85°C (D version) ⁽²⁾ -20 to 105°C (Y version) ⁽³⁾ |
| Package | | 64-pin LQFP <ul style="list-style-type: none"> • Package code: PLQP0064KB-A (previous code: 64P6Q-A) • Package code: PLQP0064GA-A (previous code: 64P6U-A) 64-pin FLGA <ul style="list-style-type: none"> • Package code: PTLG0064JA-A (previous code: 64F0G) |

NOTES:

1. I²C bus is a trademark of Koninklijke Philips Electronics N. V.
2. Specify the D version if D version functions are to be used.
3. Please contact Renesas Technology sales offices for the Y version.

1.2 Product List

Table 1.5 lists Product List for R8C/2A Group, Figure 1.1 shows a Part Number, Memory Size, and Package of R8C/2A Group, Table 1.6 lists Product List for R8C/2B Group, and Figure 1.2 shows a Part Number, Memory Size, and Package of R8C/2B Group.

Table 1.5 Product List for R8C/2A Group

Current of Nov. 2007

| Part No. | ROM Capacity | RAM Capacity | Package Type | Remarks | |
|------------------|--------------|--------------|--------------|-----------|--|
| R5F212A7SNFP | 48 Kbytes | 2.5 Kbytes | PLQP0064KB-A | N version | |
| R5F212A7SNFA | 48 Kbytes | 2.5 Kbytes | PLQP0064GA-A | | |
| R5F212A7SNLNG | 48 Kbytes | 2.5 Kbytes | PTLG0064JA-A | | |
| R5F212A8SNFP | 64 Kbytes | 3 Kbytes | PLQP0064KB-A | | |
| R5F212A8SNFA | 64 Kbytes | 3 Kbytes | PLQP0064GA-A | | |
| R5F212A8SNLNG | 64 Kbytes | 3 Kbytes | PTLG0064JA-A | | |
| R5F212AASNFP | 96 Kbytes | 7 Kbytes | PLQP0064KB-A | | |
| R5F212AASNFA | 96 Kbytes | 7 Kbytes | PLQP0064GA-A | | |
| R5F212AASNLNG | 96 Kbytes | 7 Kbytes | PTLG0064JA-A | | |
| R5F212ACSNFP | 128 Kbytes | 7.5 Kbytes | PLQP0064KB-A | | |
| R5F212ACSNFA | 128 Kbytes | 7.5 Kbytes | PLQP0064GA-A | | |
| R5F212ACSNLNG | 128 Kbytes | 7.5 Kbytes | PTLG0064JA-A | | |
| R5F212A7SDFP | 48 Kbytes | 2.5 Kbytes | PLQP0064KB-A | D version | |
| R5F212A7SDFA | 48 Kbytes | 2.5 Kbytes | PLQP0064GA-A | | |
| R5F212A8SDFP | 64 Kbytes | 3 Kbytes | PLQP0064KB-A | | |
| R5F212A8SDFA | 64 Kbytes | 3 Kbytes | PLQP0064GA-A | | |
| R5F212AASDFP | 96 Kbytes | 7 Kbytes | PLQP0064KB-A | | |
| R5F212AASDFA | 96 Kbytes | 7 Kbytes | PLQP0064GA-A | | |
| R5F212ACSDFP | 128 Kbytes | 7.5 Kbytes | PLQP0064KB-A | | |
| R5F212ACSDFA | 128 Kbytes | 7.5 Kbytes | PLQP0064GA-A | | |
| R5F212A7SNXXXFP | 48 Kbytes | 2.5 Kbytes | PLQP0064KB-A | N version | Factory programming product ⁽¹⁾ |
| R5F212A7SNXXXFA | 48 Kbytes | 2.5 Kbytes | PLQP0064GA-A | | |
| R5F212A7SNXXXLNG | 48 Kbytes | 2.5 Kbytes | PTLG0064JA-A | | |
| R5F212A8SNXXXFP | 64 Kbytes | 3 Kbytes | PLQP0064KB-A | | |
| R5F212A8SNXXXFA | 64 Kbytes | 3 Kbytes | PLQP0064GA-A | | |
| R5F212A8SNXXXLNG | 64 Kbytes | 3 Kbytes | PTLG0064JA-A | | |
| R5F212AASNXXXFP | 96 Kbytes | 7 Kbytes | PLQP0064KB-A | | |
| R5F212AASNXXXFA | 96 Kbytes | 7 Kbytes | PLQP0064GA-A | | |
| R5F212AASNXXXLNG | 96 Kbytes | 7 Kbytes | PTLG0064JA-A | | |
| R5F212ACSNXXXFP | 128 Kbytes | 7.5 Kbytes | PLQP0064KB-A | | |
| R5F212ACSNXXXFA | 128 Kbytes | 7.5 Kbytes | PLQP0064GA-A | | |
| R5F212ACSNXXXLNG | 128 Kbytes | 7.5 Kbytes | PTLG0064JA-A | | |
| R5F212A7SDXXXFP | 48 Kbytes | 2.5 Kbytes | PLQP0064KB-A | D version | Factory programming product ⁽¹⁾ |
| R5F212A7SDXXXFA | 48 Kbytes | 2.5 Kbytes | PLQP0064GA-A | | |
| R5F212A8SDXXXFP | 64 Kbytes | 3 Kbytes | PLQP0064KB-A | | |
| R5F212A8SDXXXFA | 64 Kbytes | 3 Kbytes | PLQP0064GA-A | | |
| R5F212AASDXXXFP | 96 Kbytes | 7 Kbytes | PLQP0064KB-A | | |
| R5F212AASDXXXFA | 96 Kbytes | 7 Kbytes | PLQP0064GA-A | | |
| R5F212ACSDXXXFP | 128 Kbytes | 7.5 Kbytes | PLQP0064KB-A | | |
| R5F212ACSDXXXFA | 128 Kbytes | 7.5 Kbytes | PLQP0064GA-A | | |

NOTE:

1. The user ROM is programmed before shipment.

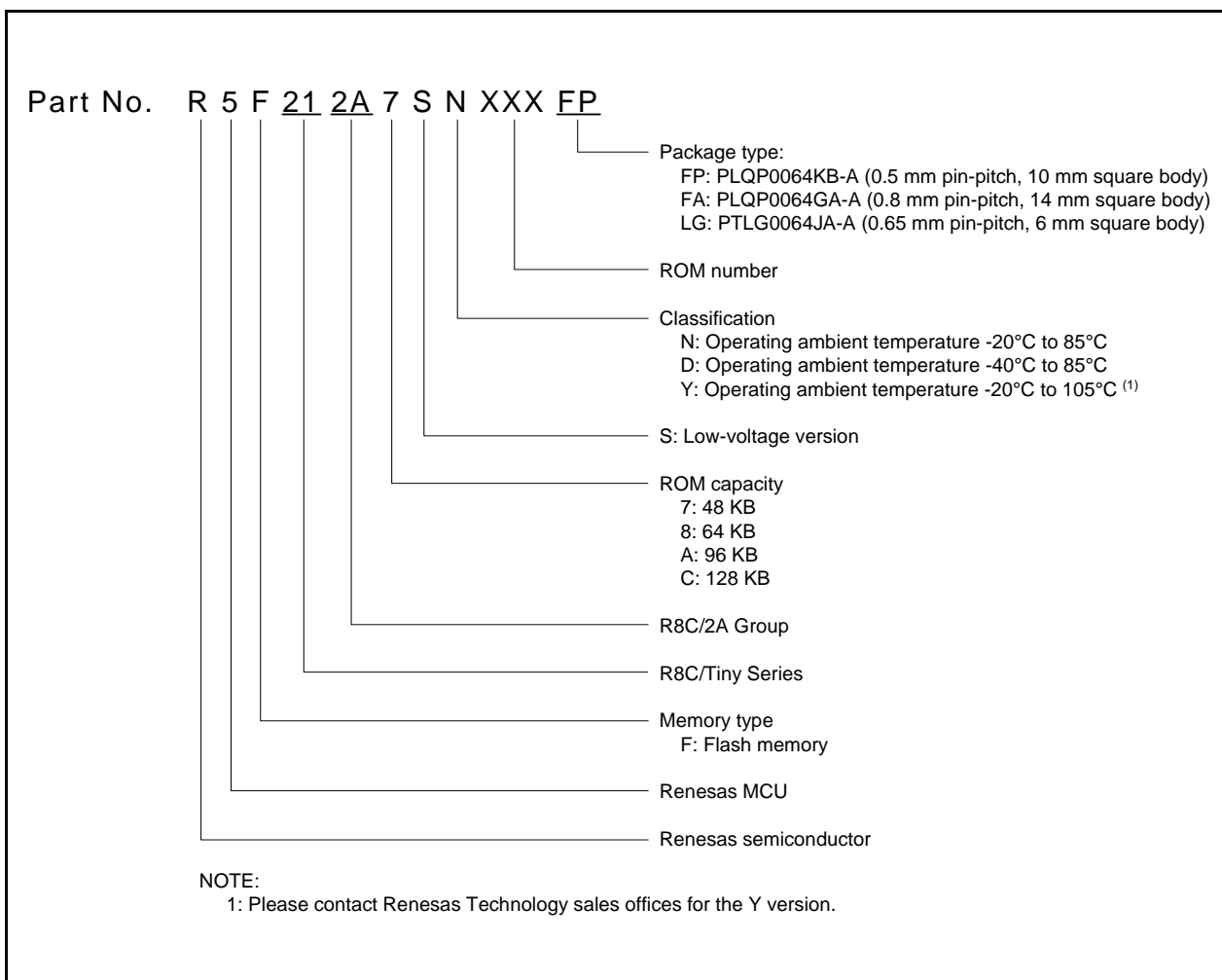


Figure 1.1 Part Number, Memory Size, and Package of R8C/2A Group

Table 1.6 Product List for R8C/2B Group

Current of Nov. 2007

| Part No. | ROM Capacity | | RAM Capacity | Package Type | Remarks | | | |
|-----------------|--------------|-------------|--------------|--------------|-----------|--|-----------|--|
| | Program ROM | Data flash | | | | | | |
| R5F212B7SNFP | 48 Kbytes | 1 Kbyte × 2 | 2.5 Kbytes | PLQP0064KB-A | N version | | | |
| R5F212B7SNFA | 48 Kbytes | 1 Kbyte × 2 | 2.5 Kbytes | PLQP0064GA-A | | | | |
| R5F212B7SNLG | 48 Kbytes | 1 Kbyte × 2 | 2.5 Kbytes | PTLG0064JA-A | | | | |
| R5F212B8SNFP | 64 Kbytes | 1 Kbyte × 2 | 3 Kbytes | PLQP0064KB-A | | | | |
| R5F212B8SNFA | 64 Kbytes | 1 Kbyte × 2 | 3 Kbytes | PLQP0064GA-A | | | | |
| R5F212B8SNLG | 64 Kbytes | 1 Kbyte × 2 | 3 Kbytes | PTLG0064JA-A | | | | |
| R5F212BASNFP | 96 Kbytes | 1 Kbyte × 2 | 7 Kbytes | PLQP0064KB-A | | | | |
| R5F212BASNFA | 96 Kbytes | 1 Kbyte × 2 | 7 Kbytes | PLQP0064GA-A | | | | |
| R5F212BASNLG | 96 Kbytes | 1 Kbyte × 2 | 7 Kbytes | PTLG0064JA-A | | | | |
| R5F212BCSNFP | 128 Kbytes | 1 Kbyte × 2 | 7.5 Kbytes | PLQP0064KB-A | | | | |
| R5F212BCSNFA | 128 Kbytes | 1 Kbyte × 2 | 7.5 Kbytes | PLQP0064GA-A | | | | |
| R5F212BCSNLG | 128 Kbytes | 1 Kbyte × 2 | 7.5 Kbytes | PTLG0064JA-A | | | | |
| R5F212B7SDFP | 48 Kbytes | 1 Kbyte × 2 | 2.5 Kbytes | PLQP0064KB-A | | | D version | |
| R5F212B7SDFA | 48 Kbytes | 1 Kbyte × 2 | 2.5 Kbytes | PLQP0064GA-A | | | | |
| R5F212B8SDFP | 64 Kbytes | 1 Kbyte × 2 | 3 Kbytes | PLQP0064KB-A | | | | |
| R5F212B8SDFA | 64 Kbytes | 1 Kbyte × 2 | 3 Kbytes | PLQP0064GA-A | | | | |
| R5F212BASDFP | 96 Kbytes | 1 Kbyte × 2 | 7 Kbytes | PLQP0064KB-A | | | | |
| R5F212BASDFA | 96 Kbytes | 1 Kbyte × 2 | 7 Kbytes | PLQP0064GA-A | | | | |
| R5F212BCSDFP | 128 Kbytes | 1 Kbyte × 2 | 7.5 Kbytes | PLQP0064KB-A | | | | |
| R5F212BCSDFA | 128 Kbytes | 1 Kbyte × 2 | 7.5 Kbytes | PLQP0064GA-A | | | | |
| R5F212B7SNXXXFP | 48 Kbytes | 1 Kbyte × 2 | 2.5 Kbytes | PLQP0064KB-A | N version | Factory programming product ⁽¹⁾ | | |
| R5F212B7SNXXXFA | 48 Kbytes | 1 Kbyte × 2 | 2.5 Kbytes | PLQP0064GA-A | | | | |
| R5F212B7SNXXXLG | 48 Kbytes | 1 Kbyte × 2 | 2.5 Kbytes | PTLG0064JA-A | | | | |
| R5F212B8SNXXXFP | 64 Kbytes | 1 Kbyte × 2 | 3 Kbytes | PLQP0064KB-A | | | | |
| R5F212B8SNXXXFA | 64 Kbytes | 1 Kbyte × 2 | 3 Kbytes | PLQP0064GA-A | | | | |
| R5F212B8SNXXXLG | 64 Kbytes | 1 Kbyte × 2 | 3 Kbytes | PTLG0064JA-A | | | | |
| R5F212BASNXXXFP | 96 Kbytes | 1 Kbyte × 2 | 7 Kbytes | PLQP0064KB-A | | | | |
| R5F212BASNXXXFA | 96 Kbytes | 1 Kbyte × 2 | 7 Kbytes | PLQP0064GA-A | | | | |
| R5F212BASNXXXLG | 96 Kbytes | 1 Kbyte × 2 | 7 Kbytes | PTLG0064JA-A | | | | |
| R5F212BCSNXXXFP | 128 Kbytes | 1 Kbyte × 2 | 7.5 Kbytes | PLQP0064KB-A | | | | |
| R5F212BCSNXXXFA | 128 Kbytes | 1 Kbyte × 2 | 7.5 Kbytes | PLQP0064GA-A | | | | |
| R5F212BCSNXXXLG | 128 Kbytes | 1 Kbyte × 2 | 7.5 Kbytes | PTLG0064JA-A | | | | |
| R5F212B7SDXXXFP | 48 Kbytes | 1 Kbyte × 2 | 2.5 Kbytes | PLQP0064KB-A | | | D version | |
| R5F212B7SDXXXFA | 48 Kbytes | 1 Kbyte × 2 | 2.5 Kbytes | PLQP0064GA-A | | | | |
| R5F212B8SDXXXFP | 64 Kbytes | 1 Kbyte × 2 | 3 Kbytes | PLQP0064KB-A | | | | |
| R5F212B8SDXXXFA | 64 Kbytes | 1 Kbyte × 2 | 3 Kbytes | PLQP0064GA-A | | | | |
| R5F212BASDXXXFP | 96 Kbytes | 1 Kbyte × 2 | 7 Kbytes | PLQP0064KB-A | | | | |
| R5F212BASDXXXFA | 96 Kbytes | 1 Kbyte × 2 | 7 Kbytes | PLQP0064GA-A | | | | |
| R5F212BCSDXXXFP | 128 Kbytes | 1 Kbyte × 2 | 7.5 Kbytes | PLQP0064KB-A | | | | |
| R5F212BCSDXXXFA | 128 Kbytes | 1 Kbyte × 2 | 7.5 Kbytes | PLQP0064GA-A | | | | |

NOTE:

1. The user ROM is programmed before shipment.

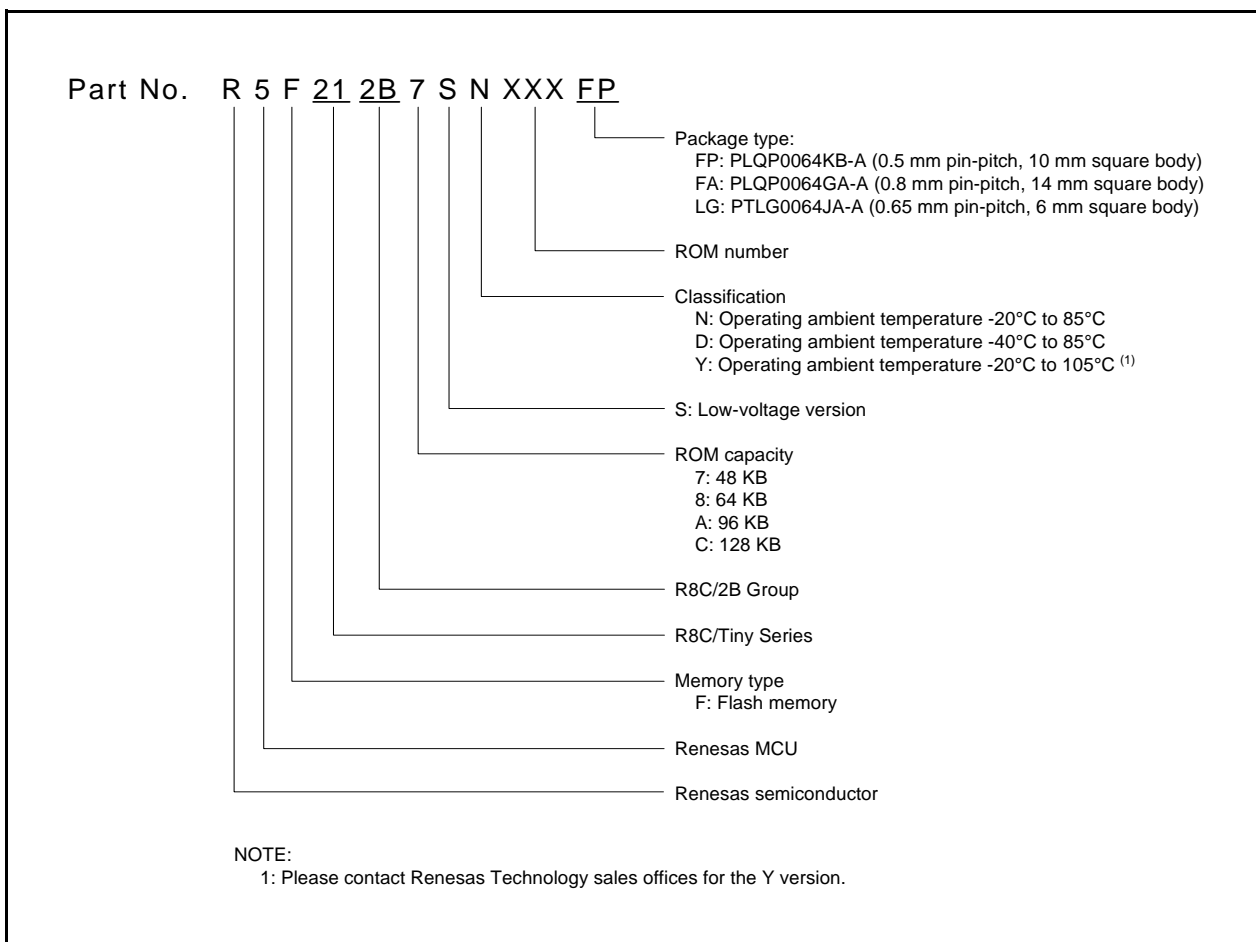


Figure 1.2 Part Number, Memory Size, and Package of R8C/2B Group

1.3 Block Diagram

Figure 1.3 shows a Block Diagram.

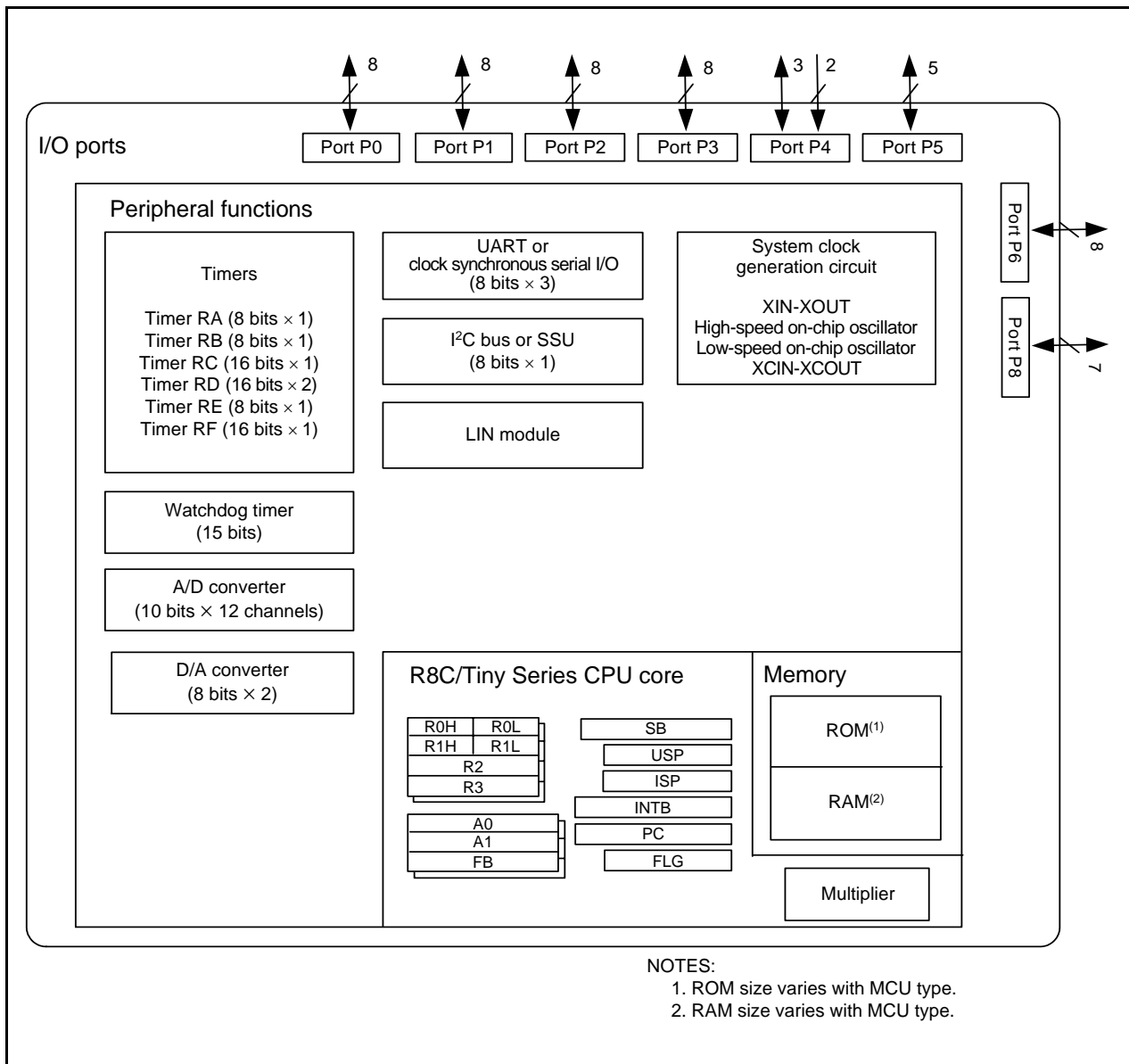


Figure 1.3 Block Diagram

1.4 Pin Assignment

Figure 1.4 shows 64-pin LQFP Package Pin Assignment (Top View). Figure 1.5 shows 64-pin FLGA Package Pin Assignment (Top Perspective View). Tables 1.7 and 1.8 outlines the Pin Name Information by Pin Number.

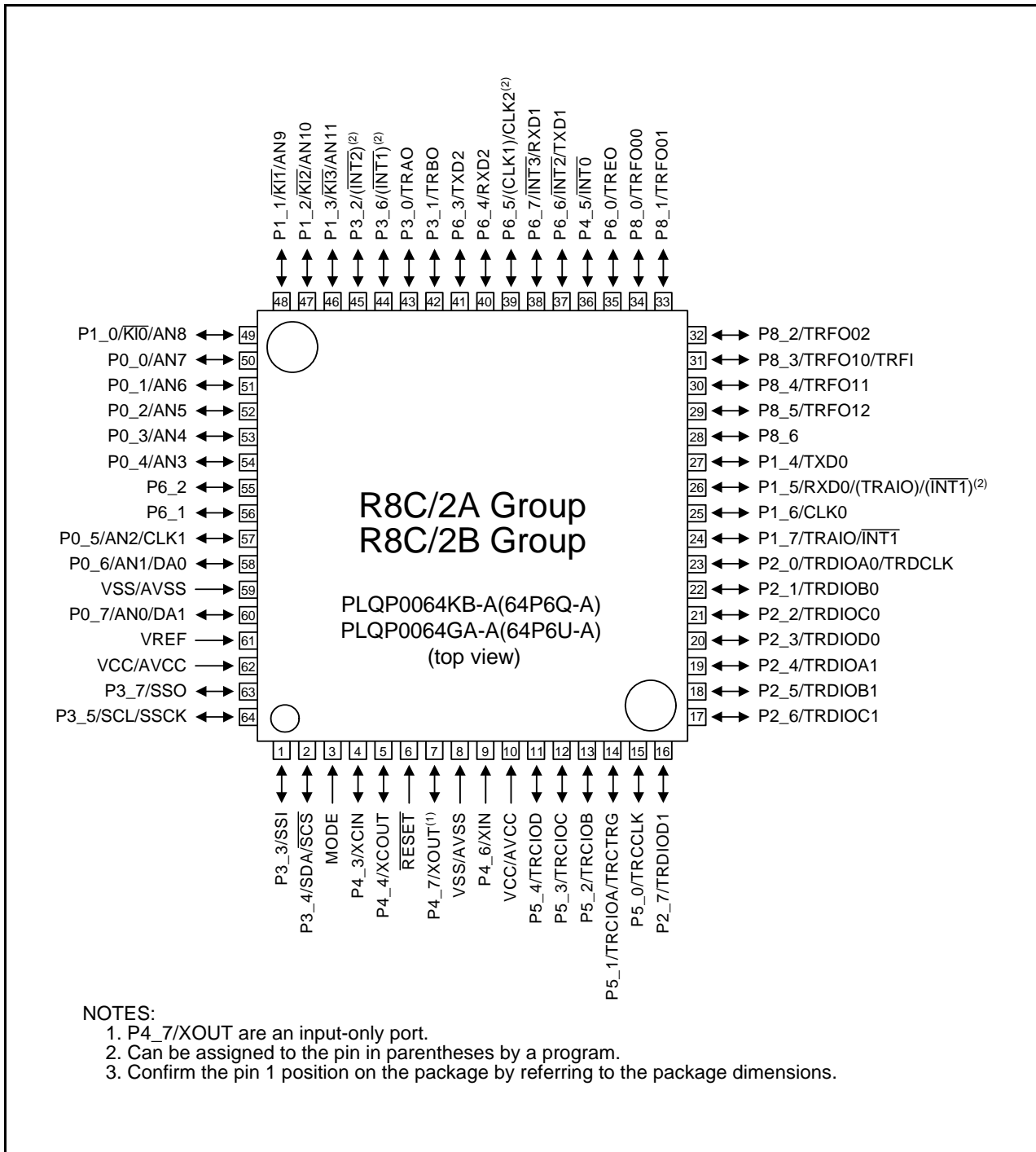


Figure 1.4 64-pin LQFP Package Pin Assignment (Top View)

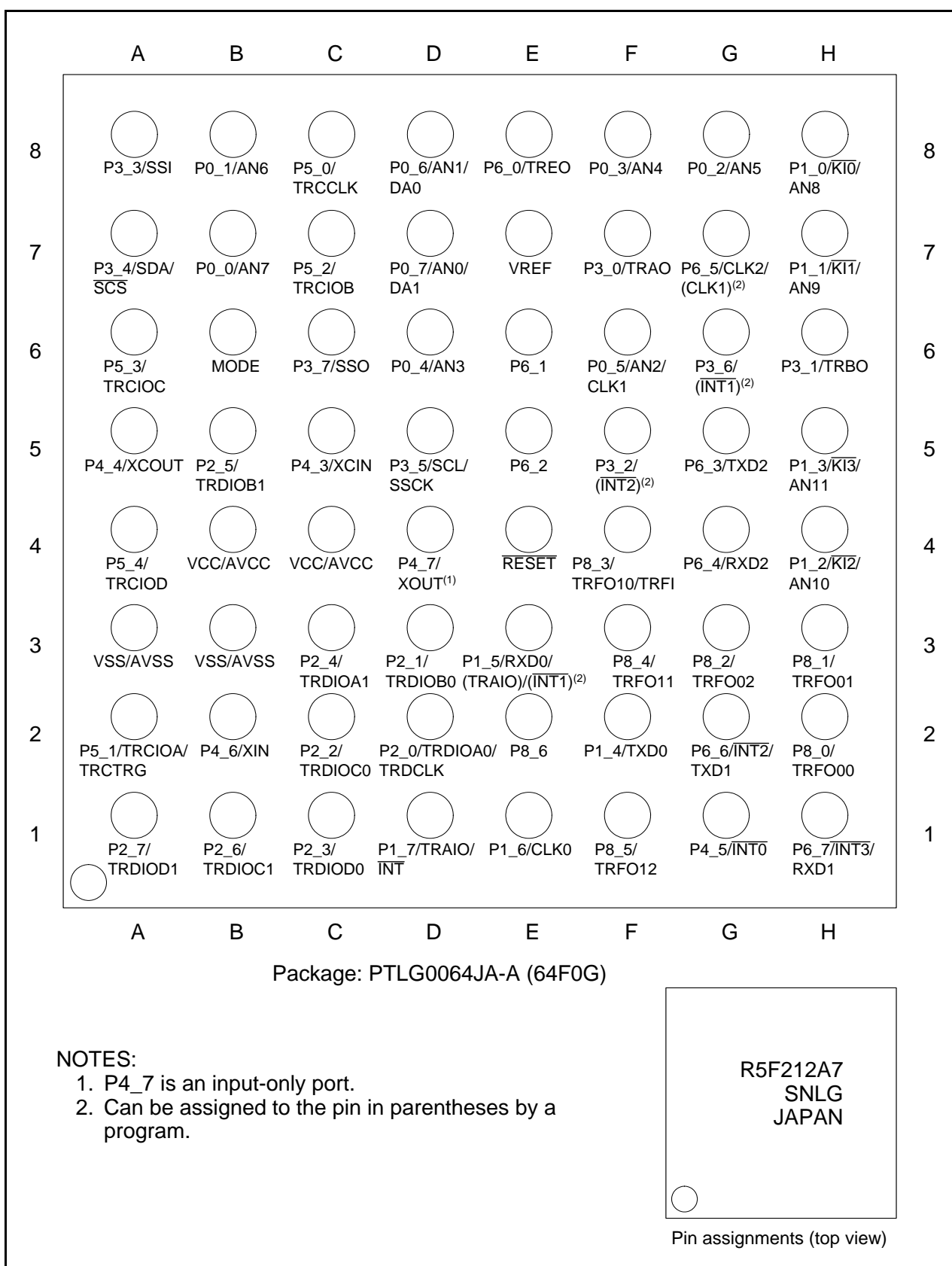


Figure 1.5 64-pin FLGA Package Pin Assignment (Top Perspective View)

Table 1.7 Pin Name Information by Pin Number (1)

| Pin Number | Control Pin | Port | I/O Pin Functions for of Peripheral Modules | | | | | |
|------------|-------------|------|---|------------------------|---------------------------------|-----|----------------------|------------------------------|
| | | | Interrupt | Timer | Serial Interface | SSU | I ² C bus | A/D Converter, D/A Converter |
| 1 | | P3_3 | | | | SSI | | |
| 2 | | P3_4 | | | | SCS | SDA | |
| 3 | MODE | | | | | | | |
| 4 | XCIN | P4_3 | | | | | | |
| 5 | XCOU | P4_4 | | | | | | |
| 6 | RESET | | | | | | | |
| 7 | XOUT | P4_7 | | | | | | |
| 8 | VSS/AVSS | | | | | | | |
| 9 | XIN | P4_6 | | | | | | |
| 10 | VCC/AVCC | | | | | | | |
| 11 | | P5_4 | | TRCIOD | | | | |
| 12 | | P5_3 | | TRCIOC | | | | |
| 13 | | P5_2 | | TRCIOB | | | | |
| 14 | | P5_1 | | TRCIOA/TRCTR | | | | |
| 15 | | P5_0 | | TRCCLK | | | | |
| 16 | | P2_7 | | TRDIOD1 | | | | |
| 17 | | P2_6 | | TRDIOC1 | | | | |
| 18 | | P2_5 | | TRDIQB1 | | | | |
| 19 | | P2_4 | | TRDIOA1 | | | | |
| 20 | | P2_3 | | TRDIOD0 | | | | |
| 21 | | P2_2 | | TRDIOC0 | | | | |
| 22 | | P2_1 | | TRDIQB0 | | | | |
| 23 | | P2_0 | | TRDIOA0/TRDCLK | | | | |
| 24 | | P1_7 | INT1 | TRAIO | | | | |
| 25 | | P1_6 | | | CLK0 | | | |
| 26 | | P1_5 | (INT1) ⁽¹⁾ | (TRAIO) ⁽¹⁾ | RXD0 | | | |
| 27 | | P1_4 | | | TXD0 | | | |
| 28 | | P8_6 | | | | | | |
| 29 | | P8_5 | | TRFO12 | | | | |
| 30 | | P8_4 | | TRFO11 | | | | |
| 31 | | P8_3 | | TRFO10/TRFI | | | | |
| 32 | | P8_2 | | TRFO02 | | | | |
| 33 | | P8_1 | | TRFO01 | | | | |
| 34 | | P8_0 | | TRFO00 | | | | |
| 35 | | P6_0 | | TREO | | | | |
| 36 | | P4_5 | INT0 | INT0 | | | | |
| 37 | | P6_6 | INT2 | | TXD1 | | | |
| 38 | | P6_7 | INT3 | | RXD1 | | | |
| 39 | | P6_5 | | | (CLK1) ⁽¹⁾ / CLK2 | | | |
| 40 | | P6_4 | | | RXD2 | | | |
| 41 | | P6_3 | | | TXD2 | | | |
| 42 | | P3_1 | | TRBO | | | | |
| 43 | | P3_0 | | TRAO | | | | |
| 44 | | P3_6 | (INT1) ⁽¹⁾ | | | | | |
| 45 | | P3_2 | (INT2) ⁽¹⁾ | | | | | |

NOTE:

1. Can be assigned to the pin in parentheses by a program.

Table 1.8 Pin Name Information by Pin Number (2)

| Pin Number | Control Pin | Port | I/O Pin Functions for of Peripheral Modules | | | | | A/D Converter, D/A Converter |
|------------|-------------|------|---|-------|------------------|------|----------------------|------------------------------|
| | | | Interrupt | Timer | Serial Interface | SSU | I ² C bus | |
| 46 | | P1_3 | $\overline{KI3}$ | | | | | AN11 |
| 47 | | P1_2 | $\overline{KI2}$ | | | | | AN10 |
| 48 | | P1_1 | $\overline{KI1}$ | | | | | AN9 |
| 49 | | P1_0 | $\overline{KI0}$ | | | | | AN8 |
| 50 | | P0_0 | | | | | | AN7 |
| 51 | | P0_1 | | | | | | AN6 |
| 52 | | P0_2 | | | | | | AN5 |
| 53 | | P0_3 | | | | | | AN4 |
| 54 | | P0_4 | | | | | | AN3 |
| 55 | | P6_2 | | | | | | |
| 56 | | P6_1 | | | | | | |
| 57 | | P0_5 | | | CLK1 | | | AN2 |
| 58 | | P0_6 | | | | | | AN1/DA0 |
| 59 | VSS/AVSS | | | | | | | |
| 60 | | P0_7 | | | | | | AN0/DA1 |
| 61 | VREF | | | | | | | |
| 62 | VCC/AVCC | | | | | | | |
| 63 | | P3_7 | | | | SSO | | |
| 64 | | P3_5 | | | | SSCK | SCL | |

1.5 Pin Functions

Tables 1.9 and 1.10 list Pin Functions.

Table 1.9 Pin Functions (1)

| Item | Pin Name | I/O Type | Description |
|---|--|----------|---|
| Power supply input | VCC, VSS | – | Apply 2.2 V to 5.5 V to the VCC pin. Apply 0 V to the VSS pin. |
| Analog power supply input | AVCC, AVSS | – | Power supply for the A/D converter. Connect a capacitor between AVCC and AVSS. |
| Reset input | $\overline{\text{RESET}}$ | I | Input “L” on this pin resets the MCU. |
| MODE | MODE | I | Connect this pin to VCC via a resistor. |
| XIN clock input | XIN | I | These pins are provided for XIN clock generation circuit I/O. Connect a ceramic resonator or a crystal oscillator between the XIN and XOUT pins ⁽¹⁾ . To use an external clock, input it to the XIN pin and leave the XOUT pin open. |
| XIN clock output | XOUT | O | |
| XCIN clock input | XCIN | I | These pins are provided for XCIN clock generation circuit I/O. Connect a crystal oscillator between the XCIN and XCOU pins ⁽¹⁾ . To use an external clock, input it to the XCIN pin and leave the XCOU pin open. |
| XCIN clock output | XCOU | O | |
| $\overline{\text{INT}}$ interrupt input | $\overline{\text{INT0}}$ to $\overline{\text{INT3}}$ | I | $\overline{\text{INT}}$ interrupt input pins. $\overline{\text{INT0}}$ is timer RD input pin. $\overline{\text{INT1}}$ is timer RA input pin. |
| Key input interrupt | $\overline{\text{KI0}}$ to $\overline{\text{KI3}}$ | I | Key input interrupt input pins |
| Timer RA | TRAIO | I/O | Timer RA I/O pin |
| | TRAO | O | Timer RA output pin |
| Timer RB | TRBO | O | Timer RB output pin |
| Timer RC | TRCLK | I | External clock input pin |
| | TRCTR | I | External trigger input pin |
| | TRCIOA, TRCIOB, TRCIO, TRCIOD | I/O | Timer RC I/O pins |
| Timer RD | TRDIOA0, TRDIOA1, TRDIOB0, TRDIOB1, TRDIOC0, TRDIOC1, TRDIOD0, TRDIOD1 | I/O | Timer RD I/O pins |
| | TRDCLK | I | External clock input pin |
| Timer RE | TREO | O | Divided clock output pin |
| Timer RF | TRFI | I | Timer RF input pin |
| | TRFO00 to TRFO02, TRFO10 to TRFO12 | O | Timer RF output pins |
| Serial interface | CLK0, CLK1, CLK2 | I/O | Transfer clock I/O pins |
| | RXD0, RXD1, RXD2 | I | Serial data input pins |
| | TXD0, TXD1, TXD2 | O | Serial data output pins |
| I ² C bus | SCL | I/O | Clock I/O pin |
| | SDA | I/O | Data I/O pin |
| SSU | SSI | I/O | Data I/O pin |
| | $\overline{\text{SCS}}$ | I/O | Chip-select signal I/O pin |
| | SSCK | I/O | Clock I/O pin |
| | SSO | I/O | Data I/O pin |
| Reference voltage input | VREF | I | Reference voltage input pin to A/D converter and D/A converter |

I: Input O: Output I/O: Input and output

NOTE:

1. Refer to the oscillator manufacturer for oscillation characteristics.

Table 1.10 Pin Functions (2)

| Item | Pin Name | I/O Type | Description |
|---------------|---|----------|---|
| A/D converter | AN0 to AN11 | I | Analog input pins to A/D converter |
| D/A converter | DA0 to DA1 | O | D/A converter output pins |
| I/O port | P0_0 to P0_7, P1_0 to P1_7, P2_0 to P2_7, P3_0 to P3_7, P4_3 to P4_5, P5_0 to P5_4, P6_0 to P6_7, P8_0 to P8_6 | I/O | CMOS I/O ports. Each port has an I/O select direction register, allowing each pin in the port to be directed for input or output individually. Any port set to input can be set to use a pull-up resistor or not by a program. P2_0 to P2_7 also function as LED drive ports. |
| Input port | P4_6, P4_7 | I | Input-only ports |

I: Input O: Output I/O: Input and output

2. Central Processing Unit (CPU)

Figure 2.1 shows the CPU Registers. The CPU contains 13 registers. R0, R1, R2, R3, A0, A1, and FB configure a register bank. There are two sets of register bank.

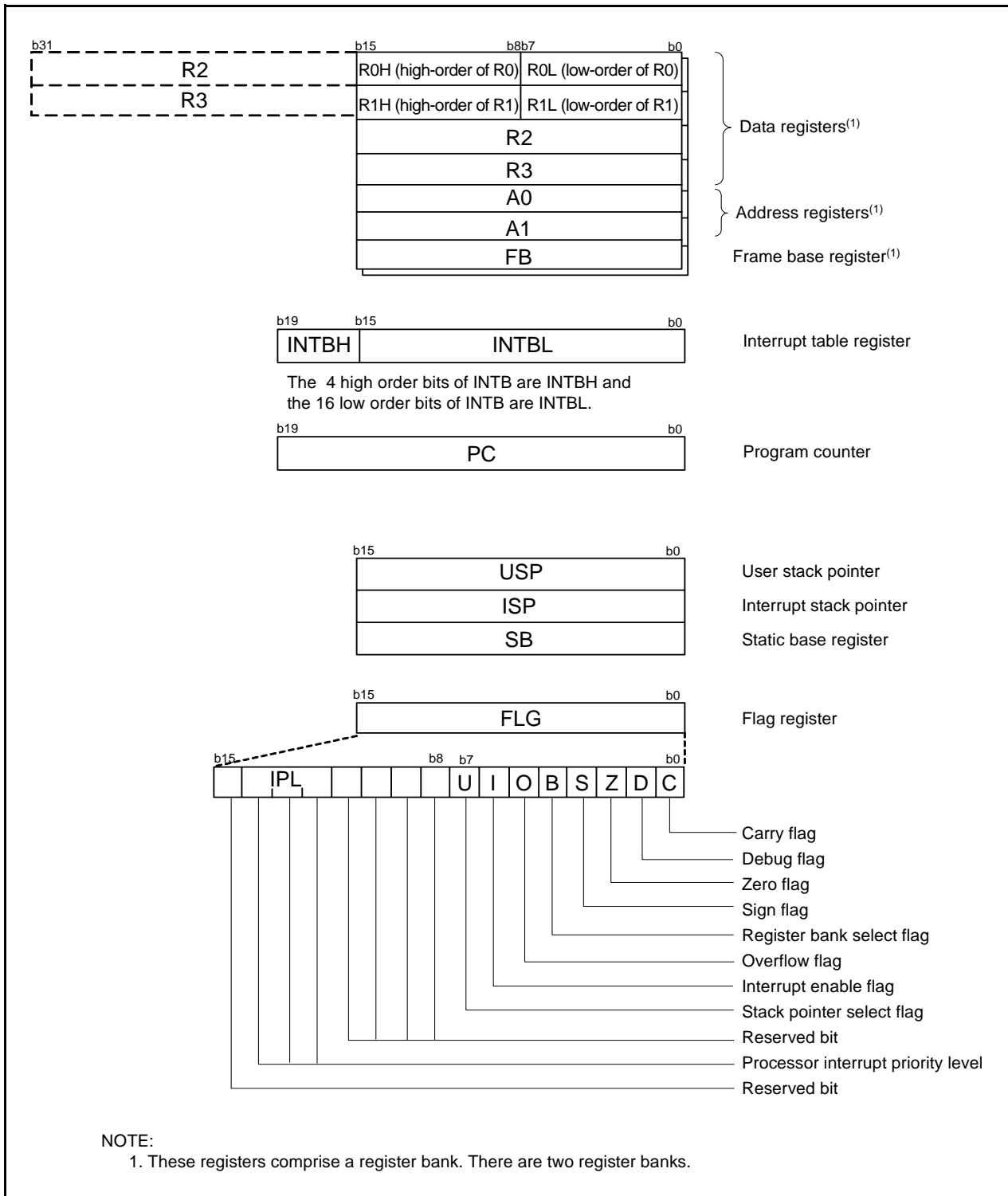


Figure 2.1 CPU Registers

2.1 Data Registers (R0, R1, R2, and R3)

R0 is a 16-bit register for transfer, arithmetic, and logic operations. The same applies to R1 to R3. R0 can be split into high-order bits (R0H) and low-order bits (R0L) to be used separately as 8-bit data registers. R1H and R1L are analogous to R0H and R0L. R2 can be combined with R0 and used as a 32-bit data register (R2R0). R3R1 is analogous to R2R0.

2.2 Address Registers (A0 and A1)

A0 is a 16-bit register for address register indirect addressing and address register relative addressing. It is also used for transfer, arithmetic, and logic operations. A1 is analogous to A0. A1 can be combined with A0 and as a 32-bit address register (A1A0).

2.3 Frame Base Register (FB)

FB is a 16-bit register for FB relative addressing.

2.4 Interrupt Table Register (INTB)

INTB is a 20-bit register that indicates the start address of an interrupt vector table.

2.5 Program Counter (PC)

PC is 20 bits wide and indicates the address of the next instruction to be executed.

2.6 User Stack Pointer (USP) and Interrupt Stack Pointer (ISP)

The stack pointers (SP), USP, and ISP, are each 16 bits wide. The U flag of FLG is used to switch between USP and ISP.

2.7 Static Base Register (SB)

SB is a 16-bit register for SB relative addressing.

2.8 Flag Register (FLG)

FLG is an 11-bit register indicating the CPU state.

2.8.1 Carry Flag (C)

The C flag retains carry, borrow, or shift-out bits that have been generated by the arithmetic and logic unit.

2.8.2 Debug Flag (D)

The D flag is for debugging only. Set it to 0.

2.8.3 Zero Flag (Z)

The Z flag is set to 1 when an arithmetic operation results in 0; otherwise to 0.

2.8.4 Sign Flag (S)

The S flag is set to 1 when an arithmetic operation results in a negative value; otherwise to 0.

2.8.5 Register Bank Select Flag (B)

Register bank 0 is selected when the B flag is 0. Register bank 1 is selected when this flag is set to 1.

2.8.6 Overflow Flag (O)

The O flag is set to 1 when an operation results in an overflow; otherwise to 0.

2.8.7 Interrupt Enable Flag (I)

The I flag enables maskable interrupts.

Interrupt are disabled when the I flag is set to 0, and are enabled when the I flag is set to 1. The I flag is set to 0 when an interrupt request is acknowledged.

2.8.8 Stack Pointer Select Flag (U)

ISP is selected when the U flag is set to 0; USP is selected when the U flag is set to 1.

The U flag is set to 0 when a hardware interrupt request is acknowledged or the INT instruction of software interrupt numbers 0 to 31 is executed.

2.8.9 Processor Interrupt Priority Level (IPL)

IPL is 3 bits wide and assigns processor interrupt priority levels from level 0 to level 7.

If a requested interrupt has higher priority than IPL, the interrupt is enabled.

2.8.10 Reserved Bit

If necessary, set to 0. When read, the content is undefined.

3. Memory

3.1 R8C/2A Group

Figure 3.1 is a Memory Map of R8C/2A Group. The R8C/2A group has 1 Mbyte of address space from addresses 00000h to FFFFFh.

The internal ROM is allocated lower addresses, beginning with address 0FFFFh. For example, a 48-Kbyte internal ROM area is allocated addresses 04000h to 0FFFFh.

The fixed interrupt vector table is allocated addresses 0FFDCh to 0FFFFh. They store the starting address of each interrupt routine.

The internal RAM is allocated higher addresses, beginning with address 00400h. For example, a 2.5-Kbyte internal RAM area is allocated addresses 00400h to 00DFFh. The internal RAM is used not only for storing data but also for calling subroutines and as stacks when interrupt requests are acknowledged.

Special function registers (SFRs) are allocated addresses 00000h to 002FFh. The peripheral function control registers are allocated here. All addresses within the SFR, which have nothing allocated are reserved for future use and cannot be accessed by users.

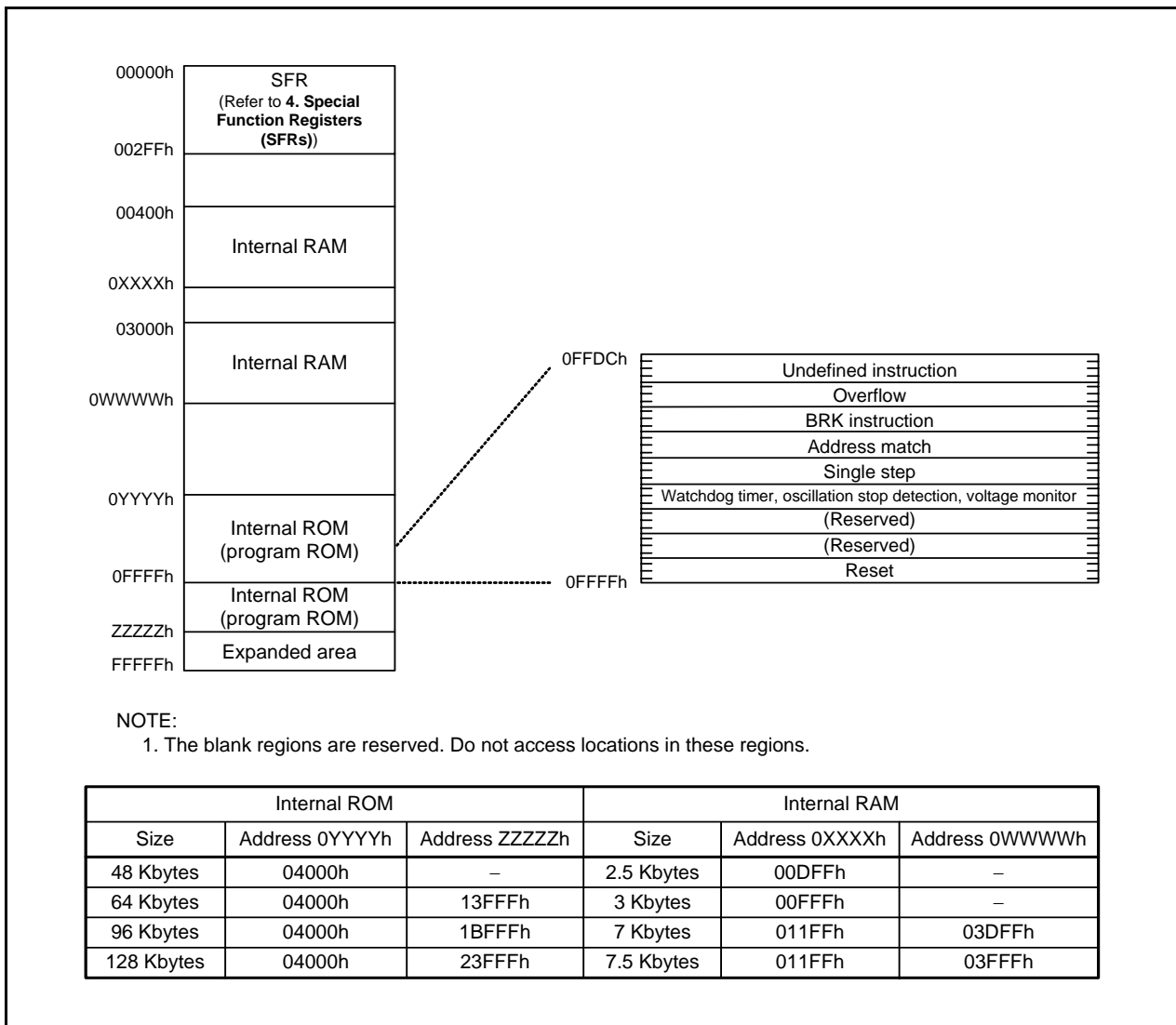


Figure 3.1 Memory Map of R8C/2A Group

3.2 R8C/2B Group

Figure 3.2 is a Memory Map of R8C/2B Group. The R8C/2B group has 1 Mbyte of address space from addresses 00000h to FFFFFh.

The internal ROM (program ROM) is allocated lower addresses, beginning with address 0FFFFh. For example, a 48-Kbyte internal ROM area is allocated addresses 04000h to 0FFFFh.

The fixed interrupt vector table is allocated addresses 0FFDCh to 0FFFFh. They store the starting address of each interrupt routine.

The internal ROM (data flash) is allocated addresses 02400h to 02BFFh.

The internal RAM area is allocated higher addresses, beginning with address 00400h. For example, a 2.5-Kbyte internal RAM is allocated addresses 00400h to 00DFFh. The internal RAM is used not only for storing data but also for calling subroutines and as stacks when interrupt requests are acknowledged.

Special function registers (SFRs) are allocated addresses 00000h to 002FFh. The peripheral function control registers are allocated here. All addresses within the SFR, which have nothing allocated are reserved for future use and cannot be accessed by users.

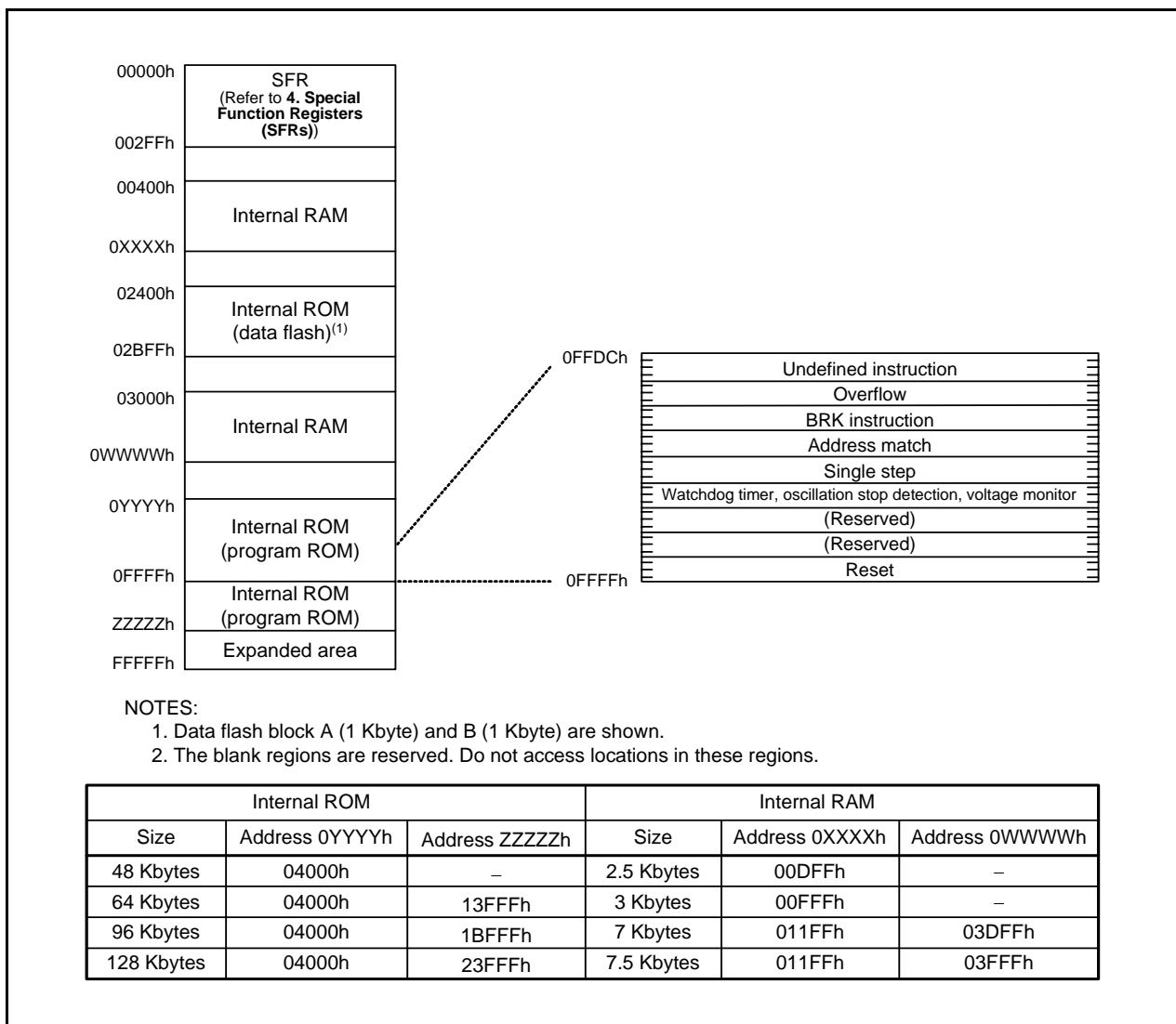


Figure 3.2 Memory Map of R8C/2B Group

4. Special Function Registers (SFRs)

An SFR (special function register) is a control register for a peripheral function. Tables 4.1 to 4.12 list the special function registers.

Table 4.1 SFR Information (1)(1)

| Address | Register | Symbol | After reset |
|---------|---|--------|--|
| 0000h | | | |
| 0001h | | | |
| 0002h | | | |
| 0003h | | | |
| 0004h | Processor Mode Register 0 | PM0 | 00h |
| 0005h | Processor Mode Register 1 | PM1 | 00h |
| 0006h | System Clock Control Register 0 | CM0 | 01101000b |
| 0007h | System Clock Control Register 1 | CM1 | 00100000b |
| 0008h | Module Operation Enable Register | MSTCR | 00h |
| 0009h | | | |
| 000Ah | Protect Register | PRCR | 00h |
| 000Bh | | | |
| 000Ch | Oscillation Stop Detection Register | OCD | 00000100b |
| 000Dh | Watchdog Timer Reset Register | WDTR | XXh |
| 000Eh | Watchdog Timer Start Register | WDTS | XXh |
| 000Fh | Watchdog Timer Control Register | WDC | 00X11111b |
| 0010h | Address Match Interrupt Register 0 | RMAD0 | 00h |
| 0011h | | | 00h |
| 0012h | | | 00h |
| 0013h | Address Match Interrupt Enable Register | AIER | 00h |
| 0014h | Address Match Interrupt Register 1 | RMAD1 | 00h |
| 0015h | | | 00h |
| 0016h | | | 00h |
| 0017h | | | |
| 0018h | | | |
| 0019h | | | |
| 001Ah | | | |
| 001Bh | | | |
| 001Ch | Count Source Protection Mode Register | CSPR | 00h 10000000b ⁽⁶⁾ |
| 001Dh | | | |
| 001Eh | | | |
| 001Fh | | | |
| 0020h | | | |
| 0021h | | | |
| 0022h | | | |
| 0023h | High-Speed On-Chip Oscillator Control Register 0 | FRA0 | 00h |
| 0024h | High-Speed On-Chip Oscillator Control Register 1 | FRA1 | When shipping |
| 0025h | High-Speed On-Chip Oscillator Control Register 2 | FRA2 | 00h |
| 0026h | | | |
| 0027h | | | |
| 0028h | Clock Prescaler Reset Flag | CPSRF | 00h |
| 0029h | | | |
| 002Ah | | | |
| 002Bh | High-Speed On-Chip Oscillator Control Register 6 | FRA6 | When Shipping |
| 002Ch | High-Speed On-Chip Oscillator Control Register 7 | FRA7 | When Shipping |
| 0030h | | | |
| 0031h | Voltage Detection Register 1 ⁽²⁾ | VCA1 | 00001000b |
| 0032h | Voltage Detection Register 2 ⁽²⁾ | VCA2 | 00h ⁽³⁾ 00100000b ⁽⁴⁾ |
| 0033h | | | |
| 0034h | | | |
| 0035h | | | |
| 0036h | Voltage Monitor 1 Circuit Control Register ⁽⁵⁾ | VW1C | 00001000b |
| 0037h | Voltage Monitor 2 Circuit Control Register ⁽⁵⁾ | VW2C | 00h |
| 0038h | Voltage Monitor 0 Circuit Control Register ⁽²⁾ | VW0C | 0000X000b ⁽³⁾ 0100X001b ⁽⁴⁾ |
| 0039h | | | |
| 003Ah | | | |
| 003Eh | | | |
| 003Fh | | | |

X: Undefined

NOTES:

1. The blank regions are reserved. Do not access locations in these regions.
2. Software reset, watchdog timer reset, voltage monitor 1 reset, or voltage monitor 2 reset do not affect this register.
3. The LVD0ON bit in the OFS register is set to 1 and hardware reset.
4. Power-on reset, voltage monitor 0 reset, or the LVD0ON bit in the OFS register is set to 0 and hardware reset.
5. Software reset, watchdog timer reset, voltage monitor 1 reset, or voltage monitor 2 reset do not affect b2 and b3.
6. The CSPROINI bit in the OFS register is set to 0.

Table 4.2 SFR Information (2)(1)

| Address | Register | Symbol | After reset |
|---------|---|---------------|-------------|
| 0040h | | | |
| 0041h | | | |
| 0042h | | | |
| 0043h | | | |
| 0044h | | | |
| 0045h | | | |
| 0046h | | | |
| 0047h | Timer RC Interrupt Control Register | TRCIC | XXXXX000b |
| 0048h | Timer RD0 Interrupt Control Register | TRD0IC | XXXXX000b |
| 0049h | Timer RD1 Interrupt Control Register | TRD1IC | XXXXX000b |
| 004Ah | Timer RE Interrupt Control Register | TREIC | XXXXX000b |
| 004Bh | UART2 Transmit Interrupt Control Register | S2TIC | XXXXX000b |
| 004Ch | UART2 Receive Interrupt Control Register | S2RIC | XXXXX000b |
| 004Dh | Key Input Interrupt Control Register | KUPIC | XXXXX000b |
| 004Eh | | | |
| 004Fh | SSU/IIC Interrupt Control Register ⁽²⁾ | SSUIC / IICIC | XXXXX000b |
| 0050h | Compare 1 Interrupt Control Register | CMP1IC | XXXXX000b |
| 0051h | UART0 Transmit Interrupt Control Register | S0TIC | XXXXX000b |
| 0052h | UART0 Receive Interrupt Control Register | S0RIC | XXXXX000b |
| 0053h | UART1 Transmit Interrupt Control Register | S1TIC | XXXXX000b |
| 0054h | UART1 Receive Interrupt Control Register | S1RIC | XXXXX000b |
| 0055h | INT2 Interrupt Control Register | INT2IC | XX00X000b |
| 0056h | Timer RA Interrupt Control Register | TRAIC | XXXXX000b |
| 0057h | | | |
| 0058h | Timer RB Interrupt Control Register | TRBIC | XXXXX000b |
| 0059h | INT1 Interrupt Control Register | INT1IC | XX00X000b |
| 005Ah | INT3 Interrupt Control Register | INT3IC | XX00X000b |
| 005Bh | Timer RF Interrupt Control Register | TRFIC | XXXXX000b |
| 005Ch | Compare 0 Interrupt Control Register | CMP0IC | XXXXX000b |
| 005Dh | INT0 Interrupt Control Register | INT0IC | XX00X000b |
| 005Eh | A/D Conversion Interrupt Control Register | ADIC | XXXXX000b |
| 005Fh | Capture Interrupt Control Register | CAPIC | XXXXX000b |
| 0060h | | | |
| 0061h | | | |
| 0062h | | | |
| 0063h | | | |
| 0064h | | | |
| 0065h | | | |
| 0066h | | | |
| 0067h | | | |
| 0068h | | | |
| 0069h | | | |
| 006Ah | | | |
| 006Bh | | | |
| 006Ch | | | |
| 006Dh | | | |
| 006Eh | | | |
| 006Fh | | | |
| 0070h | | | |
| 0071h | | | |
| 0072h | | | |
| 0073h | | | |
| 0074h | | | |
| 0075h | | | |
| 0076h | | | |
| 0077h | | | |
| 0078h | | | |
| 0079h | | | |
| 007Ah | | | |
| 007Bh | | | |
| 007Ch | | | |
| 007Dh | | | |
| 007Eh | | | |
| 007Fh | | | |

X: Undefined

NOTES:

1. The blank regions are reserved. Do not access locations in these regions.
2. Selected by the IICSEL bit in the PMR register.

Table 4.3 SFR Information (3)⁽¹⁾

| Address | Register | Symbol | After reset |
|---------|---|---------------|-----------------|
| 0080h | | | |
| 0081h | | | |
| 0082h | | | |
| 0083h | | | |
| 0084h | | | |
| 0085h | | | |
| 0086h | | | |
| 0087h | | | |
| 0088h | | | |
| 0089h | | | |
| 008Ah | | | |
| 008Bh | | | |
| 008Ch | | | |
| 008Dh | | | |
| 008Eh | | | |
| 008Fh | | | |
| 0090h | | | |
| 0091h | | | |
| 0092h | | | |
| 0093h | | | |
| 0094h | | | |
| 0095h | | | |
| 0096h | | | |
| 0097h | | | |
| 0098h | | | |
| 0099h | | | |
| 009Ah | | | |
| 009Bh | | | |
| 009Ch | | | |
| 009Dh | | | |
| 009Eh | | | |
| 009Fh | | | |
| 00A0h | UART0 Transmit/Receive Mode Register | U0MR | 00h |
| 00A1h | UART0 Bit Rate Register | U0BRG | XXh |
| 00A2h | UART0 Transmit Buffer Register | U0TB | XXh |
| 00A3h | | | XXh |
| 00A4h | UART0 Transmit/Receive Control Register 0 | U0C0 | 00001000b |
| 00A5h | UART0 Transmit/Receive Control Register 1 | U0C1 | 00000010b |
| 00A6h | UART0 Receive Buffer Register | U0RB | XXh |
| 00A7h | | | XXh |
| 00A8h | UART1 Transmit/Receive Mode Register | U1MR | 00h |
| 00A9h | UART1 Bit Rate Register | U1BRG | XXh |
| 00AAh | UART1 Transmit Buffer Register | U1TB | XXh |
| 00ABh | | | XXh |
| 00ACh | UART1 Transmit/Receive Control Register 0 | U1C0 | 00001000b |
| 00ADh | UART1 Transmit/Receive Control Register 1 | U1C1 | 00000010b |
| 00AEh | UART1 Receive Buffer Register | U1RB | XXh |
| 00AFh | | | XXh |
| 00B0h | | | |
| 00B1h | | | |
| 00B2h | | | |
| 00B3h | | | |
| 00B4h | | | |
| 00B5h | | | |
| 00B6h | | | |
| 00B7h | | | |
| 00B8h | SS Control Register H / IIC bus Control Register 1 ⁽²⁾ | SSCRH / ICCR1 | 00h |
| 00B9h | SS Control Register L / IIC bus Control Register 2 ⁽²⁾ | SSCRL / ICCR2 | 01111101b |
| 00BAh | SS Mode Register / IIC bus Mode Register ⁽²⁾ | SSMR / ICMR | 00011000b |
| 00BBh | SS Enable Register / IIC bus Interrupt Enable Register ⁽²⁾ | SSER / ICIER | 00h |
| 00BCh | SS Status Register / IIC bus Status Register ⁽²⁾ | SSSR / ICSR | 00h / 0000X000b |
| 00BDh | SS Mode Register 2 / Slave Address Register ⁽²⁾ | SSMR2 / SAR | 00h |
| 00BEh | SS Transmit Data Register / IIC bus Transmit Data Register ⁽²⁾ | SSTDR / ICDRT | FFh |
| 00BFh | SS Receive Data Register / IIC bus Receive Data Register ⁽²⁾ | SSRDR / ICDRR | FFh |

X: Undefined

NOTES:

1. The blank regions are reserved. Do not access locations in these regions.
2. Selected by the IICSEL bit in the PMR register.

Table 4.4 SFR Information (4)⁽¹⁾

| Address | Register | Symbol | After reset |
|---------|---|--------|-------------|
| 00C0h | | | |
| 00C1h | | | |
| 00C2h | | | |
| 00C3h | | | |
| 00C4h | | | |
| 00C5h | | | |
| 00C6h | | | |
| 00C7h | | | |
| 00C8h | | | |
| 00C9h | | | |
| 00CAh | | | |
| 00CBh | | | |
| 00CCh | | | |
| 00CDh | | | |
| 00CEh | | | |
| 00CFh | | | |
| 00D0h | | | |
| 00D1h | | | |
| 00D2h | | | |
| 00D3h | | | |
| 00D4h | | | |
| 00D5h | | | |
| 00D6h | | | |
| 00D7h | | | |
| 00D8h | D/A Register 0 | DA0 | 00h |
| 00D9h | | | |
| 00DAh | D/A Register 1 | DA1 | 00h |
| 00DBh | | | |
| 00DCh | D/A Control Register | DACON | 00h |
| 00DDh | | | |
| 00DEh | | | |
| 00DFh | | | |
| 00E0h | Port P0 Register | P0 | XXh |
| 00E1h | Port P1 Register | P1 | XXh |
| 00E2h | Port P0 Direction Register | PD0 | 00h |
| 00E3h | Port P1 Direction Register | PD1 | 00h |
| 00E4h | Port P2 Register | P2 | XXh |
| 00E5h | Port P3 Register | P3 | XXh |
| 00E6h | Port P2 Direction Register | PD2 | 00h |
| 00E7h | Port P3 Direction Register | PD3 | 00h |
| 00E8h | Port P4 Register | P4 | XXh |
| 00E9h | Port P5 Register | P5 | XXh |
| 00EAh | Port P4 Direction Register | PD4 | 00h |
| 00EBh | Port P5 Direction Register | PD5 | 00h |
| 00ECh | Port P6 Register | P6 | XXh |
| 00EDh | | | |
| 00EEh | Port P6 Direction Register | PD6 | 00h |
| 00EFh | | | |
| 00F0h | | | |
| 00F1h | | | |
| 00F2h | | | |
| 00F3h | | | |
| 00F4h | Port P2 Drive Capacity Control Register | P2DRR | 00h |
| 00F5h | UART1 Function Select Register | U1SR | 000000XXb |
| 00F6h | | | |
| 00F7h | | | |
| 00F8h | Port Mode Register | PMR | 00h |
| 00F9h | External Input Enable Register | INTEN | 00h |
| 00FAh | INT Input Filter Select Register | INTF | 00h |
| 00FBh | Key Input Enable Register | KIEN | 00h |
| 00FCh | Pull-Up Control Register 0 | PUR0 | 00h |
| 00FDh | Pull-Up Control Register 1 | PUR1 | XX000000b |
| 00FEh | | | |
| 00FFh | | | |

X: Undefined

NOTE:

1. The blank regions are reserved. Do not access locations in these regions.

Table 4.5 SFR Information (5)(1)

| Address | Register | Symbol | After reset |
|---------|---|---------|-------------|
| 0100h | Timer RA Control Register | TRACR | 00h |
| 0101h | Timer RA I/O Control Register | TRAIOC | 00h |
| 0102h | Timer RA Mode Register | TRAMR | 00h |
| 0103h | Timer RA Prescaler Register | TRAPRE | FFh |
| 0104h | Timer RA Register | TRA | FFh |
| 0105h | LIN Control Register 2 | LINCR2 | 00h |
| 0106h | LIN Control Register | LINCR | 00h |
| 0107h | LIN Status Register | LINST | 00h |
| 0108h | Timer RB Control Register | TRBCR | 00h |
| 0109h | Timer RB One-Shot Control Register | TRBOCR | 00h |
| 010Ah | Timer RB I/O Control Register | TRBIOC | 00h |
| 010Bh | Timer RB Mode Register | TRBMR | 00h |
| 010Ch | Timer RB Prescaler Register | TRBPRE | FFh |
| 010Dh | Timer RB Secondary Register | TRBSC | FFh |
| 010Eh | Timer RB Primary Register | TRBPR | FFh |
| 010Fh | | | |
| 0110h | | | |
| 0111h | | | |
| 0112h | | | |
| 0113h | | | |
| 0114h | | | |
| 0115h | | | |
| 0116h | | | |
| 0117h | | | |
| 0118h | Timer RE Second Data Register / Counter Data Register | TRESEC | 00h |
| 0119h | Timer RE Minute Data Register / Compare Data Register | TREMIN | 00h |
| 011Ah | Timer RE Hour Data Register | TREHR | 00h |
| 011Bh | Timer RE Day of Week Data Register | TREWK | 00h |
| 011Ch | Timer RE Control Register 1 | TRECR1 | 00h |
| 011Dh | Timer RE Control Register 2 | TRECR2 | 00h |
| 011Eh | Timer RE Clock Source Select Register | TRECSR | 00001000b |
| 011Fh | | | |
| 0120h | Timer RC Mode Register | TRCMR | 01001000b |
| 0121h | Timer RC Control Register 1 | TRCCR1 | 00h |
| 0122h | Timer RC Interrupt Enable Register | TRCIER | 01110000b |
| 0123h | Timer RC Status Register | TRCSR | 01110000b |
| 0124h | Timer RC I/O Control Register 0 | TRCIOR0 | 10001000b |
| 0125h | Timer RC I/O Control Register 1 | TRCIOR1 | 10001000b |
| 0126h | Timer RC Counter | TRC | 00h |
| 0127h | | | 00h |
| 0128h | Timer RC General Register A | TRCGRA | FFh |
| 0129h | | | FFh |
| 012Ah | Timer RC General Register B | TRCGRB | FFh |
| 012Bh | | | FFh |
| 012Ch | Timer RC General Register C | TRCGRC | FFh |
| 012Dh | | | FFh |
| 012Eh | Timer RC General Register D | TRCGRD | FFh |
| 012Fh | | | FFh |
| 0130h | Timer RC Control Register 2 | TRCCR2 | 00011111b |
| 0131h | Timer RC Digital Filter Function Select Register | TRCDF | 00h |
| 0132h | Timer RC Output Master Enable Register | TRCOER | 01111111b |
| 0133h | | | |
| 0134h | | | |
| 0135h | | | |
| 0136h | | | |
| 0137h | Timer RD Start Register | TRDSTR | 1111100b |
| 0138h | Timer RD Mode Register | TRDMR | 00001110b |
| 0139h | Timer RD PWM Mode Register | TRDPMR | 10001000b |
| 013Ah | Timer RD Function Control Register | TRDFCR | 10000000b |
| 013Bh | Timer RD Output Master Enable Register 1 | TRDOER1 | FFh |
| 013Ch | Timer RD Output Master Enable Register 2 | TRDOER2 | 01111111b |
| 013Dh | Timer RD Output Control Register | TRDOCR | 00h |
| 013Eh | Timer RD Digital Filter Function Select Register 0 | TRDDF0 | 00h |
| 013Fh | Timer RD Digital Filter Function Select Register 1 | TRDDF1 | 00h |

NOTE:

1. The blank regions are reserved. Do not access locations in these regions

Table 4.6 SFR Information (6)(1)

| Address | Register | Symbol | After reset |
|---------|---|----------|-------------|
| 0140h | Timer RD Control Register 0 | TRDCR0 | 00h |
| 0141h | Timer RD I/O Control Register A0 | TRDIORA0 | 10001000b |
| 0142h | Timer RD I/O Control Register C0 | TRDIORC0 | 10001000b |
| 0143h | Timer RD Status Register 0 | TRDSR0 | 11000000b |
| 0144h | Timer RD Interrupt Enable Register 0 | TRDIER0 | 11100000b |
| 0145h | Timer RD PWM Mode Output Level Control Register 0 | TRDPOCR0 | 11111000b |
| 0146h | Timer RD Counter 0 | TRD0 | 00h |
| 0147h | | | 00h |
| 0148h | Timer RD General Register A0 | TRDGRA0 | FFh |
| 0149h | | | FFh |
| 014Ah | Timer RD General Register B0 | TRDGRB0 | FFh |
| 014Bh | | | FFh |
| 014Ch | Timer RD General Register C0 | TRDGRC0 | FFh |
| 014Dh | | | FFh |
| 014Eh | Timer RD General Register D0 | TRDGRD0 | FFh |
| 014Fh | | | FFh |
| 0150h | Timer RD Control Register 1 | TRDCR1 | 00h |
| 0151h | Timer RD I/O Control Register A1 | TRDIORA1 | 10001000b |
| 0152h | Timer RD I/O Control Register C1 | TRDIORC1 | 10001000b |
| 0153h | Timer RD Status Register 1 | TRDSR1 | 11000000b |
| 0154h | Timer RD Interrupt Enable Register 1 | TRDIER1 | 11100000b |
| 0155h | Timer RD PWM Mode Output Level Control Register 1 | TRDPOCR1 | 11111000b |
| 0156h | Timer RD Counter 1 | TRD1 | 00h |
| 0157h | | | 00h |
| 0158h | Timer RD General Register A1 | TRDGRA1 | FFh |
| 0159h | | | FFh |
| 015Ah | Timer RD General Register B1 | TRDGRB1 | FFh |
| 015Bh | | | FFh |
| 015Ch | Timer RD General Register C1 | TRDGRC1 | FFh |
| 015Dh | | | FFh |
| 015Eh | Timer RD General Register D1 | TRDGRD1 | FFh |
| 015Fh | | | FFh |
| 0160h | UART2 Transmit/Receive Mode Register | U2MR | 00h |
| 0161h | UART2 Bit Rate Register | U2BRG | XXh |
| 0162h | UART2 Transmit Buffer Register | U2TB | XXh |
| 0163h | | | XXh |
| 0164h | UART2 Transmit/Receive Control Register 0 | U2C0 | 00001000b |
| 0165h | UART2 Transmit/Receive Control Register 1 | U2C1 | 00000010b |
| 0166h | UART2 Receive Buffer Register | U2RB | XXh |
| 0167h | | | XXh |
| 0168h | | | |
| 0169h | | | |
| 016Ah | | | |
| 016Bh | | | |
| 016Ch | | | |
| 016Dh | | | |
| 016Eh | | | |
| 016Fh | | | |
| 0170h | | | |
| 0171h | | | |
| 0172h | | | |
| 0173h | | | |
| 0174h | | | |
| 0175h | | | |
| 0176h | | | |
| 0177h | | | |
| 0178h | | | |
| 0179h | | | |
| 017Ah | | | |
| 017Bh | | | |
| 017Ch | | | |
| 017Dh | | | |
| 017Eh | | | |
| 017Fh | | | |

X: Undefined

NOTE:

1. The blank regions are reserved. Do not access locations in these regions.

Table 4.7 SFR Information (7)(1)

| Address | Register | Symbol | After reset |
|---------|---------------------------------|--------|-------------|
| 0180h | | | |
| 0181h | | | |
| 0182h | | | |
| 0183h | | | |
| 0184h | | | |
| 0185h | | | |
| 0186h | | | |
| 0187h | | | |
| 0188h | | | |
| 0189h | | | |
| 018Ah | | | |
| 018Bh | | | |
| 018Ch | | | |
| 018Dh | | | |
| 018Eh | | | |
| 018Fh | | | |
| 0190h | | | |
| 0191h | | | |
| 0192h | | | |
| 0193h | | | |
| 0194h | | | |
| 0195h | | | |
| 0196h | | | |
| 0197h | | | |
| 0198h | | | |
| 0199h | | | |
| 019Ah | | | |
| 019Bh | | | |
| 019Ch | | | |
| 019Dh | | | |
| 019Eh | | | |
| 019Fh | | | |
| 01A0h | | | |
| 01A1h | | | |
| 01A2h | | | |
| 01A3h | | | |
| 01A4h | | | |
| 01A5h | | | |
| 01A6h | | | |
| 01A7h | | | |
| 01A8h | | | |
| 01A9h | | | |
| 01AAh | | | |
| 01ABh | | | |
| 01ACh | | | |
| 01ADh | | | |
| 01AEh | | | |
| 01AFh | | | |
| 01B0h | | | |
| 01B1h | | | |
| 01B2h | | | |
| 01B3h | Flash Memory Control Register 4 | FMR4 | 01000000b |
| 01B4h | | | |
| 01B5h | Flash Memory Control Register 1 | FMR1 | 1000000Xb |
| 01B6h | | | |
| 01B7h | Flash Memory Control Register 0 | FMR0 | 00000001b |
| 01B8h | | | |
| 01B9h | | | |
| 01BAh | | | |
| 01BBh | | | |
| 01BCh | | | |
| 01BDh | | | |
| 01BEh | | | |
| 01BFh | | | |

X: Undefined

NOTE:

1. The blank regions are reserved. Do not access locations in these regions.

Table 4.8 SFR Information (8)(1)

| Address | Register | Symbol | After reset |
|---------|----------|--------|-------------|
| 01C0h | | | |
| 01C1h | | | |
| 01C2h | | | |
| 01C3h | | | |
| 01C4h | | | |
| 01C5h | | | |
| 01C6h | | | |
| 01C7h | | | |
| 01C8h | | | |
| 01C9h | | | |
| 01CAh | | | |
| 01CBh | | | |
| 01CCh | | | |
| 01CDh | | | |
| 01CEh | | | |
| 01CFh | | | |
| 01D0h | | | |
| 01D1h | | | |
| 01D2h | | | |
| 01D3h | | | |
| 01D4h | | | |
| 01D5h | | | |
| 01D6h | | | |
| 01D7h | | | |
| 01D8h | | | |
| 01D9h | | | |
| 01DAh | | | |
| 01DBh | | | |
| 01DCh | | | |
| 01DDh | | | |
| 01DEh | | | |
| 01DFh | | | |
| 01E0h | | | |
| 01E1h | | | |
| 01E2h | | | |
| 01E3h | | | |
| 01E4h | | | |
| 01E5h | | | |
| 01E6h | | | |
| 01E7h | | | |
| 01E8h | | | |
| 01E9h | | | |
| 01EAh | | | |
| 01EBh | | | |
| 01ECh | | | |
| 01EDh | | | |
| 01EEh | | | |
| 01EFh | | | |
| 01F0h | | | |
| 01F1h | | | |
| 01F2h | | | |
| 01F3h | | | |
| 01F4h | | | |
| 01F5h | | | |
| 01F6h | | | |
| 01F7h | | | |
| 01F8h | | | |
| 01F9h | | | |
| 01FAh | | | |
| 01FBh | | | |
| 01FCh | | | |
| 01FDh | | | |
| 01FEh | | | |
| 01FFh | | | |

NOTE:
 1. The blank regions are reserved. Do not access locations in these regions.

Table 4.9 SFR Information (9)⁽¹⁾

| Address | Register | Symbol | After reset |
|---------|----------|--------|-------------|
| 0200h | | | |
| 0201h | | | |
| 0202h | | | |
| 0203h | | | |
| 0204h | | | |
| 0205h | | | |
| 0206h | | | |
| 0207h | | | |
| 0208h | | | |
| 0209h | | | |
| 020Ah | | | |
| 020Bh | | | |
| 020Ch | | | |
| 020Dh | | | |
| 020Eh | | | |
| 020Fh | | | |
| 0210h | | | |
| 0211h | | | |
| 0212h | | | |
| 0213h | | | |
| 0214h | | | |
| 0215h | | | |
| 0216h | | | |
| 0217h | | | |
| 0218h | | | |
| 0219h | | | |
| 021Ah | | | |
| 021Bh | | | |
| 021Ch | | | |
| 021Dh | | | |
| 021Eh | | | |
| 021Fh | | | |
| 0220h | | | |
| 0221h | | | |
| 0222h | | | |
| 0223h | | | |
| 0224h | | | |
| 0225h | | | |
| 0226h | | | |
| 0227h | | | |
| 0228h | | | |
| 0229h | | | |
| 022Ah | | | |
| 022Bh | | | |
| 022Ch | | | |
| 022Dh | | | |
| 022Eh | | | |
| 022Fh | | | |
| 0230h | | | |
| 0231h | | | |
| 0232h | | | |
| 0233h | | | |
| 0234h | | | |
| 0235h | | | |
| 0236h | | | |
| 0237h | | | |
| 0238h | | | |
| 0239h | | | |
| 023Ah | | | |
| 023Bh | | | |
| 023Ch | | | |
| 023Dh | | | |
| 023Eh | | | |
| 023Fh | | | |

NOTE:
 1. The blank regions are reserved. Do not access locations in these regions.

Table 4.10 SFR Information (10)(1)

| Address | Register | Symbol | After reset |
|---------|----------|--------|-------------|
| 0240h | | | |
| 0241h | | | |
| 0242h | | | |
| 0243h | | | |
| 0244h | | | |
| 0245h | | | |
| 0246h | | | |
| 0247h | | | |
| 0248h | | | |
| 0249h | | | |
| 024Ah | | | |
| 024Bh | | | |
| 024Ch | | | |
| 024Dh | | | |
| 024Eh | | | |
| 024Fh | | | |
| 0250h | | | |
| 0251h | | | |
| 0252h | | | |
| 0253h | | | |
| 0254h | | | |
| 0255h | | | |
| 0256h | | | |
| 0257h | | | |
| 0258h | | | |
| 0259h | | | |
| 025Ah | | | |
| 025Bh | | | |
| 025Ch | | | |
| 025Dh | | | |
| 025Eh | | | |
| 025Fh | | | |
| 0260h | | | |
| 0261h | | | |
| 0262h | | | |
| 0263h | | | |
| 0264h | | | |
| 0265h | | | |
| 0266h | | | |
| 0267h | | | |
| 0268h | | | |
| 0269h | | | |
| 026Ah | | | |
| 026Bh | | | |
| 026Ch | | | |
| 026Dh | | | |
| 026Eh | | | |
| 026Fh | | | |
| 0270h | | | |
| 0271h | | | |
| 0272h | | | |
| 0273h | | | |
| 0274h | | | |
| 0275h | | | |
| 0276h | | | |
| 0277h | | | |
| 0278h | | | |
| 0279h | | | |
| 027Ah | | | |
| 027Bh | | | |
| 027Ch | | | |
| 027Dh | | | |
| 027Eh | | | |
| 027Fh | | | |

NOTE:
 1. The blank regions are reserved. Do not access locations in these regions.

Table 4.11 SFR Information (11)(1)

| Address | Register | Symbol | After reset |
|---------|------------------------------|--------|----------------------|
| 0280h | | | |
| 0281h | | | |
| 0282h | | | |
| 0283h | | | |
| 0284h | | | |
| 0285h | | | |
| 0286h | | | |
| 0287h | | | |
| 0288h | | | |
| 0289h | | | |
| 028Ah | | | |
| 028Bh | | | |
| 028Ch | | | |
| 028Dh | | | |
| 028Eh | | | |
| 028Fh | | | |
| 0290h | Timer RF Register | TRF | 00h |
| 0291h | | | 00h |
| 0292h | | | |
| 0293h | | | |
| 0294h | | | |
| 0295h | | | |
| 0296h | | | |
| 0297h | | | |
| 0298h | | | |
| 0299h | | | |
| 029Ah | Timer RF Control Register 0 | TRFCR0 | 00h |
| 029Bh | Timer RF Control Register 1 | TRFCR1 | 00h |
| 029Ch | Capture / Compare 0 Register | TRFM0 | 0000h ⁽²⁾ |
| 029Dh | | | FFFFh ⁽³⁾ |
| 029Eh | Compare 1 Register | TRFM1 | FFh |
| 029Fh | | | FFh |
| 02A0h | | | |
| 02A1h | | | |
| 02A2h | | | |
| 02A3h | | | |
| 02A4h | | | |
| 02A5h | | | |
| 02A6h | | | |
| 02A7h | | | |
| 02A8h | | | |
| 02A9h | | | |
| 02AAh | | | |
| 02ABh | | | |
| 02ACh | | | |
| 02ADh | | | |
| 02AEh | | | |
| 02AFh | | | |
| 02B0h | | | |
| 02B1h | | | |
| 02B2h | | | |
| 02B3h | | | |
| 02B4h | | | |
| 02B5h | | | |
| 02B6h | | | |
| 02B7h | | | |
| 02B8h | | | |
| 02B9h | | | |
| 02BAh | | | |
| 02BBh | | | |
| 02BCh | | | |
| 02BDh | | | |
| 02BEh | | | |
| 02BFh | | | |

NOTES:

1. The blank regions are reserved. Do not access locations in these regions.
2. After input capture mode.
3. After output compare mode.

Table 4.12 SFR Information (12)(1)

| Address | Register | Symbol | After reset |
|---------|----------------------------------|--------|-------------|
| 02C0h | A/D Register 0 | AD0 | XXh |
| 02C1h | | | XXh |
| 02C2h | | | |
| 02C3h | | | |
| 02C4h | | | |
| 02C5h | | | |
| 02C6h | | | |
| 02C7h | | | |
| 02C8h | | | |
| 02C9h | | | |
| 02CAh | | | |
| 02CBh | | | |
| 02CCh | | | |
| 02CDh | | | |
| 02CEh | | | |
| 02CFh | | | |
| 02D0h | | | |
| 02D1h | | | |
| 02D2h | | | |
| 02D3h | | | |
| 02D4h | A/D Control Register 2 | ADCON2 | 00001000b |
| 02D5h | | | |
| 02D6h | A/D Control Register 0 | ADCON0 | 00000011b |
| 02D7h | A/D Control Register 1 | ADCON1 | 00h |
| 02D8h | | | |
| 02D9h | | | |
| 02DAh | | | |
| 02DBh | | | |
| 02DCh | | | |
| 02DDh | | | |
| 02DEh | | | |
| 02DFh | | | |
| 02E0h | | | |
| 02E1h | | | |
| 02E2h | | | |
| 02E3h | | | |
| 02E4h | Port P8 Direction Register | PD8 | 00h |
| 02E5h | | | |
| 02E6h | Port P8 Register | P8 | XXh |
| 02E7h | | | |
| 02E8h | | | |
| 02E9h | | | |
| 02EAh | | | |
| 02EBh | | | |
| 02ECh | | | |
| 02EDh | | | |
| 02EEh | | | |
| 02EFh | | | |
| 02F0h | | | |
| 02F1h | | | |
| 02F2h | | | |
| 02F3h | | | |
| 02F4h | | | |
| 02F5h | | | |
| 02F6h | | | |
| 02F7h | | | |
| 02F8h | | | |
| 02F9h | | | |
| 02FAh | | | |
| 02FBh | | | |
| 02FCh | Pull-Up Control Register 2 | PUR2 | XXX00000b |
| 02FDh | | | |
| 02FEh | | | |
| 02FFh | Timer RF Output Control Register | TRFOUT | 00h |
| FFFFh | Option Function Select Register | OFS | (Note 2) |

X: Undefined

NOTES:

1. The blank regions are reserved. Do not access locations in these regions.
2. The OFS register cannot be changed by a program. Use a flash programmer to write to it.

5. Electrical Characteristics

The electrical characteristics of N version ($T_{opr} = -20^{\circ}\text{C}$ to 85°C) and D version ($T_{opr} = -40^{\circ}\text{C}$ to 85°C) are listed below.

Please contact Renesas Technology sales offices for the electrical characteristics in the Y version ($T_{opr} = -20^{\circ}\text{C}$ to 105°C).

Table 5.1 Absolute Maximum Ratings

| Symbol | Parameter | Condition | Rated Value | Unit |
|------------------|-------------------------------|--------------------------------|--|--------------------|
| V_{cc}/AV_{cc} | Supply voltage | | -0.3 to 6.5 | V |
| V_i | Input voltage | | -0.3 to $V_{cc} + 0.3$ | V |
| V_o | Output voltage | | -0.3 to $V_{cc} + 0.3$ | V |
| P_d | Power dissipation | $T_{opr} = 25^{\circ}\text{C}$ | 700 | mW |
| T_{opr} | Operating ambient temperature | | -20 to 85 (N version) / -40 to 85 (D version) | $^{\circ}\text{C}$ |
| T_{stg} | Storage temperature | | -65 to 150 | $^{\circ}\text{C}$ |

Table 5.2 Recommended Operating Conditions

| Symbol | Parameter | | Conditions | Standard | | | Unit | | |
|--|--|--|---------------------------------|--------------------------------|---------------------------------|---------------------|------|----|-----|
| | | | | Min. | Typ. | Max. | | | |
| V _{CC} /AV _{CC} | Supply voltage | | | 2.2 | – | 5.5 | V | | |
| V _{SS} /AV _{SS} | Supply voltage | | | – | 0 | – | V | | |
| V _{IH} | Input “H” voltage | | | 0.8 V _{CC} | – | V _{CC} | V | | |
| V _{IL} | Input “L” voltage | | | 0 | – | 0.2 V _{CC} | V | | |
| I _{OH} (sum) | Peak sum output “H” current | Sum of all pins I _{OH} (peak) | | – | – | –240 | mA | | |
| I _{OH} (sum) | Average sum output “H” current | Sum of all pins I _{OH} (avg) | | – | – | –120 | mA | | |
| I _{OH} (peak) | Peak output “H” current | Except P2_0 to P2_7 | | – | – | –10 | mA | | |
| | | P2_0 to P2_7 | | – | – | –40 | mA | | |
| I _{OH} (avg) | Average output “H” current | Except P2_0 to P2_7 | | – | – | –5 | mA | | |
| | | P2_0 to P2_7 | | – | – | –20 | mA | | |
| I _{OL} (sum) | Peak sum output “L” current | Sum of all pins I _{OL} (peak) | | – | – | 240 | mA | | |
| I _{OL} (sum) | Average sum output “L” current | Sum of all pins I _{OL} (avg) | | – | – | 120 | mA | | |
| I _{OL} (peak) | Peak output “L” current | Except P2_0 to P2_7 | | – | – | 10 | mA | | |
| | | P2_0 to P2_7 | | – | – | 40 | mA | | |
| I _{OL} (avg) | Average output “L” current | Except P2_0 to P2_7 | | – | – | 5 | mA | | |
| | | P2_0 to P2_7 | | – | – | 20 | mA | | |
| f _(XIN) | XIN clock input oscillation frequency | | 3.0 V ≤ V _{CC} ≤ 5.5 V | 0 | – | 20 | MHz | | |
| | | | 2.7 V ≤ V _{CC} < 3.0 V | 0 | – | 10 | MHz | | |
| | | | 2.2 V ≤ V _{CC} < 2.7 V | 0 | – | 5 | MHz | | |
| f _(XCIN) | XCIN clock input oscillation frequency | | 2.2 V ≤ V _{CC} ≤ 5.5 V | 0 | – | 70 | kHz | | |
| | | | System clock | OCD2 = 0 XIN clock selected | 3.0 V ≤ V _{CC} ≤ 5.5 V | 0 | – | 20 | MHz |
| | | | | | 2.7 V ≤ V _{CC} < 3.0 V | 0 | – | 10 | MHz |
| 2.2 V ≤ V _{CC} < 2.7 V | 0 | – | | | 5 | MHz | | | |
| OCD2 = 1 On-chip oscillator clock selected | FRA01 = 0 Low-speed on-chip oscillator clock selected | – | | 125 | – | kHz | | | |
| | FRA01 = 1 High-speed on-chip oscillator clock selected 3.0 V ≤ V _{CC} ≤ 5.5 V | – | | – | 20 | MHz | | | |
| | FRA01 = 1 High-speed on-chip oscillator clock selected 2.7 V ≤ V _{CC} ≤ 5.5 V | – | | – | 10 | MHz | | | |
| FRA01 = 1 High-speed on-chip oscillator clock selected 2.2 V ≤ V _{CC} ≤ 5.5 V | – | – | 5 | MHz | | | | | |

NOTES:

- V_{CC} = 2.2 to 5.5 V at T_{opr} = -20 to 85°C (N version) / -40 to 85°C (D version), unless otherwise specified.
- The average output current indicates the average value of current measured during 100 ms.

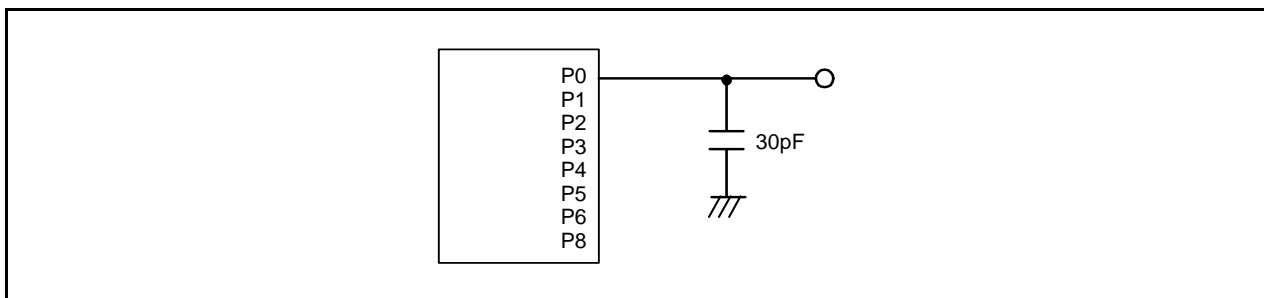
**Figure 5.1 Ports P0 to P6, P8 Timing Measurement Circuit**

Table 5.3 A/D Converter Characteristics(1)

| Symbol | Parameter | | Conditions | Standard | | | Unit |
|--------------|-------------------------------|-------------------------|---|----------|------|-----------|---------------|
| | | | | Min. | Typ. | Max. | |
| – | Resolution | | $V_{ref} = AV_{CC}$ | – | – | 10 | Bit |
| – | Absolute accuracy | 10-bit mode | $\phi_{AD} = 10 \text{ MHz}, V_{ref} = AV_{CC} = 5.0 \text{ V}$ | – | – | ± 3 | LSB |
| | | 8-bit mode | $\phi_{AD} = 10 \text{ MHz}, V_{ref} = AV_{CC} = 5.0 \text{ V}$ | – | – | ± 2 | LSB |
| | | 10-bit mode | $\phi_{AD} = 10 \text{ MHz}, V_{ref} = AV_{CC} = 3.3 \text{ V}$ | – | – | ± 5 | LSB |
| | | 8-bit mode | $\phi_{AD} = 10 \text{ MHz}, V_{ref} = AV_{CC} = 3.3 \text{ V}$ | – | – | ± 2 | LSB |
| | | 10-bit mode | $\phi_{AD} = 5 \text{ MHz}, V_{ref} = AV_{CC} = 2.2 \text{ V}$ | – | – | ± 5 | LSB |
| | | 8-bit mode | $\phi_{AD} = 5 \text{ MHz}, V_{ref} = AV_{CC} = 2.2 \text{ V}$ | – | – | ± 2 | LSB |
| R_{ladder} | Resistor ladder | | $V_{ref} = AV_{CC}$ | 10 | – | 40 | $k\Omega$ |
| t_{conv} | Conversion time | 10-bit mode | $\phi_{AD} = 10 \text{ MHz}, V_{ref} = AV_{CC} = 5.0 \text{ V}$ | 3.3 | – | – | μs |
| | | 8-bit mode | $\phi_{AD} = 10 \text{ MHz}, V_{ref} = AV_{CC} = 5.0 \text{ V}$ | 2.8 | – | – | μs |
| V_{ref} | Reference voltage | | | 2.2 | – | AV_{CC} | V |
| V_{IA} | Analog input voltage(2) | | | 0 | – | AV_{CC} | V |
| – | A/D operating clock frequency | Without sample and hold | $V_{ref} = AV_{CC} = 2.7 \text{ to } 5.5 \text{ V}$ | 0.25 | – | 10 | MHz |
| | | With sample and hold | $V_{ref} = AV_{CC} = 2.7 \text{ to } 5.5 \text{ V}$ | 1 | – | 10 | MHz |
| | | Without sample and hold | $V_{ref} = AV_{CC} = 2.2 \text{ to } 5.5 \text{ V}$ | 0.25 | – | 5 | MHz |
| | | With sample and hold | $V_{ref} = AV_{CC} = 2.2 \text{ to } 5.5 \text{ V}$ | 1 | – | 5 | MHz |

NOTES:

- $V_{CC}/AV_{CC} = V_{ref} = 2.2 \text{ to } 5.5 \text{ V}$ at $T_{opr} = -20 \text{ to } 85^\circ\text{C}$ (N version) / $-40 \text{ to } 85^\circ\text{C}$ (D version), unless otherwise specified.
- When the analog input voltage is over the reference voltage, the A/D conversion result will be 3FFh in 10-bit mode and FFh in 8-bit mode.

Table 5.4 D/A Converter Characteristics(1)

| Symbol | Parameter | | Conditions | Standard | | | Unit |
|------------|-------------------------------|--|------------|----------|------|------|---------------|
| | | | | Min. | Typ. | Max. | |
| – | Resolution | | | – | – | 8 | Bit |
| – | Absolute accuracy | | | – | – | 1.0 | % |
| t_{su} | Setup time | | | – | – | 3 | μs |
| R_o | Output resistor | | | 4 | 10 | 20 | $k\Omega$ |
| I_{vref} | Reference power input current | | (NOTE 2) | – | – | 1.5 | mA |

NOTES:

- $V_{CC}/AV_{CC} = V_{ref} = 2.7 \text{ to } 5.5 \text{ V}$ at $T_{opr} = -20 \text{ to } 85^\circ\text{C}$ (N version) / $-40 \text{ to } 85^\circ\text{C}$ (D version), unless otherwise specified.
- This applies when one D/A converter is used and the value of the DAI register ($i = 0$ or 1) for the unused D/A converter is 00h. The resistor ladder of the A/D converter is not included. Also, even if the VCUT bit in the ADCON1 register is set to 0 (V_{REF} not connected), I_{vref} flows into the D/A converters.

Table 5.5 Flash Memory (Program ROM) Electrical Characteristics

| Symbol | Parameter | Conditions | Standard | | | Unit |
|-------------------------|---|----------------------------|----------------------|------|----------------------------|-------|
| | | | Min. | Typ. | Max. | |
| – | Program/erase endurance ⁽²⁾ | R8C/2A Group | 100 ⁽³⁾ | – | – | times |
| | | R8C/2B Group | 1,000 ⁽³⁾ | – | – | times |
| – | Byte program time | | – | 50 | 400 | μs |
| – | Block erase time | | – | 0.4 | 9 | s |
| t _d (SR-SUS) | Time delay from suspend request until suspend | | – | – | 97+CPU clock × 6 cycles | μs |
| – | Interval from erase start/restart until following suspend request | | 650 | – | – | μs |
| – | Interval from program start/restart until following suspend request | | 0 | – | – | ns |
| – | Time from suspend until program/erase restart | | – | – | 3+CPU clock × 4 cycles | μs |
| – | Program, erase voltage | | 2.7 | – | 5.5 | V |
| – | Read voltage | | 2.2 | – | 5.5 | V |
| – | Program, erase temperature | | 0 | – | 60 | °C |
| – | Data hold time ⁽⁷⁾ | Ambient temperature = 55°C | 20 | – | – | year |

NOTES:

- V_{CC} = 2.7 to 5.5 V at T_{opr} = 0 to 60°C, unless otherwise specified.
- Definition of programming/erasure endurance
The programming and erasure endurance is defined on a per-block basis.
If the programming and erasure endurance is n (n = 100 or 10,000), each block can be erased n times. For example, if 1,024 1-byte writes are performed to block A, a 1 Kbyte block, and then the block is erased, the programming/erasure endurance still stands at one.
However, the same address must not be programmed more than once per erase operation (overwriting prohibited).
- Endurance to guarantee all electrical characteristics after program and erase. (1 to Min. value can be guaranteed).
- In a system that executes multiple programming operations, the actual erasure count can be reduced by writing to sequential addresses in turn so that as much of the block as possible is used up before performing an erase operation. For example, when programming groups of 16 bytes, the effective number of rewrites can be minimized by programming up to 128 groups before erasing them all in one operation. It is also advisable to retain data on the erase count of each block and limit the number of erase operations to a certain number.
- If an error occurs during block erase, attempt to execute the clear status register command, then execute the block erase command at least three times until the erase error does not occur.
- Customers desiring program/erase failure rate information should contact their Renesas technical support representative.
- The data hold time includes time that the power supply is off or the clock is not supplied.

Table 5.6 Flash Memory (Data flash Block A, Block B) Electrical Characteristics⁽⁴⁾

| Symbol | Parameter | Conditions | Standard | | | Unit |
|-------------------------|---|-----------------------------|-----------------------|------|----------------------------|-------|
| | | | Min. | Typ. | Max. | |
| – | Program/erase endurance ⁽²⁾ | | 10,000 ⁽³⁾ | – | – | times |
| – | Byte program time (program/erase endurance ≤ 1,000 times) | | – | 50 | 400 | μs |
| – | Byte program time (program/erase endurance > 1,000 times) | | – | 65 | – | μs |
| – | Block erase time (program/erase endurance ≤ 1,000 times) | | – | 0.2 | 9 | s |
| – | Block erase time (program/erase endurance > 1,000 times) | | – | 0.3 | – | s |
| t _d (SR-SUS) | Time delay from suspend request until suspend | | – | – | 97+CPU clock × 6 cycles | μs |
| – | Interval from erase start/restart until following suspend request | | 650 | – | – | μs |
| – | Interval from program start/restart until following suspend request | | 0 | – | – | ns |
| – | Time from suspend until program/erase restart | | – | – | 3+CPU clock × 4 cycles | μs |
| – | Program, erase voltage | | 2.7 | – | 5.5 | V |
| – | Read voltage | | 2.2 | – | 5.5 | V |
| – | Program, erase temperature | | -20 ⁽⁸⁾ | – | 85 | °C |
| – | Data hold time ⁽⁹⁾ | Ambient temperature = 55 °C | 20 | – | – | year |

NOTES:

- V_{CC} = 2.7 to 5.5 V at T_{opr} = -20 to 85°C (N version) / -40 to 85°C (D version), unless otherwise specified.
- Definition of programming/erasure endurance
The programming and erasure endurance is defined on a per-block basis.
If the programming and erasure endurance is n (n = 100 or 10,000), each block can be erased n times. For example, if 1,024 1-byte writes are performed to block A, a 1 Kbyte block, and then the block is erased, the programming/erasure endurance still stands at one.
However, the same address must not be programmed more than once per erase operation (overwriting prohibited).
- Endurance to guarantee all electrical characteristics after program and erase. (1 to Min. value can be guaranteed).
- Standard of block A and block B when program and erase endurance exceeds 1,000 times. Byte program time to 1,000 times is the same as that in program ROM.
- In a system that executes multiple programming operations, the actual erasure count can be reduced by writing to sequential addresses in turn so that as much of the block as possible is used up before performing an erase operation. For example, when programming groups of 16 bytes, the effective number of rewrites can be minimized by programming up to 128 groups before erasing them all in one operation. It is also advisable to retain data on the erase count of each block and limit the number of erase operations to a certain number.
- If an error occurs during block erase, attempt to execute the clear status register command, then execute the block erase command at least three times until the erase error does not occur.
- Customers desiring program/erase failure rate information should contact their Renesas technical support representative.
- 40°C for D version.
- The data hold time includes time that the power supply is off or the clock is not supplied.

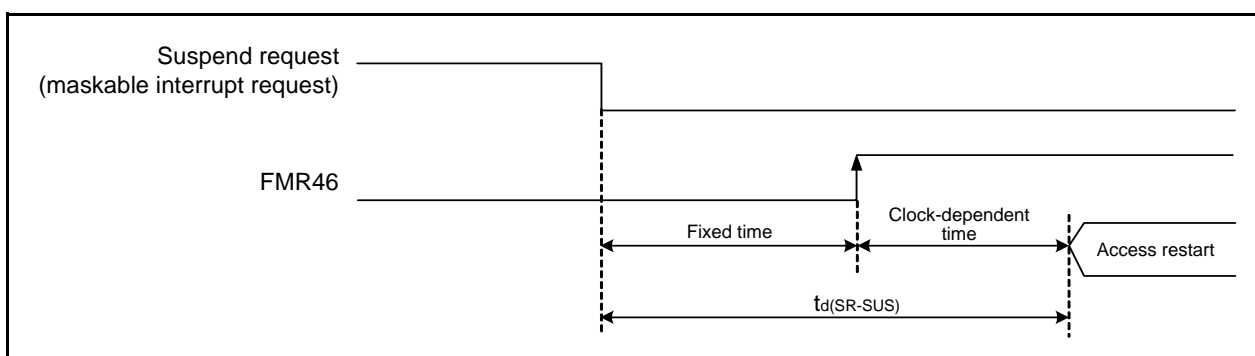


Figure 5.2 Time delay until Suspend

Table 5.7 Voltage Detection 0 Circuit Electrical Characteristics

| Symbol | Parameter | Condition | Standard | | | Unit |
|---------------------|--|------------------------------------|----------|------|------|------|
| | | | Min. | Typ. | Max. | |
| V _{det0} | Voltage detection level | | 2.2 | 2.3 | 2.4 | V |
| – | Voltage detection circuit self power consumption | VCA25 = 1, V _{CC} = 5.0 V | – | 0.9 | – | μA |
| t _{d(E-A)} | Waiting time until voltage detection circuit operation starts ⁽²⁾ | | – | – | 300 | μs |
| V _{ccmin} | MCU operating voltage minimum value | | 2.2 | – | – | V |

NOTES:

1. The measurement condition is V_{CC} = 2.2 V to 5.5 V and T_{opr} = -20 to 85°C (N version) / -40 to 85°C (D version).
2. Necessary time until the voltage detection circuit operates when setting to 1 again after setting the VCA25 bit in the VCA2 register to 0.

Table 5.8 Voltage Detection 1 Circuit Electrical Characteristics

| Symbol | Parameter | Condition | Standard | | | Unit |
|---------------------|--|------------------------------------|----------|------|------|------|
| | | | Min. | Typ. | Max. | |
| V _{det1} | Voltage detection level | | 2.70 | 2.85 | 3.00 | V |
| – | Voltage monitor 1 interrupt request generation time ⁽²⁾ | | – | 40 | – | μs |
| – | Voltage detection circuit self power consumption | VCA26 = 1, V _{CC} = 5.0 V | – | 0.6 | – | μA |
| t _{d(E-A)} | Waiting time until voltage detection circuit operation starts ⁽³⁾ | | – | – | 100 | μs |

NOTES:

1. The measurement condition is V_{CC} = 2.2 V to 5.5 V and T_{opr} = -20 to 85°C (N version) / -40 to 85°C (D version).
2. Time until the voltage monitor 1 interrupt request is generated after the voltage passes V_{det1}.
3. Necessary time until the voltage detection circuit operates when setting to 1 again after setting the VCA26 bit in the VCA2 register to 0.

Table 5.9 Voltage Detection 2 Circuit Electrical Characteristics

| Symbol | Parameter | Condition | Standard | | | Unit |
|---------------------|--|------------------------------------|----------|------|------|------|
| | | | Min. | Typ. | Max. | |
| V _{det2} | Voltage detection level | | 3.3 | 3.6 | 3.9 | V |
| – | Voltage monitor 2 interrupt request generation time ⁽²⁾ | | – | 40 | – | μs |
| – | Voltage detection circuit self power consumption | VCA27 = 1, V _{CC} = 5.0 V | – | 0.6 | – | μA |
| t _{d(E-A)} | Waiting time until voltage detection circuit operation starts ⁽³⁾ | | – | – | 100 | μs |

NOTES:

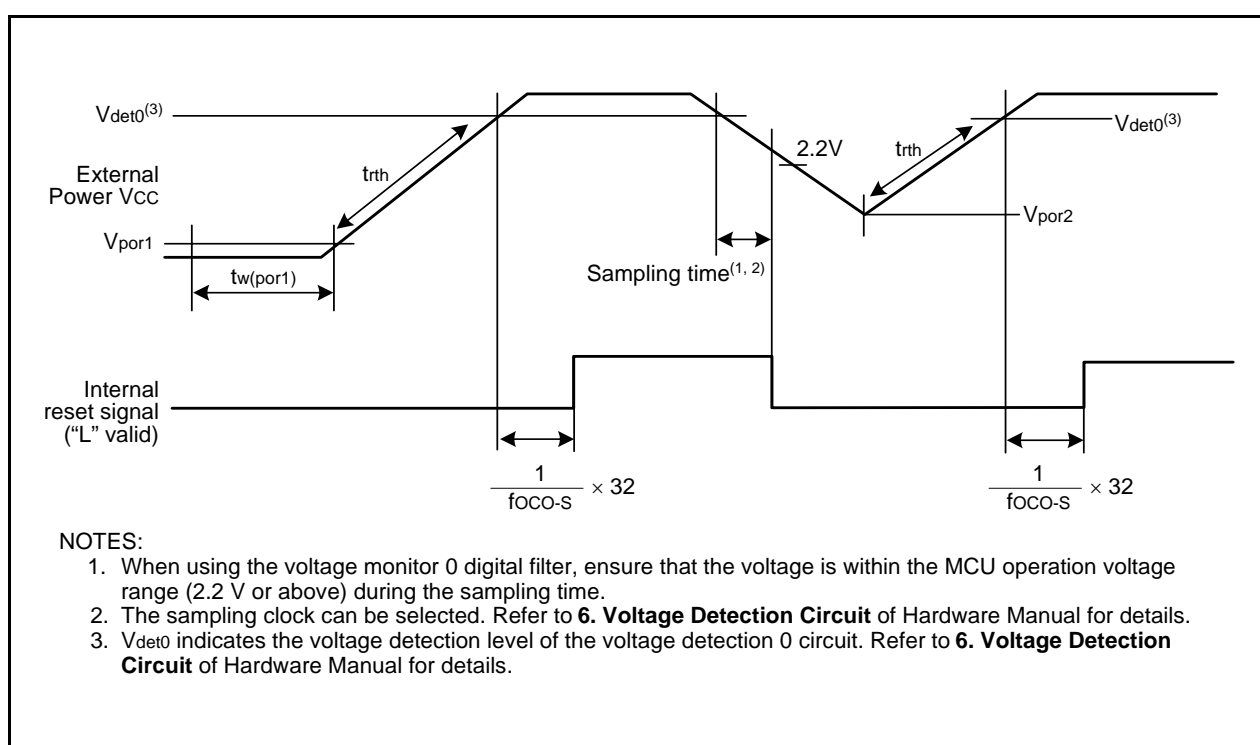
1. The measurement condition is V_{CC} = 2.2 V to 5.5 V and T_{opr} = -20 to 85°C (N version) / -40 to 85°C (D version).
2. Time until the voltage monitor 2 interrupt request is generated after the voltage passes V_{det2}.
3. Necessary time until the voltage detection circuit operates after setting to 1 again after setting the VCA27 bit in the VCA2 register to 0.

Table 5.10 Power-on Reset Circuit, Voltage Monitor 0 Reset Electrical Characteristics⁽³⁾

| Symbol | Parameter | Condition | Standard | | | Unit |
|-------------------|---|-----------|----------|------|-------------------|---------|
| | | | Min. | Typ. | Max. | |
| V _{por1} | Power-on reset valid voltage ⁽⁴⁾ | | – | – | 0.1 | V |
| V _{por2} | Power-on reset or voltage monitor 0 reset valid voltage | | 0 | – | V _{det0} | V |
| tr _{th} | External power V _{CC} rise gradient ⁽²⁾ | | 20 | – | – | mV/msec |

NOTES:

- The measurement condition is T_{opr} = -20 to 85°C (N version) / -40 to 85°C (D version), unless otherwise specified.
- This condition (external power V_{CC} rise gradient) does not apply if V_{CC} ≥ 1.0 V.
- To use the power-on reset function, enable voltage monitor 0 reset by setting the LVD0ON bit in the OFS register to 0, the VW0C0 and VW0C6 bits in the VW0C register to 1 respectively, and the VCA25 bit in the VCA2 register to 1.
- tw_(por1) indicates the duration the external power V_{CC} must be held below the effective voltage (V_{por1}) to enable a power on reset. When turning on the power for the first time, maintain tw_(por1) for 30 s or more if -20°C ≤ T_{opr} ≤ 85°C, maintain tw_(por1) for 3,000 s or more if -40°C ≤ T_{opr} < -20°C.



NOTES:

- When using the voltage monitor 0 digital filter, ensure that the voltage is within the MCU operation voltage range (2.2 V or above) during the sampling time.
- The sampling clock can be selected. Refer to **6. Voltage Detection Circuit** of Hardware Manual for details.
- V_{det0} indicates the voltage detection level of the voltage detection 0 circuit. Refer to **6. Voltage Detection Circuit** of Hardware Manual for details.

Figure 5.3 Power-on Reset Circuit Electrical Characteristics

Table 5.11 High-speed On-Chip Oscillator Circuit Electrical Characteristics

| Symbol | Parameter | Condition | Standard | | | Unit |
|---------|--|--|----------|--------|------|------|
| | | | Min. | Typ. | Max. | |
| fOCO40M | High-speed on-chip oscillator frequency temperature • supply voltage dependence | V _{CC} = 2.7 V to 5.5 V -20°C ≤ T _{opr} ≤ 85°C ⁽²⁾ | 39.2 | 40 | 40.8 | MHz |
| | | V _{CC} = 2.7 V to 5.5 V -40°C ≤ T _{opr} ≤ 85°C ⁽²⁾ | 39.0 | 40 | 41.0 | MHz |
| | | V _{CC} = 2.2 V to 5.5 V -20°C ≤ T _{opr} ≤ 85°C ⁽³⁾ | 35.2 | 40 | 44.8 | MHz |
| | | V _{CC} = 2.2 V to 5.5 V -40°C ≤ T _{opr} ≤ 85°C ⁽³⁾ | 34.0 | 40 | 46.0 | MHz |
| - | High-speed on-chip oscillator frequency when correction value in FRA7 register is written to FRA1 register | V _{CC} = 5.0 V, T _{opr} = 25°C | - | 36.864 | - | MHz |
| | | V _{CC} = 2.7 V to 5.5 V -20°C ≤ T _{opr} ≤ 85°C | -3% | - | 3% | % |
| - | Value in FRA1 register after reset | | 08h | - | F7h | - |
| - | Oscillation frequency adjustment unit of high- speed on-chip oscillator | Adjust FRA1 register (value after reset) to -1 | - | +0.3 | - | MHz |
| - | Oscillation stability time | V _{CC} = 5.0 V, T _{opr} = 25°C | - | 10 | 100 | μs |
| - | Self power consumption at oscillation | V _{CC} = 5.0 V, T _{opr} = 25°C | - | 550 | - | μA |

NOTES:

- V_{CC} = 2.2 to 5.5 V, T_{opr} = -20 to 85°C (N version) / -40 to 85°C (D version), unless otherwise specified.
- These standard values show when the FRA1 register value after reset is assumed.
- These standard values show when the correction value in the FRA6 register is written to the FRA1 register.

Table 5.12 Low-speed On-Chip Oscillator Circuit Electrical Characteristics

| Symbol | Parameter | Condition | Standard | | | Unit |
|--------|--|--|----------|------|------|------|
| | | | Min. | Typ. | Max. | |
| fOCO-S | Low-speed on-chip oscillator frequency | | 30 | 125 | 250 | kHz |
| - | Oscillation stability time | V _{CC} = 5.0 V, T _{opr} = 25°C | - | 10 | 100 | μs |
| - | Self power consumption at oscillation | V _{CC} = 5.0 V, T _{opr} = 25°C | - | 15 | - | μA |

NOTE:

- V_{CC} = 2.2 to 5.5 V, T_{opr} = -20 to 85°C (N version) / -40 to 85°C (D version), unless otherwise specified.

Table 5.13 Power Supply Circuit Timing Characteristics

| Symbol | Parameter | Condition | Standard | | | Unit |
|----------------------|--|-----------|----------|------|------|------|
| | | | Min. | Typ. | Max. | |
| t _d (P-R) | Time for internal power supply stabilization during power-on ⁽²⁾ | | 1 | - | 2000 | μs |
| t _d (R-S) | STOP exit time ⁽³⁾ | | - | - | 150 | μs |

NOTES:

- The measurement condition is V_{CC} = 2.2 to 5.5 V and T_{opr} = 25°C.
- Waiting time until the internal power supply generation circuit stabilizes during power-on.
- Time until system clock supply starts after the interrupt is acknowledged to exit stop mode.

Table 5.14 Timing Requirements of Clock Synchronous Serial I/O with Chip Select⁽¹⁾

| Symbol | Parameter | | Conditions | Standard | | | Unit |
|--------|------------------------------------|--------|---|------------|------|------------------------|---------------------|
| | | | | Min. | Typ. | Max. | |
| tsucyc | SSCK clock cycle time | | | 4 | – | – | tcyc ⁽²⁾ |
| tHI | SSCK clock "H" width | | | 0.4 | – | 0.6 | tsucyc |
| tLO | SSCK clock "L" width | | | 0.4 | – | 0.6 | tsucyc |
| tRISE | SSCK clock rising time | Master | | – | – | 1 | tcyc ⁽²⁾ |
| | | Slave | | – | – | 1 | μs |
| tFALL | SSCK clock falling time | Master | | – | – | 1 | tcyc ⁽²⁾ |
| | | Slave | | – | – | 1 | μs |
| tsu | SSO, SSI data input setup time | | | 100 | – | – | ns |
| tH | SSO, SSI data input hold time | | | 1 | – | – | tcyc ⁽²⁾ |
| tLEAD | $\overline{\text{SCS}}$ setup time | Slave | | 1tcyc + 50 | – | – | ns |
| tLAG | $\overline{\text{SCS}}$ hold time | Slave | | 1tcyc + 50 | – | – | ns |
| tOD | SSO, SSI data output delay time | | | – | – | 1 | tcyc ⁽²⁾ |
| tSA | SSI slave access time | | $2.7\text{ V} \leq V_{\text{CC}} \leq 5.5\text{ V}$ | – | – | $1.5\text{tcyc} + 100$ | ns |
| | | | $2.2\text{ V} \leq V_{\text{CC}} < 2.7\text{ V}$ | – | – | $1.5\text{tcyc} + 200$ | ns |
| tOR | SSI slave out open time | | $2.7\text{ V} \leq V_{\text{CC}} \leq 5.5\text{ V}$ | – | – | $1.5\text{tcyc} + 100$ | ns |
| | | | $2.2\text{ V} \leq V_{\text{CC}} < 2.7\text{ V}$ | – | – | $1.5\text{tcyc} + 200$ | ns |

NOTES:

1. $V_{\text{CC}} = 2.2$ to 5.5 V , $V_{\text{SS}} = 0\text{ V}$ at $T_{\text{opr}} = -20$ to 85°C (N version) / -40 to 85°C (D version), unless otherwise specified.
2. $1\text{tcyc} = 1/f_1(\text{s})$

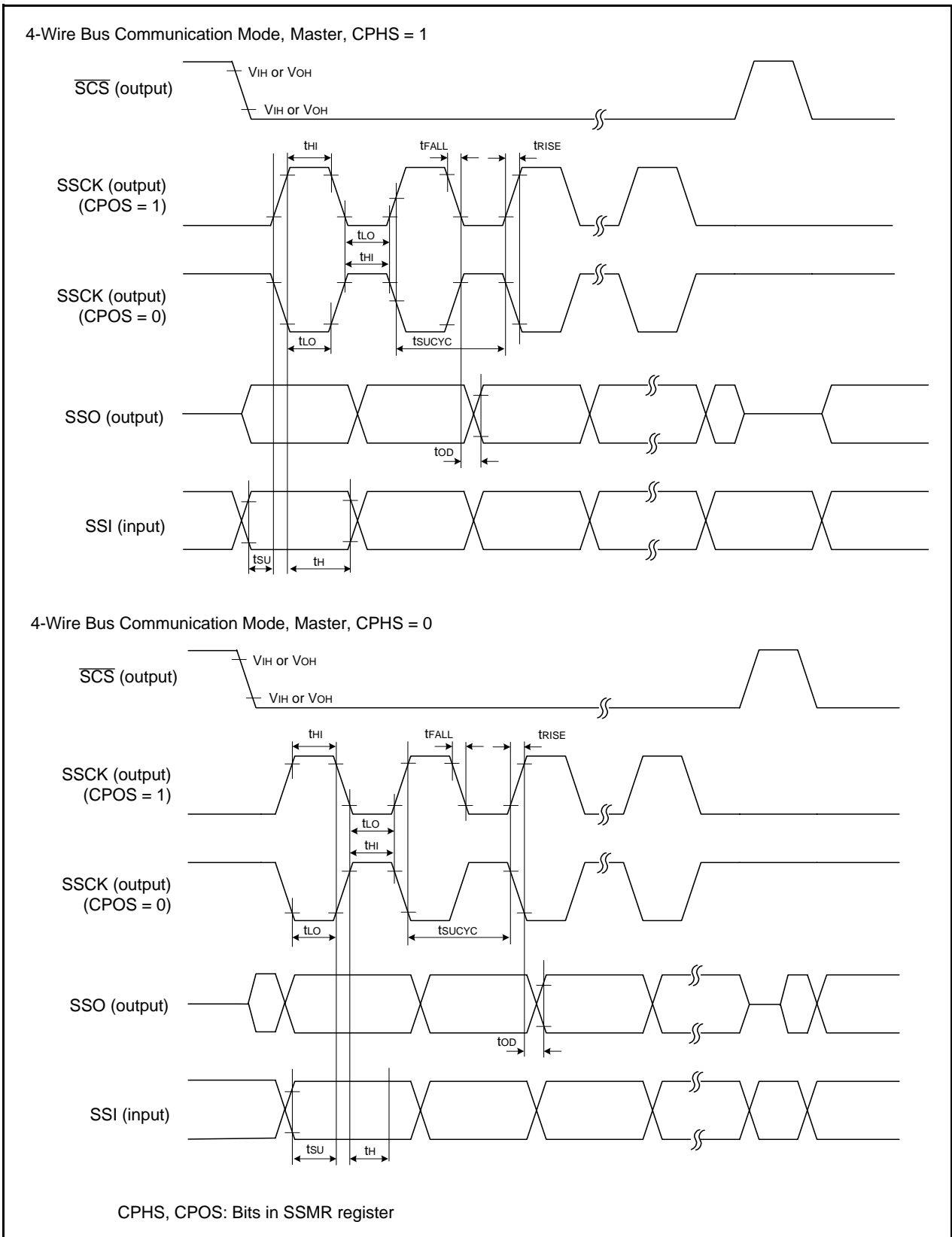


Figure 5.4 I/O Timing of Clock Synchronous Serial I/O with Chip Select (Master)

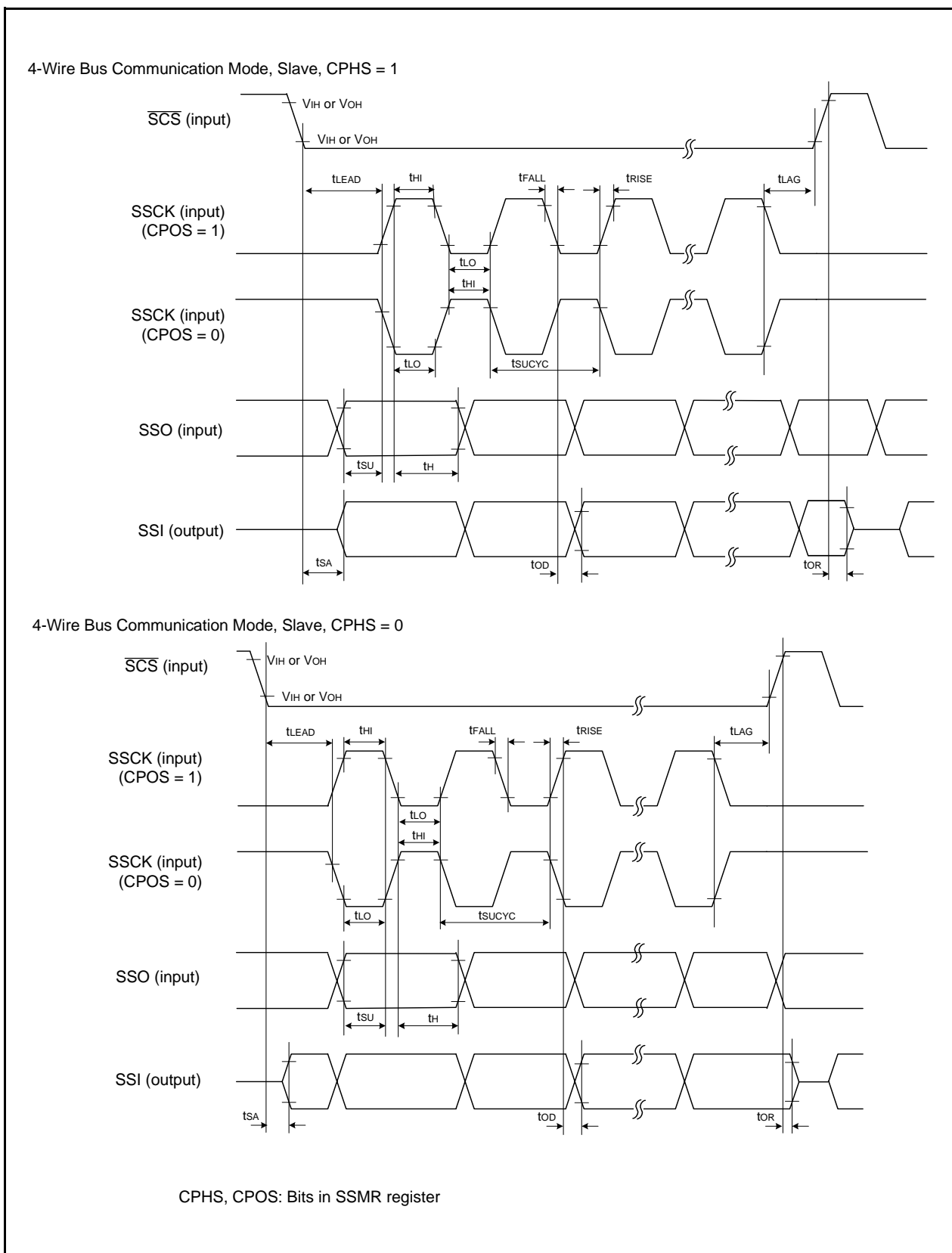


Figure 5.5 I/O Timing of Clock Synchronous Serial I/O with Chip Select (Slave)

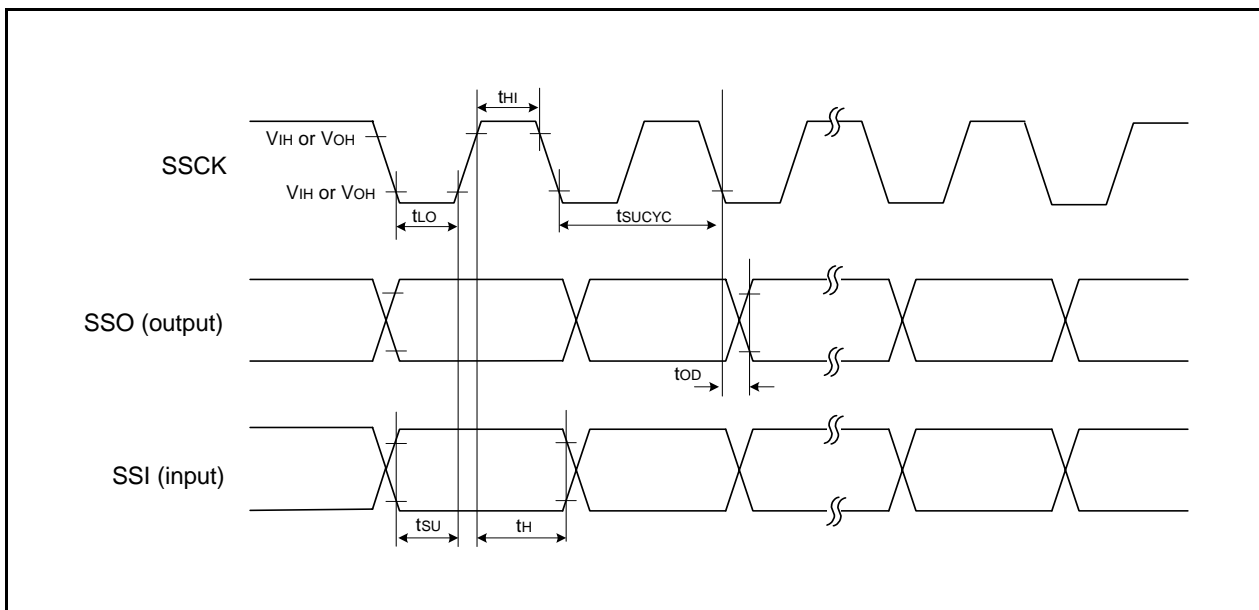


Figure 5.6 I/O Timing of Clock Synchronous Serial I/O with Chip Select (Clock Synchronous Communication Mode)

Table 5.15 Timing Requirements of I²C bus Interface (1)

| Symbol | Parameter | Condition | Standard | | | Unit |
|--------|---|-----------|-----------------------------|------|----------------------|------|
| | | | Min. | Typ. | Max. | |
| tSCL | SCL input cycle time | | 12tcyc + 600 ⁽²⁾ | – | – | ns |
| tSCLH | SCL input “H” width | | 3tcyc + 300 ⁽²⁾ | – | – | ns |
| tSCLL | SCL input “L” width | | 5tcyc + 500 ⁽²⁾ | – | – | ns |
| tsf | SCL, SDA input fall time | | – | – | 300 | ns |
| tSP | SCL, SDA input spike pulse rejection time | | – | – | 1tcyc ⁽²⁾ | ns |
| tBUF | SDA input bus-free time | | 5tcyc ⁽²⁾ | – | – | ns |
| tSTAH | Start condition input hold time | | 3tcyc ⁽²⁾ | – | – | ns |
| tSTAS | Retransmit start condition input setup time | | 3tcyc ⁽²⁾ | – | – | ns |
| tSTOP | Stop condition input setup time | | 3tcyc ⁽²⁾ | – | – | ns |
| tSDAS | Data input setup time | | 1tcyc + 20 ⁽²⁾ | – | – | ns |
| tSDAH | Data input hold time | | 0 | – | – | ns |

NOTES:

1. VCC = 2.2 to 5.5 V, VSS = 0 V and Topr = -20 to 85°C (N version) / -40 to 85°C (D version), unless otherwise specified.
2. 1tcyc = 1/f1(s)

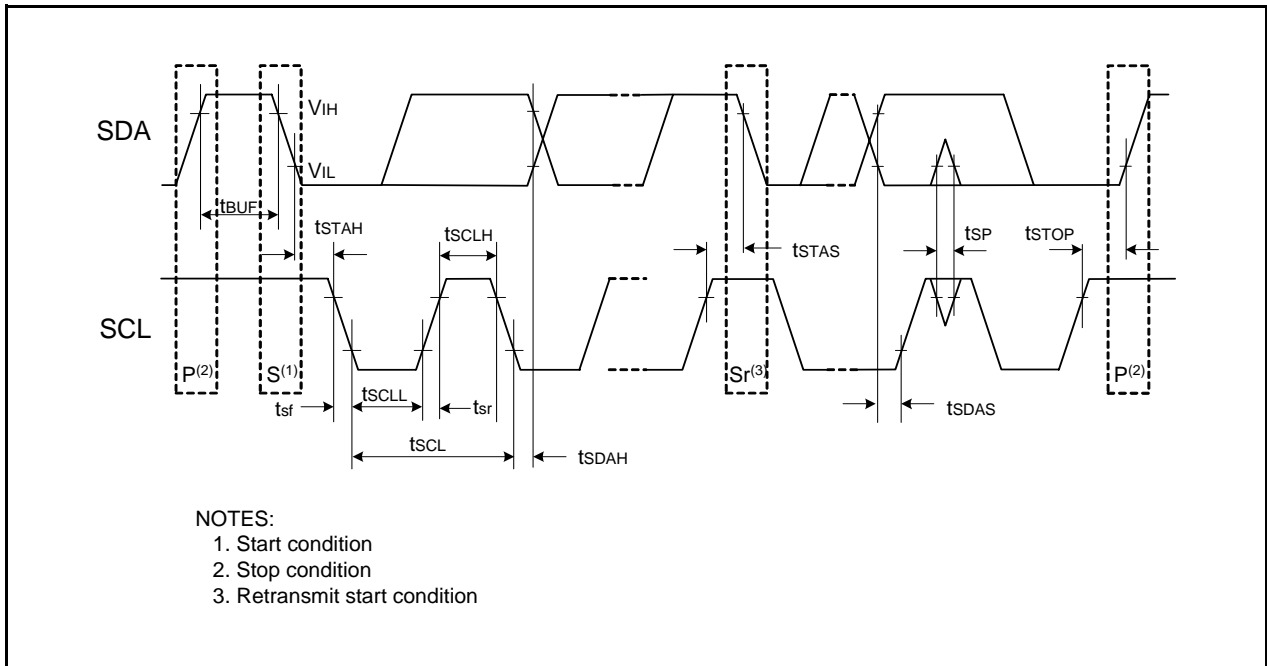


Figure 5.7 I/O Timing of I²C bus Interface

Table 5.16 Electrical Characteristics (1) [V_{CC} = 5 V]

| Symbol | Parameter | | Condition | Standard | | | Unit | | |
|----------------------------------|---------------------|---|---------------------------|---------------------------|-----------------------|------|-----------------|------|----|
| | | | | Min. | Typ. | Max. | | | |
| V _{OH} | Output "H" voltage | Except P2_0 to P2_7, XOUT | I _{OH} = -5 mA | | V _{CC} - 2.0 | - | V _{CC} | V | |
| | | | I _{OH} = -200 μA | | V _{CC} - 0.5 | - | V _{CC} | V | |
| | P2_0 to P2_7 | | Drive capacity HIGH | I _{OH} = -20 mA | V _{CC} - 2.0 | - | V _{CC} | V | |
| | | | Drive capacity LOW | I _{OH} = -5 mA | V _{CC} - 2.0 | - | V _{CC} | V | |
| | XOUT | | Drive capacity HIGH | I _{OH} = -1 mA | V _{CC} - 2.0 | - | V _{CC} | V | |
| | | | Drive capacity LOW | I _{OH} = -500 μA | V _{CC} - 2.0 | - | V _{CC} | V | |
| V _{OL} | Output "L" voltage | Except P2_0 to P2_7, XOUT | I _{OL} = 5 mA | | - | - | 2.0 | V | |
| | | | I _{OL} = 200 μA | | - | - | 0.45 | V | |
| | P2_0 to P2_7 | | Drive capacity HIGH | I _{OL} = 20 mA | - | - | 2.0 | V | |
| | | | Drive capacity LOW | I _{OL} = 5 mA | - | - | 2.0 | V | |
| | XOUT | | Drive capacity HIGH | I _{OL} = 1 mA | - | - | 2.0 | V | |
| | | | Drive capacity LOW | I _{OL} = 500 μA | - | - | 2.0 | V | |
| V _{T+} -V _{T-} | Hysteresis | INT0, INT1, INT2, INT3, KI0, KI1, KI2, KI3, TRAIO, TRFI, RXD0, RXD1, CLK0, CLK1, CLK2, SSI, SCL, SDA, SSO | | | 0.1 | 0.5 | - | V | |
| | | RESET | | | 0.1 | 1.0 | - | V | |
| I _{IH} | Input "H" current | | | V _I = 5 V | | - | - | 5.0 | μA |
| I _{IL} | Input "L" current | | | V _I = 0 V | | - | - | -5.0 | μA |
| R _{PULLUP} | Pull-up resistance | | | V _I = 0 V | | 30 | 50 | 167 | kΩ |
| R _{IXIN} | Feedback resistance | XIN | | | - | 1.0 | - | - | MΩ |
| R _{IXCIN} | Feedback resistance | XCIN | | | - | 18 | - | - | MΩ |
| V _{RAM} | RAM hold voltage | | | During stop mode | | 1.8 | - | - | V |

NOTE:

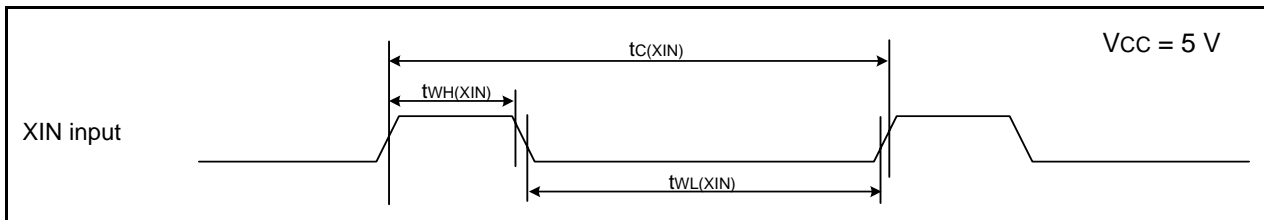
- V_{CC} = 4.2 to 5.5 V at T_{opr} = -20 to 85°C (N version) / -40 to 85°C (D version), f(XIN) = 20 MHz, unless otherwise specified.

**Table 5.17 Electrical Characteristics (2) [V_{CC} = 5 V]
(T_{opr} = -20 to 85°C (N version) / -40 to 85°C (D version), unless otherwise specified.)**

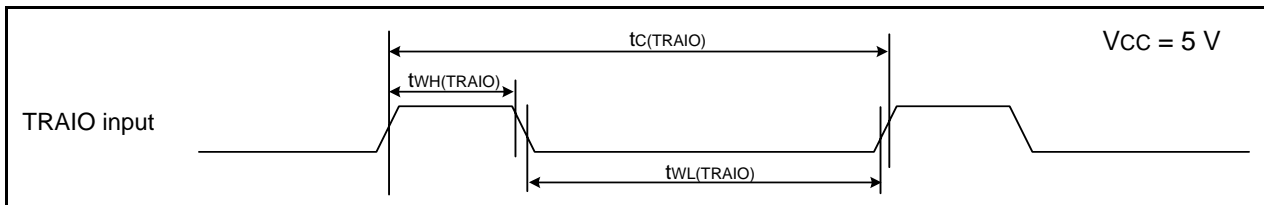
| Symbol | Parameter | Condition | Standard | | | Unit | |
|-----------------|---|--|--|------|------|------|----|
| | | | Min. | Typ. | Max. | | |
| I _{CC} | Power supply current (V _{CC} = 3.3 to 5.5 V) Single-chip mode, output pins are open, other pins are V _{SS} | High-speed clock mode | XIN = 20 MHz (square wave) High-speed on-chip oscillator off Low-speed on-chip oscillator on = 125 kHz No division | – | 12 | 20 | mA |
| | | | XIN = 16 MHz (square wave) High-speed on-chip oscillator off Low-speed on-chip oscillator on = 125 kHz No division | – | 10 | 16 | mA |
| | | | XIN = 10 MHz (square wave) High-speed on-chip oscillator off Low-speed on-chip oscillator on = 125 kHz No division | – | 7 | – | mA |
| | | | XIN = 20 MHz (square wave) High-speed on-chip oscillator off Low-speed on-chip oscillator on = 125 kHz Divide-by-8 | – | 5.5 | – | mA |
| | | | XIN = 16 MHz (square wave) High-speed on-chip oscillator off Low-speed on-chip oscillator on = 125 kHz Divide-by-8 | – | 4.5 | – | mA |
| | | | XIN = 10 MHz (square wave) High-speed on-chip oscillator off Low-speed on-chip oscillator on = 125 kHz Divide-by-8 | – | 3 | – | mA |
| | | High-speed on-chip oscillator mode | XIN clock off High-speed on-chip oscillator on f _{OCO} = 10 MHz Low-speed on-chip oscillator on = 125 kHz No division | – | 6 | 12 | mA |
| | | | XIN clock off High-speed on-chip oscillator on f _{OCO} = 10 MHz Low-speed on-chip oscillator on = 125 kHz Divide-by-8 | – | 2.5 | – | mA |
| | | Low-speed on-chip oscillator mode | XIN clock off High-speed on-chip oscillator off Low-speed on-chip oscillator on = 125 kHz Divide-by-8, FMR47 = 1 | – | 150 | 400 | μA |
| | | Low-speed clock mode | XIN clock off High-speed on-chip oscillator off Low-speed on-chip oscillator off XCIN clock oscillator on = 32 kHz FMR47 = 1 | – | 150 | 400 | μA |
| | | | XIN clock off High-speed on-chip oscillator off Low-speed on-chip oscillator off XCIN clock oscillator on = 32 kHz Program operation on RAM Flash memory off, FMSTP = 1 | – | 35 | – | μA |
| | | Wait mode | XIN clock off High-speed on-chip oscillator off Low-speed on-chip oscillator on = 125 kHz While a WAIT instruction is executed Peripheral clock operation VCA27 = VCA26 = VCA25 = 0 VCA20 = 1 | – | 30 | 90 | μA |
| | | | XIN clock off High-speed on-chip oscillator off Low-speed on-chip oscillator on = 125 kHz While a WAIT instruction is executed Peripheral clock off VCA27 = VCA26 = VCA25 = 0 VCA20 = 1 | – | 18 | 55 | μA |
| | | | XIN clock off High-speed on-chip oscillator off Low-speed on-chip oscillator off XCIN clock oscillator on = 32 kHz (high drive) While a WAIT instruction is executed VCA27 = VCA26 = VCA25 = 0 VCA20 = 1 | – | 3.5 | – | μA |
| | | | XIN clock off High-speed on-chip oscillator off Low-speed on-chip oscillator off XCIN clock oscillator on = 32 kHz (low drive) While a WAIT instruction is executed VCA27 = VCA26 = VCA25 = 0 VCA20 = 1 | – | 2.3 | – | μA |
| | | | XIN clock off, T _{opr} = 25°C High-speed on-chip oscillator off Low-speed on-chip oscillator off CM10 = 1 Peripheral clock off VCA27 = VCA26 = VCA25 = 0 | – | 0.7 | 3.0 | μA |
| | | Stop mode | XIN clock off, T _{opr} = 85°C High-speed on-chip oscillator off Low-speed on-chip oscillator off CM10 = 1 Peripheral clock off VCA27 = VCA26 = VCA25 = 0 | – | 1.7 | – | μA |

Timing Requirements**(Unless Otherwise Specified: $V_{CC} = 5\text{ V}$, $V_{SS} = 0\text{ V}$ at $T_{\text{opr}} = 25^\circ\text{C}$) [$V_{CC} = 5\text{ V}$]****Table 5.18 XIN Input, XCIN Input**

| Symbol | Parameter | Standard | | Unit |
|------------------------------|-----------------------|----------|------|---------------|
| | | Min. | Max. | |
| $t_{c(\text{XIN})}$ | XIN input cycle time | 50 | – | ns |
| $t_{\text{WH}(\text{XIN})}$ | XIN input “H” width | 25 | – | ns |
| $t_{\text{WL}(\text{XIN})}$ | XIN input “L” width | 25 | – | ns |
| $t_{c(\text{XCIN})}$ | XCIN input cycle time | 14 | – | μs |
| $t_{\text{WH}(\text{XCIN})}$ | XCIN input “H” width | 7 | – | μs |
| $t_{\text{WL}(\text{XCIN})}$ | XCIN input “L” width | 7 | – | μs |

**Figure 5.8 XIN Input and XCIN Input Timing Diagram when $V_{CC} = 5\text{ V}$** **Table 5.19 TRAIO Input, $\overline{\text{INT1}}$ Input**

| Symbol | Parameter | Standard | | Unit |
|-------------------------------|------------------------|----------|------|------|
| | | Min. | Max. | |
| $t_{c(\text{TRAIO})}$ | TRAIO input cycle time | 100 | – | ns |
| $t_{\text{WH}(\text{TRAIO})}$ | TRAIO input “H” width | 40 | – | ns |
| $t_{\text{WL}(\text{TRAIO})}$ | TRAIO input “L” width | 40 | – | ns |

**Figure 5.9 TRAIO Input and $\overline{\text{INT1}}$ Input Timing Diagram when $V_{CC} = 5\text{ V}$** **Table 5.20 TRFI Input**

| Symbol | Parameter | Standard | | Unit |
|------------------------------|-----------------------|--------------------|------|------|
| | | Min. | Max. | |
| $t_{c(\text{TRFI})}$ | TRFI input cycle time | 400 ⁽¹⁾ | – | ns |
| $t_{\text{WH}(\text{TRFI})}$ | TRFI input “H” width | 200 ⁽²⁾ | – | ns |
| $t_{\text{WL}(\text{TRFI})}$ | TRFI input “L” width | 200 ⁽²⁾ | – | ns |

NOTES:

1. When using timer RF input capture mode, adjust the cycle time to $(1/\text{timer RF count source frequency} \times 3)$ or above.
2. When using timer RF input capture mode, adjust the pulse width to $(1/\text{timer RF count source frequency} \times 1.5)$ or above.

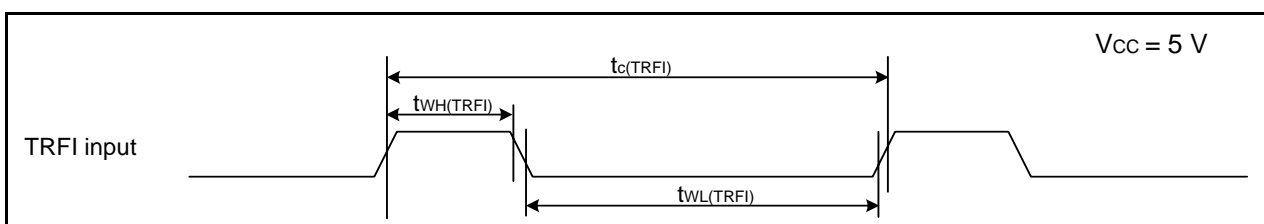
**Figure 5.10 TRFI Input Timing Diagram when $V_{CC} = 5\text{ V}$**

Table 5.21 Serial Interface

| Symbol | Parameter | Standard | | Unit |
|---------------|------------------------|----------|------|------|
| | | Min. | Max. | |
| $t_{c(CK)}$ | CLKi input cycle time | 200 | – | ns |
| $t_{w(CKH)}$ | CLKi input “H” width | 100 | – | ns |
| $t_{w(CKL)}$ | CLKi input “L” width | 100 | – | ns |
| $t_{d(C-Q)}$ | TXDi output delay time | – | 50 | ns |
| $t_h(C-Q)$ | TXDi hold time | 0 | – | ns |
| $t_{su(D-C)}$ | RXDi input setup time | 50 | – | ns |
| $t_h(C-D)$ | RXDi input hold time | 90 | – | ns |

$i = 0$ to 2

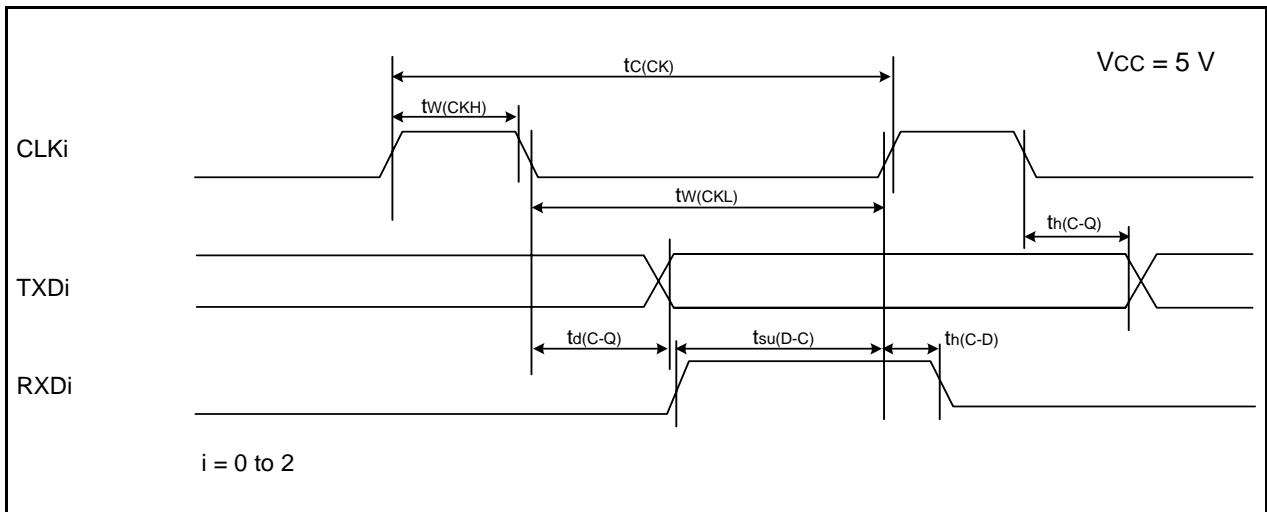


Figure 5.11 Serial Interface Timing Diagram when Vcc = 5 V

Table 5.22 External Interrupt \overline{INTi} ($i = 0, 2, 3$) Input

| Symbol | Parameter | Standard | | Unit |
|--------------|-----------------------------------|--------------------|------|------|
| | | Min. | Max. | |
| $t_{w(INH)}$ | $\overline{INT0}$ input “H” width | 250 ⁽¹⁾ | – | ns |
| $t_{w(INL)}$ | $\overline{INT0}$ input “L” width | 250 ⁽²⁾ | – | ns |

NOTES:

1. When selecting the digital filter by the \overline{INTi} input filter select bit, use an \overline{INTi} input HIGH width of either (1/digital filter clock frequency × 3) or the minimum value of standard, whichever is greater.
2. When selecting the digital filter by the \overline{INTi} input filter select bit, use an \overline{INTi} input LOW width of either (1/digital filter clock frequency × 3) or the minimum value of standard, whichever is greater.

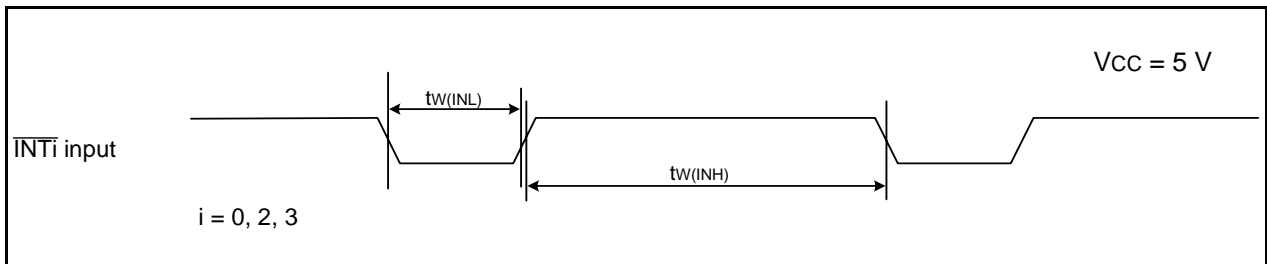


Figure 5.12 External Interrupt \overline{INTi} Input Timing Diagram when Vcc = 5 V

Table 5.23 Electrical Characteristics (3) [V_{CC} = 3 V]

| Symbol | Parameter | | Condition | | Standard | | | Unit |
|----------------------------------|---------------------|--|-------------------------|---------------------------|-----------------------|------|-----------------|------|
| | | | | | Min. | Typ. | Max. | |
| V _{OH} | Output "H" voltage | Except P2_0 to P2_7, XOUT | I _{OH} = -1 mA | | V _{CC} - 0.5 | - | V _{CC} | V |
| | | P2_0 to P2_7 | Drive capacity HIGH | I _{OH} = -5 mA | V _{CC} - 0.5 | - | V _{CC} | V |
| | | | Drive capacity LOW | I _{OH} = -1 mA | V _{CC} - 0.5 | - | V _{CC} | V |
| | | XOUT | Drive capacity HIGH | I _{OH} = -0.1 mA | V _{CC} - 0.5 | - | V _{CC} | V |
| | | | Drive capacity LOW | I _{OH} = -50 μA | V _{CC} - 0.5 | - | V _{CC} | V |
| V _{OL} | Output "L" voltage | Except P2_0 to P2_7, XOUT | I _{OL} = 1 mA | | - | - | 0.5 | V |
| | | P2_0 to P2_7 | Drive capacity HIGH | I _{OL} = 5 mA | - | - | 0.5 | V |
| | | | Drive capacity LOW | I _{OL} = 1 mA | - | - | 0.5 | V |
| | | XOUT | Drive capacity HIGH | I _{OL} = 0.1 mA | - | - | 0.5 | V |
| | | | Drive capacity LOW | I _{OL} = 50 μA | - | - | 0.5 | V |
| V _{T+} -V _{T-} | Hysteresis | $\overline{\text{INT0}}, \overline{\text{INT1}}, \overline{\text{INT2}}, \overline{\text{INT3}}, \text{KI0}, \text{KI1}, \text{KI2}, \text{KI3}, \text{TRAIO}, \text{TRFI}, \text{RXD0}, \text{RXD1}, \text{CLK0}, \text{CLK1}, \text{CLK2}, \text{SSI}, \text{SCL}, \text{SDA}, \text{SSO}$ | | | 0.1 | 0.3 | - | V |
| | | $\overline{\text{RESET}}$ | | | 0.1 | 0.4 | - | V |
| I _{IH} | Input "H" current | | V _I = 3 V | | - | - | 4.0 | μA |
| I _{IL} | Input "L" current | | V _I = 0 V | | - | - | -4.0 | μA |
| R _{PULLUP} | Pull-up resistance | | V _I = 0 V | | 66 | 160 | 500 | kΩ |
| R _{fXIN} | Feedback resistance | XIN | | | - | 3.0 | - | MΩ |
| R _{fXCIN} | Feedback resistance | XCIN | | | - | 18 | - | MΩ |
| V _{RAM} | RAM hold voltage | | During stop mode | | 1.8 | - | - | V |

NOTE:

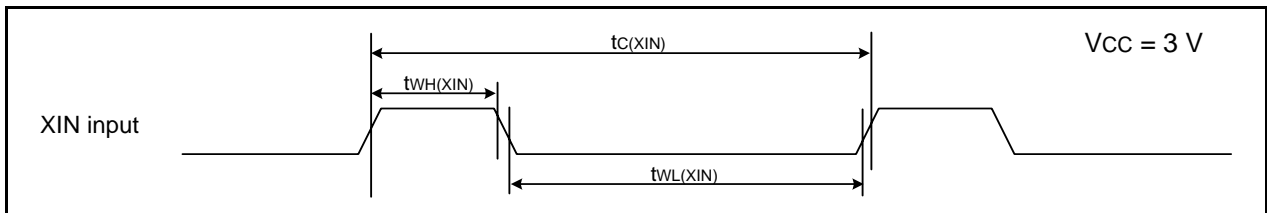
- V_{CC} = 2.7 to 3.3 V at T_{opr} = -20 to 85°C (N version) / -40 to 85°C (D version), f(XIN) = 10 MHz, unless otherwise specified.

**Table 5.24 Electrical Characteristics (4) [V_{CC} = 3 V]
(T_{opr} = -20 to 85°C (N version) / -40 to 85°C (D version), unless otherwise specified.)**

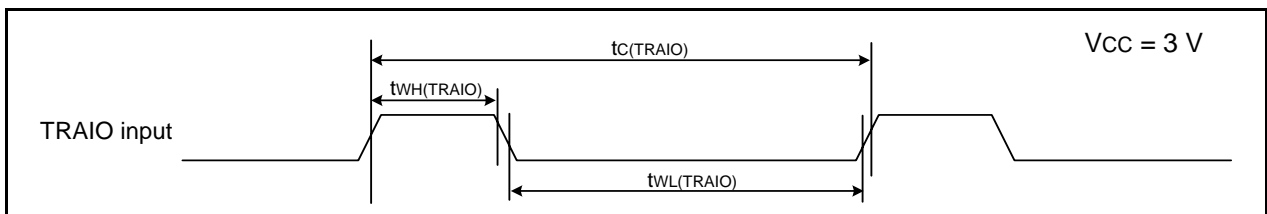
| Symbol | Parameter | Condition | Standard | | | Unit | |
|-----------------|---|------------------------------------|--|------|------|------|----|
| | | | Min. | Typ. | Max. | | |
| I _{CC} | Power supply current (V _{CC} = 2.7 to 3.3 V) Single-chip mode, output pins are open, other pins are V _{SS} | High-speed clock mode | XIN = 10 MHz (square wave) High-speed on-chip oscillator off Low-speed on-chip oscillator on = 125 kHz No division | – | 5.5 | – | mA |
| | | | XIN = 10 MHz (square wave) High-speed on-chip oscillator off Low-speed on-chip oscillator on = 125 kHz Divide-by-8 | – | 2 | – | mA |
| | | High-speed on-chip oscillator mode | XIN clock off High-speed on-chip oscillator on f _{OCO} = 10 MHz Low-speed on-chip oscillator on = 125 kHz No division | – | 5.5 | 11 | mA |
| | | | XIN clock off High-speed on-chip oscillator on f _{OCO} = 10 MHz Low-speed on-chip oscillator on = 125 kHz Divide-by-8 | – | 2.2 | – | mA |
| | | Low-speed on-chip oscillator mode | XIN clock off High-speed on-chip oscillator off Low-speed on-chip oscillator on = 125 kHz Divide-by-8, FMR47 = 1 | – | 145 | 400 | μA |
| | | Low-speed clock mode | XIN clock off High-speed on-chip oscillator off Low-speed on-chip oscillator off XCIN clock oscillator on = 32 kHz FMR47 = 1 | – | 145 | 400 | μA |
| | | | XIN clock off High-speed on-chip oscillator off Low-speed on-chip oscillator off XCIN clock oscillator on = 32 kHz Program operation on RAM Flash memory off, FMSTP = 1 | – | 30 | – | μA |
| | | Wait mode | XIN clock off High-speed on-chip oscillator off Low-speed on-chip oscillator on = 125 kHz While a WAIT instruction is executed Peripheral clock operation VCA27 = VCA26 = VCA25 = 0 VCA20 = 1 | – | 28 | 85 | μA |
| | | | XIN clock off High-speed on-chip oscillator off Low-speed on-chip oscillator on = 125 kHz While a WAIT instruction is executed Peripheral clock off VCA27 = VCA26 = VCA25 = 0 VCA20 = 1 | – | 17 | 50 | μA |
| | | | XIN clock off High-speed on-chip oscillator off Low-speed on-chip oscillator off XCIN clock oscillator on = 32 kHz (high drive) While a WAIT instruction is executed VCA27 = VCA26 = VCA25 = 0 VCA20 = 1 | – | 3.3 | – | μA |
| | | | XIN clock off High-speed on-chip oscillator off Low-speed on-chip oscillator off XCIN clock oscillator on = 32 kHz (low drive) While a WAIT instruction is executed VCA27 = VCA26 = VCA25 = 0 VCA20 = 1 | – | 2.1 | – | μA |
| | | Stop mode | XIN clock off, T _{opr} = 25°C High-speed on-chip oscillator off Low-speed on-chip oscillator off CM10 = 1 Peripheral clock off VCA27 = VCA26 = VCA25 = 0 | – | 0.65 | 3.0 | μA |
| | | | XIN clock off, T _{opr} = 85°C High-speed on-chip oscillator off Low-speed on-chip oscillator off CM10 = 1 Peripheral clock off VCA27 = VCA26 = VCA25 = 0 | – | 1.65 | – | μA |

Timing requirements**(Unless Otherwise Specified: $V_{CC} = 3\text{ V}$, $V_{SS} = 0\text{ V}$ at $T_{\text{opr}} = 25^\circ\text{C}$) [$V_{CC} = 3\text{ V}$]****Table 5.25 XIN Input, XCIN Input**

| Symbol | Parameter | Standard | | Unit |
|------------------------------|-----------------------|----------|------|---------------|
| | | Min. | Max. | |
| $t_{c(\text{XIN})}$ | XIN input cycle time | 100 | – | ns |
| $t_{\text{WH}(\text{XIN})}$ | XIN input “H” width | 40 | – | ns |
| $t_{\text{WL}(\text{XIN})}$ | XIN input “L” width | 40 | – | ns |
| $t_{c(\text{XCIN})}$ | XCIN input cycle time | 14 | – | μs |
| $t_{\text{WH}(\text{XCIN})}$ | XCIN input “H” width | 7 | – | μs |
| $t_{\text{WL}(\text{XCIN})}$ | XCIN input “L” width | 7 | – | μs |

**Figure 5.13 XIN Input and XCIN Input Timing Diagram when $V_{CC} = 3\text{ V}$** **Table 5.26 TRAIO Input, $\overline{\text{INT1}}$ Input**

| Symbol | Parameter | Standard | | Unit |
|-------------------------------|------------------------|----------|------|------|
| | | Min. | Max. | |
| $t_{c(\text{TRAIO})}$ | TRAIO input cycle time | 300 | – | ns |
| $t_{\text{WH}(\text{TRAIO})}$ | TRAIO input “H” width | 120 | – | ns |
| $t_{\text{WL}(\text{TRAIO})}$ | TRAIO input “L” width | 120 | – | ns |

**Figure 5.14 TRAIO Input and $\overline{\text{INT1}}$ Input Timing Diagram when $V_{CC} = 3\text{ V}$** **Table 5.27 TRFI Input**

| Symbol | Parameter | Standard | | Unit |
|------------------------------|-----------------------|---------------------|------|------|
| | | Min. | Max. | |
| $t_{c(\text{TRFI})}$ | TRFI input cycle time | 1200 ⁽¹⁾ | – | ns |
| $t_{\text{WH}(\text{TRFI})}$ | TRFI input “H” width | 600 ⁽²⁾ | – | ns |
| $t_{\text{WL}(\text{TRFI})}$ | TRFI input “L” width | 600 ⁽²⁾ | – | ns |

NOTES:

1. When using timer RF input capture mode, adjust the cycle time to $(1/\text{timer RF count source frequency} \times 3)$ or above.
2. When using timer RF input capture mode, adjust the pulse width to $(1/\text{timer RF count source frequency} \times 1.5)$ or above.

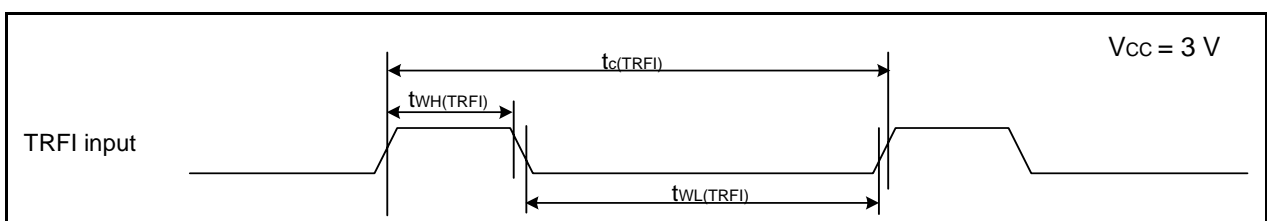
**Figure 5.15 TRFI Input Timing Diagram when $V_{CC} = 3\text{ V}$**

Table 5.28 Serial Interface

| Symbol | Parameter | Standard | | Unit |
|---------------|------------------------|----------|------|------|
| | | Min. | Max. | |
| $t_{c(CK)}$ | CLKi input cycle time | 300 | – | ns |
| $t_{w(CKH)}$ | CLKi input “H” width | 150 | – | ns |
| $t_{w(CKL)}$ | CLKi Input “L” width | 150 | – | ns |
| $t_{d(C-Q)}$ | TXDi output delay time | – | 80 | ns |
| $t_h(C-Q)$ | TXDi hold time | 0 | – | ns |
| $t_{su(D-C)}$ | RXDi input setup time | 70 | – | ns |
| $t_h(C-D)$ | RXDi input hold time | 90 | – | ns |

$i = 0$ to 2

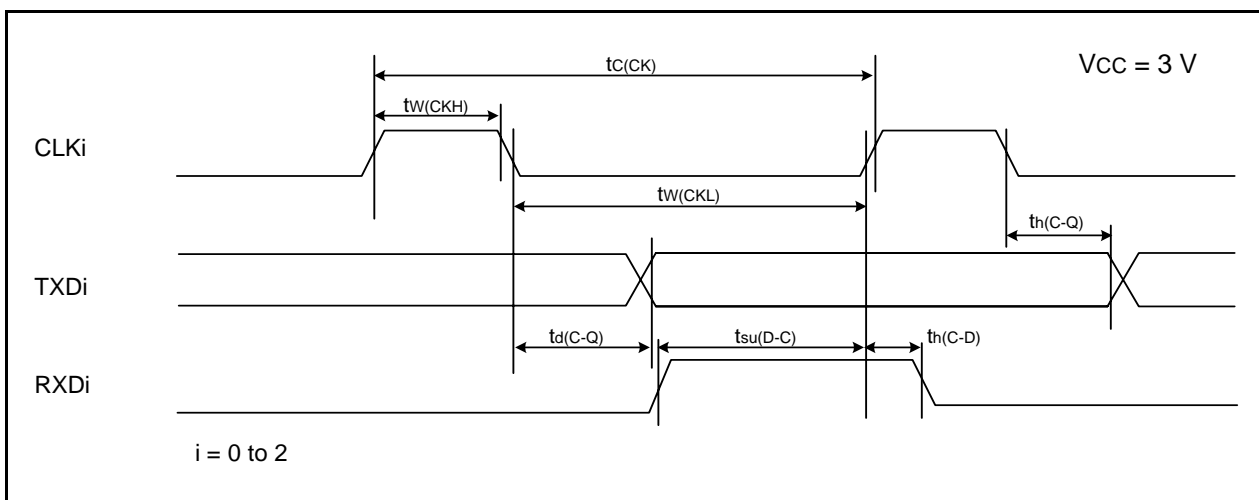


Figure 5.16 Serial Interface Timing Diagram when Vcc = 3 V

Table 5.29 External Interrupt \overline{INTi} ($i = 0, 2, 3$) Input

| Symbol | Parameter | Standard | | Unit |
|--------------|-----------------------------------|--------------------|------|------|
| | | Min. | Max. | |
| $t_{w(INH)}$ | $\overline{INT0}$ input “H” width | 380 ⁽¹⁾ | – | ns |
| $t_{w(INL)}$ | $\overline{INT0}$ input “L” width | 380 ⁽²⁾ | – | ns |

NOTES:

1. When selecting the digital filter by the \overline{INTi} input filter select bit, use an \overline{INTi} input HIGH width of either (1/digital filter clock frequency × 3) or the minimum value of standard, whichever is greater.
2. When selecting the digital filter by the \overline{INTi} input filter select bit, use an \overline{INTi} input LOW width of either (1/digital filter clock frequency × 3) or the minimum value of standard, whichever is greater.

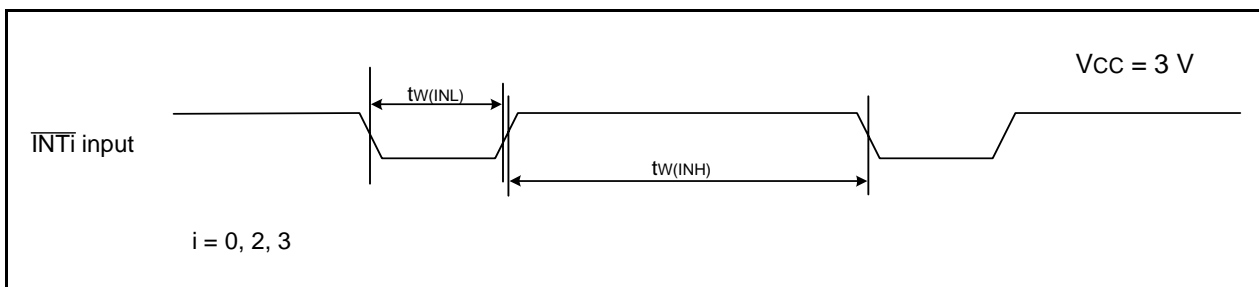


Figure 5.17 External Interrupt \overline{INTi} Input Timing Diagram when Vcc = 3 V

Table 5.30 Electrical Characteristics (5) [V_{CC} = 2.2 V]

| Symbol | Parameter | | Condition | | Standard | | | Unit |
|----------------------------------|---------------------|--|-------------------------|---------------------------|-----------------------|------|-----------------|------|
| | | | | | Min. | Typ. | Max. | |
| V _{OH} | Output "H" voltage | Except P2_0 to P2_7, XOUT | I _{OH} = -1 mA | | V _{CC} - 0.5 | – | V _{CC} | V |
| | | P2_0 to P2_7 | Drive capacity HIGH | I _{OH} = -2 mA | V _{CC} - 0.5 | – | V _{CC} | V |
| | | | Drive capacity LOW | I _{OH} = -1 mA | V _{CC} - 0.5 | – | V _{CC} | V |
| | | XOUT | Drive capacity HIGH | I _{OH} = -0.1 mA | V _{CC} - 0.5 | – | V _{CC} | V |
| | | | Drive capacity LOW | I _{OH} = -50 μA | V _{CC} - 0.5 | – | V _{CC} | V |
| V _{OL} | Output "L" voltage | Except P2_0 to P2_7, XOUT | I _{OL} = 1 mA | | – | – | 0.5 | V |
| | | P2_0 to P2_7 | Drive capacity HIGH | I _{OL} = 2 mA | – | – | 0.5 | V |
| | | | Drive capacity LOW | I _{OL} = 1 mA | – | – | 0.5 | V |
| | | XOUT | Drive capacity HIGH | I _{OL} = 0.1 mA | – | – | 0.5 | V |
| | | | Drive capacity LOW | I _{OL} = 50 μA | – | – | 0.5 | V |
| V _{T+} -V _{T-} | Hysteresis | $\overline{\text{INT0}}, \overline{\text{INT1}}, \overline{\text{INT2}}, \overline{\text{INT3}}, \text{KI0}, \text{KI1}, \text{KI2}, \text{KI3}, \text{TRAIO}, \text{TRFI}, \text{RXD0}, \text{RXD1}, \text{CLK0}, \text{CLK1}, \text{CLK2}, \text{SSI}, \text{SCL}, \text{SDA}, \text{SSO}$ | | | 0.05 | 0.3 | – | V |
| | | $\overline{\text{RESET}}$ | | | 0.05 | 0.15 | – | V |
| I _{IH} | Input "H" current | | V _I = 2.2 V | | – | – | 4.0 | μA |
| I _{IL} | Input "L" current | | V _I = 0 V | | – | – | -4.0 | μA |
| R _{PULLUP} | Pull-up resistance | | V _I = 0 V | | 100 | 200 | 600 | kΩ |
| R _{fXIN} | Feedback resistance | XIN | | | – | 5 | – | MΩ |
| R _{fXCIN} | Feedback resistance | XCIN | | | – | 35 | – | MΩ |
| V _{RAM} | RAM hold voltage | | During stop mode | | 1.8 | – | – | V |

NOTE:

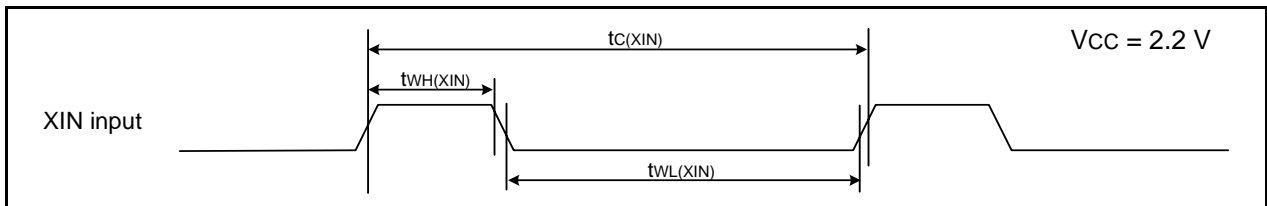
- V_{CC} = 2.2 V at T_{opr} = -20 to 85°C (N version) / -40 to 85°C (D version), f(XIN) = 5 MHz, unless otherwise specified.

**Table 5.31 Electrical Characteristics (6) [V_{CC} = 2.2 V]
(T_{opr} = -20 to 85°C (N version) / -40 to 85°C (D version), unless otherwise specified.)**

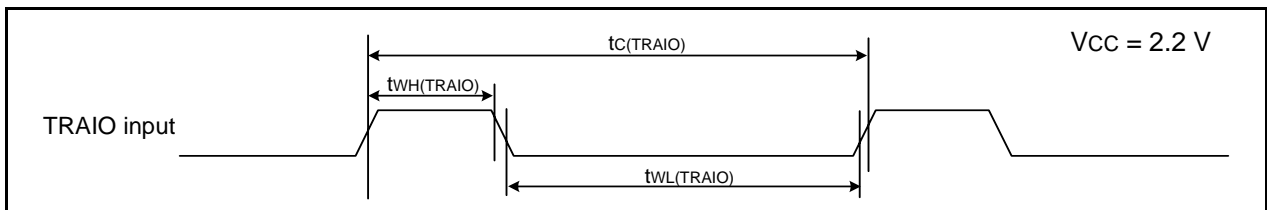
| Symbol | Parameter | Condition | Standard | | | Unit | |
|-----------------|--|---|--|------|------|------|----|
| | | | Min. | Typ. | Max. | | |
| I _{CC} | Power supply current (V _{CC} = 2.2 to 2.7 V) Single-chip mode, output pins are open, other pins are V _{SS} | High-speed clock mode | XIN = 5 MHz (square wave) High-speed on-chip oscillator off Low-speed on-chip oscillator on = 125 kHz No division | – | 2.5 | – | mA |
| | | | XIN = 5 MHz (square wave) High-speed on-chip oscillator off Low-speed on-chip oscillator on = 125 kHz Divide-by-8 | – | 1 | – | mA |
| | | High-speed on-chip oscillator mode | XIN clock off High-speed on-chip oscillator on f _{OCO} = 5 MHz Low-speed on-chip oscillator on = 125 kHz No division | – | 4 | – | mA |
| | | | XIN clock off High-speed on-chip oscillator on f _{OCO} = 5 MHz Low-speed on-chip oscillator on = 125 kHz Divide-by-8 | – | 1.7 | – | mA |
| | | Low-speed on- chip oscillator mode | XIN clock off High-speed on-chip oscillator off Low-speed on-chip oscillator on = 125 kHz Divide-by-8, FMR47 = 1 | – | 110 | 300 | μA |
| | | Low-speed clock mode | XIN clock off High-speed on-chip oscillator off Low-speed on-chip oscillator off XCIN clock oscillator on = 32 kHz FMR47 = 1 | – | 125 | 350 | μA |
| | | | XIN clock off High-speed on-chip oscillator off Low-speed on-chip oscillator off XCIN clock oscillator on = 32 kHz Program operation on RAM Flash memory off, FMSTP = 1 | – | 27 | – | μA |
| | | Wait mode | XIN clock off High-speed on-chip oscillator off Low-speed on-chip oscillator on = 125 kHz While a WAIT instruction is executed Peripheral clock operation VCA27 = VCA26 = VCA25 = 0 VCA20 = 1 | – | 20 | 60 | μA |
| | | | XIN clock off High-speed on-chip oscillator off Low-speed on-chip oscillator on = 125 kHz While a WAIT instruction is executed Peripheral clock off VCA27 = VCA26 = VCA25 = 0 VCA20 = 1 | – | 12 | 40 | μA |
| | | | XIN clock off High-speed on-chip oscillator off Low-speed on-chip oscillator off XCIN clock oscillator on = 32 kHz (high drive) While a WAIT instruction is executed VCA27 = VCA26 = VCA25 = 0 VCA20 = 1 | – | 2.8 | – | μA |
| | | | XIN clock off High-speed on-chip oscillator off Low-speed on-chip oscillator off XCIN clock oscillator on = 32 kHz (low drive) While a WAIT instruction is executed VCA27 = VCA26 = VCA25 = 0 VCA20 = 1 | – | 1.9 | – | μA |
| | | | XIN clock off, T _{opr} = 25°C High-speed on-chip oscillator off Low-speed on-chip oscillator off CM10 = 1 Peripheral clock off VCA27 = VCA26 = VCA25 = 0 | – | 0.6 | 3.0 | μA |
| | | Stop mode | XIN clock off, T _{opr} = 85°C High-speed on-chip oscillator off Low-speed on-chip oscillator off CM10 = 1 Peripheral clock off VCA27 = VCA26 = VCA25 = 0 | – | 1.60 | – | μA |

Timing requirements**(Unless Otherwise Specified: $V_{CC} = 2.2\text{ V}$, $V_{SS} = 0\text{ V}$ at $T_{opr} = 25^\circ\text{C}$) [$V_{CC} = 2.2\text{ V}$]****Table 5.32 XIN Input, XCIN Input**

| Symbol | Parameter | Standard | | Unit |
|----------------|-----------------------|----------|------|---------------|
| | | Min. | Max. | |
| $t_{c(XIN)}$ | XIN input cycle time | 200 | – | ns |
| $t_{WH(XIN)}$ | XIN input “H” width | 90 | – | ns |
| $t_{WL(XIN)}$ | XIN input “L” width | 90 | – | ns |
| $t_{c(XCIN)}$ | XCIN input cycle time | 14 | – | μs |
| $t_{WH(XCIN)}$ | XCIN input “H” width | 7 | – | μs |
| $t_{WL(XCIN)}$ | XCIN input “L” width | 7 | – | μs |

**Figure 5.18 XIN Input and XCIN Input Timing Diagram when $V_{CC} = 2.2\text{ V}$** **Table 5.33 TRAIO Input, $\overline{\text{INT1}}$ Input**

| Symbol | Parameter | Standard | | Unit |
|------------------------|------------------------|----------|------|------|
| | | Min. | Max. | |
| $t_{c(\text{TRAIO})}$ | TRAIO input cycle time | TBD | – | ns |
| $t_{WH(\text{TRAIO})}$ | TRAIO input “H” width | TBD | – | ns |
| $t_{WL(\text{TRAIO})}$ | TRAIO input “L” width | TBD | – | ns |

**Figure 5.19 TRAIO Input and $\overline{\text{INT1}}$ Input Timing Diagram when $V_{CC} = 2.2\text{ V}$** **Table 5.34 TRFI Input**

| Symbol | Parameter | Standard | | Unit |
|-----------------------|-----------------------|---------------------|------|------|
| | | Min. | Max. | |
| $t_{c(\text{TRFI})}$ | TRFI input cycle time | 2000 ⁽¹⁾ | – | ns |
| $t_{WH(\text{TRFI})}$ | TRFI input “H” width | 1000 ⁽²⁾ | – | ns |
| $t_{WL(\text{TRFI})}$ | TRFI input “L” width | 1000 ⁽²⁾ | – | ns |

NOTES:

1. When using timer RF input capture mode, adjust the cycle time to $(1/\text{timer RF count source frequency} \times 3)$ or above.
2. When using timer RF input capture mode, adjust the pulse width to $(1/\text{timer RF count source frequency} \times 1.5)$ or above.

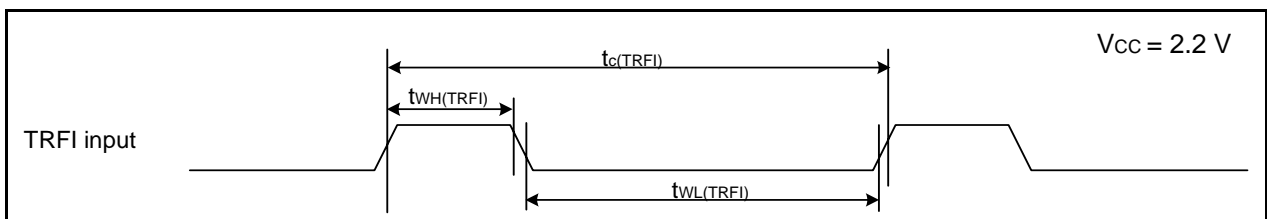
**Figure 5.20 TRFI Input Timing Diagram when $V_{CC} = 2.2\text{ V}$**

Table 5.35 Serial Interface

| Symbol | Parameter | Standard | | Unit |
|---------------|------------------------|----------|------|------|
| | | Min. | Max. | |
| $t_{c(CK)}$ | CLKi input cycle time | 800 | – | ns |
| $t_{w(CKH)}$ | CLKi input “H” width | 400 | – | ns |
| $t_{w(CKL)}$ | CLKi input “L” width | 400 | – | ns |
| $t_{d(C-Q)}$ | TXDi output delay time | – | 200 | ns |
| $t_{h(C-Q)}$ | TXDi hold time | 0 | – | ns |
| $t_{su(D-C)}$ | RXDi input setup time | 150 | – | ns |
| $t_{h(C-D)}$ | RXDi input hold time | 90 | – | ns |

$i = 0$ to 2

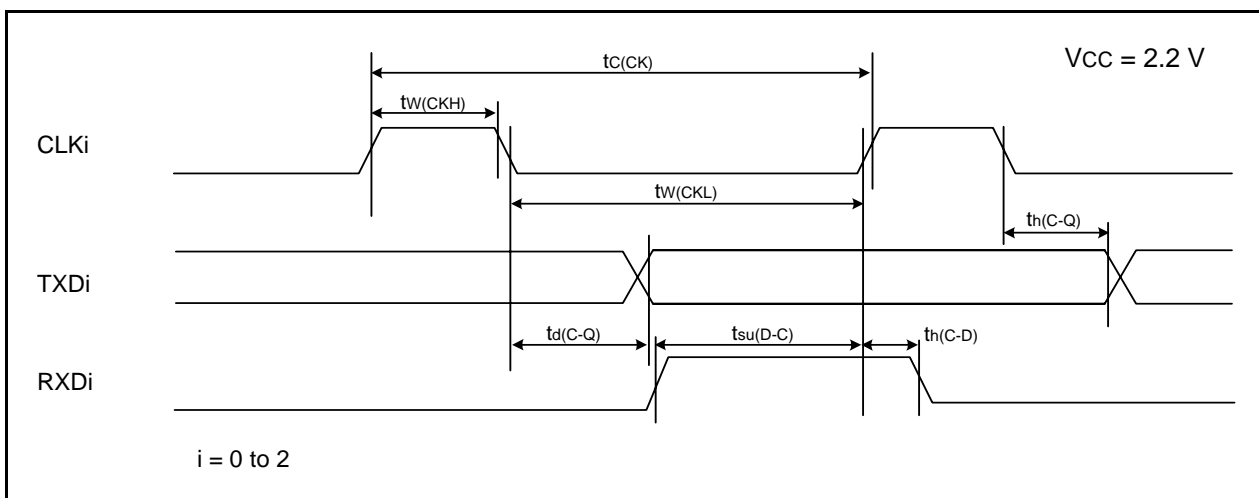


Figure 5.21 Serial Interface Timing Diagram when Vcc = 2.2 V

Table 5.36 External Interrupt \overline{INTi} ($i = 0, 2, 3$) Input

| Symbol | Parameter | Standard | | Unit |
|--------------|-----------------------------------|---------------------|------|------|
| | | Min. | Max. | |
| $t_{w(INH)}$ | $\overline{INT0}$ input “H” width | 1000 ⁽¹⁾ | – | ns |
| $t_{w(INL)}$ | $\overline{INT0}$ input “L” width | 1000 ⁽²⁾ | – | ns |

NOTES:

1. When selecting the digital filter by the \overline{INTi} input filter select bit, use an \overline{INTi} input HIGH width of either (1/digital filter clock frequency × 3) or the minimum value of standard, whichever is greater.
2. When selecting the digital filter by the \overline{INTi} input filter select bit, use an \overline{INTi} input LOW width of either (1/digital filter clock frequency × 3) or the minimum value of standard, whichever is greater.

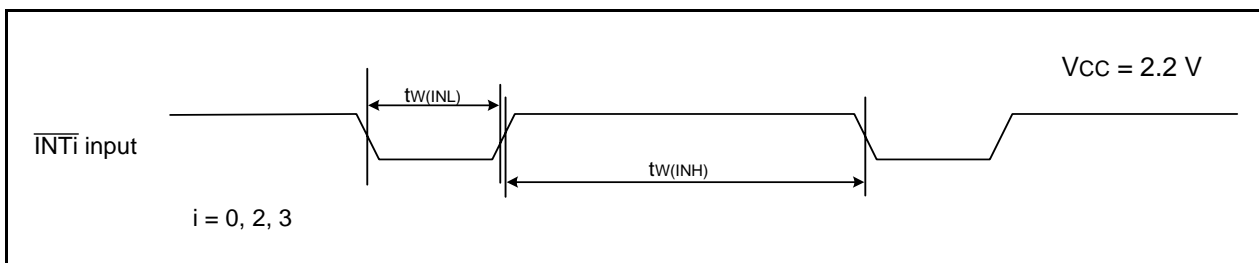


Figure 5.22 External Interrupt \overline{INTi} Input Timing Diagram when Vcc = 2.2 V

Package Dimensions

Diagrams showing the latest package dimensions and mounting information are available in the “Packages” section of the Renesas Technology website.

| | | | |
|---|------------------------------|---|--------------------|
| JEITA Package Code P-LQFP64-10x10-0.50 | RENASAS Code PLQP0064KB-A | Previous Code 64P6Q-A / FP-64K / FP-64KV | MASS[Typ.] 0.3g |
|---|------------------------------|---|--------------------|

NOTE)

- DIMENSIONS **1* AND **2* DO NOT INCLUDE MOLD FLASH.
- DIMENSION **3* DOES NOT INCLUDE TRIM OFFSET.

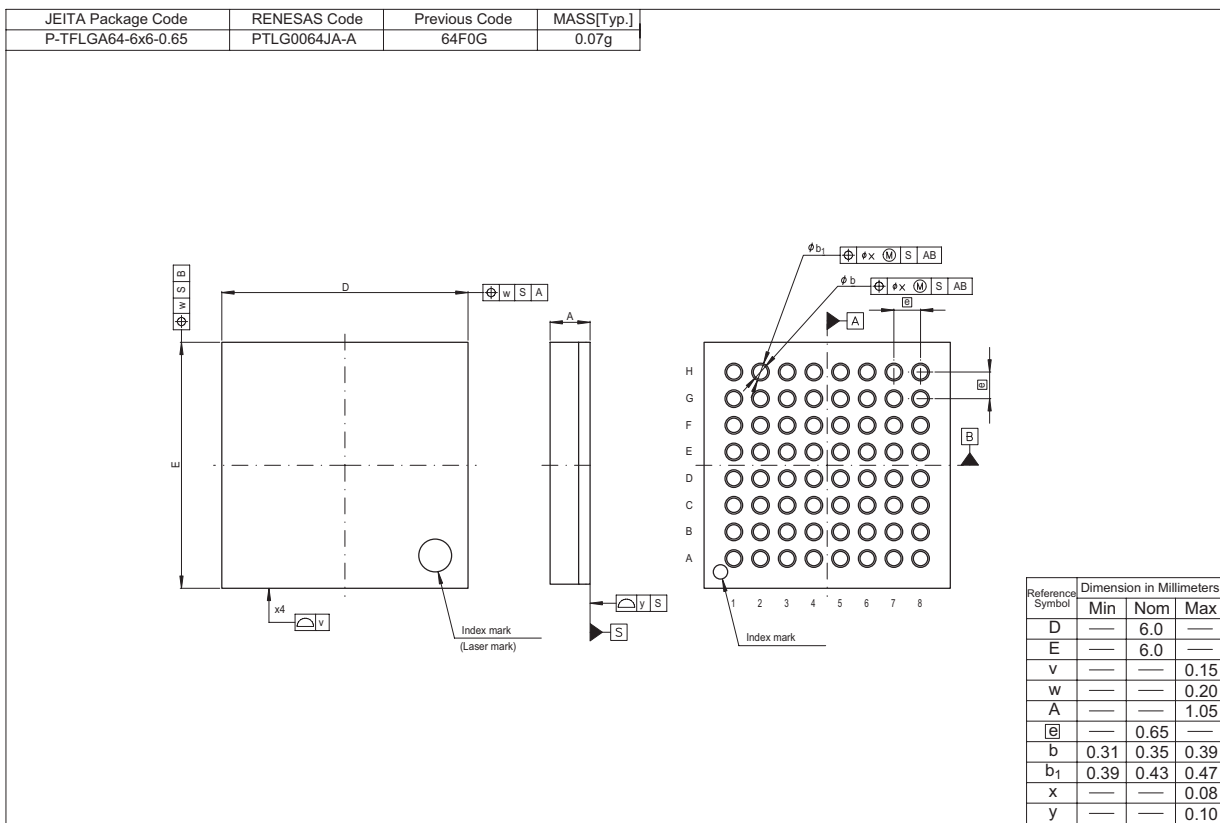
| Reference Symbol | Dimension in Millimeters | | |
|------------------|--------------------------|-------|------|
| | Min | Nom | Max |
| D | 9.9 | 10.0 | 10.1 |
| E | 9.9 | 10.0 | 10.1 |
| A ₂ | — | 1.4 | — |
| H _D | 11.8 | 12.0 | 12.2 |
| H _E | 11.8 | 12.0 | 12.2 |
| A | — | — | 1.7 |
| A ₁ | 0.05 | 0.1 | 0.15 |
| b _p | 0.15 | 0.20 | 0.25 |
| b ₁ | — | 0.18 | — |
| c | 0.09 | 0.145 | 0.20 |
| c ₁ | — | 0.125 | — |
| θ | 0° | — | 8° |
| Ⓜ | — | 0.5 | — |
| x | — | — | 0.08 |
| y | — | — | 0.08 |
| Z _D | — | 1.25 | — |
| Z _E | — | 1.25 | — |
| L | 0.35 | 0.5 | 0.65 |
| L ₁ | — | 1.0 | — |

| | | | |
|---|------------------------------|--------------------------|--------------------|
| JEITA Package Code P-LQFP64-14x14-0.80 | RENASAS Code PLQP0064GA-A | Previous Code 64P6U-A | MASS[Typ.] 0.7g |
|---|------------------------------|--------------------------|--------------------|

NOTE)

- DIMENSIONS **1* AND **2* DO NOT INCLUDE MOLD FLASH.
- DIMENSION **3* DOES NOT INCLUDE TRIM OFFSET.

| Reference Symbol | Dimension in Millimeters | | |
|------------------|--------------------------|-------|------|
| | Min | Nom | Max |
| D | 13.9 | 14.0 | 14.1 |
| E | 13.9 | 14.0 | 14.1 |
| A ₂ | — | 1.4 | — |
| H _D | 15.8 | 16.0 | 16.2 |
| H _E | 15.8 | 16.0 | 16.2 |
| A | — | — | 1.7 |
| A ₁ | 0 | 0.1 | 0.2 |
| b _p | 0.32 | 0.37 | 0.42 |
| b ₁ | — | 0.35 | — |
| c | 0.09 | 0.145 | 0.20 |
| c ₁ | — | 0.125 | — |
| θ | 0° | — | 8° |
| Ⓜ | — | 0.8 | — |
| x | — | — | 0.20 |
| y | — | — | 0.10 |
| Z _D | — | 1.0 | — |
| Z _E | — | 1.0 | — |
| L | 0.3 | 0.5 | 0.7 |
| L ₁ | — | 1.0 | — |



| | |
|-------------------------|---|
| REVISION HISTORY | R8C/2A Group, R8C/2B Group Datasheet |
|-------------------------|---|

| Rev. | Date | Description | |
|------|--------------|-------------|--|
| | | Page | Summary |
| 0.01 | Apr 03, 2006 | – | First Edition issued |
| 0.10 | Jun 26, 2006 | All pages | <p>Pin name revised CMP0_0 → TRFO00, CMP0_1 → TRFO01, CMP0_2 → TRFO02, CMP1_0 → TRFO10, CMP1_1 → TRFO11, CMP1_2 → TRFO12, TRFIN → TRFI</p> <p>2, 4 Table 1.1 Specifications for R8C/2A Group (1) and Table 1.3 Specifications for R8C/2B Group (1); I/O Ports: • Input-only: 3 pins → 2 pins revised Interrupts: • Internal: 17 sources → 23 sources revised</p> <p>3, 5 Table 1.2 Specifications for R8C/2A Group (2) and Table 1.4 Specifications for R8C/2B Group (2); ROM Correction Function deleted</p> <p>8 Figure 1.3 Block Diagram revised</p> <p>9 Figure 1.4 Pin Assignment (Top View) revised</p> <p>10, 11 Table 1.7 Pin Name Information by Pin Number (1) and Table 1.8 Pin Name Information by Pin Number (2) revised</p> <p>12, 13 Table 1.9 Pin Functions (1) and Table 1.10 Pin Functions (2) revised</p> <p>19 Table 4.1 SFR Information (1); • 0008h: Module Standby Control Register, MSTCR, 00h added • 001Ch: “00h” → “00h, 1000000b” revised • NOTE6 added</p> <p>20 Table 4.2 SFR Information (2); • 005Fh: Capture Interrupt Control Register, CAPIC, XXXXX000b added</p> <p>22 Table 4.4 SFR Information (4); • 00DCh: “00DDh” → “00DCh” revised • 00F5h: “XXXX00XXb” → “00h” revised</p> <p>23 Table 4.5 SFR Information (5); • 0105h: LIN Special Function Register, LINCR2, 00h added</p> <p>30 Table 4.12 SFR Information (12); • 02C2h, 02C3h: A/D Register 1, AD1, XXh deleted • 02C4h, 02C5h: A/D Register 2, AD2, XXh deleted • 02C6h, 02C7h: A/D Register 3, AD3, XXh deleted</p> <p>31 Package Dimensions; “Diagrams showing the latest package dimensions... in the “Packages” section of the Renesas Technology website.” added</p> |
| 0.20 | Sep 15, 2006 | 31 to 54 | 5. Electrical Characteristics added |
| 0.30 | Dec 22, 2006 | 6 | Table 1.5 and Figure 1.1 revised |
| | | 7 | Table 1.6 and Figure 1.2 revised |
| | | 17 | Figure 3.1 revised |
| | | 18 | Figure 3.2 revised |

REVISION HISTORY
R8C/2A Group, R8C/2B Group Datasheet

| Rev. | Date | Description | |
|------|--|-------------|---|
| | | Page | Summary |
| 0.30 | Dec 22, 2006 | 19 | Table 4.1; <ul style="list-style-type: none"> • 000Ah: "00XX000b" → "00h" revised • 0008h: "Module Standby Control Register" → "Module Operation Enable Register" revised • 000Fh: "00011111b" → "00X11111b" revised |
| | | 37 | Table 5.11 revised |
| 1.00 | Feb 09, 2007 | All pages | "Preliminary" deleted |
| | | 3 | Table 1.2 revised |
| | | 5 | Table 1.4 revised |
| | | 6 | Table 1.5 and Figure 1.1 revised |
| | | 7 | Table 1.6 and Figure 1.2 revised |
| | | 17 | Figure 3.1 revised |
| | | 18 | Figure 3.2 revised |
| | | 19 | Table 4.1; <ul style="list-style-type: none"> • 0008h: "Module Standby Control Register" → "Module Operation Enable Register" revised • 000Ah: "00XX000b" → "00h" revised • 000Fh: "00011111b" → "00X11111b" revised • 002Bh: "High-Speed On-Chip Oscillator Control Register 6" added |
| | | 23 | Table 4.5; 0105h: "LIN Control Register 2" register name revised |
| | | 31 | Table 5.2 revised |
| | | 32 | Table 5.3 and Table 5.4; NOTE1 revised |
| | | 37 | Table 5.11 revised |
| | | 44 | Table 5.17 revised |
| | | 46 | Table 5.21 and Figure 5.11; "i = 0 to 2" revised |
| | | 48 | Table 5.24 revised |
| 50 | Table 5.28 revised, Figure 5.16 "i = 0 to 2" revised | | |
| 52 | Table 5.31 revised | | |
| 53 | Table 5.34 revised | | |
| 54 | Table 5.35 and Figure 5.21; "i = 0 to 2" revised | | |
| 2.00 | Oct 17, 2007 | All pages | "PTLG0064JA-A (64F0G) package" added |
| | | 3, 5 | Table 1.2 and Table 1.4; <ul style="list-style-type: none"> • Operating Ambient Temperature: Y version added • Package: 64-pin FLGA added |
| | | 6 to 7 | Table 1.5 and Figure 1.1 revised |
| | | 8 | Table 1.6 and Figure 1.2 revised |
| | | 10 | Figure 1.4 "64-pin LQFP Package" added |
| | | 11 | Figure 1.5 added |
| | | 19 to 20 | Figure 3.1 and Figure 3.2 revised |
| | | 24 | Table 4.4; 00F5h: "00h" → "000000XXb" revised |

| | |
|------------------|--------------------------------------|
| REVISION HISTORY | R8C/2A Group, R8C/2B Group Datasheet |
|------------------|--------------------------------------|

| Rev. | Date | Description | |
|------|--------------|--|---|
| | | Page | Summary |
| 2.00 | Oct 17, 2007 | 33 59 | Table 5.1; Pd: Rated Value "TBD" → "700" revised, "NOTE1" added Package Dimensions "PTLG0064JA-A (64F0G) package" added |
| 2.10 | Nov 26, 2007 | 2, 4 6, 7 8, 9 20, 21 22 35 41 | Table 1.1, Table 1.3 Clock: "Real-time clock (timer RE)" added Table 1.5 and Figure 1.1 revised Table 1.6 and Figure 1.2 revised Figure 3.1 and Figure 3.2 revised Table 4.1 002Ch: High-Speed On-Chip Oscillator Control Register 7 added Table 5.2 NOTE2 revised Table 5.11 revised |
| | | | |

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