THE DATASHEET OF

PSB 21373 H V1.1

www.win-source.net 0086-755-83957316

Data Sheet, DS 3, May 2002

SCOUT-DX

Siemens Codec with 2-Wire Data Transceiver Featuring Speakerphone Function

PSB 21373 Version 1.1

Wired Communications

Never stop thinking.

Data Sheet

Revision History:	**2002-05-13**	DS 3
Previous Version:	Prel. Data Sheet, DS2	

Page	Subjects (major changes since last revision)
Page 32	Figure 10 with clock signals added
Page 62	BCL=' 0' changed to BCL='1'
Page 80	BCL changed from 'low' to 'high'
Page 106	Note regarding AXI input added
Page 143	Recommendation regarding CRAM programming modified
Page 158	BCL is inverted compared to last description (DS1); figure 75 added
Page 161	'*Rising*' BCL edge changed to '*falling*' edge
Page 232	Figure 80 (BCL)modified
Page 234	SDX output delay added
Page 236	DC charateristics of transceiver modified

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Edition 2002-05-13

Published by Infineon Technologies AG,
St.-Martin-Strasse 53,
D-81541 München, Germany

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1 Overview

The SCOUT™-DX integrates all necessary functions for the completion of a cost effective digital voice terminal solution.

The SCOUT-DX combines the functionality of the ARCOFI®-SP PSB 2163 (Audio Ringing Codec Filter with Speakerphone) and a two wire line interface[1)] on a single chip.

The SCOUT-DX is suited for the use in basic PBX voice terminals just as, in combination with an additional device on the modular IOM®-2 interface, in high end featurephones e.g. with acoustic echo cancellation.

The transceiver implements the subscriber access functions for a digital terminal to be connected to the two wire line interface. It covers complete layer-1 and basic layer-2 functions for digital terminals.

The codec performs encoding, decoding, filtering functions and tone generation (ringing, audible feedback tones and DTMF signal). An analog front end offers three analog inputs and two analog outputs with programmable amplifiers.

The IOM-2 interface allows a modular design with functional extensions (e.g. acoustic echo cancellation, modem extension) by connecting other voice/data devices to the SCOUT-DX.

A serial microcontroller interface (SCI) is supported.

The SCOUT-DX is a CMOS device offered in a P-MQFP-44 package and operates with a 5 V supply.

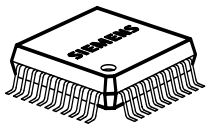
[1)] compatible to TP3406 of *National Semiconductor Corporation*

Siemens Codec with 2-Wire Data Transceiver Featuring Speakerphone Function SCOUT-DX

PSB 21373

Version 1.1 **CMOS**

1.1 Features



P-MQFP-44-1

- Serial control interface (SCI)
- IOM-2 interface in TE mode, single/double clock, two serial data strobe signals
- Various possibilities of microcontroller data access, data control and data manipulation to all IOM-2 timeslots
- Power supply 5 V
- Monitor channel handler (master/slave)
- Sophisticated power management for restricted power mode
- Programmable microcontroller clock output and reset (input/output) pins
- Advanced CMOS technology

Transceiver part

- Two wire transceiver with AMI coded 2B+D channels for loop length up to 1.8 km (6 kft)
- Conversion of the frame structure between the two wire line interface and IOM-2
- Receive timing recovery
- Continuously adapted receive thresholds
- Activation and deactivation procedures with automatic activation from power down state
- HDLC controller. Access to B1, B2 or D channels or the combination of them e.g. for 144 kbit data transmission (2B+D)
- FIFO buffer with 64 bytes per direction and programmable FIFO thresholds for efficient transfer of data packets

Type	Package
PSB 21373	P-MQFP-44-1

- Implementation of IOM-2 MONITOR and C/I-channel protocol to control peripheral devices
- Realization of layer 1 state machine in software possible
- Watchdog timer
- Programmable reset sources
- Test loops and functions

Codec part

- Applications in digital terminal equipment featuring voice functions
- Digital signal processing performs all CODEC functions
- Fully compatible with the ITU-T G.712 and ETSI (NET33) specification
- PCM A-Law/µ-Law (ITU-T G.711) and 8/16-bit linear data; maskable codec data
- Flexible configuration of all internal functions
- Three analog inputs for the handset microphone , the speakerphone and the headset
- Two differential outputs for a handset ear piece (200 Ω) and a loudspeaker (50 Ω)
- Flexible test and maintenance loopbacks in the analog front end and the digital signal processor
- Independent gain programmable amplifiers for all analog inputs and outputs
- Full digital speakerphone and loud hearing support without any external components (speakerphone test and optimization function is available)
- Enhanced voice data manipulation for features like:
  - Three-party conferencing
  - Voice monitoring
- Two transducer correction filters
- Side tone gain adjustment
- Flexible DTMF, tone and ringing generator
- Direct and indirect CRAM access

1.2 Pin Configuration

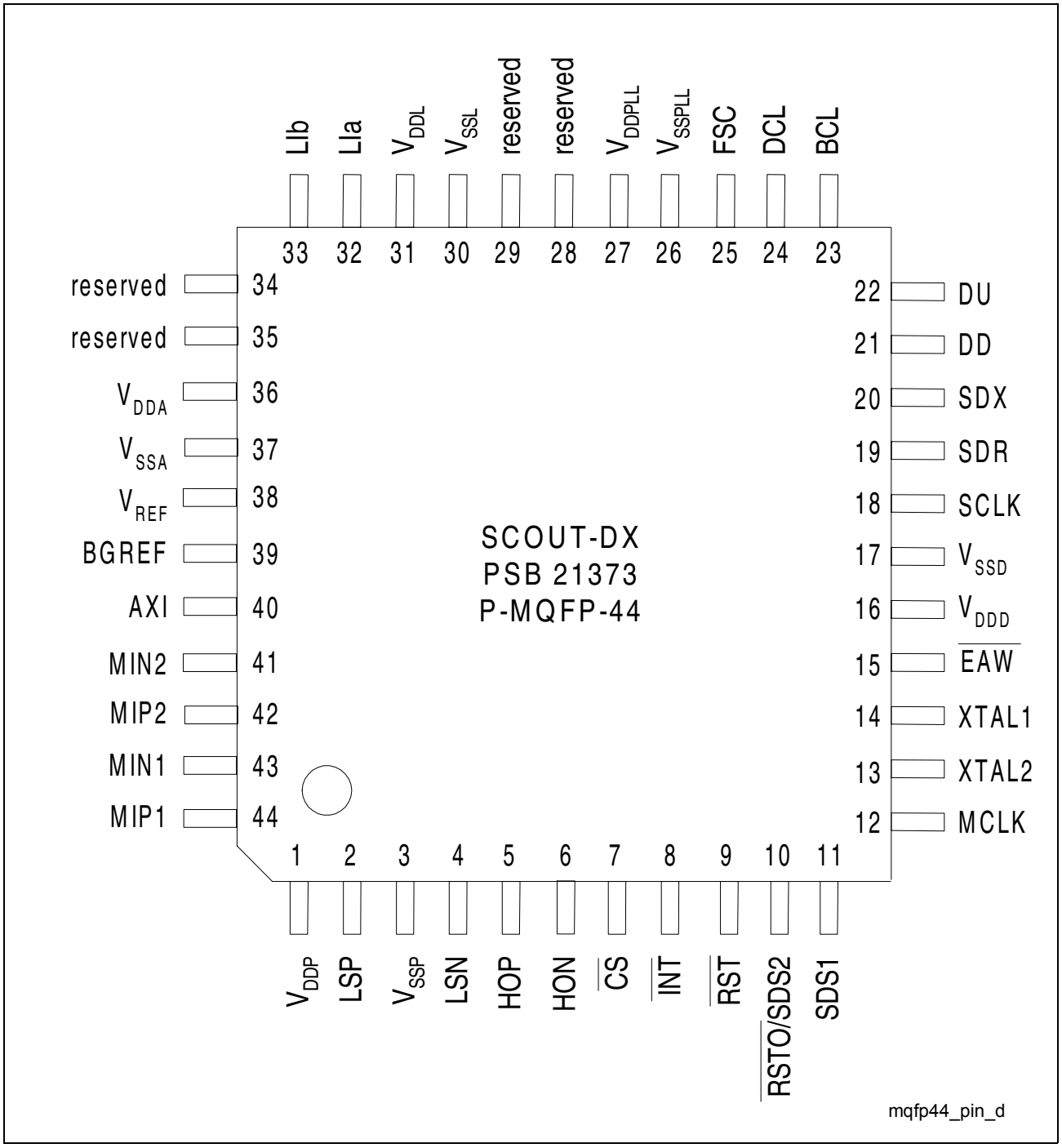


Figure 1
Pin Configuration

1.3 Logic Symbol

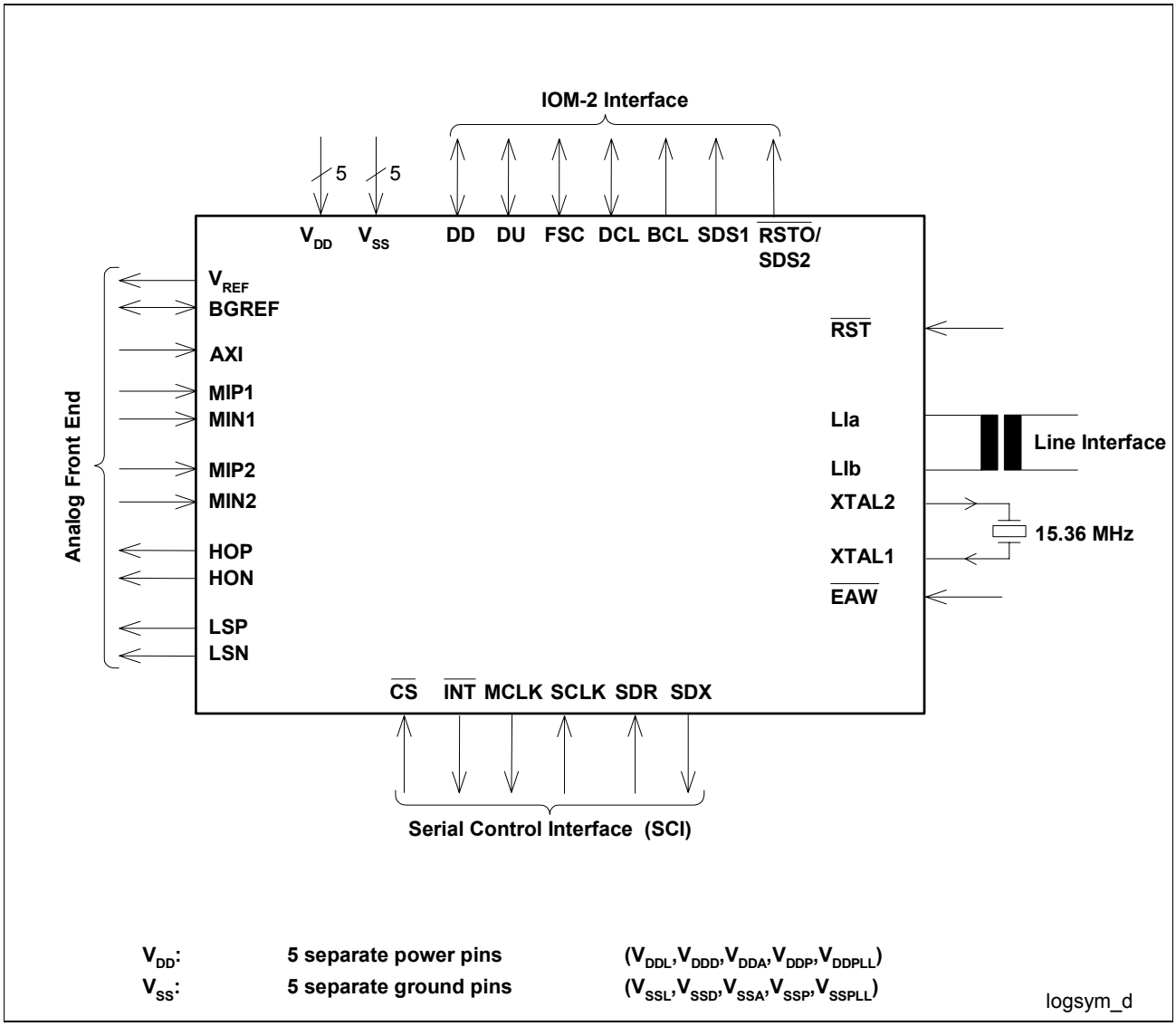


Figure 2
Logic Symbol of the SCOUT-DX in P-MQFP-44

1.4 Pin Definitions and Function

Table 1

Pin No.	Symbol	Input (I) Output (O) Open Drain (OD)	Function
			Power supply (5 V ± 5 %)
31	V_{DDL}	–	Supply voltage for line driver
16	V_{DDD}	–	Supply voltage for digital parts
36	V_{DDA}	–	Supply voltage for analog parts
1	V_{DDP}	–	Supply voltage for loudspeaker
27	V_{DDPLL}	–	Supply voltage for internal PLL
30	V_{SSL}	–	Ground for line driver
17	V_{SSD}	–	Ground for digital parts
37	V_{SSA}	–	Ground for analog parts
3	V_{SSP}	–	Ground for loudspeaker
26	V_{SSPLL}	–	Ground for internal PLL
			IOM-2 Interface
21	DD	I/OD/O	Data Downstream
22	DU	I/OD/O	Data Upstream
25	FSC	I/O	Frame Synchronization Clock (8 kHz)
24	DCL	I/O	Data Clock (double clock, 1.536 MHz)
23	BCL	O	Bit Clock (768kHz)
11	SDS1	O	**Programmable strobe signal or bit clock**
10	$\overline{\text{RSTO}}$/ SDS2	OD O	**Reset Output (active low)** **Strobe signal for each IOM® time slot and/or D channel indication (programmable)**
			RESET
9	$\overline{\text{RST}}$	I	Reset (active low)

Table 1

Pin No.	Symbol	Input (I) Output (O) Open Drain (OD)	Function
			Transceiver
32 33	LIa LIb	I/O I/O	Line Interface
13 14	XTAL2 XTAL1	OI I	Oscillator output Oscillator or 15.36 MHz input
15	$\overline{\text{EAW}}$	I	External Awake. A low level on this input starts the oscillator from the power down state and generates a reset pulse if enabled (see **chapter 7.2.10**)
			Microcontroller Interface
7	$\overline{\text{CS}}$	I	Chip Select (active low)
8	$\overline{\text{INT}}$	OD	**Interrupt request** (active low)
12	MCLK	O	**Microcontroller Clock**
18	SCLK	I	Clock for the serial control interface
19	SDR	I	Serial Data Receive
20	SDX	OD/O	Serial Data Transmit

Table 1

Pin No.	Symbol	Input (I) Output (O) Open Drain (OD)	Function
			Analog Frontend
38	V_{REF}	O	2.4 V Reference voltage for biasing external circuitry. An external capacity of ≥ 100 nF has to be connected.
39	BGREF	I/O	Reference Bandgap voltage for internal references. An external capacity of ≥ 22 nF has to be connected.
40	AXI	I	Single-ended Auxiliary Input
44 43	MIP1 MIN1	I I	Symmetrical differential Microphone Input 1
42 41	MIP2 MIN2	I I	Symmetrical differential Microphone Input 2
5 6	HOP HON	O O	Differential Handset ear piece Output for 200 Ω transducers
2 4	LSP LSN	O O	Differential Loudspeaker output for 50 Ω
			Reserved Pins
28	reserved	I	This input is not used for normal operation and must be connected to *VDD*.
29	reserved	I	This input is not used for normal operation and must be connected to *VSS*.
34	reserved	I	This input is not used for normal operation and must be connected to *VDD*.
35	reserved	I	This input is not used for normal operation and must be connected to *VDD*.

1.5 Typical Applications

The SCOUT-DX can be used in a variety of applications like

- PBX voice terminal with speakerphone (**Figure 3**)
- PBX voice terminal as featurephone with acoustic echo cancellation (**Figure 4**)
- PBX voice terminal with tip/ring extension (**Figure 5**)

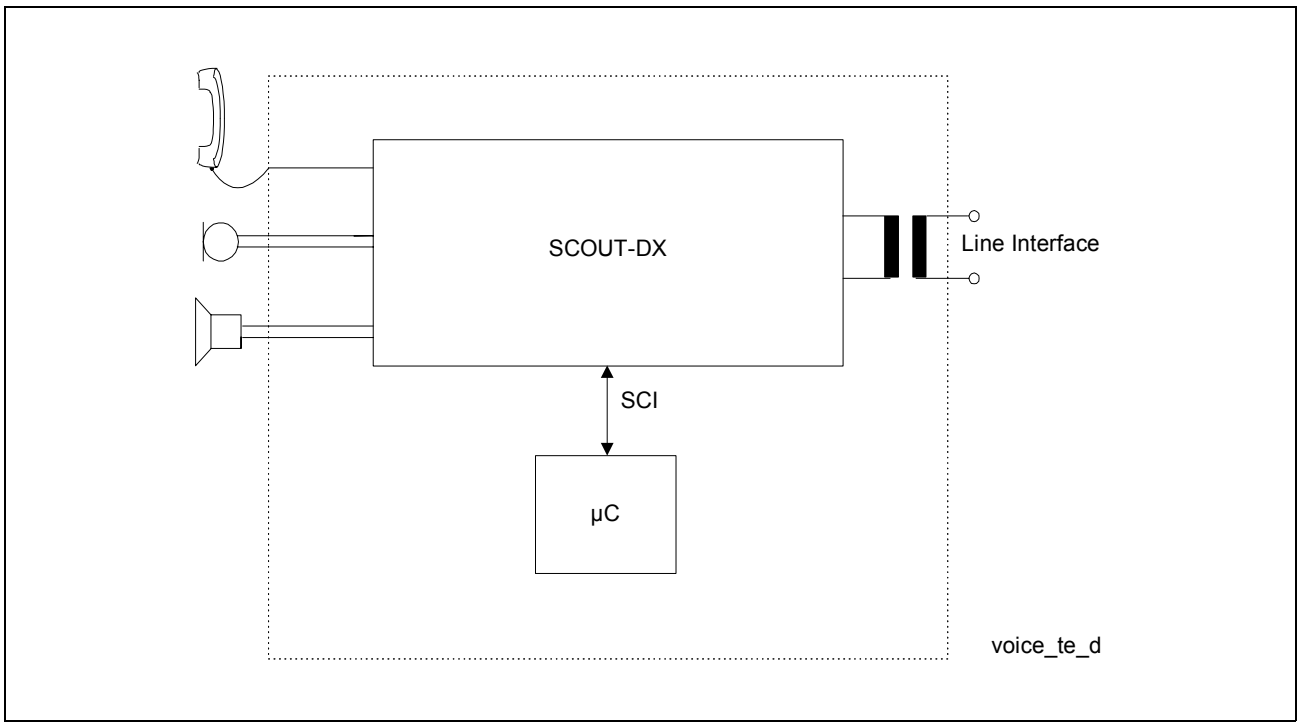


Figure 3
PBX Voice Terminal with Speakerphone

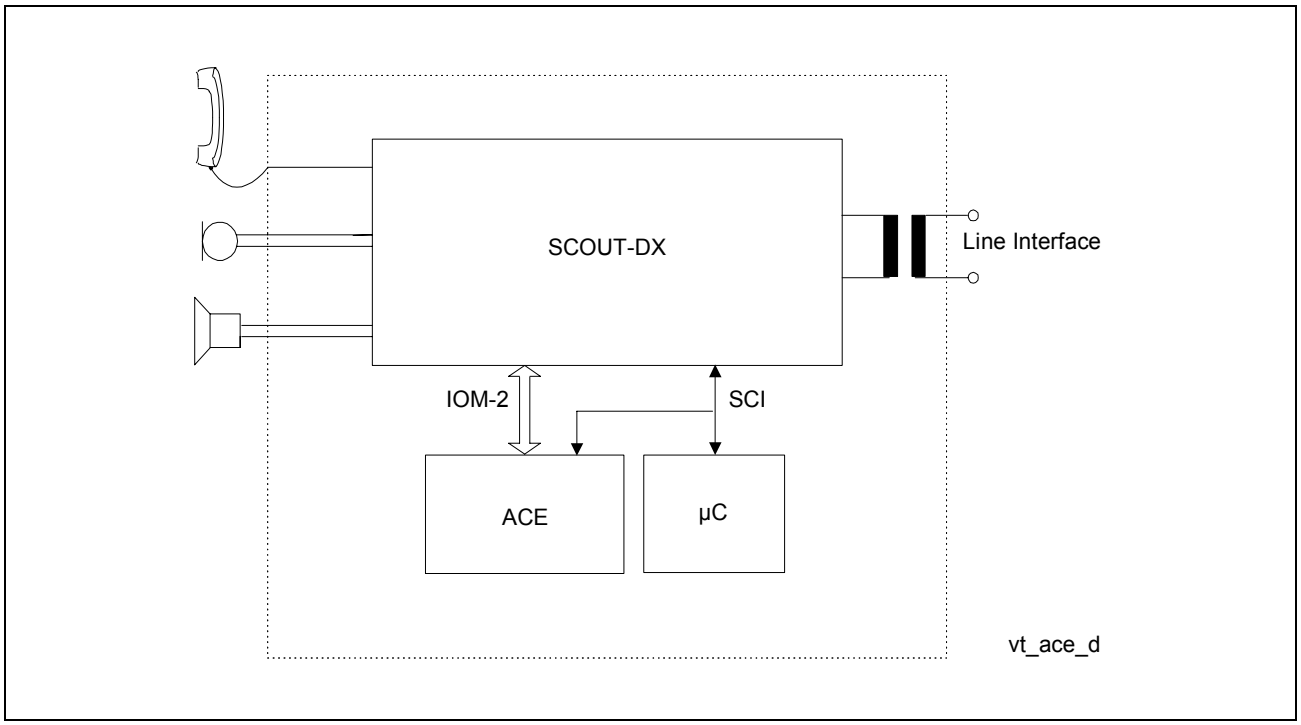


Figure 4
PBX Voice Terminal as Featurephone with Acoustic Echo Cancellation

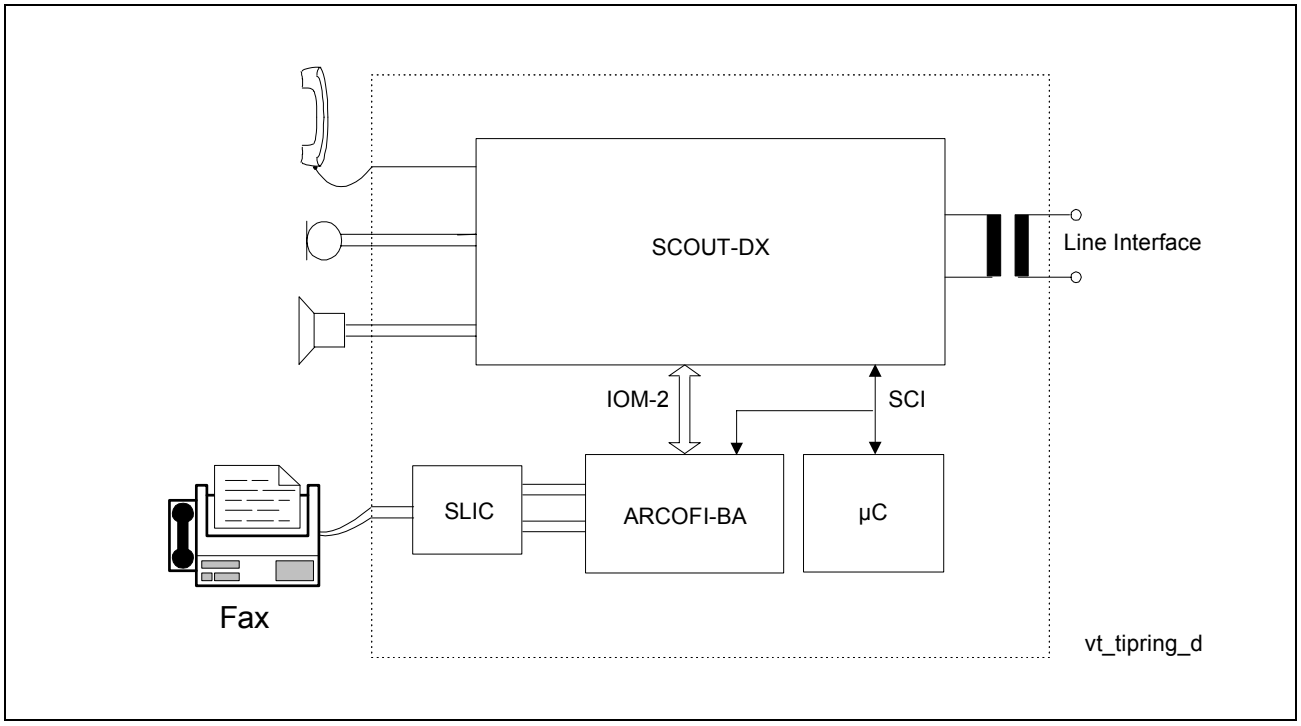


Figure 5
PBX Voice Terminal with Tip/Ring Extension

1.6 General Functions and Device Architecture

Figure 6 shows the architecture of the SCOUT-DX containing the following functional blocks:

- Two wire line interface
- Serial microcontroller interface
- HDLC controller with 64 byte FIFOs per direction and programmable FIFO threshold
- IOM-2 handler and interface for terminal application, MONITOR handler
- Clock and timing generation
- Digital PLL to synchronize IOM-2 to the line interface
- Reset generation (watchdog timer)
- Analog Front End (AFE) of the codec part
- Digital Signal Processor (DSP) for codec/filter functions, tone generation, voice data manipulation and speakerphone function

These functional blocks are described in the following chapters.

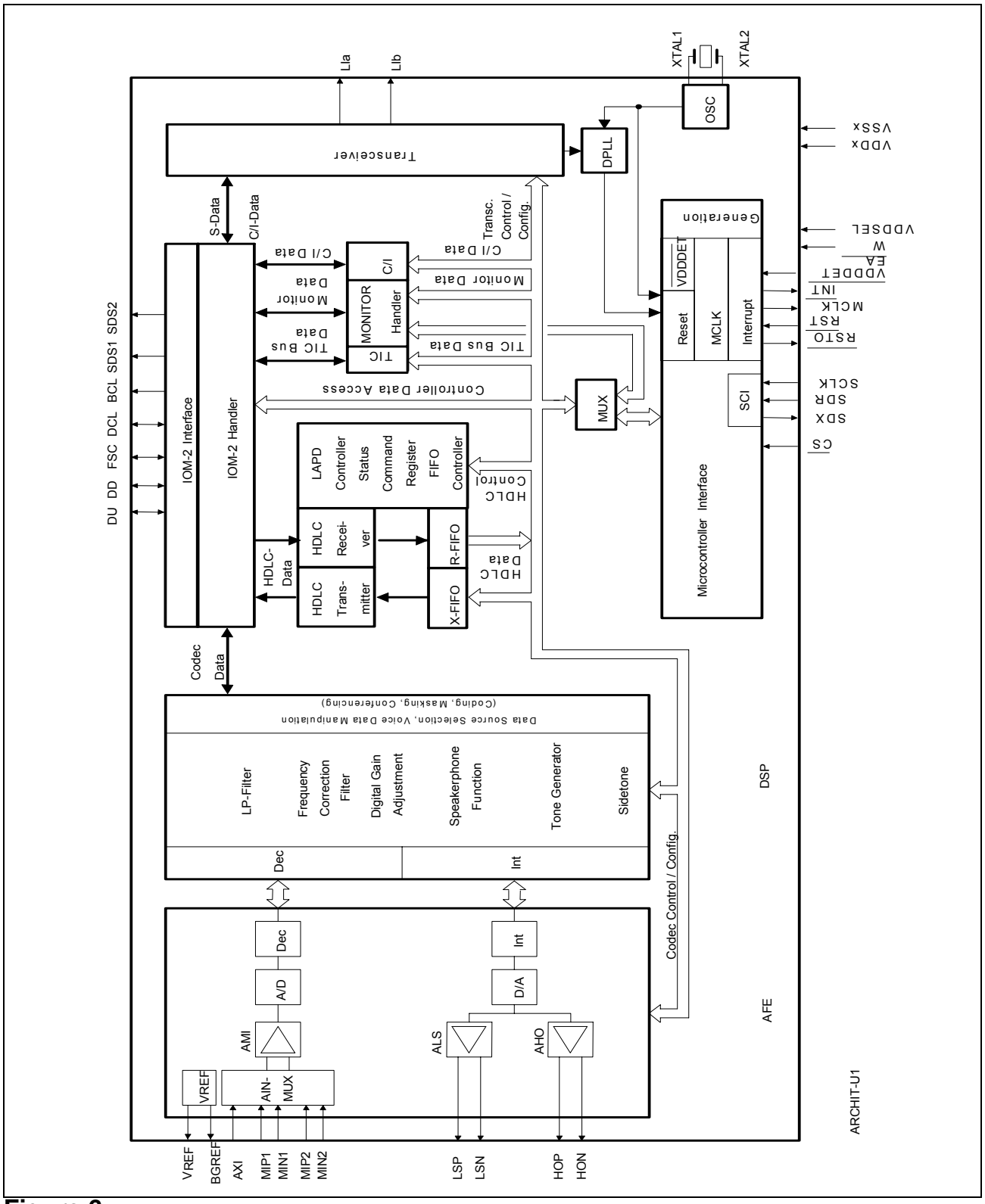


Figure 6
Architecture of the SCOUT-DX

2 Interfaces

The SCOUT-DX provides the following interfaces:

- Serial microcontroller interface together with a reset and microcontroller clock generation.
- IOM-2 interface as an universal backplane for terminals
- Line interface towards the two wire subscriber line
- Analog Front End (AFE) as interface between the analog transducers and the digital signal processor of the codec part

The microcontroller and IOM-2 interface are described in **chapter 2.1** or **2.2** respectively. The line interface is described in the **chapter 2.3**, the analog front end (AFE) in **chapter 4.1**

2.1 Microcontroller Interface

The SCOUT-DX supports a serial microcontroller interface. For applications where no controller is connected to the SCOUT-DX microcontroller interface programming is done via the IOM-2 MONITOR channel from a master device. In such applications the SCOUT-DX operates in the IOM-2 slave mode (refer to the corresponding chapter of the IOM-2 MONITOR handler).
The interface selections are all done by pinstrapping. The possible interface selections are listed in **table 2**. The selection pins are evaluated when the reset input $\overline{RST}$ is released. For the pin levels stated in the tables the following is defined:
'High': dynamic pin value which must be 'High' when the pin level is evaluated
V_{DD}, V_{SS}: static 'High' or 'Low' level

Table 2
Interface Selection

PIN $\overline{\textbf{CS}}$	**Interface Type/Mode**
'High'	Serial Control Interface (SCI)
V_{SS}	IOM-2 MONITOR Channel (Slave Mode)

The mapping of all accessible registers can be found in **figure 76** in **chapter 7**.
The microcontroller interface also consists of a microcontroller clock generation at pin MCLK and an interrupt request at pin $\overline{INT}$.

2.1.1 Serial Control Interface (SCI)

The serial control interface (SCI) is compatible to the SPI interface of Motorola or Siemens C510 family of microcontrollers.
The SCI consists of 4 lines: SCLK, SDX, SDR and $\overline{CS}$. Data are transferred via the lines SDR and SDX at the rate given by SCLK. The falling edge of $\overline{CS}$ indicates the beginning of a serial access to the registers. Incoming data is latched at the rising edge of SCLK and shifts out at the falling edge of SCLK. Each access must be terminated by a rising edge of $\overline{CS}$. Data is transferred in groups of 8-bits with the MSB first.
Figure 7 shows the timing of a one byte read/write access via the serial control interface.

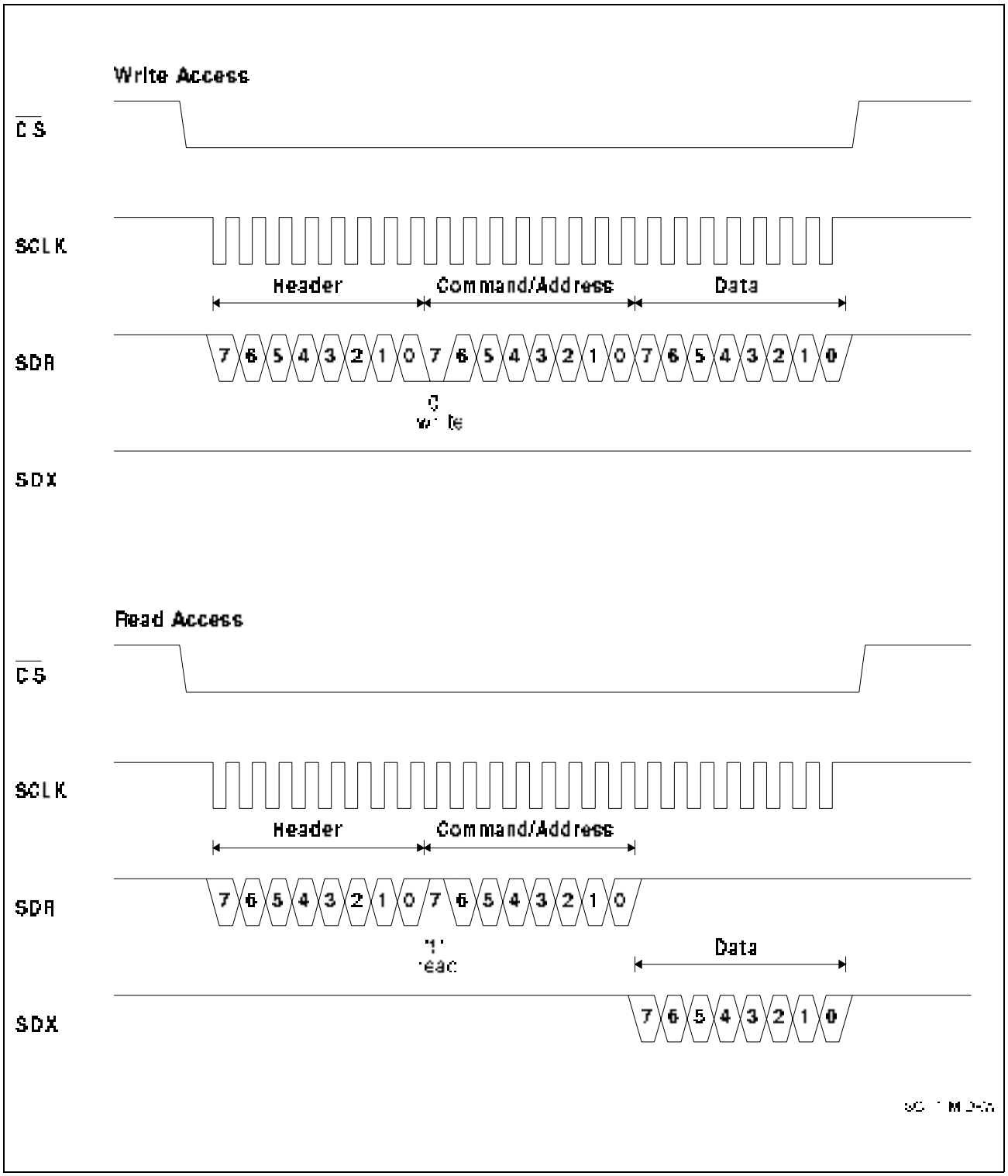


Figure 7
Serial Control Interface Timing

2.1.1.1 Programming Sequences

The principle structure of a read/write access to the SCOUT-DX registers via the serial control interface is shown in **figure 8**.

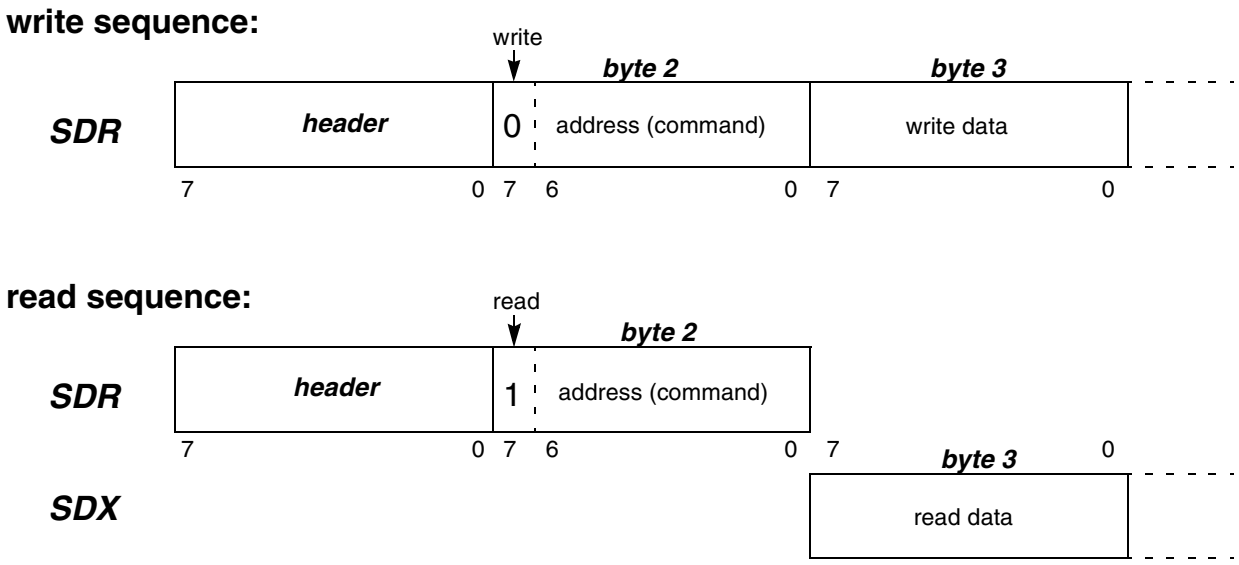


Figure 8
Serial Command Structure

A new programming sequence starts with the transfer of a header byte. The header byte specifies different programming sequences allowing a flexible and optimized access to the individual functional blocks of the SCOUT-DX.
The possible sequences are listed in **table 3** and are described afterwards.

Table 3
Header Byte Code

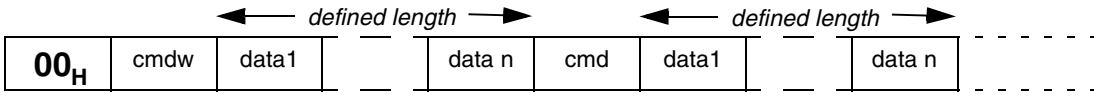
Header Byte	Sequence	Sequence Type	Access to
00_H	Cmd-Data-Data-Data	ARCOFI compatible, non-interleaved	Codec reg./CRAM (indirect)
08_H		ARCOFI compatible, interleaved	
40_H	Adr-Data-Adr-Data	non-interleaved	Address Range 00_H-$6F_H$
44_H			CRAM (80_H-FF_H)
48_H		interleaved	Address Range 00_H-$6F_H$
$4C_H$			CRAM (80_H-FF_H)

Table 3
Header Byte Code (cont'd)

$4A_H$	Adr-Data-Data-Data	Read-/Write-only	Address Range 00_H-$6F_H$
$4E_H$		(address auto increment)	CRAM (80_H-FF_H)
43_H		Read-/Write-only	Address Range 00_H-$6F_H$
41_H		non-interleaved	
49_H		interleaved	

Header 00_H: ARCOFI Compatible Sequence

This programming sequence is compatible to the SOP, COP and XOP command sequences of the ARCOFI. It gives indirect access to the codec registers 60_H-$6F_H$ and the CRAM (80_H-FF_H). The codec command word (cmdw) is followed by a defined number of data bytes (data n; n = 0, 1, 4 or 8). The number of data bytes depends on the codec command word. The commands can be applied in any order and number. The coding of the different SOP, COP and XOP commands is listed in the description of the command word (CMDW) in **chapter 4.8**.
Structure of the ARCOFI compatible sequence:



Header 40_H, 44_H: Non-interleaved A-D-A-D Sequences

The non-interleaved A-D-A-D sequences give direct read/write access to the address range 00_H-$6F_H$ (header 40_H) or the CRAM range 80_H-FF_H (header 44_H) respectively and can have any length. In this mode SDX and SDR can be connected together allowing data transmission on one line.
Example for a read/write access with header 40_H or 44_H:

SDR	header	wradr	wrdata	rdadr		rdadr		wradr	wrdata	
SDX					rddata		rdata			

Header 48_H, $4C_H$: Interleaved A-D-A-D Sequences

The interleaved A-D-A-D sequences give direct read/write access to the address range 00_H-$6F_H$ (header 48_H) or the CRAM range 80_H-FF_H (header $4C_H$) respectively and can have any length. This mode allows a time optimized access to the registers by

interleaving the data on SDX and SDR.
Example for a read/write access with header 48_H or $4C_H$:

SDR	header	wradr	wrdata	rdadr	rdadr	wradr	wrdata			
SDX					rddata	rddata				

Header $4A_H$, $4E_H$: Read-/Write-only A-D-D-D Sequences (Address Auto increment)

The A-D-D-D sequences give a fast read-/write-only access to the address range 00_H-$6F_H$ (header $4A_H$) or the CRAM range 80_H-FF_H (header $4E_H$) respectively.
The starting address (wradr, rdadr) is autoincremented after every data byte. The sequence can have any length and is terminated by the rising edge of $\overline{CS}$.

Example for a write access with header $4A_H$ or $4E_H$:

SDR	header	wradr	wrdata (wradr)	wrdata (wradr+1)	wrdata (wradr+2)	wrdata (wradr+3)	wrdata (wradr+4)	wrdata (wradr+5)	wrdata (wradr+6)	
SDX										

Example for a read access with header $4A_H$ or $4E_H$:

SDR	header	rdadr								
SDX			rddata (rdadr)	rddata (rdadr+1)	rddata (rdadr+2)	rddata (rdadr+3)	rddata (rdadr+4)	rddata (rdadr+5)	rddata (rdadr+6)	

Header 43_H: Read-/Write- only A-D-D-D Sequence

This mode (header 43_H) can be used for a fast access to the HDLC FIFO data. Any address (rdadr, wradr) in the range between 00h and 1F gives access to the current FIFO location selected by an internal pointer which is automatically incremented with every data byte following the first address byte. The sequence can have any length and is terminated by the rising edge of $\overline{CS}$.

Example for a write access with header 43_H:

SDR	header	wradr	wrdata (wradr)	wrdata (wradr)	wrdata (wradr)	wrdata (wradr)	wrdata (wradr)	wrdata (wradr)	wrdata (wradr)	
SDX										

Example for a read access with header 43_H:

SDR	header	rdadr								
SDX			rddata (rdadr)	rddata (rdadr)	rddata (rdadr)	rddata (rdadr)	rddata (rdadr)	rddata (rdadr)	rddata (rdadr)	

Header 41_H: Non-interleaved A-D-D-D Sequence

This sequence (header 41_H) allows in front of the A-D-D-D write access a non-interleaved A-D-A-D read access. This mode is useful for reading status information before writing to the HDLC XFIFO. The termination condition of the read access is the reception of the wradr. The sequence can have any length and is terminated by the rising edge of $\overline{CS}$.

Example for a read/write access with header 41_H:

SDR	header	rdadr		rdadr		wradr	wrdata (wradr)	wrdata (wradr)	wrdata (wradr)	
SDX			rddata		rddata					

Header 49_H: Interleaved A-D-D-D Sequence

This sequence (header 49_H) allows in front of the A-D-D-D write access an interleaved A-D-A-D read access. This mode is useful for reading status information before writing to the HDLC XFIFO. The termination condition of the read access is the reception of the wradr. The sequence can have any length and is terminated by the rising edge of the $\overline{CS}$ line.

Example for a read/write access with header 49_H:

SDR	header	rdadr	rdadr	wradr	wrdata (wradr)	wrdata (wradr)	wrdata (wradr)			
SDX			rddata	rddata						

2.1.2 Interrupt Structure and Logic

Special events in the SCOUT-DX are indicated by means of a single interrupt output, which requests the host to read status information from the SCOUT-DX or transfer data from/to the SCOUT-DX.

Since only one $\overline{\text{INT}}$ request output is provided, the cause of an interrupt must be determined by the host reading the interrupt status registers of the SCOUT-DX.

The structure of the interrupt status registers is shown in **figure 9**.

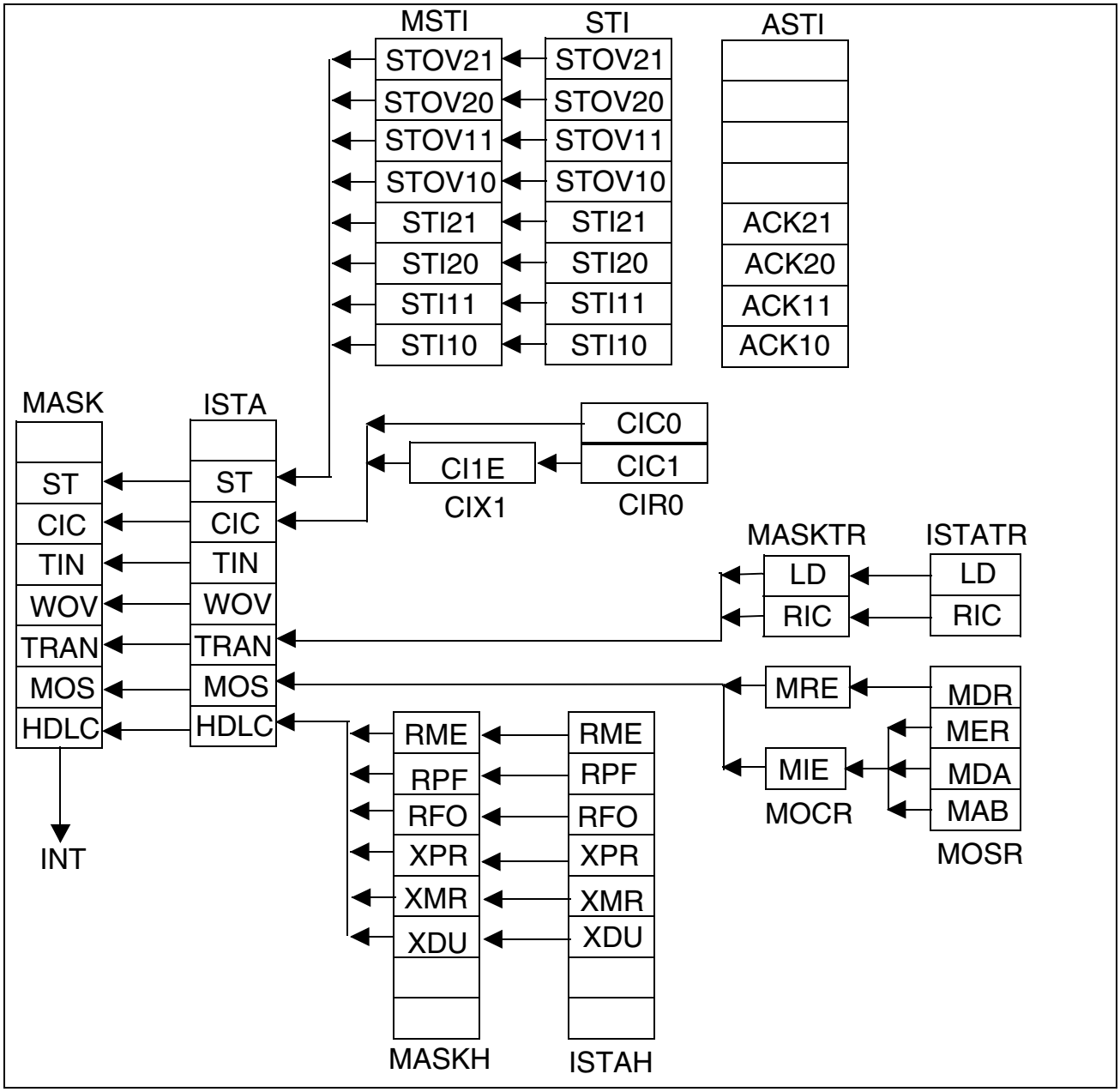


Figure 9
SCOUT-DX Interrupt Status Registers

Five interrupt bits in the ISTA register point at interrupt sources in the HDLC Controller (HDLC), Monitor- (MOS) and C/I- (CIC) handler, the transceiver (TRAN) and the synchronous transfer (ST). The timer interrupt (TIN) and the watchdog timer overflow (WOV) can be read directly from the ISTA register. All these interrupt sources are described in the corresponding chapters. After the SCOUT-DX has requested an interrupt by setting its $\overline{INT}$ pin to low, the host must read first the SCOUT-DX interrupt status register (ISTA) in the associated interrupt service routine. The $\overline{INT}$ pin of the SCOUT-DX remains active until all interrupt sources are cleared by reading the corresponding interrupt register. Therefore it is possible that the $\overline{INT}$ pin is still active when the interrupt service routine is finished.
Each interrupt indication of the interrupt status registers can selectively be masked by setting the respective bit in the MASK register.
For some interrupt controllers or hosts it might be necessary to generate a new edge on the interrupt line to recognize pending interrupts. This can be done by masking all interrupts at the end of the interrupt service routine (writing FF_H into the MASK register) and write back the old mask to the MASK register.

2.1.3 Microcontroller Clock Generation

The microcontroller clock is provided by the pin MCLK. Five clock rates are selectable by a programmable prescaler (see chapter clock generation **figure 73**) which is controlled by the MODE1.MCLK bits corresponding following table. By setting the clock divider selection bit (MODE1.CDS) a doubled MCLK frequency is available.
The possible MCLK frequencies are listed in **table 4**.

Table 4
MCLK Frequencies

MCLK Bits	MCLK Frequency with MODE1.CDS = ’0’	MCLK Frequency with MODE1.CDS = ’1’
’00’	3.84 MHz (default)	7.68 MHz (default)
’01’	0.96 MHz	1.92 MHz
’10’	7.68 MHz	15.36 MHz
’11’	disabled	disabled

The clock rate is changed after $\overline{CS}$ becomes inactive.

2.2 IOM-2 Interface

The SCOUT-DX supports the IOM-2 interface in terminal mode with single clock and double clock. The IOM-2 interface consists of four lines: FSC, DCL, DD and DU. The rising edge of FSC indicates the start of an IOM-2 frame. The FSC signal is generated by the receive DPLL which synchronizes to the received line frame. The DCL and the BCL output clock signals synchronize the data transfer on both data lines. The DCL is twice the bit rate, the BCL output rate is equal to the bit rate. The bits are shifted out with the rising edge of the first DCL clock cycle and sampled at the falling edge of the second clock cycle. The BCL clock together with the two serial data strobe signals (SDS1, SDS2) can be used to connect time slot oriented standard devices to the IOM-2 interface.
The IOM-2 interface can be enabled/disabled with the DIS_IOM bit in the IOM_CR register. The BCL clock output can be enabled separately with the EN_BCL bit.
The clock rate or frequency respectively of the IOM-signals in TE mode are:
DD, DU: 768 kbit/s
DCL: 1536 kHz (double clock rate); 768 kHz (single clock rate if DIS_TR = ’1’)
FSC: 8 kHz.

If the transceiver is disabled (TR_CONF.DIS_TR) the DCL and FSC pins become input and the HDLC and codec parts can still work via IOM-2. In this case it can be selected with the clock mode bit (IOM_CR.CLKM) between a double clock and a single clock input.

Note: One IOM-2 frame has to consist of a multiple of 16 (8) DCL clocks for a double (single) clock selection.

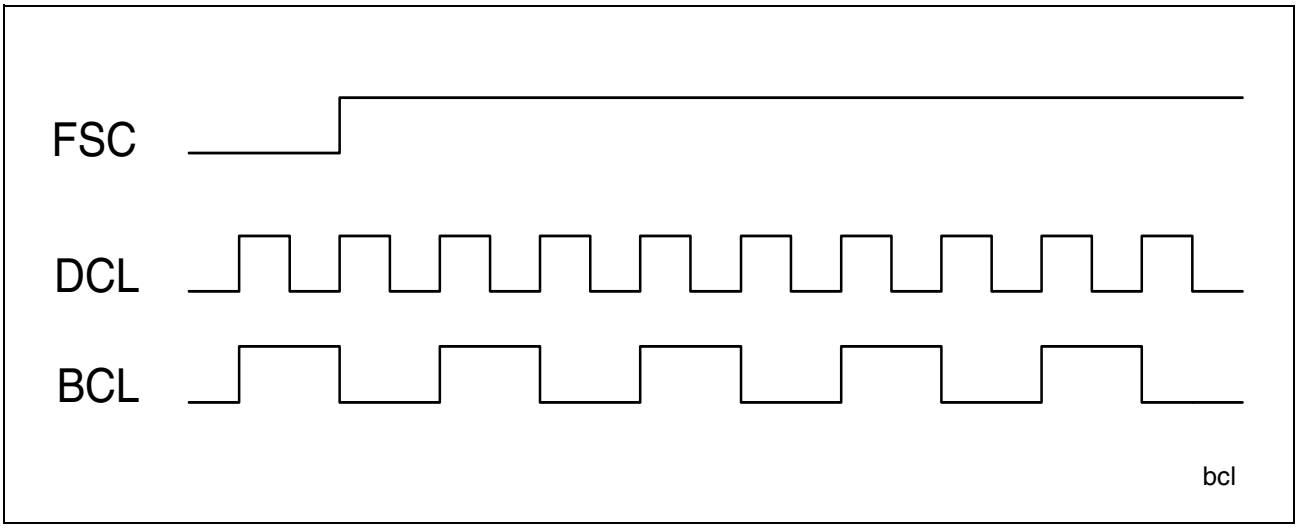


Figure 10 Clock waveforms

2.2.1 IOM-2 Frame Structure

The frame structure on the IOM-2 data ports (DU,DD) in IOM-2 terminal mode is shown in **figure 11.**

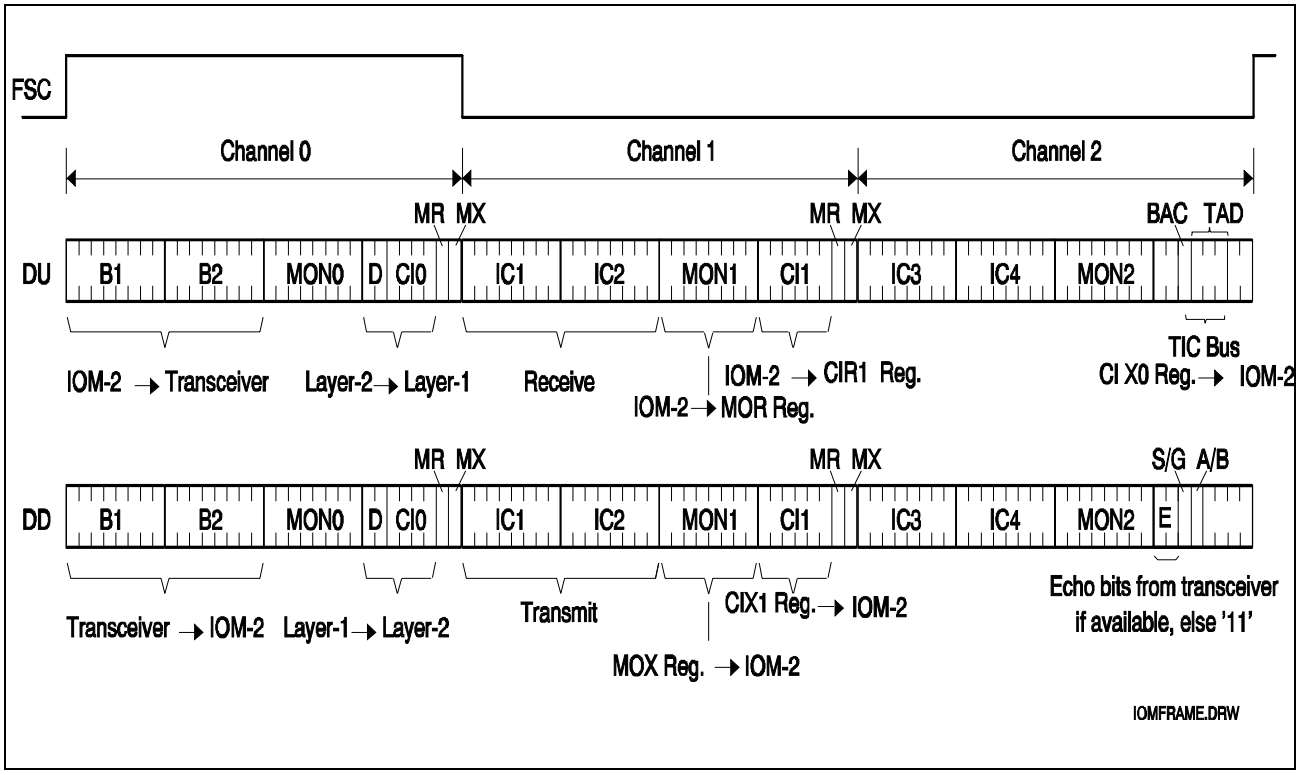


Figure 11
IOM®-2 Frame Structure in Terminal Mode

The frame is composed of three channels

- Channel 0 contains 144-kbit/s of user and signaling data (2B + D), a MONITOR programming channel (MON0) and a command/indication channel (CI0) for control and programming of the layer-1 transceiver.
- Channel 1 contains two 64-kbit/s intercommunication channels (IC) plus a MONITOR and command/indicate channel (MON1, CI1) to program or transfer data to other IOM-2 devices.
- Channel 2 is used for the TIC-bus access. Additionally channel 2 supports further IC and MON channels.

*Note: Each octett related to any integrated functional block can be programmed to any timeslot (**see chapter 7.3.2**) except the C/I0- and D- channels that are always related to timeslot 0.*

2.2.2 IOM-2 Handler

The IOM-2 handler offers a great flexibility for handling the data transfer between the different functional units of the SCOUT-DX and voice/data devices connected to the IOM-2 interface. Additionally it provides a microcontroller access to all time slots of the IOM-2 interface via the four controller data access registers (CDA). **Figure 12** shows the architecture of the IOM-2 handler. For illustrating the functional description it contains all configuration and control registers of the IOM-2 handler. A detailed register description can be found in **chapter 7.3**

The PCM data of the functional units

- Codec (CO)
- Transceiver (TR) and the
- Controller data access (CDA)

can be configured by programming the time slot and data port selection registers (TSDP). With the TSS bits (Time Slot Selection) the PCM data of the functional units can be assigned to each of the 12 PCM time slots of the IOM-2 frame. With the DPS bit (Data Port Selection) the output of each functional unit is assigned to DU or DD respectively. The input is assigned vice versa. With the control registers (CR) the access to the data of the functional units can be controlled by setting the corresponding control bits (EN, SWAP).

To avoid data collisions it has to be noticed that the C/I and D channels of the enabled transceiver are always related to time slot 3. If the monitor handler is enabled its data is related to time slot TS (2, 6 or 10) and the appropriate MR and MX bits to time slot TS+1 depending on the MCS bits of register MON_CR.

The IOM-2 handler provides also access to the

- MONITOR channel (MON)
- C/I channels (CI0,CI1)
- TIC bus (TIC) and
- D- and B-channel for HDLC control

The access to these channels is controlled by the registers HCI_CR and MON_CR.
The IOM-2 interface with the two Serial Data Strobes (SDS1,2) is controlled by the control registers IOM_CR, SDS1_CR and SDS2_CR.

The reset configuration of the SCOUT-DX IOM-2 handler corresponds to the defined frame structure and data ports in IOM-2 terminal mode (see **figure 11**).

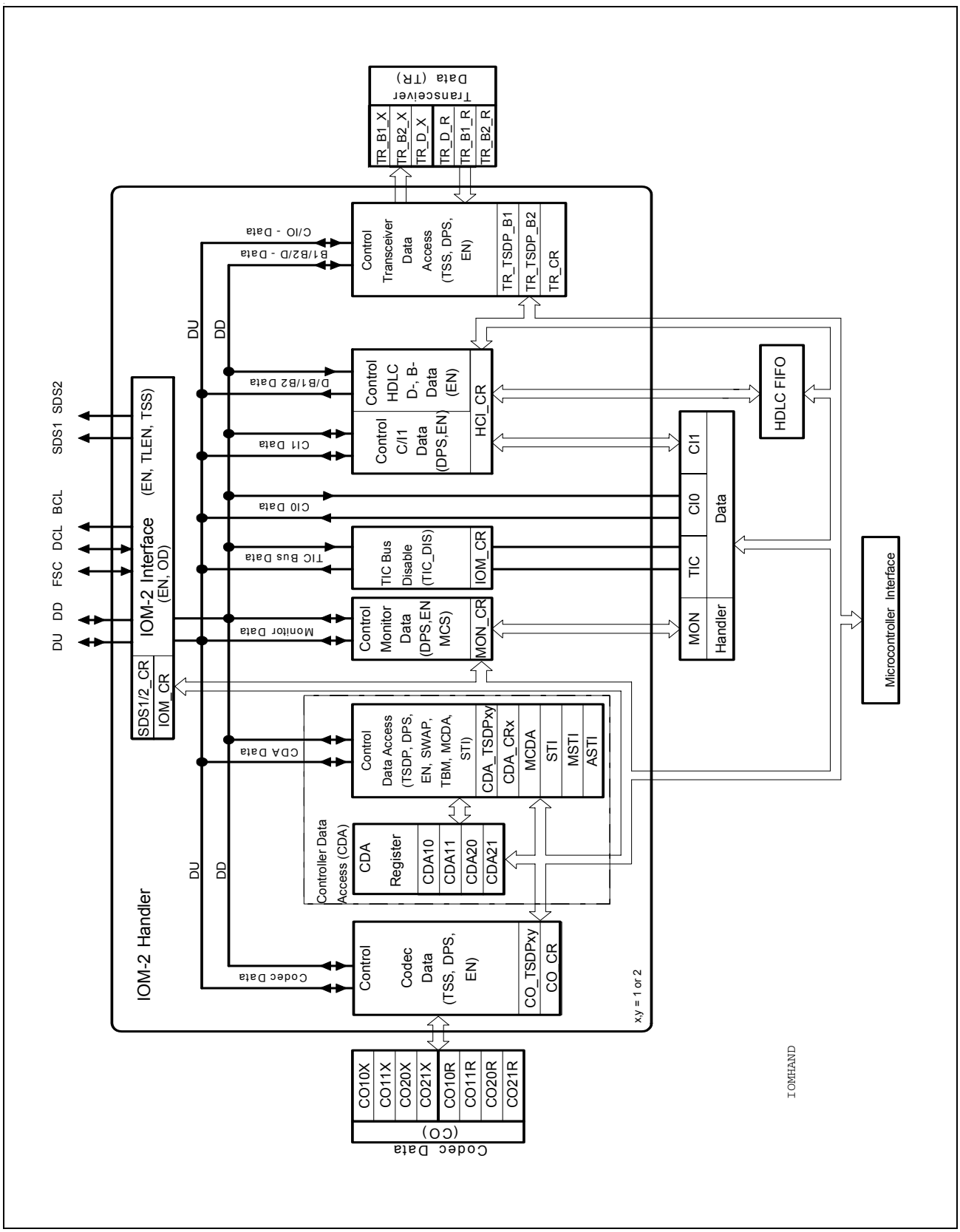


Figure 12
Architecture of the IOM Handler

2.2.2.1 Controller Data Access (CDA)

The IOM-2 handler provides with his four controller data access registers (CDA10, CDA11, CDA20, CDA21) a very flexible solution for the access to the 12
IOM-2 time slots by the microcontroller.

The functional unit CDA (controller data access) allows with its control and configuration registers

- looping of up to four independent PCM channels from DU to DD or vice versa over the four CDA registers
- shifting or switching of two independent PCM channels to another two independent PCM channels on both data ports (DU, DD)
- monitoring of up to four time slots on the IOM-2 interface simultaneously
- microcontroller read and write access to each PCM channel

The access principle which is identical for the two channel register pairs CDA10/11 and CDA20/21 is illustrated in **figure 13**. The index variables x,y used in the following description can be 1 or 2 for x, and 0 or 1 for y. The prefix 'CDA_' from the register names has been omitted for simplification.

To each of the four CDAxy data registers a TSDPxy register is assigned by which the time slot and the data port can be determined. With the TSS (Time Slot Selection) bits a time slot from 0...11 can be selected. With the DPS (Data Port Selection) bit the output of the CDAxy register can be assigned to DU or DD respectively. The time slot and data port for the output of CDAxy is always defined by its own TSDPxy register. The input of CDAxy depends on the SWAP bit in the control registers CRx.
If the SWAP bit = '0' the time slot and data port for the input and output of the CDAxy register is defined by its own TSDPxy register. The data port for the CDAxy input is vice versa to the output setting for CDAxy.
If the SWAP bit = '1', the input port and time slot of the CDAx0 is defined by the TSDP register of CDAx1 and the input port and time slot of CDAx1 is defined by the TSDP register of CDAx0.

The input and output of every CDAxy register can be enabled or disabled by setting the corresponding EN (-able) bit in the control register CDAx_CR. If the input of a register is disabled the output value in the register is retained.

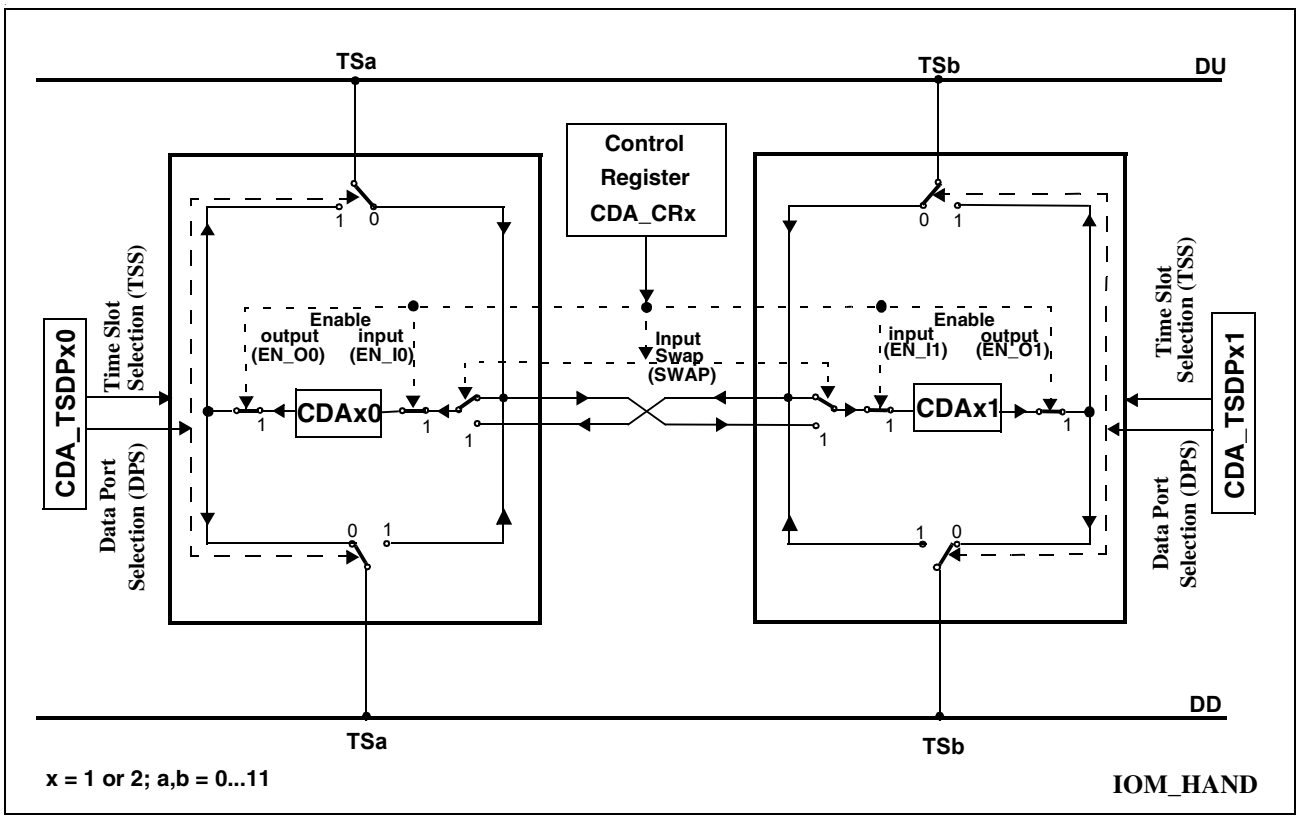


Figure 13
Data Access via CDAx0 and CDAx1 register pairs

2.2.2.1.1 Looping and Shifting Data

Figure 14 gives examples for typical configurations with the above explained control and configuration possibilities with the bits TSS, DPS, EN and SWAP in the registers TSDPxy or CDAx_CR:

a) looping IOM-2 time slot data from DU to DD or vice versa (SWAP = ’0’)

b) shifting data from TSa to TSb on DU and DD (SWAP = ’1’)

c) switching data from TSa (DU) to TSb(DD) and TSb (DU) to TSa (DD)

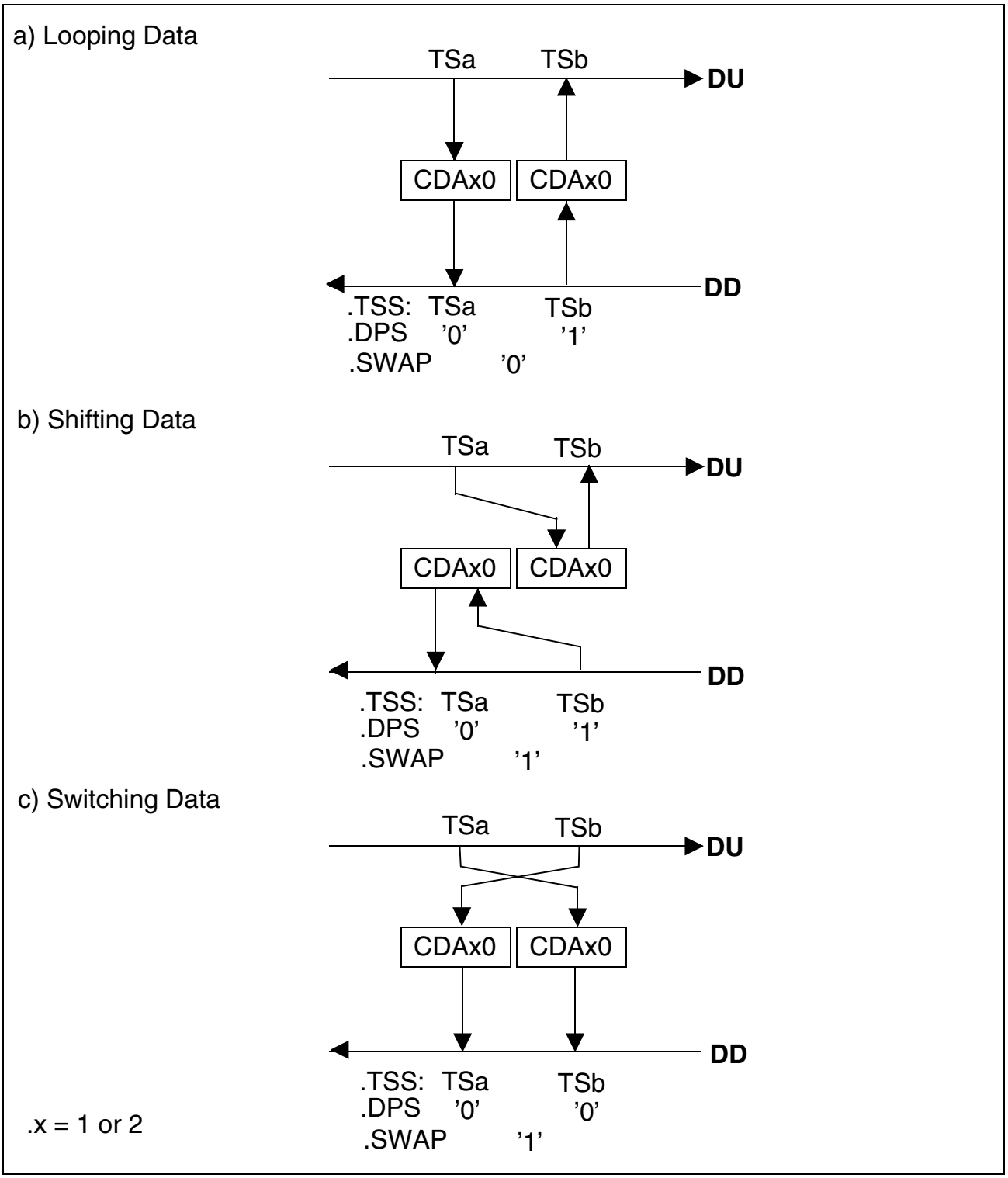


Figure 14
Examples for Data Access via CDAxy Registers
a) Looping Data
b) Shifting Data
c) Switching Data

2.2.2.1.2 Monitoring Data

Figure 15 gives an example for monitoring of two IOM-2 time slots each on DU or DD simultaneously. For monitoring on DU and/or DD the channel registers with even numbers (CDA10, CDA20) are assigned to time slots with even numbers TS(2n) and the channel registers with odd numbers (CDA11, CDA21) are assigned to time slots with odd numbers TS(2m+1) (n,m = 0...5). The user has to take care of this restriction by programming the appropriate time slots.

.

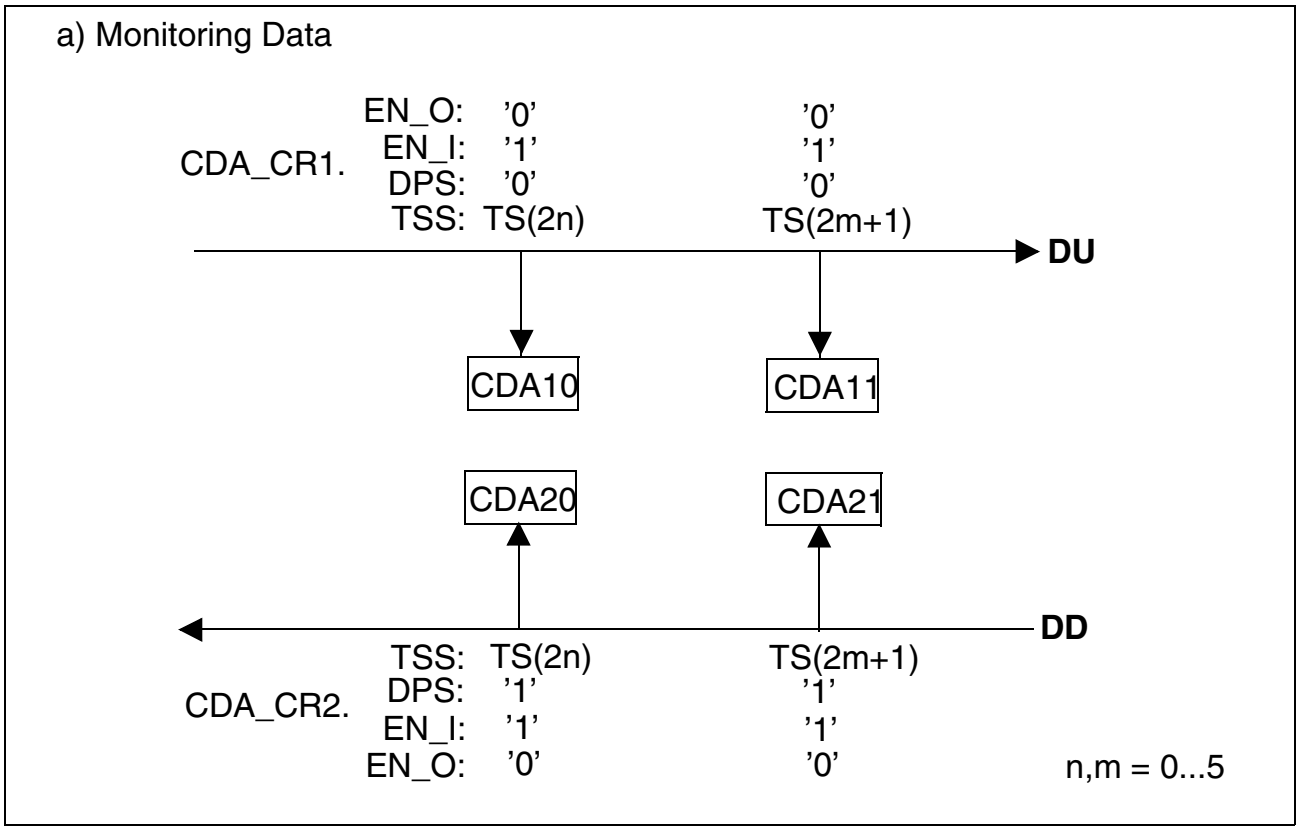


Figure 15
Example for Monitoring Data

2.2.2.1.3 Monitoring TIC Bus

Monitoring the TIC bus (TS11) is handled as a special case. The TIC bus can be monitored with the registers CDAx0 by setting the EN_TBM (Enable TIC Bus Monitoring) bit in the control registers CRx. The TSDPx0 must be set to 08_h for monitoring from DU or 88_h for monitoring from DD respectively.

2.2.2.1.4 Synchronous Transfer

While looping, shifting and switching the data can be accessed by the controller between the synchronous transfer interrupt (STI) and the status overflow interrupt (STOV).

The microcontroller access to the CDAxy registers can be synchronized by means of four programmable synchronous transfer interrupts (STIxy) and synchronous transfer overflow interrupts (STOVxy) in the STI register.
Depending on the DPS bit in the corresponding CDA_TSDPxy register the STIxy is generated two (for DPS='0') or one (for DPS='1') BCL clock after the selected time slot (CDA_TSDPxy.TSS). One BCL clock is equivalent to two DCL clocks.
A non masked synchronous transfer overflow ($STOVx_0y_0$) interrupt is generated if the appropriate $STIx_1y_1$ is not acknowledged in time. The $STIx_1y_1$ is acknowledged in time if bit $ACKx_1y_1$ in the ASTI register is set to '1' one BCL clock (for DPS='0') or zero BCL clocks (for DPS='1') before the time slot which is selected for the appropriate $STOVx_0y_0$.
If $STIx_1y_1$ and $STOVx_1y_1$ are not masked $STOVx_1y_1$ is only related to $STIx_1y_1$ (**see example a), c) and d) of figure 17**).
If $STIx_1y_1$ is masked but $STOVx_1y_1$ is not masked, $STOVx_0y_0$ is related to each enabled STIxy (**see example b) and d) of figure 17**).
Setting the corresponding bits in the MSTI (Mask Synchronous Transfer Interrupts) register masks the STIxy and the STOVxy interrupt. The interrupt structure of the synchronous transfer is shown in **figure 16**. Examples of the described synchronous transfer interrupt controlling are illustrated in **Figure 17**. A read to the STI register clears the STIxy and STOVxy interrupts.

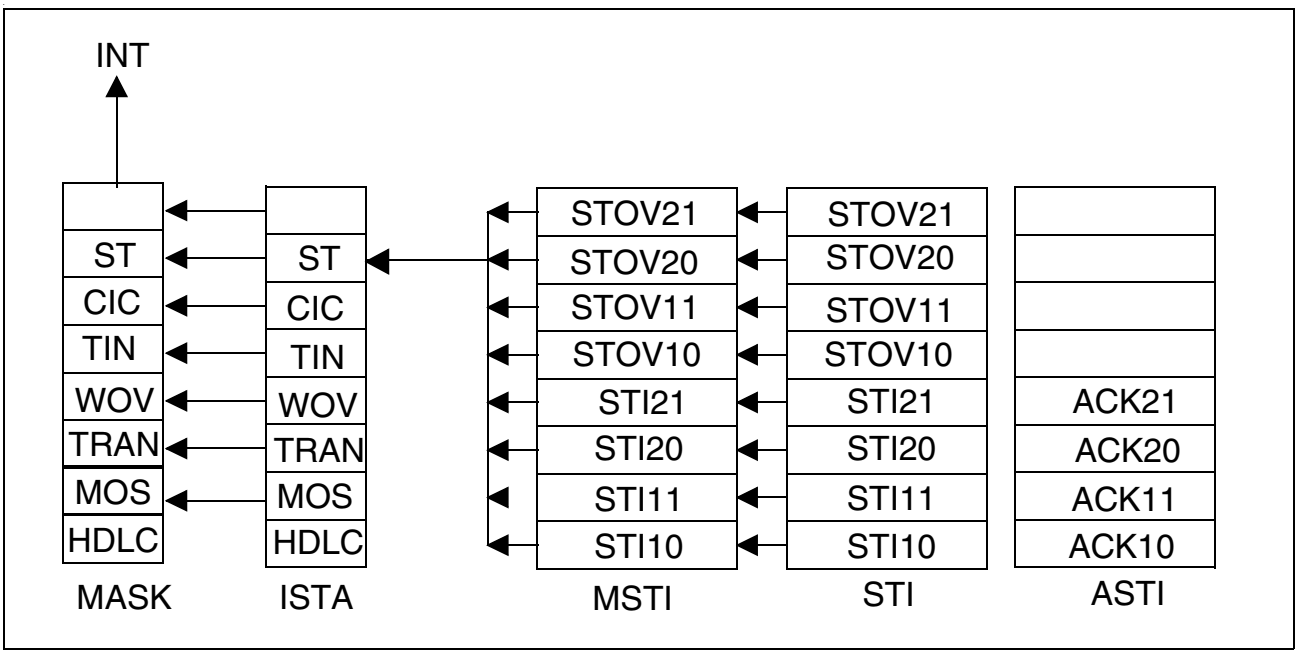


Figure 16
Interrupt Structure of the Synchronous Data Transfer

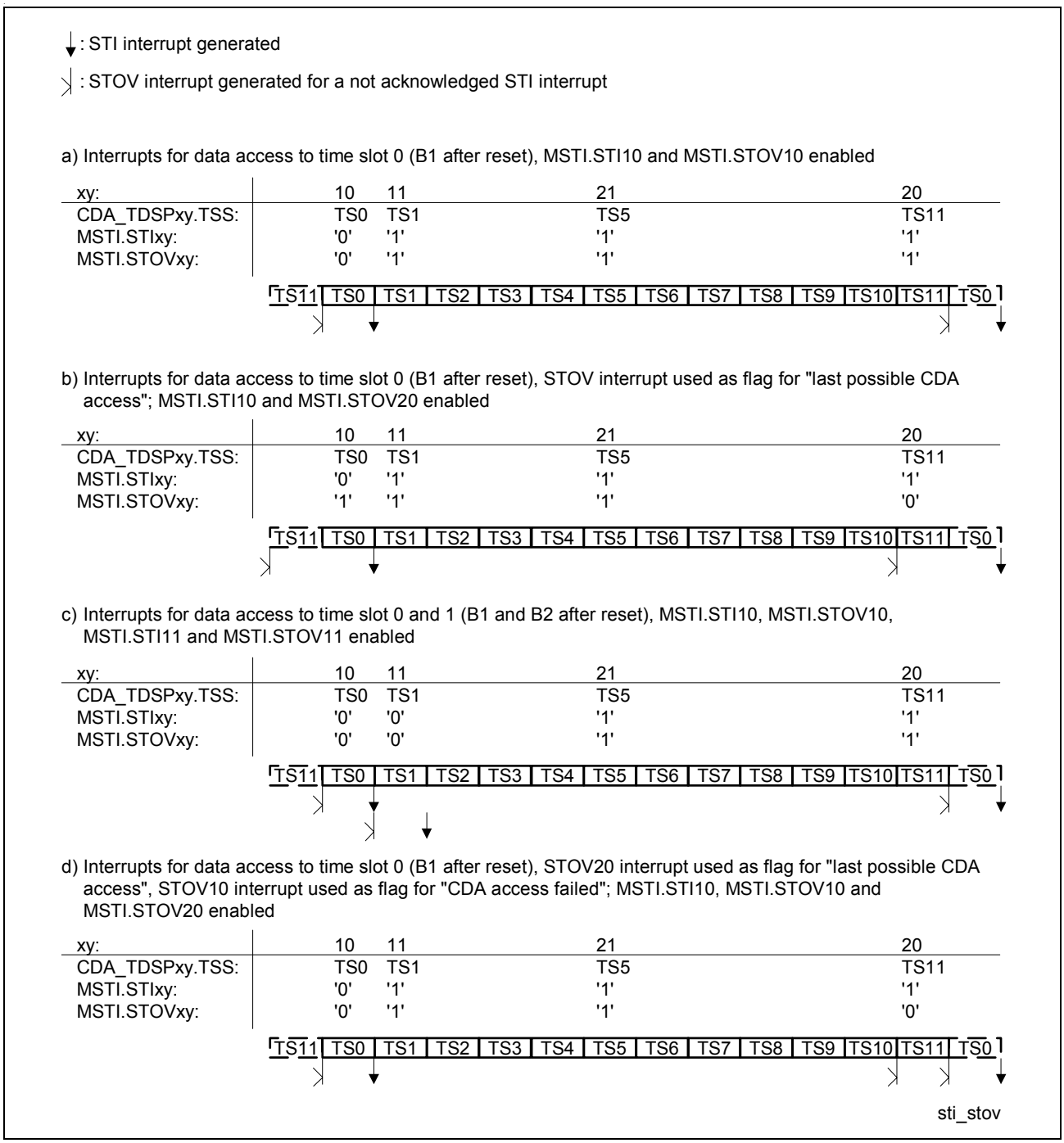


Figure 17
Examples for the Synchronous Transfer Interrupt Control with one enabled STIxy

Figure 18 shows the timing of looping TSa on DU to TSa on DD (a = 0...11) via CDAxy register. TSa is read in the CDAxy register from DU and is written one frame later on DD.

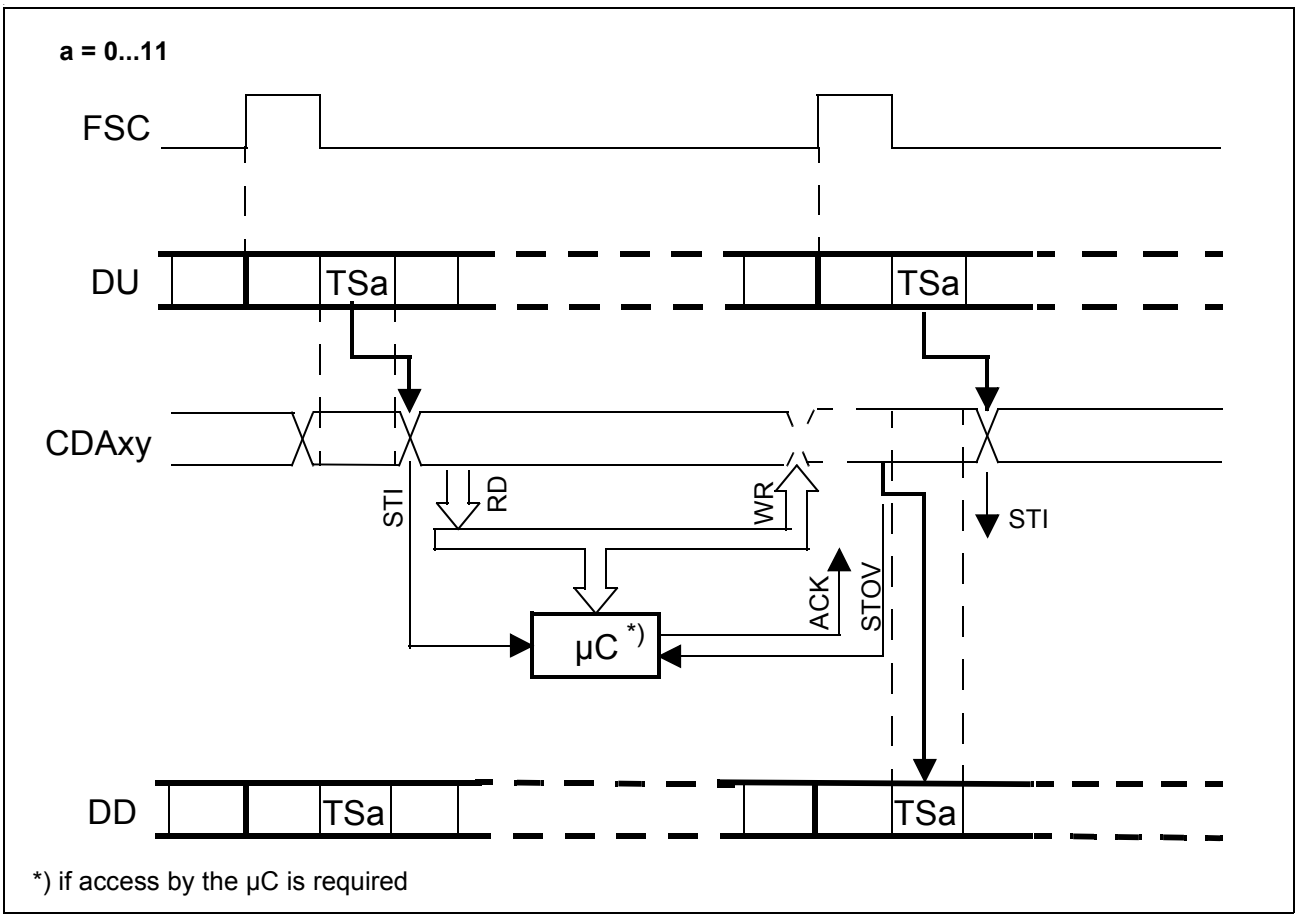


Figure 18
Data Access when Looping TSa from DU to DD

Figure 19 shows the timing of shifting data from TSa to TSb on DU(DD). In figure 19a) shifting is done in one frame because TSa and TSb didn't succeed direct one another (a,b = 0...9 and b ≥ a+2). In figure 19b) shifting is done from one frame to the following frame. This is the case when the time slots succeed one other (b = a+1) or b is smaller than a (b < a).

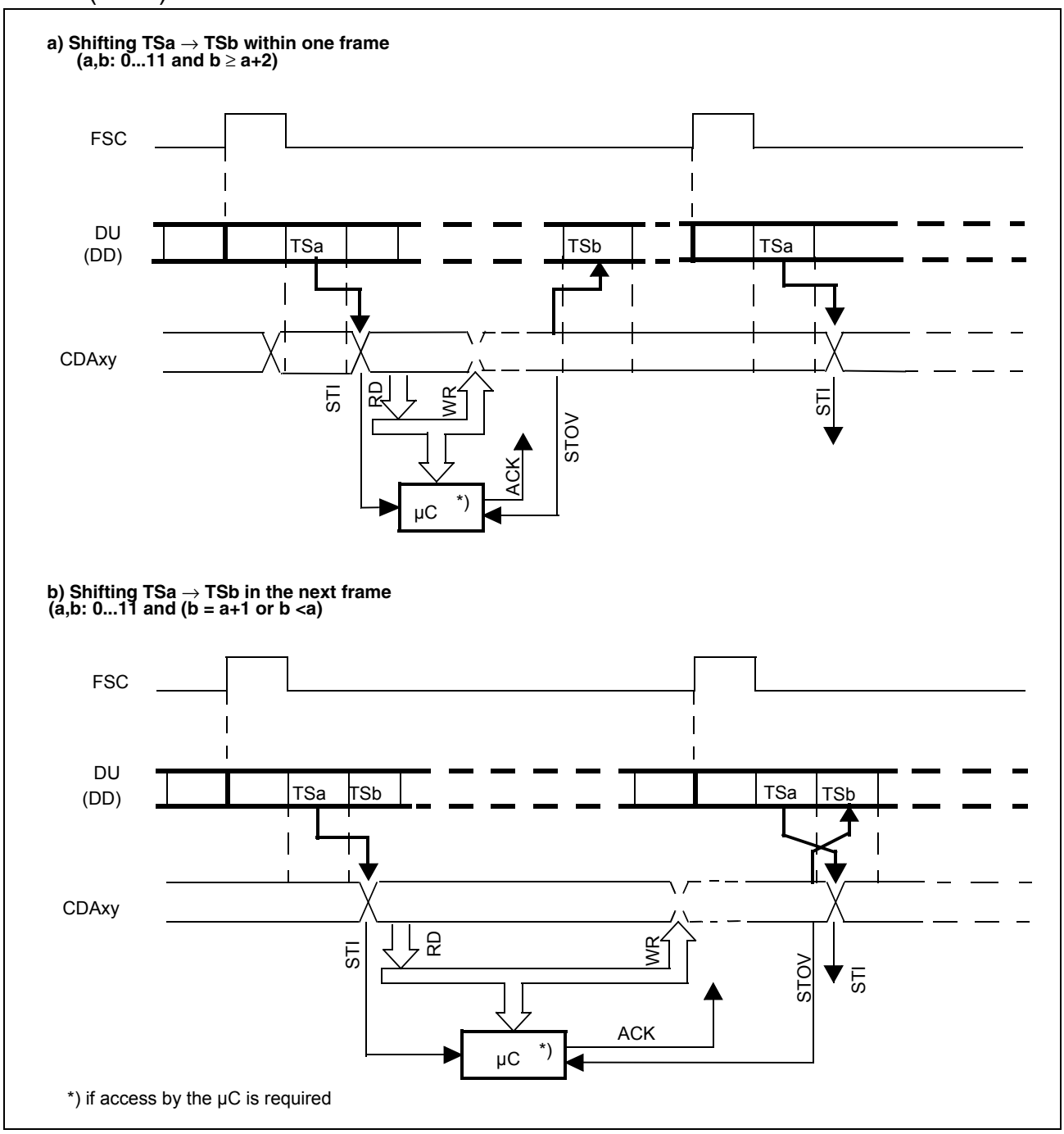


Figure 19
Data Access when Shifting TSa to TSb on DU (DD)

2.2.3 Serial Data Strobe Signal and strobed Data Clock

For time slot oriented standard devices connected to the IOM-2 interface the SCOUT-DX provides two independent data strobe signals SDS1 and SDS2. The SDS2 function is shared with the $\overline{\text{RSTO}}$ function at pin $\overline{\text{RSTO}}$/SDS2, therefore the SDS2 functionality must be selected by setting the RSS bits in the MODE1 register to ’01’.

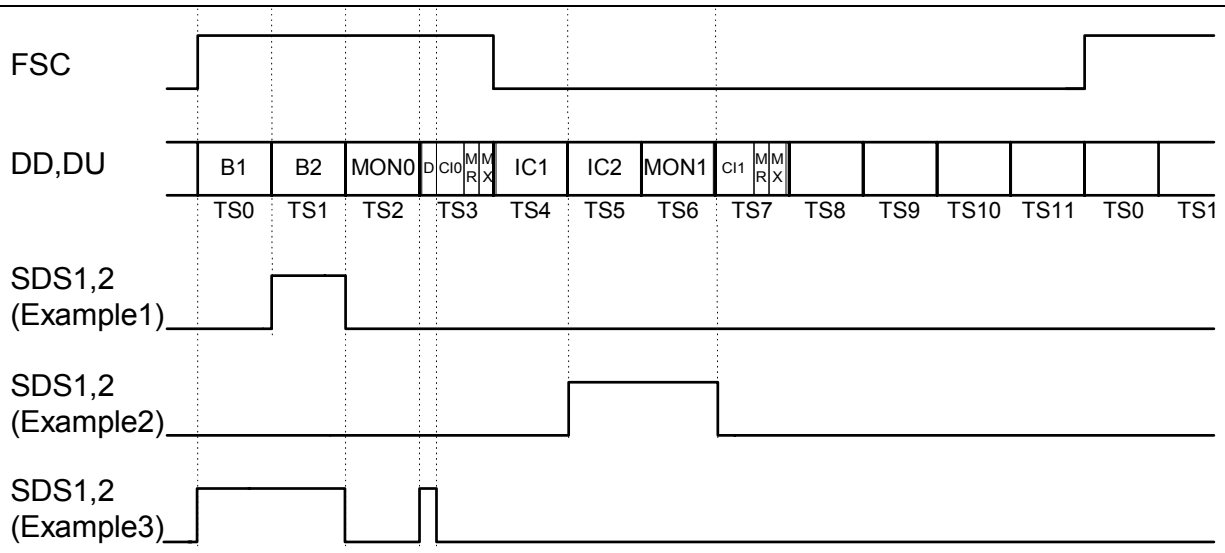
Instead of a data strobe signal a strobed IOM bit clock can be provided on pin SDS1 and SDS2.

2.2.3.1 Serial Data Strobe Signal

The two strobe signals can be generated with every 8-kHz frame and are controlled by the registers SDS1/2_CR. By programming the TSS bits and three enable bits (ENS_TSS, ENS_TSS+1, ENS_TSS+3) a data strobe can be generated for the IOM-2 time slots TS, TS+1 and TS+3 and any combination of them.

The data strobes for TS and TS+1 are always 8 bits long (bit7 to bit0) whereas the data strobe for TS+3 is always 2 bits long (bit7, bit6).

Figure 20 shows three examples for the generation of a strobe signal. In example 1 the SDS is active during channel B2 on IOM-2 whereas in the second example during IC1 and IC2. The third example shows a strobe signal for 2B+D channels which is used e.g. at an IDSL (144kbit/s) transmission.



Example 1: TSS = '0_H'
ENS_TSS = '0'
ENS_TSS+1 = '1'
ENS_TSS+3 = '0'

Example 2: TSS = '5_H'
ENS_TSS = '1'
ENS_TSS+1 = '1'
ENS_TSS+3 = '0'

Example 3: TSS = '0_H'
ENS_TSS = '1'
ENS_TSS+1 = '1'
ENS_TSS+3 = '1'

strobe.vsd

Figure 20
Data Strobe Signal

2.2.3.2 Strobed IOM Bit Clock

The strobed IOM bit clock is active during the programmed window (see **chapter 7.3.8**). Outside the programmed window a ’0’ is driven. Two examples are shown in **figure 21**.

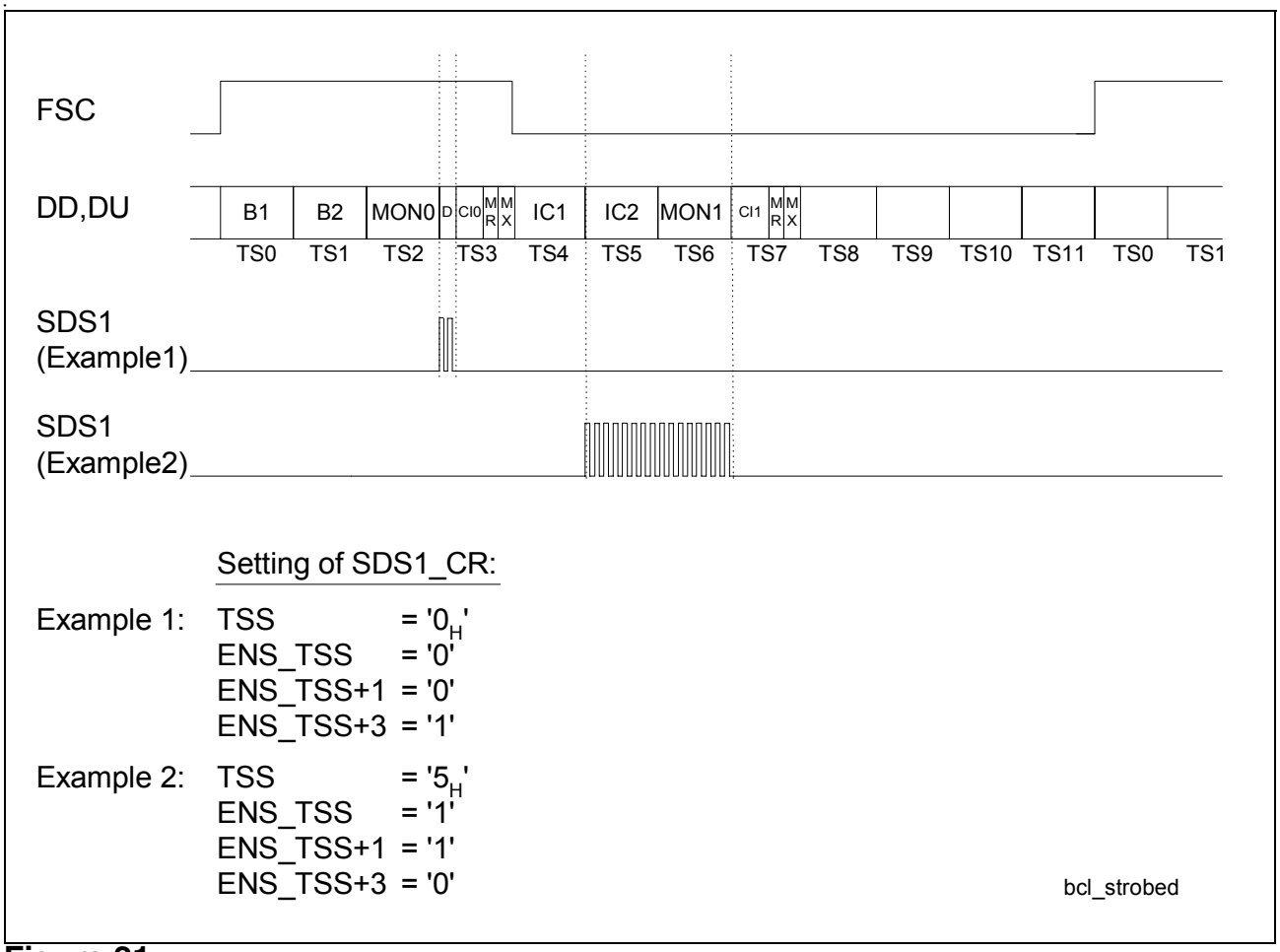


Figure 21
Strobed IOM Bit Clock. Register SDS_CONF programmed to 01_H or 03_H

2.2.4 IOM-2 Monitor Channel

The IOM-2 MONITOR channel (**see figure 11**) is utilized for information exchange between the SCOUT-DX and other devices connected to the MONITOR channel.

The MONITOR channel data can be controlled by the bits in the MONITOR control register (MON_CR). For the MONITOR data one of the three IOM channels can be selected by setting the MONITOR channel selection bits (MCS). The DPS bit in the same register selects between an output on DU or DD respectively and with EN_MON the MONITOR data can be enabled/disabled. The default value is MONITOR channel 0 (MON0) enabled and transmission on DD.

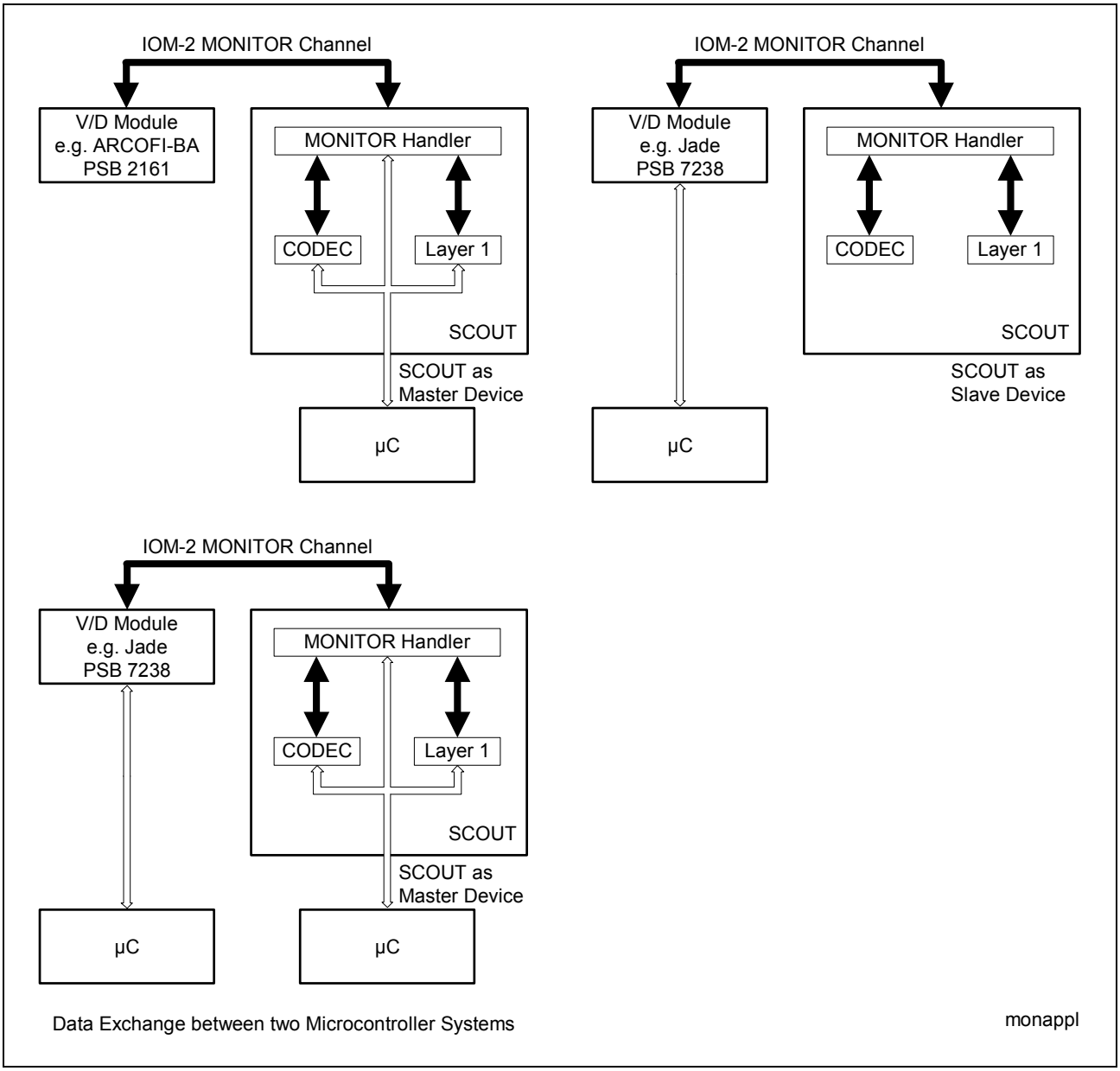


Figure 22
Examples of MONITOR Channel Applications

The MONITOR channel can be used in following applications which are illustrated in **figure 22**:

- As a **master device** the SCOUT-DX can program and control other devices attached to the IOM-2 which do not need a microcontroller interface e.g. ARCOFI-BA PSB 2161. This facilitates redesigning existing terminal designs in which e.g. an interface of an expansion slot is realized with IOM-2 interface and monitor programming.
- As a **slave device** the codec and the transceiver part of the SCOUT-DX is programmed and controlled from a master device on IOM-2 (e.g. JADE PSB 7238). This is used in applications where no microcontroller is connected directly to the SCOUT-DX. The HDLC controlling is processed by the master device therefore the HDLC data is transferred via IOM-2 interface directly to the master device.
- For **data exchange** between two microcontroller systems attached to two different devices on one IOM-2 backplane. Use of the MONITOR channel avoids the necessity of a dedicated serial communication path between the two systems. This simplifies the system design of terminal equipment.

2.2.4.1 Handshake Procedure

The MONITOR channel operates on an asynchronous basis. While data transfers on the bus take place synchronized to frame sync, the flow of data is controlled by a handshake procedure using the MONITOR Channel Receive (MR) and MONITOR Channel Transmit (MX) bits. Data is placed onto the MONITOR channel and the MX bit is activated. This data will be transmitted once per 8-kHz frame until the transfer is acknowledged via the MR bit.

The MONITOR channel protocol is described In the following section and illustrated in **Figure 23**. The relevant control and status bits for transmission and reception are listed in **table 5** and **table 6**.

Table 5
Transmission of MONITOR Data

Control/ Status Bit	Register	Bit	Function
Control	MOCR	MXC	MX Bit Control
		MIE	Interrupt (MDA, MAB, MER) Enable
Status	MOSR	MDA	Data Acknowledged Interrupt
		MAB	Data Abort Interrupt
	MSTA	MAC	Transmission Active

Table 6
Reception of MONITOR Data

Control/ Status Bit	Register	Bit	Function
Control	MOCR	MRC	MR Bit Control
		MRE	Receive Interrupt (MDR) Enable
Status	MOSR	MDR	Data Received Interrupt
		MER	End of Reception Interrupt

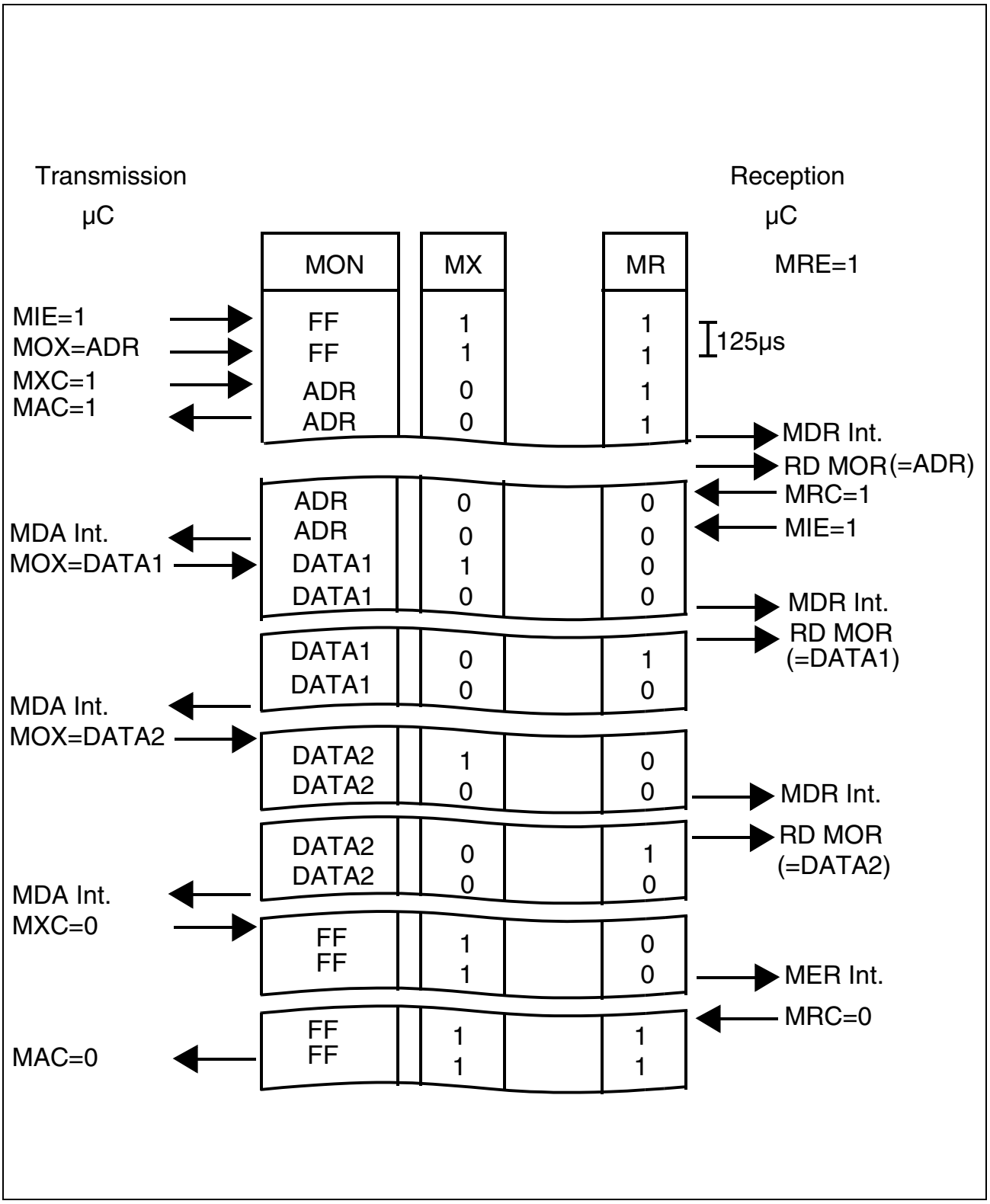


Figure 23
MONITOR Channel Protocol (IOM-2)

Before starting a transmission, the microcontroller should verify that the transmitter is inactive, i.e. that a possible previous transmission has been terminated. This is indicated by a ’0’ in the MONITOR Channel Active MAC status bit.

After having written the MONITOR Data Transmit (MOX) register, the microcontroller sets the MONITOR Transmit Control bit MXC to ’1’. This enables the MX bit to go active (0), indicating the presence of valid MONITOR data (contents of MOX) in the corresponding frame. As a result, the receiving device stores the MONITOR byte in its MONITOR Receive MOR register and generates an MDR interrupt status (MRE must be ’1’).

Alerted by the MDR interrupt, the microcontroller reads the MONITOR Receive (MOR) register. When it is ready to accept data (e.g. based on the value in MOR, which in a point-to-multipoint application might be the address of the destination device), it sets the MR control bit MRC to ’1’ to enable the receiver to store succeeding MONITOR channel bytes and acknowledge them according to the MONITOR channel protocol. In addition, it enables other MONITOR channel interrupts by setting MONITOR Interrupt Enable (MIE) to ’1’.

As a result, the first MONITOR byte is acknowledged by the receiving device setting the MR bit to ’0’. This causes a MONITOR Data Acknowledge MDA interrupt status at the transmitter.

A new MONITOR data byte can now be written by the microcontroller in MOX. The MX bit is still in the active (0) state. The transmitter indicates a new byte in the MONITOR channel by returning the MX bit active after sending it once in the inactive state. As a result, the receiver stores the MONITOR byte in MOR and generates a new MDR interrupt status. When the microcontroller has read the MOR register, the receiver acknowledges the data by returning the MR bit active after sending it once in the inactive state. This in turn causes the transmitter to generate an MDA interrupt status.

This "MDA interrupt – write data – MDR interrupt – read data – MDA interrupt" handshake is repeated as long as the transmitter has data to send.

When the last byte has been acknowledged by the receiver (MDA interrupt status), the microcontroller sets the MONITOR Transmit Control bit MXC to ’0’. This enforces an inactive (’1’) state in the MX bit. Two frames of MX inactive signifies the end of a message. Thus, a MONITOR Channel End of Reception MER interrupt status is generated by the receiver when the MX bit is received in the inactive state in two consecutive frames. As a result, the microcontroller sets the MR control bit MRC to 0, which in turn enforces an inactive state in the MR bit. This marks the end of the transmission, making the MONITOR Channel Active MAC bit return to ’0’.

During a transmission process, it is possible for the receiver to ask a transmission to be aborted by sending an inactive MR bit value in two consecutive frames. This is effected by the microcontroller writing the MR control bit MRC to ’0’. An aborted transmission is indicated by a MONITOR Channel Data Abort MAB interrupt status at the transmitter.

The MONITOR transfer protocol rules are summarized in the following section

- A pair of MX and MR in the inactive state for two or more consecutive frames indicates an **idle state** or an **end of transmission**.
- A **start of a transmission** is initiated by the transmitter by setting the MXC bit to '1' enabling the internal MX control. The receiver acknowledges the received first byte by setting the MR control bit to '1' enabling the internal MR control.
- The internal MX,MR control indicates or acknowledges a new byte in the MON slot by toggling MX,MR from the active to the inactive state for one frame.
- Two frames with the MX-bit in the inactive state indicate the **end of transmission**.
- Two frames with the MR-bit set to inactive indicate a receiver request for **abort**.
- The transmitter can **delay a transmission** sequence by sending the same byte continuously. In that case the MX-bit remains active in the IOM-2 frame following the first byte occurrence.
- Since a **double last-look criterion** is implemented the receiver is able to receive the MON slot data at least twice (in two consecutive frames). The receiver acknowledge the data after the reception of two identical bytes in two successive frames.
- To control this handshake procedure a collision detection mechanism is implemented in the transmitter. This is done by making a **collision check** per bit on the transmitted MONITOR data and the MX bit.
- Monitor data will be transmitted repeatedly until its reception is acknowledged or the transmission time-out timer expires.
- Two frames with the MX bit in the inactive state indicates the **end of a message** (EOM).
- Transmission and reception of monitor messages can be performed simultaneously. This feature is used by the SCOUT-DX to send back the response before the transmission from the controller is completed (the SCOUT-DX does not wait for EOM from the controller). MONITOR control commands nevertheless are processed sequential that means e.g. during a read on a register no further command is executed.

2.2.4.2 Error Treatment

In case the SCOUT-DX does not detect identical monitor messages in two successive frames, transmission is not aborted. Instead the SCOUT-DX will wait until two identical bytes are received in succession.

A transmission is aborted by the SCOUT-DX if

- an error in the MR handshaking occurs
- a collision on the IOM bus of the MONITOR data or MX bit occurs
- the transmission time-out timer expires

A reception is aborted by the SCOUT-DX if

- an error in the handshaking occurs or
- an abort request from the opposite device occurs

MX/MR Treatment in Error Case:

In the master mode the MX/MR bits are under control of the microcontroller through MXC or MRC respectively. An abort is indicated by an MAB interrupt or MER interrupt respectively.

In the slave mode the MX/MR bits are under control of the SCOUT-DX. An abort is always indicated by setting the MX/MR bit inactive for two or more IOM-2 frames. The controller must react with EOM.

Figure 24 shows an example for an abort requested by the receiver, **Figure 25** shows an example for an abort requested by the transmitter and **Figure 26** shows an example for a successful transmission.

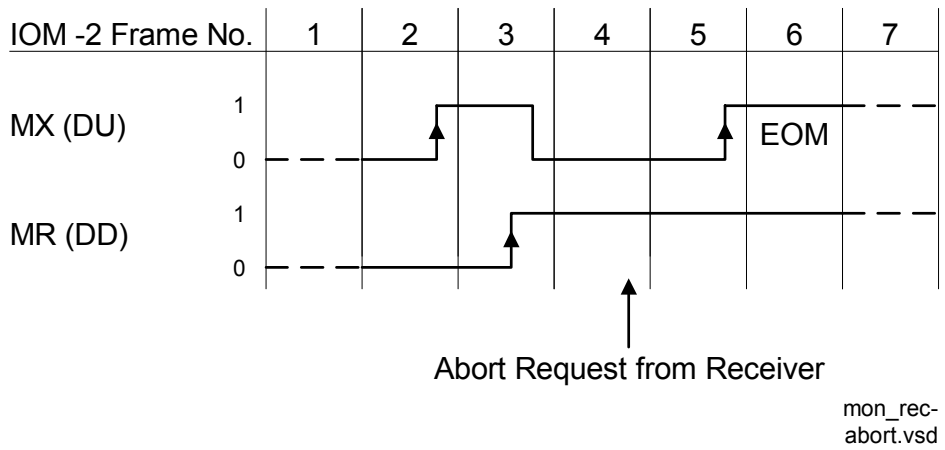


Figure 24
Monitor Channel, Transmission Abort requested by the Receiver

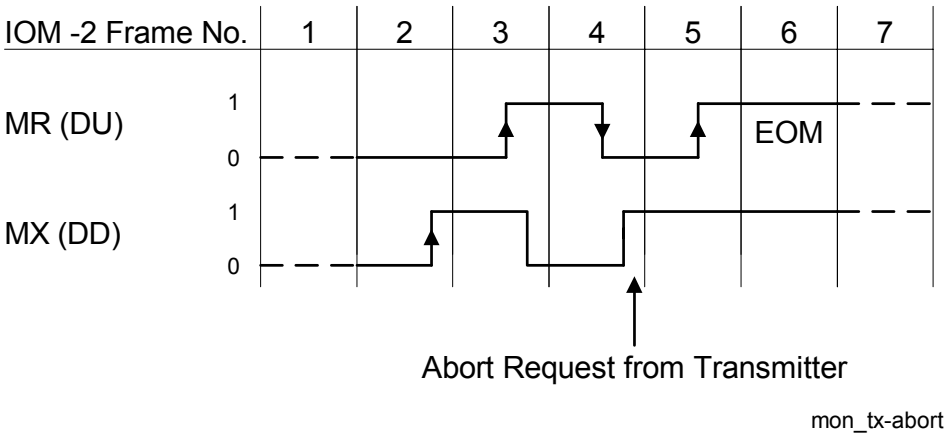


Figure 25
Monitor Channel, Transmission Abort requested by the Transmitter

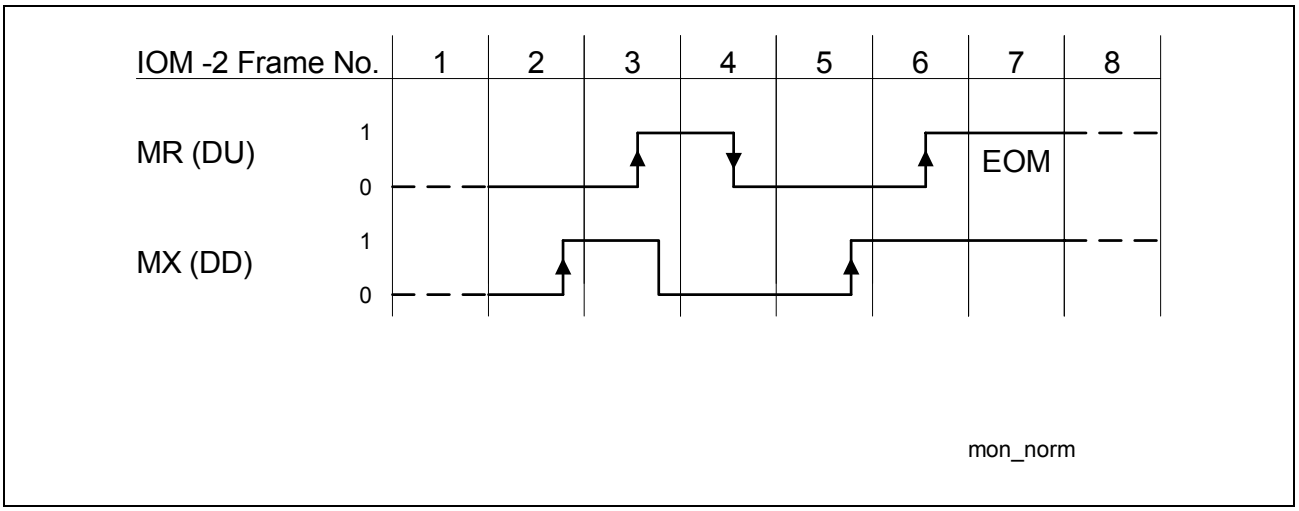


Figure 26
Monitor Channel, normal End of Transmission

2.2.4.3 MONITOR Channel Programming as a Master Device

As a master device the SCOUT-DX can program and control other devices attached to the IOM-2 interface. The master mode is selected by default if the microcontroller interface is used. The monitor data is written by the microcontroller in the MOX register and transmitted via IOM-2 DD(DU) line to the programmed/controlled device e.g. ARCOFI-BA PSB 2161. The transfer of the commands in the MON channel is regulated by the handshake protocol mechanism with MX, MR which is described in the previous chapters **2.2.4.1** and **2.2.4.2**.
If the transmitted command was a read command the slave device responds by sending the requested data.
The data structure of the transmitted monitor message depends on the device which is programmed. Therefore the first byte of the message is a specific address code which contains in the higher nibble a MONITOR channel address to identify different devices. The length of the messages depends on the accessed device and the command following the address byte.

2.2.4.4 MONITOR Channel Programming as a Slave Device

Applications in which no controller is connected to the SCOUT-DX it must operate in the MONITOR slave mode which can be selected by pinstrapping the microcontroller interface pins according to **chapter 2.1**. As a slave device the codec and the transceiver part of the SCOUT-DX is programmed and controlled by a master device at the IOM-2 interface. All programming data required by the SCOUT-DX are received in the MONITOR time slot of channel 0 on the IOM-2 and is transferred in the MOR register. The transfer of the commands in the MON channel is regulated by the handshake protocol mechanism with MX, MR which is described in the previous chapters **2.2.4.1** and **2.2.4.2**.

The first byte of the MONITOR message must contain in the higher nibble the MONITOR channel address code which is ’1010’ for the SCOUT-DX. The lower nibble distinguishes between a programming command or an identification command.

Identification Command

In order to be able to identify unambiguously different hardware designs of the SCOUT-DX by software, the following identification command is used:

DD 1st byte value	1	0	1	0	0	0	0	0
DD 2nd byte value	0	0	0	0	0	0	0	0

The SCOUT-DX responds to this DD identification sequence by sending a DU identification sequence:

DU 1st byte value	1	0	1	0	0	0	0	0	
DU 2nd byte value	1	0	DESIGN						<IDENT>

DESIGN: six bit code, specific for each device in order to identify differences in operation (**see chapter 7.2.12**).

This identification sequence is usually done once, when the terminal is connected for the first time. This function is used by the software to distinguish between different possible hardware configurations. However this sequence is not compulsory.

Programming Sequence

The programming sequence is characterized by a ’1’ being sent in the lower nibble of the received address code. The data structure after this first byte is equivalent to the structure of the serial control interface described in **chapter 2.1.1**.

DD 1st byte value	1	0	1	0	0	0	0	1
DD 2nd byte value	Header Byte							
DD 3rd byte value	R/W	Command/ Register Address						
DD 4th byte value	Data 1							
DD (nth + 3) byte value	Data n							

All registers can be read back when setting the R/W bit to ’1’ in the byte for the command/ register address. The SCOUT-DX responds by sending his IOM specific address byte ($A1_h$) followed by the requested data.

2.2.4.5 MONITOR Time-Out Procedure

To prevent lock-up situations in a MONITOR transmission a time-out procedure can be enabled by setting the time-out bit (TOUT) in the MONITOR configuration register (MCONF). An internal timer is always started when the transmitter must wait for the reply of the addressed device or for transmit data from the microcontroller. After 40 IOM frames (5ms) without reply the timer expires and the transmission will be aborted.

2.2.4.6 MONITOR Interrupt Logic

Figure 27 shows the MONITOR interrupt structure of the SCOUT-DX. The MONITOR Data Receive interrupt status **MDR** has two enable bits, MONITOR Receive interrupt Enable (**MRE**) and MR bit Control (**MRC**). The MONITOR channel End of Reception **MER**, MONITOR channel Data Acknowledged **MDA** and MONITOR channel Data Abort **MAB** interrupt status bits have a common enable bit MONITOR Interrupt Enable **MIE**.

MRE inactive (0) prevents the occurrence of **MDR** status, including when the first byte of a packet is received. When **MRE** is active (1) but **MRC** is inactive, the **MDR** interrupt status is generated only for the first byte of a receive packet. When both **MRE** and **MRC** are active, **MDR** is always generated and all received MONITOR bytes - marked by a 1-to-0 transition in MX bit - are stored. (Additionally, an active **MRC** enables the control of the MR handshake bit according to the MONITOR channel protocol.)

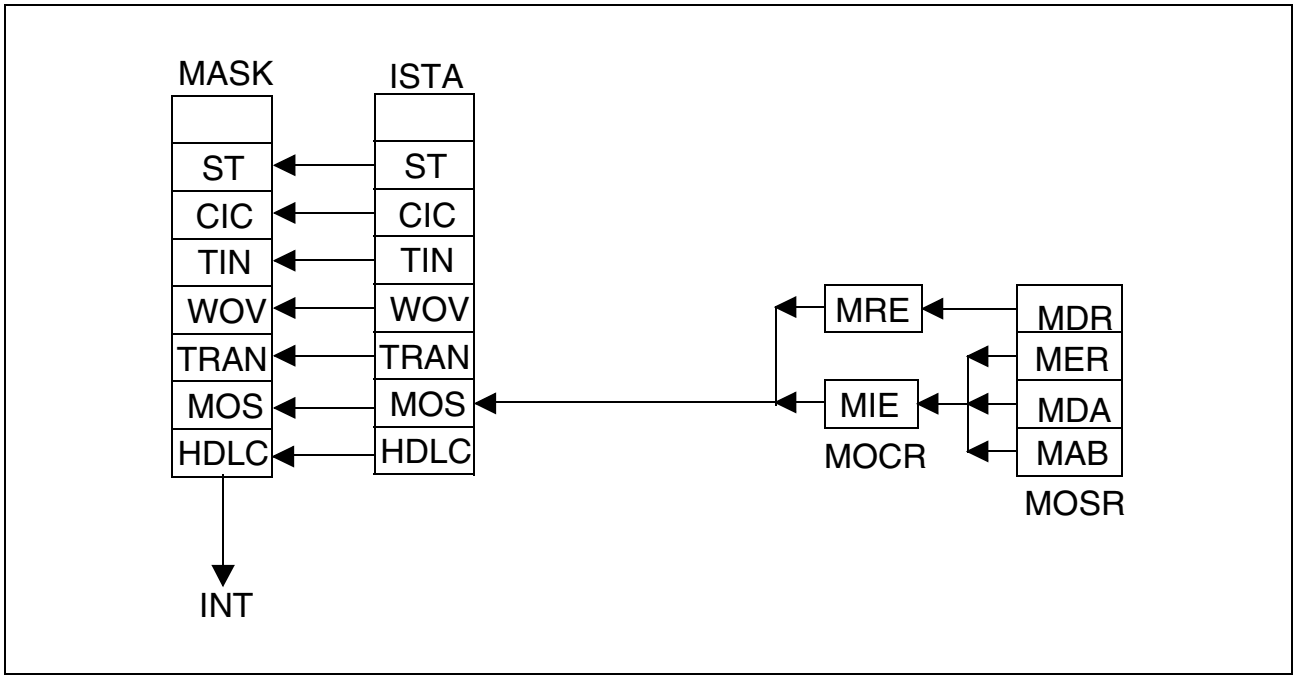


Figure 27
MONITOR Interrupt Structure

2.2.5 C/I Channel Handling

The Command/Indication channel carries real-time status information between the SCOUT-DX and another device connected to the IOM.

1) One C/I channel (called C/I0) conveys the commands and indications between the layer-1 and the layer-2 parts of the SCOUT-DX. It can be accessed by an external layer-2 device e.g. to control the layer-1 activation/deactivation procedures. C/I0 channel access may be arbitrated via the TIC bus access protocol. In this case the arbitration is done in C/I channel 2 (**see figure 11**).

The C/I0 channel is accessed via register CIR0 (in receive direction, layer-1 to layer-2) and register CIX0 (in transmit direction, layer-2 to layer-1). The C/I0 code is four bits long. A listing and explanation of the layer-1 C/I codes can be found in **chapter 2.3.4.1.3** and **2.3.4.1.6**. In the receive direction, the code from layer-1 is continuously monitored, with an interrupt being generated anytime a change occurs (ISTA.CIC). A new code must be found in two consecutive IOM frames to be considered valid and to trigger a C/I code change interrupt status (double last look criterion).

In the transmit direction, the code written in CIX0 is continuously transmitted in C/I0.

2) A second C/I channel (called C/I1) can be used to convey real time status information between the SCOUT-DX and various non-layer-1 peripheral devices e.g. PSB 2161 ARCOFI-BA. The C/I1 channel consists of four or six bits in each direction.The width can be changed from 4bit to 6bit by setting bit CIX1.CICW.

The C/I1 channel is accessed via registers CIR1 and CIX1. A change in the received C/I1 code is indicated by an interrupt status without double last look criterion.

2.2.5.1 CIC Interrupt Logic

Figure 28 shows the CIC interrupt structure.

A CIC interrupt may originate

– from a change in received C/I channel 0 code (CIC0)

  or

– from a change in received C/I channel 1 code (CIC1).

The two corresponding status bits CIC0 and CIC1 are read in CIR0 register. CIC1 can be individually disabled by clearing the enable bit CI1E in the CIX1 register. In this case the occurrence of a code change in CIR1 will not be displayed by CIC1 until the corresponding enable bit has been set to one.
Bits CIC0 and CIC1 are cleared by a read of CIR0.
An interrupt status is issued every time a valid new code is loaded into CIR0 or CIR1.

The CIR0 is buffered with a FIFO size of two. If a second code change occurs in the received C/I channel 0 before the first one has been read, immediately after reading of CIR0 a new interrupt will be generated and the new code will be stored in CIR0. If several

consecutive codes are detected, only the first and the last code is obtained at the first and second register read, respectively.

For CIR1 no FIFO is available. The actual code of the received C/I channel 1 is always stored in CIR1.

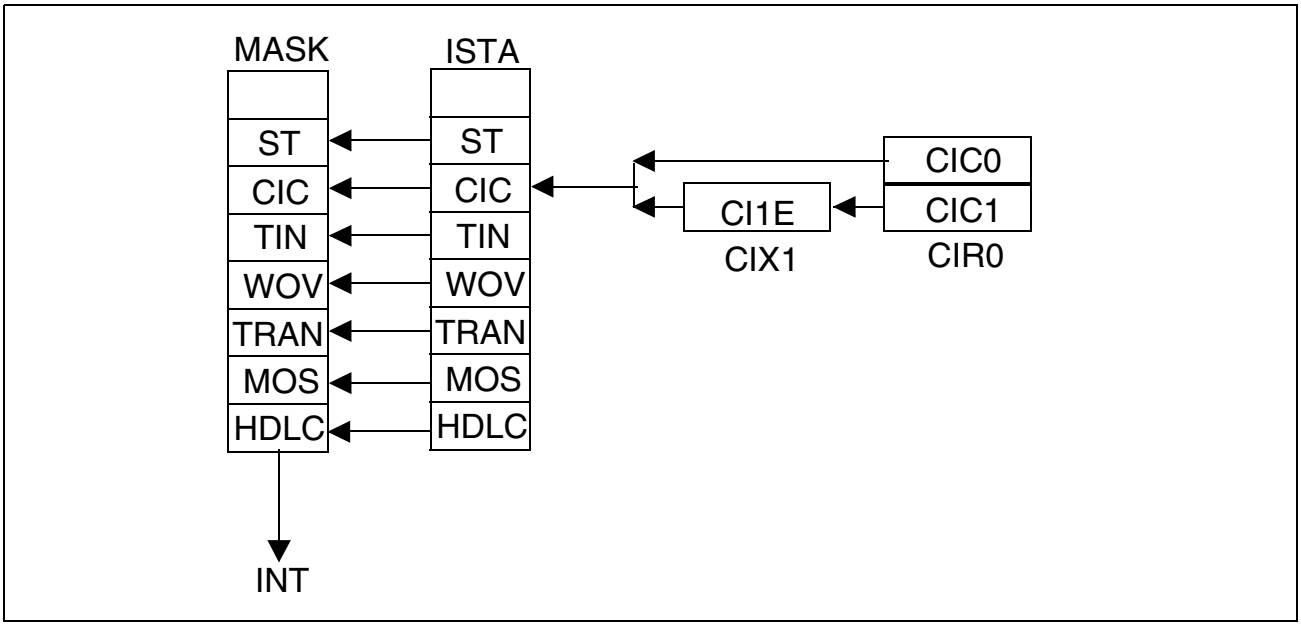


Figure 28
CIC Interrupt Structure

2.2.6 Settings after Reset (see also chapter 7.3)

After reset the codec, the TIC-bus access, the serial data strobes (pin SDS1 and SDS2) and the controller data access are disabled.
The IOM handler is enabled except the generation of the bit clock (pin BCL).
The monitor handler is enabled for channel MON0 and the transceiver for the channels B1, B2, C/I0 and D.
The HDLC controller is connected to the D channels.
The pins DD and DU are in open drain state.
The synchronous transfer interrupts and synchronous transfer overflow interrupts are masked.

2.2.7 D-Channel Access Control

D-channel access control was defined to guarantee all connected HDLC controllers a fair chance to transmit data in the D-channel. Collisions are possible on the IOM-2 interface, if there is more than one HDLC controller connected. This arbitration mechanism is implemented in the SCOUT-DX and will be described in the following chapter.

2.2.7.1 TIC Bus D-Channel Access Control

The TIC bus is implemented to organize the access to the layer-1 functions provided in the SCOUT-DX (C/I-channel) and to the D-channel from up to 7 external communication controllers (see **figure 29**).
To this effect the outputs of the controllers (ICC:ISDN Communication Controller PEB 2070) are wired-or and connected to pin DU. The inputs of the ICCs are connected to pin DD. External pull-up resistors on DU/DD are required. The arbitration mechanism must be activated by setting MODEH.DIM2-0=00x.

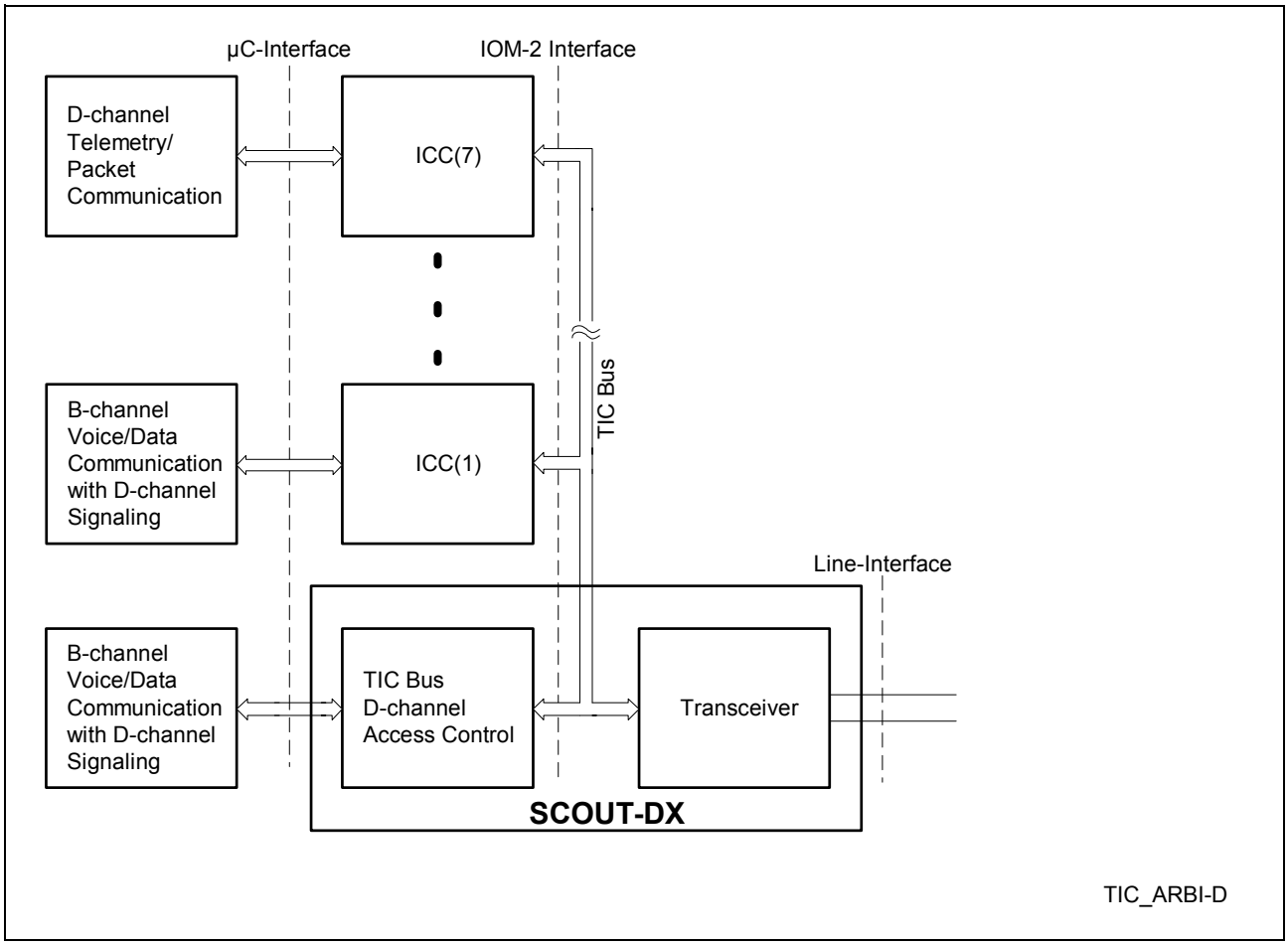


Figure 29
Applications of TIC Bus in IOM-2 Bus Configuration

The arbitration mechanism is implemented in the last octet in IOM channel 2 of the IOM-2 interface (see **figure 30**). An access request to the TIC bus may either be generated by software (µP access to the C/I channel) or by the SCOUT-DX itself (transmission of an HDLC frame in the D-channel). A software access request to the bus is effected by setting the BAC bit (CIX0 register) to ’1’.

In the case of an access request, the SCOUT-DX checks the Bus Accessed-bit BAC (bit 5 of DU last octet of channel 2, see **figure 30**) for the status "bus free“, which is indicated by a logical ’1’. If the bus is free, the SCOUT-DX transmits its individual TIC bus address TAD programmed in the CIX0 register and compares it bit by bit with the value on DU. If a sent bit set to ’1’ is read back as ’0’ because of the access of another D-channel source with a lower TAD, the SCOUT-DX withdraws immediately from the TIC bus. The TIC bus is occupied by the device which sends its address error-free. If more than one device attempt to seize the bus simultaneously, the one with the lowest address wins and starts D-channel transmission.

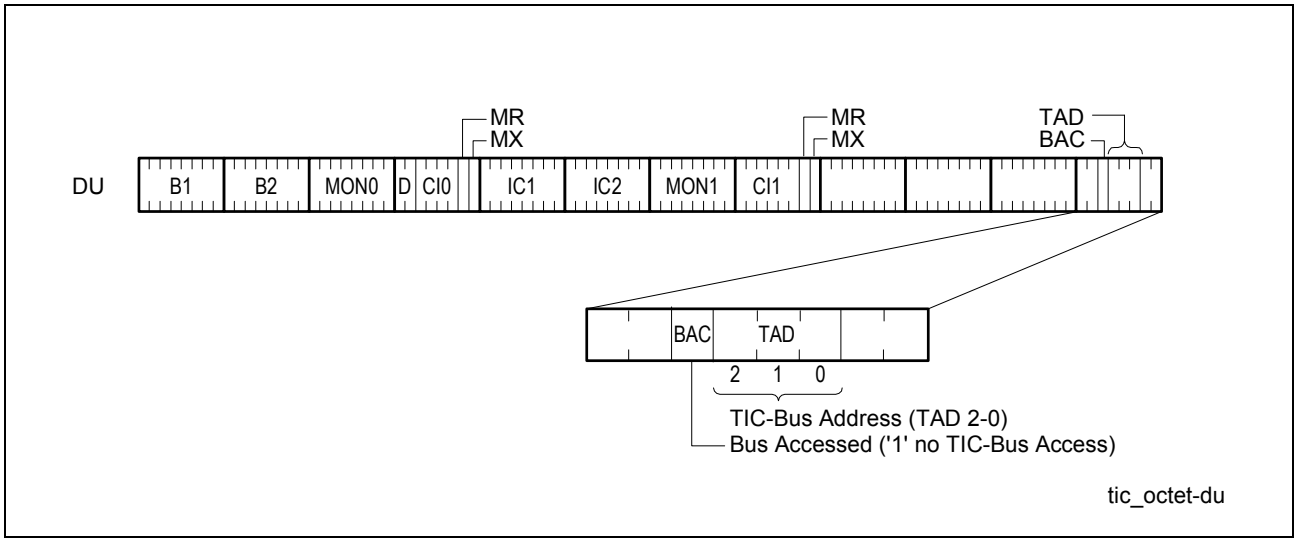


Figure 30
Structure of Last Octet of Ch2 on DU

When the TIC bus is seized by the SCOUT-DX, the bus is identified to other devices as occupied via the DU channel 2 Bus Accessed-bit state ’0’ until the access request is withdrawn. After a successful bus access, the SCOUT-DX is automatically set into a lower priority class, that is, a new bus access cannot be performed until the status "bus free" is indicated in two successive frames.

If none of the devices connected to the IOM interface requests access to the D and C/I channels, the TIC bus address 7 will be present. The device with this address will therefore have access, by default, to the D and C/I channels.

Note: Bit BAC (CIX0 register) should be reset by the µP when access to the C/I channels is no more requested, to grant other devices access to the D and C/I channels.

2.2.8 Activation/Deactivation of IOM-2 Interface

The IOM-2 interface can be switched off in the inactive state, reducing power consumption to a minimum. In this deactivated state is FSC = ’1’, DCL = ’0’ and BCL = ’1’ and the data lines are ’1’. The data between the functional blocks of the SCOUT-DX is then transferred internally.

The IOM-2 interface can be kept active while the line interface is deactivated by setting the CFS bit to "0" (MODE register). This is the case after a hardware reset. If the IOM-2 interface should be switched off while the line interface is deactivated, the CFS bit should be set to ’1’. In this case the internal oscillator is disabled when no signal (info 0) is present on the line interface and the C/I command is ’1111’ = DIU (refer to **chapter 2.3.4.1.3** and **2.3.4.1.6**). If the TE wants to activate the line, it has first to activate the IOM-2 interface either by using the "Software Power Up" function (IOM_CR.SPU bit) or by setting the CFS bit to "0" again.

The deactivation procedure is shown in **figure 31**. After detecting the code DIU (Deactivate Indication Upstream) the layer 1 of the SCOUT-DX responds by transmitting DID (Deactivate Indication Downstream) during subsequent frames and stops the timing signals synchronously with the end of the last C/I (C/I0) channel bit of the fourth frame.

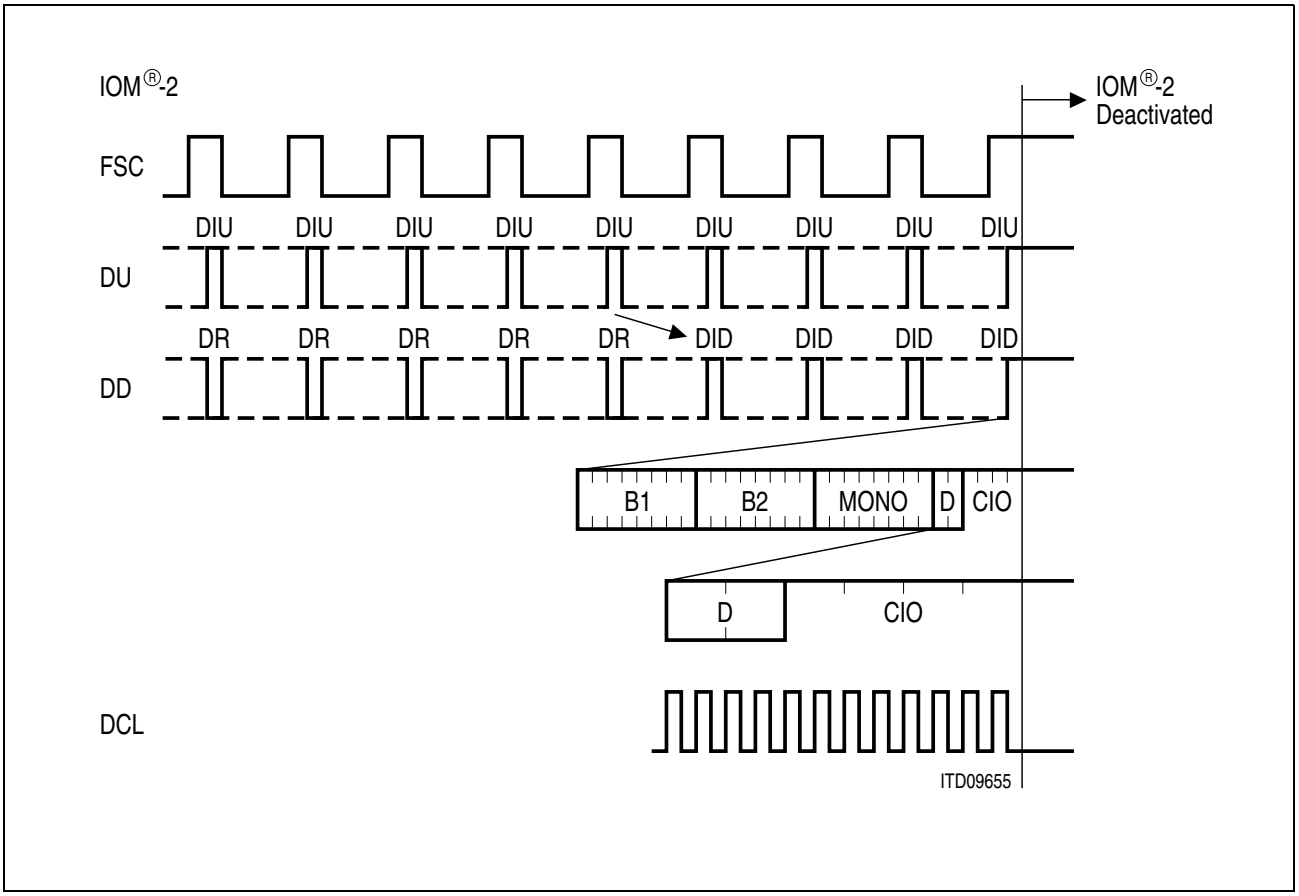


Figure 31
Deactivation of the IOM®-Interface

The clock pulses will be enabled again when the DU line is pulled low (bit SPU in the IOM_CR register) i.e. the C/I command TIM = "0000" is received by layer 1, or when a non-zero level on the line interface is detected. The clocks are turned on after approximately 0.2 to 4 ms depending on the capacitances on XTAL 1/2.

DCL is activated such that its first rising edge occurs with the beginning of the bit following the C/I (C/I0) channel.

After the clocks have been enabled this is indicated by the PU code in the C/I channel and by a CIC interrupt. The DU line may be released by resetting the Software Power Up bit IOM_CR =’0’ and the C/I code written to CIX0 before (e.g. TIM or AR8) is output on DU.

The SCOUT-DX supplies IOM timing signals as long as there is no DIU command in the C/I (C/I0) channel. If timing signals are no longer required and activation is not yet requested, this is indicated by programming DIU in the CIX0 register.

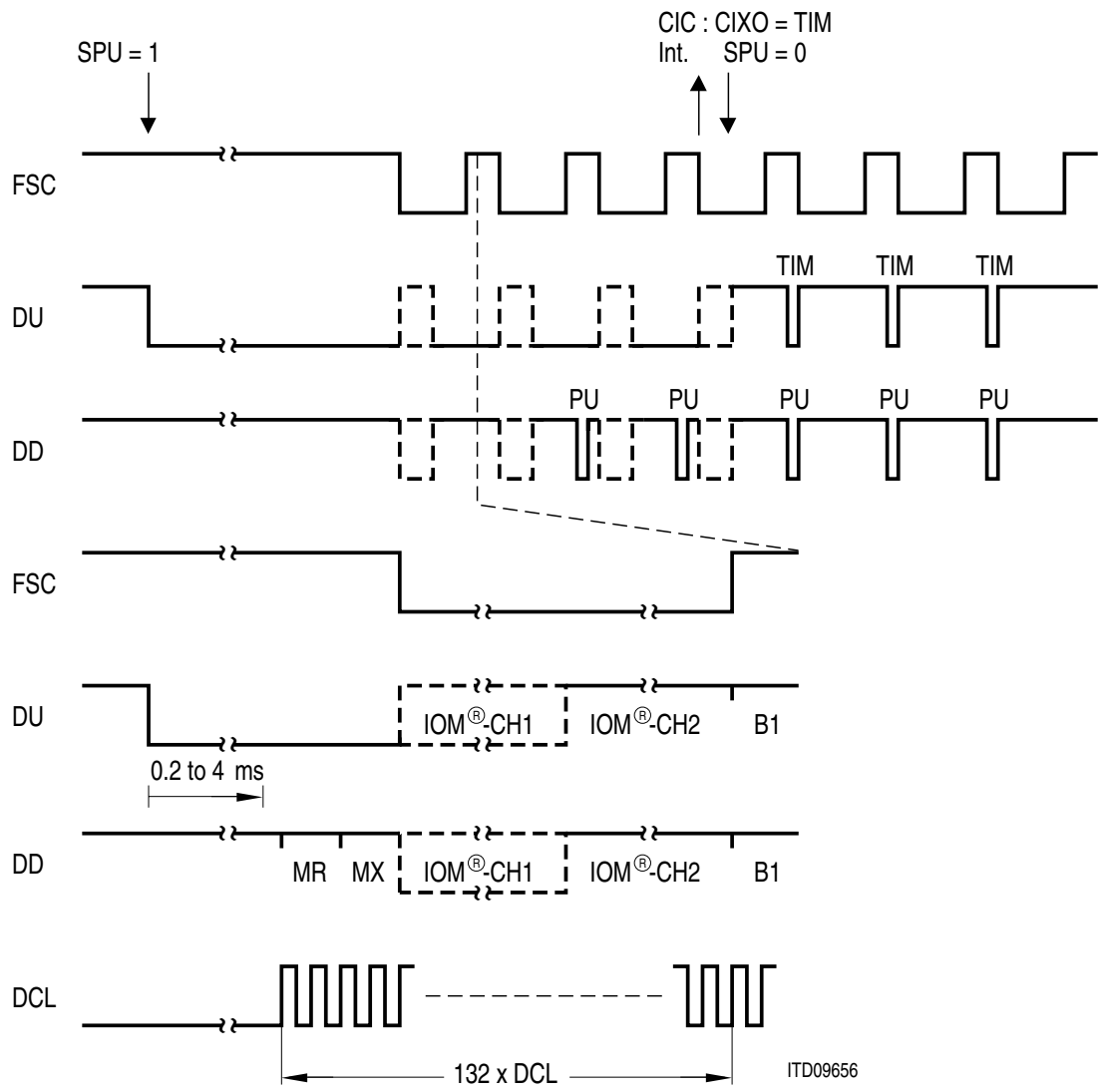


Figure 32
Activation of the IOM-Interface

2.3 Line Interface

The layer-1 functions for the line interface of the SCOUT-DX are:

- conversion of the frame structure between IOM and line interface
- conversion from/to binary to/from AMI coding
- level detection
- receive timing recovery
- IOM-2 timing synchronous to the line interface
- activation/deactivation procedures, triggered by primitives received over the IOM C/I channel or by INFO's received from the line
- execution of test loops

2.3.1 Burst Frame

Figure 33 demonstrates the general principles of the line interface communication scheme. A frame transmitted by the exchange (LT) is received by the terminal equipment (TE) after a line propagation delay. The terminal equipment waits the minimum guard time (t_g = 15.625 µs) while the line clears. It then transmits a frame to the exchange. The exchange will begin a transmission every 250 µs (known as the burst repetition period). Within a burst, the data rate is 384 kbit/s.

One frame contains the framing bit (F) and the user channels (2B + D). It can readily be seen that in the 250-µs burst repetition period, 4 D-bits, 16 B1-bits and 16 B2-bits are transferred in each direction. This gives an effective full duplex data rate of 16 kbit/s for the D-channel and 64 kbit/s for each B-channel.

The B- and D- channels are scrambled according to the following feed back polynom:

$$X^9 + X^5 + 1$$

AMI-coding is used for the line interface. A logical ‘0’ corresponds to a neutral level, a logical ‘1’ is coded as alternate positive and negative pulses.

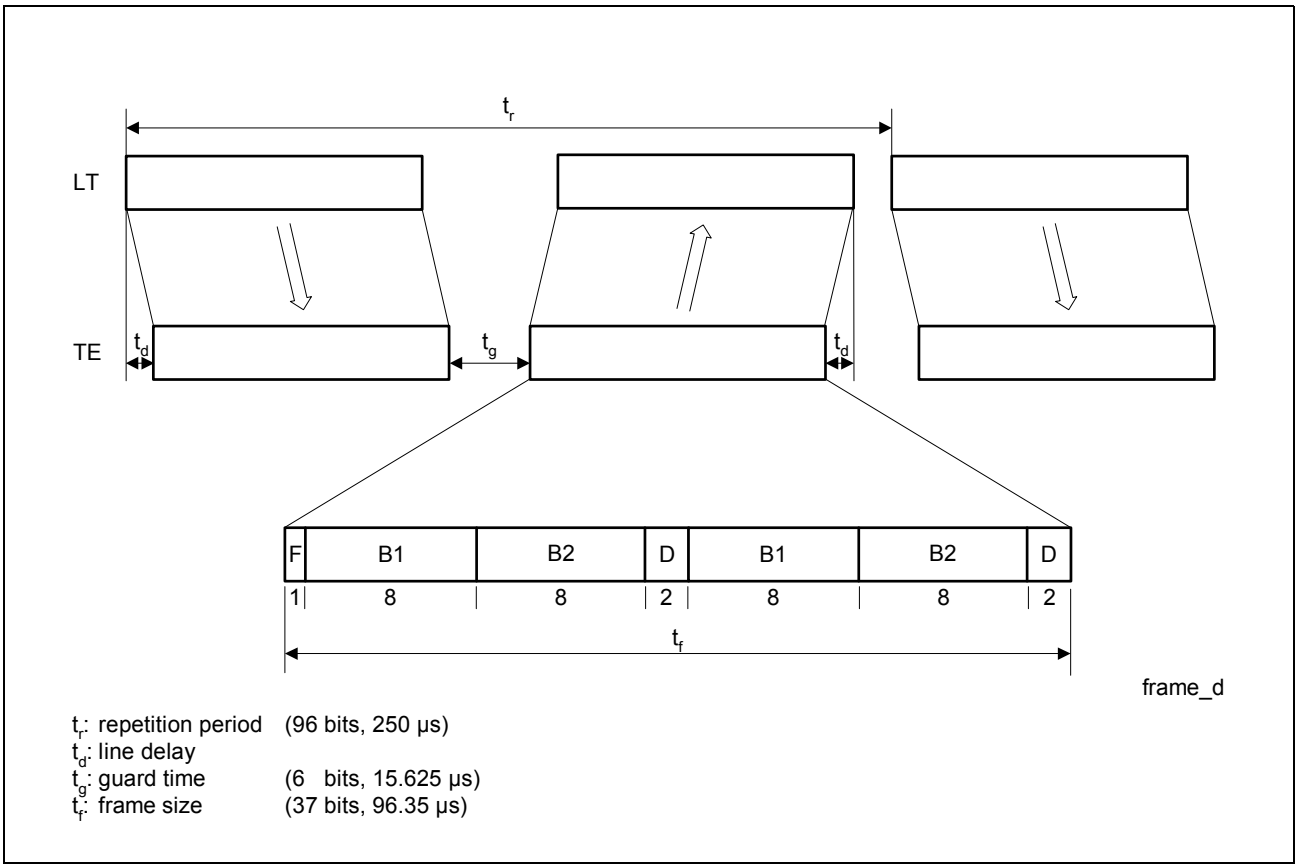


Figure 33
Line Interface Structure

2.3.2 Transceiver Timing

The receive PLL uses the 15.36-MHz clock to generate an internal 384-kHz signal which is used to synchronize the PLL to the frame received from the line interface. The PLL outputs the FSC-signal as well as the 1.536-MHz double bit clock signal and the 768-kHz bit clock.

2.3.3 Data Transfer and Delay between IOM and Line Interface

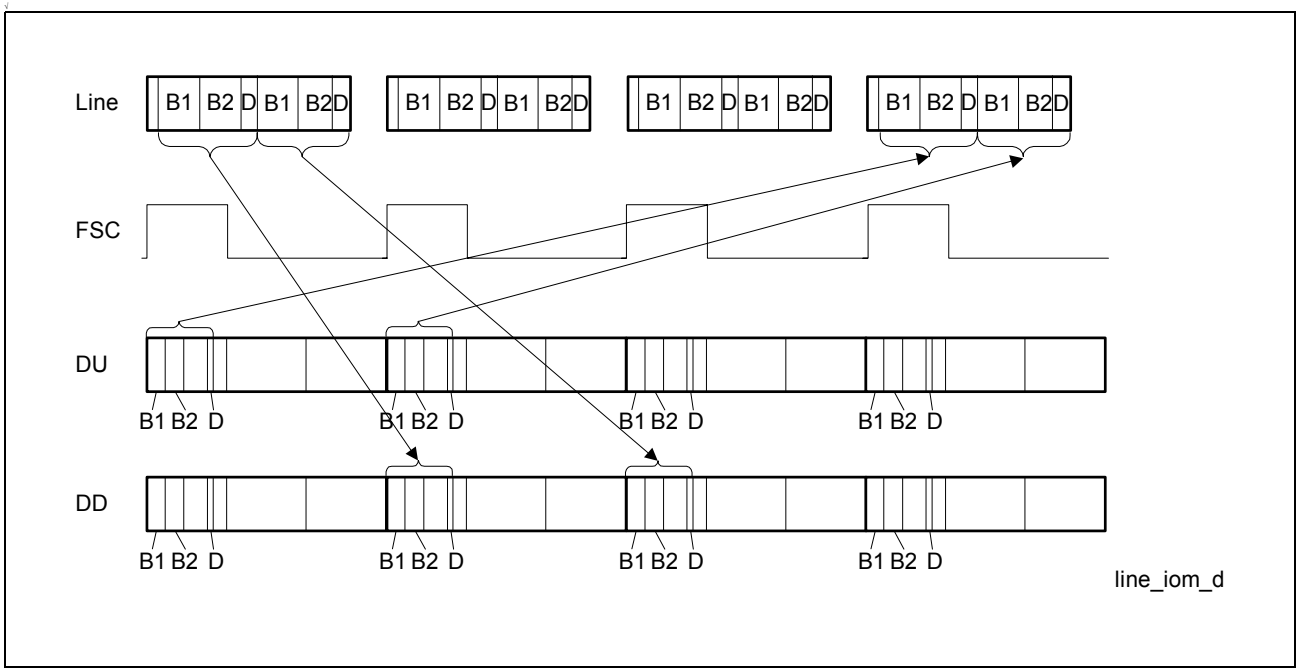


Figure 34
Data Delay between IOM and Line Interface

The IOM-interface B-channels are used to convey the two 64-kbit/s user channels in both directions.

Only in the activated states the data is transferred transparently. In all other states logical ’1’s are transmitted to the IOM interface.

2.3.4 Control of the Line Interface

The layer-1 activation/deactivation can be controlled by an internal state machine via the IOM-2 C/I0 channel or by software via the microcontroller interface directly. In the default state the internal layer-1 state machine of the SCOUT-DX is used.

To disable the internal state machine TR_CONF0.L1SW must be set to '1' and a C/I code TIM ('0000') has to be programmed into CIX0.CODX0

If the internal state machine is disabled the layer-1 commands, which are normally generated by the internal state machine can be written directly into the TR_CMD register and the indications can be read out of the TR_STA register respectively. The SCOUT-DX layer-1 control flow is shown in **figure 35**.

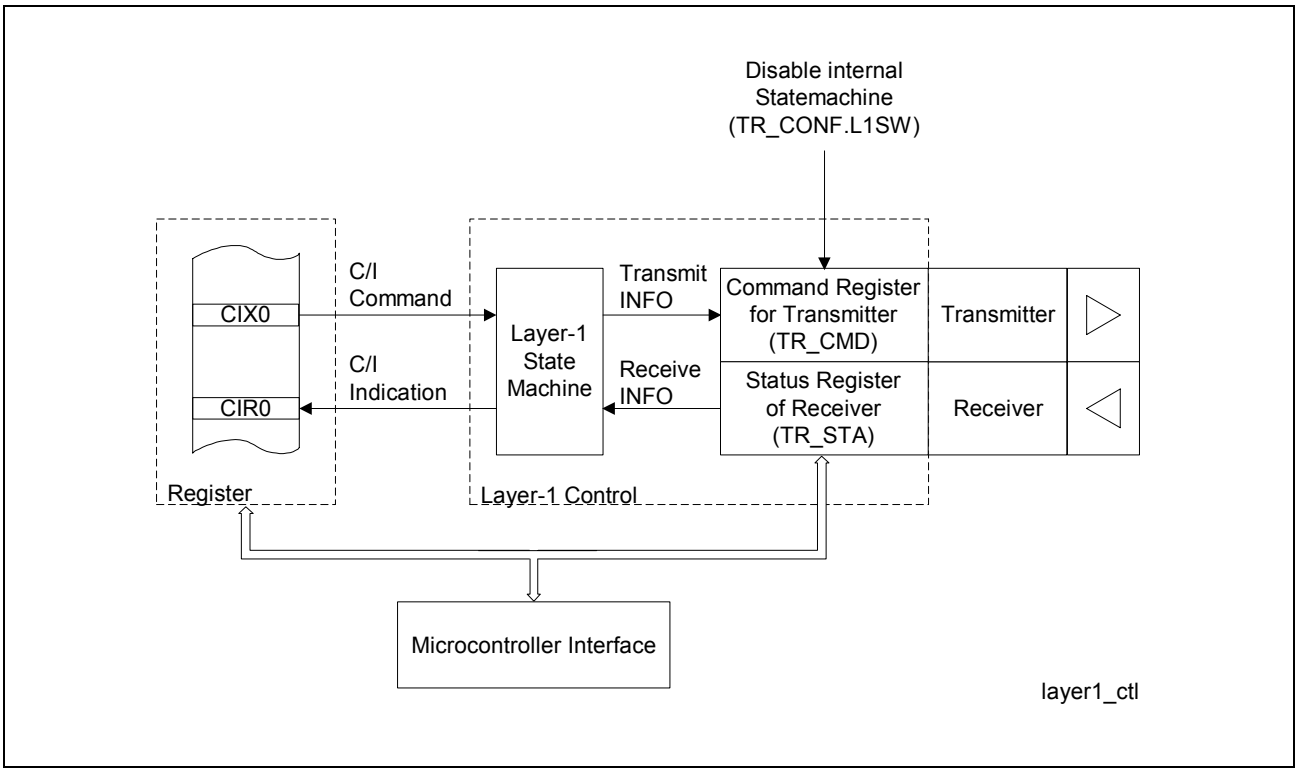


Figure 35
Layer-1 Control

2.3.4.1 Internal Layer-1 State machine

In the following sections the layer-1 control by the SCOUT-DX state machine will be described. For the description of the IOM-2 C/I0 channel see also **chapter 2.2.5**.

The layer-1 functions are controlled by commands issued via the CIX0 register. These commands, sent over the IOM C/I channel 0 to layer 1, trigger certain procedures, such as activation/deactivation, switching of test loops and transmission of special pulse patterns. Responses from layer 1 are obtained by reading the CIR0 register after a CIC interrupt (ISTA).

2.3.4.1.1 State Transition Diagram

The state machine includes all information relevant to the user. The state diagram notation is given in **figure 36**.

The informations contained in the state diagrams are:
- State name
- Signal received from the line interface (INFO) (see **chapter 2.3.4.1.4**)
- Signal transmitted to the line interface (INFO) (see **chapter 2.3.4.1.7**)
- C/I code received (commands) (see **chapter 2.3.4.1.3**)
- C/I code transmitted (indications) (see **chapter 2.3.4.1.6**)
- Transition criteria

The transition criteria is grouped into:
- C/I commands (see **chapter 2.3.4.1.3**)
- Signals received from the line interface (INFOs) (see **chapter 2.3.4.1.4**)
- Reset (see **chapter 2.3.4.1.5**)

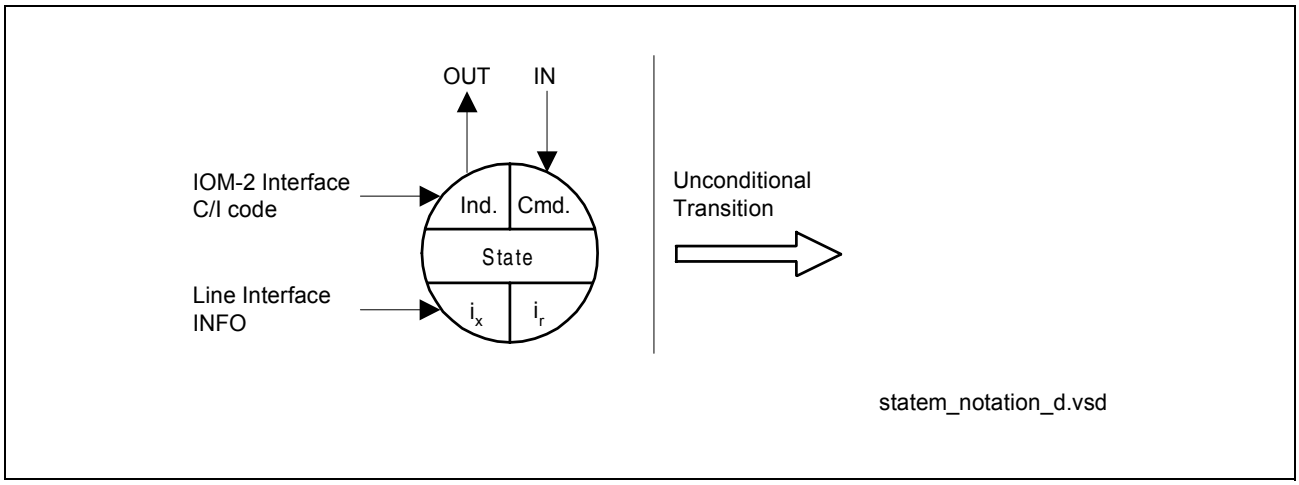
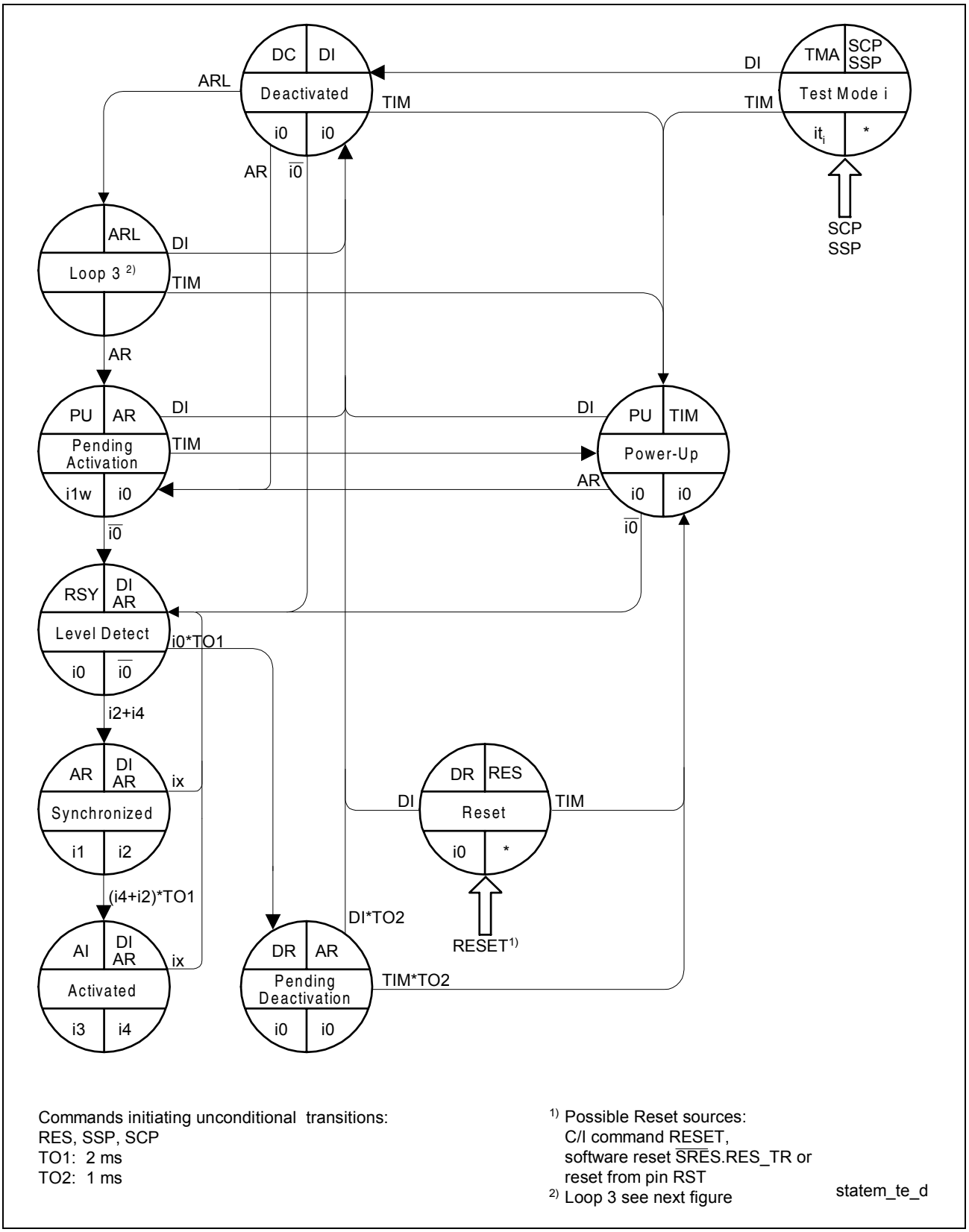


Figure 36
State Diagram Notation

As can be seen from the transition criteria, combinations of multiple conditions are possible as well. A "*" stands for a logical AND combination. And a "+" indicates a logical OR combination.

The sections following the state diagram contain detailed information about all states and signals used.

Figure 37 shows the state transition diagram of the SCOUT-DX state machine. **Figure 38** shows this for the state Loop 3.



Commands initiating unconditional transitions:
RES, SSP, SCP
TO1: 2 ms
TO2: 1 ms

1) Possible Reset sources:
C/I command RESET,
software reset $\overline{\text{SRES}}$.RES_TR or
reset from pin RST
2) Loop 3 see next figure

statem_te_d

Figure 37
State Transition Diagram

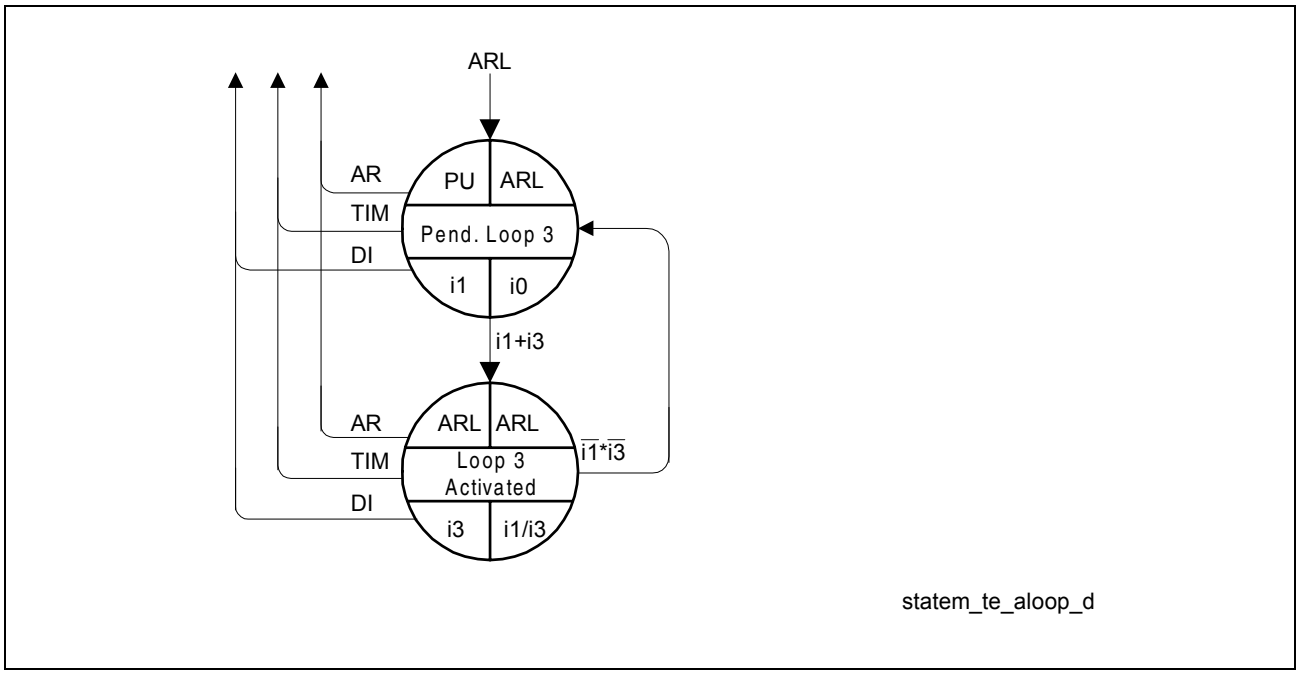


Figure 38
State Transition Diagram of the Loop 3 State

2.3.4.1.2 States

Reset, Pending Deactivation

State after reset or deactivation from the line interface by info 0. Note that no activation from the terminal side is possible starting from this state. A ‘DI’-command has to be issued to enter the state ’Deactivated’.

Deactivated

The line interface is deactivated and the IOM-2 interface is or will be deactivated. Activation is possible from the line interface and from the IOM-2 interface.

Power-Up

The line interface is deactivated and the IOM-2 interface is activated, i.e. the clocks are running.

Pending Activation

Upon the command Activation Request (AR) the SCOUT-DX transmits the 2-kHz info 1w towards the network, waiting for info 2.

Level Detect

During the first period of receiving info 2 or under severe disturbances on the line, the receiver recognizes the receipt of a signal but is not (yet) synchronized.

Synchronized

The receiver is synchronized and detects info 2. It continues the activation procedure by transmission of info 1.

Activated

The receiver is synchronized and detects info 4. It concludes the activation procedure by transmission of info 3. All user channels are now conveyed transparently.

Analog Loop 3 Pending

Upon the C/I-command Activation Request Loop (ARL) the SCOUT-DX loops back the transmitter to the receiver and activates by transmission of info 1. The receiver is not yet synchronized.

Analog Loop 3 Synchronized

After synchronization the transmitter continues by transmitting info 3.

Analog Loop 3 Activated

After recognition of the looped back info 3 the channels are looped back transparently.

Test Mode i

After entering test mode initiated by SCP-, SSP-commands.

Level Detect, Resynchronization

During the first period of receiving info 2 or under severe disturbances on the line the receiver recognizes the receipt of a signal but is not (yet) synchronized. In extremely rare situations of severe line disturbances, the receiver might become locked in this state. To avoid this, it is recommended that the software issues an RES command to restart activation if SCOUT-DX remains in this state longer than an acceptable period. This time out period should be at least 110 ms, but the exact period should be chosen by the user based on system concerns.

Reset state

A software reset (RES) forces the SCOUT-DX to an idle state where INFO 0 is transmitted. Thus activation from the LT is not possible. Clocks are still supplied.

2.3.4.1.3 C/I Commands

Command (Upstream)	Abbr.	Code	Remarks
Timing	TIM	0000	Layer-2 device requires clocks to be activated
Reset	RES	0001	State machine reset
Send Single Pulses	SSP	0010	AMI coded pulses transmitted at 4 kHz
Send Continuous Pulses	SCP	0011	AMI coded pulses transmitted continuously
Activate Request	AR	1000	
Activate Request Loop 3	ARL	1001	Local analog loop
Deactivation Indication	DI	1111	

2.3.4.1.4 Receive Infos on the Line (Downstream)

Name	Abbr.	Description
Info 0	i0	No signal on the line
Info 2	i2	4-kHz burst signal F='1' B1-, B2- and D- channels are scrambled '1's.
Info 4	i4	4-kHz burst signal F='1' B1-, B2- and D- channels are scrambled data.
Info X	ix	Any signal except info 2 or info 4

2.3.4.1.5 Reset

RES A low signal on the $\overline{RST}$ pin or setting the RES_TR bit in the SRES register to '1' resets also the layer-1 state machine. The reset signals should be applied for a minimum of 2 DCL clock cycles. The function of these reset events is identical to the C/I code RES concerning the state machine.

2.3.4.1.6 C/I Indications

Indication (Downstream)	Abbr.	Code	Remarks
Deactivation Request	DR	0000	
Power-Up	PU	0111	
Test Mode Acknowledge	TMA	0010	Acknowledge for both SSP and SCP
Resynchronization	RSY	0100	Receiver not synchronous
Activation Request	AR	1000	Receiver synchronized
Activation Request Loop 3	ARL	1001	Local loop synchronized
Activation Indication	AI	1100	
Activation Indication Loop 3	AIL	1101	Local loop activated
Deactivation Confirmation	DC	1111	Line- and if MODE1.CFS = ’1’ also IOM-interface are powered down

2.3.4.1.7 Transmit Infos on the Line (Upstream)

Name	Abbr.	Description
Info 0	i0	No signal on the line
Info 1w	i1w	Asynchronous wake signal 2-kHz burst rate F='1' B1-, B2- and D- channels are scrambled '1's.
Info 1	i1	4-kHz burst signal F='1' B1-, B2- and D- channels are scrambled '1's.
Info 3	i3	4-kHz burst signal F='1' B1-, B2- and D- channels are scrambled data.
Test Info 1	it_1	AMI-coded pulses are transmitted continuously
Test Info 2	it_2	One AMI-coded pulse is transmitted in each frame

2.3.4.1.8 Example of Activation/Deactivation

An example of an activation/deactivation of the line interface initiated by the terminal with the time relationships mentioned in the previous chapters is shown in **figure 39**.

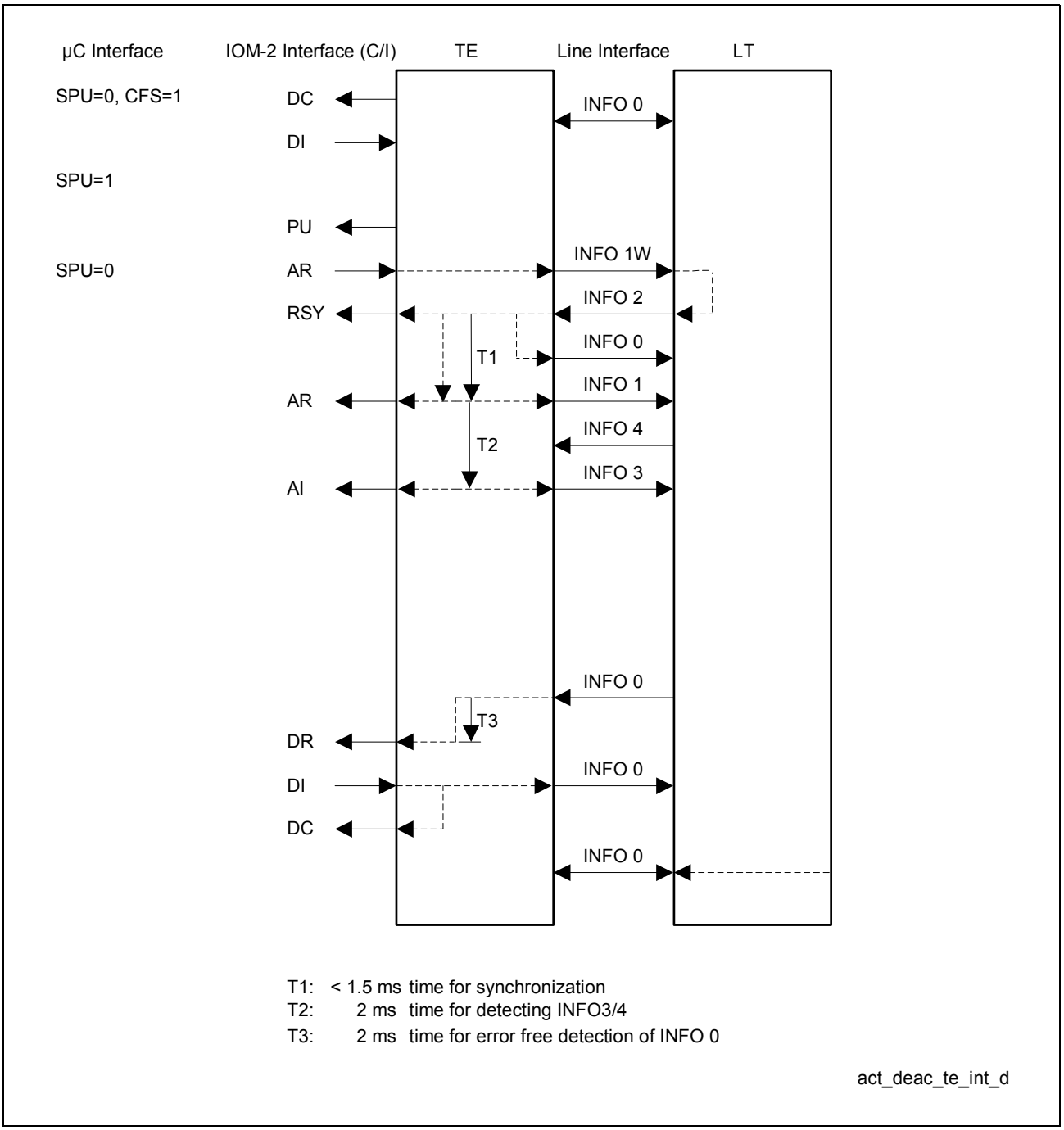


Figure 39
Example of Activation/Deactivation Initiated by the Terminal (TE). Activation/Deactivation under control of the internal layer-1 state machine

2.3.4.2 External Layer-1 State machine

Instead of using the integrated layer-1 state machine it is also possible to implement the layer-1 state machine completely in software.

The internal layer-1 state machine can be disabled by setting the L1SW bit in the TR_CONF0 register (see **chapter 7.2.6**) to ’1’.

The transmitter is completely under control of the microcontroller via register TR_CMD (see **chapter 7.2.5**).

The status of the receiver is stored in register TR_STA (see **chapter 7.2.4**) and has to be evaluated by the microcontroller. This register is updated continuously. If not masked a RIC interrupt (see **chapter 7.2.6**) is generated by any change of the register contents. The interrupt is cleared after a read access to this register.

2.3.4.2.1 Activation initiated by the Terminal (TE, SCOUT-DX)

INFO 1W has to be transmitted as long as INFO 0 is received.
INFO 0 has to be transmitted thereafter as long as no valid INFO (INFO 2 or INFO 4) is received.
After reception of INFO 2 transmission of INFO 1 has to be started. After additional 8 frames (2 ms, synchronization time for the LT) transmission of INFO 3 has to be started.

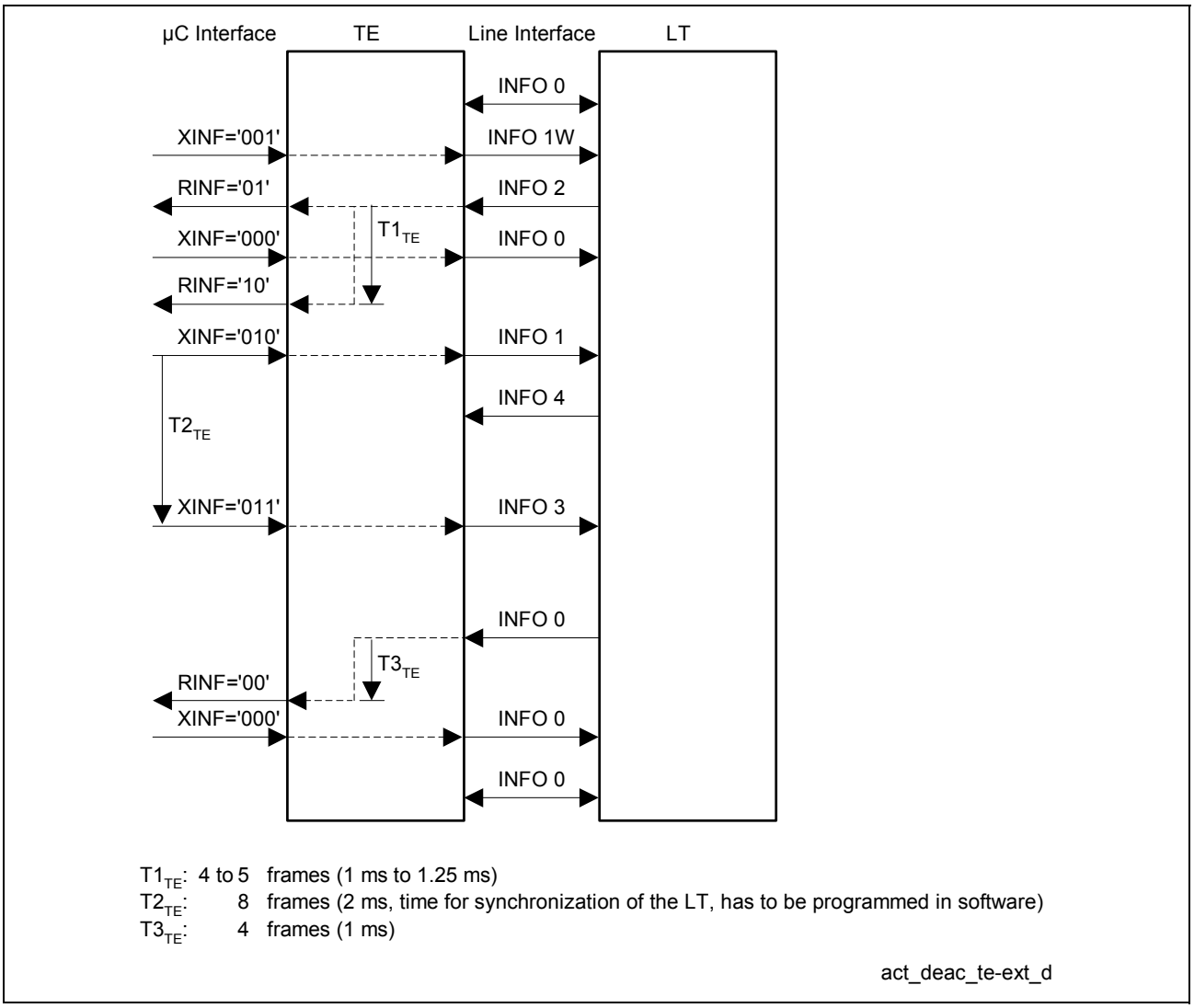


Figure 40
Example of Activation/Deactivation initiated by the Terminal (TE). Activation/Deactivation completely under software control

2.3.4.2.2 Activation initiated by the Line Termination LT

INFO 0 has to be transmitted as long as no valid INFO (INFO 2 or INFO 4) is received. After reception of INFO 2 transmission of INFO 1 has to be started. After additional 8 frames (2 ms, synchronization time for the LT) transmission of INFO 3 has to be started.

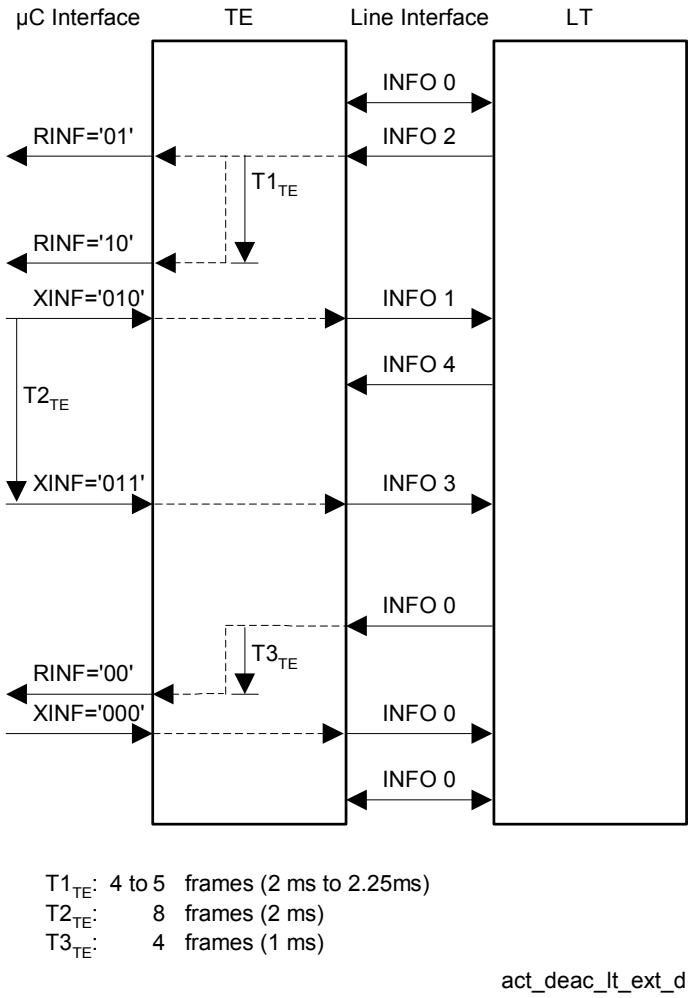


Figure 41
Example of Activation/Deactivation initiated by the Line termination (LT). Activation/Deactivation completely under software control

2.3.5 Level Detection Power Down

If MODE1.CFS is set to ’0’, the clocks are also provided in power down state, whereas if CFS is set to ’1’ only the analog level detector is active in power down state. All clocks, including the IOM interface, are stopped. The data lines and the FSC are ’high’, whereas DCL is ’low’ and BCL is ’high’.

An activation initiated from the exchange side (any signal detected on the line interface) will have the consequence that clock signals are provided automatically if the bit LDD of register TR_CONF0 is set to ’0’.

From the terminal side an activation must be started by setting and resetting the SPU-bit in the IOM_CR register and writing TIM to the CIX0 register or by resetting MODE1.CFS=0.

2.3.6 Transceiver Enable/Disable

The layer-1 part of the SCOUT-DX can be enabled/disabled by configuration with the two bits TR_CONF0.DIS_TR and TR_CONF2.DIS_TX .
By default all layer-1 functions are enabled (DIS_TR = ’0’, DIS_TX = ’0’). If DIS_TX = ’1’ only the transmit buffers are disabled. The receiver will monitor for incoming calls in this configuration.
If DIS_TR = ’1’ all layer-1 functions are disabled including the level detection circuit of the receiver. In this case the power consumption of the layer-1 is reduced to a minimum. The HDLC controller and codec part can still operate via IOM-2. The DCL and FSC pins become inputs.

2.3.7 Test Functions

The SCOUT-DX provides several test and diagnostic functions for the transceiver:

2.3.7.1 Line Transceiver Test

Two test loops allow the local or the remote test of the transceiver function.

– The local loop (test loop 3) which is activated by a C/I0 ARL command loops the transmit data of the transmitter to its receiver. The information of the IOM-2 upstream B- and D-channels is looped back to the downstream B- and D-channels.
– The remote loop (test loop 2) is activated by TR_CONF.RLP (see **chapter 7.2.3**). The data received from the line interface is looped back to the line interface. The D-channel information received from the line card is transparently forwarded to the downstream IOM-2 D-channel.
  The downstream B-channel information on IOM-2 is fixed to ‘FF’$_H$ while test loop 2 is active.

2.3.7.2 Test Signals on the Line Interface

Two kinds of test signals may be sent by the SCOUT-DX:

– The single pulses are of alternating polarity at 2 kHz (one pulse per frame). The corresponding C/I command is SSP (Send single pulses).
– The continuous pulses are pulses of alternating polarity. The corresponding C/I command is SCP (Send continuous pulses).

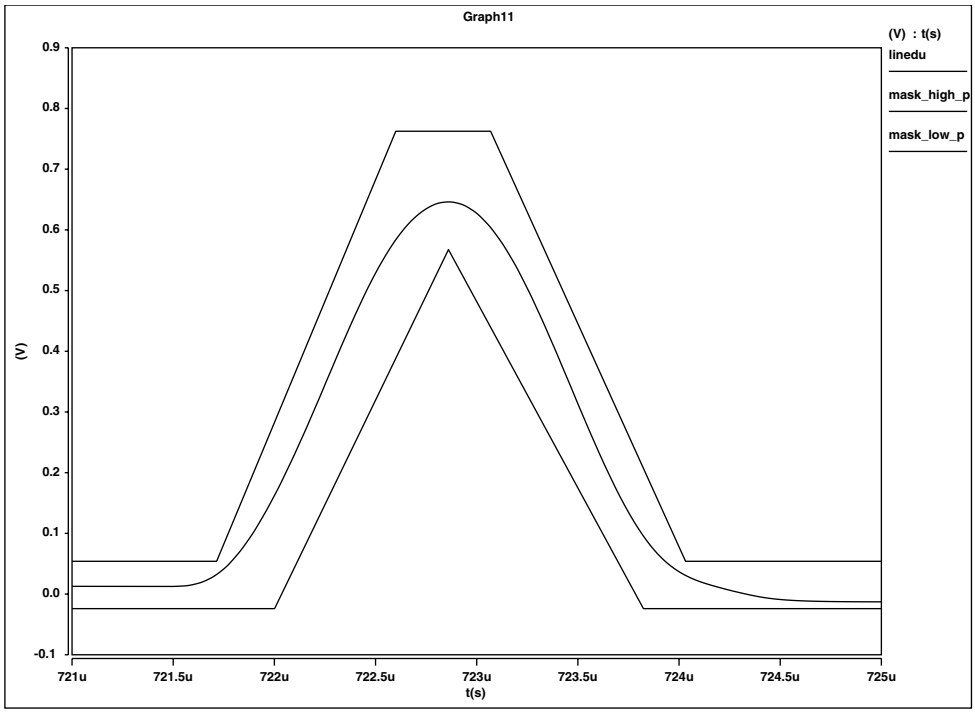
2.3.8 Transmitter Characteristics

The transmit pulses are raised cosine shaped in order to reduce RF energy, crosstalk and intersymbol interference.

Figure 42 shows a single pulse in the time domain compared against the pulse mask.

Figure 43 shows the theoretical power density of a random pattern scrambled by the polynom specified in **chapter 2.3.1**.

Figure 44 shows the typical power density of a random pattern scrambled by the polynom specified in **chapter 2.3.1**. This figure is obtained after the simulation of the integrated pulse shaper together with the external circuit of **figure 45**.



pulse_mask_d

Figure 42
Simulated Single Pulse compared against the Pulse Mask

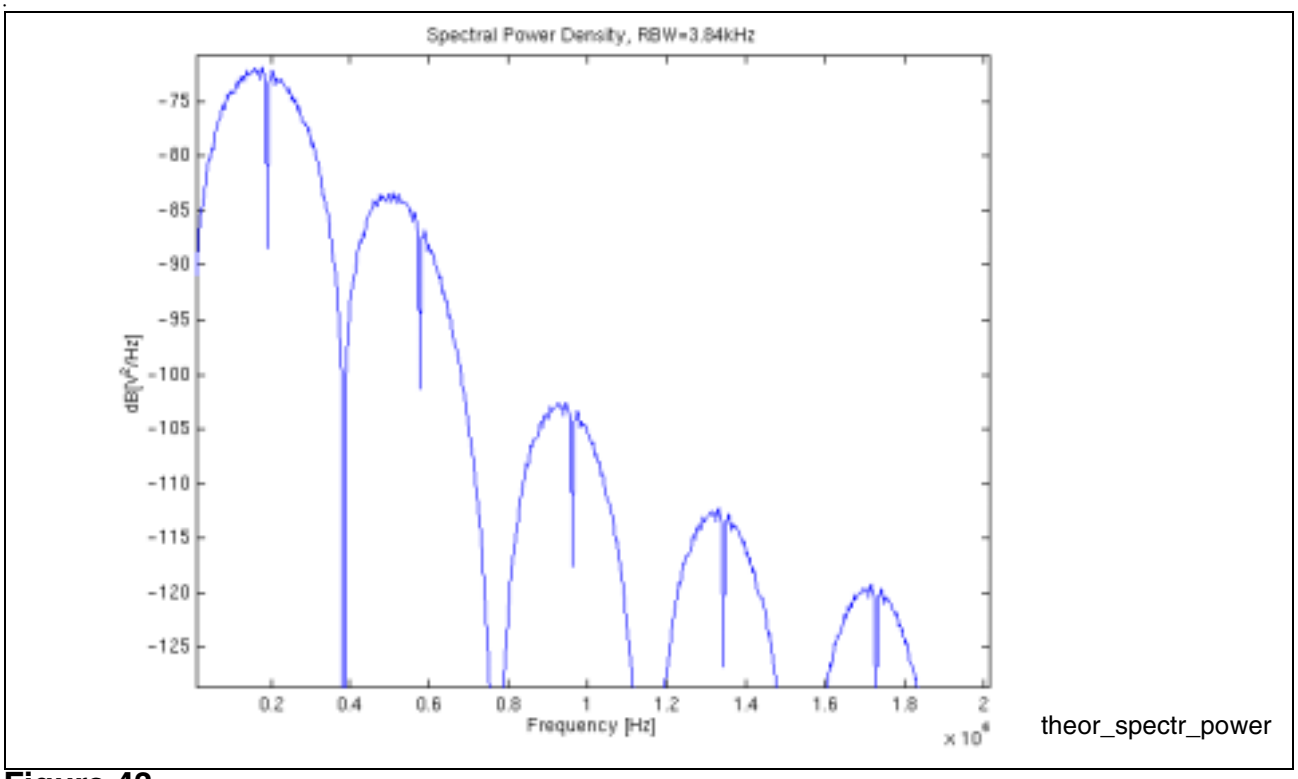


Figure 43
Theoretical spectral Power Density of a scrambled random Pattern

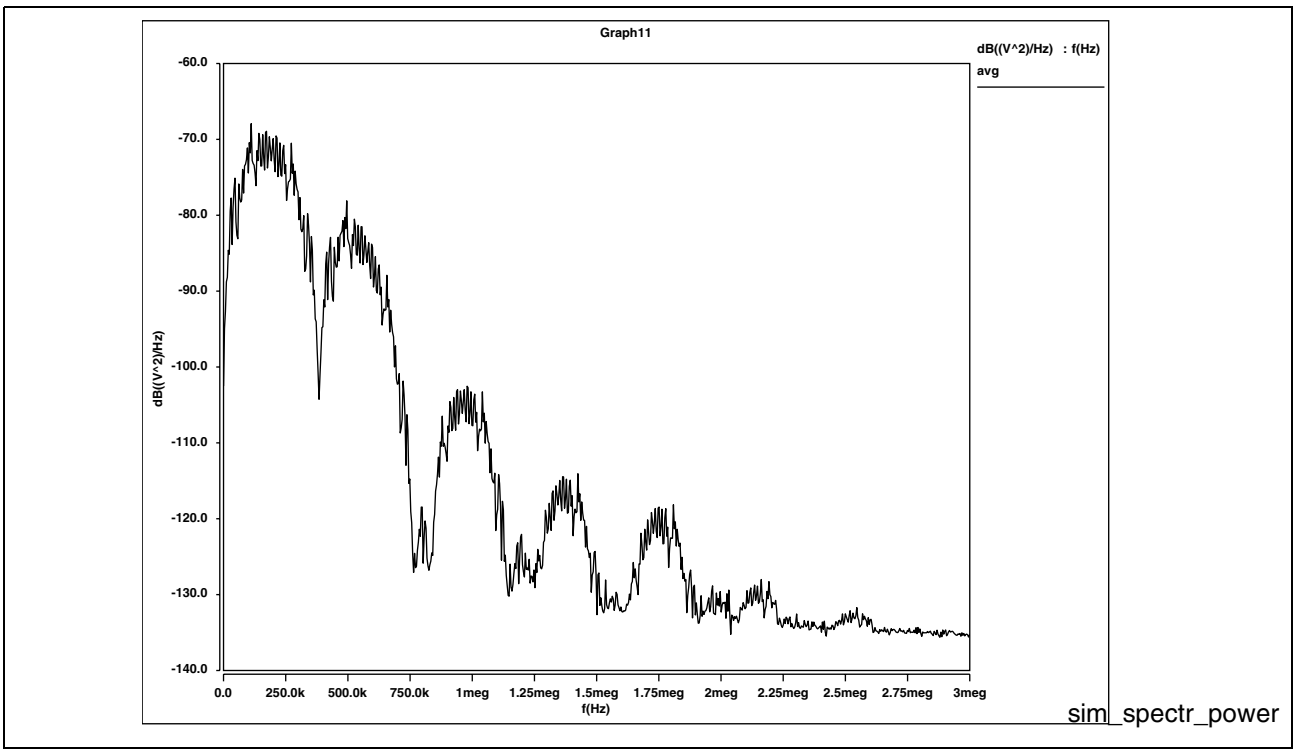


Figure 44
Typical spectral Power Density of a scrambled random Pattern

2.3.9 Receiver Characteristics

The SCOUT-DX covers the electrical requirements of the line interface for loop lengths of up to 1.8 km (6 kft) on AWG 24 cable.

In order to additionally reduce the bit error rate in severe conditions, the SCOUT-DX performs oversampling of the received signal and uses majority decision logic. The receive signal is sampled at 15.36 MHz clock intervals (XTAL).

2.3.10 Line Interface Circuitry

The connection of the line transformer is shown in **figure 45**. External to the line interface pins LIa and LIb a transformer and external resistors are connected as shown. Note that the internal resistors of the transformer are calculated as zero. The actual values of the external resistors must take into account the real resistor of the chosen transformer.

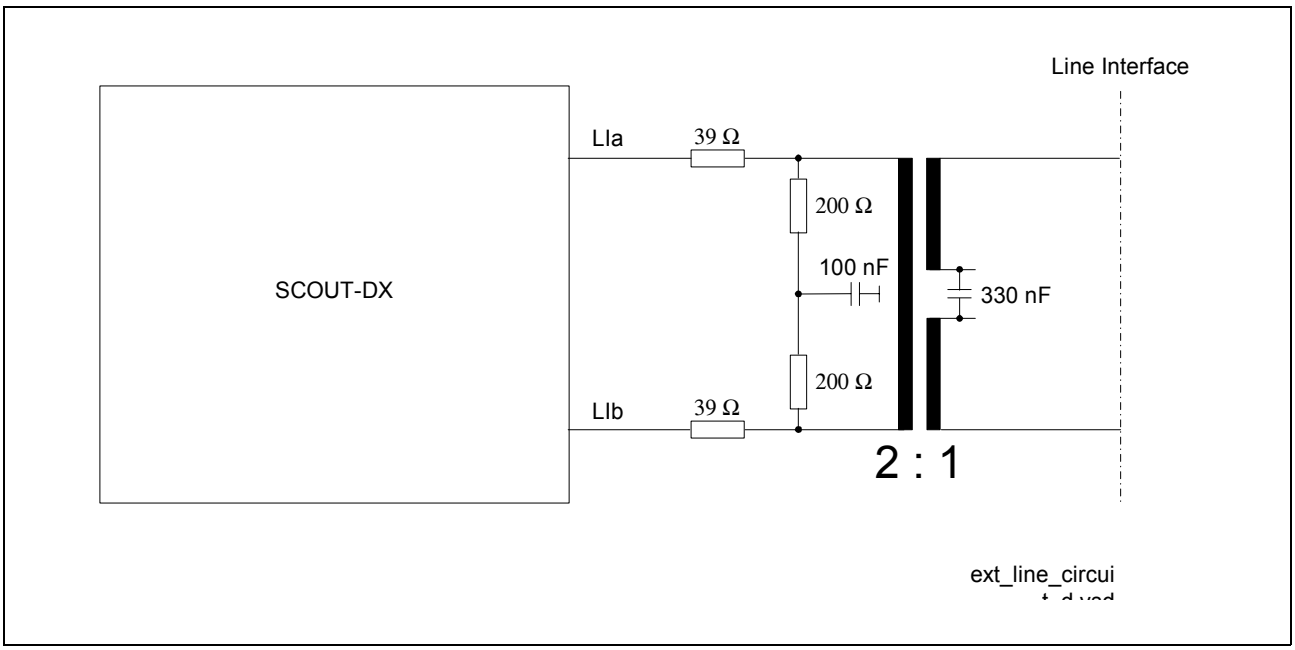


Figure 45
Connection of the Line Transformers to the SCOUT-DX

Because the SCOUT-DX will generate a voltage swing of about 1.4 Vpk at LIa/LIb (figure 44), a 2:1 transformer is needed to achieve the required 0.65 Vpk on the line interface. E.g. the use of a VAC 3-M5032-X013 transformer is recommended.

3 HDLC Controller

The HDLC controller handles layer-2 functions of the D- channel protocol (LAPD) or B-channel protocols. It can access the D or B-channels or any combination of them e.g. 18-bit IDSL data (2B+D) by setting the enable HDLC channel bits (EN_D, EN_B1H, EN_B2H) in the HCI_CR register.

It performs the framing functions used in HDLC based communication: flag generation/ recognition, bit stuffing, CRC check and address recognition.

One 64 byte FIFO for the receive and one for the transmit direction are available. They are implemented as cyclic buffers. The transceiver reads and writes data sequentially with constant data rate whereas the data transfer between FIFO and microcontroller uses a block oriented protocol with variable block sizes.

The configuration, control and status bits related to the HDLC controller are all assigned to the address range 20_H-29_H. (see **chapter 7.1**).

3.1 Message Transfer Modes

The HDLC controller can be programmed to operate in various modes, which are different in the treatment of the HDLC frame in receive direction. Thus the receive data flow and the address recognition features can be programmed in a flexible way to satisfy different system requirements.
The structure of a LAPD two-byte address is shown below.

High Address Byte			Low Address Byte	
SAPI1, 2, SAPG	C/R	0	TEI 1, 2, TEIG	EA

For the address recognition the HDLC controller contains four programmable registers for individual SAPI and TEI values (SAP1, 2 and TEI1, 2), plus two fixed values for the “group” SAPI (SAPG = ’FE’ or ’FC’) and TEI (TEIG = ’FF’).
The received C/R bit is excluded from the address comparison. EA is the address field extension bit which is set to ’1’ for LAPD protocol.

There are 5 different operating modes which can be selected via the mode selection bits MDS2-0 in the MODEH register:

3.1.1 Non-Auto Mode (MDS2-0 = ’01x’)

Characteristics: Full address recognition with one-byte (MDS = ’010’) or two-byte (MDS = ’011’) address comparison

All frames with valid addresses are accepted and the bytes following the address are transferred to the µP via RFIFO.

3.1.2 Transparent Mode 0 (MDS2-0 = ’110’).

Characteristics: no address recognition

Every received frame is stored in RFIFO (first byte after opening flag to CRC field).

3.1.3 Transparent Mode 1 (MDS2-0 = ’111’).

Characteristics: SAPI recognition

A comparison is performed on the first byte after the opening flag with SAP1, SAP2 and “group” SAPI (FE_H/FC_H). In the case of a match, all following bytes are stored in RFIFO.

3.1.4 Transparent Mode 2 (MDS2-0 = ’101’).

Characteristics: TEI recognition

A comparison is performed only on the second byte after the opening flag, with TEI1, TEI2 and group TEI (FF_H). In case of a match the rest of the frame is stored in the RFIFO.

3.1.5 Extended Transparent Mode (MDS2-0 = ’100’).

Characteristics: fully transparent

In extended transparent mode fully transparent data transmission/reception without HDLC framing is performed i.e. without FLAG generation/recognition, CRC generation/check, bit stuffing mechanism. This allows user specific protocol variations.
Also refer to **chapter 3.5**.

3.2 Data Reception

3.2.1 Structure and Control of the Receive FIFO

3.2.1.1 General Description

The 64-byte cyclic RFIFO buffer has variable FIFO block sizes (thresholds) of 4, 8, 16 or 32 bytes which can be selected by setting the corresponding RFBS bits in the EXMR register. The variable block size allows an optimized HDLC processing concerning frame length, I/O throughput and interrupt load.
The transfer protocol between HDLC FIFO and microcontroller is block orientated with

the microcontroller as master. The control of the data transfer between the CPU and the HDLC controller is handled via interrupts (HDLC controller → Host) and commands (Host → HDLC controller).

There are three different interrupt indications in the ISTAH register concerned with the reception of data:

– **RPF** (**R**eceive **P**ool **F**ull) interrupt, indicating that a data block of the selected length (EXMR.RFBS) can be read from RFIFO. The message which is currently received exceeds the block size so further blocks will be received to complete the message.
– **RME** (**R**eceive **M**essage **E**nd) interrupt, indicating that the reception of one message is completed, i.e. either
  - a short message is received
    (message length ≤ the defined block size (EXMR.RFBS) or
  - the last part of a long message is received
    (message length > the defined block size (EXMR.RFBS))
    and is stored in the RFIFO.
– **RFO** (**R**eceive **F**rame **O**verflow) interrupt, indicating that a complete frame could not be stored in RFIFO and is therefore lost as the RFIFO is occupied. This occurs if the host fails to respond quickly enough to RPF/RME interrupts since previous data was not read by the host.

There are two control commands (bits of CMDR) that are used with the reception of data:

– **RMC** (**R**eceive **M**essage **C**omplete) command, telling the HDLC controller that a data block has been read from the RFIFO and the corresponding FIFO space can be released for new receive data.
– **RRES** (**R**eceiver **R**eset) command, resetting the HDLC receiver and clearing the receive FIFO of any data (e.g. used before start of reception). It has to be used after having changed the mode.

The following description of the receive FIFO operation is illustrated in **figure 46** for a RFIFO block size (threshold) of 16 and 32 bytes.

The RFIFO requests service from the microcontroller by setting a bit in the ISTAH register, which causes an interrupt (RPF, RME, RFO). The microcontroller then reads status information (RBCH,RBCL), data from the RFIFO and changes the RFIFO block size (EXMR.RFBS). A block transfer is completed by the microcontroller via a receive message complete (CMDR.RMC) command. This causes the space of the transferred bytes being released for new data and in case the frame was complete (RME) the reset of the receive byte counter RBC (RBCH,RBCL).
The total length of the frame is contained in the RBCH and RBCL registers (RBC11...0). If a frame is longer than 4095 bytes, the RBCH.OV (overflow) bit will be set. The least significant bits of RBCL contain the number of valid bytes in the last data block indicated by RME (length of last data block ≤ selected block size). **Table 7** shows which RBC bits contain the number of bytes in the last data block or number of complete data blocks respectively. If the number of bytes in the last data block is ’0’ the length of the last received block is equal to the block size.

Table 7
Receive Byte Count with RBC11...0 in the RBCH and RBCL registers

EXMR.RFBS bits	Selected block size	Number of	
		complete data blocks in	bytes in the last data block in
’00’	32 byte	RBC11...5	RBC4...0
’01’	16 byte	RBC11...4	RBC3...0
’10’	8 byte	RBC11...3	RBC2...0
’11’	4 byte	RBC11...2	RBC1...0

The transfer block size (EXMR.RFBS) is 32 bytes by default. If it is necessary to react to an incoming frame within the first few bytes the microcontroller can set the RFIFO block size to a smaller value. Each time a CMDR.RMC or CMDR.RRES command is issued, the RFIFO access controller sets its block size to the value specified in EXMR.RFBS, so the microcontroller has to write the new value for RFBS before the RMC command. When setting an initial value for RFBS before the first HDLC activities, a RRES command must be issued afterwards.

The RFIFO can hold any number of frames fitting in the 64 bytes. At the end of a frame, the RSTA byte is always appended.

All generated interrupts are inserted together with all additional information into a wait line to be individually passed to the host. For example if several data blocks have been received to be read by the host and the host acknowledges the current block, a new RPF or RME interrupt from the wait line is immediately generated to indicate new data.

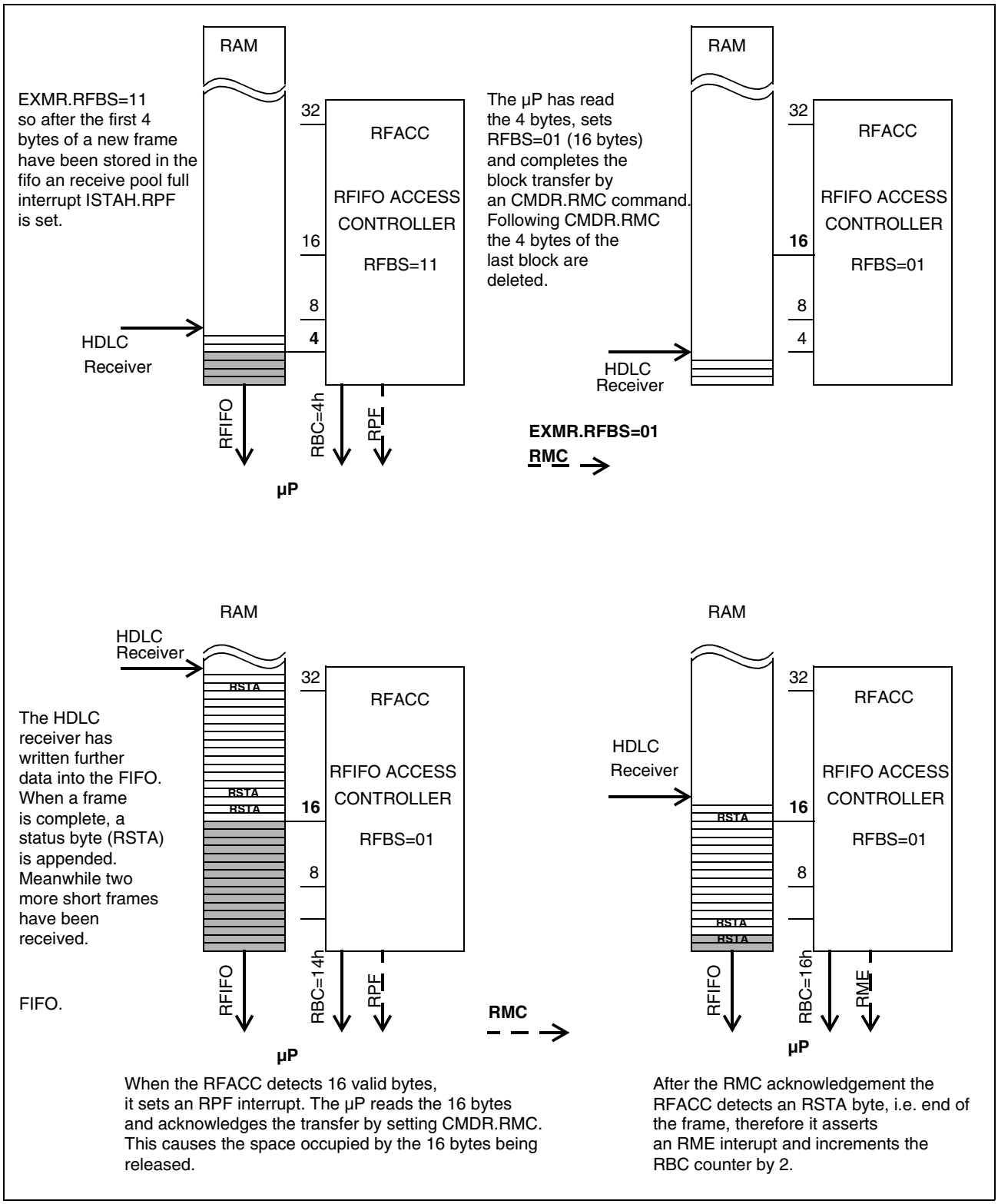


Figure 46
RFIFO Operation

3.2.1.2 Possible Error Conditions during Reception of Frames

If parts of a frame get lost because the receive FIFO is full, the Receive Data Overflow (RDO) byte in the RSTA byte will be set. If a complete frame is lost, i.e. if the FIFO is full when a new frame is received, the receiver will assert a Receive Frame Overflow (RFO) interrupt.

The microcontroller sees a cyclic buffer, i.e. if it tries to read more data than available, it reads the same data again and again. On the other hand, if it doesn't read or doesn't want to read all data, they are deleted anyway after the RMC command.

If the microcontroller reads data without a prior RME or RPF interrupt, the read data is undefined but the content of the RFIFO would not be corrupted.

3.2.1.3 Data Reception Procedure

The general procedures for a data reception sequence are outlined in the flow diagram in **figure 47**.

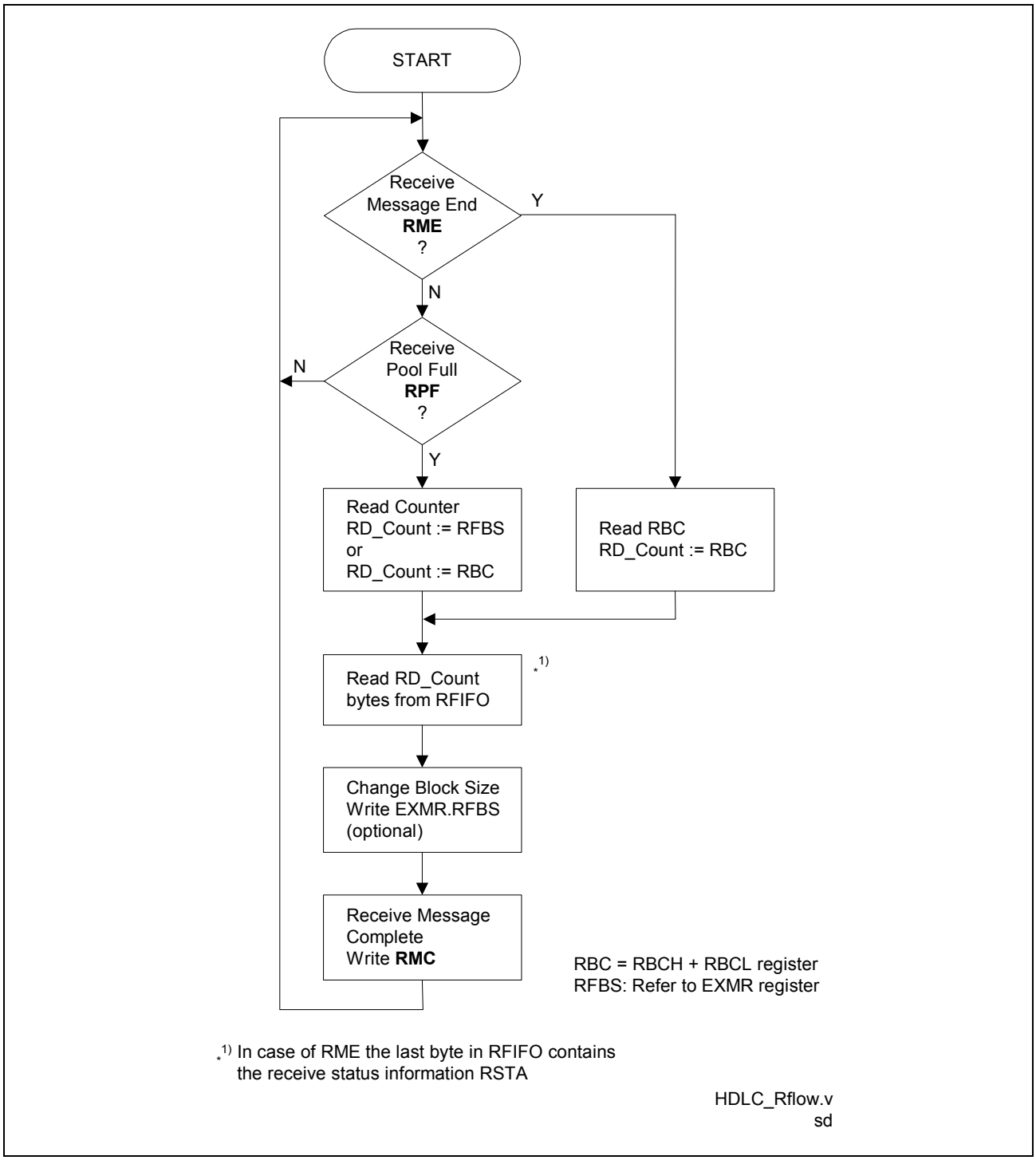


Figure 47
Data Reception Procedures

Figure 48 gives an example of an interrupt controlled reception sequence, supposed that a long frame (68 byte) followed by two short frames (12 byte each) is received. The FIFO threshold (block size) is set to 32 byte (EXMR.RFBS = ’00’) in this example:

- After 32 bytes of frame 1 have been received an RPF interrupt is generated to indicate that a data block can be read from the RFIFO.
- The host reads the first data block from RFIFO and acknowledges the reception by RMC. Meanwhile the second data block is received and stored in RFIFO.
- The second 32 byte block is indicated by RPF which is read and acknowledged by the host as described before.
- The reception of the remaining 4 bytes plus RSTA are indicated by RME.
- The host gets the number of received bytes (COUNT = 5) from RBCL/RBCH and reads out the RFIFO. The frame is acknowledged by RMC.
- The second frame is received and indicated by RME interrupt.
- The host gets the number of bytes (COUNT = 13) from RBCL/RBCH and reads out the RFIFO. The RFIFO is acknowledged by RMC.
- The third frame is transferred in the same way.

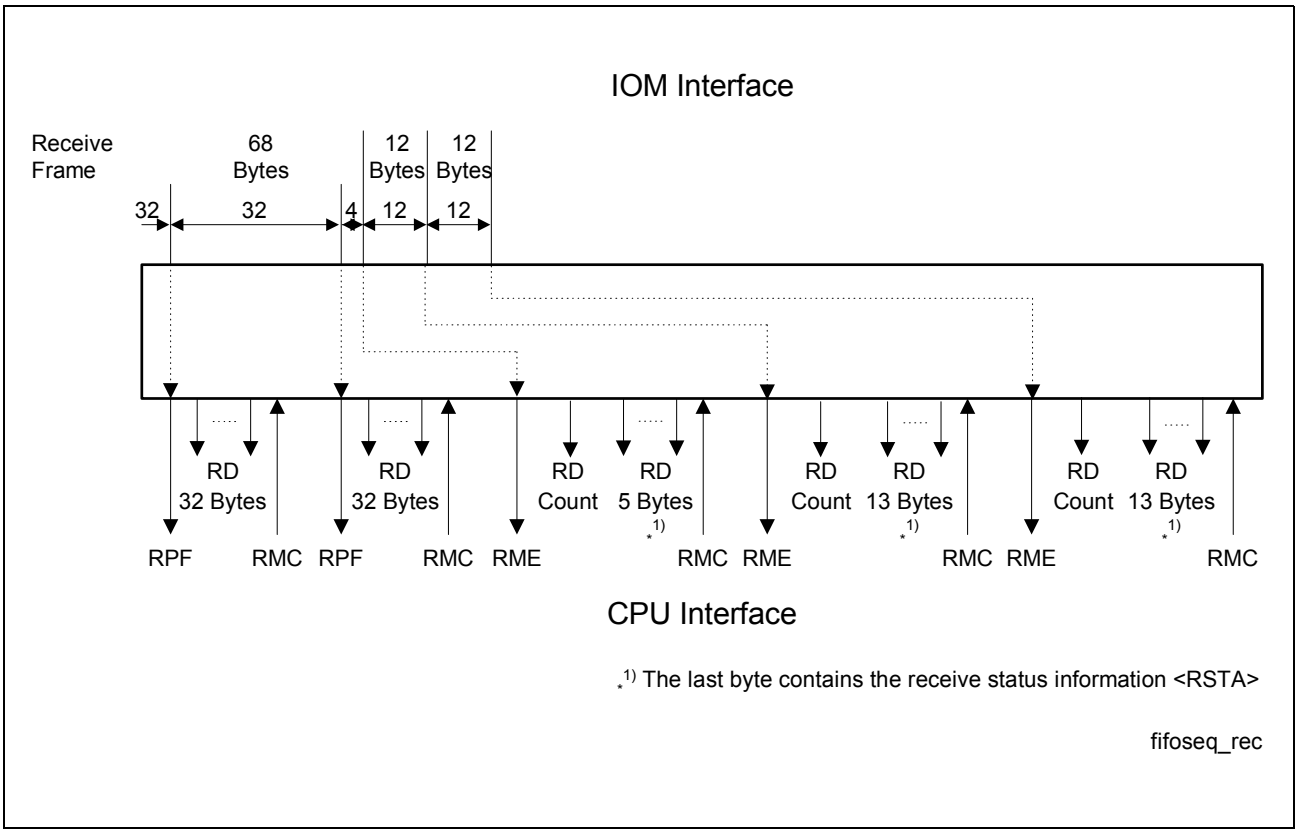


Figure 48
Reception Sequence, Example

3.2.2 Receive Frame Structure

The management of the received HDLC frames as affected by the different operating modes (see **chapter 3.1**) is shown in **figure 49**.

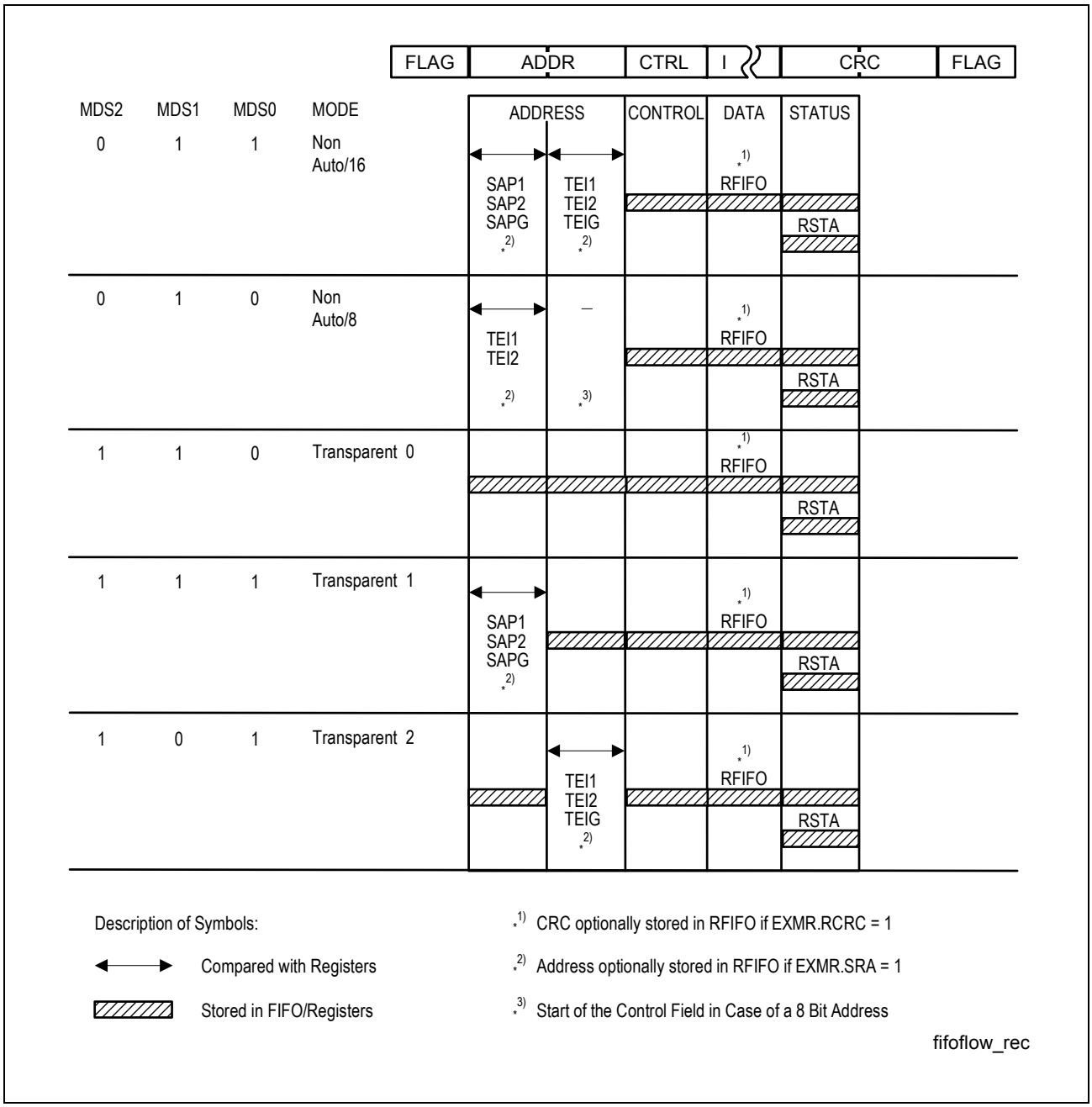


Figure 49
Receive Data Flow

The HDLC controller indicates to the host that a new data block can be read from the RFIFO by means of an RPF interrupt (see previous chapter). User data is stored in the RFIFO and information about the received frame is available in the RSTA, RBCL and RBCH registers which are listed in **table 8**.

Table 8
Receive Information at RME Interrupt

Information	Location	Bit	Mode
Type of frame (Command/ Response)	RFIFO (last byte)	C/R	Non-auto mode, 2-byte address field Transparent mode 1
Recognition of SAPI	RFIFO (last byte)	SA1, 0	Non-auto mode, 2-byte address field Transparent mode 1
Recognition of TEI	RFIFO (last byte)	TA	All except transparent mode 0
Result of CRC check (correct/incorrect)	RFIFO (last byte)	CRC	All
Valid Frame	RFIFO (last byte)	VFR	All
Abort condition detected (yes/no)	RFIFO (last byte)	RAB	All
Data overflow during reception of a frame (yes/no)	RFIFO (last byte)	RDO	All
Number of bytes received in RFIFO	RBCL Reg.	RBC4-0	All
Message length	RBCL Reg. RBCH Reg.	RBC11-0	All
RFIFO Overflow	RBCH Reg.	OV	All

3.3 Data Transmission

3.3.1 Structure and Control of the Transmit FIFO

3.3.1.1 General Description

The 64-byte cyclic XFIFO buffer has variable FIFO block sizes (thresholds) of 16 or 32 bytes, selectable by the XFBS bit in the EXMR register.

There are three different interrupt indications in the ISTAH register concerned with the transmission of data:

– **XPR** (**T**ransmit **P**ool **R**eady) interrupt, indicating that a data block of up to 16 or 32 byte (block size selected via EXMR:XFBS) can be written to the XFIFO.
  An XPR interrupt is generated either
  - after an XRES (Transmitter Reset) command (which is issued for example for frame abort) or
  - when a data block from the XFIFO is transmitted and the corresponding FIFO space is released to accept further data from the host.

– **XDU** (**T**ransmit **D**ata **U**nderrun) interrupt, indicating that the transmission of the current frame has been aborted (seven consecutive ’1’s are transmitted) as the XFIFO holds no further transmit data. This occurs if the host fails to respond to an XPR interrupt quickly enough.

– **XMR** (**T**ransmit **M**essage **R**epeat) interrupt, indicating that the transmission of the complete last frame has to be repeated as a collision on the S bus has been detected and the XFIFO does not hold the first data bytes of the frame (collision after the 16th or 32nd byte of the frame, respectively).

Three different control commands are used for transmission of data:

– **XTF** (**T**ransmit **T**ransparent **F**rame) command, telling the HDLC controller that up to 16 or 32 byte (according to selected block size) have been written to the XFIFO and should be transmitted. A start flag is generated automatically.

– **XME** (**T**ransmit **M**essage **E**nd) command, telling the HDLC controller that the last data block written to the XFIFO completes the corresponding frame and should be transmitted. This implies that according to the selected mode a frame end (CRC + closing flag) is generated and appended to the frame.

– **XRES** (**T**ransmitter **R**eset) command, resetting the HDLC transmitter and clearing the transmit FIFO of any data.

Optionally two additional status conditions can be read by the host:

– **XDOV** (**T**ransmit **D**ata **O**verflow), indicating that the data block size has been exceeded, i.e. more than 16 or 32 byte were entered and data was overwritten.

– **XFW** (**T**ransmit **F**IFO **W**rite Enable), indicating that data can be written to the XFIFO. This status flag may be polled instead of or in addition to XPR.

The XFIFO requests service from the microcontroller by setting a bit in the ISTAH register, which causes an interrupt (XPR, XDU, XMR). The microcontroller can then read the status register STAR (XFW, XDOV), write data in the FIFO and it can change the transmit FIFO block size (EXMR.XFBS) if required.
The instant of the initiation of a transmit pool ready (XPR) interrupt after different transmit control commands is listed in **table 9**.

Table 9
XPR Interrupt (availability of the XFIFO) after XTF, XME Commands

CMDR.	Transmit pool ready (XPR) interrupt initiated...
XTF	as soon as the selected buffer size in the FIFO is available
XTF & XME	after the successful transmission of the closing flag. The transmitter sends always an abort sequence
XME	as soon as the selected buffer size in the FIFO is available, two consecutive frames share flags

When setting XME the transmitter appends the FCS and the end flag at the end of the frame. When XTF & XME has been set, the XFIFO is locked until successful transmission of the current frame, so a consecutive XPR interrupt also indicates successful transmission of the frame whereas after XME or XTF the XPR interrupt is asserted as soon as there is space for one data block in the XFIFO.

The transfer block size is 32 bytes by default, but sometimes, if the microcontroller has a high computational load, it is useful to increase the maximum reaction time for an XPR interrupt. The maximum reaction time is:
t_{max} = (XFIFO size - XFBS) / data transmission rate
A selected block size of 16 bytes means that an XPR interrupt is indicated when there are still 48 bytes (64 bytes - 16 bytes) to be transmitted. With a 32 bytes block size the XPR is initiated when there are still 32 bytes (64 bytes - 32 bytes), i.e. the maximum reaction time for the smaller block size is 50 % higher with the trade-off of a doubled interrupt load. A selected block size of 32 or 16 bytes respectively always indicates the available space in the XFIFO. So any number of bytes smaller than the selected XFBS may be stored in the FIFO during one “write block“ access cycle.

Similar to RFBS for the receive FIFO, a new setting of XFBS takes effect after the next XTF,XME or XRES command. XRES resets the XFIFO.

The XFIFO can hold any number of frames fitting in the 64 bytes.

3.3.1.2 Possible Error Conditions during Transmission of Frames

If the transmitter sees an empty FIFO, i.e. if the microcontroller does not react quickly enough to an XPR interrupt, an XDU (transmit data underrun) interrupt will be raised. If the HDLC channel becomes unavailable during transmission the transmitter tries to repeat the current frame as specified in the LAPD protocol. This is impossible after the first data block has been sent (16 or 32 bytes), in this case an XMR transmit message repeat interrupt is set and the microcontroller has to send the whole frame again.

Both XMR and XDU interrupts cause a reset of the XFIFO. The XFIFO is locked while an XMR or XDU interrupt is pending, i.e. all write actions of the microcontroller will be ignored as long as the microcontroller has not read the ISTAH register with the set XDU, XMR interrupts.

If the microcontroller writes more data than allowed (16 or 32 bytes), then the data in the XFIFO will be corrupted and the STAR.XDOV bit is set. If this happens, the microcontroller has to abort the transmission by CMDR.XRES and to restart.

3.3.1.3 Data Transmission Procedure

The general procedures for a data transmission sequence are outlined in the flow diagram in **figure 50**.

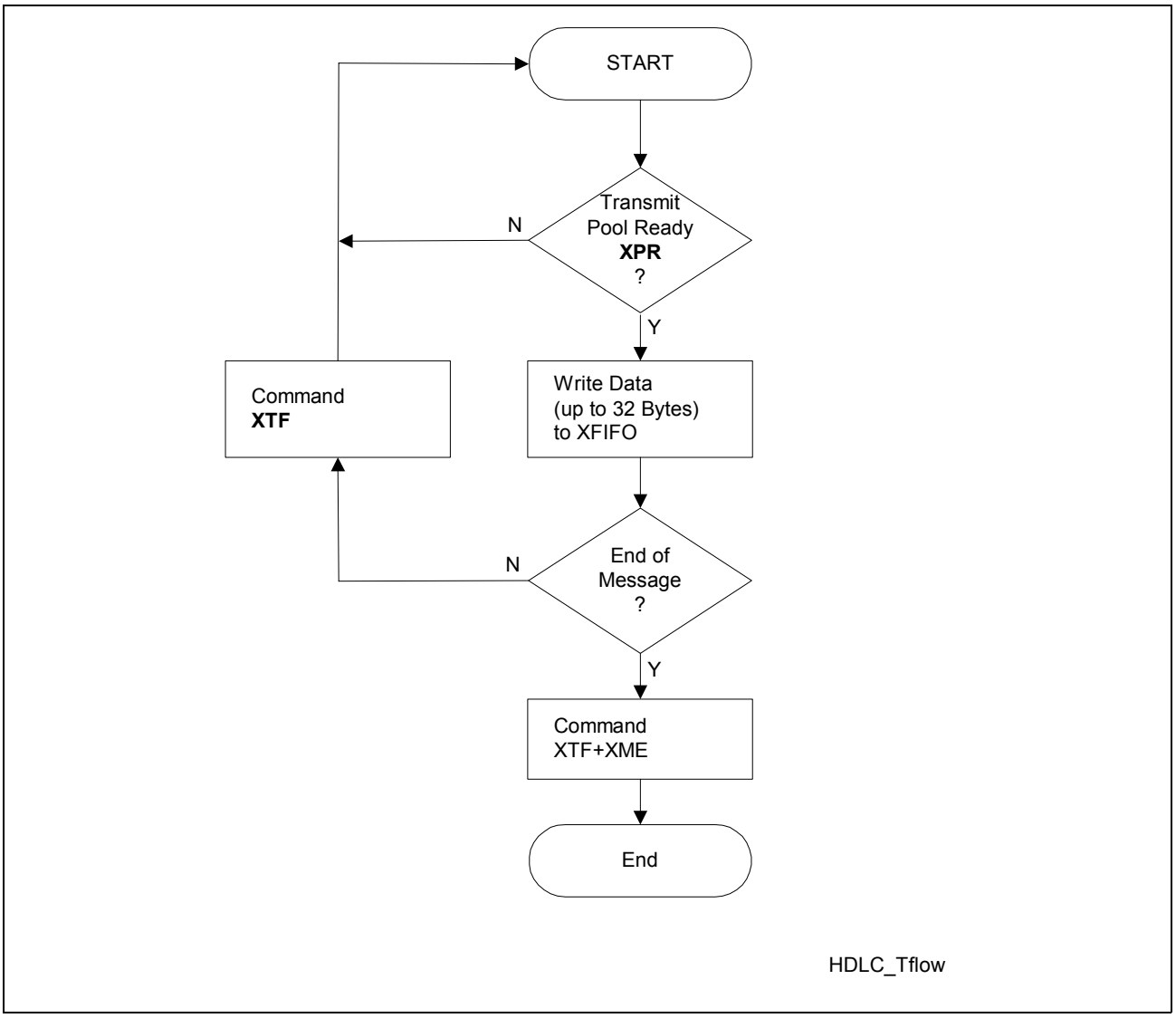


Figure 50
Data Transmission Procedure

The following description gives an example for the transmission of a 76 byte frame with a selected block size of 32 byte (EXMR:XFBS=0):

- The host writes 32 bytes to the XFIFO, issues an XTF command and waits for an XPR interrupt in order to continue with entering data.
- The HDLC controller immediately issues an XPR interrupt (as remaining XFIFO space is not used) and starts transmission.
- Due to the XPR interrupt the host writes the next 32 bytes to the XFIFO, followed by the XTF command, and waits for XPR.
- As soon as the last byte of the first block is transmitted, the HDLC controller issues an XPR interrupt (XFIFO space of first data block is free again) and continues transmitting the second block.
- The host writes the remaining 12 bytes of the frame to the XFIFO and issues the XTF command together with XME to indicate that this is the end of frame.
- After the last byte of the frame has been transmitted the HDLC controller releases an XPR interrupt and the host may proceed with transmission of a new frame.

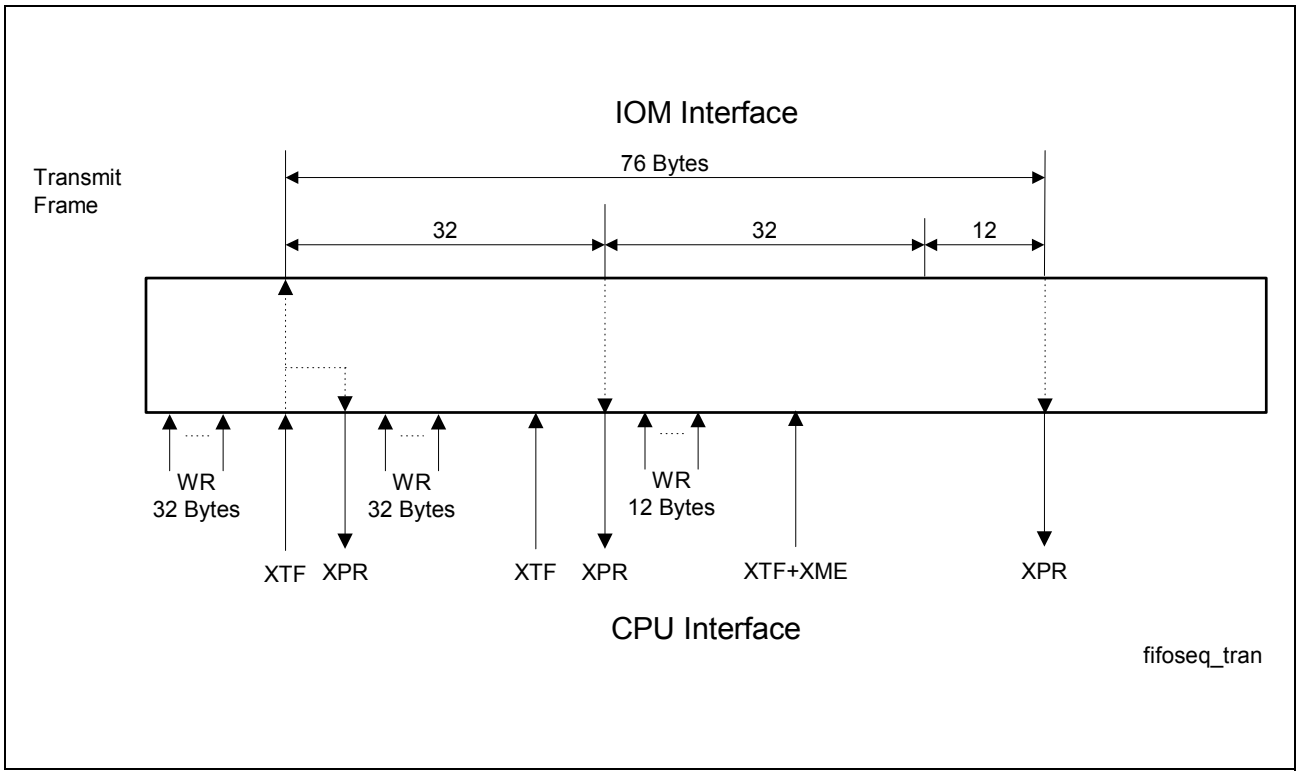


Figure 51
Transmission Sequence, Example

3.3.2 Transmit Frame Structure

The transmission of transparent frames (XTF command) is shown in **figure 52**.

For transparent frames, the whole frame including address and control field must be written to the XFIFO. The host configures whether the CRC is generated and appended to the frame (default) or not (selected in EXMR.XCRC).

Furthermore, the host selects the interframe time fill signal which is transmitted between HDLC frames (EXMR:ITF). One option is to send continuous flags ('01111110'), however if D-channel access handling is required, the signal must be set to idle (continuous '1's are transmitted).

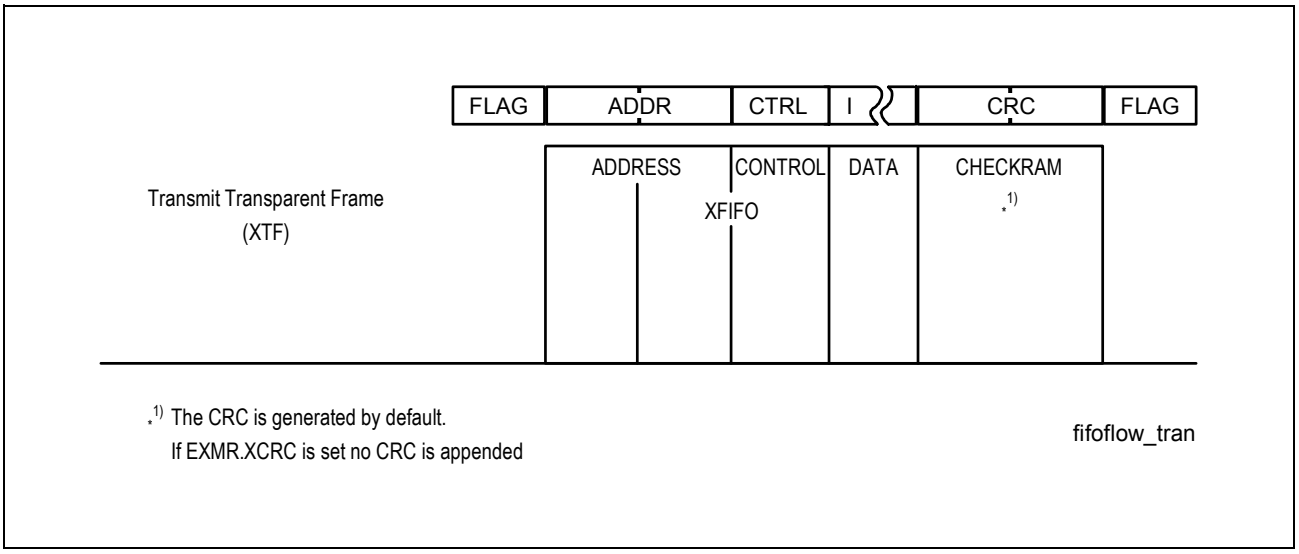


Figure 52
Transmit Data Flow

3.4 Access to IOM Channels

By setting the enable HDLC data bits (EN_D, EN_B1H, EN_B2H) in the HCI_CR register the HDLC controller can access the D, B1, B2 channels or the combination of them (e.g. 18 bit IDSL data (2B+D)). In all modes sending works always frame aligned, i.e. it starts with the first selected channel whereas reception looks for a flag anywhere in the serial data stream.

3.5 Extended Transparent Mode

This non-HDLC mode is selected by setting MODE2...0 to ’100’. In extended transparent mode fully transparent data transmission/reception without HDLC framing is performed i.e. without FLAG generation/recognition, CRC generation/check, bit stuffing mechanism. This allows user specific protocol variations.

3.5.1 Transmitter

The transmitter sends the data out of the FIFO without manipulation. Transmission is always IOM-frame aligned and byte aligned, i.e. transmission starts in the first selected channel (B1, B2, D, according to the setting of register HCI_CR in the IOM Handler) of the next IOM frame.

The FIFO indications and commands are the same as in other modes.

If the microcontroller sets XTF & XME the transmitter responds with an XPR interrupt after sending the last byte, then it returns to its idle state (sending continuous ‘1’).

If the collision detection is enabled (MODE.DIM = ’0x1’) the stop go bit (S/G) can be used as clear to send indication as in any other mode. If the S/G bit is set to ’1’ (stop) during transmission the transmitter responds always with an XMR (transmit message repeat) interrupt.

If the microcontroller fails to respond to a XPR interrupt in time and the transmitter runs out of data then it will assert an XDU (transmit data underrun) interrupt.

3.5.2 Receiver

The reception is IOM-frame aligned and byte aligned, like transmission, i.e. reception starts in the first selected channel (B1, B2, D, according to the setting of register HCI_CR in the IOM Handler) of the next IOM frame. The FIFO indications and commands are the same as in others modes.

All incoming data bytes are stored in the RFIFO and additionally made available in RSTA. If the FIFO is full an RFO interrupt is asserted (EXMR.SRA = ’0’).

Note: In the extended transparent mode the EXMR register has to be set to ’xxx00000’

3.6 HDLC Controller Interrupts

The cause of an interrupt related to the HDLC controller is indicated by the HDLC bit in the ISTA register. This bit points at the different interrupt sources of the HDLC controller part in the ISTAH register. The individual interrupt sources of the HDLC controller during reception and transmission of data are explained in **chapter 3.2.1** or **3.3.1** respectively.

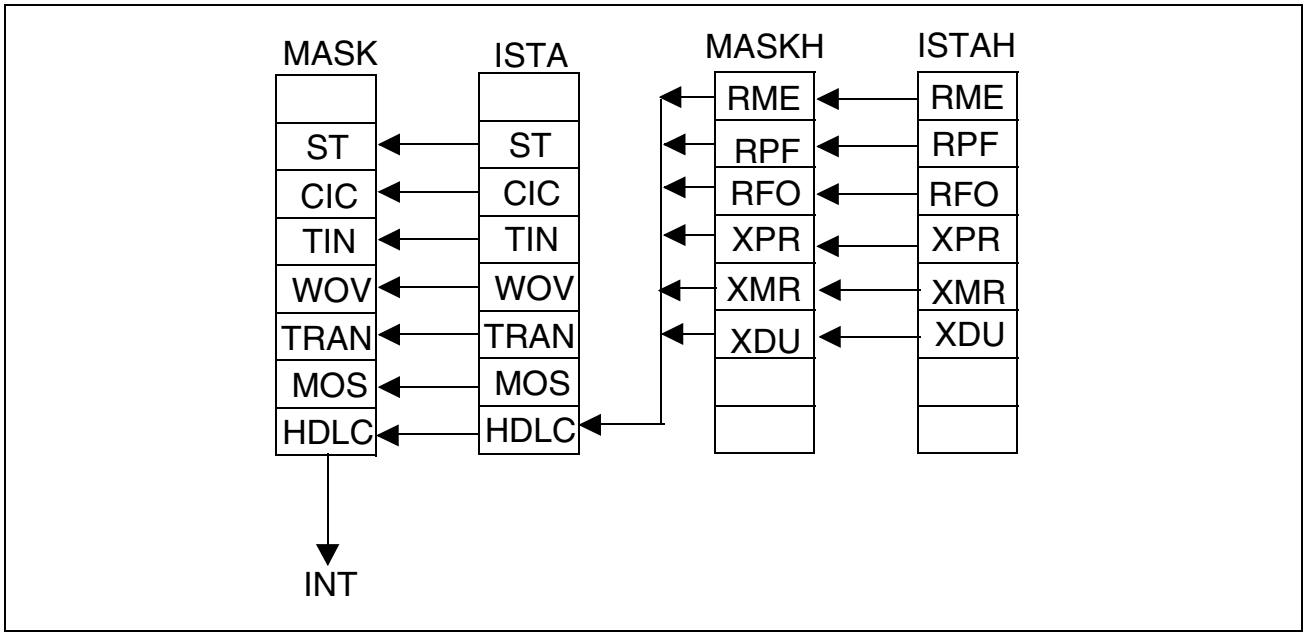


Figure 53
Interrupt Status Registers of the HDLC Controller

Each interrupt source in ISTAH register can be selectively masked by setting to “1” the corresponding bit in MASKH.

3.7 Test Functions

The following test and diagnostic functions for the D-channel are available:

– Digital loop via TLP (Test Loop, TMH register) command bit (**figure 54**): The TX path of layer 2 is internally connected with the RX path of layer 2. The output from layer 1 on DD is ignored. This is used for testing layer 2 functionality excluding layer 1 (loop back between XFIFO and RFIFO).
– Test of layer-2 functions while disabling all layer-1 functions and pins associated with them (including clocking) via bit TR_CONF0.DIS_TR. The HDLC controller and codec part can still operate via IOM-2. DCL and FSC pins become input.

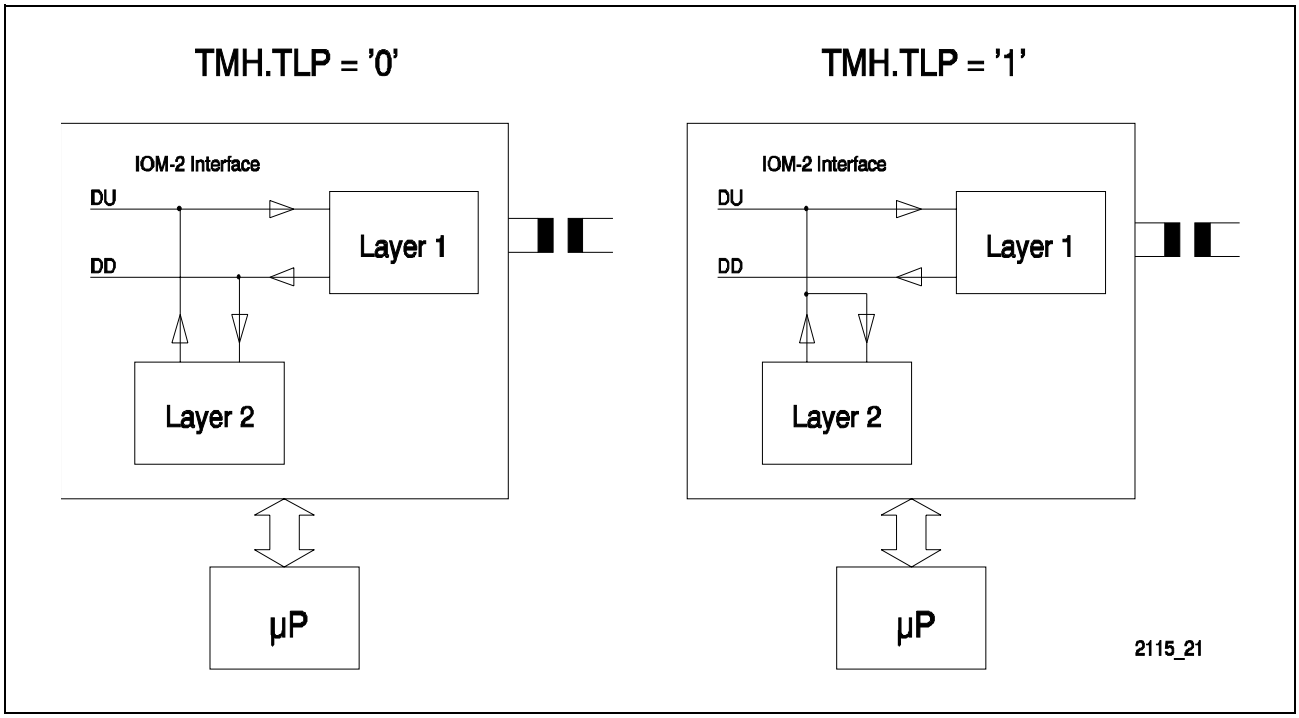


Figure 54
Layer 2 Test Loops

4 Codec

The codec bridges the gap between the audio world of microphones, earphones, loudspeakers and the PCM digital world by providing a full PCM codec with all the necessary transmit and receive filters.
Because the requirements for the codec correspond to the ARCOFI-SP PSB 2163 or ARCOFI®-BA PSB 2161 respectively the architecture, functionality and transmission characteristics are similar to those devices.

A block diagram of the codec is shown in **figure 55**.

The codec can be subdivided into three main blocks:

- Analog Front End (AFE)
- Digital Signal Processor (DSP)
- Codec Digital Interface (CDI)

A detailed description can be found in the following chapters.

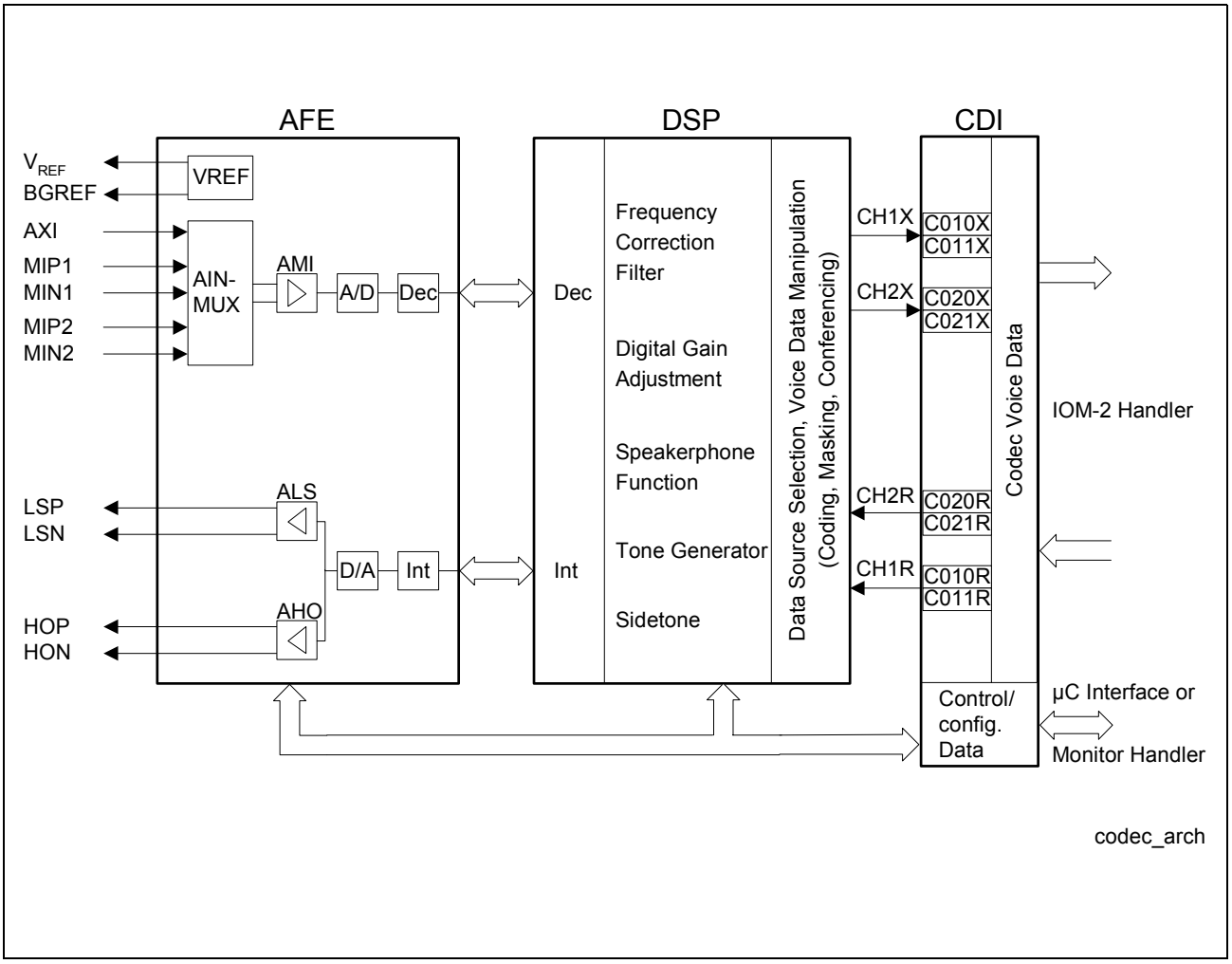


Figure 55
Architecture of the codec

The controlling and programming of the various operation modes, configurations and coefficients can be done via the microcontroller interface or the IOM-2 monitor channel and is described in the corresponding interface section. An overview on these programmable parameters can be found in **chapter 4.8**.

4.1 Analog Front End (AFE) Description

The Analog Front End section of the codec is the interface between the analog transducers and the digital signal processor. In the transmit direction the AFE function is to amplify the transducer input signals (microphones) and to convert them into digital signals. In the AFE receive section the incoming digital signal is converted to an analog signal which is output to an ear piece and/or a loudspeaker.

The three AFE configuration registers (ACR, ATCR, ARCR) provide a high flexibility to accommodate an extensive set of user procedures and terminal attributes.

•**Figure 56** shows the block diagram of the Analog Front End:

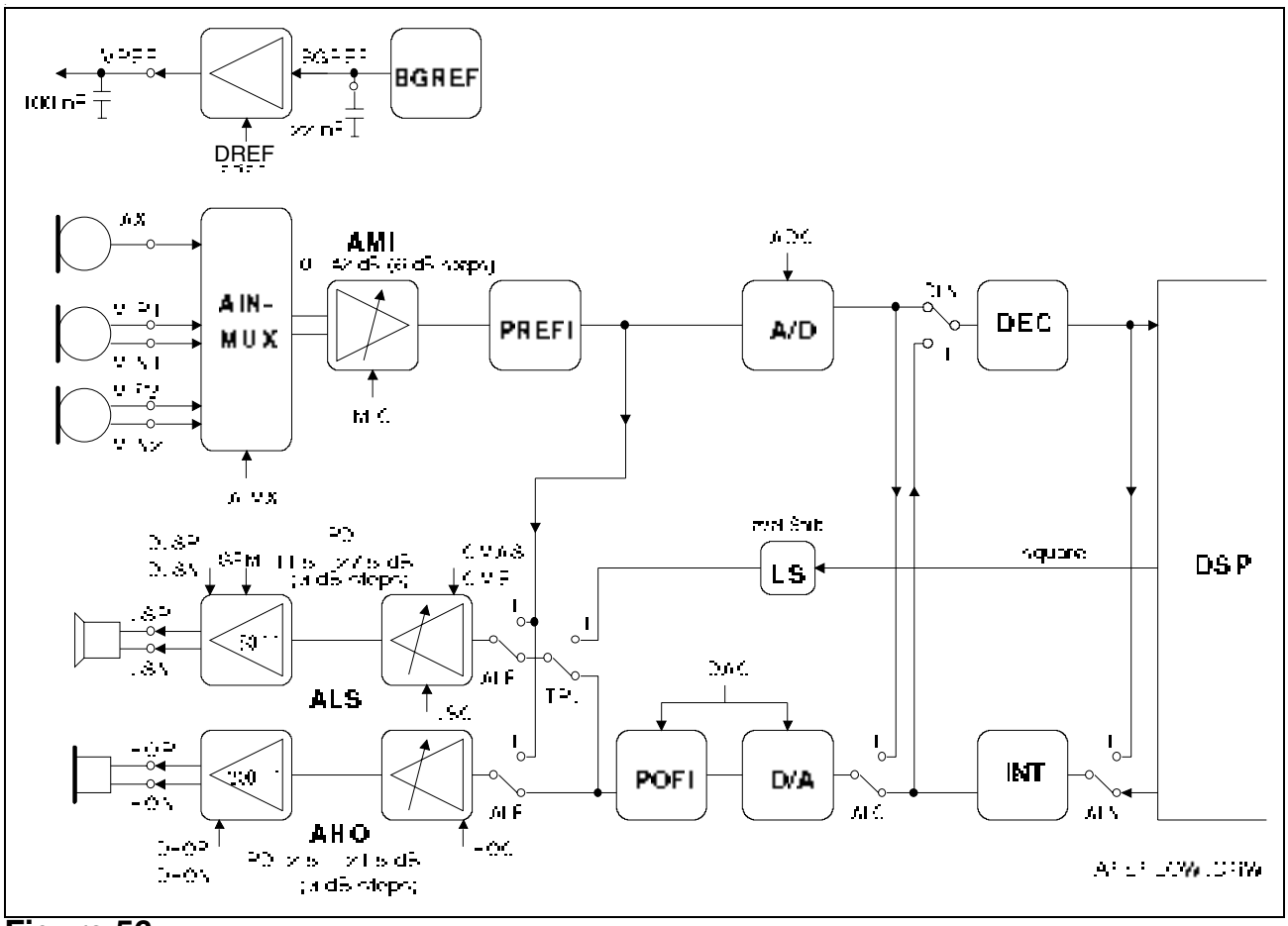


Figure 56
Block Diagram of AFE

Two differential inputs (MIP1/MIN1 and MIP2/MIN2) and one single-ended input (AXI) can be connected to the amplifier AMI via an analog input multiplexer (ATCR.AIMX). The programmable amplifier AMI (ATCR.MIC) provides a coarse gain adjustment range from

0...42 dB in 6 dB steps. The maximum value of the programmable gain adjustment of the microphone amplifier with specified transmission characteristics is 36 dB for the differential input. The maximum gain value with specified transmission characteristics of the single ended input AXI is 24 dB. Fine gain adjustment is performed in the digital domain via the programmable gain adjustment stage GX (see signal processor section). This allows a perfect level adaptation to various types of microphone transducers without loss in the signal to noise performance.

The fully differential output HOP/HON connects the amplifier AHO to a handset hairpiece. Differential output LSP/LSN is provided for use with a 50 Ω loudspeaker. The programmable amplifiers AHO and ALS (ARCR.HOC, ARCR.LSC) provide a coarse gain adjustment range from 11.5 dB...-21.5 dB (ALS) or 2.5 dB...-21.5 dB (AHO) respectively. The step size is for both amplifiers 3dB. Fine gain adjustment is performed in the digital domain via the programmable adjustment stage GR.
Each output of the differential amplifiers AHO and ALS can be powered down separately (ACR.DHOP, DHON, DLSP, DLSN). By setting ACR.SEM, a powered down loudspeaker output can be grounded internally for a single ended operation.

The bandgap reference voltage is low-pass filtered via a capacity connected to pin BGREF. The internal and external reference voltages are derived from this filtered bandgap reference voltage providing a good noise performance.
A square wave signal from the tone generator can be output directly to the loudspeaker amplifier (TGSR.TRL) via a level shifter. The A/D and D/A converters can be powered down by setting the ACR.ADC and ACR.DAC bits.

Note: The single-ended input (AXI) is internally connected to VREF. To avoid an unsymmetric input signal to the internal amplifer module, external resitors must not be connected between AXI and GND or AXI and VREF.

4.1.1 AFE Attenuation Plan

Figure 57 shows the attenuation plan of the AFE for the transmit and receive direction. The levels are given for the digital reference level (0 dBm0) and the max. PCM level in A-law coding (3.14 dBm0) for a supply voltage of 5 V.

The stated microphone amplifier gain (36 dB or 30 dB respectively) is the maximum gain for guaranteed transmission characteristics.

In the receive path the stated loudspeaker or handset output amplification is the maximum selectable gain at the maximum digital PCM level (3.14 dBm0) for guaranteed transmission characteristics.

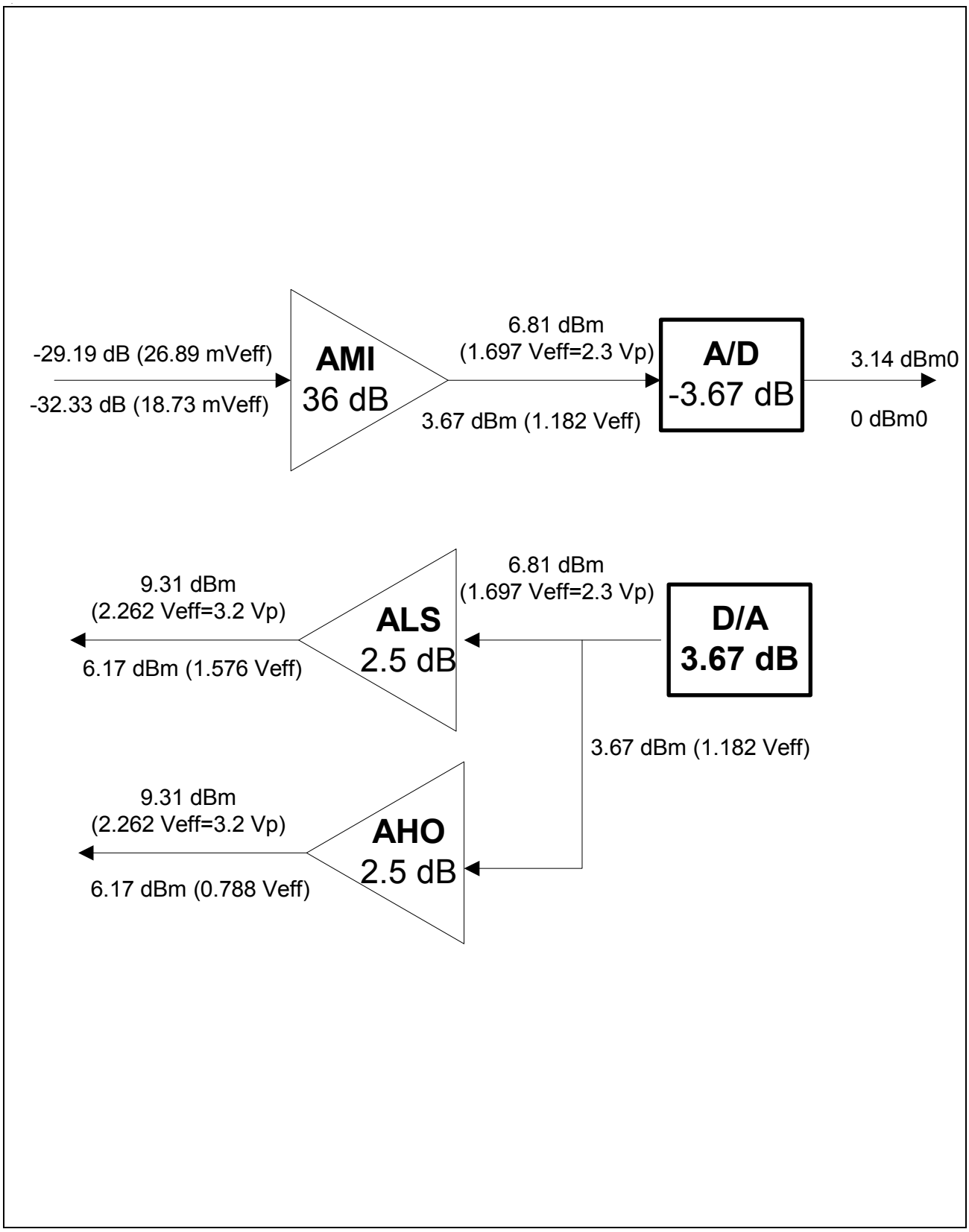


Figure 57
AFE Attenuation Plan

4.2 Signal Processor (DSP) Description

The signal processor (DSP) has been conceived to perform all ITU-T and ETSI (NET33) recommended filtering in transmit and receive paths and is therefore fully compatible to the ITU-T G.712 and ETSI (NET33) specifications. The data processed by the DSP is provided in the transmit direction by an oversampling A/D-converter situated in the analog front end (AFE). Once processed, the speech signal is converted into an 8-bit A-law or μ-law PCM format or remains as a 16-bit linear word (2s complement) if the compression stage is bypassed. In the receive direction, the incoming PCM data is expanded into a linear format (if the linear mode is selected, the expansion logic is bypassed) and subsequently processed until it is passed to the oversampling D/A-converter.

Additionally to these standard codec functions an universal tone generation unit and a high quality speakerphone function is provided. **Figure 58** shows the processor signal flow graph which illustrates the following description of the signal processing in receive and transmit direction, the tone generation and speakerphone function.

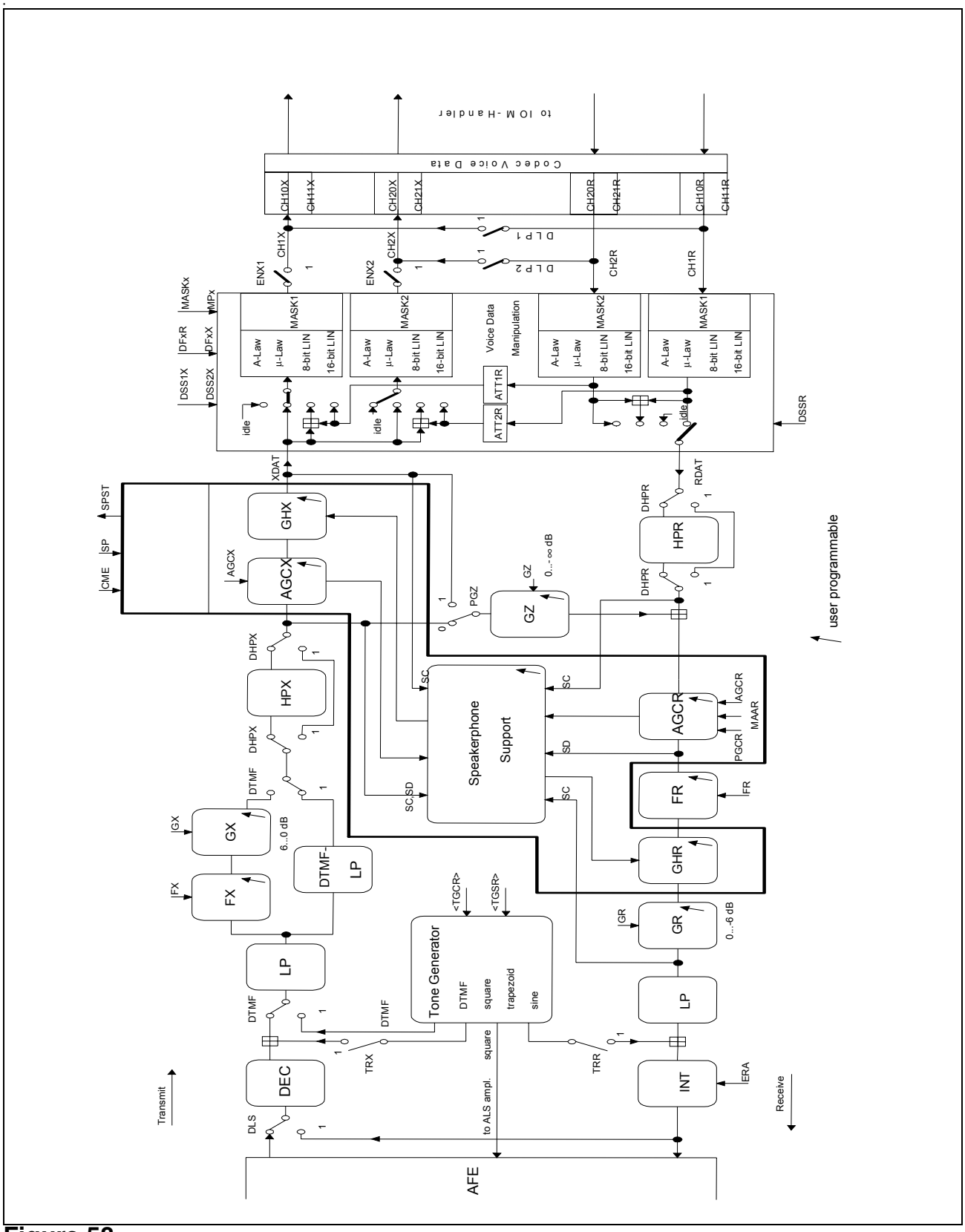


Figure 58
Processor Signal Flow Graph

4.2.1 Transmit Signal Processing

In the transmit direction a series of decimation filters reduces the sampling rate down to the 8-kHz PCM-rate. These filters attenuate the out-of-band noise by limiting the transmit signal to the voice band. The decimation stages end with a low-pass filter (LP).

If the tone generation unit is connected to the transmit direction (TGSR.DTMF = ’1’), a special 2-kHz DTMF low-pass filter is placed in the transmit path. This filter guarantees an attenuation of all unwanted frequency components, if DTMF signals are transmitted. Additionally, it is possible to add a programmable tone signal to the transmit voice signal (TGSR.TRX = ’1’).

The GX-gain adjustment stage is digitally programmable allowing the gain to be programmed from + 6 to 0 dB in steps of ≤ 0.25 dB (values from – ∞ dB to 12 dB are programmable but the transmission characteristics are only guaranteed in a specific range, see **table 10** and **11**). Two bytes are necessary to set GX to the desired value. After reset, the GX-gain stage is bypassed.
The transmit path contains a programmable high performance frequency response correction filter FX allowing an optimum adaptation to different types of microphones (dynamic, piezoelectric or electret). Twelve bytes are necessary to set FX to the desired frequency correction function. After reset, the FX-frequency correction filter is bypassed. **Figure 59** shows the architecture of the FX/FR-filter.

A high-pass filter (HPX) is also provided to remove unwanted DC components.

In the voice data manipulation block a data format selection (A-law, µ-law, 8-bit linear, 16 bit linear), the masking of the 8-bit data and the data source selection for the two data channels at the interface to the IOM handler is realized.

4.2.2 Receive Signal Processing

The incoming data from the IOM handler is similar to transmit direction processed by the VDM block. A programmable sidetone gain stage GZ adds a sidetone signal to the incoming voice signal. The sidetone gain can be programmed from – 54 to 0 dB within a ± 1 dB tolerance range (values from – ∞ dB to 12 dB are programmable but the transmission characteristics are only guaranteed in a specific range, see **table 10** and **11**). Respectively two bytes are coded in the CRAM to set GZ to the desired value. After reset, the GZ-gain stage is disabled (– ∞ dB).

A high-pass filter (HPR) is also provided to remove disturbances from 0 to 50/60 Hz due to the telecommunication network.

The frequency response correction filter (FR) is similar to the FX-filter allowing an optimum adaptation to different types of loudspeakers or ear pieces. Twelve bytes are necessary to set FR to the desired frequency correction function. After reset, the FR-frequency correction filter is bypassed.

The GR-gain adjustment stage is digitally programmable from – 6 to 0 dB in steps ≤ 0.25 dB (– ∞ dB and others are also possible). Respectively two bytes are coded in the CRAM to set GR to the desired value. After reset, the GR-gain stage is bypassed.

A low-pass filter limits the signal bandwidth in the receive direction according to ITU-T and ETSI (NET33) recommendations.

A series of low-pass interpolation filters increases the sampling frequency up to the desired value. The last interpolator feeds the D/A-converter.

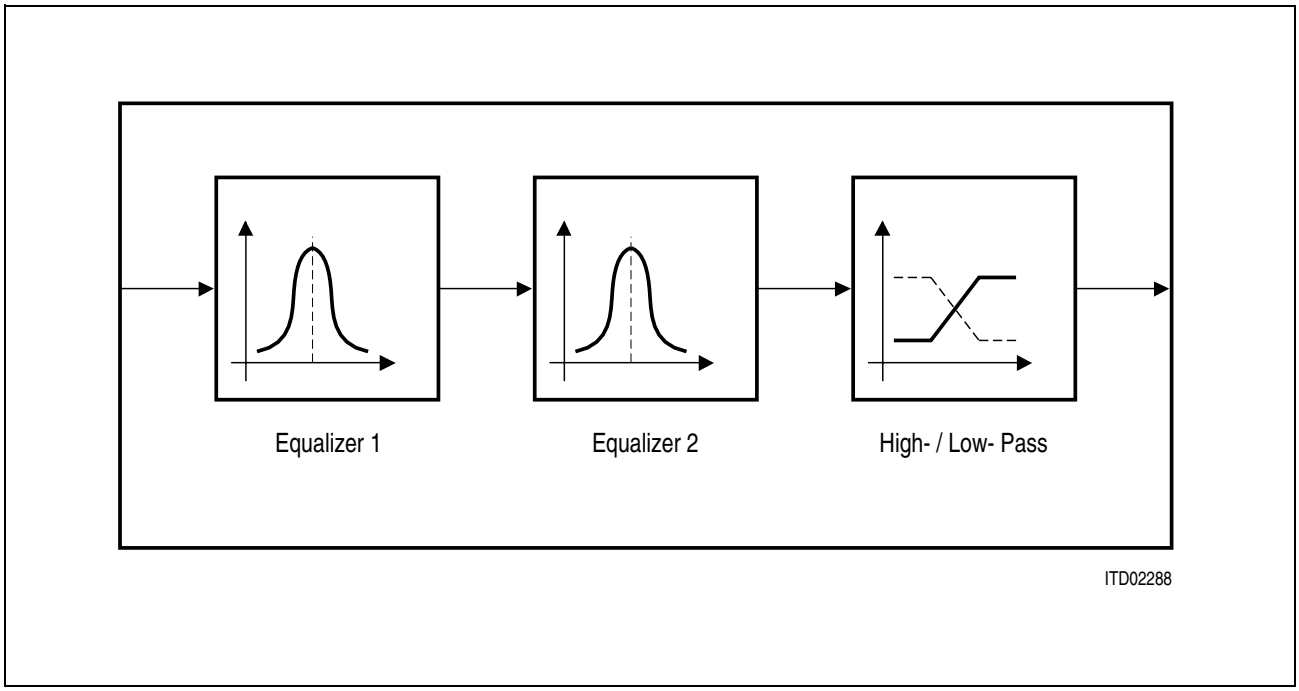


Figure 59
Architecture of the FX- and FR-Correction Filter

4.2.3 Programmable Coefficients for Transmit and Receive

This section gives a short overview of important programmable coefficients. For more detailed information a coefficient software package is available (SCOUT MASTER SIPO 21383).

Table 10 Description of the programmable Level Adjustment Parameters

Parameter	# of CRAM Bytes	Range	Comment
GX	2	12 to −∞ dB **6 to 0 dB**	Transmit gain adjustment Transmission characteristics guaranteed
GR	2	12 to −∞ dB **0 to -6 dB**	Receive gain adjustment Transmission characteristics guaranteed
GZ	2	12 to −∞ dB	Sidetone gain adjustment

Table 11 Subset of Coefficients for GX, GR and GZ:

Gain [dB]	MSB	LSB	Gain [dB]	MSB	LSB	Gain [dB]	MSB	LSB
12.0	10_H	01_H	0	$A0_H$	01_H	-12.0	$A9_H$	01_H
11.0	10_H	31_H	-0.5	$B3_H$	42_H	-13.0	$9C_H$	51_H
10.0	10_H	13_H	-1.0	$A3_H$	$2B_H$	-14.0	99_H	13_H
9.0	01_H	$4B_H$	-1.5	$A2_H$	32_H	-15.0	$8C_H$	$1B_H$
8.0	20_H	94_H	-2.0	BB_H	$4A_H$	-16.0	82_H	$7B_H$
7.0	30_H	94_H	-2.5	BB_H	13_H	-17.0	84_H	$4B_H$
6.0	13_H	51_H	-3.0	BA_H	29_H	-18.0	89_H	$6A_H$
5.5	$B0_H$	39_H	-3.5	BA_H	$5B_H$	-19.0	$8B_H$	$0C_H$
5.0	$A0_H$	49_H	-4.0	$A2_H$	01_H	-20.0	84_H	$1C_H$
4.5	23_H	01_H	-4.5	AA_H	$1B_H$	-21.0	$8C_H$	$1C_H$
4.0	22_H	$B4_H$	-5.0	$9B_H$	$3A_H$	-22.0	82_H	$7C_H$
3.5	23_H	12_H	-5.5	AA_H	33_H	-23.0	84_H	$4C_H$
3.0	32_H	$A4_H$	-6.0	AA_H	22_H	-24.0	89_H	$6B_H$
2.5	$B1_H$	BC_H	-7.0	$B9_H$	$2C_H$	-25.0	$8B_H$	$0D_H$
2.0	$B1_H$	03_H	-8.0	$9A_H$	BC_H	-26.0	84_H	$1D_H$
1.5	33_H	39_H	-9.0	$9B_H$	13_H	−∞	88_H	01_H
1.0	$B2_H$	$5A_H$	-10.0	$9B_H$	32_H			
0.5	$B3_H$	49_H	-11.0	93_H	02_H			

4.3 Tone Generation

The ASP contains a universal tone generator which can be used for tone alerting, call progress tones, DTMF-signals or other audible feedback tones.
All the tone generation configurations are programmable in the registers TGCR (Tone Generator Configuration Register) and TGSR (Tone Generator Switch Register) and the CRAM parameters.
The tone generation unit consists of following main blocks:

- Four Signal Generators
- Sequence Generator
- Control Generator
- Tone Filter
- Tone Level Adjustment

Figure Chapter • shows the signal flow graph of the tone generation unit and illustrates the following functional description.

4.3.1 Four Signal Generators

The four signal generators can be programmed by CRAM parameters in frequency (Fn,FD) and gain (Gn,GDn). For the signal generators F1,F2,F3 a trapezoid or square waveform can be selected by setting the TGCR.SQTR bit. The signal generator FD has a trapezoid waveform.
The signal generators in conjunction with the tone sequence generator and the control generator allow to generate different multitone patterns without reprogramming the necessary parameters.

4.3.2 Sequence Generator

The sequence generator can be enabled or disabled by setting the TGCR.SEQ (Sequence Generator) bit. If the sequence generator is enabled depending on the TGCR.TM (Tone Mode) bit two or three tone sequences of the signals (F1, G1), (F2,G2) and (F3,G3) are generated. The CRAM parameters T1, T2, T3 determine the duration of these individual signals.
If the sequence generator is disabled a continuous tone is generated. The selected signal generator depends on the TGCR.TM (Tone Mode) bit.
By setting the TGSR.DT (Dual Tone Mode) bit the output of the signal generator FD (FD, GDn) can be added to the tone signal which is determined by the SEQ and TM bit.

Note: The dual tone mode and the three tone sequence can only be used if the DTMF mode is disabled (TGSR.DTMF = ’0’)

Table 12 shows the programmable CRAM Parameters of the tone and sequence generator.
In **Table 13** possible tone signals are listed which can be realized with the control bits SEQ, TM and DT.

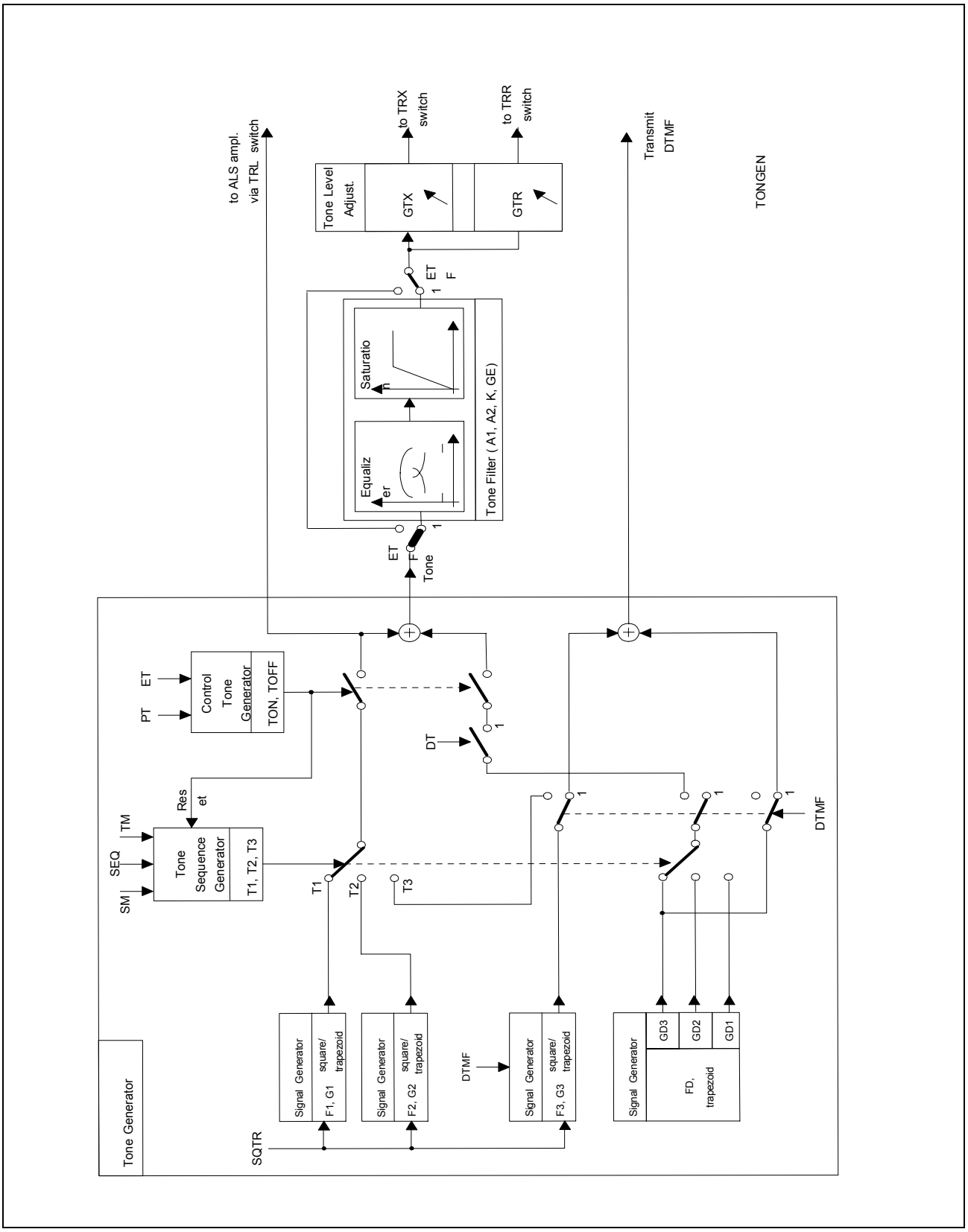


Figure 60
Signal Flow Graph of the Tone Generation Unit

Table 12 CRAM Parameters of the Signal and Sequence Generator

Parameter	# of CRAM Bytes	Range	Comment
Fn	2/2/2	50 Hz to 4 kHz	Trapezoid shaped tone
		16 kHz/m; (m ≥ 3)	Square-wave signal
Gn	1/1/1	0 dB to – 48 dB	Gain adjustment for square/trapezoid generator
Tn	2/2/2	10 ms to 8 s	Period of time for two- or three-tone sequences
FD	2	50 Hz to 4 kHz	Trapezoid shaped tone
GDn	1/1/1	0 dB to – 48 dB	Gain adjustment for trapezoid generator

n is either 1, 2 or 3

Note: 0-dB gain setting of G1, G2 or G3 and GD1, GD2 or GD3 corresponds to the maximum PCM-level (A-Law: + 3.14 dBm0)

Table 13 Tone Generation

SEQ	TM	DT	Generated tone	
0	0	0	Continuous signal	[F1, G1]
0	0	1	Continuous signal	[F1, G1] + [FD, GD1]
0	1	0	Continuous signal	[F2, G2]
0	1	1	Continuous signal	[F2, G2] + [FD, GD2]
1	0	0	tone sequence	[F1, G1, T1] / [F2, G2, T2]
1	0	1	tone sequence	[(F1, G1) + (FD, GD1), T1)] / [(F2, G2) + (FD, GD2), T2)]
1	1	0	tone sequence	(F1, G1, T1) / (F2, G2, T2) / (F3, G3, T3)
1	1	1	tone sequence	[(F1, G1) + (FD, GD1), T1] / [(F2, G2) + (FD, GD2), T2] / [(F3, G3) + (FD, GD3), T3]

4.3.3 Control Generator

Controlling of the generated tone follows the setting of the control bits ET (Enable Tone) and PT (Pulsed Tone) and the CRAM parameters TON and TOFF corresponding **table 14** and **table 15**.

Table 14 Control Generator

ET	PT	Generator Output
0	0	No tone
1	0	continuous tone generation without breaks
1	1	the tone is pulsed with the programmable parameters TON, TOFF

Table 15 CRAM Parameters of the Control Generator

Parameter	# of CRAM Bytes	Range	Comment
TON	2	20 ms to 16 min	Period while the tone generator is turned on
TOFF	2	20 ms to 16 min	Period while the tone generator is turned off

Four typical examples for the control generator programming are shown in **Figure 61**.
In the automatic stop mode (TGCR.SM = ’1’) the selected tone sequence is only stopped after a sequence is completed. This avoids unpleasant sounds when stopping the tone generator.
The tone signal can be fed directly to the input of the loudspeaker amplifier by setting the TGSR.TRL bit to ’1’. In this mode only a square wave (fixed amplitude of VDD) is available from the signal generators (F1, F2, F3)and the TGCR.SQTR bit has no effect.

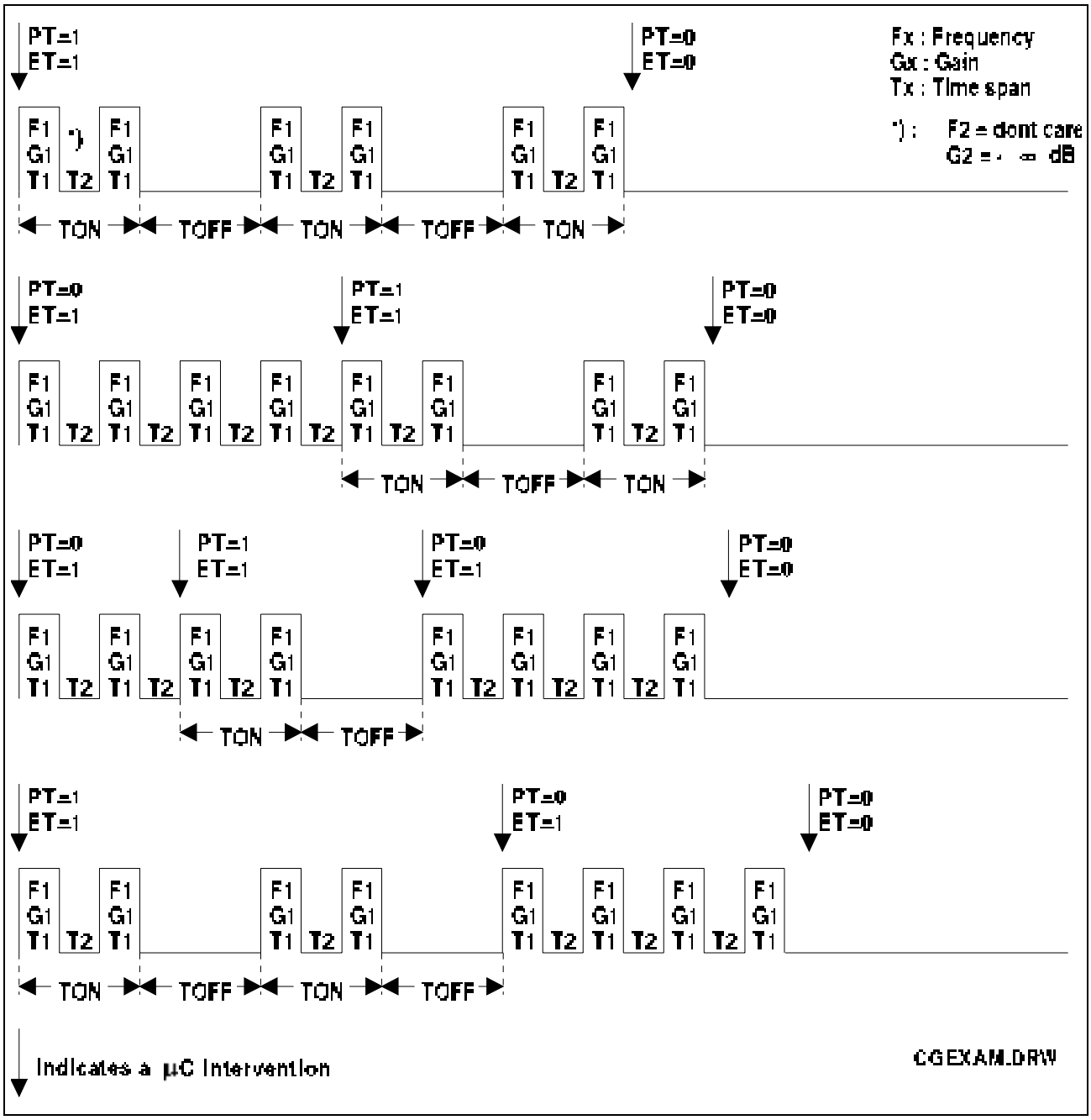


Figure 61
Typical Control Generator Applications

4.3.4 Tone Filter

A programmable tone filter can be switched in the tone signal path by setting the ETF (Enable Tone Filter) bit. The tone filter contains a programmable equalizer and a saturation amplifier (see **figure Chapter •**).
A generated square-wave or trapezoid signal can be converted by the equalizer into a sine-wave signal. The equalizer is realized as a band-pass filter. The filter parameters

(center frequency, bandwidth and attenuation of the stop-band) are programmable by the CRAM parameters listed in **Table Chapter 16**

Table 16 CRAM Parameters of the Tone Filter

Parameter	# of CRAM Bytes	Range	Comment
A1	1	200 Hz to 4 kHz	Center frequency
A2	1	0 to – 1	Determines with A1 and K the bandwidth. The closer A2 comes to -1, the smaller the bandwidth.
K	1	0 to 54 dB	Attenuation of the stop-band
GE	1	+ 12 to – 12 dB	Saturation amplification

A maximum attenuation of the first harmonic frequency of 50 dB is possible. **Figure Chapter 62** shall illustrate the equalizer parameters.

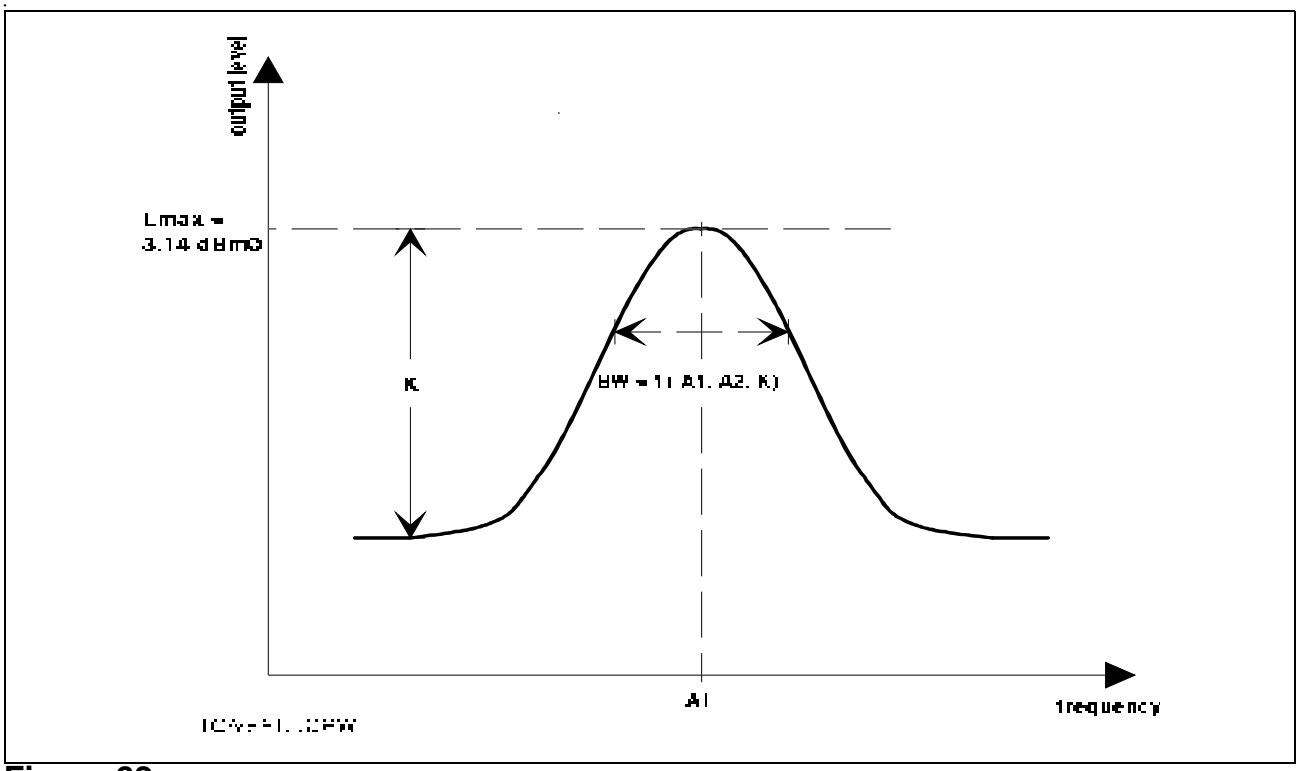


Figure 62
Filter Parameters of the Equalizer

The two main purposes of the programmable saturation amplification are:

- Level balancing of the filtered signal (avoidance of overload effects).
- Amplification up to + 12 dB followed by a saturation (3.14 dBm0) of the incoming signal. This saturation amplification converts a sine-wave signal into a square-wave

or a trapezoid signal where their edges are eliminated. This method produces pleasant ringing tones.

4.3.5 Tone Level Adjustment

The generated tone signal can be amplified separate for transmit and receive direction with the gain parameters GTX, GTR and switched to the transmit/receive channels by setting TGSR.TRX (Tone Ringing Transmit) and TRR (Tone Ringing Receive).

Table 17 CRAM Parameters of the Tone Level Adjustment

Parameter	# of CRAM Bytes	Range	Comment
GTX	1	0 dB to – 50 dB (also – ∞ dB)	Level adjustment in transmit direction
GTR	1	0 dB to – 50 dB (also – ∞ dB)	Level adjustment in receive direction

4.3.6 DTMF Mode

The DTMF mode of the tone generator is selected by setting the TGSR.DTMF to'1'. The trapezoid output signal of the signal generators (F3, G3) and (FD, GD3) are added and fed in the transmit path. The CRAM parameters for the DTMF signals are listed in **table 18**

In the DTMF mode a special DTMF filter is switched to the transmit channel. Undesirable frequency components are filtered by this special DTMF-low-pass filter to the following limits:

Frequency Band	Min. Attenuation
0 – 300 Hz	33 dB
300 – 3400 Hz	20 dB
3400 – 4000 Hz	33 dB

The pre-emphasis of 2 dB between the high and the low DTMF-frequency groups has to be set with the independent gain parameters (G3 and GD3 resp.) of the trapezoid generators. All generated DTMF-frequencies are guaranteed within a ± 1 % deviation.

Table 18 DTMF-frequency (F3,FD) Programming

ITU-T Q.23	SCOUT-DX	Relative Deviation	Coefficients	
[Hz]	Nominal [Hz]	from ITU-T	high [HEX]	low [HEX]
Low Group				
697	697.1	+ 143 ppm	4F	16
770	770.3	+ 390 ppm	A6	18
852	852.2	+ 235 ppm	45	1B
941	941.4	+ 425 ppm	20	1E
High Group				
1209	1209.5	+ 414 ppm	B4	26
1336	1336.9	+ 674 ppm	C8	2A
1477	1477.7	+ 474 ppm	49	2F
1633	1632.8	– 122 ppm	40	34

Note: The deviations due to the inaccuracy of the incoming clock DCL/MCLK, when added to the nominal deviations tabulated above give the total absolute deviation from the CCITT-recommended frequencies

4.4 Speakerphone Support

The speakerphone option of the SCOUT-DX performs all functions required for echo suppression without any external components, just by software. All these operational functions realized by the signal processor are completely parameterized. This technique offers a high level of flexibility and reproducibility.

Basically, three static mode of operation can be distinguished: “transmit mode”, “receive mode”, and “idle mode”. In the speech mode the receive path is attenuated while in listen mode the attenuation is switched to the transmit path. In the idle mode the attenuation is halved between transmit and receive paths. The amount of switchable attenuation can be chosen by software. The speakerphone goes into transmit mode if both, the speech detector and the speech comparator SCAE, indicate the presence of a speech signal in the transmit direction that is strong enough. Switching into receive mode appears if the speech comparator SCLE and the speech detector in the receive path both detect a speech signal that is strong enough. If no speech is detected at all, the speakerphone goes into idle mode.

As the signal flow graph of the speakerphone option shows (see **figure Chapter 63**), the complete operational algorithm is situated between the analog front end/signal processing and the compression/expansion logic. Thus telephone sets can be optimized and adjusted to the particular physical and acoustic environment.

The main features of the speakerphone signal processing are:

- Two separate attenuation stages activated by voice, one for the transmit and one for the receive path. They are controlled by the current and past speech activities.
- Immediate mode switching mainly controlled by two comparators, one at the acoustic side and one at the line side. Capable of handling very long echo times.
- All parameters can be adjusted independently and are closely related to the physical phenomenons.
- Speech detection by special speech detectors in the respective transmit and receive directions. Different time constants are separately programmable for signal and noise.
- Background noise monitoring to eliminate continuous background noise from speech control. All time constants are user programmable.

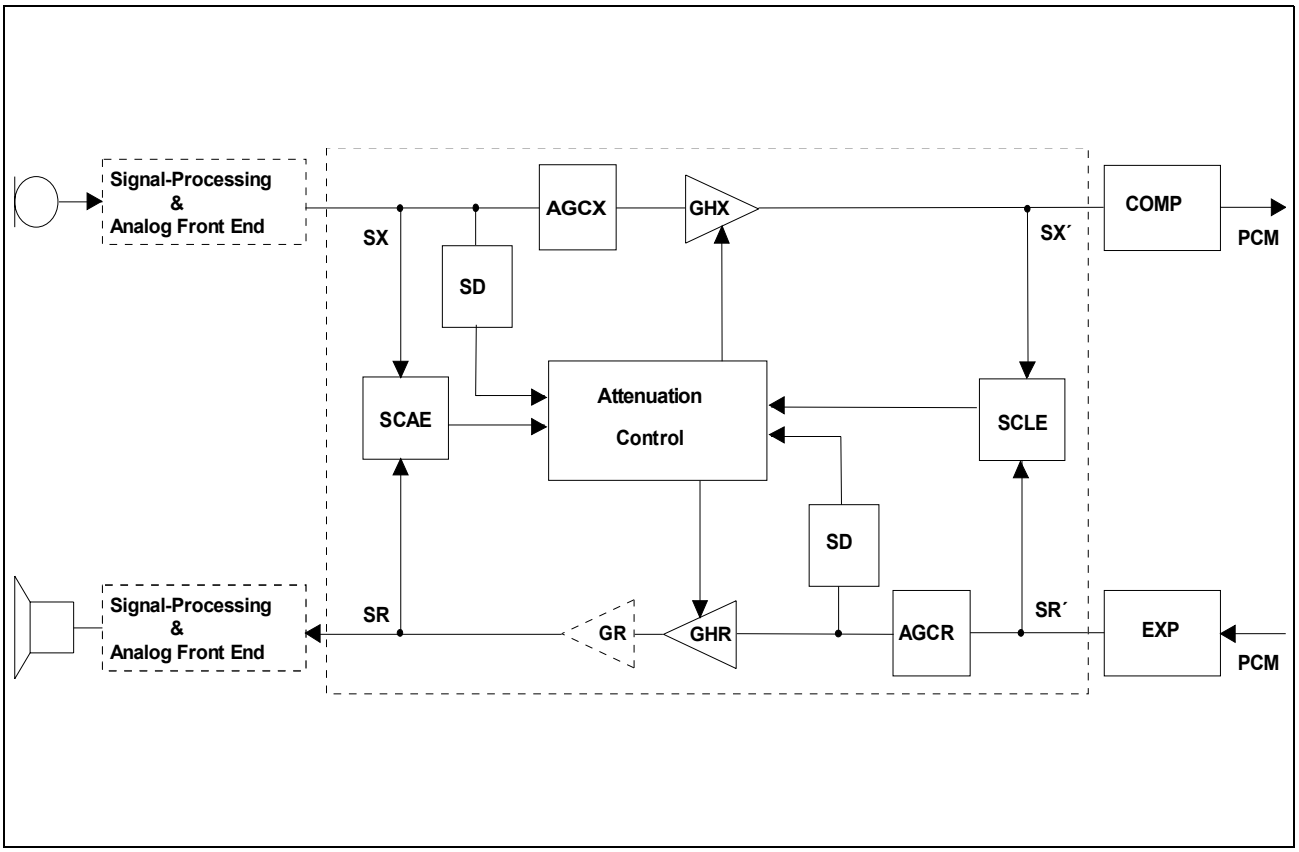


Figure 63
Speakerphone Signal Flow Graph of the SCOUT-DX

4.4.1 Attenuation Control Unit

The Attenuation Control unit controls the attenuation stages GHX of the transmit and GHR of the receive directions respectively. The programmable loss is switched either completely to a single path or, in the “IDLE” mode, is halved to each direction.

In addition, attenuation is also influenced by the Automatic Gain Control stages (AGCX and AGCR). In order to keep the total loop gain always constant, the sweep range (of ATT) is automatically enlarged with high-gain amplification of the AGCs while it will be accordingly reduced with low-gain.

Changing from one speakerphone mode into another one depends on the determinations of one comparator plus the corresponding speech detector. Hence attenuation is influenced by the current and past speech activities. Also rate of change varies: changing from “transmit mode” or “receive mode” to “idle mode” is programmable by the rate factor DS. Direct changes from “transmit mode” to “receive mode” or vice-versa and changes from “idle mode” to “transmit mode” or “receive mode” can be programmed via the factor SW in a large range.

Description of the programmable parameters:

Parameter	# of CRAM Bytes	Range	Comment
TW	1	16 ms to 4 s	Wait time
ATT	1	0 dB to 95 dB	Attenuation programmed in GHR or GHX if speech activity for the other side was detected
DS	1	0.6 to 680 ms/dB	Decay Speed (Decay Time TD = DS × ATT/2)
SW	1	0.0052 to 10 ms/dB	Switching time (dependent on ATT)

4.4.2 Speakerphone Test Function and Self Adaption

For optimizing the speakerphone performance the SCOUT-DX provides following test functions:
- The two register bits (XCSR.SPST) indicate the different speakerphone states (receive, transmit and idle).
- The momentary magnitude of the AGC attenuation in receive direction can be read out by an SOP_D command.

4.4.3 Speech Detector

The speech detectors (see **figure Chapter 64**) contained in both transmit and receive directions consist of two main blocks:

- Background Noise Monitor (BNM)
- Signal Processing

Although the speech detector is fully parameterized, the standard coefficient set for the speech detector fits perfectly to almost every application and normally don’t have to be altered.

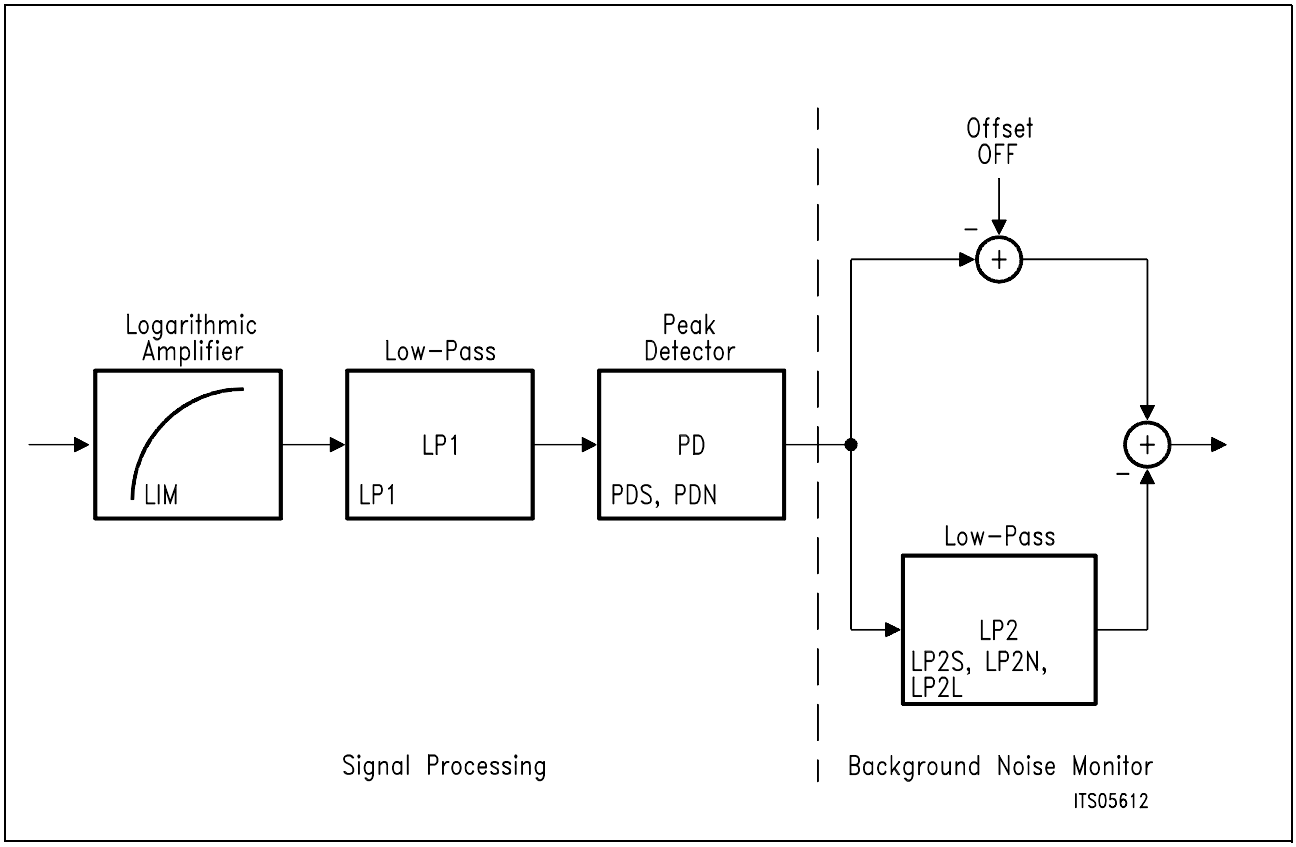


Figure 64
Speech Detector Signal Flow Graph

4.4.3.1 Background Noise Monitor

The tasks of the noise monitor are to differentiate voice signals from background noise, even if it exceeds the voice level, and to recognize voice signals without any delay. Therefore the background noise monitor consists of the low-pass filter 2 (LP2) and the offset in two separate branches. Basically it works on the burst-characteristic of the speech: voice signals consist of short peaks with high power (bursts). In contrast, background noise can be regarded approximately stationary from its average power.

Low-pass filter 2 provides different time constants for noise (non-detected speech) and speech. It determines the average of the noise reference level. In case of background noise the level at the output of LP2 is approximately the level of the input. Due to the offset OFF the comparator remains in the initial state. In case of speech at the comparator input the difference between the signal levels of the offset branch and of the LP2-branch increases and the comparator changes state. At speech bursts the digital signals arriving at the comparator via the offset branch change faster than those via the LP2-branch so that the comparator changes its polarity. Hence two logical levels are generated: one for speech and one for noise.

A small fade constant (LP2N) enables fast settling down the LP2 to the average noise level after the end of speech recognition. However, a too small time constant for LP2N can cause rapid charging to such a high level that after recognizing speech the danger of an unwanted switching back to noise exists. It is recommended to choose a large rising constant (LP2S) so that speech itself charges the LP2 very slowly. Generally, it is not recommended to choose an infinite LP2S because then approaching the noise level is disabled. During continuous speech or tones the LP2 will be charged until the limitation LP2L is reached. Then the value of LP2 is frozen until a break discharges the LP2. This limitation LP2L of this charging especially on the RX-path permits transmission of continuous tones and “music on hold”.

The offset stage represents the exact level threshold in [dB] between the speech signal and averaged noise.

4.4.3.2 Signal Processing

As described in the preceding chapter, the background noise monitor is able to discriminate between speech and noise. In very short speech pauses e.g. between two words, however, it changes immediately to non-speech, which is equal to noise. Therefore a peak detection is required in front of the Noise Monitor.

The main task of the Peak Detector is to bridge the very short speech pauses during a monologue so that this time constant has to be long. Furthermore, the speech bursts are stored so that a sure speech detection is guaranteed. But if no speech is recognized the noise low-pass LP2 must be charged rapidly to the average noise level.

Additionally the noise edges are to be smoothed. Therefore two time constants are necessary and are separately programmable: PDS for speech and PDN for space (background noise) signals.

The Peak Detector is very sensitive to spikes. The LP1 filters the incoming signal containing noise in a way that main spikes are eliminated. Due to the programmable time constant it is possible to refuse high-energy sibilants and noise edges.

To compress the speech signals in their amplitudes and to ease the detection of speech, the signals have to be companded logarithmically. Hereby, the speech detector should not be influenced by the system noise which is always present but should discriminate between speech and background noise. The limitation of the logarithmic amplifier can be programmed via the parameter LIM, where the upper half-byte features LIMX and the lower half-byte LIMR. LIM is related to the maximum PCM level (+3.14 dBm0). A signal exceeding the limitation defined by LIM is getting amplified logarithmically, while very smooth system noise below is neglected. It should be the level of the minimum system noise which is always existing; in the transmit path the noise generated by the telephone circuitry itself and in receive direction the level of the first bit which is stable without any speech signal at the receive path.

Description of the programmable speech detector parameters:

Parameter	# of CRAM Bytes	Range	Comment
LP1	1	1 to 512 ms	Time constant LP1
OFF	1	0 to 50 dB	Level offset up to detected noise
PDS	1	1 to 512 ms	Time constant PD (signal)
PDN	1	1 to 512 ms	Time constant PD (noise)
LP2S	1	4 to 2000 ms	Time constant LP2 (signal)
LP2N	1	1 to 512 ms	Time constant LP2 (noise)
LP2L	1	0 to 95 dB	Limitation of LP2, related to LIM
LIMX, LIMR	1	– 36 to – 78 dB	Limitation of logarithmic amplifier

4.4.4 Speech Comparators (SC)

Switching from one active mode to another one is controlled by the speech comparators, provided the speech detectors are indicating speech. There are two speech comparators, one at the acoustic (AE) and one at the line side (LE). These comparators continuously compare the signal levels of both signal paths and control the effect of the echoes at the acoustic side and the line side. Once speech activity has been detected, the comparator switches at once in that direction in which the speech signal is stronger. For this purpose each signal is compared to the sum of the other and the returned echo.

4.4.4.1 Speech Comparator at the Acoustic Side (SCAE)

In principle, the SCAE works according to the following equation:

if SX > SR + VAE then TX
else RX

Being in RX-mode, the speech comparator at the acoustic side controls the switching to TX-mode. Only if the SX-signal is higher than the SR-signal plus the expected/measured acoustic level enhancement (VAE), the comparator switches immediately to TX-mode. Physically the level enhancement (VAE) is divided into two parts: GAE and GDAE.

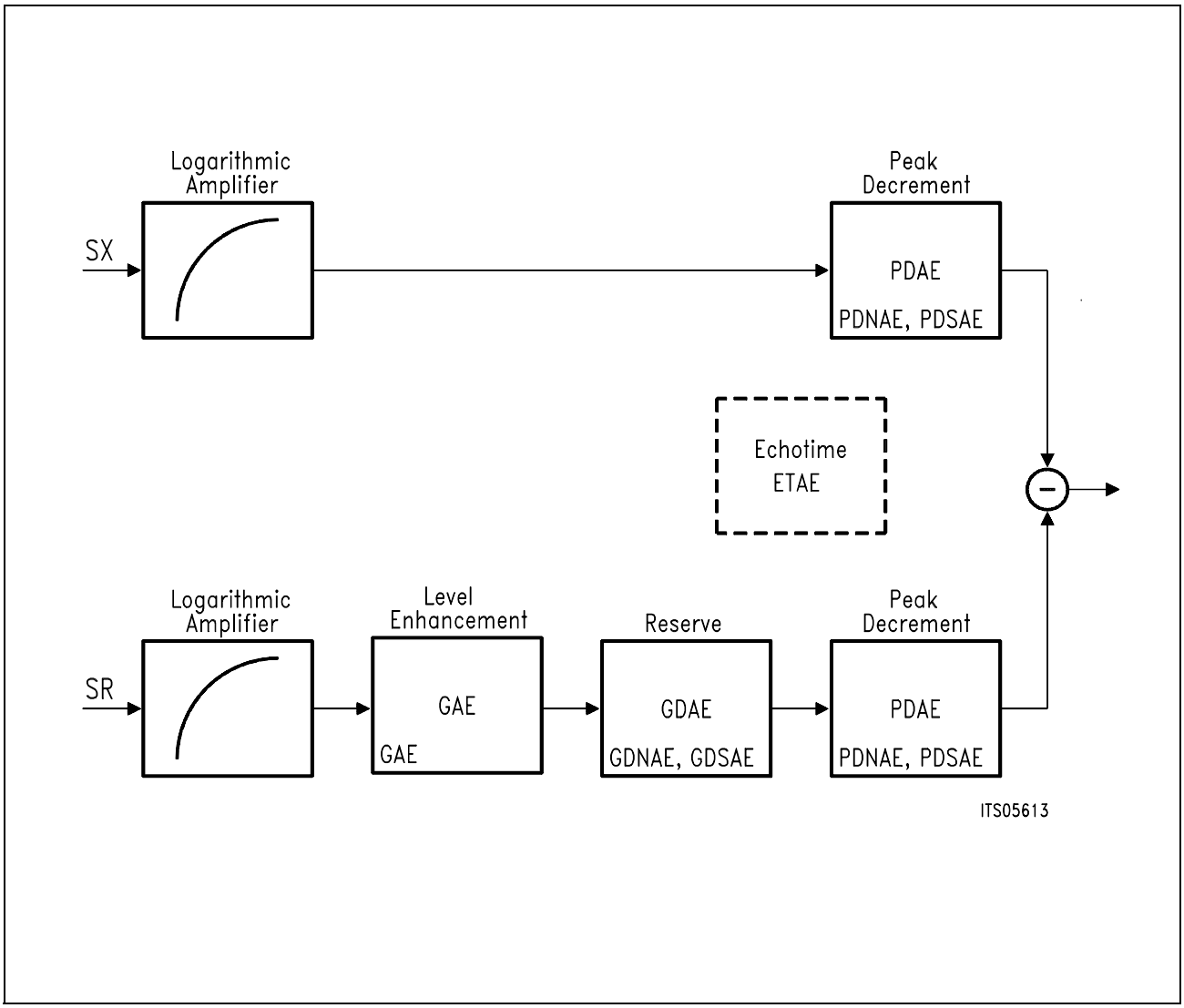


Figure 65
Speech Comparator at the Acoustic Side

At the SCAE-input, logarithmic amplifiers compress the signal range. Hence after the required signal processing for controlling the acoustic echo, pure logarithmic levels on both paths are compared.

Principally, the main task of the comparator is to control the echo. The internal coupling due to the direct sound and mechanical resonances are covered by GAE. The external coupling, mainly caused by the acoustic feedback, is controlled by GDAE/PDAE.

The Gain of the Acoustic Echo (GAE) corresponds to the terminal couplings of the complete telephone: GAE is the measured or calculated level enhancement between both receive and transmit inputs of the SCAE (see **figure Chapter 63**). It equals the sum of the amplification of ALS plus the gain due to the loudspeaker/microphone coupling plus the TX-amplification of AMIC1 and GX1. To succeed in a sure differentiation between original speech and echo, it must be guaranteed that the TX-signal does not run into saturation due to the loudspeaker/microphone coupling. Therefore, it is recommended to reduce the TX-gain by 10 dB in front of the SCAE at least in the loudest loudspeaker volume step. To fulfill the sending loudness rating, this gain is realized by the LGAX/AGCX which follows the SCAE. Of course, the GAE has to be reduced by the same amount.

To control the acoustic feedback two parameters are necessary: GDAE-features the actual reserve on the measured GAE. Together with the Peak Decrement (PDAE) it simulates the echo behavior at the acoustic side: After RX-speech has ended there is a short time during which hard couplings through the mechanics and resonances and the direct echo are present. Till the end of that time (Δt) the level enhancement VAE must be at least equal to GAE to prevent clipping caused by these internal couplings. Then, only the acoustic feedback is present. This coupling, however, is reduced by air attenuation. For this in general the longer the delay, the smaller the echo being valid. This echo behavior is featured by the decrement PDAE.

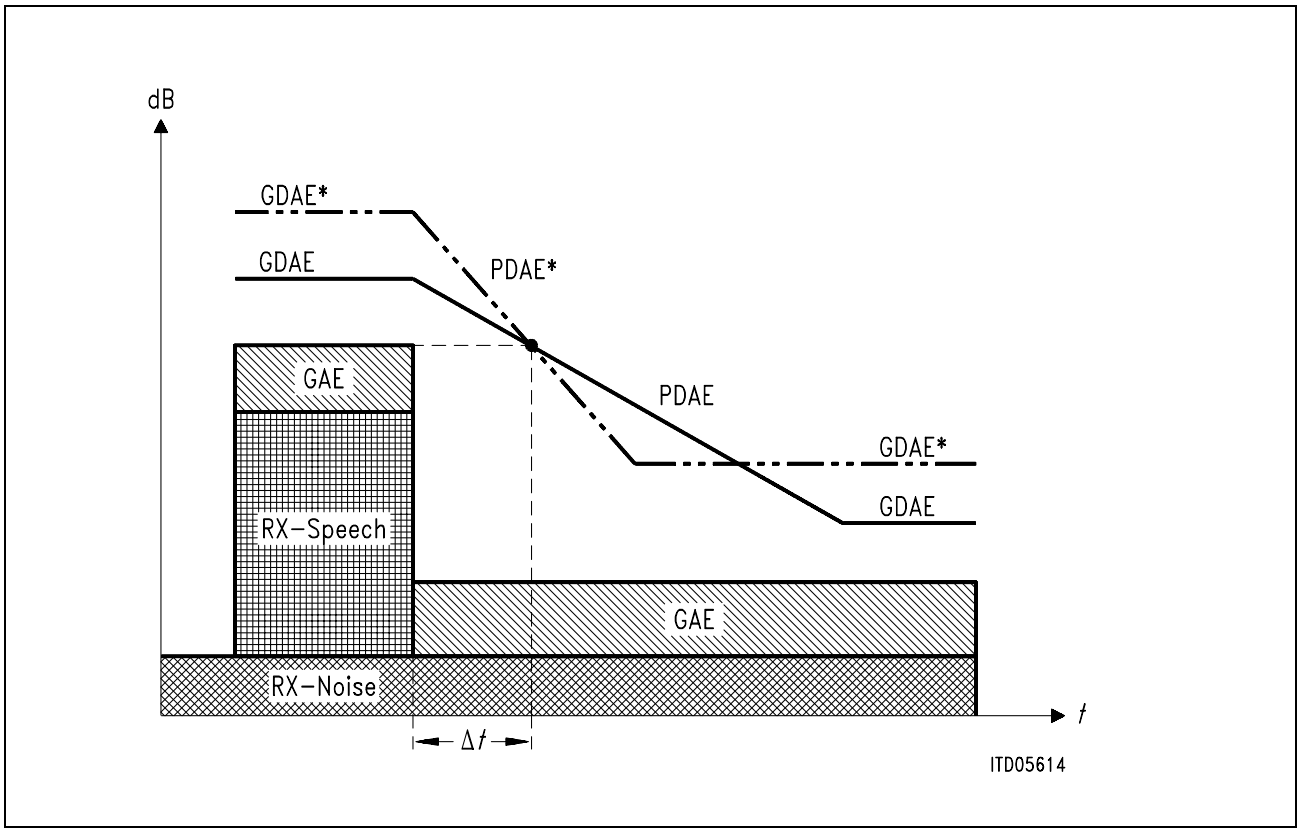


Figure 66
Interdependence of GDAE and PDAE

According to **figure 66**, a compromise between the reserve GDAE and the decrement PDAE has to be made: a smaller reserve (GDAE) above the level enhancement GAE requires a longer time to decrease (PDAE). It is easy to overshout the other side but the intercommunication is harder because after the end of the speech, the level of the estimated echo has to be exceeded. On the contrary, with a higher reserve (GDAE*) it is harder to overshout continuous speech or tones, but it enables a faster intercommunication because of a stronger decrement (PDAE*).

Two pairs of coefficients, GDSAE/PDSAE when speech is detected, and GDNAE/PDNAE in case of noise, offer a different echo handling for speech and non-speech.

With speech, even if very strong resonances are present, the performance will not be worsened by the high GDSAE needed. Only when speech is detected, a high reserve prevents clipping. A time period ETAE [ms] after speech end, the parameters of the comparator are switched to the “noise” values. If both sets of the parameters are equal, ETAE has no function.

Description of the programmable parameters:

Parameter	# of CRAM Bytes	Range	Comment
GAE	1	– 48 to + 48 dB	Gain of Acoustic Echo
GDSAE	1	0 to 48 dB	Reserve when speech is detected
PDSAE	1	0.16 to 42 ms/dB	Peak Decrement when speech is detected
GDNAE	1	0 to 48 dB	Reserve when noise is detected
PDNAE	1	0.16 to 42 ms/dB	Peak Decrement when noise is detected
ETAE	1	0 to 1020 ms	Echo time

4.4.4.2 Speech Comparator at the Line Side (SCLE)

Principally, the SCLE works similarly to the SCAE. The formula of SCLE is the following:

if SR > SX + VLE then RX
else TX

Being in TX-mode, the speech comparator at the line side controls the switching to RX-mode. When the SR-signal is higher than the SX-signal plus the expected/measured echo return loss (VLE) and if SDR has detected speech, the comparator switches immediately to RX-mode.

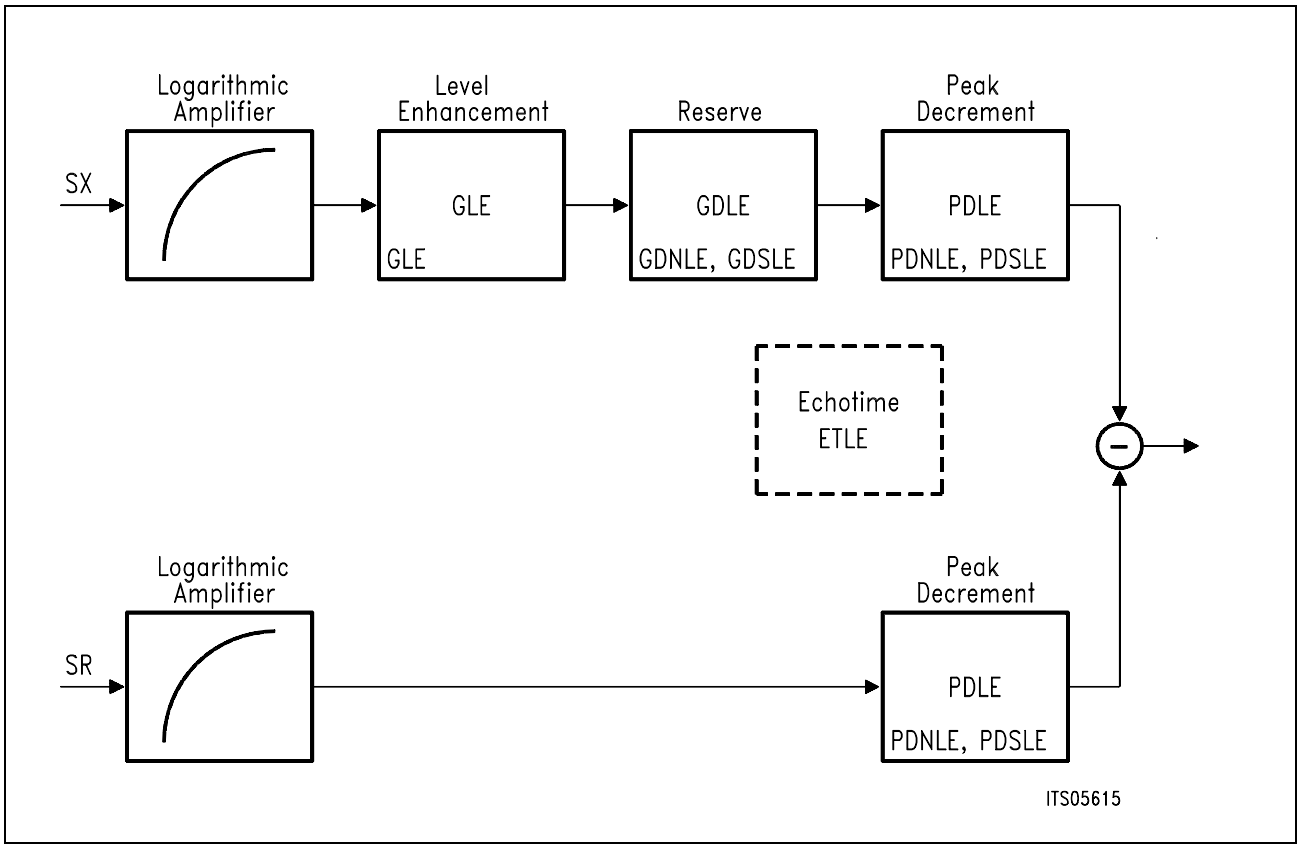


Figure 67
Speech Comparator at the Line Side

The Gain of the Line Echo (GLE) directly corresponds to the echo return loss of the link. Generally, it is specified to 27 dB. However, the worst case loss can be estimated to 10 dB. This means, the echo returns at least attenuated by 10 dB.

Similarly to the acoustic side, GDLE at the line side features the reserve above GLE which is necessary to control the echo via the decrement PDLE. GDLE and PDLE are interdependent. Exactly Δt [ms] after the end of RX-speech the level enhancement VLE must be at least GLE to prevent clipping.

Two pairs of coefficients are available: GDSLE/PDSLE while speech is detected and GDNLE/PDNLE in case of noise. This offers the possibility to control separately the far-end echo during speech and the near-end echo while noise is detected. However, this requires an attenuation between the speech detectors SDX and SDR: If the SDX does not recognize any speech, the SDR must not detect speech due to the far-end echo. Note, that LIMX and LIMR are also influencing the sensitivity of the speech detection. ETLE [ms] after the final speech detection the parameter sets are switched. If both sets are equal, ETLE has no meaning.

Description of the programmable parameters:

Parameter	# of CRAM Bytes	Range	Comment
GLE	1	– 48 to + 48 dB	Gain of Line Echo
GDSLE	1	0 to 48 dB	Reserve when speech is detected
PDSLE	1	0.16 to 42 ms/dB	Peak Decrement when speech is detected
GDNLE	1	0 to 48 dB	Reserve when noise is detected
PDNLE	1	0.16 to 42 ms/dB	Peak Decrement when noise is detected
ETLE	1	0 to 1020 ms	Echo time

4.4.4.3 Automatic Gain Control of the Transmit Direction (AGCX)

Optionally an AGCX is inserted into the transmit path (see **figure 68**) to reach nearly constant loudness ratings independent from the varying distance between the speaking person and the microphone. The AGCX works only together with the speakerphone function (GCR.SP=1).

Operation of the AGCX depends on a threshold level. The threshold is defined by the parameter COMX (value relative to the maximum PCM-value). Regulation follows two time constants: TMHX for signal amplitudes above the threshold and TMLX for amplitudes below. Usually TMHX will be chosen up to 10 times faster than TMLX. The bold line in **figure Chapter 69** depicts the steady-state output level of the AGCX as a function of the input level.

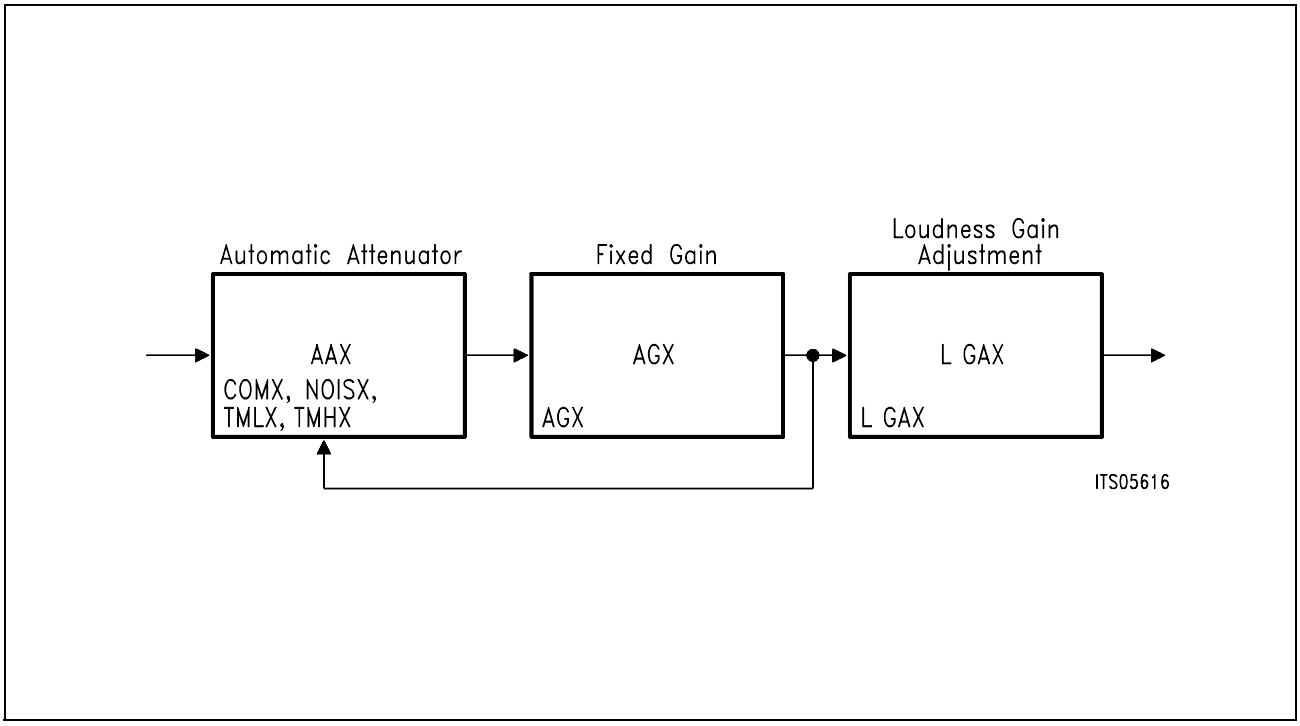


Figure 68
Block Diagram of the AGC in Transmit Direction

For reasons of physiological acceptance the AGCX gain is automatically reduced in case of continuous background noise e.g. by ventilators. The reduction is programmed via the NOISX-parameter. When the noise level increases the threshold determined by NOISX, the amplification will be reduced by the same amount the noise level is above the threshold.

A programmable Loudness Gain Adjustment stage (LGAX) offers the possibility to amplify the transmit signal after the speech detector SDX. If a lower signal range in front of the SDX is necessary to determine between speech and echo a part of the transmit signal amplification can be transferred to the LGAX. It is enabled with the bit GCR.SP.

Note: Even if the AGCX is disabled in speakerphone mode the LGAX remains enabled.

If the speakerphone is in receive mode, the AGCX is not working; instead the last gain setting is used and regulation starts with this value as soon as the speakerphone returns into transmit mode again. For transmission measurements with this transient behavior it is recommended not to use a continuous sine wave signals but some kind of synthetic speech (e.g. switched noise or Composite Source Signal CSS). The sweep range of the switchable attenuation ATT (see **chapter 4.4.1**) is affected by the AGCX.
If the automatic gain control enlarges the signal level, the sweep range will be increased accordingly in order to obtain a constant over-all gain in transmit and receive direction (constant TCL, constant echo return loss).

The initial gain (AGIX) is used immediately after enabling the AGCX to allow a fast settling time of the AGC.

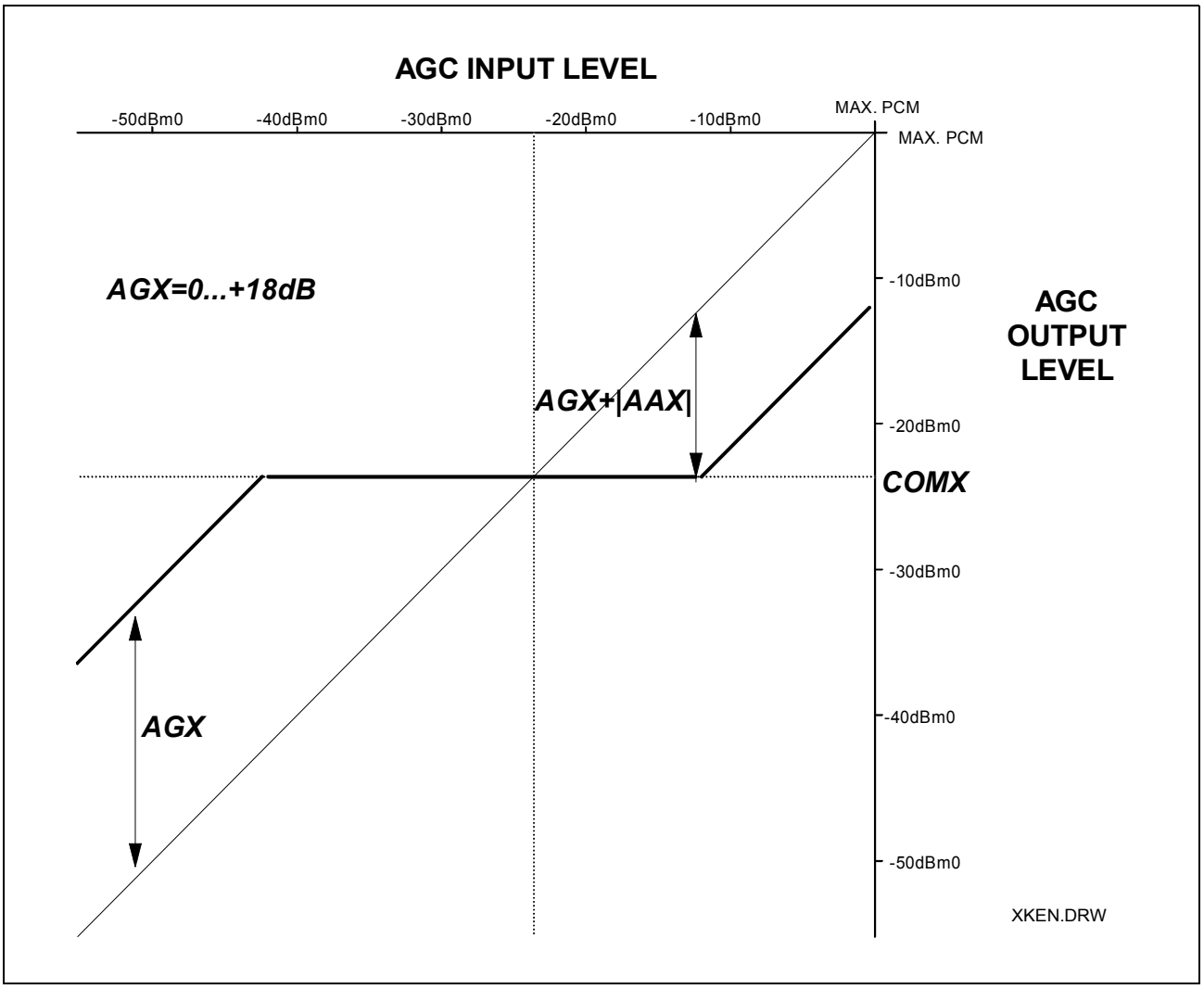


Figure 69
Level Diagram For the AGC in Transmit Direction

Description of the programmable parameters:

Parameter	# of CRAM Bytes	Range	Comment
LGAX	1	– 12 to 12 dB	Loudness Gain Adjustment
COMX	1	0 to – 73 dB	Compare level rel. to max. PCM-value
AAX	1	0 to 47 dB	Attenuation range of Automatic Control
AGX	1	0 to 18 dB	Gain range of Automatic control
AGIX	1	0 to 18 dB	Initial AGC gain transmit
TMLX	1	1 to 2700 ms/dB	Settling time constant for lower levels
TMHX	1	1 to 340 ms/dB	Settling time constant for higher levels
NOISX	1	0 to – 95 dB	Threshold for AGC-reduction by background noise

4.4.5 Automatic Gain Control of the Receive Direction (AGCR)

The Automatic Gain Control of the receive direction AGCR (see **figure Chapter 70**) is similar to the transmit AGC. One additional parameter (AAR) offers more flexibility since the AGCR is able to attenuate signals as well. Depending on the parameters AAR and AGR different behaviours of the AGCR are possible as **figure Chapter 71** illustrates. For example with AGR set to 0dB and AAR set to maximum (-48 dB) the AGCR acts as a limiter.

The AGCR is working only together with the speakerphone function (GCR.SP=1). The digital gain stage LGAR is always enabled in speakerphone mode, independent of the setting of GCR.AGCR.

It is highly recommended to program reasonable amplifications in the digital gain stages. Otherwise the ASP will run into saturation above the 3.14 dB PCM-value.

Note that the speech detector for the receive direction is supplied with the signal that comes out of the AGR-block unless XCR.PGCR = ’1’.

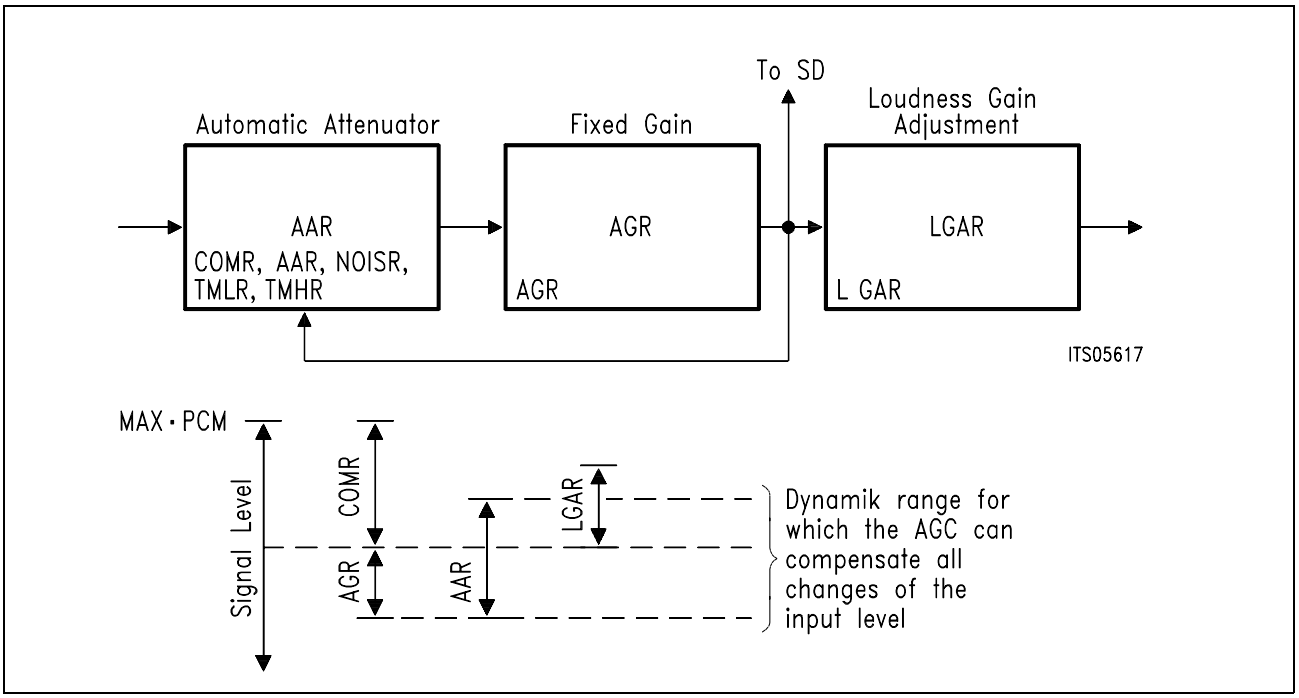


Figure 70
Function of the Receive AGC

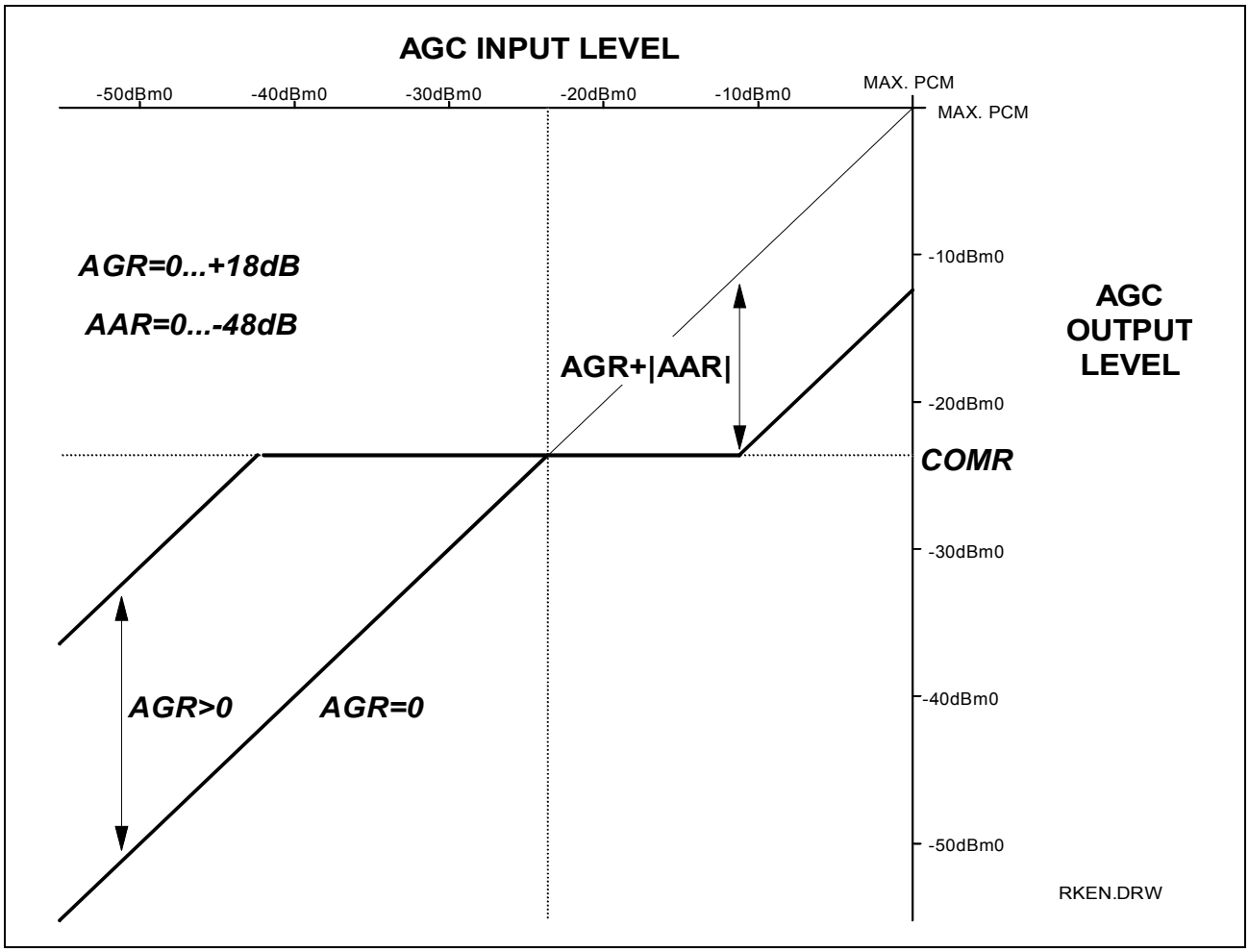


Figure 71
Level Diagram For the AGC in Receive Direction

If the speakerphone is in transmit mode, the AGCR is not working; instead the last gain setting is used and the regulation starts with this value when the speakerphone has gone back into receive mode again.
The initial attenuation (AGIR) is used immediately after enabling the AGCR to allow a fast settling time of the AGC.
The sweep range of the switchable attenuation ATT is affected by the AGCR. If the automatic gain control enlarges or reduces the signal level, the sweep range will be adjusted automatically in a way, that the over-all gain in transmit and receive direction remains constant (constant TCL, constant echo return loss).
Because of this the AGCR can be used for a comfortable receive volume control where the TCL value is the same for each volume setting and thus providing an optimal speakerphone performance. For such a volume control the momentary attenuation of the AGCR has to be read out by a SOP_D command. The parameters AGIR, COMR, can be determined for the desired volume change and written back in the CRAM.

Description of the programmable parameters:

Parameter	# of CRAM Bytes	Range	Comment
LGAR	1	– 12 to 12 dB	Loudspeaker Gain Adjustment
COMR	1	0 to – 73 dB	Compare level rel. to max. PCM-value
AAR	1	0 to – 47 dB	Attenuation range of Automatic control
AGIR	1	18 to – 47 dB	Initial AGC attenuation/ gain receive
AGR	1	0 to 18 dB	Gain range of Automatic control
TMLR	1	1 to 2700 ms/dB	Settling time constant for lower levels
TMHR	1	1 to 340 ms/dB	Settling time constant for higher levels
NOISR	1	0 to – 95 dB	Threshold for AGC-reduction by background noise

4.4.6 Speakerphone Coefficient Set

Table 19 shows a possible configuration for a speakerphone application and can be used as a basic programming set.

Table 19 Basic Coefficient Set

CMD Sequence	Coefficient	Code	Value
COP_A	GAE	$0E_H$	5.3 dB
COP_A	GLE	$E5_H$	– 10.2 dB
COP_A	ATT	48_H	28.2 dB
COP_A	ETAE	$0C_H$	48.0 ms
COP_A	ETLE	32_H	200.0 ms
COP_A	TW	09_H	144.0 ms
COP_A	DS	25_H	99 ms/dB
COP_A	SW	64_H	0.6 ms/dB
COP_B	GDSAE	20_H	6.0 dB
COP_B	PDSAE	05_H	8.5 ms/dB
COP_B	GDNAE	20_H	6.0 dB
COP_B	PDNAE	05_H	8.5 ms/dB
COP_B	GDSLE	40_H	12.0 dB
COP_B	PDSLE	02_H	21.3 ms/dB
COP_B	GDNLE	40_H	12.0 dB
COP_B	PDNLE	02_H	21.3 ms/dB

Table 19 Basic Coefficient Set (cont'd)

CMD Sequence	Coefficient	Code	Value
COP_C	LIMX, LIMR	44_H	– 54 dB, – 54 dB
COP_C	OFFX	$0C_H$	4.5 dB
COP_C	OFFR	$0C_H$	4.5 dB
COP_C	LP2LX	20_H	12 dB
COP_C	LP2LR	20_H	12 dB
COP_C	LP1X	$E1_H$	4.0 ms
COP_C	LP1R	$E1_H$	4.0 ms
COP_C	reserved 00_H		
COP_D	PDSX	26_H	102.3 ms
COP_D	PDNX	$F4_H$	32.0 ms
COP_D	LP2SX	20_H	6.6 s
COP_D	LP2NX	44_H	30.0 ms
COP_D	PDSR	26_H	102.3 ms
COP_D	PDNR	$F4_H$	32.0 ms
COP_D	LP2SR	20_H	6.6 s
COP_D	LP2NR	44_H	30.0 ms
COP_E	LGAX	13_H	4.50 dB
COP_E	COMX	$C3_H$	– 20.4 dB
COP_E	AGX	01_H	12.0 dB
COP_E	TMHX	$0A_H$	14.0 ms/dB
COP_E	TMLX	24_H	383.0 ms/dB
COP_E	NOISX	$4F_H$	– 66.2 dB
COP_E	AGIX		0 dB
COP_E	reserved 00_H		
COP_F	LGAR	12_H	5.5 dB
COP_F	COMR	$B2_H$	– 15.1 dB
COP_F	AAR	55_H	– 33.2 dB
COP_F	AGR	00_H	18.1 dB
COP_F	TMHR	$0A_H$	14.0 ms/dB
COP_F	TMLR	$2F_H$	500.9 ms/dB
COP_F	NOISR	$4F_H$	– 66.23 dB
COP_F	AGIR		0 dB

4.5 Controlled Monitoring

A so called “controlled monitoring” can be done when the bit GCR.CME is set. This mode can only be used together with the speakerphone mode (GCR.SP). With CME = ’1’ the attenuation stage GHR is fixed to a value of 0 dB but the attenuation takes place in the analog loudspeaker amplifier ALS in a way that the amplification of the ALS is set to – 9.5 dB or -21.5 dB (depends on ATCR.CMAS setting) as soon as the attenuation control unit switches to transmit mode. Therefore in transmit direction the same behavior as in speakerphone mode occurs but in the receive direction the handset output offers a signal as in normal handset mode while the volume at the loudspeaker output will be reduced to a low level during transmit mode. If the programming for the loudspeaker output (ARCR.LSC) is already chosen for values of less or equal – 9.5 dB, no further attenuation takes place.
In order to get a stable controlled monitoring due to the feedback of the microphone signal to the loudspeaker via the sidetone stage it is possible to change the tap of the sidetone signal from before to after the attenuation stage (PFCR.PGZ = ’1’).

4.6 Voice Data Manipulation

The codec offers several possibilities of manipulating and controlling the codec data to support a variety of applications and operating modes. All the functions and modes can be selected by setting the register bits listed in **table 20**. The signal paths and functions are illustrated in the voice data manipulation block of **figure 58**.

Possible applications and operating modes which can be realized by the voice data manipulation of the codec together with the time slot and data port selection of the integrated IOM-2 Handler are e.g.:

- Three party conferencing with
  - 1 device internal and 2 external subscribers or
  - 2 device internal, tip-ring extension and 1 external subscriber
  The addition of the subscriber information can be done completely in the terminal by the integrated codec
- Communication between codec and other voice data processing devices on IOM-2 (e.g. ACE, Jade, SAM and ISAR)
- The data formats
  PCM A-Law
  PCM µ-Law
  8-bit Linear and
  16-bit Linear are provided.
  The 8-bit formats of CH1 and CH2 in both directions can be masked by an implemented mask register
- Monitoring a running phone call

- Intercommunication: During a running phone call a voice announcement or a query can be switched or added to the desired outputs (handset, loudspeaker or transmit direction)

Table 20 Voice Data Manipulation

Register	Bits	Description
DSSR Data Source Selection Register	DSS1X, DSS2X: Data Source Selection CH1X, Data Source Selection CH2X	As data source for the transmit data channels CH1X or CH2X respectively can be selected: - Codec voice data XDAT - Addition of XDAT and the receive channel CH2R or CH1R respectively. - Receive channel CH2R or CH1R respectively - Idle code The data of the receive channels can be attenuated individually by ATT1R, ATT2R to ensure an acceptable speech quality in the three party conferences
	DSSR: Data Source Selection Receive	As data source for the codec receive data channel RDAT can be selected: - Receive channel CH1R - Receive channel CH2R - Addition of CH1R and CH2R - Idle code
	ENX1, ENX2: Enable Transmit CH1, CH2	The transmit data of CH1X, CH2X can be enabled or disabled
DFR Data Format Register	DF1R, DF2R: Data Format CH1R, CH2R	The data format A-Law µ-Law 8-bit linear and 16-bit linear can be selected
	8LIN1, 8LIN2: 8-bit Linear CH1, 8-bit Linear CH2	An 8-bit linear code can be selected for transmit and receive separately
MASK1R, MASK2R Mask Channel 1,2 Register	MASK1, MASK2: Mask Data CH1, CH2	The 8-bit formats of CH1 and CH2 in both directions can be masked by an implemented mask register

4.7 Test Functions

The codec provides several test and diagnostic functions which can be grouped as follows:

- All programmable configuration registers and coefficient RAM-locations are readable
- Digital loop via PCM-register (DLP)
- Digital loop via signal processor (DLS)
- Digital loop via noise shaper (DLN)
- Analog loop via analog front end (ALF)
- Analog loop via converter (ALC)
- Analog loop via noise shaper (ALN)
- Analog loop via Z-sidetone (ALZ); sidetone gain stage GZ must be enabled (PFCR.GZ = 1) and sidetone gain must be programmed with 0 dB; depending on the DSSR bit setting in the Data Source Selection Register (DSSR) an addition to the incoming voice signal is executed.

4.8 Programming of the Codec

During initialization of the codec a subset of configuration registers and coefficient RAM (CRAM) locations has to be programmed to set the configuration parameters according to the application and desired features.
The codec can be programmed via microcontroller interface (see **chapter 2.1**) or the IOM-2 MONITOR channel (see **chapter 2.2.4**).

The coefficient RAM (CRAM) can generally be programmed in power-up as well as in power-down mode. However, due to the general possibility of concurrent accesses of the ARCOFI®-DSP and the microcontroller, access collisions can not totally be eliminated. To ensure the error free programming of the CRAM, it's recommended to delay the access after switching from power-down to power-up (or after switching from power-up to power-down respectively) by a setup time of 4 IOM-2 frames plus the setup time of the oscillator, i.e in total about 5 ms.

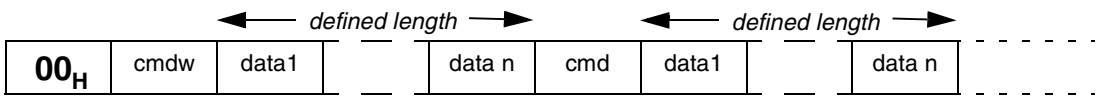
An ARCOFI® compatible programming sequence is available (see **chapter 2.1.1.1** and **chapter 4.8.1**) which allows using the SOP, COP and XOP command sequences of the ARCOFI.

The codec can also be programmed by addressing the configuration registers and coefficient RAM (CRAM) locations directly (see **chapter 4.8.2**).

The following two **chapters 4.8.1** and **4.8.2** give an overview of the access to the codec parameters.
For more detailed information about the individual parameters refer to the corresponding sections in the functional and register description of the codec.

4.8.1 Indirect Programming of the Codec (SOP, COP, XOP)

This programming sequence is compatible to the SOP, COP and XOP command sequences of the ARCOFI. It gives indirect access to the codec registers 60_H-$6E_H$ and the CRAM (80_H-FF_H). The codec command word (cmdw) is followed by a defined number of data bytes (data n; n = 0, 1, 4 or 8). The number of data bytes depends on the codec command. The commands can be applied in any order and number. The coding of the different SOP, COP and XOP commands is listed in the description of the command word (CMDW) in chapter **4.8.1.1**.
Structure of the ARCOFI compatible sequence:



4.8.1.1 Description of the Command Word (CMDW)

Value after reset: BF_H

	7							0
CMDW	R/W	0	CMD5	CMD4	CMD3	CMD2	CMD1	CMD0

R/W 0: writing to configuration registers or to coefficient RAM
1: reading from configuration registers or from coefficient RAM

CMDx Address to internal programmable locations

CMD	5	4	3	2	1	0	
	0	0	X	X	X	X	code reserved
	0	1	X	X	X	X	status operation (SOP)
	1	0	X	X	X	X	coefficient operation (COP)
	1	1	X	X	X	X	extended operation (XOP)

Coding of Status Operations (SOP):

Bit 3	2	1	0	CMD Name	Status	CMD Seq. Len.	CMD Sequence Description (Registers being accessed)
0	0	0	0	SOP_0	R/W	2	<GCR>
0	0	0	1	SOP_1	R/W	2	<PFCR>
0	0	1	0	SOP_2	R/W	2	<TGCR>
0	0	1	1	SOP_3	R/W	2	<TGSR>
0	1	0	0	SOP_4	R/W	2	<ACR>
0	1	0	1	SOP_5	R/W	2	<ATCR>
0	1	1	0	SOP_6	R/W	2	<ARCR>
0	1	1	1	SOP_7	R/W	2	<DFR>
1	0	0	0	SOP_8	R/W	2	<DSSR>
1	0	0	1	SOP_9	R/W	2	<XCR/XSR>
1	0	1	0	SOP_A	R/W	2	<MASK1R>
1	0	1	1	SOP_B	R/W	2	<MASK2R>
1	1	0	0	SOP_C	R/W	2	<TFCR>
1	1	0	1	SOP_D	R/W	2	<TMR1>
1	1	1	0	SOP_E	R/W	2	<TMR2>
1	1	1	1	SOP_F	R/W	9	<DFR>..<GCR>

Coding of Coefficient Operations (COP)

Bit 3	2	1	0	CMD Name	Status	CMD Seq. Len.	CMD Sequence Description	Comments
0	0	0	0	COP_0	R/W	9	<F1> <F1> <G1> <GD1> <T1> <T1> <..> <..>	Tone generator 1
0	0	0	1	COP_1	R/W	9	<F2> <F2> <G2> <GD2> <T2> <T2>	Tone generator 2
							<GTR> <GTX>	Additional TG gain
0	0	1	0	COP_2	R/W	9	<F3> <F3> <G3> <GD3> <T3> <T3>	Tone generator 3
							<FD> <FD>	Dual tone frequency
0	0	1	1	COP_3	R/W	5	<K> <A1> <A2> <GE>	Tone filter
0	1	0	0	COP_4	R/W	5	<TON> <TON> <TOFF> <TOFF>	Control generator
0	1	0	1	COP_5	R/W	9	<GX> <GX>	Transmit gain
							<GR> <GR>	Receive gain
							<ATT1R> <ATT2R> <..> <..>	Conferencing Atten.
0	1	1	0	COP_6	R/W	5	<GZ> <GZ> <..> <..>	Sidetone gain
0	1	1	1	COP_7	R/W	9	<FX1>..<FX8>	Correction filter FX
1	0	0	0	COP_8	R/W	9	<FX9>..<FX12>	
							<FR9>..<FR12>	Correction filter FR
1	0	0	1	COP_9	R/W	9	<FR1>..<FR8>	
1	0	1	0	COP_A	R/W	9	<SP1>..<SP8>	Coefficients for
1	0	1	1	COP_B	R/W	9	<SP9>..<SP16>	Speakerphone
1	1	0	0	COP_C	R/W	9	<SP17>..<SP24>	
1	1	0	1	COP_D	R/W	9	<SP25>..<SP32>	
1	1	1	0	COP_E	R/W	9	<AGCX1>..<AGCX8>	AGC transmit
1	1	1	1	COP_F	R/W	9	<AGCR1>..<AGCR8>	AGC receive

Coding of Extended Operations (XOP)

Bit 3	2	1	0	CMD Name	Status	CMD Seq. Len.	Comments
0	1	1	0	XOP_6	R/W	6	Sequence for volume control of the loudspeaker (SEQ = <ARCR register> <CRAM.LGAR> <CRAM.ATT> <CRAM.GAE> <CRAM.COMR>)
1	1	1	1	XOP_F	R/W	1	No operation (NOP)

4.8.2 Direct Programming of the Codec

The codec registers (60_H-$6F_H$) and the CRAM (80_H-FF_H) are directly accessible (see **chapter 2.1** and **4.8.2.1**).

4.8.2.1 CRAM Back-Up Procedure

For the direct access to individual CRAM coefficients via microcontroller a back-up procedure is provided. This ensures that the codec DSP always works with a consistent and valid coefficient block during the changing of CRAM parameters. The following section describes this back-up procedure.

*Note: For the ARCOFI compatible programming sequence (see **chapter 2.1.1.1**) such a back-up procedure for the CRAM blocks is not necessary because it is done automatically.*

The control of the back-up procedure is done with the CRAM Control Register (CCR) and the CRAM Status Register (CSR).The Control and Status bits in these registers are explained in the following section:

CRAM Block Address (CBADR)

The CRAM range (80_H to FF_H) is subdivided in 16 CRAM blocks with the block address CBADR ='0_H' to'F_H'. Each coefficient block has 8 bytes. The mapping of the CRAM coefficients corresponds to the COP_x sequences of the ARCOFI (see **table 22** and **chapter 4.8.1.1**).

DSP CRAM Access (DCA)

By setting this bit it is possible to select whether the codec DSP has access to the CRAM blocks in the normal CRAM range ('0') or to a temporary 8-byte CRAM block ('1').

Start Back-up Procedure (SBP)

Setting this bit starts the transfer of a CRAM block (CBADR) to the temporary 8-byte CRAM block.

Busy Back-up Procedure (BSYB)

This status bit indicates if a transfer of a CRAM block (CBADR) to the temporary 8-byte CRAM block is running ('1') or not ('0'). If the transfer is running no CRAM access via microcontroller interface is allowed.

Figure 72 shows the access structure of CRAM and temporary CRAM. **Figure • 73** gives a signal flow of the back-up procedure of a CRAM block x (x = 0...F).

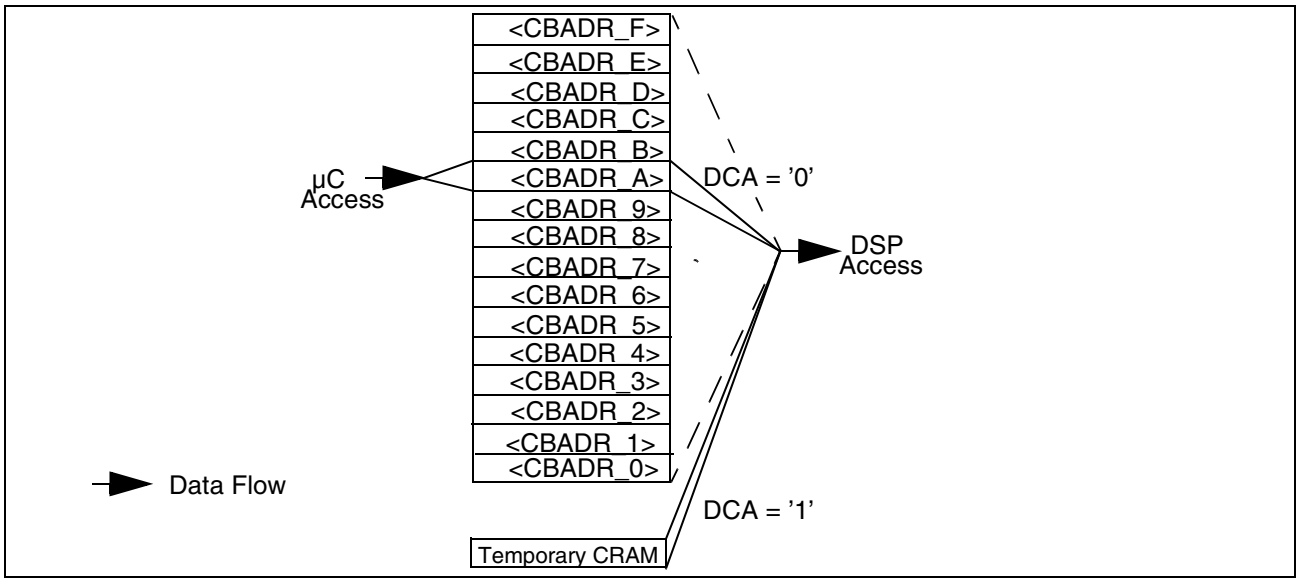


Figure 72
CRAM Access Structure

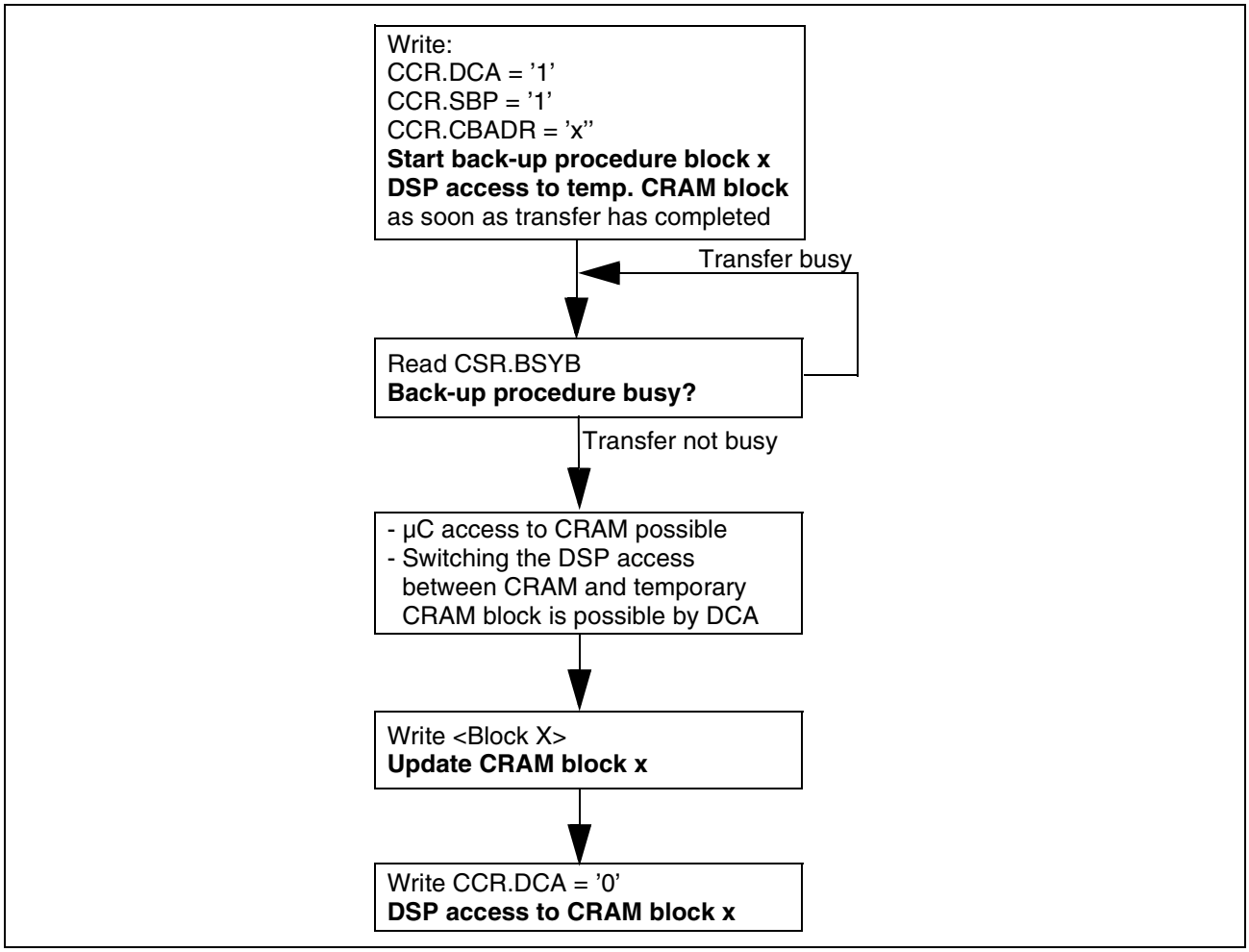


Figure 73
Signal Flow of the Back-up Procedure

4.8.3 Reference Tables for the Register and CRAM Locations

Table 21 Configuration Registers

Address	CMDW WR/RD	Register	Bit	Effect
SOP_0				
60_H	$10_H/90_H$	GCR	SP AGCX AGCR MGCR CME PU ATT2R ATT1R	Speakerphone ON/OFF TX-automatic gain control (if GCR.SP = 1) RX-automatic gain control (if GCR.SP = 1) Modified gain control receive Controlled monitoring enable Power-up/down mode Attenuation of the receive channel related to transmit channel 2 Attenuation of the receive channel related to transmit channel 1
SOP_1				
61_H	$11_H/91_H$	PFCR	GX GR GZ FX PGZ FR DHPR DHPX	TX digital gain RX digital gain Sidetone gain TX-frequency correction filter Position sidetone gain RX-frequency correction filter Disable high-pass (50 Hz) receive Disable high-pass (50 Hz) transmit
SOP_2				
62_H	$12_H/92_H$	TGCR	ET DT ETF PT SEQ TM SM SQTR	Enable tone generator Dual tone mode Enable tone filter Pulsed tone Sequence generator Tone mode Stop mode Square/trapezoid shaped signal

Table 21 Configuration Registers (cont'd)

Address	CMDW WR/RD	Register	Bit	Effect
SOP_3				
63_H	$13_H/93_H$	TGSR	- TRL - TRR DTMF TRX - -	*Reserved* Tone ringing via loudspeaker *Reserved* Tone ringing in receive direction DTMF mode Tone ringing in transmit direction *Reserved* *Reserved*
SOP_4				
64_H	$14_H/94_H$	ACR	- ADC DAC SEM DHOP DHON DLSP DLSN	*Reserved* A/D power down/activate D/A power down/activate Single ended mode of loudspeaker amplifier Disable HOP (tristate) Disable HON (tristate) Disable LSP (tristate) Disable LSN (tristate)
SOP_5				
65_H	$15_H/95_H$	ATCR	MIC(7:4) - CMAS AIMX(1:0)	Microphone amplifier control *Reserved* Controlled monitoring attenuation select Analog input multiplexer
SOP_6				
66_H	$16_H/96_H$	ARCR	HOC(7:4) LSC(3:0)	Handset output amplifier control Loudspeaker output amplifier control
SOP_7				
67_H	$17_H/97_H$	DFR	DF2R(7:6) DF2X(5:4) DF1R(3:2) DF1X(1:0)	Data format CH2 receive Data format CH2 transmit Data format CH1 receive Data format CH1 transmit

Table 21 Configuration Registers (cont'd)

Address	CMDW WR/RD	Register	Bit	Effect
SOP_8				
68_H	$18_H/98_H$	DSSR	DSSR(7:6) ENX2 ENX1 DSS2X(3:2) DSS1X(1:0)	Data source selection receive Enable transmit CH2 Enable transmit CH2 Data source selection CH2 Transmit Data source selection CH1 Transmit
SOP_9				
69_H	19_H/-	XCR	PGCR PGCX ERA - - - - MAAR	Position of gain control receive Position of gain control transmit Enhanced reverse attenuation *Reserved* *Reserved* *Reserved* *Reserved* Monitoring AGC Attenuation Receive
	-/99_H	XSR if MAAR = '0'	PGCR PGCX ERA - - - SPST(1:0)	Read-back position of gain control receive Read-back position of gain control transmit Read-back enhanced reverse attenuation *Reserved* *Reserved* *Reserved* Speakerphone state
	-/99_H	XSR if MAAR = '1'		Value of the momentary AGC attenuation
SOP_A				
$6A_H$	$1A_H/9A_H$	MASK1R	MASK1(7:2) MP1(1:0)	Mask register CH1 Mask Position CH1
SOP_B				
$6B_H$	$1B_H/9B_H$	MASK2R	MASK2(7:2) MP2(1:0)	Mask register CH2 Mask Position CH2

Table 21 Configuration Registers (cont'd)

Address	CMDW WR/RD	Register	Bit	Effect
SOP_C				
$6C_H$	$1C_H/9C_H$	TFCR	- - ALTF(5:3) DLTF(2:0)	*Reserved* *Reserved* Analog Loops and test functions Digital Loops and test functions
SOP_D				
$6D_H$	$1D_H/9D_H$	TMR1		*Reserved*
SOP_E				
$6E_H$	$1E_H/9E_H$	TMR2		*Reserved*
SOP_F				
-	$1F_H/9F_H$	DFR-GCR		ARCOFI compatible sequence for WR/ RD of 8 bytes (Registers)
For the register below there is no command word available				
$6F_H$	WR/	CCR	- - DCA SBP CBADR(3:0)	*Reserved* *Reserved* DSP CRAM access Start back-up procedure CRAM block address
	RD	CSR	- - DCA BSYB CBADR(3:0)	*Reserved* *Reserved* DSP CRAM access Busy back-up procedure CRAM block address

Table 22 Coefficient RAM (CRAM)

Address	CMDW WR/RD	Mnemonic	Description
COP_0: Tone generator parameter set 1			
87_H	$20_H/A0_H$	F1	Tone generator frequency higher byte
86_H			Tone generator frequency lower byte
85_H		G1	Tone generator amplitude
84_H		GD1	Trapezoid generator amplitude
83_H		T1	Beat tone time higher byte
82_H			Beat tone time lower byte
81_H		-	*Reserved*
80_H		-	*Reserved*
COP_1: Tone generator parameter set 2; tone generator level adjustment			
$8F_H$	$21_H/A1_H$	F2	Tone generator frequency higher byte
$8E_H$			Tone generator frequency lower byte
$8D_H$		G2	Tone generator amplitude
$8C_H$		GD2	Trapezoid generator amplitude
$8B_H$		T2	Beat tone time span higher byte
$8A_H$			Beat tone time span lower byte
89_H		GTR	Level adjustment for receive path
88_H		GTX	Level adjustment for transmit path
COP_2: Tone generator parameter set 3; Parameter set for the DTMF-generator (TGSR.DTMF = 1)			
97_H	$22_H/A2_H$	F3	Tone generator frequency higher byte
96_H			Tone generator frequency lower byte
95_H		G3	Tone generator amplitude
94_H		GD3	Trapezoid generator amplitude
93_H		T3	Beat tone time span higher byte
92_H			Beat tone time span lower byte
91_H		FD	Dual tone frequency higher byte
90_H			Dual tone frequency lower byte
COP_3: Tone filter			
$9B_H$	$23_H/A3_H$	K	Attenuation of the stop-band
$9A_H$		A1	Center frequency
99_H		A2	Bandwidth
98_H		GE	Saturation amplification

Table 22 Coefficient RAM (CRAM) (cont'd)

Address	CMDW WR/RD	Mnemonic	Description
COP_4: Control generator			
$A3_H$	$24_H/A4_H$	TON	Turn-on period of the tone generator higher byte
$A2_H$			Turn-on period of the tone generator lower byte
$A1_H$		TOFF	Turn-off period of the tone generator higher byte
$A0_H$			Turn-off period of the tone generator lower byte
COP_5: Receive and transmit gain			
AF_H	$25_H/A5_H$	GX	Transmit gain higher byte
AE_H			Transmit gain lower byte
AD_H		GR	Receive gain higher byte
AC_H			Receive gain lower byte
AB_H		ATT1R	Conferencing attenuation CH1R
AA_H		ATT2R	Conferencing attenuation CH2R
$A9_H$		-	*Reserved*
$A8_H$		-	*Reserved*
COP_6:Sidetone gain			
$B3_H$	$26_H/A6_H$	GZ	Sidetone gain higher byte
$B2_H$			Sidetone gain lower byte
$B1_H$		-	*Reserved*
$B0_H$		-	*Reserved*
COP_7:Transmit correction filter part 5 to part 12			
BF_H	$27_H/A7_H$	FX	Transmit correction filter coefficients part 1
BE_H			Transmit correction filter coefficients part 2
BD_H			Transmit correction filter coefficients part 3
BC_H			Transmit correction filter coefficients part 4
BB_H			Transmit correction filter coefficients part 5
BA_H			Transmit correction filter coefficients part 6
$B9_H$			Transmit correction filter coefficients part 7
$B8_H$			Transmit correction filter coefficients part 8

Table 22 Coefficient RAM (CRAM) (cont'd)

Address	CMDW WR/RD	Mnemonic	Description
COP_8:Transmit correction filter part 1 to part 4 and receive correction filter part 9 to part 12			
$C7_H$	$28_H/A8_H$	FX	Transmit correction filter coefficients part 9
$C6_H$			Transmit correction filter coefficients part 10
$C5_H$			Transmit correction filter coefficients part 11
$C4_H$			Transmit correction filter coefficients part 12
$C3_H$		FR	Receive correction filter coefficients part 9
$C2_H$			Receive correction filter coefficients part 10
$C1_H$			Receive correction filter coefficients part 11
$C0_H$			Receive correction filter coefficients part 12
COP_9:Receive correction filter part 1 to part 8			
CF_H	$29_H/A9_H$	FR	Receive correction filter coefficients 1
CE_H			Receive correction filter coefficients 2
CD_H			Receive correction filter coefficients 3
CC_H			Receive correction filter coefficients 4
CB_H			Receive correction filter coefficients 5
CA_H			Receive correction filter coefficients 6
$C9_H$			Receive correction filter coefficients 7
$C8_H$			Receive correction filter coefficients 8
COP_A:Parameter set for transmit and receive speech comparator Parameter set for speakerphone control unit			
$D7_H$	$2A_H/AA_H$	GAE	Gain of acoustic echo
$D6_H$		GLE	Gain of line echo
$D5_H$		ATT	Attenuation programmed in GHR or GHX
$D4_H$		ETAE	Echo time (acoustic side)
$D3_H$		ETLE	Echo time (line side)
$D2_H$		TW	Wait time
$D1_H$		DS	Decay speed
$D0_H$		SW	Switching time

Table 22 Coefficient RAM (CRAM) (cont'd)

Address	CMDW WR/RD	Mnemonic	Description
COP_B:Parameter set for transmit and receive speech comparator			
DF_H	$2B_H/AB_H$	GDSAE	Reserve when speech is detected (acoustic side)
DE_H		PDSAE	Peak decrement when speech is detected (acoustic side)
DD_H		GDNAE	Reserve when noise is detected (acoustic side)
DC_H		PDNAE	Peak decrement when noise is detected (acoustic side)
DB_H		GDSLE	Reserve when speech is detected (line side)
DA_H		PDSLE	Peak decrement when speech is detected (line side)
$D9_H$		GDNLE	Reserve when noise is detected (line side)
$D8_H$		PDNLE	Peak decrement when noise is detected (line side)
COP_C:Parameter set for transmit and receive speech detector			
$E7_H$	$2C_H/AC_H$	LIM	Starting level of the logarithmic amplifiers
$E6_H$		OFFX	Level offset up to detected noise (transmit)
$E5_H$		OFFR	Level offset up to detected noise (receive)
$E4_H$		LP2LX	Limitation for LP2 (transmit)
$E3_H$		LP2LR	Limitation for LP2 (receive)
$E2_H$		LP1X	Time constant LP1 (transmit)
$E1_H$		LP1R	Time constant LP1 (receive)
$E0_H$		-	*Reserved*
COP_D:Parameter set for receive and transmit speech detector			
EF_H	$2D_H/AD_H$	PDSX	Time constant PD for signal (transmit)
EE_H		PDNX	Time constant PD for noise (transmit)
ED_H		LP2SX	Time constant LP2 for signal (transmit)
EC_H		LP2NX	Time constant LP2 for noise (transmit)
EB_H		PDSR	Time constant PD for signal (receive)
EA_H		PDNR	Time constant PD for noise (receive)
$E9_H$		LP2SR	Time constant LP2 for signal (receive)
$E8_H$		LP2NR	Time constant LP2 for noise (receive)

Table 22 Coefficient RAM (CRAM) (cont'd)

Address	CMDW WR/RD	Mnemonic	Description
COP_E:Parameter set for transmit AGC			
$F7_H$	$2E_H/AE_H$	LGAX	Loudness gain adjustment
$F6_H$		COMX	Compare level rel. to max. PCM-value
$F5_H$		AAX	Attenuation range of automatic control
$F4_H$		AGX	Gain range of automatic control
$F3_H$		TMHX	Settling time constant for higher levels
$F2_H$		TMLX	Settling time constant for lower levels
$F1_H$		NOISX	Threshold for AGC-reduction by background noise
$F0_H$		AGIX	Initial AGC gain transmit
COP_F:Parameter set for receive AGC			
FF_H	$2F_H/AF_H$	LGAR	Loudness gain adjustment
FE_H		COMR	Compare level rel. to max. PCM-value
FD_H		AAR	Attenuation range of automatic control
FC_H		AGR	Gain range of automatic control
FB_H		TMHR	Settling time constant for higher lower levels
FA_H		TMLR	Settling time constant for lower levels
$F9_H$		NOISR	Threshold for AGC-reduction by background noise
$F8_H$		AGIR	Initial AGC attenuation/gain receive

5 Clock Generation

Figure 73 shows the clock system of the SCOUT-DX. The oscillator is used to generate a 15.36 MHz clock signal. The DPLL generates the IOM-2 clocks FSC (8 kHz), DCL (1536 kHz) and BCL (768 kHz) synchronous to the received frames of the line interface. The prescaler for the microcontroller clock output (MCLK) divides the 15.36 MHz clock by 1, 2 and 8 corresponding to the MCLK control bits in the MODE1 register. Additionally it is possible to disable the MCLK output by setting the MCLK bits to'11'. With the CDS bit (Clock Divider Selection) in the MODE1 register a double clock rate for the MCLK output can be selected.

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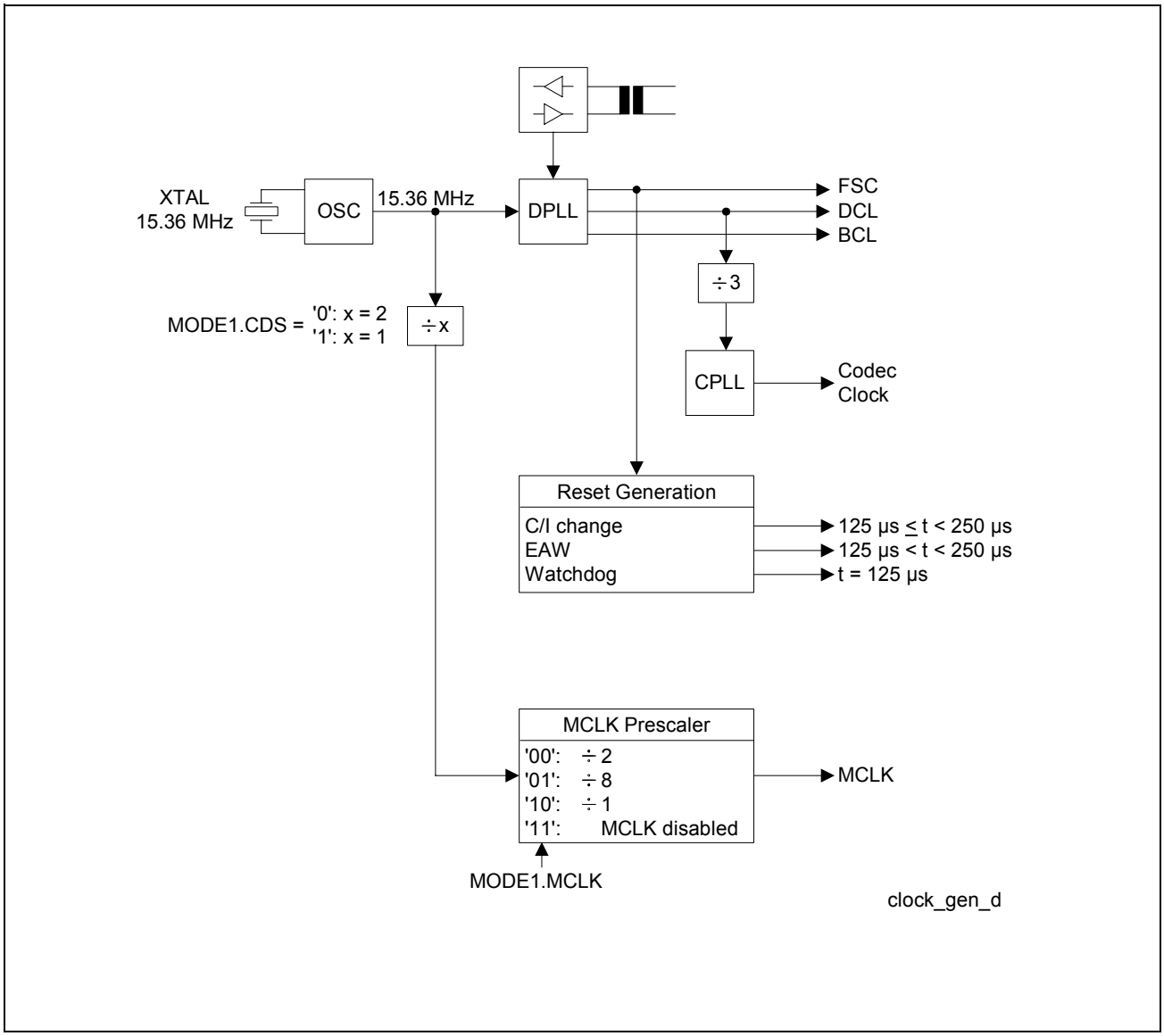

Figure 73
Clock System of the SCOUT-DX

5.1 Jitter

5.1.1 Jitter on IOM-2

The receive PLL readjusts, if the integrator function is enabled (TR_CONF1.RPLL_INTD = ’0’) if six consecutive pulses on the line interface deviate in the same direction. If the integrator function is disabled by setting TR_CONF1.RPLL_INTD to’1’ this is done after the deviation of every pulse. Adjusting on the positive and negative pulses is done by adding/subtracting 1 XTAL from/to the DCL clock.

5.1.2 Jitter on the Line Interface

The transmit clock of the line interface is derived from the receive clock of the line interface.

5.1.3 Jitter on MCLK

Jitter on the MCLK output is directly related to the crystal tolerance. Only clock dividers are involved.

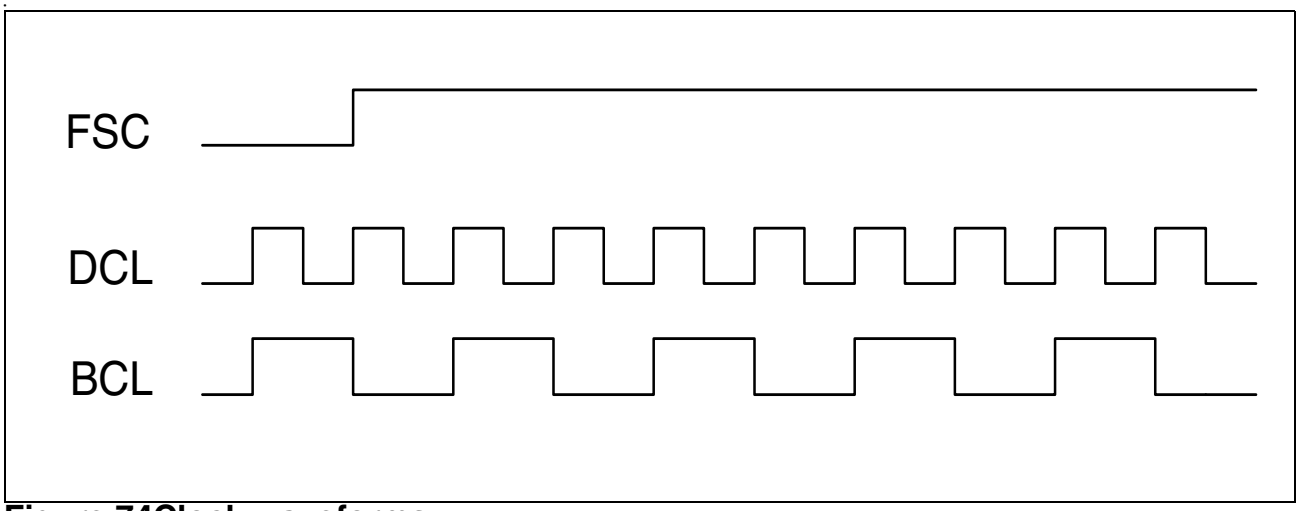

Figure 74Clock waveforms

6 Reset

The SCOUT-DX can be reset completely by a hardware reset (pin $\overline{RST}$). Additionally each functional block can be reset separately via register SRES.

If enabled an exchange awake, subscriber awake or watchdog time out can generate a reset on pin $\overline{RSTO}$/SDS2. A hardware reset always generates a reset on pin $\overline{RSTO}$/SDS2 (see **figure 75**).

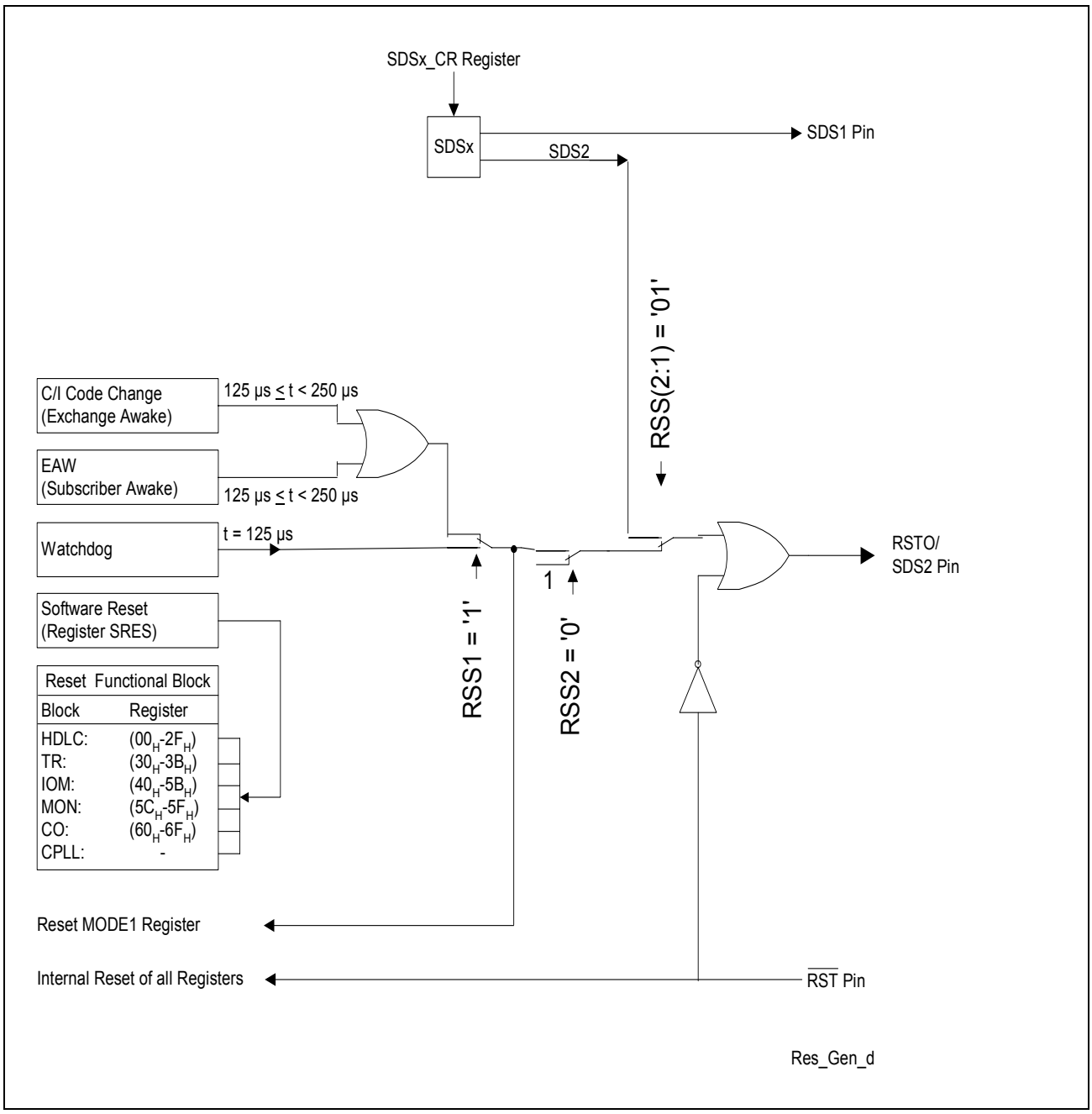

Figure 75
Reset Generation. The above mentioned reset pulse widths are controlled by the clock pin FSC

6.1 Reset Source Selection

The internal reset sources C/I code change, $\overline{\text{EAW}}$ and Watchdog can be output at the low active reset pin $\overline{\text{RSTO}}$/SDS2. The selection of these reset sources can be done with the RSS2,1 bits in the MODE1 register according **table 23**.
If RSS2,1 ='01' the $\overline{\text{RSTO}}$/SDS2 pin has SDS2 functionality and a serial data strobe signal (see **chapter 2.2.3**) is output at the $\overline{\text{RSTO}}$/SDS2 pin. In this case no reset except the hardware reset is output at $\overline{\text{RSTO}}$/SDS2. The internal reset sources set the MODE1 register to its default value.

Table 23
Reset Source Selection

RSS2 Bit 1	RSS1 Bit 0	C/I Code Change	EAW	Watchdog Timer	SDS2 Functionality
0	0	--	--	--	--
0	1	--	--	--	x
1	0	x	x	--	--
1	1	--	--	x	--

- **C/I Code Change (Exchange Awake)** A change in the downstream C/I channel (C/I0) generates a reset pulse of 125µs ≤ t ≤ 250µs.
- **$\overline{\text{EAW}}$ (Subscriber Awake)**
  A low pulse of at least 65 as pulse width on the $\overline{\text{EAW}}$ input starts the oscillator from the power down state and generates a reset pulse of 125 µs ≤ t ≤ 250 µs.
- **Watchdog Timer**
  After the selection of the watchdog timer (RSS ='11') an internal timer is reset and started. During every time period of 128 ms the microcontroller has to program the WTC1- and WTC2 bits in the following sequence to reset and restart the watchdog timer:

		WTC1	WTC2
	1. 2.	1 0	0 1

If not, the timer expires and a WOV-interrupt (ISTA Register) together with a reset pulse of 125 µs is generated.
If the watchdog timer is enabled (RSS = '11') the RSS bits can only be changed by a hardware reset.

6.2 External Reset Input

At the active low $\overline{RST}$ input pin an external reset can be applied forcing the device into the reset state. This external reset signal is additionally fed to the $\overline{RSTO}$/SDS2 output. The length of the reset signal is specified in **chapter 8.1.8**.

After an external reset ($\overline{RST}$) all internal registers are set to their reset values (see register description in **chapter 7**).

6.3 Software Reset Register (SRES)

Every internal functional block can be reset separately by setting the corresponding bit in the SRES register (see **chapter 7.2.13**). The reset state is activated as long as the bit is set to'1'. The address range of the registers which will be reset at each SRES bit is listed in **figure 75**.

6.4 Pin Behavior during Reset

During each reset the reference voltage (V_{REF}) stays applied, the oscillator and data clocks (DCL) keep running.

In all cases the microcontroller clock is running.

During any reset that has an influence on the IOM handler (see **figure 75**) the pin FSC is set to'1', the pin SDS1 is set to'0' and pin BCL, DD and DU are in the high-impedance state.

During any reset that has an influence on the codec (see **figure 75**) the pins LSP, LSN, HOP and HON are in the high-impedance state.

During any reset that has an influence on the transceiver (see **figure 75**) the pins Via and LIb are in the high-impedance state.

During hardware reset the pins SDX and $\overline{INT}$ are in the high-impedance state.

A hardware reset is always output at pin $\overline{RSTO}$/SDS2. This reset will be released by the falling edge of BCL following the release of the pin $\overline{RST}$.

7 Detailed Register Description

The register mapping is shown in **Figure 76**.

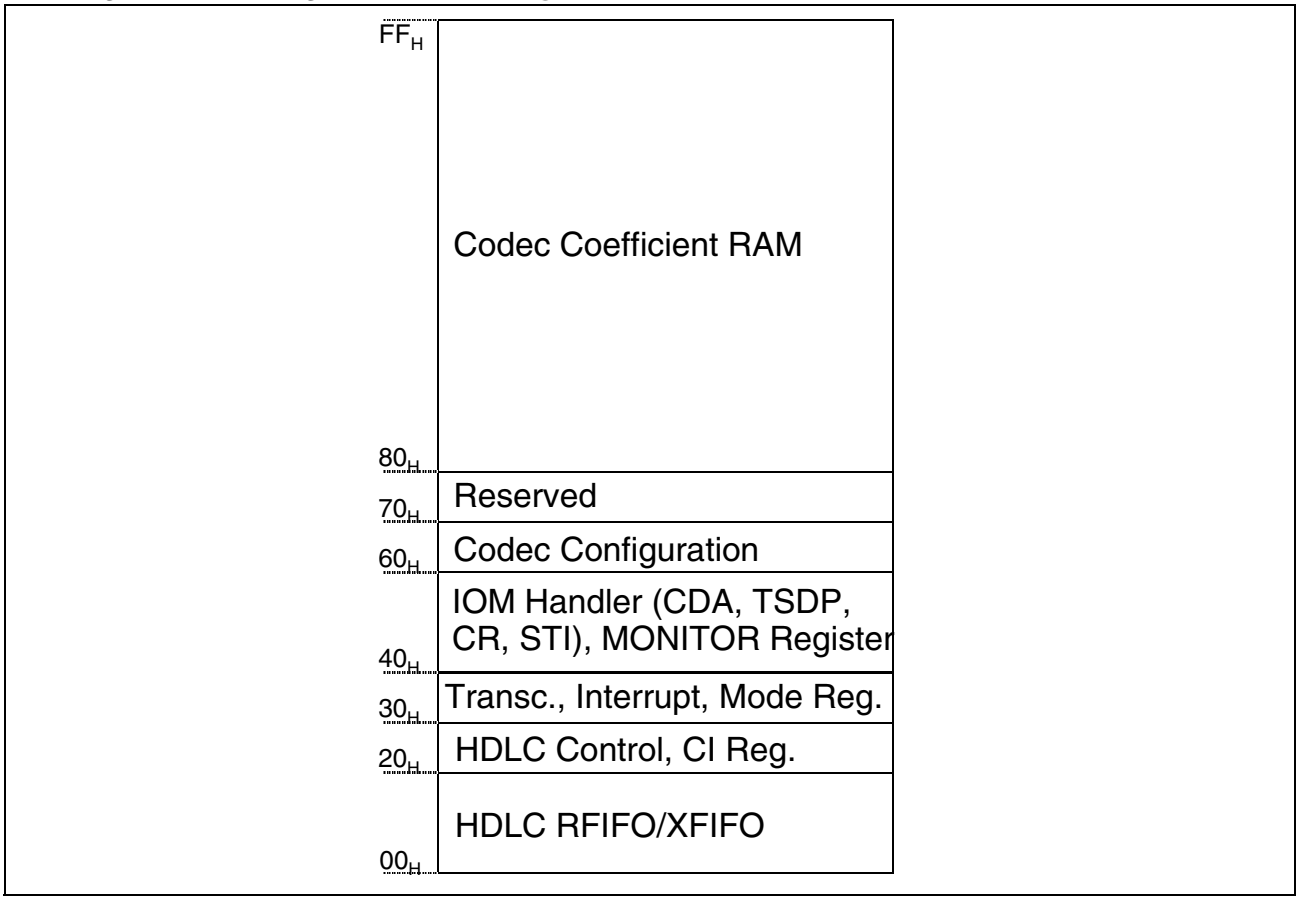

Figure 76
Register Mapping

The register address range from 00-1F$_H$ is assigned to the two FIFOs having an identical address range. The address range 20-2F$_H$ pertains to the HDLC controller and the CI handler. The register set ranging from 30-3F$_H$ pertains to the transceiver, interrupt and general configuration registers. The address range from 40-59$_H$ is assigned to the IOM handler with the registers for timeslot and data port selection (TSDP) and the control registers (CR) for the codec data (CO), transceiver data (TR), Monitor data (MON), HDLC/CI data (HCI) and controller access data (CDA), serial data strobe signal (SDS), IOM interface (IOM) and synchronous transfer interrupt (STI). The address range from 5C-5F$_H$ pertains to the MONITOR handler. The codec configuration registers and the codec coefficient RAM (CRAM) are assigned to the address range 60-6F$_H$ or 80-FF$_H$ respectively.

The register summaries are shown in the following tables containing the abbreviation of the register name and the register bits, the register address, the reset values and the register type (Read/Write). A detailed register description follows these register summaries. The register summaries and the description are sorted in ascending order of the register address.

HDLC Control Registers, CI Handler

Name	7	6	5	4	3	2	1	0	ADDR	R/W	RES
RFIFO	D-Channel Receive FIFO								00_H-$1F_H$	R	
XFIFO	D-Channel Transmit FIFO								00_H-$1F_H$	W	
ISTAH	RME	RPF	RFO	XPR	XMR	XDU	0	0	20_H	R	10_H
MASKH	RME	RPF	RFO	XPR	XMR	XDU	0	0	20_H	W	FC_H
STAR	XDOV	XFW	0	0	RACI	0	XACI	0	21_H	R	40_H
CMDR	RMC	RRES	0	STI	XTF	0	XME	XRES	21_H	W	00_H
MODEH	MDS2	MDS1	MDS0	0	RAC	DIM2	DIM1	DIM0	22_H	R/W	$C0_H$
EXMR	XFBS	RFBS		SRA	XCRC	RCRC	0	ITF	23_H	R/W	00_H
TIMR	CNT			VALUE					24_H	R/W	00_H
SAP1	SAPI1						0	MHA	25_H	W	FC_H
SAP2	SAPI2						0	MLA	26_H	W	FC_H
RBCL	RBC7							RBC0	26_H	R	00_H
RBCH	0	0	0	OV	RBC11			RBC8	27_H	R	00_H
TEI1	TEI1							EA	27_H	W	FF_H
TEI2	TEI2							EA	28_H	W	FF_H
RSTA	VFR	RDO	CRC	RAB	SA1	SA0	C/R	TA	28_H	R	$0E_H$
TMH	0	0	0	0	0	0	0	TLP	29_H	R/W	00_H
	Reserved								$2A_H$-$2D_H$		
CIR0	CODR0				CIC0	CIC1	S/G	BAS	$2E_H$	R	$F3_H$
CIX0	CODX0				TBA2	TBA1	TBA0	BAC	$2E_H$	W	FE_H
CIR1	CODR1						0	0	$2F_H$	R	FC_H
CIX1	CODX1						CICW	CI1E	$2F_H$	W	FE_H

Transceiver, Interrupt, General Configuration Registers

NAME	7	6	5	4	3	2	1	0	ADDR	R/W	RES
TR_ CONF0	DIS_ TR	0	0	0	L1SW	0	0	LDD	30_H	R/W	00_H
TR_ CONF1	RPLL_ INTD	1	1	0	0	0	1	0	31_H	R/W	62_H
TR_ CONF2	DIS_ TX	0	0	0	0	0	RLP	0	32_H	R/W	00_H
TR_STA	RINF		0	RDS	0	FSYN	0	0	33_H	R	00_H
TR_CMD	XINF			0	0	PD	LP_A	0	34_H	R/W	00_H
	Reserved								35_H	R/W	
	Reserved								36_H-37_H		
ISTATR	0	x	x	x	LD	RIC	0	0	38_H	R	00_H
MASKTR	0	1	1	1	LD	RIC	1	1	39_H	R/W	$7F_H$
	Reserved								$3A_H$- $3B_H$		
ISTA	0	ST	CIC	TIN	WOV	TRAN	MOS	HDLC	$3C_H$	R	01_H
MASK	0	ST	CIC	TIN	WOV	TRAN	MOS	HDLC	$3C_H$	W	$7F_H$
MODE1	MCLK		CDS	WTC1	WTC2	CFS	RSS2	RSS1	$3D_H$	R/W	00_H
MODE2	0	0	0	0	0	DREF	0	PPSDX	$3E_H$	R/W	00_H
ID	0	0	DESIGN						$3F_H$	R	$0x_H$
SRES	0	0	RES_ CPLL	RES_ MON	RES_ HDLC	RES_ IOM	RES_ TR	RES_ CO	$3F_H$	W	00_H

IOM Handler (Timeslot , Data Port Selection, CDA Data and CDA Control Register)

Name	7	6	5	4	3	2	1	0	ADDR	R/W	RES
CDA10	Controller Data Access Register (CH10)								40_H	R/W	FF_H
CDA11	Controller Data Access Register (CH11)								41_H	R/W	FF_H
CDA20	Controller Data Access Register (CH20)								42_H	R/W	FF_H
CDA21	Controller Data Access Register (CH21)								43_H	R/W	FF_H
CDA_ TSDP10	DPS	0	0	0	TSS				44_H	R/W	00_H
CDA_ TSDP11	DPS	0	0	0	TSS				45_H	R/W	01_H
CDA_ TSDP20	DPS	0	0	0	TSS				46_H	R/W	80_H
CDA_ TSDP21	DPS	0	0	0	TSS				47_H	R/W	81_H
CO_ TSDP10	DPS	0	0	0	TSS				48_H	R/W	80_H
CO_ TSDP11	DPS	0	0	0	TSS				49_H	R/W	81_H
CO_ TSDP20	DPS	0	0	0	TSS				$4A_H$	R/W	81_H
CO_ TSDP21	DPS	0	0	0	TSS				$4B_H$	R/W	85_H
TR_ TSDP_B1	DPS	0	0	0	TSS				$4C_H$	R/W	00_H
TR_ TSDP_B2	DPS	0	0	0	TSS				$4D_H$	R/W	01_H

Name	7	6	5	4	3	2	1	0	ADDR	R/W	RES
CDA1_CR	0	0	EN_TBM	EN_I1	EN_I0	EN_O1	EN_O0	SWAP	$4E_H$	R/W	00_H
CDA2_CR	0	0	EN_TBM	EN_I1	EN_I0	EN_O1	EN_O0	SWAP	$4F_H$	R/W	00_H

IOM Handler (Control Registers, Synchronous Transfer Interrupt Control), MONITOR Handler

Name	7	6	5	4	3	2	1	0	ADDR	R/W	RES
CO_CR	0	0	0	0	EN21	EN20	EN11	EN10	50_H	R/W	00_H
TR_CR	0	0	EN_D	EN_B2R	EN_B1R	EN_B2X	EN_B1X	0	51_H	R/W	$3E_H$
HCI_CR	DPS_CI1	EN_CI1	EN_D	EN_B2H	EN_B1H	0	0	0	52_H	R/W	$A0_H$
MON_CR	DPS	EN_MON	0	0	0	0	MCS		53_H	R/W	40_H
SDS1_CR	ENS_TSS	ENS_TSS+1	ENS_TSS+3	0	TSS				54_H	R/W	00_H
SDS2_CR	ENS_TSS	ENS_TSS+1	ENS_TSS+3	0	TSS				55_H	R/W	00_H
IOM_CR	SPU	0	0	TIC_DIS	EN_BCL	CLKM	DIS_OD	DIS_IOM	56_H	R/W	00_H
MCDA	MCDA21		MCDA20		MCDA11		MCDA10		57_H	R	FF_H
STI	STOV21	STOV20	STOV11	STOV10	STI21	STI20	STI11	STI10	58_H	R	00_H
ASTI	0	0	0	0	ACK21	ACK20	ACK11	ACK10	58_H	W	00_H
MSTI	STOV21	STOV20	STOV11	STOV10	STI21	STI20	STI11	STI10	59_H	R/W	FF_H

Name	7	6	5	4	3	2	1	0	ADDR	R/W	RES
SDS_ CONF	0	0	0	0	0	0	SDS2_ BCL	SDS1_ BCL	$5A_H$	R/W	00_H
	Reserved								$5B_H$		
MOR	MONITOR Receive Data								$5C_H$	R	FF_H
MOX	MONITOR Transmit Data								$5C_H$	W	FF_H
MOSR	MDR	MER	MDA	MAB	0	0	0	0	$5D_H$	R	00_H
MOCR	MRE	MRC	MIE	MXC	0	0	0	0	$5E_H$	R/W	00_H
MSTA	0	0	0	0	0	MAC	0	TOUT	$5F_H$	R	00_H
MCONF	0	0	0	0	0	0	0	TOUT	$5F_H$	W	00_H

Codec Configuration Registers

Name	7	6	5	4	3	2	1	0	ADDR	R/W	RES
GCR	SP	AGCX	AGCR	MGCR	CME	PU	ATT2R	ATT1R	60_H	R/W	00_H
PFCR	GX	GR	GZ	FX	PGZ	FR	DHPR	DHPX	61_H	R/W	00_H
TGCR	ET	DT	ETF	PT	SEQ	TM	SM	SQTR	62_H	R/W	00_H
TGSR	0	TRL	0	TRR	DTMF	TRX	0	0	63_H	R/W	00_H
ACR	0	ADC	DAC	SEM	DHOP	DHON	DLSP	DLSN	64_H	R/W	00_H
ATCR	MIC				0	CMAS	AIMX		65_H	R/W	00_H
ARCR	HOC				LSC				66_H	R/W	00_H
DFR	DF2R		DF2X		DF1R		DF1X		67_H	R/W	00_H
DSSR	DSSR		ENX2	ENX1	DSS2X		DSS1X		68_H	R/W	00_H

XCR	PGCR	PGCX	ERA	0	0	0	0	MAAR	69_H	W	00_H
XSR	PGCR	PGCX	ERA	0	0	0	SPST		69_H	R	00_H
	Momentary AGC Attenuation (if XCR.MAAR = ’1’)								69_H	R	00_H
MASK1R	MASK1						MP1		$6A_H$	R/W	00_H
MASK2R	MASK2						MP2		$6B_H$	R/W	00_H
TFCR	0	0	ALTF			DLTF			$6C_H$	R/W	00_H
	Reserved								$6D_H$		
	Reserved								$6E_H$		
CCR	0	0	DCA	SBP	CBADR				$6F_H$	W	00_H
CSR	0	0	DCA	BSYB	CBADR				$6F_H$	R	00_H
Name	7	6	5	4	3	2	1	0	ADDR	R/W	RES
	Reserved								70_H-$7E_H$		
NOP	1	1	1	1	1	1	1	1	$7F_H$	R	FF_H

*Note: Address 80_H-FF_H belong to the coefficient RAM (see **chapter 4.8.3** and **chapter 7.4.14**)*

7.1 HDLC Control and C/I Registers

7.1.1 RFIFO - Receive FIFO

	7 … 0	
RFIFO	Receive data	RD (00_H-$1F_H$)

A read access to any address within the range 00h-1Fh gives access to the “current” FIFO location selected by an internal pointer which is automatically incremented after each read access. This allows for the use of efficient “move string” type commands by the microcontroller.

The RFIFO contains up to 32 bytes of received data.

After an ISTAH.RPF interrupt, a complete data block is available. The block size can be 4, 8, 16, 32 bytes depending on the EXMR.RFBS setting.

After an ISTAH.RME interrupt, the number of received bytes can be obtained by reading the RBCL register.

7.1.2 XFIFO - Transmit FIFO

	7 … 0	
XFIFO	Transmit data	WR (00_H-$1F_H$)

A write access to any address within the range 00-$1F_H$ gives access to the “current” FIFO location selected by an internal pointer which is automatically incremented after each write access. This allows the use of efficient “move string” type commands by the microcontroller.

Depending on EXMR.XFBS up to 16 or 32 bytes of transmit data can be written to the XFIFO following an ISTAH.XPR interrupt.

7.1.3 ISTAH - Interrupt Status Register HDLC

Value after reset: 10_H

	7							0	
ISTAH	RME	RPF	RFO	XPR	XMR	XDU	0	0	RD (20_H)

RME ... Receive Message End

One complete frame of length less than or equal to the defined block size (EXMR.RFBS) or the last part of a frame of length greater than the defined block size has been received. The contents are available in the RFIFO. The message length and additional information may be obtained from RBCH and RBCL and the RSTA register.

RPF ... Receive Pool Full

A data block of a frame longer than the defined block size (EXMR.RFBS) has been received and is available in the RFIFO. The frame is not yet complete.

RFO ... Receive Frame Overflow

The received data of a frame could not be stored, because the RFIFO is occupied. The whole message is lost.
This interrupt can be used for statistical purposes and indicates that the microcontroller does not respond quickly enough to an RPF or RME interrupt (ISTAH).

XPR ... Transmit Pool Ready

A data block of up to the defined block size (EXMR.XFBS) can be written to the XFIFO. An XPR interrupt will be generated in the following cases:

- after an XTF or XME command as soon as the 16 or 32 respectively bytes in the XFIFO are available and the frame is not yet complete
- after an XTF together with an XME command is issued, when the whole frame has been transmitted

XMR ... Transmit Message Repeat

The transmission of the last frame has to be repeated because a collision has been detected after the $16^{th}/32^{th}$ data byte of a transmit frame.

XDU ... Transmit Data Underrun

The current transmission of a frame is aborted by transmitting seven ’1’s because the XFIFO holds no further data. This interrupt occurs whenever the microcontroller has failed to respond to an XPR interrupt (ISTAH register) quickly enough, after having initiated a transmission and the message to be transmitted is not yet complete.

7.1.4 MASKH - Mask Register HDLC

Value after reset: FC_H

	7							0	
MASKH	RME	RPF	RFO	XPR	XMR	XDU	0	0	WR (20_H)

Each interrupt source in the ISTAH register can be selectively masked by setting to ’1’ the corresponding bit in MASK. Masked interrupt status bits are not indicated when ISTAH is read. Instead, they remain internally stored and pending, until the mask bit is reset to ’0’.

7.1.5 STAR - Status Register

Value after reset: 40_H

	7							0	
STAR	XDOV	XFW	0	0	RACI	0	XACI	0	RD (21_H)

XDOV ... Transmit Data Overflow

More than 16/32 bytes have been written in one pool of the XFIFO, i.e. data has been overwritten.

XFW ... Transmit FIFO Write Enable

Data can be written in the XFIFO. This bit may be polled instead of (or in addition to) using the XPR interrupt.

RACI ... Receiver Active Indication

The HDLC receiver is active when RACI = ’1’. This bit may be polled. The RACI bit is set active after a begin flag has been received and is reset after receiving an abort sequence.

XACI ... Transmitter Active Indication

The HDLC-transmitter is active when XACI = ’1’. This bit may be polled. The XACI-bit is active when an XTF-command is issued and the frame has not been completely transmitted.

7.1.6 CMDR - Command Register

Value after reset: 00_H

	7							0	
CMDR	RMC	RRES	0	STI	XTF	0	XME	XRES	WR (21_H)

RMC ... Receive Message Complete

Reaction to RPF (Receive Pool Full) or RME (Receive Message End) interrupt. By setting this bit, the microcontroller confirms that it has fetched the data, and indicates that the corresponding space in the RFIFO may be released.

RRES ... Receiver Reset

HDLC receiver is reset, the RFIFO is cleared of any data.

STI ... Start Timer

The hardware timer is started when STI is set to one. The timer may be stopped by a write to the TIMR register.

XTF ... Transmit Transparent Frame

After having written up to 16 or 32 bytes (EXMR.XFBS) in the XFIFO, the microcontroller initiates the transmission of a transparent frame by setting this bit to ’1’. Except in the extended transparent mode the opening flag is automatically added to the message.

XME ... Transmit Message End

By setting this bit to ’1’ the microcontroller indicates that the data block written last in the XFIFO completes the corresponding frame. Except in the extended transparent mode the transmission is terminated by appending the CRC and the closing flag sequence to the data.

XRES ... Transmitter Reset

HDLC transmitter is reset and the XFIFO is cleared of any data. This command can be used by the microcontroller to abort a frame currently in transmission.

Note: After an XPR interrupt further data has to be written to the XFIFO and the appropriate Transmit Command (XTF) has to be written to the CMDR register again to continue transmission, when the current frame is not yet complete (see also XPR in ISTAH).
During frame transmission, the 0-bit insertion according to the HDLC bit-stuffing mechanism is done automatically except in the extended mode.

7.1.7 MODEH - Mode Register

Value after reset: $C0_H$

	7							0	
MODEH	MDS2	MDS1	MDS0	0	RAC	DIM2	DIM1	DIM0	RD/WR (22_H)

MDS2-0 ... Mode Select

Determines the message transfer mode of the HDLC controller, as follows:

MDS2-0	Mode	Number of Address Bytes	Address Comparison 1.Byte	Address Comparison 2.Byte	Remark
0 0 0	Reserved				
0 0 1	Reserved				
0 1 0	Non-Auto mode	1	TEI1,TEI2	–	One-byte address compare.
0 1 1	Non-Auto mode	2	SAP1,SAP2,SAPG	TEI1,TEI2,TEIG	Two-byte address compare.
1 0 0	Extended transparent mode				
1 1 0	Transparent mode 0	–	–	–	No address compare. All frames accepted.
1 1 1	Transparent mode 1	> 1	SAP1,SAP2,SAPG	–	High-byte address compare.
1 0 1	Transparent mode 2	> 1	–	TEI1,TEI2,TEIG	Low-byte address compare.

Note: SAP1, SAP2: two programmable address values for the first received address byte (in the case of an address field longer than 1 byte);
SAPG = fixed value FC / FE_H.
TEI1, TEI2: two programmable address values for the second (or the only, in the case of a one-byte address) received address byte; TEIG = fixed value FF_H

*Two different methods of the high byte and/or low byte address comparision can be selected by setting SAP1.MHA and/or SAP2.MLA (see also description of these bits in **chapter 7.1.10** or **7.1.12** respectively)*

RAC ... Receiver Active

The HDLC receiver is activated when this bit is set to ’1’. If it is ’0’ the HDLC data is not evaluated in the receiver.

DIM2-0 ... Digital Interface Modes

These bits define the characteristics of the IOM Data Ports (DU, DD). The DIM0 bit enables/disables the collission detection. The DIM1 bit enables/disables the TIC bus access. The effect of the individual DIM bits is summarized in **table 24**.

Table 24
IOM®-2 Terminal Modes

DIM2	DIM1	DIM0	Characteristics
0	x	0	Transparent D-channel, the collission detection is disabled
0	x	1	Stop/go bit evaluated for D-channel access handling
0	0	x	Last octet of IOM channel 2 used for TIC bus access
0	1	x	TIC bus access is disabled
1	x	x	Reserved

7.1.8 EXMR- Extended Mode Register

Value after reset: 00_H

	7						0	
EXMR	XFBS	RFBS	SRA	XCRC	RCRC	0	ITF	RD/WR (23_H)

XFBS ... Transmit FIFO Block Size

0: Block size for the transmit FIFO data is 32 byte
1: Block size for the transmit FIFO data is 16 byte

Note: A change of XFBS will take effect after a transmitter command (CMDR.XME, CMDR.XRES, CMDR.XTF) has been written

RFBS ... Receive FIFO Block Size

RFBS Bit6	RFBS Bit5	Block Size Receive FIFO
0	0	32 byte
0	1	16 byte
1	0	8 byte
1	1	4 byte

Note: A change of RFBS will take effect after a receiver command (CMDR.RMC, CMDR.RRES,) has been written

SRA ... Store Receive Address

0: Receive Address is not stored in the RFIFO
1: Receive Address is stored in the RFIFO

XCRC ... Transmit CRC

0: CRC is transmitted
1: CRC is not transmitted

RCRC ... Receive CRC

0: CRC is not stored in the RFIFO
1: CRC is stored in the RFIFO

ITF ... Interframe Time Fill

Selects the inter-frame time fill signal which is transmitted between HDLC-frames.

0: Idle (continuous ’1’)
1: Flags (sequence of patterns: ‘0111 1110’)

Note: ITF must be set to ’0’ for power down mode.
In applications with D-channel access handling (collision resolution), the only possible inter-frame time fill is idle (continuous ’1’)*. Otherwise the D-channel on the line interface can not be accessed*

7.1.9 TIMR - Timer Register

Value after reset: 00_H

	7 … 5	4 … 0	
TIMR	CNT	VALUE	RD/WR (24_H)

CNT ...

CNT together with VALUE determine the time period T2 after which a TIN interrupt will be generated in the normal case:

T = CNT x 2.048 sec + T1 with **T1 = (VALUE+1) x 0.064 sec**

The timer can be started by setting the STI-bit in CMDR and will be stopped when a TIN interrupt is generated or the TIMR register is written.

Note: If CNT is set to 7, a TIN interrupt is indefinitely generated after every expiration of T1.

VALUE ... Determines the time period T1

T1 = (VALUE + 1) x 0.064 sec

7.1.10 SAP1 - SAPI1 Register

Value after reset: FC_H

	7 … 0			
SAP1	SAPI1	0	MHA	WR (25_H)

SAPI1 ... SAPI1 value

Value of the first programmable Service Access Point Identifier (SAPI) according to the ISDN LAPD protocol.

MHA ... Mask High Address

0: The SAPI address of an incomming frame is compared with SAP1, SAP2, SAPG
1: The SAPI address of an incomming frame is compared with SAP1 and SAPG. SAP1 can be masked with SAP2 thereby bitpositions of SAP1 are not compared if they are set to ’1’ in SAP2.

7.1.11 RBCL - Receive Frame Byte Count Low

Value after reset: 00_H

	7	0	
RBCL	RBC7	RBC0	RD (26_H)

RBC7-0 ... Receive Byte Count

Eight least significant bits of the total number of bytes in a received message.

7.1.12 SAP2 - SAPI2 Register

Value after reset: FC_H

	7		0	
SAP2	SAPI2	0	MLA	WR (26_H)

SAPI2 ... SAPI2 value

Value of the second programmable Service Access Point Identifier (SAPI) according to the ISDN LAPD-protocol.

MLA ... Mask Low Address

0: The TEI address of an incomming frame is compared with TEI1, TEI2, TEIG
1: The TEI address of an incomming frame is compared with TEI1 andTEIG.
TEI1 can be masked with TEI2 thereby bitpositions of TEI1 are not compared if they are set to ’1’ in TEI2

7.1.13 RBCH - Receive Frame Byte Count High

Value after reset: 00_H.

	7					0	
RBCH	0	0	0	OV	RBC11	RBC8	RD (27_H)

OV ... Overflow

A ’1’ in this bit position indicates a message longer than $(2^{12} - 1) = 4095$ bytes .

RBC11-8 ... Receive Byte Count

Four most significant bits of the total number of bytes in a received message.

Note: Normally RBCH and RBCL should be read by the microcontroller after an RME-interrupt in order to determine the number of bytes to be read from the RFIFO, and the total message length. The contents of the registers are valid only after an RME or RPF interrupt, and remain so until the frame is acknowledged via the RMC bit or RRES.

7.1.14 TEI1 - TEI1 Register 1

Value after reset: FF_H

	7	0	
TEI1	TEI1	EA	WR (27_H)

TEI1 ... Terminal Endpoint Identifier

In all message transfer modes except in transparent modes 0, 1 and extended transparent mode, TEI1 is used for address recognition. In the case of a two-byte address field, it contains the value of the first programmable Terminal Endpoint Identifier according to the ISDN LAPD-protocol.
In non-auto-modes with one-byte address field, TEI1 is a command address, according to X.25 LAPB.

EA ... Address field Extension bit

This bit is set to ’1’ according to HDLC/LAPD.

7.1.15 RSTA - Receive Status Register

Value after reset: $0E_H$

	7							0	
RSTA	VFR	RDO	CRC	RAB	SA1	SA0	C/R	TA	RD (28_H)

VFR ... Valid Frame

Determines whether a valid frame has been received.
The frame is valid (1) or invalid (0).
A frame is invalid when there is not a multiple of 8 bits between flag and frame end (flag, abort).

RDO ... Receive Data Overflow

If RDO=1, at least one byte of the frame has been lost, because it could not be stored in RFIFO.

CRC ... CRC Check

The CRC is correct (1) or incorrect (0).

RAB ... Receive Message Aborted

The receive message was aborted by the remote station (1), i.e. a sequence of seven 1's was detected before a closing flag.

SA1-0 ... SAPI Address Identification
TA ... TEI Address Identification

SA1-0 are significant in non-auto-mode with a two-byte address field, as well as in transparent mode 3. TA is significant in all modes except in transparent modes 0 and 1.

Two programmable SAPI values (SAP1, SAP2) plus a fixed group SAPI (SAPG of value FC/FE_H), and two programmable TEI values (TEI1, TEI2) plus a fixed group TEI (TEIG of value FF_H), are available for address comparison.

The result of the address comparison is given by SA1-0 and TA, as follows:

C/R ... Command/Response

The C/R bit contains the C/R bit of the received frame (Bit1 in the SAPI address)

Note: The contents of RSTA corresponds to the last received HDLC frame; it is duplicated into RFIFO for every frame (last byte of frame)

				Address Match with	
	SA1	**SA0**	**TA**	**1st Byte**	**2nd Byte**
Number of Address Bytes = 1	x x	x x	0 1	TEI2 TEI1	- -
Number of address Bytes=2	0 0 0 0 1 1 1	0 0 1 1 0 0 1	0 1 0 1 0 1 x	SAP2 SAP2 SAPG SAPG SAP1 SAP1 reserved	TEIG TEI2 TEIG TEI1 or TEI2 TEIG TEI1

Note: If SAP1 and SAP2 contains identical values, the combination 001 will be omitted.

7.1.16 TEI2 - TEI2 Register

Value after reset: FF_H

	7							0	
TEI2	TEI2							EA	WR (28_H)

TEI2 ... Terminal Endpoint Identifier

In all message transfer modes except in transparent modes 0, 1 and extended transparent mode, TEI2 is used for address recognition. In the case of a two-byte address field, it contains the value of the second programmable Terminal Endpoint Identifier according of the ISDN LAPD-protocol.
In non-auto-modes with one-byte address field, TEI2 is a response address, according to X.25 LAPD.

EA ... Address field Extension bit

This bit is to be set to ’1’ according to HDLC/LAPD.

7.1.17 TMH -Test Mode Register HDLC

Value after reset: 00_H

	7							0	
TMH	0	0	0	0	0	0	0	TLP	RD/WR (29_H)

TLP ... Test Loop

The TX path of layer-2 is internally connected with the RX path of layer-2. Data coming from the layer 1 controller will not be forwarded to the layer 2 controller (see **chapter 3.7**).

Bit 7:1 have always be programmed to ’0’.

7.1.18 CIR0 - Command/Indication Receive 0

Value after reset: $F3_H$

	7				0	
CIR0	CODR0	CIC0	CIC1	S/G	BAS	RD ($2E_H$)

CODR0 ... C/I Code 0 Receive

Value of the received Command/Indication code. A C/I-code is loaded in CODR0 only after being the same in two consecutive IOM-frames and the previous code has been read from CIR0.

CIC0 ... C/I Code 0 Change

A change in the received Command/Indication code has been recognized. This bit is set only when a new code is detected in two consecutive IOM-frames. It is reset by a read of CIR0.

CIC1 ... C/I Code 1 Change

A change in the received Command/Indication code in IOM-channel 1 has been recognized. This bit is set when a new code is detected in one IOM-frame. It is reset by a read of CIR0.

S/G ... Stop/Go Bit Monitoring

Indicates the availability of the D-channel on the line interface.

1: Stop
0: Go

BAS ... Bus Access Status

Indicates the state of the TIC-bus:

0: The SCOUT-DX itself occupies the D- and C/I-channel
1: Another device occupies the D- and C/I-channel

Note: The CODR0 bits are updated every time a new C/I-code is detected in two consecutive IOM-frames. If several consecutive valid new codes are detected and CIR0 is not read, only the first and the last C/I code is made available in CIR0 at the first and second read of that register, respectively.

7.1.19 CIX0 - Command/Indication Transmit 0

Value after reset: FE_H

	7				0	
CIX0	CODX0	TBA2	TBA1	TBA0	BAC	WR ($2E_H$)

CODX0 ... C/I-Code 0 Transmit

Code to be transmitted in the C/I-channel 0.

TBA2-0 ... TIC Bus Address

Defines the individual address for the SCOUT-DX on the IOM bus.

This address is used to access the C/I- and D-channel on the IOM interface.

Note: If only one device is liable to transmit in the C/I- and D-channels of the IOM it should always be given the address value '7'.

BAC ... Bus Access Control

Only valid if the TIC-bus feature is enabled (MODE:DIM2-0).

If this bit is set, the SCOUT-DX will try to access the TIC-bus to occupy the C/I-channel even if no D-channel frame has to be transmitted. It should be reset when the access has been completed to grant a similar access to other devices transmitting in that IOM-channel.

Note: If the TIC-bus address (TBA2-0) is programmed to '7' and is not blocked by another device the SCOUT-DX writes its C/I0 code to IOM continuously.

7.1.20 CIR1 - Command/Indication Receive 1

Value after reset: FC_H

	7			0	
CIR1	CODR1		0	0	RD ($2F_H$)

CODR1 ... C/I-Code 1 Receive

Value of the received Command/Indication code.

7.1.21 CIX1 - Command/Indication Transmit 1

Value after reset: FE_H

	7			0	
CIX1	CODX1		CICW	CI1E	WR ($2F_H$)

CODX1 ... C/I-Code 1 Transmit

Bits 7-2 of C/I-channel 1

CICW ... C/I-Channel Width

CICW selects between a 4 bit ('0') and 6 bit ('1') C/I1 channel width

CI1E ... C/I-channel 1 interrupt enable

Interrupt generation ISTA.CIC of CIR0.CIC1 is enabled (1) or masked (0).

7.2 Transceiver, Interrupt and General Configuration Registers

7.2.1 TR_CONF0 - Transceiver Configuration Register

Value after reset: 00_H

	7							0	
TR_ CONF0	DIS_ TR	0	0	0	L1SW	0	0	LDD	RD/WR (30_H)

DIS_TR ... Disable Transceiver

0: All layer-1 functions are enabled.
1: All layer-1 functions are disabled. The HDLC controller and codec part can still operate via IOM-2. DCL and FSC pins become input.

L1SW ... Enable Layer 1 State Machine in Software

0: Layer 1 state machine of the SCOUT-DX is used
1: Layer 1 state machine is disabled. The functionality can be realized in software. The commands can be written in register TR_CMD and the status read from the TR_STA.

LDD ... Level Detection Discard

0: Clock generation after detection of any signal on the line in the power down state
1: No clock generation after detection of any signal on the line in the power down state

Note: If an interrupt is generated by the internal level detect circuitry, the microcontroller has to set this bit to '0' for an activation of the line interface.

7.2.2 TR_CONF1 - Receiver Configuration Register

Value after reset: 62_H

	7							0	
TR_ CONF1	RPLL_ INTD	1	1	0	0	0	1	0	RD/WR (31_H)

RPLL_INTD ... Receive PLL Integrator Disable (refer to **chapter 5.1.1**)

0: The integrator function of the receive PLL is enabled
1: The integrator function of the receive PLL is disabled

7.2.3 TR_CONF2 - Transmitter Configuration Register

Value after reset: 00_H

	7							0	
TR_ CONF2	DIS_ TX	0	0	0	0	0	RLP	0	RD/WR (32_H)

DIS_TX ... Disable Line Driver

The transmitter of the U_{PN} transceiver can be disabled or enabled by setting DIS_TX. This can be used to make the analog loop (Loop3) transparent (DIS_TX = ’0’) or not (DIS_TX = ’1’).

0: Transmitter is enabled
1: Transmitter is disabled

RLP ... Remote Loop

If the remote loop is closed the data revceived from the line is looped back to the line.

0: Remote loop open
1: Remote loop closed

7.2.4 TR_STA - Transceiver Status Register

Value after reset: 00_H

	7						0	
TR_ STA	RINF	0	RCV	0	FSYN	0	0	RD (33_H)

RINF ... Receiver INFO

00: Received INFO 0
01: Received any signal except INFO 2 or INFO 4
10: Received INFO 2
11: Received INFO 4

RCV ... Received Code Violation

0: No code violation received
1: At least one code violation received

FSYN ... Frame Synchronization State

0: The receiver has not synchronized or has lost synchronization to the framing bit F
1: Thereceiver has synchronized to the framing bit F

7.2.5 TR_CMD - Transceiver Command Register

Value after reset: 00_H

	7					0	
TR_ CMD	XINF	0	0	PD	LP_A	0	RD/WR (34_H)

Normally the signals in this register are generated by the layer 1 state machine. If the internal layer 1 state machine is disabled (bit L1SW in TR_CONF = ’1’) this register can be written by the microcontroller.

XINF ... Transmit INFO

000: Transmit INFO 0
001: Transmit INFO 1W
010: Transmit INFO 1
011: Transmit INFO 3
100: Send continous 192 kHz pulses (Test Mode 2)
101: Send single 4 kHz pulses (Test Mode 1)
11x: reserved

PD ... Power Down

0: Transceiver in operational mode
1: Transceiver in power down mode. From the analog part only the level detector is active. Additionally no clocks are provided and the complete digital part of the transceiver is inactive if the CFS bit (see **chapter 7.2.10**) is set to ’1’.

LP_A ... Loop Analog

The setting of this bit corresponds to the C/I command ARL.

0: Analog loop is open
1: Analog loop is closed

7.2.6 ISTATR - Interrupt Status Register Transceiver

Value after reset: 00_H

	7							0	
ISTATR	0	x	x	x	LD	RIC	0	0	RD (38_H)

For all interrupts in the ISTATR register following logical states are defined:

0: Interrupt is not acitvated
1: Interrupt is acitvated

x ... Reserved

LD ... Level Detection

Any receive signal has been detected on the line

RIC ... Receiver INFO Change

Any bit of register TR_STA has changed. This bit is reset by reading this register

7.2.7 MASKTR - Mask Transceiver Interrupt

Value after reset: $7F_H$

	7							0	
MASKTR	0	1	1	1	LD	RIC	1	1	RD/WR (39_H)

0: The transceiver interrupts LD and RIC are enabled

1: The transceiver interrupts LD and RIC are disabled

7.2.8 ISTA - Interrupt Status Register

Value after reset: 01_H

	7							0	
ISTA	0	ST	CIC	TIN	WOV	TRAN	MOS	HDLC	RD ($3C_H$)

For all interrupts in the ISTA register following logical states are applied:

0: Interrupt is not acitvated
1: Interrupt is acitvated

ST ... Synchronous Transfer

When programmed (STI register), this interrupt is generated to enable the microcontroller to lock on to the IOM timing, for synchronous transfers.

CIC ... C/I Channel Change

A change in C/I channel 0 or C/I channel 1 has been recognized. The actual value can be read from CIR0 or CIR1.

TIN ... Timer Interrupt

The internal timer and repeat counter has expired (see TIMR register).

WOV ... Watchdog Timer Overflow

Used only if terminal specific functions are enabled (MODE.TSF=1).

Signals the expiration of the watchdog timer, which means that the microcontroller has failed to set the watchdog timer control bits WTC1 and WTC2 (ADF1 register) in the correct manner. A reset pulse has been generated by the SCOUT-DX.

TRAN ... Transceiver Interrupt

An interrupt originated in the transceiver interrupt status register (ISTATR) has been recognized.

MOS ... MONITOR Status

A change in the MONITOR Status Register (MOSR) has occured.

HDLC ... HDLC Interrupt

An interrupt originated in the HDLC interrupt sources has been recognized.

Note: A read of the ISTA register clears only the TIN and WOV interrupts. The other interrupts are cleared by reading the corresponding status register

7.2.9 MASK - Mask Register

Value after reset: $7F_H$

	7							0	
MASK	0	ST	CIC	TIN	WOV	TRAN	MOS	HDLC	WR ($3C_H$)

For the MASK register following logical states are applied:

0: Interrupt is not masked
1: Interrupt is masked

Each interrupt source in the ISTA register can be selectively masked by setting to ’1’ the corresponding bit in MASK. Masked interrupt status bits are not indicated when ISTA is read. Instead, they remain internally stored and pending, until the mask bit is reset to ’0’.

Note: In the event of a C/I channel change, CIC is set in ISTA even if the corresponding mask bit in MASK is active, but no interrupt is generated.

7.2.10 MODE1 - Mode1 Register

Value after reset: 00_H

	7						0	
MODE1	MCLK	CDS	WTC1	WTC2	CFS	RSS2	RSS1	RD/WR ($3D_H$)

MCLK ... Master Clock Frequency

The Master Clock Frequency bits control the microcontroller clock output corresponding following table.

Bit 7	Bit 6	MCLK frequency with MODE1.CDS = ’0’	MCLK frequency with MODE1.CDS = ’1’
0	0	3.84 MHz	7.68 MHz
0	1	0.96 MHz	1.92 MHz
1	0	7.68 MHz	15.36 MHz
1	1	disabled	disabled

CDS ... Clock Divider Selection

0: The 15.36 MHz oscillator clock divided by two is input to the MCLK prescaler
1: The 15.36 MHz oscillator clock is input to the MCLK prescaler.

WTC1, 2 ... Watchdog Timer Control 1, 2

If the watchdog timer is enabled (RSS = ’11’) the microcontroller has to program the WTC1 and WTC2 bit within each time period of 128 ms in the following sequence:

		WTC1	WTC2
	1. 2.	1 0	0 1

(See **chapter 6.1**).

CFS ... Configuration Select

This bit determines clock relations and recovery on the line and IOM interfaces

0: The IOM interface clock and frame signals are always active, "Power Down" state included.

The states "Power Down" and "Power Up" are thus functionally identical except for the indication: PD = 1111 and PU = 0111.

With the C/I command Timing (TIM) the microcontroller can enforce the "Power Up" state.

With C/I command Deactivation Indication (DI) the "Power Down" state is reached again.

It is also possible to activate the line Interface directly with the C/I command Activate Request (AR) without the TIM command.

1: The IOM interface clock and frame signals are normally inactive ("Power Down").

For activating the IOM-2 clocks the "Power Up" state can be induced by software (SPU-bit in SPCR register) or by resetting again CFS.

After that the line interface can be activated with the C/I command Activate Request (AR). The "Power Down" state can be reached again with the C/I command Deactivation Indication (DI).

Note: After reset the IOM interface is always active. To reach the "Power Down" state the CFS-bit has to be set.

.RSS2, RSS1 ... Reset Source Selection 2,1

The reset sources and the SDS2 functionality for the $\overline{\text{RSTO}}$/SDS2 output pin can be selected according to the table below.

RSS2 Bit 1	RSS1 Bit 0	C/I Code Change	EAW	Watchdog Timer	SDS2 Functionality
0	0	--	--	--	--
0	1	--	--	--	x
1	0	x	x	--	--
1	1	--	--	x	--

For RSS = ’00’ only a hardware reset generates a reset at pin $\overline{\text{RSTO}}$/SDS2.
For RSS = ’01’ a serial data strobe is output at pin $\overline{\text{RSTO}}$/SDS2 (see **chapter 2.2.3**).
For RSS = ’10’ an External Awake or a change in the downstream C/I0 channel generates a reset of 125 µs ≤ t ≤ 250 µs pulse length at the pin $\overline{\text{RSTO}}$ (see **chapter 6.1**).
For RSS = ’11’ the watchdog function is enabled (see **chapter 6.1**).

After a reset pulse and the corresponding interrupt (WOV or CIC) have been generated by the SCOUT-DX the actual reset source can be read from the ISTA.

7.2.11 MODE2 - Mode2 Register

Value after reset: 00_H

	7							0	
MODE2	0	0	0	0	0	DREF	0	PPSDX	RD/WR ($3E_H$)

PPSDX ... Push/Pull Output for SDX

0: The SDX pin has open drain characteristic
1: The SDX pin has push/pull characteristic

DREF ... Disable References

0: Reference voltages and currents are enabled.
1: Reference voltages and currents are disabled.

7.2.12 ID - Identification Register

Value after reset: $0x_H$

	7							0	
ID	0	0	DESIGN						RD ($3F_H$)

DESIGN ... Design Number

000001: SCOUT-DX V1.1 PSB 21373

7.2.13 SRES - Software Reset Register

Value after reset: 00_H

	7							0	
SRES	0	0	RES_ CPLL	RES_ MON	RES_ HDLC	RES_ IOM	RES_ TR	RES_ CO	WR ($3F_H$)

RES_xx ... Reset_xx

0: Deactivates the reset of the functional block xx
1: Activates the reset of the functional block xx
The reset state is activated as long as the bit is set to ’1’

Meaning of xx:

CPLL: Codec PLL
MON: Monitorhandler
HDLC: HDLC controller,
IOM: IOM Handler,
TR: Transceiver,
CO: Codec

7.3 IOM-2 and MONITOR Handler

7.3.1 CDAxy - Controller Data Access Register xy

Value after reset: See table below

	7	0	
CDAxy	Controller Data Access Register		RD/WR (40_H-43_H)

Data register CDAxy which can be accessed from the controller.

Register	Value after Reset	Register Address
CDA10	FF_H	40_H
CDA11	FF_H	41_H
CDA20	FF_H	42_H
CDA21	FF_H	43_H

7.3.2 XXX_TSDPxy - Time Slot and Data Port Selection for CHxy

Vaule after reset: See table below

	7				0	
XXX_ TSDPxy	DPS	0	0	0	TSS	RD/WR (44_H-$4D_H$)

Register	Value after Reset	Register Address
CDA_TSDP10	00_H (= output on B1-DD)	44_H
CDA_TSDP11	01_H (= output on B2-DD)	45_H
CDA_TSDP20	80_H (= output on B1-DU)	46_H
CDA_TSDP21	81_H (= output on B2-DU)	47_H
CO_TSDP10	80_H (= output on B1-DU)	48_H
CO_TSDP11	81_H (= output on B2-DU)	49_H
CO_TSDP20	81_H (= output on B2-DU)	$4A_H$
CO_TSDP21	85_H (= output on IC2-DU)	$4B_H$
TR_TSDP_B1	00_H (= output on B1-DD)	$4C_H$
TR_TSDP_B2	01_H (= output on B2-DD)	$4D_H$

This register determines the time slots and the data ports on the IOM-2 Interface for the data channels xy of the functional units XXX (Controller Data Access (CDA), Codec (CO) and Transceiver (TR)).

DPS ... Data Port Selection

0: The data channel xy of the functional unit XXX is output on DD.
The data channel xy of the functional unit XXX is input from DU.
1: The data channel xy of the functional unit XXX is output on DU.
The data channel xy of the functional unit XXX is input from DD.

Note: For the CDA (controller data access) data the input is determined by the CDA_CRx.SWAP bit. If SWAP = '0' the input for the CDAxy data is vice versa to the output setting for CDAxy. If the SWAP = '1' the input from CDAx0 is vice versa to the output setting of CDAx1 and the input from CDAx1 is vice versa to the output setting of CDAx0. See controller data access description in chapter 2.2.2.1

TSS ... Timeslot Selection

Selects one of the 12 timeslots from 0...11 on the IOM-2 interface for the data channels.

7.3.3 CDAx_CR - Control Register Controller Data Access CH1x

Value after reset: See table below

	7							0	
CDAx_ CR	0	0	EN_ TBM	EN_I1	EN_I0	EN_O1	EN_O0	SWAP	RD/WR ($4E_H$-$4F_H$)

Register	Value after Reset	Register Address
CDA1_CR	00_H	$4E_H$
CDA2_CR	00_H	$4F_H$

EN_TBM ... Enable TIC Bus Monitoring

0: The TIC bus monitoring is disabled
1: The TIC bus monitoring with the CDAx0 register is enabled. The TSDPx0 register must be set to 08_H for monitoring from DU or 88_H for monitoring from DD respectively.

EN_I1, EN_I0 ... Enable Input CDAx0, CDAx1

0: The input of the CDAx0, CDAx1 register is disabled
1: The input of the CDAx0, CDAx1 register is enabled

EN_O1, EN_O0 ... Enable Output CDAx0, CDAx1

0: The output of the CDAx0, CDAx1 register is disabled
1: The output of the CDAx0, CDAx1 register is enabled

SWAP ... Swap Inputs

0: The time slot and data port for the input of the CDAxy register is defined by its own TSDPxy register. The data port for the CDAxy input is vice versa to the output setting for CDAxy.
1: The input (time slot and data port) of the CDAx0 is defined by the TSDP register of CDAx1 and the input of CDAx1 is defined by the TSDP register of CDAx0. The data port for the CDAx0 input is vice versa to the output setting for CDAx1. The data port for the CDAx1 input is vice versa to the output setting for CDAx0. The input definition for time slot and data port CDAx0 are thus swapped to CDAx1 and for CDAx1 to CDAx0. The outputs are not affected by the SWAP bit.

7.3.4 CO_CR - Control Register Codec Data

Value after reset: 00_H

	7							0	
CO_CR	0	0	0	0	EN 21	EN 20	EN 11	EN 10	RD/WR (50_H)

EN21 **... Enable codec channel 21**
EN20 **... Enable codec channel 20**
EN11 **... Enable codec channel 11**
EN10 **... Enable codec channel 10**

0: The codec data channel xy is disabled
1: The codec data channel xy is enabled

7.3.5 TR_CR - Control Register Transceiver Data

Value after reset: $3E_H$

	7							0	
TR_CR	0	0	EN_ D	EN_ B2R	EN_ B1R	EN_ B2X	EN_ B1X	0	RD/WR (51_H)

EN_D **... Enable D-Channel Data**
EN_B2R **... Enable B2 Data received from IOM**
EN_B1R **... Enable B1 Data received from IOM**
EN_B2X **... Enable B2 Data to be transmitted to IOM**
EN_B1X **... Enable B1 Data to be transmitted to IOM**

0: The transceiver data _xxx is disabled
1: The transceiver data _xxx is enabled

7.3.6 HCI_CR - Control Register for HDLC and CI1 Data

Value after reset: $A0_H$

	7							0	
HCI_CR	DPS_ CI1	EN_ CI1	EN_ D	EN_ B2H	EN_ B1H	0	0	0	RD/WR (52_H)

DPS_CI1 ... Data Port Selection CI1 Data

0: The CI1 data is output on DD and input from DU
1: The CI1 data is output on DU and input from DD

EN_CI1 ... Enable CI1 Data
EN_D ... Enable D-Channel Data
EN_B2H ... Enable HDLC B2 Data
EN_B1H ... Enable HDLC B1 Data

0: The HDLC (D, B1, B2) and CI1 data is disabled
1: The HDLC (D, B1, B2) and CI1 data is enabled

7.3.7 MON_CR - Control Register Monitor Data

Value after reset: 40_H

	7						0	
MON_CR	DPS	EN_ MON	0	0	0	0	MCS	RD/WR (53_H)

DPS ... Data Port Selection

0: The Monitor data is output on DD and input from DU
1: The Monitor data is output on DU and input from DD

EN_MON ... Enable Output

0: The Monitor data input and output is disabled
1: The Monitor data input and output is enabled

MCS ... MONITOR Channel Selection

00: The MONITOR data is output on MON0
01: The MONITOR data is output on MON1
10: The MONITOR data is output on MON2
11: Not defined

7.3.8 SDSx_CR - Control Register Serial Data Strobe x

Value after reset: 00_H

	7				0	
SDSx_CR	ENS_ TSS	ENS_ TSS+1	ENS_ TSS+3	0	TSS	RD/WR (54_H-55_H)

Register	Value after Reset	Register Address
SDS1_CR	00_H	54_H
SDS2_CR	00_H	$55F_H$

Note: The SDS2_CR register is only applicable if a serial data strobe functionality is selected (MODE1.RSS = '01') for the pin $\overline{RSTO}$/SDS2

ENS_TSS ... Enable Serial Data Strobe of timeslot TS
ENS_TSS+1 ... Enable Serial Data Strobe of timeslot TS+1

0: The serial data strobe or bit clock on SDSx for TS, TS+1 is disabled
1: The serial data strobe or bit clock on SDSx for TS, TS+1 is enabled

ENS_TSS+3 ... Enable Serial Data Strobe of timeslot TS+3 (D-Channel)

0: The serial data strobe or bit clock on SDSx for the D-channel (bit7, 6) of TS+3 is disabled
1: The serial data strobe or bit clock on SDSx for the D-channel (bit7, 6) of TS+3 is enabled

TSS ... Timeslot Selection

Selects one of 12 timeslots on the IOM-2 interface (with respect to FSC) during which SDSx is active. The data strobe signal allows standard data devices to access a programmable channel.

7.3.9 IOM_CR - Control Register IOM Data

Value after reset: 00_H

	7							0	
IOM_CR	SPU	0	0	TIC_ DIS	EN_ BCL	CLKM	DIS_ OD	DIS_ IOM	RD/WR (56_H)

SPU ... Software Power UP

0: The DU line is normally used for transmitting data
1: Setting this bit to ’1’ will pull the DU line to low. This will enforce connected layer 1 devices to deliver IOM-clocking.

After a subsequent CIC-interrupt (C/I-code change; ISTA) and reception of the C/I-code ”PU” (Power Up indication in TE-mode) the microcontroller writes an AR or TIM command as C/I-code in the CIX0-register, resets the SPU bit and wait for the following CIC-interrupt.

TIC_DIS ... TIC Bus Disable

0: The last octet of the last IOM time slot (TS 11) is used as TIC bus
1: The TIC bus is disabled. The last octet of the last IOM time slot (TS 11) can be used as every time slot.

EN_BCL ... Enable Bit Clock BCL

0: The BCL clock is disabled
1: The BCL clock is enabled

CLKM ... Clock Mode

If the transceiver is disabled (DIS_TR = ’1’) the DCL from the IOM-2 interface is an input. With

0: A double clock per bit is expected
1: A single clock per bit is expected

DIS_OD ... Open Drain

0: IOM outputs are open drain driver
1: IOM outputs are push pull driver

DIS_IOM ... Disable IOM

DIS_IOM should be set to ’1’ if external devices connected to the IOM interface should be “disconnected“ e.g. for power saving purposes or for not disturbing the internal IOM

connection between layer 1 and layer 2. However, the SCOUT-DX internal operation between transceiver, B-channel and D-channel controller is independent of the DIS_IOM bit.

0: The IOM interface is enabled
1: The IOM interface is disabled (high impedance)

7.3.10 MCDA - Monitoring CDA Bits

Value after reset: FF_H

	7						0		
MCDA	MCDA21		MCDA20		MCDA11		MCDA10		RD (57_H)
	Bit7	Bit6	Bit7	Bit6	Bit7	Bit6	Bit7	Bit6	

MCDAxy ... Monitoring CDAxy Bits

Bit 7 and Bit 6 of the CDAxy registers are mapped into the MCDA register.

This can be used for monitoring the D-channel bits on DU and DD and the 'Echo bits' on the TIC bus with the same register

7.3.11 STI - Synchronous Transfer Interrupt

Value after reset: 00_H

	7							0	
STI	STOV 21	STOV 20	STOV 11	STOV 10	STI 21	STI 20	STI 11	STI 10	RD (58_H)

For all interrupts in the STI register following logical states are applied:

0: Interrupt is not acitvated
1: Interrupt is acitvated

STOVxy ... Synchronous Transfer Overflow Interrupt

Enabled STOV interrupts for a certain STIxy interrupt are generated when the STIxy has not been acknowledged in time via the ACKxy bit in the ASTI register. This must be one (for DPS=’0’) or zero (for DPS=’1’) BCL clocks before the time slot which is selected for the STOV.

STIxy ... Synchronous Transfer Interrupt

Depending on the DPS bit in the corresponding TSDPxy register the Synchronous Transfer Interrupt STIxy is generated two (for DPS=’0’) or one (for DPS=’1’) BCL clock after the selected time slot (TSDPxy.TSS).

Note: ST0Vxy and ACKxy are useful for synchronizing microcontroller accesses and receive/transmit operations. One BCL clock is equivalent to two DCL clocks.

7.3.12 ASTI - Acknowledge Synchronous Transfer Interrupt

Value after reset: 00_H

	7							0	
ASTI	0	0	0	0	ACK 21	ACK 20	ACK 11	ACK 10	WR (58_H)

ACKxy ... Acknowledge Synchronous Transfer Interrupt

After a STIxy interrupt the microcontroller has to acknowledge the interrupt by setting the corresponding ACKxy bit.

0: No activity is initiated
1: Sets the acknowledge bit ACKxy for a STIxy interrupt

7.3.13 MSTI - Mask Synchronous Transfer Interrupt

Value after reset: FF_H

	7							0	
MSTI	STOV 21	STOV 20	STOV 11	STOV 10	STI 21	STI 20	STI 11	STI 10	RD/WR (59_H)

For the MSTI register following logical states are applied:

0: Interrupt is not masked
1: Interrupt is masked

STOVxy ... Synchronous Transfer Overflow for STIxy

By masking the STOV bits the number and time of the STOV interrupts for a certain enabled STIxy interrupt can be controlled. For an enabled STIxy the own STOVxy is generated when the STOVxy is enabled (MSTI.STIxy and MSTI.STOVxy = ’0’). Additionally all other STOV interrupts of which the corresponding STI is disabled (MSTI.STI = ’1’ and MSTI.STOV = ’0’) are generated.

STIxy ... Synchronous Transfer Interrupt xy

The STIxy interrupts can be masked by setting the corresponding mask bit to ’1’. For a masked STIxy no STOV interrupt is generated.

7.3.14 SDS_CONF - Configuration Register for Serial Data Strobes

Value after reset: 00_H

	7							0	
SDS_ CONF	0	0	0	0	0	0	SDS2_ BCL	SDS1_ BCL	RD/WR ($5A_H$)

SDSx_BCL ... Enable IOM Bit Clock for SDSx

0: The serial data strobe is generated in the programmed timeslot (see **chapter 7.3.8**).
1: The IOM bit clock is generated in the programmed timeslot (see **chapter 7.3.8 and 2.2.3**).

7.3.15 MOR - MONITOR Receive Channel

Value after reset: FF_H

	7							0	
MOR									RD ($5C_H$)

Contains the MONITOR data received in the IOM-2 MONITOR channel according to the MONITOR channel protocol. The MONITOR channel (0,1,2) can be selected by setting the monitor channel select bit MON_CR.MCS.

7.3.16 MOX - MONITOR Transmit Channel

Value after reset: FF_H

	7							0	
MOX									WR ($5C_H$)

Contains the MONITOR data to be transmitted in IOM-2 MONITOR channel according to the MONITOR channel protocol.The MONITOR channel (0,1,2) can be selected by setting the monitor channel select bit MON_CR.MCS

7.3.17 MOSR - MONITOR Interrupt Status Register

Value after reset: 00_H

	7							0	
MOSR	MDR	MER	MDA	MAB	0	0	0	0	RD ($5D_H$)

MDR **... MONITOR channel Data Received**

MER **... MONITOR channel End of Reception**

MDA **... MONITOR channel Data Acknowledged**

The remote end has acknowledged the MONITOR byte being transmitted.

MAB **... MONITOR channel Data Abort**

7.3.18 MOCR - MONITOR Control Register

Value after reset: 00_H

	7							0	
MOCR	MRE	MRC	MIE	MXC	0	0	0	0	RD/WR ($5E_H$)

MRE ... MONITOR Receive Interrupt Enable

0: MONITOR interrupt status MDR generation is masked
1: MONITOR interrupt status MDR generation is enabled

MRC ... MR Bit Control:

Determines the value of the MR bit:

0: MR is always ’1’. In addition, the MDR interrupt is blocked, except for the first byte of a packet (if MRE = 1).
1: MR is internally controlled according to the MONITOR channel protocol. In addition, the MDR interrupt is enabled for all received bytes according to the MONITOR channel protocol (if MRE = 1).

MIE ... MONITOR Interrupt Enable

MONITOR interrupt status MER, MDA, MAB generation is enabled (1) or masked (0).

MXC ... MX Bit Control

Determines the value of the MX bit:
0: The MX bit is always ’1’.
1: The MX bit is internally controlled according to the MONITOR channel protocol.

7.3.19 MSTA - MONITOR Status Register

Value after reset: 00_H

	7							0	
MSTA	0	0	0	0	0	MAC	0	TOUT	RD ($5F_H$)

MAC ... MONITOR Transmit Channel Active

The data transmisson in the MONITOR channel is in progress

TOUT ... Time-Out

Read-back value of the TOUT bit

7.3.20 MCONF - MONITOR Configuration Register

Value after reset: 00_H

	7							0	
MCONF	0	0	0	0	0	0	0	TOUT	WR ($5F_H$)

TOUT ... Time-Out

0: The monitor time-out function is disabled
1: The monitor time-out function is enabled

7.4 Codec Configuration Registers

7.4.1 General Configuration Register (GCR)

Value after reset: 00_H

	7							0	
GCR	SP	AGCX	AGCR	MGCR	CME	PU	ATT2R	ATT1R	RD/WR (60_H)

SP ... Speakerphone

0: Speakerphone support disabled
1: Speakerphone support enabled

AGCX ... Automatic Gain Control Transmit

0: Automatic gain control disabled
1: Automatic gain control enabled; only if speakerphone support is enabled (SP=1)

AGCR ... Automatic Gain Control Receive

0: Automatic gain control disabled
1: Automatic gain control enabled; only if speakerphone support is enabled (SP=1)

MGCR ... Modified Gain Control Receive

0: AGCR starts regulation down of the attenuation immediately, regulation up is done after speech was detected two times
1: AGCR starts regulation up and down after speech was detected two times

CME ... Controlled Monitoring Enable (GCR.SP = ’1’)

0: Controlled monitoring disabled
1: Controlled monitoring enabled. ALS attenuation is fixed to the value determined by the ATCR.CMAS setting.

Note: If transmit speech is detected and LSC > -9.5 dB, the ALS programming is fixed to -9.5 dB

PU ... Power Up

0: The codec is in standby mode (power-down); all registers and the coefficient RAM contents are saved and all interface functions are available
1: The codec is in normal operation mode (power-up)

ATT2R ... Attenuation of the Receive Channel related to Transmit Channel 2
ATT1R ... Attenuation of the Receive Channel related to Transmit Channel 1

0: Attenuation value for the conferencing loop is 0 dB

1: Attenuation value for the conferencing loop loaded from CRAM

7.4.2 Programmable Filter Configuration Register (PFCR)

Value after reset: 00_H

	7							0	
PFCR	GX	GR	GZ	FX	PGZ	FR	DHPR	DHPX	RD/WR (61_H)

GX ... Transmit Gain

0: Gain set to 0 dB
1: Gain coefficients loaded from CRAM

GR ... Receive Gain

0: Gain set to 0 dB
1: Gain coefficients loaded from CRAM

GZ ... Sidetone Gain

0: Gain set to $-\infty$ dB
1: Gain coefficients loaded from CRAM

FX ... Transmit Frequency Correction Filter

0: Filter is bypassed
1: Filter coefficients loaded from CRAM

PGZ ... Position Sidetone Gain

0: Tap of the sidetone signal is before the AGC/GHX stage
1: Tap of the sidetone signal is after the AGC/GHX stage

FR ... Receive Frequency Correction Filter

0: Filter is bypassed
1: Filter coefficients loaded from CRAM

DHPR ... Disable High-Pass Receive (50/60 Hz filter)

0: Filter enabled
1: Filter disabled

DHPX ... Disable High-Pass Transmit (50/60 Hz filter)

0: Filter enabled
1: Filter disabled

7.4.3 Tone Generator Configuration Register (TGCR)

Value after reset: 00_H

	7							0	
TGCR	ET	DT	ETF	PT	SEQ	TM	SM	SQTR	RD/WR (62_H)

ET ... Enable Tone Generator

0: Tone generator is disabled
1: Tone generator is enabled; frequency and gain coefficients loaded from CRAM

DT ... Dual Tone Mode

0: Dual tone mode is disabled
1: Dual tone mode is enabled; the output of signal generator FD is added to the tone signal which is determined by TM and SEQ;
dual tone mode is only available if TGSR.DTMF = ’0’

ETF ... Enable Tone Filter

0: Tone filter is by-passed
1: Tone filter is enabled; filter coefficients loaded from CRAM

PT ... Pulsed Tone

0: Pulsed tone is disabled
1: Pulsed tone is enabled; time coefficients loaded from CRAM

SEQ ... Sequence Generator

0: Sequence generator is disabled, a continuous tone signal is generated
1: Sequence generator is enabled; time coefficients loaded from CRAM

TM ... Tone Mode

0: Two-tone sequence is activated when sequence generator is enabled with SEQ = ’1’ otherwise a continuous signal (F1, G1) is generated
1: Three-tone sequence is activated when sequence generator is enabled with SEQ = ’1’ otherwise a continuous signal (F2, G2) is generated;
three-tone sequence is only available if TGSR.DTMF = ’0’

SM ... Stop Mode

0: Automatic stop mode is disabled
1: Automatic stop mode is enabled; two and three tone ring gets turned off after the sequence is completed

SQTR ... Square/Trapezoid Waveform

0: Trapezoid shaped signal is enabled;
only available if tone ringing via loudspeaker is disabled with TGSR.TRL = ’0’
1: Square-wave signal is enabled

7.4.4 Tone Generator Switch Register (TGSR)

Value after reset: 00_H

	7							0	
TGSR	0	TRL	0	TRR	DTMF	TRX	0	0	RD/WR (63_H)

TRL ... Tone Ringing via Loaudspeaker

0: Ringing signal is not output directly to the loadspeaker pins
1: Ringing signal (square) is output directly to the loudspeaker pins LSP/LSN

TRR ... Tone Ringing Receive

0: Tone signal for receive direction is disabled
1: Tone signal for receive direction is enabled

DTMF ... DTMF Mode

0: DTMF mode is disabled
1: DTMF mode is enabled

TRX ... Tone Ringing Transmit

0: Tone generator for transmit direction is disabled
1: Tone generator for transmit direction is enabled

7.4.5 AFE Configuration Register (ACR)

Value after reset: 00_H

	7							0	
ACR	0	ADC	DAC	SEM	DHOP	DHON	DLSP	DLSN	RD/WR (64_H)

ADC ... A/D Control

0: A/D is in power down mode
1: A/D is active

DAC ... D/A Control

0: D/A and POFI are in power down mode
1: D/A and POFI are active

SEM ... Single Ended Mode (only effective if DLSP and/or DLSN='1')

0: LSP and/or LSN amplifiers are in power down and grounded internally for single ended mode
1: LSP and/or LSN amplifiers are in power down (high impedance)

DHOP ... Disable HOP Amplifier

0: HOP amplifier in normal mode
1: Disable HOP amplifier (power down, output high impedance)

DHON ... Disable HON Amplifier

0: HON amplifier in normal mode
1: Disable HON amplifier (power down, output high impedance)

DLSP ... Disable LSP Amplifier

0: LSP amplifier in normal mode
1: Disable LSP amplifier controlled by SEM setting

DLSN ... Disable LSN Amplifier

0: LSN amplifier in normal mode
1: Disable LSN amplifier controlled by SEM setting

7.4.6 AFE Transmit Configuration Register (ATCR)

Value after reset: 00_H

	7			0	
ATCR	MIC	0	CMAS	AIMX	RD/WR (65_H)

MIC **... Microphone Amplifier (AMI) Control**

Bit 7	6	5	4	Selected Mode
0	0	0	0	AMI and PREFI is in **power-down** mode
0	0	0	1	0 dB amplification
0	0	1	0	6 dB amplification
0	0	1	1	12 dB amplification
0	1	0	0	18 dB amplification
0	1	0	1	24 dB amplification
0	1	1	0	30 dB amplification
0	1	1	1	36 dB amplification
1	0	0	0	42 dB amplification
1	1	1	1	**bypass** mode, reserved for internal tests

CMAS **... Controlled Monitoring Attenuation Select**

0: In controlled monitoring mode (GCR.CME = ’1’)
the lower ALS setting is -9.5dB

1: In controlled monitoring mode (GCR.CME = ’1’)
the lower ALS setting is -21.5dB

AIMX **... Analog Input Multiplexer**

Bit 1	0	Selected Input
0	0	AMI is connected to the pins MIP1/MIN1 (differential input)
0	1	AMI is connected to the pins MIP2/MIN2 (differential input)
1	0	AMI is connected to the pin AXI (single-ended input)
1	1	not used

7.4.7 AFE Receive Configuration Register (ARCR)

Value after reset: 00_H

	7	0	
ARCR	HOC	LSC	RD/WR (66_H)

HOC **... Handset Output Amplifier (AHO) Control**

Bit 3	2	1	0	Selected Mode
0	0	0	0	AHO is in **power-down** mode
0	0	0	1	2.5 dB amplification
0	0	1	0	– 0.5 dB amplification
0	0	1	1	– 3.5 dB amplification
0	1	0	0	– 6.5 dB amplification
0	1	0	1	– 9.5 dB amplification
0	1	1	0	– 12.5 dB amplification
0	1	1	1	– 15.5 dB amplification
1	0	0	0	– 18.5 dB amplification
1	0	0	1	– 21.5 dB amplification
1	1	1	1	**bypass** mode, reserved for internal tests only

LSC **... Loudspeaker Amplifier (ALS) Control**

Bit 3	2	1	0	Selected Mode
0	0	0	0	ALS is in **power-down** mode
0	0	0	1	11.5 dB amplification
0	0	1	0	8.5 dB amplification
0	0	1	1	5.5 dB amplification
0	1	0	0	2.5 dB amplification
0	1	0	1	– 0.5 dB amplification
0	1	1	0	– 3.5 dB amplification
0	1	1	1	– 6.5 dB amplification
1	0	0	0	– 9.5 dB amplification
1	0	0	1	– 12.5 dB amplification
1	0	1	0	– 15.5 dB amplification
1	0	1	1	– 18.5 dB amplification
1	1	0	0	– 21.5 dB amplification
1	1	0	1	– 24.5 dB amplification (only for TGSR.TRL = ’1’)
1	1	1	0	– 27.5 dB amplification (only for TGSR.TRL = ’1’)
1	1	1	1	**bypass** mode, reserved for internal tests only

7.4.8 Data Format Register (DFR)

Value after reset: 00_H

	7			0	
DFR	DF2R	DF2X	DF1R	DF1X	RD/WR (67_H)

DFxR **... Data Format CHx Receive (CHxR)**

Bit 7,3	Bit 6,2	Data Format CHxR	Codec Voice Data Register
0	0	PCM A-Law	COx0R
0	1	PCM µ-Law	COx0R
1	0	8-bit linear mode	COx0R (|sign 15...9| of the internal 16 bit word)
1	1	16-bit linear mode	COx0R (MSB) (|sign 15...9| of the internal 16 bit word) COx1R (LSB) (|8...1| of the internal 16 bit word)

DFxX **... Data Format CHx Transmit (CHxX)**

Bit 5,1	Bit 4,0	Data Format CHxR	Codec Data Register
0	0	PCM A-Law	COx0X
0	1	PCM µ-Law	COx0X
1	0	8-bit linear mode	COx0X (|sign 15...9| of the internal 16 bit word)
1	1	16-bit linear mode	COx0X (MSB) (|sign 15...9| of the internal 16 bit word) COx1X (LSB) (|8...1| of the internal 16 bit word)

The small letter 'x' is a variable for channel 2 or 1.

7.4.9 Data Source Selection Register (DSSR)

Value after reset: 00_H

	7				0	
DSSR	DSSR	ENX2	ENX1	DSS2X	DSS1X	RD/WR (68_H)

DSSR ... Data Source Selection Receive

Bit7	6	
0	0	idle
0	1	CH1R
1	0	CH2R
1	1	CH1R+CH2R

ENX2 ... Enable Transmit CH2
ENX1 ... Enable Transmit CH1

0: Codec transmit data in CH2/CH1 disabled
1: Codec transmit data in CH2/CH1 enabled

DSS2X ... Data Source Selection CH2X

Bit3	2	
0	0	idle code is transmitted
0	1	XDAT is transmitted
1	0	CH1R
1	1	XDAT+ CH1R is transmitted

DSS1X ... Data Source Selection CH1X

Bit1	0	
0	0	idle code is transmitted
0	1	XDAT is transmitted
1	0	CH2R
1	1	XDAT+ CH2R is transmitted

7.4.10 Extended Configuration (XCR) and Status (XSR) Register

Extended Status Register (XSR)

If MAAR in the XCR register is set to ’0’:
Value after reset: 00_H

	7						0	
XSR	PGCR	PGCX	ERA	0	0	0	SPST	RD (69_H)

PGCR **... Position of Gain Control Receive** (see **figure 58**)

Read-back of the programmed value

PGCX **... Position of Gain Control Transmit** (see **figure 58**)

Read-back of the programmed value

ERA **... Enhanced Reverse Attenuation**

Read-back of the programmed value

SPST **... Speakerphone State**

Bit 1	0	Description
0	0	Speakerphone is in receive mode
0	1	Speakerphone is in idle mode (reached via receive mode)
1	0	Speakerphone is in transmit mode
1	1	Speakerphone is in idle mode (reached via transmit mode)

If MAAR in the XCR register is set to ’1’:

Value after reset: 00_H

	7	0	
XSR	Value of the Momentary AGC Attenuation		RD (69_H)

Extended Configuration Register (XCR)

Value after reset: 00_H

	7						0		
XCR	PGCR	PGCX	ERA	0	0	0	0	MAAR	WR (69_H)

PGCR **... Position of Gain Control Receive** (see **figure 58**)

0: In front of the speech detector
1: Behind the speech detector

PGCX **... Position of Gain Control Transmit** (see **figure 58**)

0: Behind the speech detector
1: In front of the speech detector

ERA **... Enhanced Reverse Attenuation**

0: Standard reverse attenuation in receive direction
1: Enhanced reverse attenuation in receive direction

MAAR **... Monitoring AGC Attenuation Receive**

0: The monitoring of the AGC attenuation receive in the XSR register is disabled. XSR contains the read-back values of XCR register (bit 7:2) and the speakerphone states.
1: The monitoring of the AGC attenuation receive in the XSR register is enabled. The momentory AGC attenuation can be accessed directly by the microcontroller via XSR register.

7.4.11 Mask Channel x Register (MASKxR)

Value after reset: 00_H

	7	0	
MASKxR	MASKx	MPx	RD/WR

channel 1: $6A_H$
channel 2: $6B_H$

MASKx ... Mask Channel x

The codec data in channel 1 (CH1X, CH1R) or channel 2 (CH2X,CH2R) respectively is masked with these 6 register bits. The position of this 6 bit mask on the 8 or 16 bit value respectively is determined by the MPx bits. If a mask bit is set to ’1’ the data in the corresponding bit position is masked and thus always a ’1’. With a ’0’ the data passes unchanged.

MPx ... Mask Position of Channel x

Bit 1	0	Description
0	0	Bit 5...0 of the codec data register CHx0 is masked with MASKx
0	1	Bit 7...2 of the codec data register CHx0 is masked with MASKx
1	0	Bit 5...0 of the codec data register CHx1 is masked with MASKx
1	1	Bit 7...2 of the codec data register CHx1 is masked with MASKx

7.4.12 Test Function Configuration Register (TFCR)

Value after reset: 00_H

	7			0	
TFCR	0	0	ALTF	DLTF	RD/WR ($6C_H$)

ALTF **... Analog Loop** and **Test Functions**

Bit 5	4	3	Test Function
0	0	0	NOT: No Test Mode
0	0	1	ALF: Analog Loop via Front End
0	1	0	ALC: Analog Loop via Converter
0	1	1	ALN: Analog Loop via Noise Shaper
1	X	X	*Reserved*

DLTF **... Digital Loop** and **Test Functions**

Bit 2	1	0	Test Function
0	0	0	NOT: No Test Mode
0	0	1	IDR: Initialize DRAM
0	1	0	DLN: Digital Loop via Noise Shaper
0	1	1	DLS: Digital Loop via Signal Processor
1	0	0	DLP1: Digital Loop via codec part CH1
1	0	1	DLP2: Digital Loop via codec part CH2
1	1	X	*Reserved*

7.4.13 CRAM Control (CCR) and Status (CSR) Register

The programming of the CRAM Control Register (CCR) and the CRAM Status Register (CSR) is intended for a back-up procedure for the direct access to individual CRAM coefficients. A detailed description can be found in **chapter 4.8.2.1**.

CRAM Status Register (CSR)

Value after reset: 00_H

	7				0	
CCR	0	0	DCA	BSYB	CBADR	RD ($6F_H$)

DCA ... DSP CRAM Access

Read-back of the programmed value

BSYB ... Busy Back-up Procedure

0: Momentary there is no transfer of CRAM data to the temporary area running. CRAM access via microcontroller interface is possible
1: Transfer of the CRAM block <CBADR> is running. CRAM access via microcontroller interface is not allowed

CBADR ... CRAM Block Address

Read-back of the programmed value

CRAM Control Register (CCR)

Value after reset: 00_H

	7				0	
CCR	0	0	DCA	SBP	CBADR	WR ($6F_H$)

DCA ... DSP CRAM Access

0: The normal CRAM area (80_H tp FF_H) is accessed by the codec DSP
1: The temporary CRAM area (coefficient block with 8 bytes corresponding to the COP_x sequences) is accessed by the codec DSP. The switching to the temporary CRAM block happens as soon as the transfer of the block has completed (BSYB = ’0’)

SBP ... Start Back-up Procedure

0: No back-up is initiated
1: A transition to SBP = ’1’ starts the back-up of the CRAM block <CBADR> into the temporary CRAM area

CBADR ... CRAM Block Address

Address of a coefficient block with 8 bytes corresponding to the COP_x sequences (x=0...F) of the codec programming sequences

7.4.14 CRAM (Coefficient RAM)

Address	Mnemonic	Description
80_H	-	*Reserved*
81_H	-	*Reserved*
82_H	T1	Beat tone time lower byte
83_H		Beat tone time higher byte
84_H	GD1	Trapezoid generator amplitude
85_H	G1	Tone generator amplitude
86_H	F1	Tone generator frequency lower byte
87_H		Tone generator frequency higher byte
88_H	GTX	Level adjustment for transmit path
89_H	GTR	Level adjustment for receive path
$8A_H$	T2	Beat tone time span lower byte
$8B_H$		Beat tone time span higher byte
$8C_H$	GD2	Trapezoid generator amplitude
$8D_H$	G2	Tone generator amplitude
$8E_H$	F2	Tone generator frequency lower byte
$8F_H$		Tone generator frequency higher byte
90_H	FD	Dual tone frequency lower byte
91_H		Dual tone frequency higher byte
92_H	T3	Beat tone time span lower byte
93_H		Beat tone time span higher byte
94_H	GD3	Trapezoid generator amplitude
95_H	G3	Tone generator amplitude
96_H	F3	Tone generator frequency lower byte
97_H		Tone generator frequency higher byte
98_H	GE	Saturation amplification
99_H	A2	Bandwidth
$9A_H$	A1	Center frequency
$9B_H$	K	Attenuation of the stop-band
$9C_H$	-	*Reserved*
$9D_H$	-	*Reserved*
$9E_H$	-	*Reserved*
$9F_H$	-	*Reserved*

Address	Mnemonic	Description
$A0_H$	TOFF	Turn-off period of the tone generator lower byte
$A1_H$		Turn-off period of the tone generator higher byte
$A2_H$	TON	Turn-on period of the tone generator lower byte
$A3_H$		Turn-on period of the tone generator higher byte
$A4_H$	-	*Reserved*
$A5_H$	-	*Reserved*
$A6_H$	-	*Reserved*
$A7_H$	-	*Reserved*
$A8_H$	-	*Reserved*
$A9_H$	-	*Reserved*
AA_H	ATT2R	Conferencing attenuation CH2R
AB_H	ATT1R	Conferencing attenuation CH1R
AC_H	GR	Receive gain lower byte
AD_H		Receive gain higher byte
AE_H	GX	Transmit gain lower byte
AF_H		Transmit gain higher byte
$B0_H$	-	*Reserved*
$B1_H$	-	*Reserved*
$B2_H$	GZ	Sidetone gain lower byte
$B3_H$		Sidetone gain higher byte
$B4_H$	-	*Reserved*
$B5_H$	-	*Reserved*
$B6_H$	-	*Reserved*
$B7_H$	-	*Reserved*
$B8_H$	FX	Transmit correction filter coefficients part 8
$B9_H$		Transmit correction filter coefficients part 7
BA_H		Transmit correction filter coefficients part 6
BB_H		Transmit correction filter coefficients part 5
BC_H		Transmit correction filter coefficients part 4
BD_H		Transmit correction filter coefficients part 3
BE_H		Transmit correction filter coefficients part 2
BF_H		Transmit correction filter coefficients part 1
$C0_H$	FR	Receive correction filter coefficients part 12
$C1_H$		Receive correction filter coefficients part 11
$C2_H$		Receive correction filter coefficients part 10
$C3_H$		Receive correction filter coefficients part 9
$C4_H$	FX	Transmit correction filter coefficients part 12
$C5_H$		Transmit correction filter coefficients part 11
$C6_H$		Transmit correction filter coefficients part 10
$C7_H$		Transmit correction filter coefficients part 9

Address	Mnemonic	Description
$C8_H$	FR	Receive correction filter coefficients 8
$C9_H$		Receive correction filter coefficients 7
CA_H		Receive correction filter coefficients 6
CB_H		Receive correction filter coefficients 5
CC_H		Receive correction filter coefficients 4
CD_H		Receive correction filter coefficients 3
CE_H		Receive correction filter coefficients 2
CF_H		Receive correction filter coefficients 1
$D0_H$	SW	Switching time
$D1_H$	DS	Decay speed
$D2_H$	TW	Wait time
$D3_H$	ETLE	Echo time (line side)
$D4_H$	ETAE	Echo time (acoustic side)
$D5_H$	ATT	Attenuation programmed in GHR or GHX
$D6_H$	GLE	Gain of line echo
$D7_H$	GAE	Gain of acoustic echo
$D8_H$	PDNLE	Peak decrement when noise is detected (line side)
$D9_H$	GDNLE	Reserve when noise is detected (line side)
DA_H	PDSLE	Peak decrement when speech is detected (line side)
DB_H	GDSLE	Reserve when speech is detected (line side)
DC_H	PDNAE	Peak decrement when noise is detected (acoustic side)
DD_H	GDNAE	Reserve when noise is detected (acoustic side)
DE_H	PDSAE	Peak decrement when speech is detected (acoustic side)
DF_H	GDSAE	Reserve when speech is detected (acoustic side)
$E0_H$	-	*Reserved*
$E1_H$	LP1R	Time constant LP1 (receive)
$E2_H$	LP1X	Time constant LP1 (transmit)
$E3_H$	LP2LR	Limitation for LP2 (receive)
$E4_H$	LP2LX	Limitation for LP2 (transmit)
$E5_H$	OFFR	Level offset up to detected noise (receive)
$E6_H$	OFFX	Level offset up to detected noise (transmit)
$E7_H$	LIM	Starting level of the logarithmic amplifiers
$E8_H$	LP2NR	Time constant LP2 for noise (receive)
$E9_H$	LP2SR	Time constant LP2 for signal (receive)
EA_H	PDNR	Time constant PD for noise (receive)
EB_H	PDSR	Time constant PD for signal (receive)
EC_H	LP2NX	Time constant LP2 for noise (transmit)
ED_H	LP2SX	Time constant LP2 for signal (transmit)
EE_H	PDNX	Time constant PD for noise (transmit)
EF_H	PDSX	Time constant PD for signal (transmit)

Address	Mnemonic	Description
$F0_H$	AGIX	Initial AGC gain transmit
$F1_H$	NOISX	Threshold for AGC-reduction by background noise
$F2_H$	TMLX	Settling time constant for lower levels
$F3_H$	TMHX	Settling time constant for higher levels
$F4_H$	AGX	Gain range of automatic control
$F5_H$	AAX	Attenuation range of automatic control
$F6_H$	COMX	Compare level rel. to max. PCM-value
$F7_H$	LGAX	Loudness gain adjustment
$F8_H$	AGIR	Initial AGC attenuation/gain receive
$F9_H$	NOISR	Threshold for AGC-reduction by background noise
FA_H	TMLR	Settling time constant for lower levels
FB_H	TMHR	Settling time constant for higher lower levels
FC_H	AGR	Gain range of automatic control
FD_H	AAR	Attenuation range of automatic control
FE_H	COMR	Compare level rel. to max. PCM-value
FF_H	LGAR	Loudness gain adjustment

8 Electrical Characteristics

8.1 Electrical Characteristics (general)

8.1.1 Absolute Maximum Ratings

Parameter	Symbol	Limit Values		Unit
		min.	max.	
Storage temperature	T_{STG}	– 65	150	°C
Input/output voltage on any pin with respect to ground	V_S	– 0.3	V_{DD} + 0.3	V
Maximum voltage on any pin with respect to ground	V_{max}		7	V

Note: Stresses above those listed here may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.
Maximum ratings are absolute ratings; exceeding only one of these values may cause irreversible damage to the integrated circuit.

8.1.2 DC-Characteristics

V_{DD} **= 5 V** ± **5 %**, VSS = 0 V; T_A = 0 to 70 °C

Parameter	Symbol	Limit Values			Unit	Test Condition
		min.	typ.	max.		
H-input level (except pin XTAL1)	V_{IH}	2.0		V_{DD} + 0.3	V	
L-input level (except pin XTAL1)	V_{IL}	– 0.3		0.8	V	
H-output level (except pin XTAL2, DU, DD)	V_{OH}	2.4			V	I_O = -400 µA
L-output level (except pin XTAL2, DU, DD)	V_{OL}			0.45	V	I_O = 2 mA
L-output level (pins DU,DD)	V_{OL}			0.45	V	I_O = 7 mA
H-input level (pin XTAL1)	V_{IH}	V_{DD}-0.5		V_{DD}	V	

8.1.2 DC-Characteristics (cont'd)

V_{DD} **= 5 V** ± **5 %**, VSS = 0 V; T_A = 0 to 70 °C

Parameter	Symbol	Limit Values			Unit	Test Condition
		min.	typ.	max.		
L-input level (pin XTAL1)	V_{IL}	0		0.4	V	
Input leakage current Output leakage current (all pins except SX1,2,SR1,2,XTAL1,2 BGREF, V_{ref})	I_{LI} I_{LO}	-1 -1		1 1	µA µA	$0V < V_{IN} < V_{DD}$ $0V < V_{OUT} < V_{DD}$

8.1.3 Capacitances

V_{DD} **= 5 V** ± **5 %**, VSS = 0 V; T_A = 0 to 70 °C; f_C = 1 MHz; unmeasured pins grounded.

Table 25

Parameter	Symbol	Limit Values		Unit	Remarks
		min.	max.		
Input Capacitance I/O Capacitance	C_{IN} $C_{I/O}$		7 7	pF pF	All pins except LIa and LIb
Output Capacitance against V_{SS}	C_{OUT}		25	pF	pins LIa, LIb
Load Capacitance	C_L		60	pF	pins XTAL1,2

8.1.4 Oscillator Specification

Recommended Oscillator Circuit

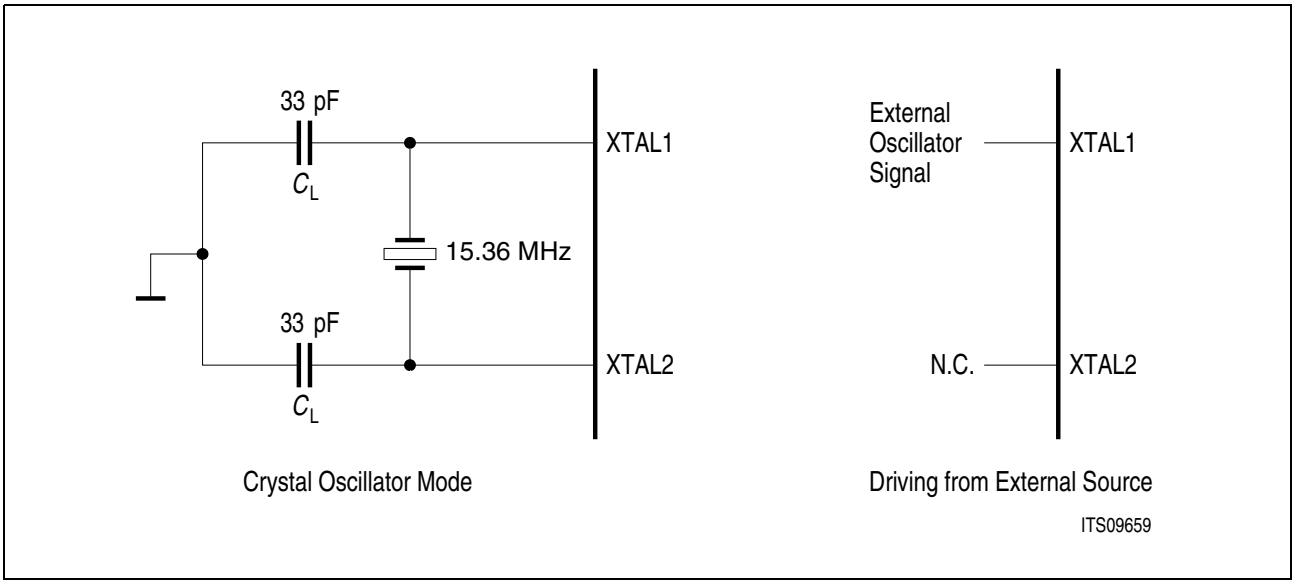

Figure 77
Oscillator Circuit

Crystal Specification

Parameter	Symbol	Limit Values	Unit
Frequency	f	15.36	MHz
Frequency calibration tolerance		max. 100	ppm
Load capacitance	C_L	max. 40	pF
Oscillator mode		fundamental	
Resistance	R1	max. 50	Ω

Note: The load capacitance C_L depends on the recommendation of the crystal specification. Typical values for C_L are 22...33 pF.

XTAL1 Clock Characteristics (external oscillator input)

Parameter	Limit Values	
	min.	max.
Duty cycle	2:3	3:2

8.1.5 AC Characteristics

V_{DD} **= 5 V** ± **5 %**, VSS = 0 V; T_A = 0 to 70 °C

Inputs are driven to 2.4 V for a logical "1" and to 0.45 V for a logical "0". Timing measurements are made at 2.0 V for a logical "1" and 0.8 V for a logical "0". The AC testing input/output waveforms are shown in **figure 78.**

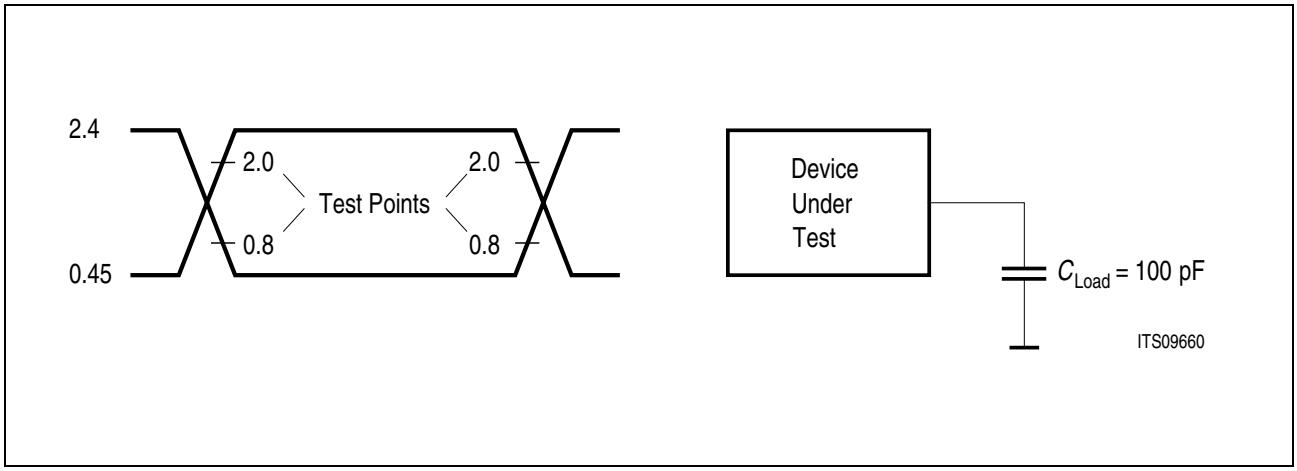

Figure 78
Input/Output Waveform for AC Tests

8.1.6 IOM-2 Interface Timing

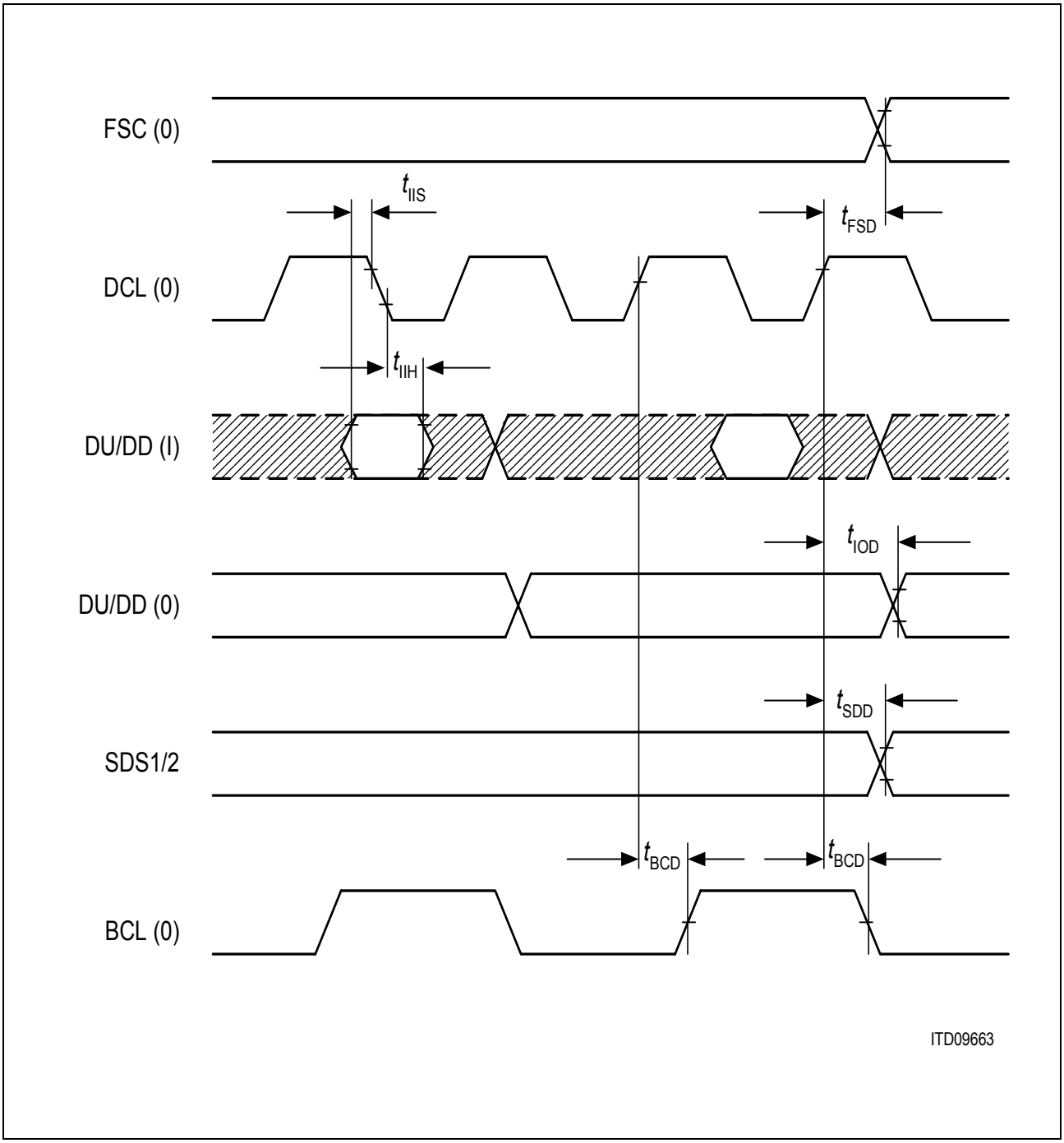

Figure 79
IOM® Timing

Parameter	Symbol	Limit Values			Unit
		min.	typ.	max.	
IOM output data delay	t_{IOD}			100	ns
IOM input data setup	t_{IIS}	20			ns
IOM input data hold	t_{IIH}	20			ns
FSC strobe delay	t_{FSD}		-130		ns
Strobe signal delay	t_{SDD}			120	ns
BCL / FSC delay	t_{BCD}			100	ns
Frame sync setup	t_{FSS}	50			ns
Frame sync hold	t_{FSH}	30			ns
Frame sync width	t_{FSW}	40			ns

DCL Clock Characteristics

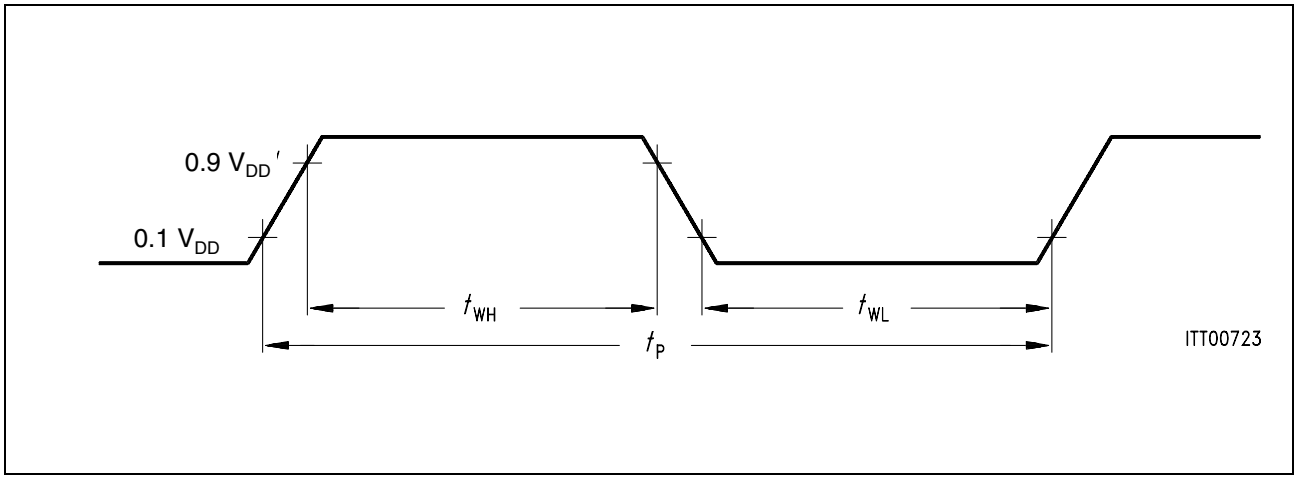

Figure 80
Definition of Clock Period and Width

Symbol	Limit Values			Unit	Test Condition
	min.	typ.	max.		
t_{PO}	585	651	717	ns	osc ± 100 ppm
t_{WHO}	260	325	391	ns	osc ± 100 ppm
t_{WLO}	260	325	391	ns	osc ± 100 ppm

8.1.7 Microcontroller Interface Timing

8.1.7.1 Serial Control Interface (SCI) Timing

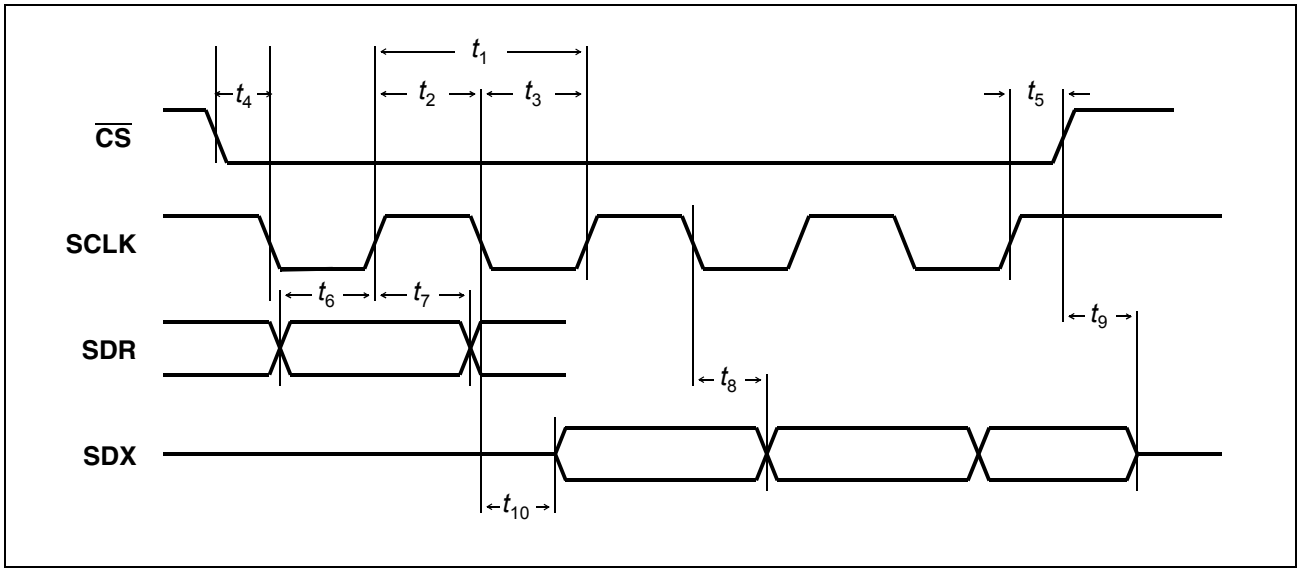

Figure 81
SCI Interface

Parameter SCI Interface	Symbol	Limit values		Unit
		Min	Max	
SCLK cycle time	t_1	500		ns
SCLK high time	t_2	100		ns
SCLK low time	t_3	100		ns
$\overline{CS}$ setup time	t_4	0		ns
$\overline{CS}$ hold time	t_5	10		ns
SDR setup time	t_6	40		ns
SDR hold time	t_7	40		ns
SDX data out delay	t_8		80	ns
$\overline{CS}$ high to SDX tristate	t_9		40	ns
SCLK to SDX active	t_{10}		80	ns

8.1.8 Reset

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Table 26
Reset Signal Characteristics

Parameter	Symbol	Limit Values	Unit	Test Conditions
		min.		
Length of active low state	$t_{\overline{RST}}$	4	ms	Power On/Power Down to Power Up (Standby)
		2 x DCL clock cycles		During Power Up (Standby)

8.2 Electrical Characteristics (Transceiver)

DC Characteristics

V_{DD} **= 5 V** ± **5 %** , VSS = 0 V; T_A = 0 to 70 °C

Parameter	Symbol	Limit Values			Unit	Test Condition
		min.	typ.	max.		
Power supply current-power-up (after reset)	I_{DUAR}		6.5		mA	
Power supply current-power down	I_{DPD}		1.4		mA	
Power supply current-Tranceiver active, sending continous pulses	I_{DTCP}		21.5		mA	280 Ω load on the line
Power supply current-codec powered up	I_{DCPU}		9.5		mA	
Power supply current-tone generation active (single tone generated)	I_{DTG}		97.5		mA	-18.5 dB amplification 50 Ω load
Absolute value of output pulse amplitude $\lvert V_{LIa} - V_{LIb} \rvert$	Vx		1.82		V	280 Ω load on the line

DC Characterisics

V_{DD} **= 5V** ± **5 %**, VSS = 0 V; T_A = 0 to 70 °C

Parameter	Symbol	Limit Values			Unit	Test Condition
		min.	typ.	max.		
Power supply current-Power Down	I_{PD}			400	µA	Inputs at V_{SS} / V_{DD} No output loads except LIa, LIb (50Ω) Codec disabled

DC Characteristics

V_{DD} **= 5 V** ± **5 %**, VSS = 0 V; T_A = 0 to 70 °C

Parameter	Symbol	Limit Values		Unit	Test Condition	Remarks
		min	max			
Transmitter output impedance	Z_X		30	W	I_{OUT} = 6.5 mA	LIa, LIb
Receiver input impedance	Z_R	40		kΩ	Transmitter inactive	LIa, LIb single ended

8.3 Electrical Characteristics (Codec)

8.3.1 DC Characterisics

V_{DD} **= 5 V** ± **5 %**, VSS = 0 V; T_A = 0 to 70 °C

Parameter	Symbol	Limit Values			Unit	Test Condition
		min.	typ.	max.		
Power supply current in Emergency Ringing Mode (AFE)	I_{TR}		12		mA	f_{TR} = 400 Hz square wave; A_{LS} = -3.5d B
Handset Mode (AFE)	I_{HS}		13		mA	
Speakerphone Mode (AFE)	I_{SP}		14		mA	
Loudhearing Mode (AFE)	I_{LH}		16		mA	

Note: ***Values are target values***
Operating power dissipation is measured with all analog outputs open.
All analog inputs are set to VREF.
The digital input signal (pin DD) is set to an idle code.

Transmission Characteristics

V_{DD} **= 5 V** ± **5 %**, VSS = 0 V; T_A = 0 to 70 °C

Parameter	Limit Values		Unit	Test Condition
	min.	max.		
Overall programming range (With specified transmission characteristics)	– 21.5 – 21.5 0 0	11.5 2.5 36 24	dB dB dB dB	Receive: loudspeaker earpiece Transmit: differential inputs single ended input
Programmable AFE gain	– 0.5 – 1.0	0.5 1.0	dB dB	step accuracy overall accuracy

Transmission Characteristics (cont'd)
V_{DD} **= 5 V** ± **5 %**, VSS = 0 V; T_A = 0 to 70 °C

Parameter	Limit Values		Unit	Test Condition
	min.	max.		
Attenuation Distortion @ 0 dBm0	0 – 0.25 – 0.25 – 0.25 – 0.25 0	 0.25 0.45 0.9 	dB dB dB dB dB dB	< 200 Hz 200 – 300 Hz 300 – 2400 Hz 2400 – 3000 Hz 3000 – 3400 Hz > 3400 Hz
Out-of-band signals		 – 35 – 45 – 45 – 65 – 35 – 40	 dB dB dB dB dB dB	receive (TGSR.ERA=0): 4.6 kHz 8.0 kHz receive(TGSR.ERA=1): 4.6 kHz 8.0 kHz transmit: 4.6 kHz 8.0 kHz
Group delay distortion @ 0 dBm0 [1)]		 750 380 130 750	 µs µs µs µs	TGSR.ERA=0 500 – 600 Hz 600 – 1000 Hz 1000 – 2600 Hz 2600 – 2800 Hz
Signal-to-total distortion (method 2, sinewave 1kHz)	35 29 24		dB dB dB	0 to – 30 dBm0 – 40 dBm0 – 45 dBm0
Gain tracking (method 2) @ – 10 dBm0	– 0.3 – 0.6 – 1.6	0.3 0.6 1.6	dB dB dB	3 to – 40 dBm0 – 40 to – 50 dBm0 – 50 to – 55 dBm0
Idle-channel noise		– 75 – 66	dBm0 dBm0	receive (A-Law; Psoph.) transmit (A-Law; Psoph.)
Cross-talk		– 66	dB	Reference: 0 dBm0

[1)] Delay measurements include delays through the A/D and D/A with all features filters FX, GX, FR and GR disabled.

8.3.2 Analog Front End Input Characteristics

V_{DD} **= 5 V** ± **5 %**, VSS = 0 V; T_A = 0 to 70 °C

Parameter	Symbol	Limit Values			Unit	Test Condition
		min.	typ	max.		
AMI-input impedance	Z_{AMI}	12.5	15		kΩ	300 – 3400 Hz
AMI-input voltage swing with specified transmisson characterisics	V_{AMI}			38	mVp	36 dB; V_{DD} = 5 V
	V_{AMI_dif}			2.4	Vp	differential; 0 dB; V_{DD} = 5 V
	V_{AMI_single}			1.67	Vp	single ended; 0 dB; V_{DD} = 5 V

8.3.3 Analog Front End Output Characteristics

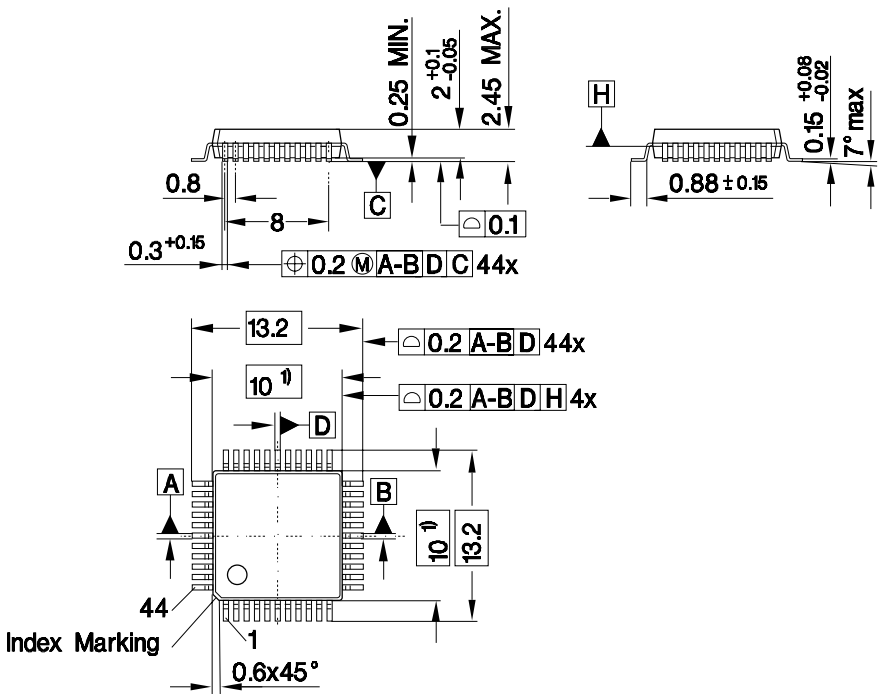
V_{DD} **= 5 V** ± **5 %**, VSS = 0 V; T_A = 0 to 70 °C

AHO-output impedance	Z_{AHO}			2	Ω	300 – 3400 Hz
ALS-output impedance	Z_{ALS}			2	Ω	300 – 3400 Hz
V_{REF} output impedance	Z_{VREF}		7	10	Ω	Load measured from V_{REF} to V_{SSA}
V_{REF} output voltage	V_{VREF}	2.25	2.4	2.55	V	I_{VREF} = – 2 mA
BGREF output impedance	Z_{BGREF}	200	300	400	kΩ	
AHO-output voltage swing	V_{AHO}			3.2	Vpk	Load (200 Ω) measured from HOP to HON
ALS-output voltage swing	V_{ALS}			3.2	Vpk	Load (50 Ω) measured from LSP to LSN

The maximum output voltage swing corresponds to the maximum incoming PCM-code (± 127)

9 Package Outlines

P-MQFP-44-1
(Plastic Metric Quad Flat Package)



1) Does not include plastic or metal protrusion of 0.25 max. per side

gpm05622

Figure 82
Package Dimensions

You can find all of our packages, sorts of packing and others in our Infineon Internet Page “Products”: http://www.infineon.com/products.

SMD = Surface Mounted Device

Dimensions in mm

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Dr. Ulrich Schumacher

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