THE DATASHEET OF

PM7545FPCZ

12-Bit Buffered Multiplying CMOS D/A Converters

PM-7545/PM-7645

FEATURES

- **Preadjusted Full Scale ..... ±1 LSB Maximum Gain Error**
- **Low Gain Temperature Coefficient ..... 2ppm/°C**
- **Small 20-Pin 0.3" Wide DIP**
- **PM-7545 TTL Compatible for V_{DD} = 5V**
- **PM-7645 TTL and 5V CMOS Compatible for V_{DD} = 15V**
- **High ESD Resistance**
- **Available in Die Form**

ORDERING INFORMATION †

MAXIMUM GAIN ERROR T_A = +25°C	PACKAGE: 20-PIN MILITARY* TEMPERATURE −55°C to +125°C	EXTENDED INDUSTRIAL TEMPERATURE −40°C to +85°C	COMMERCIAL TEMPERATURE 0°C to +70°C
±1 LSB	PM7545AR	PM7545ER	PM7545GP
±3 LSB	PM7545BR	PM7545FR	–
±3 LSB	PM7545BRC/883	PM7545FP	–
±3 LSB	–	PM7545FPC	–
±3 LSB	–	PM7545FS	–
±1 LSB	PM7645AR	PM7645ER	PM7645GP
±3 LSB	PM7645BR	PM7645FR	–
±3 LSB	–	PM7645FP	–
±3 LSB	–	PM7645FPC	–
±3 LSB	–	PM7645FS	–

* For devices processed in total compliance to MIL-STD-883, add /883 after part number. Consult factory for 883 data sheet.

† Burn-in is available on commercial and industrial temperature range parts in CerDIP, plastic DIP, and TO-can packages.

CROSS REFERENCE

PMI	ADI	TEMPERATURE RANGE
PM7545AR	AD7545GUD	MILITARY
PM7545BR	AD7545UD	
PM7545BR	AD754TD	
PM7545BR	AD7545SD	
PM7545ER	AD7545GCQ	INDUSTRIAL
PM7545FR	AD7545CQ	
PM7545FR	AD7545BQ	
PM7545FR	AD7545AQ	
PM7545GP	AD7545GLN	COMMERCIAL
PM7545FP	AD7545LN	
PM7545FP	AD7545KN	
PM7545FP	AD7545JN	
PM7545FPC	AD7545KP	

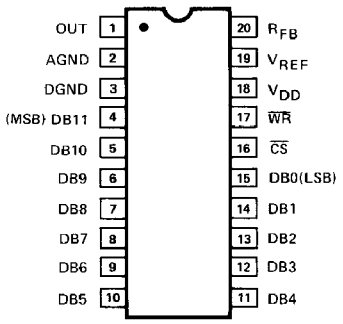
GENERAL DESCRIPTION

The PM-7545/PM-7645 are 12-bit CMOS multiplying DACs with internal data latches. Digital data is input in a 12-bit wide data format, while $\overline{CS}$ and $\overline{WR}$ control inputs are active low. During this time the latches are transparent allowing digital inputs direct connection to the DAC. When $\overline{WR}$ is returned to logic high, the current data word in the latch is saved.

REV. C

The PM-7545 operates from 5 to 15 volt power supplies, offering TTL logic compatibility at V_{DD} of 5V and CMOS logic compatibility at V_{DD} of 15V. The PM-7645 is specified for operation at V_{DD} of 15V, offering TTL logic input compatibility.

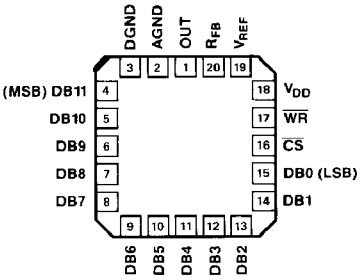
PIN CONNECTIONS



20-PIN EPOXY DIP (P-Suffix)

20-PIN HERMETIC DIP (R-Suffix)

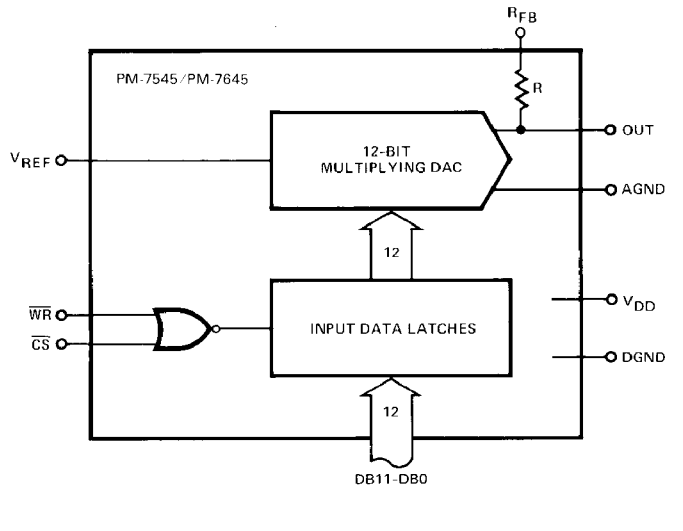
20-PIN SOL (S-Suffix)



20-CONTACT PLCC (PC-Suffix)

20-CONTACT LCC (RC-Suffix)

FUNCTIONAL DIAGRAM



One Technology Way, P.O. Box 9106, Norwood, MA 02062-9106, U.S.A.
Tel: 617/329-4700 Fax: 617/326-8703 Twx: 710/394-6577
Telex: 924491 Cable: ANALOG NORWOODMASS

ABSOLUTE MAXIMUM RATINGS (T_A = +25°C, unless otherwise noted.)

V_{DD} to DGND ..... −0.3, +17V
Digital Input Voltage to DGND ..... −0.3, V_{DD}
AGND to DGND ..... −0.3, V_{DD}
V_{RFB}, V_{REF} to DGND ..... ±25V
$V_{PIN\ 1}$ to DGND ..... −0.3, V_{DD}
Operating Temperature Range
Military (AR, BR) Grades ..... −55°C to +125°C
Industrial (ER, FR, FP, FPC, FS) Grades .... −40°C to +85°C
Commercial (GP) Grade ..... 0°C to +70°C
Junction Temperature ..... +150°C
Storage Temperature .....−65°C to +150°C
Lead Temperature (Soldering, 60 sec) ..... +300°C

PACKAGE TYPE	Θ_{jA} (Note 1)	Θ_{jC}	UNITS
20-Pin Hermetic DIP (R)	76	11	°C/W
20-Pin Plastic DIP (P)	69	27	°C/W
20-Contact LCC (RC, TC)	88	33	°C/W
20-Pin SOL (S)	88	25	°C/W
20-Contact PLCC (PC)	73	33	°C/W

NOTE:
1. Θ_{jA} is specified for worst case mounting conditions, i.e., Θ_{jA} is specified for device in socket for CerDIP, P-DIP, and LCC packages; Θ_{jA} is specified for device soldered to printed circuit board for SOL and PLCC packages.

CAUTION:
1. Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation at or above this specification is not implied. Exposure to above maximum rating conditions for extended periods may affect device reliability.
2. Do not apply voltages higher than V_{DD} or less than GND potential on any terminal except V_{REF}.
3. The digital inputs are zener protected, however, permanent damage may occur on unprotected units from high-energy electrostatic fields. Keep units in conductive foam at all times until ready to use. Use proper antistatic handling procedures.
4. Remove power before inserting or removing units from their sockets.

ELECTRICAL CHARACTERISTICS at V_{DD} = +5V, V_{REF} = +10V, V_{OUT} = 0V, AGND = DGND = 0V; T_A = −55°C to +125°C apply for PM-7545AR/BR; T_A = −40°C to +85°C apply for PM-7545ER/FR/FP/FPC/FS; T_A = 0°C to +70°C apply for PM-7545GP, unless otherwise noted. 15V operating characteristics are shown on the following pages.

			PM-7545A/E/G			PM-7545B/F			
PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	MIN	TYP	MAX	UNITS
STATIC ACCURACY									
Resolution	N		12	—	—	12	—	—	Bits
Relative Accuracy	INL	T_A = Full Temp. Range	—	—	±1/2	—	—	±1/2	LSB
Differential Nonlinearity	DNL	T_A = Full Temp. Range (Note 1)	—	—	±1	—	—	±1	LSB
Gain Error (Notes 2, 3)	G_{FSE}	T_A = +25°C	—	—	±1	—	—	±3	LSB
		T_A = Full Temp. Range	—	—	±2	—	—	±4	
Gain Temperature Coefficient ΔGain/ΔTemperature	TCG_{FS}	(Note 4)	—	±2	±5	—	±2	±5	ppm/°C
DC Supply Rejection ΔGain/ΔV_{DD}	PSS	T_A = +25°C (ΔV_{DD} = ±5%)	—	—	0.002	—	—	0.002	%/%
		T_A = Full Temp. Range (ΔV_{DD} = ±5%)	—	—	0.004	—	—	0.004	
Output Leakage Current at OUT	I_{LKG}	T_A = +25°C, $\overline{WR}$ = $\overline{CS}$ = 0V, All Digital Inputs = 0V	—	—	10	—	—	10	nA
		T_A = Full Temp. Range							
		A/B Versions	—	—	200	—	—	200	
		E/F/G/H Versions	—	—	50	—	—	50	
DYNAMIC PERFORMANCE									
Propagation Delay (Notes 4, 5, 6, 7)	t_{pD}	T_A = +25°C	—	—	300	—	—	300	ns
		(OUT Load = 100Ω, C_{EXT} = 13pF)	—	—	—	—	—	—	
Current Settling Time	t_s	T_A = Full Temp. Range (To 1/2 LSB) (Note 4) I_{OUT} Load = 100Ω	—	—	1	—	—	1	μs
Digital Charge Injection	Q	T_A = +25°C	—	—	300	—	—	300	nVs
		T_A = Full Temp. Range	—	—	400	—	—	400	
		V_{REF} = AGND (Note 4)							
AC Feedthrough at I_{OUT}	FT	T_A = Full Temp. Range V_{REF} = ±10V, f = 10kHz All Digital Inputs = 0V	—	5	—	—	5	—	mV_{p-p}

ELECTRICAL CHARACTERISTICS at V_{DD} = +5V, V_{REF} = +10V, V_{OUT} = 0V, AGND = DGND = 0V; T_A = –55°C to +125°C apply for PM-7545AR/BR; T_A = –40°C to +85°C apply for PM-7545ER/FR/FP/FPC/FS; T_A = 0°C to +70°C apply for PM-7545GP, unless otherwise noted. 15V operating characteristics are shown on the following pages. *Continued*

PARAMETER	SYMBOL	CONDITIONS	PM-7545A/E/G MIN	PM-7545A/E/G TYP	PM-7545A/E/G MAX	PM-7545B/F MIN	PM-7545B/F TYP	PM-7545B/F MAX	UNITS
REFERENCE INPUT									
Input Resistance (Pin 19 to GND)	R_{REF}	T_A = Full Temp. Range Input Resistance	7	11	15	7	11	15	kΩ
ANALOG OUTPUTS									
Output Capacitance (Note 4)	C_{OUT}	T_A = Full Temp. Range DB0-DB11 = 0V, $\overline{WR}$ = $\overline{CS}$ = 0V	—	—	70	—	—	70	pF
C_{OUT}		DB0-DB11 = V_{DD}, $\overline{WR}$ = $\overline{CS}$ = 0V	—	—	150	—	—	150	
DIGITAL INPUTS									
Input High Voltage	V_{INH}	T_A = Full Temp. Range	2.4	—	—	2.4	—	—	V
Input Low Voltage	V_{INL}		—	—	0.8	—	—	0.8	
Input Current	I_{IN}	T_A = +25°C	—	—	1	—	—	1	μA
		T_A = Full Temp. Range	—	—	10	—	—	10	
Input Capacitance DB0-DB11, $\overline{WR}$, $\overline{CS}$	C_{IN}	T_A = Full Temp. Range V_{IN} = 0 (Note 4)	—	—	8	—	—	8	pF
SWITCHING CHARACTERISTICS (Notes 4, 8, 9)		See Timing Diagram							
Chip Select to Write Setup Time	t_{CS}	T_A = +25°C	280	200	—	280	200	—	ns
		T_A = Full Temp. Range	380	270	—	380	270	—	
Chip Select to Write Hold Time	t_{CH}	T_A = Full Temp. Range	0	—	—	0	—	—	ns
Write Pulse Width	t_{WR}	T_A = +25°C	250	175	—	250	175	—	ns
		T_A = Full Temp. Range	380	270	—	380	270	—	
Data Setup Time	t_{DS}	T_A = +25°C	140	100	—	140	100	—	ns
		T_A = Full Temp. Range	210	150	—	210	150	—	
Data Hold Time	t_{DH}	T_A = Full Temp. Range	10	—	—	10	—	—	ns
POWER SUPPLY									
Supply Current	I_{DD}	T_A = Full Temp. Range (All Digital Inputs V_{INL} or V_{INH})	—	—	2	—	—	2	mA
	I_{DD}	T_A = +25°C	—	2	100	—	2	100	μA
		T_A = Full Temp. Range (All Digital Inputs 0V or V_{DD})	—	5	100	—	5	100	

NOTES:

1. 12-bit monotonic over full temperature range.
2. Includes the effects of 5ppm max. gain T.C.
3. Using internal R_{FB}. DAC register loaded with 1111 1111 1111. Gain error is adjustable using the circuits of Figures 4 and 5.
4. GUARANTEED and NOT TESTED.
5. From digital input change to 90% of final analog output.
6. All digital inputs = 0V to V_{DD}; or V_{DD} to 0V.
7. Logic inputs are MOS gates, typical input current (at +25°C) is less than 1nA.
8. Sample tested at +25°C to ensure compliance.
9. Chip select $\overline{CS}$ must be coincident or present before and/or after write WR; that is, $t_{CS} \geq t_{WR}$, $t_{CH} \geq 0$.

ELECTRICAL CHARACTERISTICS at V_{DD} = +15V, V_{REF} = +10V, V_{OUT} = 0V, AGND = DGND = 0V; T_A = –55°C to +125°C apply for PM-7545/PM-7645AR/BR; T_A = –40°C to +85°C apply for PM-7545/PM-7645ER/FR/FP/FPC/FS; T_A = 0°C to +70°C apply for PM-7545/PM-7645GP, unless otherwise noted.

			PM-7545A/E/G PM-7645A/E/G			PM-7545B/F PM-7645B/F			
PARAMETER	**SYMBOL**	**CONDITIONS**	**MIN**	**TYP**	**MAX**	**MIN**	**TYP**	**MAX**	**UNITS**
STATIC ACCURACY									
Resolution	N		12	—	—	12	—	—	Bits
Relative Accuracy	INL	T_A = Full Temp. Range	—	—	±1/2	—	—	±1/2	LSB
Differential Nonlinearity	DNL	T_A = Full Temp. Range (Note 1)	—	—	±1	—	—	±1	LSB
Gain Error (Notes 2, 3)	G_{FSE}	T_A = +25°C T_A = Full Temp. Range	— —	— —	±1 ±2	— —	— —	±3 ±4	LSB
Gain Temperature Coefficient ΔGain/ΔTemperature	TCG_{FS}	(Note 4)	—	±2	±5	—	±2	±5	ppm/°C
DC Supply Rejection ΔGain/ΔV_{DD}	PSS	T_A = +25°C T_A = Full Temp. Range (ΔV_{DD} = ±5%)	— —	— —	0.002 0.004	— —	— —	0.002 0.004	%/%
Output Leakage Current at OUT	I_{LKG}	T_A = +25°C, $\overline{WR}$ = $\overline{CS}$ = 0V, All Digital Inputs = 0V	—	—	10	—	—	10	nA
		T_A = Full Temp. Range A/B Versions E/F/G/H Versions	— —	— —	200 50	— —	— —	200 50	
DYNAMIC PERFORMANCE									
Propagation Delay (Notes 4, 5, 6, 7)	t_{pD}	T_A = +25°C (OUT Load = 100Ω, C_{EXT} = 13pF)	—	—	250	—	—	250	ns
Current Settling Time	t_s	T_A = Full Temp. Range (To 1/2 LSB) (Note 4) I_{OUT} Load = 100Ω	—	—	1	—	—	1	μs
Digital Charge Injection	Q	T_A = +25°C T_A = Full Temp. Range V_{REF} = AGND (Note 4)	— —	— —	250 300	— —	— —	250 300	nVs
AC Feedthrough at I_{OUT}	FT	T_A = Full Temp. Range V_{REF} = ±10V, f = 10kHz All Digital Inputs = 0V	—	5	—	—	5	—	mV_{p-p}
REFERENCE INPUT									
Input Resistance (Pin 19 to GND)	R_{REF}	T_A = Full Temp. Range Input Resistance	7	11	15	7	11	15	kΩ
ANALOG OUTPUTS									
Output Capacitance (Note 4) C_{OUT}	C_{OUT}	T_A = Full Temp. Range DB0-DB11 = 0V, $\overline{WR}$ = $\overline{CS}$ = 0V DB0-DB11 = V_{DD}, $\overline{WR}$ = $\overline{CS}$ = 0V	— —	— —	60 120	— —	— —	60 120	pF
DIGITAL INPUTS									
Input High Voltage Input Low Voltage	V_{INH} V_{INL}	T_A = Full Temp. Range, PM-7545	13.5 —	— —	— 1.5	13.5 —	— —	— 1.5	V
Input High Voltage Input Low Voltage	V_{INH} V_{INL}	T_A = Full Temp. Range, PM-7645	2.4 —	— —	— 0.8	2.4 —	— —	— 0.8	V
Input Current	I_{IN}	T_A = +25°C T_A = Full Temp. Range	— —	— —	1 10	— —	— —	1 10	μA
Input Capacitance DB0—DB11, $\overline{WR}$, $\overline{CS}$	C_{IN}	T_A = Full Temp. Range V_{IN} = 0 (Note 4)	—	—	8	—	—	8	pF

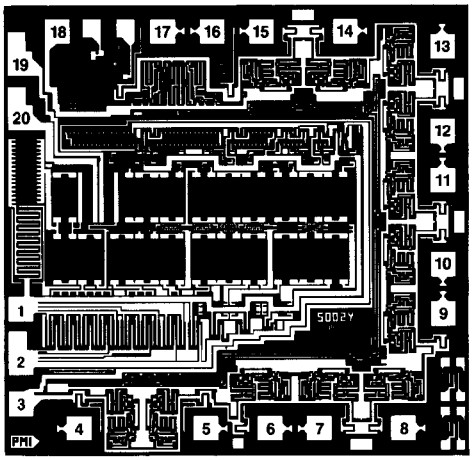
ELECTRICAL CHARACTERISTICS at V_{DD} = +15V, V_{REF} = +10V, V_{OUT} = 0V, AGND = DGND = 0V; T_A = –55°C to +125°C apply for PM-7545/PM-7645AR/BR; T_A = –40°C to +85°C apply for PM-7545/PM-7645ER/FR/FP/FPC/FS; T_A = 0°C to +70°C apply for PM-7545/PM-7645GP, unless otherwise noted. *Continued*

PARAMETER	SYMBOL	CONDITIONS	PM-7545A/E/G PM-7645A/E/G MIN	TYP	MAX	PM-7545B/F PM-7645B/F MIN	TYP	MAX	UNITS
POWER SUPPLY									
Supply Current	I_{DD}	T_A = Full Temp. Range (All Digital Inputs V_{INL} or V_{INH})	—	—	2	—	—	2	mA
	I_{DD}	T_A = +25°C	—	2	100	—	2	100	µA
		T_A = Full Temp. Range (All Digital Inputs 0V or V_{DD})	—	5	100	—	5	100	
SWITCHING CHARACTERISTICS (Notes 4, 8, 9)		See Timing Diagram	**PM-7545 A/E/G**			**PM-7545 B/F/H**			
Chip Select to Write Setup Time	t_{CS}	T_A = +25°C	180	120	—	180	120	—	ns
		T_A = Full Temp. Range	200	150	—	200	150	—	
Chip Select to Write Hold Time	t_{CH}	T_A = Full Temp. Range	0	—	—	0	—	—	ns
Write Pulse Width	t_{WR}	T_A = +25°C	160	100	—	160	100	—	ns
		T_A = Full Temp. Range	240	170	—	240	170	—	
Data Setup Time	t_{DS}	T_A = +25°C	90	60	—	90	60	—	ns
		T_A = Full Temp. Range	120	80	—	120	80	—	
Data Hold Time	t_{DH}	T_A = Full Temp. Range	10	—	—	10	—	—	ns
SWITCHING CHARACTERISTICS (Notes 4, 8, 9)		See Timing Diagram	**PM-7645 A/E/G**			**PM-7645 B/F/H**			
Chip Select to Write Setup Time	t_{CS}	T_A = +25°C	150	—	—	150	—	—	ns
		T_A = Full Temp. Range	210	—	—	210	—	—	
Chip Select to Write Hold Time	t_{CH}	T_A = Full Temp. Range	0	—	—	0	—	—	ns
Write Pulse Width	t_{WR}	T_A = +25°C	150	—	—	150	—	—	ns
		T_A = Full Temp. Range	210	—	—	210	—	—	
Data Setup Time	t_{DS}	T_A = +25°C	225	—	—	225	—	—	ns
		T_A = Full Temp. Range	300	—	—	300	—	—	
Data Hold Time	t_{DH}	T_A = Full Temp. Range	10	—	—	10	—	—	ns

NOTES:

1. 12-bit monotonic over full temperature range.
2. Includes the effects of 5ppm max. gain T.C.
3. Using internal R_{FB}. DAC register loaded with 1111 1111 1111. Gain error is adjustable using the circuits of Figures 4 and 5.
4. GUARANTEED and NOT TESTED.
5. From digital input change to 90% of final analog output.
6. All digital inputs = 0V to V_{DD}, or V_{DD} to 0V.
7. Logic inputs are MOS gates, typical input current (at +25°C) is less than 1nA.
8. Sample tested at +25°C to ensure compliance.
9. Chip select $\overline{CS}$ must be coincident or present before and/or after write $\overline{WR}$; that is, $t_{CS} \geq t_{WR}$, $t_{CH} \geq 0$.

DICE CHARACTERISTICS



DIE SIZE 0.102 × 0.100 inch, 10,200 sq. mils
(2.59 × 2.54mm, 6.58 sq. mm)

1. OUT
2. AGND
3. DGND
4. DB11 (MSB)
5. DB10
6. DB9
7. DB8
8. DB7
9. DB6
10. DB5
11. DB4
12. DB3
13. DB2
14. DB1
15. DB0 (LSB)
16. $\overline{CS}$
17. $\overline{WR}$
18. V_{DD}
19. V_{REF}
20. R_{FB}

WAFER TEST LIMITS at $T_A = 25°C$, $V_{DD} = +5$ or $+15V$, $V_{REF} = +10V$, $V_{OUT} = 0V$, AGND = DGND = 0V.

PARAMETER	SYMBOL	CONDITIONS	PM-7545G/PM-7645G LIMIT	UNITS
Relative Accuracy	INL	Endpoint Linearity Error	±1/2	LSB MAX
Differential Nonlinearity	DNL		±1/2	LSB MAX
Gain Error	G_{FSE}	DAC Latches Loaded with 1111 1111 1111	±5	LSB MAX
Output Leakage	I_{LKG}	DAC Latches Loaded with 0000 0000 0000 Pad 1	±10	nA MAX
Input Resistance	R_{REF}	Pad 19	7/15	kΩ MIN/kΩ MAX
Digital Input High	V_{INH}	$V_{DD} = 5V$ PM-7545 only $V_{DD} = 15V$	2.4 13.5	V MIN
Digital Input Low	V_{INL}	$V_{DD} = 5V$ PM-7545 only $V_{DD} = 15V$	0.8 1.5	V MAX
Digital Input High	V_{INH}	$V_{DD} = 15V$ PM-7645 only	2.4	V MIN
Digital Input Low	V_{INL}	$V_{DD} = 15V$ PM-7645 only	0.8	V MAX
Input Current	I_{IN}	$V_{IN} = 0V$ or V_{DD}	±1	μA MAX
Supply Current	I_{DD}	All Digital Inputs V_{INL} or V_{INH} All Digital Inputs 0V or V_{DD}	2 0.1	mA MAX
DC Supply Rejection ($\Delta Gain/\Delta V_{DD}$)	PSS	$\Delta V_{DD} = \pm 5\%$	0.002	%/% MAX

NOTE:
Electrical tests are performed at wafer probe to the limits shown. Due to variations in assembly methods and normal yield loss, yield after packaging is not guaranteed for standard product dice. Consult factory to negotiate specifications based on dice lot qualification through sample lot assembly and testing.

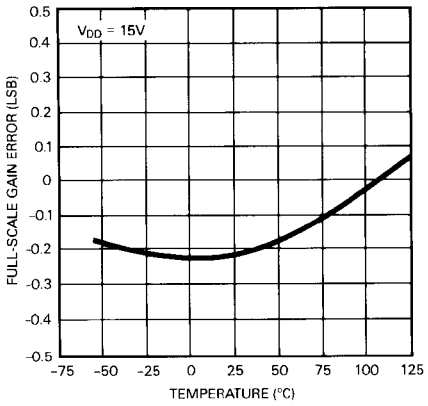
TYPICAL ELECTRICAL CHARACTERISTICS at V_{DD} = +5V or +15V, AGND = DGND = 0V, V_{REF} = +10V, OUT = 0V; T_A = 25°C, unless otherwise noted. (Note 1)

PARAMETER	SYMBOL	CONDITIONS	PM-7545G/PM-7645G TYPICAL	UNITS
Digital Input Capacitance	C_{IN}		7	pF
Output Capacitance	C_{OUT}	DAC Latches Loaded with 0000 0000 0000	50	pF
		DAC Latches Loaded with 1111 1111 1111	110	
Propagation Delay (Notes 2, 3, 4)	t_{pD}	V_{DD} = 15V	140	ns
		V_{DD} = 5V PM-7545 only	230	

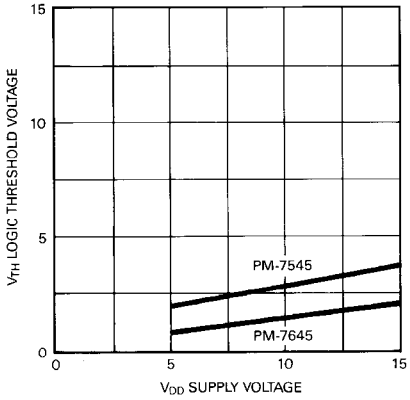
NOTES:
1. These characteristics are for design guidance only and are not subject to test.
2. From digital input change to 90% of final analog output.
3. OUT load = 100Ω, C_{EXT} = 13pF.
4. $\overline{CS}$ = $\overline{WR}$ = 0, DB0 to DB11 = 0V to V_{DD} or V_{DD} to 0V.

TYPICAL PERFORMANCE CHARACTERISTICS

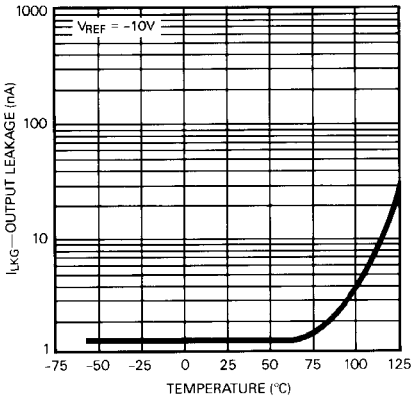
FULL-SCALE GAIN ERROR vs TEMPERATURE



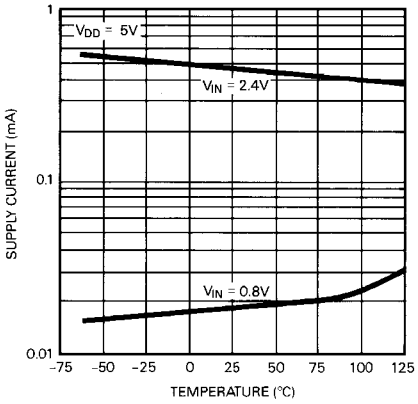
LOGIC THRESHOLD VOLTAGE vs SUPPLY VOLTAGE



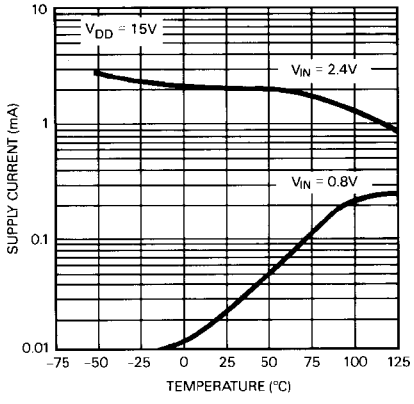
OUTPUT LEAKAGE CURRENT vs TEMPERATURE



SUPPLY CURRENT vs TEMPERATURE PM-7545



SUPPLY CURRENT vs TEMPERATURE PM-7645



PARAMETER DEFINITIONS

RELATIVE ACCURACY

Sometimes referred to as endpoint nonlinearity, and is a measure of the maximum deviation from a straight line passing through the endpoints of the DAC transfer function. Relative Accuracy is measured after the zero and full-scale points have been adjusted, and is normally expressed in LSB or as a percentage of full scale.

DIFFERENTIAL NONLINEARITY

This is the difference between the measured change and the ideal change between any two adjacent codes. A differential nonlinearity of ±1 LSB maximum over the full operating temperature range will ensure that a device is monotonic (the output will increase for an increase in digital code applied).

GAIN ERROR

Gain or full scale error is the amount of output error between the ideal output and the actual output. The ideal output is V_{REF} minus 1 LSB. The gain error is adjustable to zero using external resistance.

OUTPUT CAPACITANCE

The capacitance from OUT to AGND.

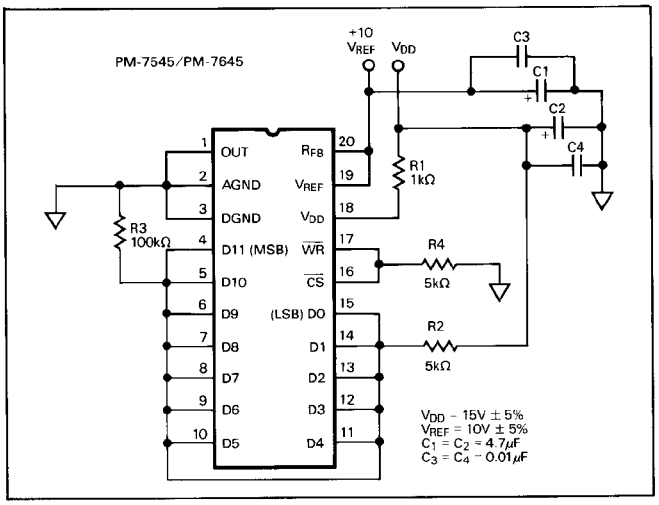
PROPAGATION DELAY

This is measured from the digital input change to the analog output current reaching 90% of its final value.

DIGITAL CHARGE INJECTION

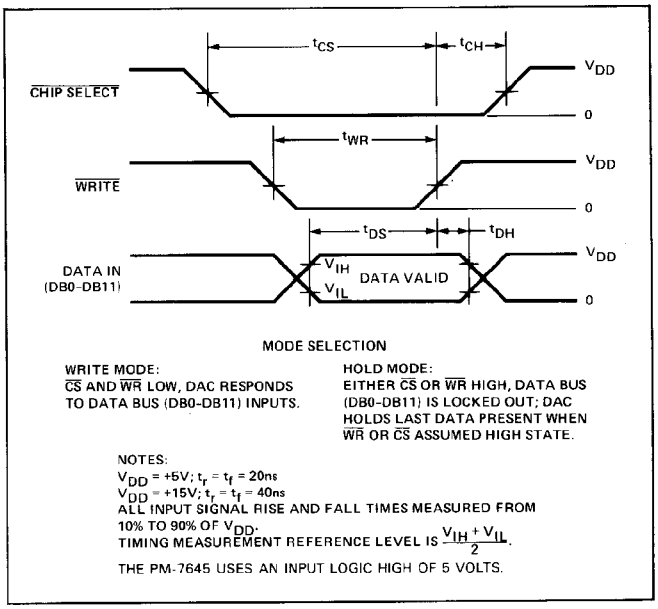
This is a measure of the amount of charge injected to the analog output from the digital inputs, when the digital inputs change states. It is the area of the glitch and is specified in nVsec; it is measured with V_{REF} = AGND.

BURN-IN CIRCUIT



LOGIC INFORMATION

WRITE CYCLE TIMING DIAGRAM



D/A CONVERTER SECTION

FIGURE 1: Simplified D/A Circuit of PM-7545

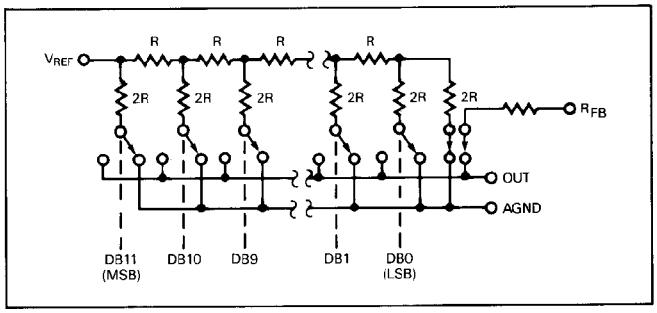


Figure 1 shows a simplified circuit of the D/A Converter section and Figure 2 gives an approximate equivalent switch circuit. R is typically 11kΩ.

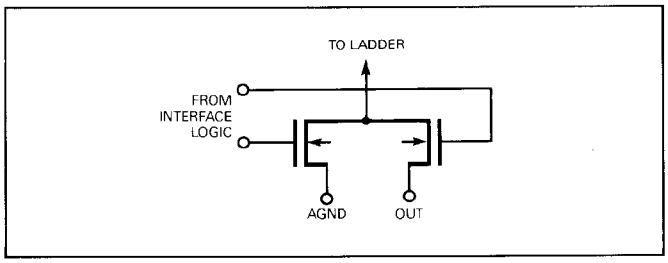
The binary-weighted currents are switched between OUT and AGND by N-channel switches, thus maintaining a constant current in each ladder leg independent of the switch state.

The capacitance at the OUT terminal, C_{OUT}, is code dependent and varies from 70pF (all switches to AGND) to 150pF (all switches to OUT). One of the current switches is shown in Figure 2.

The input resistance at V_{REF} (Figure 1) is always equal to R_{LDR} (R_{LDR} is the R/2R ladder characteristics resistance and is equal to value "R"). Since the input resistance at the V_{REF} pin is constant, the reference terminal can be driven by a reference voltage or a reference current, ac or dc, of positive or negative polarity. (If a current source is used, a low-temperature-coefficient external R_{FB} is recommended to define scale factor.)

The internal feedback resistor (R_{FB}) has a normally closed switch in series as shown in Figure 1. This switch improves performance over temperature and power supply rejection; however when the circuit is not powered up the switch assumes an open state.

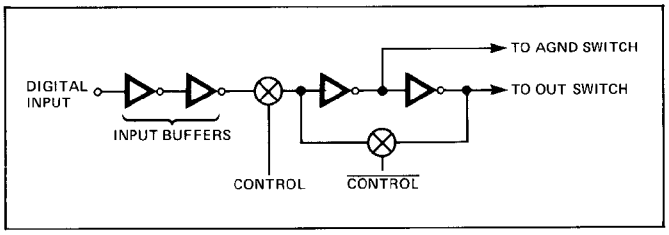
FIGURE 2: N-Channel Current Steering Switch



DIGITAL SECTION

Figure 3 shows the digital structure for one bit. The digital signals CONTROL and $\overline{\text{CONTROL}}$ are generated from $\overline{\text{CS}}$ and $\overline{\text{WR}}$.

FIGURE 3: Digital Input Structure



The input buffers are simple CMOS inverters designed such that when the PM-7545 is operated with V_{DD} = 5V, the buffers convert TTL input levels (2.4V and 0.8V) into CMOS logic levels. When the digital input is in the region of 1.0 volts to 6.0 volts, the input buffers operate in their linear region and draw current from the power supply. To minimize power supply currents, it is recommended that the digital input voltages be as close to the supply rails (V_{DD} and DGND) as is practically possible. The PM-7545 may be operated with any supply voltage in the range $5 \leq V_{DD} \leq 15$ volts. With V_{DD} = +15V, the input logic levels are CMOS compatible only, i.e., 1.5V and 13.5V. The PM-7645 operates with V_{DD} = 15V only; the buffers convert TTL input levels (2.4V and 0.8V) into CMOS logic levels.

BASIC APPLICATIONS

Figures 4 and 5 show simple unipolar and bipolar circuits using the PM-7545/PM-7645. Resistor R1 is used to trim for full scale. The following versions (PM-7545AR, PM-7545ER, PM-7545GP) have a guaranteed maximum gain error of ±1 LSB at +25° C and V_{DD} = +5V, and in many applications the gain trim resistors are not required. Capacitor C1 provides phase compensation and helps prevent overshoot and ringing when using high speed op amps. The circuits of Figures 4 and 5 have constant input impedance at the V_{REF} terminal.

The circuit of Figure 4 can either be used as a fixed reference D/A converter so that it provides an analog output voltage in the range 0 to $-V_{IN}$ (the inversion is introduced by the op amp); or V_{IN} can be an ac signal in which case the circuit behaves as an attenuator (2-Quadrant Multiplier). V_{IN} can be any voltage in the range $-20 \leq V_{IN} \leq +20$ volts (provided the op amp can handle such voltages) since V_{REF} is permitted to exceed V_{DD}. Table 2 shows the code relationship for the circuit of Figure 4.

FIGURE 4: Unipolar Binary Operation

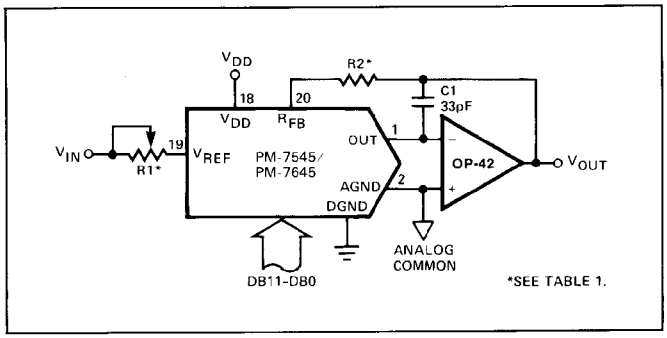


TABLE I: Recommended Trim Resistor Value vs. Grades

TRIM RESISTOR	CR	HP/FR/BR	GP/ER/AR
R1	200Ω	100Ω	20Ω
R2	68Ω	33Ω	6.8Ω

TABLE II: Unipolar Binary Code Table for Circuit of Figure 4

BINARY NUMBER IN DAC REGISTER			ANALOG OUTPUT
1111	1111	1111	$-V_{IN} \cdot \left\{ \frac{4095}{4096} \right\}$
1000	0000	0000	$-V_{IN} \cdot \left\{ \frac{2048}{4096} \right\} = -1/2V_{IN}$
0000	0000	0001	$-V_{IN} \cdot \left\{ \frac{1}{4096} \right\}$
0000	0000	0000	0 Volts

Figure 5 and Table 3 illustrate the recommended circuit and code relationship for bipolar operation. The D/A function itself uses offset binary code. The inverter U_1 on the MSB line, converts 2's-complement input code to offset binary code. The inverter U_1 may be omitted if the inversion is done in software.

R3, R4 and R5 must match within 0.01% and should be the same type of resistors (preferably wire-wound or metal foil), so that their temperature coefficients match. Mismatch of R3 value to R4 causes both offset and full scale error. Mismatch of R5 to R4 and R3 causes full scale error.

TABLE III: 2's Complement Code Table for Circuit of Figure 5

DATA INPUT			ANALOG OUTPUT
0111	1111	1111	$+V_{IN} \cdot \left\{ \frac{2047}{2048} \right\}$
0000	0000	0001	$+V_{IN} \cdot \left\{ \frac{1}{2048} \right\}$
0000	0000	0000	0 Volts
1111	1111	1111	$-V_{IN} \cdot \left\{ \frac{1}{2048} \right\}$
1000	0000	0000	$-V_{IN} \cdot \left\{ \frac{2048}{2048} \right\}$

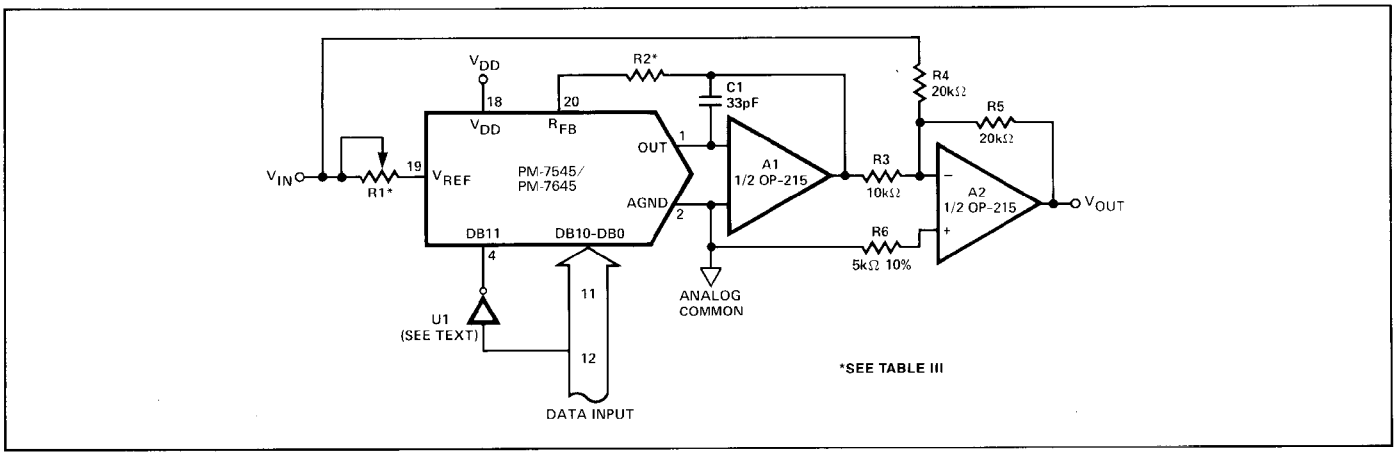
APPLICATION HINTS

Output Offset: CMOS D/A converters exhibit a code-dependent output resistance that causes a code-dependent error voltage at the output of the amplifier. The maximum amplitude of this offset, which adds to the D/A converter nonlinearity, is 0.67 V_{OS} where V_{OS} is the amplifier input-offset voltage. To maintain monotonic operation, it is recommended that V_{OS} be no greater than 10% of 1 LSB over the temperature range of operation.

General Ground Management: AC or transient voltages between AGND and DGND can cause noise injection into the analog output. The simplest method of ensuring that voltages at AGND and DGND are equal is to tie AGND and DGND together at the PM-7545/PM-7645. It is recommended that two diodes (1N914 or equivalent) be connected in inverse parallel between AGND and DGND pins in complex systems where AGND and DGND tie on the backplane.

Digital Glitches: When $\overline{WR}$ and $\overline{CS}$ are both low, the latches are transparent and the D/A converter inputs follow the data inputs. Some bus systems do not always have data valid for the whole period during which $\overline{WR}$ is low. This will allow invalid data to briefly appear at the DAC inputs during the write cycle. This can cause unwanted glitches at the DAC output. Retiming the write pulse $\overline{WR}$, so that it only occurs when data is valid, will eliminate the problem.

FIGURE 5: Bipolar Operation (2's Complement Code)

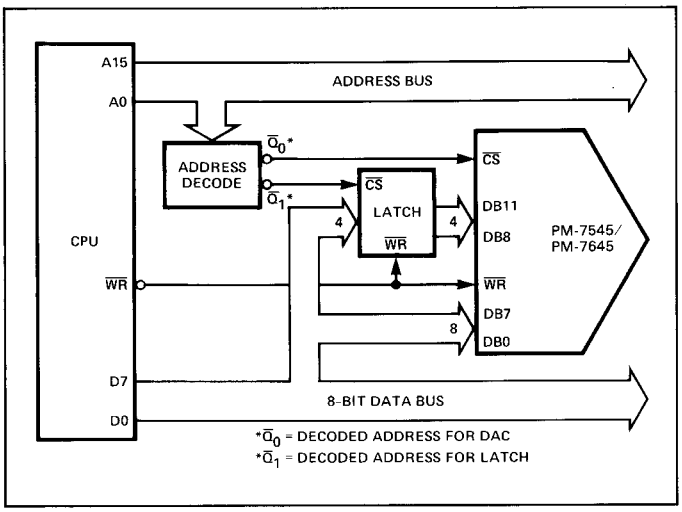


INTERFACING THE PM-7545/PM-7645 TO MICROPROCESSORS

The PM-7545 can be directly interfaced to either an 8 or 16-bit microprocessor via its 12-bit wide data latch using the $\overline{CS}$ and $\overline{WR}$ control signals.

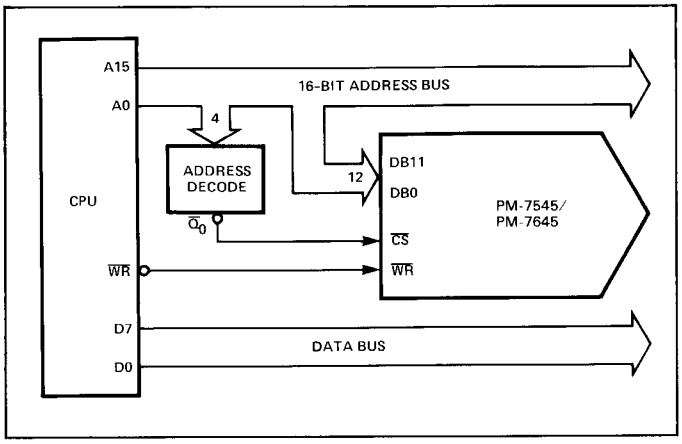
An 8-bit processor interface configuration is shown in Figure 6. It uses two memory addresses, one for the lower 8-bits and one for the upper 4-bits of data into the DAC via the latch.

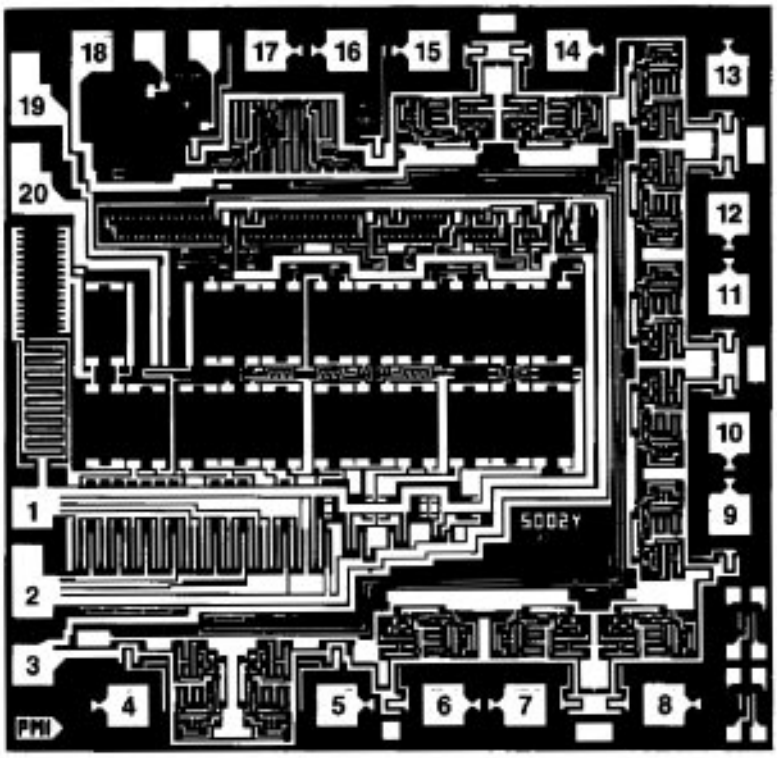
FIGURE 6: 8-Bit Processor to PM-7545/7645 Interface



Connection to an 8-bit processor with a full 16-bit wide address bus (such as the 6800, 8080, Z80) is shown in Figure 7. The 12 lower address lines are fed directly to the PM-7545; this allows the PM-7545 to use 4k bytes for its address location. The address field of the instruction is organized so that the lower 12-bits contain the DAC data. Data is written into the DAC using a single write instruction.

FIGURE 7: Connecting the PM-7545/7645 to an 8-Bit Microprocessor via the Address Bus

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