



**THE DATASHEET OF
PL123E-090C-R**



Low Skew Zero Delay Buffer

FEATURES

- Frequency Range 10MHz to 220MHz
- Zero input - output delay.
- Low Output to Output Skew
- Optional Drive Strength:
 Standard (8mA) *PL123E-09*
 High (12mA) *PL123E-09H*
- 2.5V or 3.3V, $\pm 10\%$ operation.
- Available in 16-Pin SOP or TSSOP packages

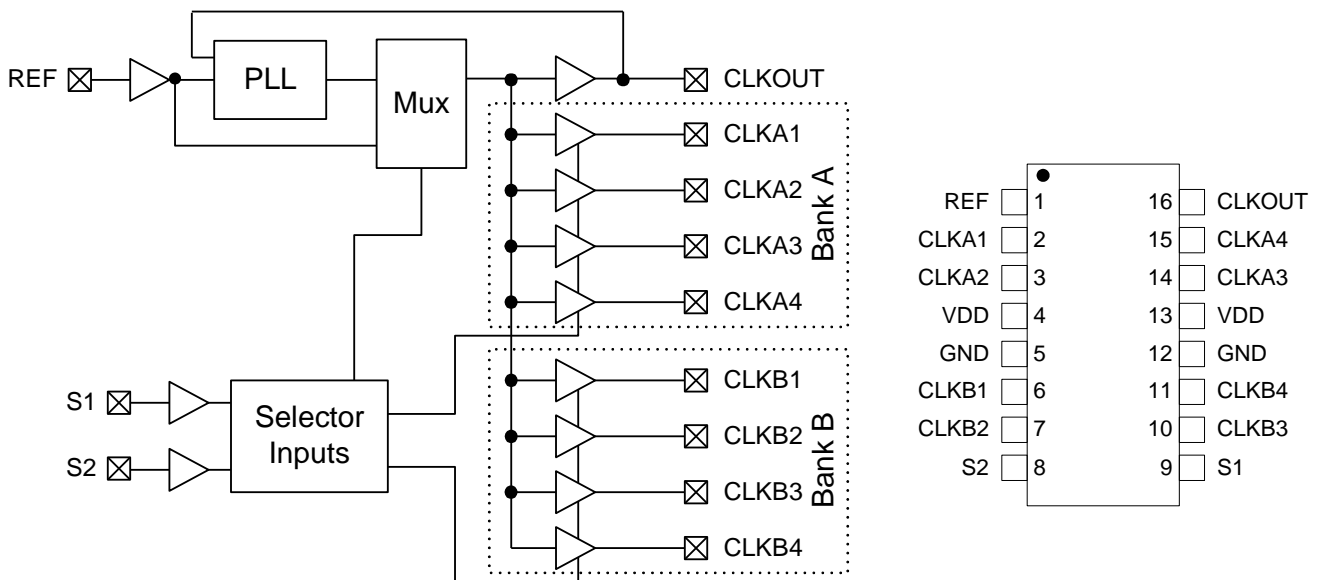
DESCRIPTION

The PL123E-09 (-09H for High Drive) is a high performance, low skew, low jitter zero delay buffer designed to distribute high speed clocks. It has two low-skew output banks, of 4 outputs each, that are synchronized with the input. Control of the two banks of outputs is achieved by using the S1 and S2 inputs as shown in the Selector Definition table on page 2.

The synchronization is established via CLKOUT feed back to the input of the PLL. Since the skew between the input and output is less than $\pm 100\text{ps}$, the device acts as a zero delay buffer. The input output propagation delay can be advanced or delayed by adjusting the load on the CLKOUT pin.

These parts are not intended for 5V input-tolerant applications.

BLOCK DIAGRAM



Low Skew Zero Delay Buffer

PIN DESCRIPTIONS

| Name | Package Type | | Type | Description |
|-----------------------|--------------|---------|------|---|
| | TSSOP-16L | SOP-16L | | |
| REF ^[1] | 1 | 1 | I | Input reference frequency. |
| CLKA1 ^[2] | 2 | 2 | O | Buffered clock output, Bank A |
| CLKA2 ^[2] | 3 | 3 | O | Buffered clock output, Bank A |
| VDD | 4,13 | 4,13 | P | VDD connection |
| GND | 5,12 | 5,12 | P | GND connection |
| CLKB1 ^[2] | 6 | 6 | O | Buffered clock output, Bank B |
| CLKB2 ^[2] | 7 | 7 | O | Buffered clock output, Bank B |
| S2 ^[3] | 8 | 8 | I | Selector input |
| S1 ^[3] | 9 | 9 | I | Selector input |
| CLKB3 ^[2] | 10 | 10 | O | Buffered clock output, Bank B |
| CLKB4 ^[2] | 11 | 11 | O | Buffered clock output, Bank B |
| CLKA3 ^[2] | 14 | 14 | O | Buffered clock output, Bank A |
| CLKA4 ^[2] | 15 | 15 | O | Buffered clock output, Bank A |
| CLKOUT ^[2] | 16 | 16 | O | Buffered clock output. Internal feedback on this pin. |

Notes: 1: Weak pull-down. 2: Weak pull-down on all outputs. 3: Weak Pull-Up on S1 and S2

SELECTOR DEFINITION

| S2 | S1 | CLOCK A1–A4 (Bank A) | CLOCK B1–B4 (Bank B) | CLKOUT | Output Source | PLL Shutdown |
|----|----|-------------------------|-------------------------|--------|---------------|--------------|
| 0 | 0 | Three-state | Three-state | Driven | PLL | N |
| 0 | 1 | Driven | Three-state | Driven | PLL | N |
| 1 | 0 | Driven | Driven | Driven | Reference | Y |
| 1 | 1 | Driven | Driven | Driven | PLL | N |

INPUT / OUTPUT SKEW CONTROL

The PL123E-09 will achieve Zero Delay from input to output when all the outputs are loaded equally. Adjustments to the input/output delay can be made by adding additional loading to the CLKOUT pin.

Please contact Micrel for more information.

Low Skew Zero Delay Buffer**LAYOUT RECOMMENDATIONS**

The following guidelines are to assist you with a performance optimized PCB design:

Signal Integrity and Termination Considerations

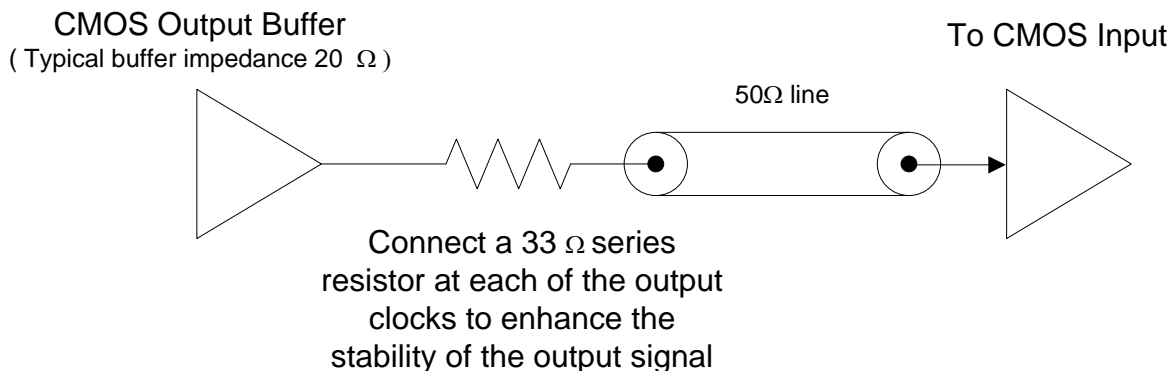
- Keep traces short!
- Trace = Inductor. With a capacitive load this equals ringing!
- Long trace = Transmission Line. Without proper termination this will cause reflections (looks like ringing).
- Design long traces as “striplines” or “microstrips” with defined impedance.
- Match trace at one side to avoid reflections bouncing back and forth.

Decoupling and Power Supply Considerations

- Place decoupling capacitors as close as possible to the VDD pin(s) to limit noise from the power supply
- Addition of a ferrite bead in series with VDD can help prevent noise from other board sources
- Value of decoupling capacitor is frequency dependent. Typical values to use are 0.1 μF for designs using frequencies < 50MHz and 0.01 μF for designs using frequencies > 50MHz.

Typical CMOS termination

Place Series Resistor as close as possible to CMOS output



Low Skew Zero Delay Buffer

ABSOLUTE MAXIMUM CONDITIONS

Supply Voltage to Ground Potential -0.5V to 4.6V
 DC Input Voltage $V_{SS} - 0.5V$ to 4.6V
 Storage Temperature -65°C to 150°C

Junction Temperature 150°C
 Static Discharge Voltage
 (per MIL-STD-883, Method 3015)..... > 2000V

OPERATING CONDITIONS

| Description | Parameter | Min | Max | Unit |
|--|-------------|------|------|----------|
| Supply Voltage | V_{DD} | 2.25 | 3.63 | V |
| Load Capacitance, <100 MHz, 3.3V | $C_L^{[4]}$ | - | 30 | pF |
| Load Capacitance, <100 MHz, 2.5V with High Drive | | - | 30 | pF |
| Load Capacitance, <133.3 MHz, 3.3V | | - | 22 | pF |
| Load Capacitance, <133.3 MHz, 2.5V with High Drive | | - | 22 | pF |
| Load Capacitance, <133.3 MHz, 2.5V with Standard Drive | | - | 15 | pF |
| Load Capacitance, >133.3 MHz, 3.3V | | - | 15 | pF |
| Load Capacitance, >133.3 MHz, 2.5V with High Drive | | - | 15 | pF |
| Input Capacitance ^[5] | C_{IN} | - | 5 | pF |
| Closed-loop bandwidth (typical), 3.3V | BW | | 1 | MHz |
| Closed-loop bandwidth (typical), 2.5V | | | 0.5 | MHz |
| Output Impedance (typical), 3.3V High Drive | R_{OUT} | | 23 | Ω |
| Output Impedance (typical), 3.3V Standard Drive | | | 33 | Ω |
| Output Impedance (typical), 2.5V High Drive | | | 26 | Ω |
| Output Impedance (typical), 2.5V Standard Drive | | | 39 | Ω |
| Power-up time for all V_{DD} 's to reach minimum specified voltage (power ramps must be monotonic) | t_{PU} | 0.01 | 250 | ms |

Notes:

4. Applies to Test Circuit #1.
5. Applies to both REF Clock and internal feedback path on CLKOUT.
6. Theta Ja, EIA JEDEC 51 test board conditions, 2S2P; Theta Jc Mil-Spec 883E Method 1012.1.

Low Skew Zero Delay Buffer
3.3V DC ELECTRICAL SPECIFICATIONS

| Description | Parameter | Test Conditions | Min | Max | Unit |
|-----------------------|-----------|---|------------|----------------|---------|
| Supply Voltage | V_{DD} | | 2.97 | 3.63 | V |
| Input LOW Voltage | V_{IL} | | – | 0.8 | V |
| Input HIGH Voltage | V_{IH} | | 2.5 | $V_{DD} + 0.3$ | V |
| Input Leakage Current | I_{IL} | $0 < V_{IN} < V_{IL}$ | – | ± 10 | μA |
| Input HIGH Current | I_{IH} | $V_{IN} = V_{DD}$ | – | 100 | μA |
| Output LOW Voltage | V_{OL} | $I_{OL} = 8 \text{ mA}$ (Standard Drive) $I_{OL} = 12 \text{ mA}$ (High Drive) | – – | 0.4 0.4 | V V |
| Output HIGH Voltage | V_{OH} | $I_{OH} = -8 \text{ mA}$ (Standard Drive) $I_{OH} = -12 \text{ mA}$ (High Drive) | 2.4 2.4 | – – | V V |
| Supply Current | I_{DD} | Unloaded outputs, 66-MHz REF | – | 45 | mA |

2.5V DC ELECTRICAL SPECIFICATIONS

| Description | Parameter | Test Conditions | Min | Max | Unit |
|-----------------------|-----------|---|----------------------------------|----------------|---------|
| Supply Voltage | V_{DD} | | 2.25 | 2.75 | V |
| Input LOW Voltage | V_{IL} | | – | 0.7 | V |
| Input HIGH Voltage | V_{IH} | | 1.7 | $V_{DD} + 0.3$ | V |
| Input Leakage Current | I_{IL} | $0 < V_{IN} < V_{IL}$ | – | ± 10 | μA |
| Input HIGH Current | I_{IH} | $V_{IN} = V_{DD}$ | – | 100 | μA |
| Output LOW Voltage | V_{OL} | $I_{OL} = 8 \text{ mA}$ (Standard Drive) $I_{OL} = 12 \text{ mA}$ (High Drive) | – – | 0.5 0.5 | V V |
| Output HIGH Voltage | V_{OH} | $I_{OH} = -8 \text{ mA}$ (Standard Drive) $I_{OH} = -12 \text{ mA}$ (High Drive) | $V_{DD} - 0.6$ $V_{DD} - 0.6$ | – – | V V |
| Supply Current | I_{DD} | Unloaded outputs, 66-MHz REF | – | 30 | mA |

Low Skew Zero Delay Buffer
3.3V AND 2.5V AC ELECTRICAL SPECIFICATIONS

| Description | Parameter | Test Conditions | Min | Typ | Max | Unit |
|--|---------------------------------|--|------|-----|------|------|
| Maximum Frequency ^[7] (Input/Output) | 1/t ₁ | 3.3V High Drive | 10 | – | 220 | MHz |
| | | 3.3V Standard Drive | 10 | – | 167 | MHz |
| | | 2.5V High Drive | 10 | – | 200 | MHz |
| | | 2.5V Standard Drive | 10 | – | 134 | MHz |
| Input Duty Cycle (PLL Mode only) | T _{IDC} | <133.3 MHz | 25 | – | 75 | % |
| | | >133.3 MHz | 40 | – | 60 | % |
| Output Duty Cycle ^[8] | t ₂ ÷ t ₁ | <133.3 MHz | 47 | – | 53 | % |
| | | >133.3 MHz | 45 | – | 55 | % |
| Rise, Fall Time (3.3V) ^[8] | t ₃ , t ₄ | Standard Drive, CL = 30 pF, <100 MHz | – | 1.6 | – | ns |
| | | Standard Drive, CL = 22 pF, <133.3 MHz | – | 1.6 | – | ns |
| | | Standard Drive, CL = 15 pF, <167 MHz | – | 0.6 | – | ns |
| | | High Drive, CL = 30 pF, <100 MHz | – | 1.2 | – | ns |
| | | High Drive, CL = 22 pF, <133.3 MHz | – | 1.2 | – | ns |
| | | High Drive, CL = 15 pF, >133.3 MHz | – | 0.5 | – | ns |
| Rise, Fall Time (2.5V) ^[8] | t ₃ , t ₄ | Standard Drive, CL = 15 pF, <133.33 MHz | – | 1.5 | – | ns |
| | | High Drive, CL = 30 pF, <100 MHz | – | 2.1 | – | ns |
| | | High Drive, CL = 22 pF, <133.3 MHz | – | 1.3 | – | ns |
| | | High Drive, CL = 15 pF, >133.3 MHz | – | 1.2 | – | ns |
| Output to Output Skew ^[8] | t ₅ | All outputs equally loaded | – | – | 100 | ps |
| Delay, REF Rising Edge to CLKOUT Rising Edge ^[8] | t ₆ | PLL enabled @ 3.3V | –100 | – | 100 | ps |
| | | PLL enabled @ 2.5V | –200 | – | 200 | ps |
| Part to Part Skew ^[8] | t ₇ | Measured at V _{DD} /2. Any output to any output, 3.3V supply | – | – | ±150 | ps |
| | | Measured at V _{DD} /2. Any output to any output, 2.5V supply | – | – | ±300 | ps |
| PLL Lock Time ^[8] | t _{LOCK} | Stable power supply, valid clocks presented on REF and CLKOUT pins | – | – | 1.0 | ms |
| Cycle-to-Cycle Jitter, Peak ^[8, 9] | T _{JCC} | 3.3V, >66 MHz, <15 pF | – | – | 55 | ps |
| | | 3.3V, >66 MHz, <30 pF, Standard. Drive | – | – | 125 | ps |
| | | 3.3V, >66 MHz, <30 pF, High Drive | – | – | 100 | ps |
| | | 2.5V, >66 MHz, <15 pF, Standard. Drive | – | – | 95 | ps |
| | | 2.5V, >66 MHz, <15 pF, High Drive | – | – | 65 | ps |
| | | 2.5V, >66 MHz, <30 pF, High Drive | – | – | 145 | ps |

Low Skew Zero Delay Buffer

3.3V AND 2.5V AC ELECTRICAL SPECIFICATIONS (continued)

| Description | Parameter | Test Conditions | Min | Typ | Max | Unit |
|--------------------------------------|------------------|--|-----|-----|-----|------|
| Period Jitter, Peak ^[8,9] | T _{PER} | 3.3V, 66–100 MHz, <15 pF | – | – | 75 | ps |
| | | 3.3V, >100 MHz, <15 pF | – | – | 45 | ps |
| | | 3.3V, >66 MHz, <30 pF, Standard Drive | – | – | 100 | ps |
| | | 3.3V, >66 MHz, <30 pF, High Drive | – | – | 70 | ps |
| | | 2.5V, >66 MHz, <15 pF, Standard. Drive | – | – | 60 | ps |
| | | 2.5V, 66–100 MHz, <15 pF, High Drive | – | – | 60 | ps |
| | | 2.5V, >100 MHz, <15 pF, High Drive | – | – | 45 | ps |

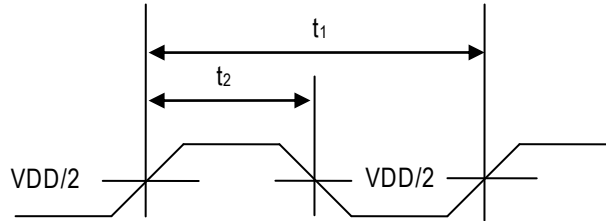
Notes:

7. For the given maximum loading conditions. See C_L in Operating Conditions Table.
8. Parameter is guaranteed by design and characterization. Not 100% tested in production.
9. Typical jitter is measured at 3.3V or 2.5V, 29°C, with all outputs driven into the maximum specified load.

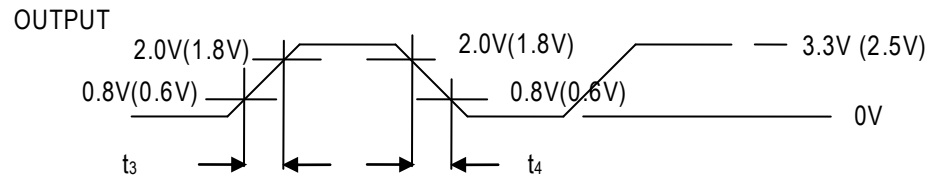
Low Skew Zero Delay Buffer

SWITCHING WAVEFORMS

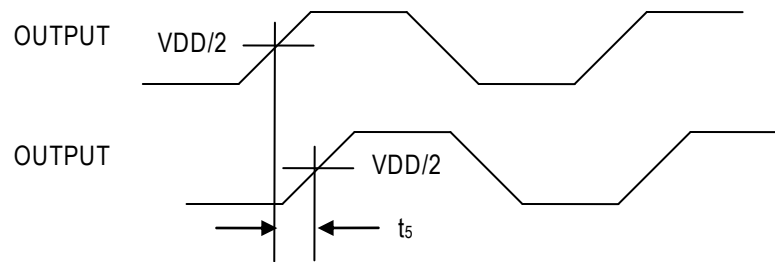
Duty Cycle Timing



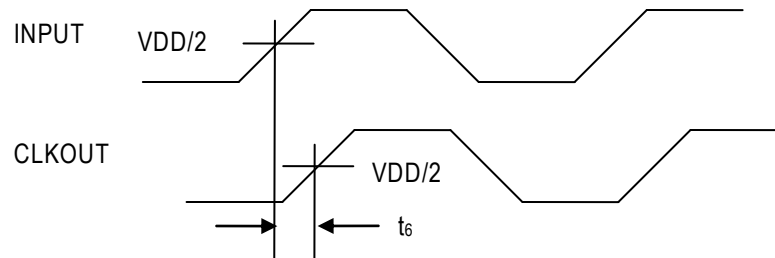
All Outputs Rise/Fall Time



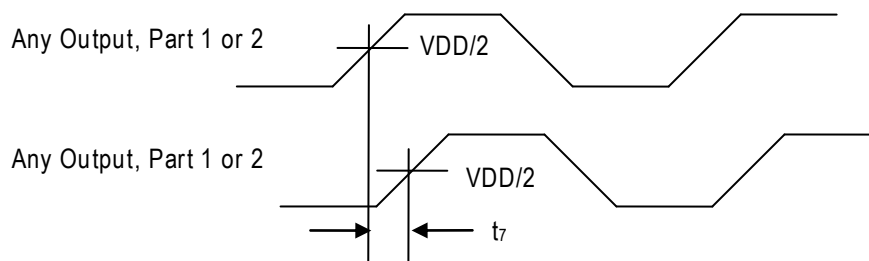
Output-Output Skew



Input-Output Propagation Delay



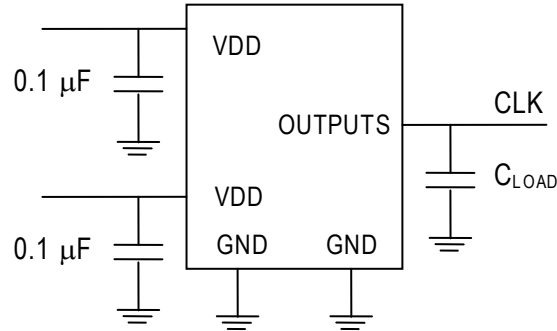
Device-Device Skew



Low Skew Zero Delay Buffer

TEST CIRCUITS

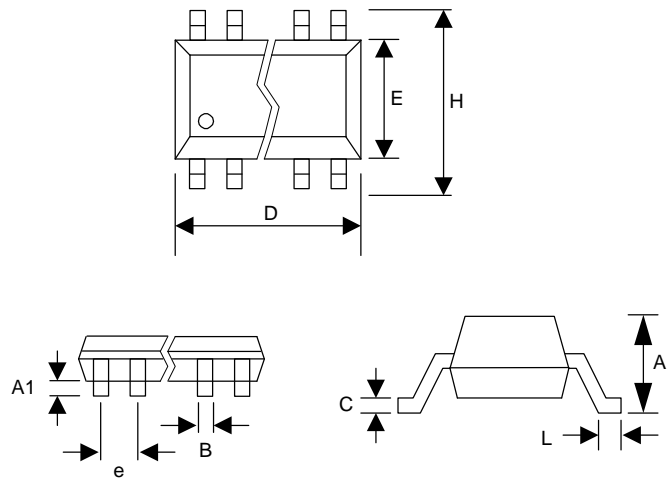
Test Circuit #1



PACKAGE DRAWINGS (GREEN PACKAGE COMPLIANT)

16 PIN Narrow SOP, TSSOP (mm)

| Symbol | SOP | | TSSOP | |
|--------|----------|-------|----------|------|
| | Min. | Max. | Min. | Max. |
| A | 1.35 | 1.75 | - | 1.20 |
| A1 | 0.10 | 0.25 | 0.05 | 0.15 |
| B | 0.33 | 0.51 | 0.19 | 0.30 |
| C | 0.19 | 0.25 | 0.09 | 0.20 |
| D | 9.80 | 10.00 | 4.90 | 5.10 |
| E | 3.80 | 4.00 | 4.30 | 4.50 |
| H | 5.80 | 6.20 | 6.40 BSC | |
| L | 0.40 | 1.27 | 0.45 | 0.75 |
| e | 1.27 BSC | | 0.65 BSC | |



Low Skew Zero Delay Buffer

ORDERING INFORMATION

For part ordering, please contact our Sales Department:

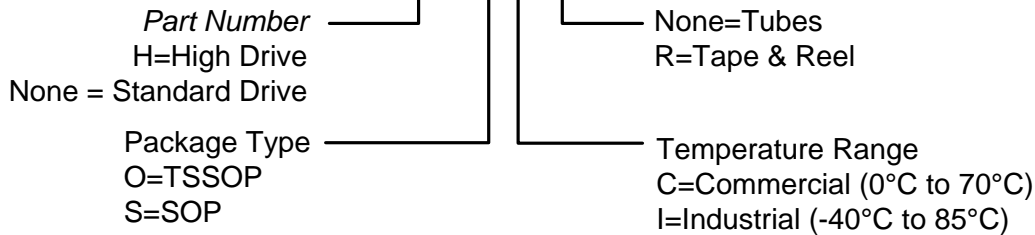
2180 Fortune Drive, San Jose, CA 95131, USA

Tel: (408) 944-0800 Fax: (408) 474-1000

PART NUMBER

The order number for this device is a combination of the following:
Device number, Package type and Operating temperature range

PL123E-09(H) X X - X



| Part/Order Number | Marking | Package Option |
|-------------------|----------------|------------------------------|
| PL123E-09OC | P123E09 OC | 16-Pin TSSOP Tube |
| PL123E-09OC-R | LLLLL | 16-Pin TSSOP (Tape and Reel) |
| PL123E-09HOC | P123E09H OC | 16-Pin TSSOP Tube |
| PL123E-09HOC-R | LLLLL | 16-Pin TSSOP (Tape and Reel) |
| PL123E-09SC | P123E09 SC | 16-Pin SOP Tube |
| PL123E-09SC-R | LLLLL | 16-Pin SOP (Tape and Reel) |
| PL123E-09HSC | P123E09H SC | 16-Pin SOP Tube |
| PL123E-09HSC-R | LLLLL | 16-Pin SOP (Tape and Reel) |
| PL123E-09OI | P123E09 OI | 16-Pin TSSOP Tube |
| PL123E-09OI-R | LLLLL | 16-Pin TSSOP (Tape and Reel) |
| PL123E-09HOI | P123E09H OI | 16-Pin TSSOP Tube |
| PL123E-09HOI-R | LLLLL | 16-Pin TSSOP (Tape and Reel) |
| PL123E-09SI | P123E09 SI | 16-Pin SOP Tube |
| PL123E-09SI-R | LLLLL | 16-Pin SOP (Tape and Reel) |
| PL123E-09HSI | P123E09H SI | 16-Pin SOP Tube |
| PL123E-09HSI-R | LLLLL | 16-Pin SOP (Tape and Reel) |

*Note: LLLLL designates lot number

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