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## Full-Featured, Low Pin Count Microcontrollers with XLP Product Brief

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### Description

PIC16(L)F183XX microcontrollers feature Analog, Core Independent Peripherals and communication peripherals, combined with eXtreme Low Power (XLP) for a wide range of general purpose and low-power applications. The Peripheral Pin Select (PPS) functionality enables pin mapping when using the digital peripherals (CLC, CWG, CCP, PWM and communications) to add flexibility to the application design.

### Core Features

- C Compiler Optimized RISC Architecture
- Only 49 Instructions
- Operating Speed:
  - DC – 32 MHz clock input
  - 125 ns minimum instruction cycle
- Interrupt Capability
- 16-Level Deep Hardware Stack
- Up to Four 8-Bit Timers
- Up to Three 16-Bit Timers
- Low-Current Power-on Reset (POR)
- Configurable Power-up Timer (PWRTE)
- Brown-out Reset (BOR) with Fast Recovery
- Low-Power BOR (LPBOR) Option
- Extended Watchdog Timer (WDT) with Dedicated On-Chip Oscillator for Reliable Operation
- Programmable Code Protection

### Memory

- Up to 28 KB Program Flash Memory (PFM)
- Up to 2 KB Data SRAM Memory
- 256B of EEPROM Data Flash Memory (DFM)
- Direct, Indirect and Relative Addressing modes

### Operating Characteristics

- Operating Voltage Range:
  - 1.8V to 3.6V (PIC16LF183XX)
  - 2.3V to 5.5V (PIC16F183XX)
- Temperature Range:
  - Industrial: -40°C to 85°C
  - Extended: -40°C to 125°C

### eXtreme Low-Power (XLP) Features

- Sleep mode: 40 nA @ 1.8V, typical
- Watchdog Timer: 250 nA @ 1.8V, typical
- Secondary Oscillator: 300 nA @ 32 kHz
- Operating Current:
  - 8 uA @ 32 kHz, 1.8V, typical
  - 37 uA/MHz @ 1.8V, typical

### Power-Saving Functionality

- Doze mode: Ability to run the CPU core slower than the system clock used by the internal peripherals
- Idle mode: Ability to put the CPU core to sleep while internal peripherals continue operating from the system clock
- Sleep mode: Lowest Power Consumption
- Peripheral Module Disable: Peripheral power disable hardware module to minimize power consumption of unused peripherals

### Digital Peripherals

- Configurable Logic Cell (CLC):
  - Up to four CLCs
  - Integrated combinational and sequential logic
- Complementary Waveform Generator (CWG):
  - Rising and falling edge dead-band control
  - Full-bridge, half-bridge, 1-channel drive
  - Up to two CWGs
  - Multiple signal sources
- Up to Four Capture/Compare/PWM (CCP) modules
- PWM: Two 10-bit Pulse-Width Modulators
- Numerically Controlled Oscillator (NCO):
  - Precision linear frequency generator (@50% duty cycle) with 0.0001% step size of source input clock
  - Input Clock:  $0 \text{ Hz} < F_{NCO} < 32 \text{ MHz}$
  - Resolution:  $F_{NCO}/2^{20}$
- Serial Communications:
  - SPI, I<sup>2</sup>C, EUSART
  - RS-232, RS-485, LIN compatible
- Data Signal Modulator (DSM):
  - Modulates a carrier signal with digital data to create custom carrier synchronized output waveforms

# PIC16(L)F183XX

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- Peripheral Pin Select (PPS):
  - I/O pin remapping of digital peripherals
- Up to 18 I/O Pins:
  - Individually programmable pull ups
  - Slew rate control
  - Interrupt-on-change with edge-select
  - Input level selection control (ST or TTL)
  - Digital open-drain enable

## Analog Peripherals

- 10-Bit Analog-to-Digital Converter (ADC):
  - Up to 17 external channels
  - Conversion available during Sleep
- Comparator:
  - Up to two comparators
  - Low and High-Speed modes
  - Fixed Voltage Reference at inverting/noninverting input(s)
  - Comparator outputs externally accessible
- 5-Bit Digital-to-Analog Converter (DAC):
  - 5-bit resolution, rail-to-rail
  - Positive Reference Selection
  - Unbuffered I/O pin output
  - Internal connections to ADCs and comparators
- Voltage Reference:
  - Fixed Voltage Reference with 1.024V, 2.048V and 4.096V output levels

## Clocking Structure

- High-Precision Internal Oscillator:
  - Selectable frequency range up to 32 MHz
- x2/x4 PLL with Internal and External Sources
- Low-Power Internal 32 kHz Oscillator (LFINTOSC)
- External 32 kHz Crystal Oscillator (SOCS)
- External High-Speed Crystal Oscillators

TABLE 1: PIC16(L)F183XX Family Types

Device	Data Sheet Index	Program Memory (KB)	Program Memory (KW)	EEPROM (B)	RAM (B)	I/Os <sup>(1)</sup>	10-bit ADCs	Comparators	5-bit DAC	Timers 0/1/2	CCP/PWM	CWG	EUSART	SPI	I <sup>2</sup> C
<a href="#">PIC16(L)F18313</a>	(A)	3.5	2	256	256	6	5	1	1	1/1/1	2/2	1	1	1	1
<a href="#">PIC16(L)F18323</a>	(A)	3.5	2	256	256	12	11	2	1	1/1/1	2/2	1	1	1	1
<a href="#">PIC16(L)F18324</a>	(B)	7	4	256	512	12	11	2	1	1/3/3	4/2	2	1	1	1
<a href="#">PIC16(L)F18325</a>	(C)	14	8	256	1K	12	11	2	1	1/3/3	4/2	2	1	2	2
<a href="#">PIC16(L)F18326</a>	(D)	28	16	256	2K	12	11	2	1	1/3/3	4/2	2	1	2	2
<a href="#">PIC16(L)F18344</a>	(B)	7	4	256	512	18	17	2	1	1/3/3	4/2	2	1	1	1
<a href="#">PIC16(L)F18345</a>	(C)	14	8	256	1K	18	17	2	1	1/3/3	4/2	2	1	2	2
<a href="#">PIC16(L)F18346</a>	(D)	28	16	256	2K	18	17	2	1	1/3/3	4/2	2	1	2	2

**Note 1:** One pin is input-only.

**Note 2:** Debugging Methods: (I) – Integrated on Chip; E – using Emulation Header.

**Data Sheet Index:** (Unshaded devices are described in this document.)

- A)** [DS40001799](#) [PIC16\(L\)F18313/18323 Data Sheet, Full-Featured, Low Pin Count Microcontrollers with XLP](#)
- B)** [DS40001800](#) [PIC16\(L\)F18324/18344 Data Sheet, Full-Featured, Low Pin Count Microcontrollers with XLP](#)
- C)** [DS40001795](#) [PIC16\(L\)F18325/18345 Data Sheet, Full-Featured, Low Pin Count Microcontrollers with XLP](#)
- D)** [Future Release](#) [PIC16\(L\)F18326/18346 Data Sheet, Full-Featured, Low Pin Count Microcontrollers with XLP](#)

**Note:** For other small form-factor package availability and marking information, please visit <http://www.microchip.com/packaging> or contact your local sales office.

# PIC16(L)F183XX

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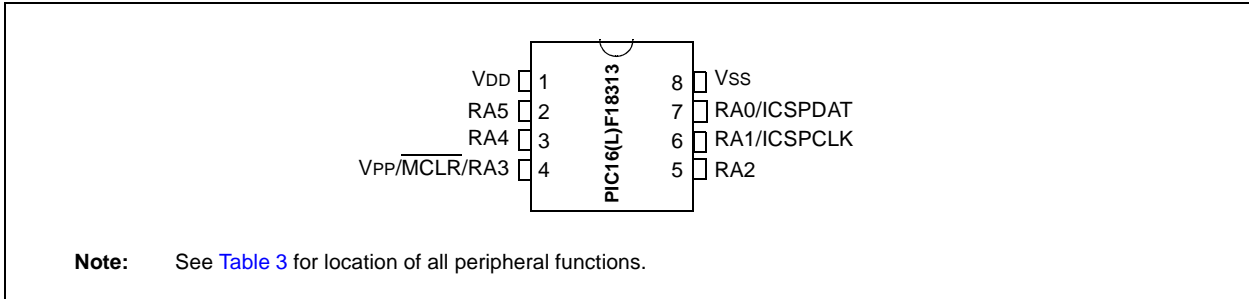
**TABLE 2: PACKAGES**

Packages	PDIP	SOIC	UDFN	TSSOP	UQFN	SSOP
PIC16(L)F18313	X	X	X			
PIC16(L)F18323	X	X		X	X	
PIC16(L)F18324	X	X		X	X	
PIC16(L)F18325	X	X		X	X	
PIC16(L)F18326	X	X		X	X	
PIC16(L)F18344	X	X			X	X
PIC16(L)F18345	X	X			X	X
PIC16(L)F18346	X	X			X	X

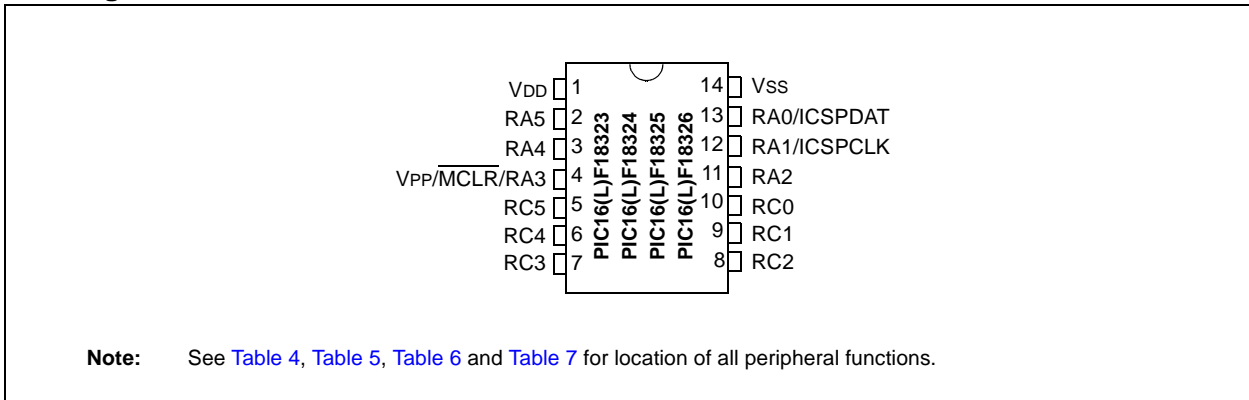
**Note:** Pin details are subject to change.

## PIN DIAGRAMS

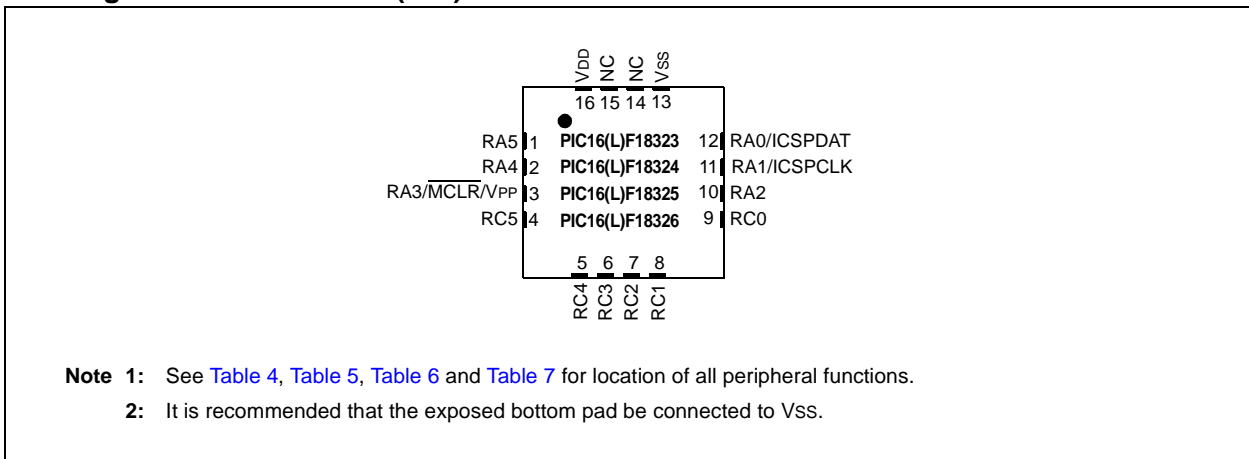
### Pin Diagram – 8-Pin PDIP, SOIC, UDFN



### Pin Diagram – 14-Pin PDIP, SOIC, TSSOP

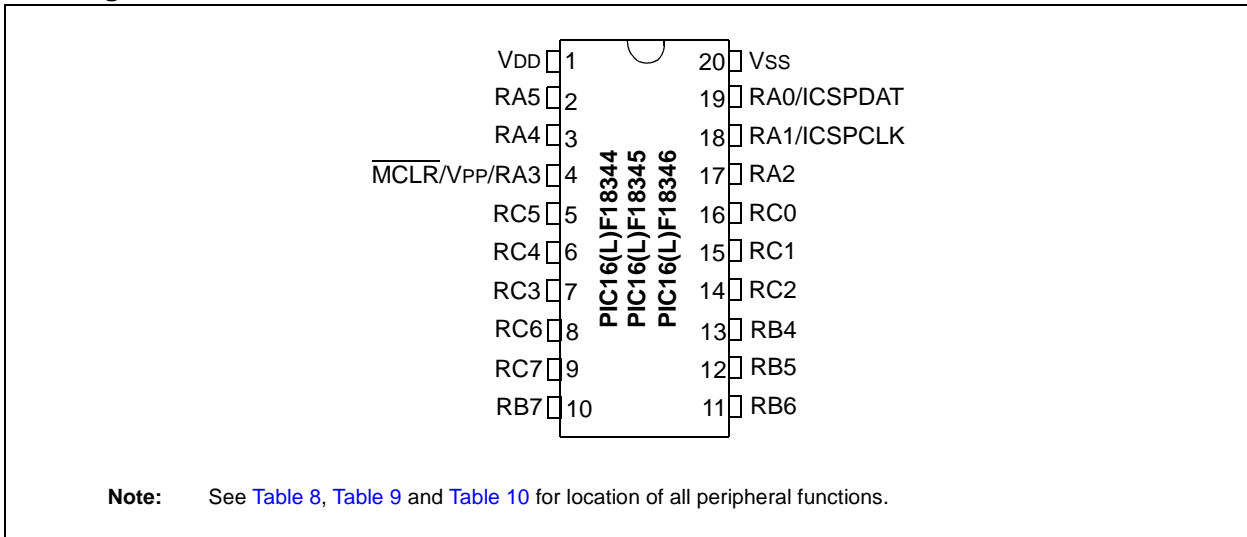


### Pin Diagram – 16-Pin UQFN (4x4)

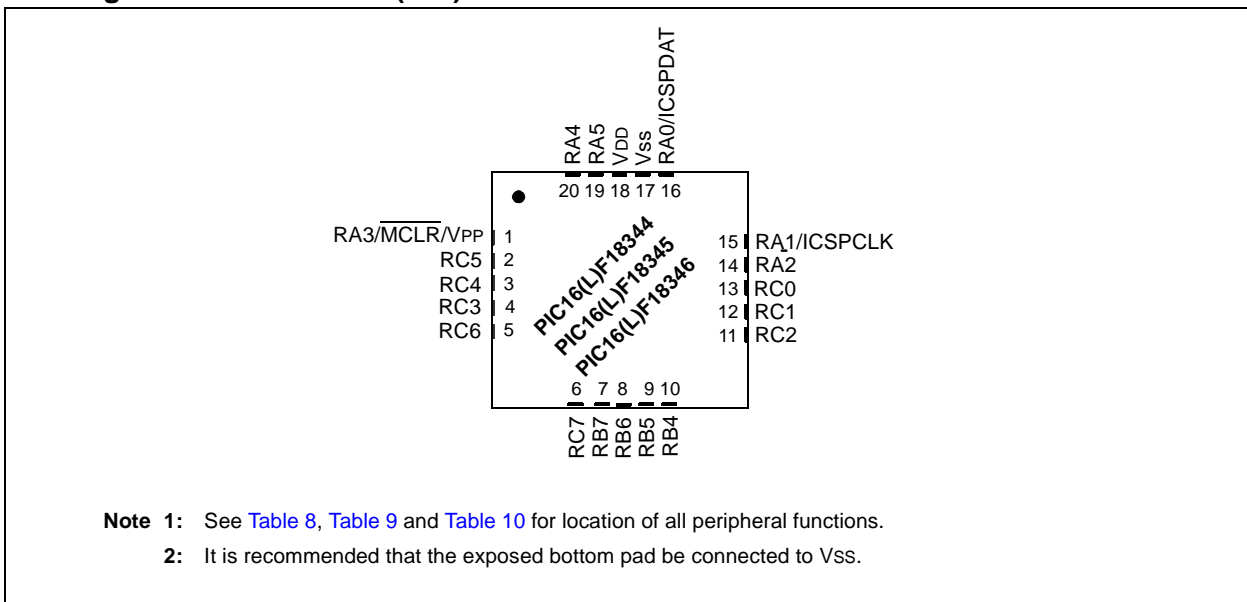


# PIC16(L)F183XX

## Pin Diagram – 20-Pin PDIP, SOIC, SSOP



## Pin Diagram – 20-Pin UQFN (4x4)



## PIN ALLOCATION TABLES

**TABLE 3: 8-PIN ALLOCATION TABLE (PIC16(L)F18313)**

I/O <sup>(2)</sup>	8-Pin PDIP/SOIC/UDFN	ADC	Reference	Comparator	NCO	DAC	DSM	Timers	CCP	PWM	CWG	MSSP	EUSART	CLC	CLKR
RA0	7	ANA0	—	C1IN0+	—	DAC1OUT	MDCIN1 <sup>(1)</sup>	—	—	—	—	—	TX <sup>(1)</sup> CK <sup>(1)</sup>	CLCIN3 <sup>(1)</sup>	—
RA1	6	ANA1	VREF+	C1IN0-	—	DAC1REF+	MDMIN <sup>(1)</sup>	—	—	—	—	SCK <sup>(1)</sup> SCL <sup>(1,3,4)</sup>	RX <sup>(1)</sup> DT <sup>(1,3)</sup>	CLCIN2 <sup>(1)</sup>	—
RA2	5	ANA2	VREF-	—	—	DAC1REF-	—	TOCK <sup>(1)</sup>	—	—	CWG1 <sup>(1)</sup>	SDA <sup>(1,3,4)</sup> SDO <sup>(1)</sup>	—	—	—
RA3	4	—	—	—	—	—	—	—	—	—	—	SS <sup>(1)</sup>	—	CLCIN0 <sup>(1)</sup>	—
RA4	3	ANA4	—	C1IN1-	—	—	—	T1G <sup>(1)</sup> SOSCO	—	—	—	—	—	—	—
RA5	2	ANA5	—	—	—	—	MDCIN2 <sup>(1)</sup>	T1CK <sup>(1)</sup> SOSCIN SOSCI	CCP1 <sup>(1)</sup> CCP2 <sup>(1)</sup>	—	—	—	—	CLCIN1 <sup>(1)</sup>	—
VDD	1	—	—	—	—	—	—	—	—	—	—	—	—	—	—
VSS	8	—	—	—	—	—	—	—	—	—	—	—	—	—	—
OUT <sup>(2)</sup>	—	—	—	C1OUT	NCO	—	DSM	TMR0	CCP1	PWM5	CWG1A	SDA <sup>(3)</sup>	CK	CLC1OUT	CLKR
	—	—	—	—	—	—	—	—	CCP2	PWM6	CWG1B	SCL <sup>(3)</sup>	DT <sup>(3)</sup>	CLC2OUT	—
	—	—	—	—	—	—	—	—	—	—	CWG1C	SDO	TX	—	—
—	—	—	—	—	—	—	—	—	—	—	CWG1D	SCK	—	—	—

**Note 1:** Default peripheral input. Input can be moved to any other pin with the PPS input selection registers.

**2:** All pin outputs default to PORT latch data. Any pin can be selected as a digital peripheral output with the PPS output selection registers.

**3:** These peripheral functions are bidirectional. The output pin selections must be the same as the input pin selections.

**4:** These pins are configured for I<sup>2</sup>C logic levels; clock and data signals may be assigned to any of these pins. Assignments to the other pins (e.g., RA5) will operate, but ST as selected by the INLVL register.



**TABLE 4: 14/16-PIN ALLOCATION TABLE (PIC16(L)F18323) (CONTINUED)**

I/O <sup>(2)</sup>	14/16-Pin PDIP/SOIC/TSSOP	16-Pin UQFN	ADC	Reference	Comparator	NCO	DAC	DSM	Timers	CCP	PWM	CWG	MSSP	EUSART	CLC
OUT <sup>(2)</sup>	—	—	—	—	C1OUT	NCO	—	DSM	TMR0	CCP1	PWM5	CWG1A	SDA <sup>(3)</sup>	CK	CLC1OUT
	—	—	—	—	C2OUT	—	—	—	—	CCP2	PWM6	CWG1B	SCL <sup>(3)</sup>	DT <sup>(3)</sup>	CLC2OUT
	—	—	—	—	—	—	—	—	—	—	—	CWG1C	SDO	TX	—
	—	—	—	—	—	—	—	—	—	—	—	CWG1D	SCK	—	—

**Note 1:** Default peripheral input. Input can be moved to any other pin with the PPS input selection registers.

**2:** All pin outputs default to PORT latch data. Any pin can be selected as a digital peripheral output with the PPS output selection registers.

**3:** These peripheral functions are bidirectional. The output pin selections must be the same as the input pin selections.

**4:** These pins are configured for I<sup>2</sup>C logic levels; clock and data signals may be assigned to any of these pins. Assignments to other pins (e.g. RA5) will operate, but I<sup>2</sup>C will not operate. I<sup>2</sup>C pins are configured by the INLV register.

TABLE 5: 14/16-PIN ALLOCATION TABLE (PIC16(L)F18324)

I/O <sup>(2)</sup>	14/16-Pin PDIP/SOIC/TSSOP	16-Pin UQFN	ADC	Reference	Comparator	NCO	DAC	DSM	Timers	CCP	PWM	CWG	MSSP	EUSART	CLC
RA0	13	12	ANA0	—	C1IN0+	—	DAC1OUT	—	—	—	—	—	—	—	—
RA1	12	11	ANA1	VREF+	C1IN0- C2IN0-	—	DAC1REF+	—	—	—	—	—	—	—	—
RA2	11	10	ANA2	VREF-	—	—	DAC1REF-	—	TOCK1 <sup>(1)</sup>	CCP3 <sup>(1)</sup>	—	CWG1 <sup>(1)</sup> CWG2 <sup>(1)</sup>	—	—	—
RA3	4	3	—	—	—	—	—	—	—	—	—	—	—	—	—
RA4	3	2	ANA4	—	—	—	—	—	T1G <sup>(1)</sup> SOSCO	—	—	—	—	—	—
RA5	2	1	ANA5	—	—	—	—	—	T1CK1 <sup>(1)</sup> SOSCIN SOSCI	—	—	—	—	—	CLCIN3 <sup>(1)</sup>
RC0	10	9	ANC0	—	C2IN0+	—	—	—	T5CK1 <sup>(1)</sup>	—	—	—	SOCK <sup>(1)</sup> SCL <sup>(1,3,4)</sup>	—	—
RC1	9	8	ANC1	—	C1IN1- C2IN1-	—	—	—	—	CCP4 <sup>(1)</sup>	—	—	SDI <sup>(1)</sup> SDA <sup>(1,3,4)</sup>	—	CLCIN2 <sup>(1)</sup>
RC2	8	7	ANC2	—	C1IN2- C2IN2-	—	—	MDCIN1 <sup>(1)</sup>	—	—	—	—	—	—	—
RC3	7	6	ANC3	—	C1IN3- C2IN3-	—	—	MDMIN <sup>(1)</sup>	T5G <sup>(1)</sup>	CCP2 <sup>(1)</sup>	—	—	SS <sup>(1)</sup>	—	CLCIN0 <sup>(1)</sup>
RC4	6	5	ANC4	—	—	—	—	—	T3G <sup>(1)</sup>	—	—	—	—	TX <sup>(1)</sup> CK <sup>(1)</sup>	CLCIN1 <sup>(1)</sup>
RC5	5	4	ANC5	—	—	—	—	MDCIN2 <sup>(1)</sup>	T3CK1 <sup>(1)</sup>	CCP1 <sup>(1)</sup>	—	—	—	RX <sup>(1)</sup> DT <sup>(1,3)</sup>	—
VDD	1	16	—	—	—	—	—	—	—	—	—	—	—	—	—
VSS	14	13	—	—	—	—	—	—	—	—	—	—	—	—	—

**Note 1:** Default peripheral input. Input can be moved to any other pin with the PPS input selection registers.

**Note 2:** All pin outputs default to PORT latch data. Any pin can be selected as a digital peripheral output with the PPS output selection registers.

**Note 3:** These peripheral functions are bidirectional. The output pin selections must be the same as the input pin selections.

**Note 4:** These pins are configured for I<sup>2</sup>C logic levels; clock and data signals may be assigned to any of these pins. Assignments to other pins (e.g. RA5) will operate, but I<sup>2</sup>C will not.

**TABLE 5: 14/16-PIN ALLOCATION TABLE (PIC16(L)F18324) (CONTINUED)**

I/O <sup>(2)</sup>	14/16-Pin PDIP/SOIC/TSSOP	16-Pin UQFN	ADC	Reference	Comparator	NCO	DAC	DSM	Timers	CCP	PWM	CWG	MSSP	EUSART	CLC
OUT <sup>(2)</sup>	—	—	—	—	C1OUT	NCO	—	DSM	TMR0	CCP1	PWM5	CWG1A CWG2A	SDA <sup>(3)</sup>	CK	CLC1OUT
	—	—	—	—	C2OUT	—	—	—	—	CCP2	PWM6	CWG1B CWG2B	SCL <sup>(3)</sup>	DT <sup>(3)</sup>	CLC2OUT
	—	—	—	—	—	—	—	—	—	CCP3	—	CWG1C CWG2C	SDO	TX	CLC3OUT
	—	—	—	—	—	—	—	—	—	CCP4	—	CWG1D CWG2D	SCK	—	CLC4OUT

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**4:** These pins are configured for I<sup>2</sup>C logic levels; clock and data signals may be assigned to any of these pins. Assignments to other pins (e.g. RA5) will operate, but I<sup>2</sup>C will not operate in TTL/ST as selected by the INLV register.

TABLE 6: 14/16-PIN ALLOCATION TABLE (PIC16(L)F18325)

I/O(2)	14/16-Pin PDIP/SOIC/TSSOP	16-Pin UQFN	ADC	Reference	Comparator	NCO	DAC	DSM	Timers	CCP	PWM	CWG	MSSP	EUSART	CLC
RA0	13	12	ANA0	—	C1IN0+	—	DAC1OUT	—	—	—	—	—	SS2(1)	—	—
RA1	12	11	ANA1	VREF +	C1IN0- C2IN0-	—	DAC1REF+	—	—	—	—	—	—	—	—
RA2	11	10	ANA2	VREF-	—	—	DAC1REF-	—	T0CK1(1)	CCP3(1)	—	CWG1(1) CWG2(1)	—	—	—
RA3	4	3	—	—	—	—	—	—	—	—	—	—	—	—	—
RA4	3	2	ANA4	—	—	—	—	—	T1G(1) SOSCO	—	—	—	—	—	—
RA5	2	1	ANA5	—	—	—	—	—	T1CK1(1) SOSCIN SOSCI	—	—	—	—	—	CLCIN3(1)
RC0	10	9	ANC0	—	C2IN0+	—	—	—	T5CK1(1)	—	—	—	SCK1(1) SCL1(1,3,4)	—	—
RC1	9	8	ANC1	—	C1IN1- C2IN1-	—	—	—	—	CCP4(1)	—	—	SD11(1) SDA1(1,3,4)	—	CLCIN2(1)
RC2	8	7	ANC2	—	C1IN2- C2IN2-	—	—	MDCIN1(1)	—	—	—	—	—	—	—
RC3	7	6	ANC3	—	C1IN3- C2IN3-	—	—	MDMIN(1)	T5G(1)	CCP2(1)	—	—	SS1(1)	—	CLCIN0(1)
RC4	6	5	ANC4	—	—	—	—	—	T3G(1)	—	—	—	SCK2(1) SCL2(1,3,4)	TX(1) CK(1)	CLCIN1(1)
RC5	5	4	ANC5	—	—	—	—	MDCIN2(1)	T3CK1(1)	CCP1(1)	—	—	SD12(1) SDA2(1,3,4)	RX(1) DT(1,3)	—
VDD	1	16	—	—	—	—	—	—	—	—	—	—	—	—	—
VSS	14	13	—	—	—	—	—	—	—	—	—	—	—	—	—

**Note 1:** Default peripheral input. Input can be moved to any other pin with the PPS input selection registers.

**2:** All pin outputs default to PORT latch data. Any pin can be selected as a digital peripheral output with the PPS output selection registers.

**3:** These peripheral functions are bidirectional. The output pin selections must be the same as the input pin selections.

**4:** These pins are configured for I<sup>2</sup>C logic levels; clock and data signals may be assigned to any of these pins. Assignments to other pins (e.g. RA5) will operate, but I<sup>2</sup>C will not operate as selected by the INLV register.

**TABLE 6: 14/16-PIN ALLOCATION TABLE (PIC16(L)F18325) (CONTINUED)**

I/O <sup>(2)</sup>	14/16-Pin PDIP/SOIC/TSSOP	16-Pin UQFN	ADC	Reference	Comparator	NCO	DAC	DSM	Timers	CCP	PWM	CWG	MSSP	EUSART	CLC
OUT <sup>(2)</sup>	—	—	—	—	C1OUT	DDS	—	DSM	TMR0	CCP1	PWM5	CWG1A CWG2A	SDA1 <sup>(3)</sup> SDA2 <sup>(3)</sup>	CK	CLC1OUT
	—	—	—	—	C2OUT	—	—	—	—	CCP2	PWM6	CWG1B CWG2B	SCL1 <sup>(3)</sup> SCL2 <sup>(3)</sup>	DT <sup>(3)</sup>	CLC2OUT
	—	—	—	—	—	—	—	—	—	CCP3	—	CWG1C CWG2C	SDO1 SDO2	TX	CLC3OUT
	—	—	—	—	—	—	—	—	—	CCP4	—	CWG1D CWG2D	SCK1 SCK2	—	CLC4OUT

**Note 1:** Default peripheral input. Input can be moved to any other pin with the PPS input selection registers.

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**4:** These pins are configured for I<sup>2</sup>C logic levels; clock and data signals may be assigned to any of these pins. Assignments to other pins (e.g. RA5) will operate, but I<sup>2</sup>C will not operate in TTL/ST as selected by the INLVL register.

TABLE 7: 14/16-PIN ALLOCATION TABLE (PIC16(L)F18326)

I/O(2)	14/16-Pin PDIP/SOIC/TSSOP		16-Pin UQFN		ADC	Reference	Comparator	NCO	DAC	DSM	Timers	CCP	PWM	CWG	MSSP	EUSART	CLC	
	13	12	11	10														
RA0		ANA0	—	C1IN0+	—	DAC1OUT	—	—	—	—	—	—	—	—	SS2(1)	—	—	
RA1		ANA1	VREF + C2IN0-	C1IN0-	—	DAC1REF+	—	—	—	—	—	—	—	—	—	—	—	
RA2		ANA2	VREF-	—	—	DAC1REF-	—	T0CK1(1)	—	—	—	—	—	CWG1(1) CWG2(1)	—	—	—	
RA3		—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	
RA4		ANA4	—	—	—	—	—	T1G(1) SOSCO	—	—	—	—	—	—	—	—	—	
RA5		ANA5	—	—	—	—	—	T1CK1(1) SOSCIN SOSCI	—	—	—	—	—	—	—	—	CLCIN3(1)	
RC0		ANC0	—	C2IN0+	—	—	—	T5CK1(1)	—	—	—	—	—	—	SCK1(1) SCL1(1,3,4)	—	—	
RC1		ANC1	—	C1IN1- C2IN1-	—	—	—	—	—	—	—	CCP4(1)	—	—	SDI1(1) SDA1(1,3,4)	—	CLCIN2(1)	
RC2		ANC2	—	C1IN2- C2IN2-	—	—	—	MDCIN1(1)	—	—	—	—	—	—	—	—	—	
RC3		ANC3	—	C1IN3- C2IN3-	—	—	—	MDMIN(1)	—	—	T5G(1)	CCP2(1)	—	—	SS1(1)	—	CLCIN0(1)	
RC4		ANC4	—	—	—	—	—	—	—	—	T3G(1)	—	—	—	SCK2(1) SCL2(1,3,4)	TX(1) CK(1)	CLCIN1(1)	
RC5		ANC5	—	—	—	—	—	MDCIN2(1)	—	—	T3CK1(1)	CCP1(1)	—	—	SDI2(1) SDA2(1,3,4)	RX(1) DT(1,3)	—	
VDD		—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
VSS		—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—

**Note 1:** Default peripheral input. Input can be moved to any other pin with the PPS input selection registers.

**2:** All pin outputs default to PORT latch data. Any pin can be selected as a digital peripheral output with the PPS output selection registers.

**3:** These peripheral functions are bidirectional. The output pin selections must be the same as the input pin selections.

**4:** These pins are configured for I<sup>2</sup>C logic levels; clock and data signals may be assigned to any of these pins. Assignments to other pins (e.g. RA5) will operate, but I<sup>2</sup>C will not operate as selected by the INLV register.

**TABLE 7: 14/16-PIN ALLOCATION TABLE (PIC16(L)F18326) (CONTINUED)**

I/O <sup>(2)</sup>	14/16-Pin PDIP/SOIC/TSSOP	16-Pin UQFN	ADC	Reference	Comparator	NCO	DAC	DSM	Timers	CCP	PWM	CWG	MSSP	EUSART	CLC
OUT <sup>(2)</sup>	—	—	—	—	C1OUT	DDS	—	DSM	TMR0	CCP1	PWM5	CWG1A CWG2A	SDA1 <sup>(3)</sup> SDA2 <sup>(3)</sup>	CK	CLC1OUT
	—	—	—	—	C2OUT	—	—	—	—	CCP2	PWM6	CWG1B CWG2B	SCL1 <sup>(3)</sup> SCL2 <sup>(3)</sup>	DT <sup>(3)</sup>	CLC2OUT
	—	—	—	—	—	—	—	—	—	CCP3	—	CWG1C CWG2C	SDO1 SDO2	TX	CLC3OUT
	—	—	—	—	—	—	—	—	—	CCP4	—	CWG1D CWG2D	SCK1 SCK2	—	CLC4OUT

**Note 1:** Default peripheral input. Input can be moved to any other pin with the PPS input selection registers.

**2:** All pin outputs default to PORT latch data. Any pin can be selected as a digital peripheral output with the PPS output selection registers.

**3:** These peripheral functions are bidirectional. The output pin selections must be the same as the input pin selections.

**4:** These pins are configured for I<sup>2</sup>C logic levels; clock and data signals may be assigned to any of these pins. Assignments to other pins (e.g. RA5) will operate, but I<sup>2</sup>C will not operate in TTL/ST as selected by the INLVL register.

**TABLE 8: 20-PIN ALLOCATION TABLE (PIC16(L)F18344)**

I/O <sup>(2)</sup>	20-Pin PDIP/SOIC/SSOP	20-Pin UQFN	ADC	Reference	Comparator	NCO	DAC	DSM	Timers	CCP	PWM	CWG	MSSP	EUSART	CLC
RA0	19	16	ANA0	—	C1IN0+	—	DAC1OUT	—	—	—	—	—	—	—	—
RA1	18	15	ANA1	VREF +	C1IN0- C2IN0-	—	DAC1REF+	—	—	—	—	—	—	—	—
RA2	17	14	ANA2	VREF-	—	—	DAC1REF-	—	T0CK1 <sup>(1)</sup>	CCP3 <sup>(1)</sup>	—	CWG1 <sup>(1)</sup> CWG2 <sup>(1)</sup>	—	—	CLCIN0 <sup>(1)</sup>
RA3	4	1	—	—	—	—	—	—	—	—	—	—	—	—	—
RA4	3	20	ANA4	—	—	—	—	—	T1G <sup>(1)</sup> T3G <sup>(1)</sup> T5G <sup>(1)</sup> SOSCO	CCP4 <sup>(1)</sup>	—	—	—	—	—
RA5	2	19	ANA5	—	—	—	—	—	T1CK <sup>(1)</sup> T3CK <sup>(1)</sup> T5CK <sup>(1)</sup> SOSCIN SOSCI	—	—	—	—	—	—
RB4	13	10	ANB4	—	—	—	—	—	—	—	—	—	SD1 <sup>(1)</sup> SDA <sup>(1,3,4)</sup>	—	CLCIN2 <sup>(1)</sup>
RB5	12	9	ANB5	—	—	—	—	—	—	—	—	—	—	RX <sup>(1)</sup> DT <sup>(1)</sup>	CLCIN3 <sup>(1)</sup>
RB6	11	8	ANB6	—	—	—	—	—	—	—	—	—	SC1 <sup>(1)</sup> SCL <sup>(1,3,4)</sup>	—	—
RB7	10	7	ANB7	—	—	—	—	—	—	—	—	—	—	TX <sup>(1)</sup> CK <sup>(1)</sup>	—
RC0	16	13	ANC0	—	C2IN0+	—	—	—	—	—	—	—	—	—	—
RC1	15	12	ANC1	—	C1IN1- C2IN1-	—	—	—	—	—	—	—	—	—	—
RC2	14	11	ANC2	—	C1IN2- C2IN2-	—	—	MDCIN1 <sup>(1)</sup>	—	—	—	—	—	—	—

**Note 1:** Default peripheral input. Input can be moved to any other pin with the PPS input selection registers.

**2:** All pin outputs default to PORT latch data. Any pin can be selected as a digital peripheral output with the PPS output selection registers.

**3:** These peripheral functions are bidirectional. The output pin selections must be the same as the input pin selections.

**4:** These pins are configured for I<sup>2</sup>C logic levels; clock and data signals may be assigned to any of these pins. Assignments to other pins (e.g., RA5) will operate, but TTL/ST as selected by the INLVL register.

**TABLE 8: 20-PIN ALLOCATION TABLE (PIC16(L)F18344) (CONTINUED)**

I/O <sup>(2)</sup>	20-Pin PDIP/SOIC/SSOP	20-Pin UQFN	ADC	Reference	Comparator	NCO	DAC	DSM	Timers	CCP	PWM	CWG	MSSP	EUSART	CLC
RC3	7	4	ANC3	—	C1IN3- C2IN3-	—	—	MDMIN <sup>(1)</sup>	—	CCP2 <sup>(1)</sup>	—	—	—	—	CLCIN1 <sup>(1)</sup>
RC4	6	3	ANC4	—	—	—	—	—	—	—	—	—	—	—	—
RC5	5	2	ANC5	—	—	—	—	MDCIN2 <sup>(1)</sup>	—	CCP1 <sup>(1)</sup>	—	—	—	—	—
RC6	8	5	ANC6	—	—	—	—	—	—	—	—	—	SS <sup>(1)</sup>	—	—
RC7	9	6	ANC7	—	—	—	—	—	—	—	—	—	—	—	—
V <sub>DD</sub>	1	18	—	—	—	—	—	—	—	—	—	—	—	—	—
V <sub>SS</sub>	20	17	—	—	—	—	—	—	—	—	—	—	—	—	—
OUT <sup>(2)</sup>	—	—	—	—	C1OUT	NCO	—	DSM	TMR0	CCP1	PWM5	CWG1A CWG2A	SDO	DT <sup>(3)</sup>	CLC1OUT
	—	—	—	—	C2OUT	—	—	—	—	CCP2	PWM6	CWG1B CWG2B	SCK	CK	CLC2OUT
	—	—	—	—	—	—	—	—	—	CCP3	—	CWG1C CWG2C	SCL <sup>(3)</sup>	TX	CLC3OUT
	—	—	—	—	—	—	—	—	—	CCP4	—	CWG1D CWG2D	SDA <sup>(3)</sup>	—	CLC4OUT

**Note 1:** Default peripheral input. Input can be moved to any other pin with the PPS input selection registers.

**2:** All pin outputs default to PORT latch data. Any pin can be selected as a digital peripheral output with the PPS output selection registers.

**3:** These peripheral functions are bidirectional. The output pin selections must be the same as the input pin selections.

**4:** These pins are configured for I<sup>2</sup>C logic levels; clock and data signals may be assigned to any of these pins. Assignments to other pins (e.g., RA5) will operate, but TTL/ST as selected by the INLVL register.

**TABLE 9: 20-PIN ALLOCATION TABLE (PIC16(L)F18345)**

I/O <sup>(2)</sup>	20-Pin PDIP/SOIC/SOP	20-Pin UQFN	ADC	Reference	Comparator	NCO	DAC	DSM	Timers	CCP	PWM	CWG	MSSP	EUSART	CLC	
RA0	19	16	ANA0	—	C1IN0+	—	DAC1OUT	—	—	—	—	—	—	—	—	
RA1	18	15	ANA1	VREF +	C1IN0- C2IN0-	—	DAC1REF+	—	—	—	—	—	SS2 <sup>(1)</sup>	—	—	
RA2	17	14	ANA2	VREF-	—	—	DAC1REF-	—	T0CK1 <sup>(1)</sup>	CCP3 <sup>(1)</sup>	—	CWG1 <sup>(1)</sup> CWG2 <sup>(1)</sup>	—	—	CLCIN0 <sup>(1)</sup>	
RA3	4	1	—	—	—	—	—	—	—	—	—	—	—	—	—	
RA4	3	20	ANA4	—	—	—	—	—	T1G <sup>(1)</sup> T3G <sup>(1)</sup> T5G <sup>(1)</sup> SOSCO	CCP4 <sup>(1)</sup>	—	—	—	—	—	
RA5	2	19	ANA5	—	—	—	—	—	T1CK1 <sup>(1)</sup> T3CK1 <sup>(1)</sup> T5CK1 <sup>(1)</sup> SOSCIN SOSCI	—	—	—	—	—	—	
RB4	13	10	ANB4	—	—	—	—	—	—	—	—	—	SD1 <sup>(1)</sup> SDA1 <sup>(1,3,4)</sup>	—	CLCIN2 <sup>(1)</sup>	
RB5	12	9	ANB5	—	—	—	—	—	—	—	—	—	SD2 <sup>(1)</sup> SDA2 <sup>(1,3,4)</sup>	RX <sup>(1)</sup> DT <sup>(1)</sup>	CLCIN3 <sup>(1)</sup>	
RB6	11	8	ANB6	—	—	—	—	—	—	—	—	—	SCK1 <sup>(1)</sup> SCL1 <sup>(1,3,4)</sup>	—	—	
RB7	10	7	ANB7	—	—	—	—	—	—	—	—	—	SCK2 <sup>(1)</sup> SCL2 <sup>(1,3,4)</sup>	TX <sup>(1)</sup> CK <sup>(1)</sup>	—	
RC0	16	13	ANC0	—	C2IN0+	—	—	—	—	—	—	—	—	—	—	—
RC1	15	12	ANC1	—	C1IN1- C2IN1-	—	—	—	—	—	—	—	—	—	—	—
RC2	14	11	ANC2	—	C1IN2- C2IN2-	—	—	MDCIN1 <sup>(1)</sup>	—	—	—	—	—	—	—	—
RC3	7	4	ANC3	—	C1IN3- C2IN3-	—	—	MDMIN <sup>(1)</sup>	—	CCP2 <sup>(1)</sup>	—	—	—	—	—	CLCIN1 <sup>(1)</sup>

**Note 1:** Default peripheral input. Input can be moved to any other pin with the PPS input selection registers.

**Note 2:** All pin outputs default to PORT latch data. Any pin can be selected as a digital peripheral output with the PPS output selection registers.

**Note 3:** These peripheral functions are bidirectional. The output pin selections must be the same as the input pin selections.

**Note 4:** These pins are configured for I<sup>2</sup>C logic levels; clock and data signals may be assigned to any of these pins. Assignments to other pins (e.g., RA5) will operate, but TTL/ST as selected by the INLVL register.

**TABLE 9: 20-PIN ALLOCATION TABLE (PIC16(L)F18345) (CONTINUED)**

I/O <sup>(2)</sup>	20-Pin PDIP/SOIC/SSOP	20-Pin UQFN	ADC	Reference	Comparator	NCO	DAC	DSM	Timers	CCP	PWM	CWG	MSSP	EUSART	CLC
RC4	6	3	ANC4	—	—	—	—	—	—	—	—	—	—	—	—
RC5	5	2	ANC5	—	—	—	—	MDCIN2 <sup>(1)</sup>	CCP1 <sup>(1)</sup>	—	—	—	—	—	—
RC6	8	5	ANC6	—	—	—	—	—	—	—	—	—	SS <sup>(1)</sup>	—	—
RC7	9	6	ANC7	—	—	—	—	—	—	—	—	—	—	—	—
VDD	1	18	—	—	—	—	—	—	—	—	—	—	—	—	—
VSS	20	17	—	—	—	—	—	—	—	—	—	—	—	—	—
OUT <sup>(2)</sup>	—	—	—	—	C1OUT	NCO	—	DSM	TMR0	CCP1	PWM5	CWG1A CWG2A	SDO1 SDO2	DT <sup>(3)</sup>	CLC1OUT
	—	—	—	—	C2OUT	—	—	—	—	CCP2	PWM6	CWG1B CWG2B	SCK1 SCK2	CK	CLC2OUT
	—	—	—	—	—	—	—	—	—	CCP3	—	CWG1C CWG2C	SCL1 <sup>(3)</sup> SCL2 <sup>(3)</sup>	TX	CLC3OUT
	—	—	—	—	—	—	—	—	—	CCP4	—	CWG1D CWG2D	SDA1 <sup>(3)</sup> SDA2 <sup>(3)</sup>	—	CLC4OUT

**Note 1:** Default peripheral input. Input can be moved to any other pin with the PPS input selection registers.

**Note 2:** All pin outputs default to PORT latch data. Any pin can be selected as a digital peripheral output with the PPS output selection registers.

**Note 3:** These peripheral functions are bidirectional. The output pin selections must be the same as the input pin selections.

**Note 4:** These pins are configured for I<sup>2</sup>C logic levels; clock and data signals may be assigned to any of these pins. Assignments to other pins (e.g., RA5) will operate, but not TTL/ST as selected by the INLV register.

TABLE 10: 20-PIN ALLOCATION TABLE (PIC16(L)F18346)

I/O <sup>(2)</sup>	20-Pin PDIP/SOIC/SSOP	20-Pin UQFN	ADC	Reference	Comparator	NCO	DAC	DSM	Timers	CCP	PWM	CWG	MSSP	EUSART	CLC
RA0	19	16	ANA0	—	C1IN0+	—	DAC1OUT	—	—	—	—	—	—	—	—
RA1	18	15	ANA1	VREF +	C1IN0- C2IN0-	—	DAC1REF+	—	—	—	—	—	SS2 <sup>(1)</sup>	—	—
RA2	17	14	ANA2	VREF-	—	—	DAC1REF-	—	T0CK <sup>(1)</sup>	CCP3 <sup>(1)</sup>	—	CWG1 <sup>(1)</sup> CWG2 <sup>(1)</sup>	—	—	CLCIN0 <sup>(1)</sup>
RA3	4	1	—	—	—	—	—	—	—	—	—	—	—	—	—
RA4	3	20	ANA4	—	—	—	—	—	T1G <sup>(1)</sup> T3G <sup>(1)</sup> T5G <sup>(1)</sup> SOSCO	CCP4 <sup>(1)</sup>	—	—	—	—	—
RA5	2	19	ANA5	—	—	—	—	—	T1CK <sup>(1)</sup> T3CK <sup>(1)</sup> T5CK <sup>(1)</sup> SOSCIN SOSCI	—	—	—	—	—	—
RB4	13	10	ANB4	—	—	—	—	—	—	—	—	—	SD1 <sup>(1)</sup> SDA1 <sup>(1,3,4)</sup>	—	CLCIN2 <sup>(1)</sup>
RB5	12	9	ANB5	—	—	—	—	—	—	—	—	—	SD2 <sup>(1)</sup> SDA2 <sup>(1,3,4)</sup>	RX <sup>(1)</sup> DT <sup>(1)</sup>	CLCIN3 <sup>(1)</sup>
RB6	11	8	ANB6	—	—	—	—	—	—	—	—	—	SC1 <sup>(1)</sup> SCL1 <sup>(1,3,4)</sup>	—	—
RB7	10	7	ANB7	—	—	—	—	—	—	—	—	—	SCK2 <sup>(1)</sup> SCL2 <sup>(1,3,4)</sup>	TX <sup>(1)</sup> CK <sup>(1)</sup>	—
RC0	16	13	ANC0	—	C2IN0+	—	—	—	—	—	—	—	—	—	—
RC1	15	12	ANC1	—	C1IN1- C2IN1-	—	—	—	—	—	—	—	—	—	—
RC2	14	11	ANC2	—	C1IN2- C2IN2-	—	—	MDCIN1 <sup>(1)</sup>	—	—	—	—	—	—	—

**Note 1:** Default peripheral input. Input can be moved to any other pin with the PPS input selection registers.

**2:** All pin outputs default to PORT latch data. Any pin can be selected as a digital peripheral output with the PPS output selection registers.

**3:** These peripheral functions are bidirectional. The output pin selections must be the same as the input pin selections.

**4:** These pins are configured for I<sup>2</sup>C logic levels; clock and data signals may be assigned to any of these pins. Assignments to other pins (e.g., RA5) will operate, but TTL/ST as selected by the INLVL register.

**TABLE 10: 20-PIN ALLOCATION TABLE (PIC16(L)F18346) (CONTINUED)**

I/O <sup>(2)</sup>	20-Pin PDIP/SOIC/SSOP	20-Pin UQFN	ADC	Reference	Comparator	NCO	DAC	DSM	Timers	CCP	PWM	CWG	MSSP	EUSART	CLC
RC3	7	4	ANC3	—	C1IN3- C2IN3-	—	—	MDMIN <sup>(1)</sup>	—	CCP2 <sup>(1)</sup>	—	—	—	—	CLCIN1 <sup>(1)</sup>
RC4	6	3	ANC4	—	—	—	—	—	—	—	—	—	—	—	—
RC5	5	2	ANC5	—	—	—	—	MDCIN2 <sup>(1)</sup>	—	CCP1 <sup>(1)</sup>	—	—	—	—	—
RC6	8	5	ANC6	—	—	—	—	—	—	—	—	—	SS <sup>(1)</sup>	—	—
RC7	9	6	ANC7	—	—	—	—	—	—	—	—	—	—	—	—
V <sub>DD</sub>	1	18	—	—	—	—	—	—	—	—	—	—	—	—	—
V <sub>SS</sub>	20	17	—	—	—	—	—	—	—	—	—	—	—	—	—
OUT <sup>(2)</sup>	—	—	—	—	C1OUT	NCO	—	DSM	TMR0	CCP1	PWM5	CWG1A CWG2A	SDO1 SDO2	DT <sup>(3)</sup>	CLC1OUT
	—	—	—	—	C2OUT	—	—	—	—	CCP2	PWM6	CWG1B CWG2B	SK1 SK2	CK	CLC2OUT
	—	—	—	—	—	—	—	—	—	CCP3	—	CWG1C CWG2C	SCL1 <sup>(3)</sup> SCL2 <sup>(3)</sup>	TX	CLC3OUT
	—	—	—	—	—	—	—	—	—	CCP4	—	CWG1D CWG2D	SDA1 <sup>(3)</sup> SDA2 <sup>(3)</sup>	—	CLC4OUT

**Note 1:** Default peripheral input. Input can be moved to any other pin with the PPS input selection registers.

**2:** All pin outputs default to PORT latch data. Any pin can be selected as a digital peripheral output with the PPS output selection registers.

**3:** These peripheral functions are bidirectional. The output pin selections must be the same as the input pin selections.

**4:** These pins are configured for I<sup>2</sup>C logic levels; clock and data signals may be assigned to any of these pins. Assignments to other pins (e.g., RA5) will operate, but TTL/ST as selected by the INLVL register.

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#### India - Pune

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#### Korea - Seoul

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