PIC16(L)F1782/1783 Family Silicon Errata and Data Sheet Clarification

The PIC16(L)F1782/1783 family devices that you have received conform functionally to the current Device Data Sheet (DS41579**D**), except for the anomalies described in this document.

The silicon issues discussed in the following pages are for silicon revisions with the Device and Revision IDs listed in Table 1. The silicon issues are summarized in Table 2.

The errata described in this document will be addressed in future revisions of the PIC16(L)F1782/1783 silicon.

Note:	This document summarizes all silicon errata issues from all revisions of silicon, previous as well as current. Only the issues indicated in the last column of Table 2 apply to the current silicon revision (**B4**).

Data Sheet clarifications and corrections start on page 10, following the discussion of silicon issues.

The silicon revision level can be identified using the current version of MPLAB® IDE and Microchip's programmers, debuggers, and emulation tools, which are available at the Microchip corporate web site (www.microchip.com).

For example, to identify the silicon revision level using MPLAB IDE in conjunction with a hardware debugger:

1. Using the appropriate interface, connect the device to the hardware debugger.
2. Open an MPLAB IDE project.
3. Configure the MPLAB IDE project for the appropriate device and hardware debugger.
4. Based on the version of MPLAB IDE you are using, do one of the following:
   a) For MPLAB IDE 8, select *Programmer > Reconnect*.
   b) For MPLAB X IDE, select *Window > Dashboard* and click the **Refresh Debug Tool Status** icon ( ).
5. Depending on the development tool used, the part number *and* Device Revision ID value appear in the **Output** window.

Note:	If you are unable to extract the silicon revision level, please contact your local Microchip sales office for assistance.

The DEVREV values for the various PIC16(L)F1782/1783 silicon revisions are shown in Table 1.

TABLE 1: SILICON DEVREV VALUES

Part Number	DEVICE ID<13:0>(1),(2)		
	DEV<8:0>	REV<4:0> Silicon Revision	
		B2	B4
PIC16F1782	01 0111 000	0 0110	0 1000
PIC16LF1782	01 0111 001	0 0110	0 1000
PIC16F1783	01 0110 010	0 0110	0 1000
PIC16LF1783	01 0111 010	0 0110	0 1000

Note 1: The Device ID is located in the configuration memory at address 8006h.

2: Refer to the *"PIC16(L)F178X Memory Programming Specification"* (DS41457) for detailed information on Device and Revision IDs for your specific device.

TABLE 2: SILICON ISSUE SUMMARY

Module	Feature	Item Number	Issue Summary	Affected Revisions(1)	
				B2	B4
ADC	FOSC/2	1.1	FOSC/2 not functional.	X	
ADC	Offset	1.2	Time between conversions affects offset.	X	
ADC	INL (12-bit mode)	1.3	INL is ±4 LSb.	X	
ADC	FRC	1.4	ADC not functional if using FRC with FOSC<2 MHz.	X	
Op Amp	Offset	2.1	Offset increases when Common mode <200 mV.	X	
Comparator	Low-Power mode	3.1	Improper Low-Power mode operation.	X	X
Comparator	Typical Offset Performance mode	3.2	Normal Speed mode.	X	
Data EEPROM	Endurance	4.1	Limited to 10k cycles, VDD <2.3V, PIC16LF1782/1783.	X	
HF Internal Oscillator	Clock Switching	5.1	Clock switching can cause a single corrupted instruction.	X	
PSMC	Rising Edge Input	6.1	Period and falling edge race condition.	X	X
PSMC	Auto-shutdown	6.2	Failure to auto-restart after shutdown from comparator.	X	
Low-Dropout (LDO) Voltage Regulator	Low-Power Sleep	7.1	Unexpected Resets may occur at ambient temperatures below 0°C.	X	X
FVR	FVR Module	8.1	Use of FVR module can cause device to Reset.	X	X
PFM	PFM Self-Write	9.1	PFM self-write will not work depending on clock selection.		X

Note 1: Only those issues indicated in the last column apply to the current silicon revision.

Silicon Errata Issues

Note:	This document summarizes all silicon errata issues from all revisions of silicon, previous as well as current. Only the issues indicated by the shaded column in the following tables apply to the current silicon revision (**B4**).

1. Module: ADC

1.1 Operation with FOSC/2

The ADC is not functional when the ADCS<2:0> bits of ADCON1 select the FOSC/2 frequency.

Work around

Use the FRC selection which provides a valid TAD time, regardless of the system clock frequency.

Affected Silicon Revisions

B2	B4						
X							

1.2 ADC Offset

The offset error exceeds the data sheet specification when the time between conversions is greater than 100 us.

Work around

The time dependent error is insignificant when the time between conversions is less than 100 us. When the time between conversions is greater than 100 us, take two back-to-back ADC conversions and discard the results of the first conversion.

Affected Silicon Revisions

B2	B4						
X							

1.3 ADC INL (12-bit mode)

The ADC linearity is ±4 LSb for the 12-bit mode. Below are typical INL graphs in 12-bit mode (See Figure 1 and Figure 2).

Work around

None.

Affected Silicon Revisions

B2	B4						
X							

FIGURE 1: ADC 12-BIT MODE, SINGLE-ENDED INL, VDD = 3.0V, TAD = 4 us, 25°C, TYPICAL MEASURED VALUES

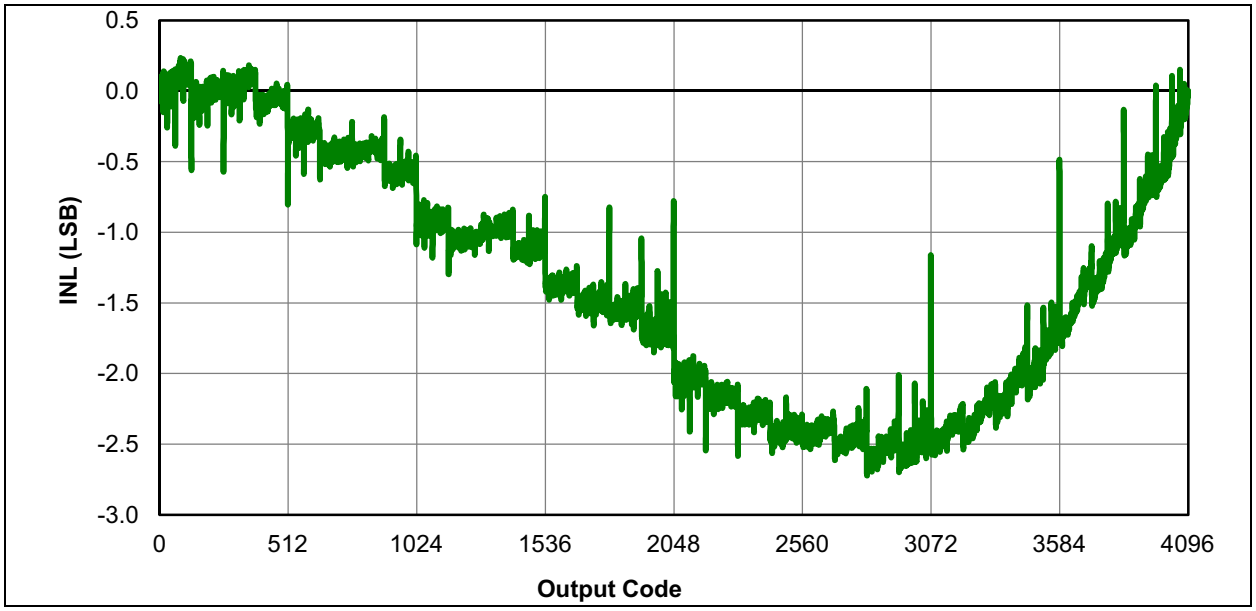
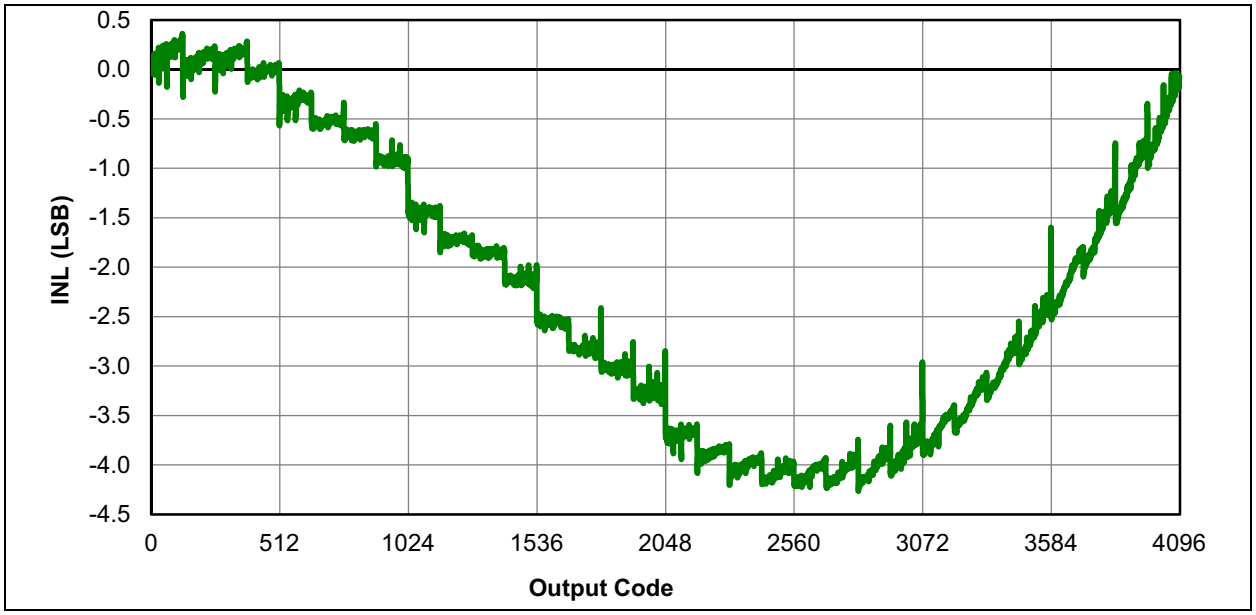


FIGURE 2: ADC 12-BIT MODE, SINGLE-ENDED INL, VDD = 5.5V, TAD = 4 us, 25°C, TYPICAL MEASURED VALUES



1.4 Incorrect Readings if using Fosc<2 MHz

The ADC is not functional if using FRC with FOSC frequencies less than 2 MHz.

Work around

Use frequencies greater than 2 MHz for correct ADC functionality.

Affected Silicon Revisions

B2	B4						
X							

2. Module: Op Amp

2.1 Offset at Low Common Mode

The op amp offset at Common mode input voltages below 200 mV increases with respect to temperature. Below are typical graphs showing the increase in offset (See Figure 3, Figure 4 and Figure 5).

Work around

None.

Affected Silicon Revisions

B2	B4						
X							

FIGURE 3: OP AMP TYPICAL OFFSET VOLTAGE AT 25°C, HIGH GBWP MODE (OPAxSP = 1), VDD = 3.6V, 0V ≤ CMV ≤ 5.5V

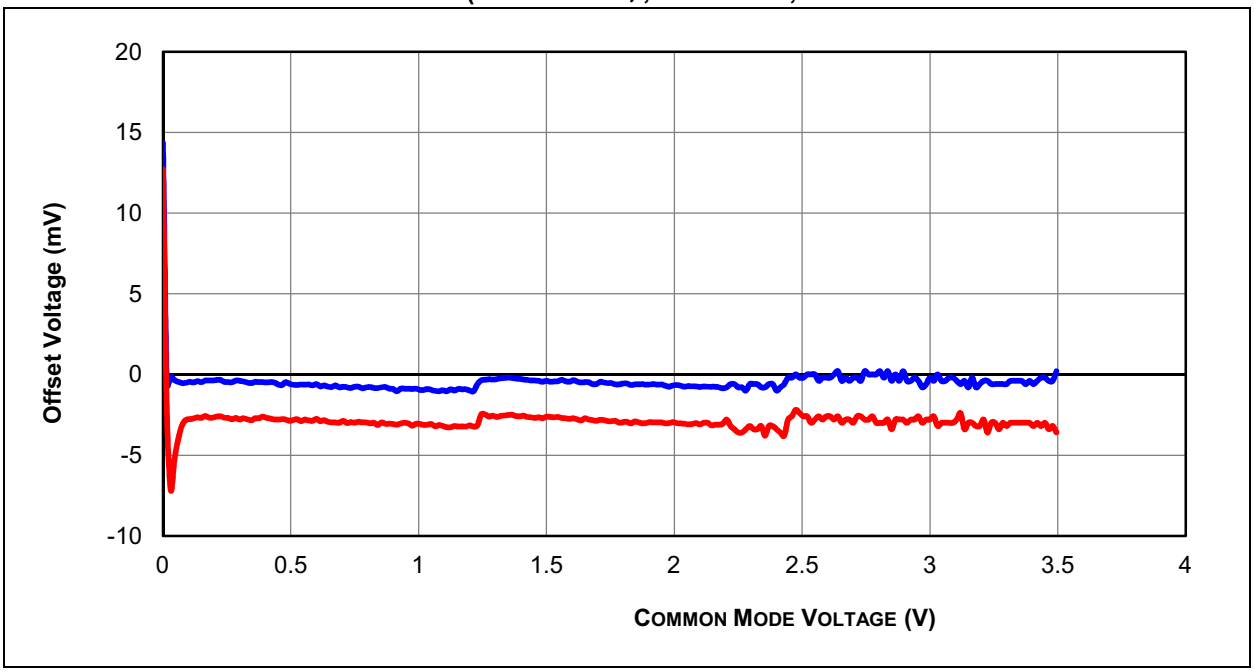


FIGURE 4: **OP AMP TYPICAL OFFSET VOLTAGE AT LOW VCM, 85°C, HIGH GBWP MODE (OPAxSP = 1), VDD = 3.6V, 0V ≤ CMV ≤ 0.5V**

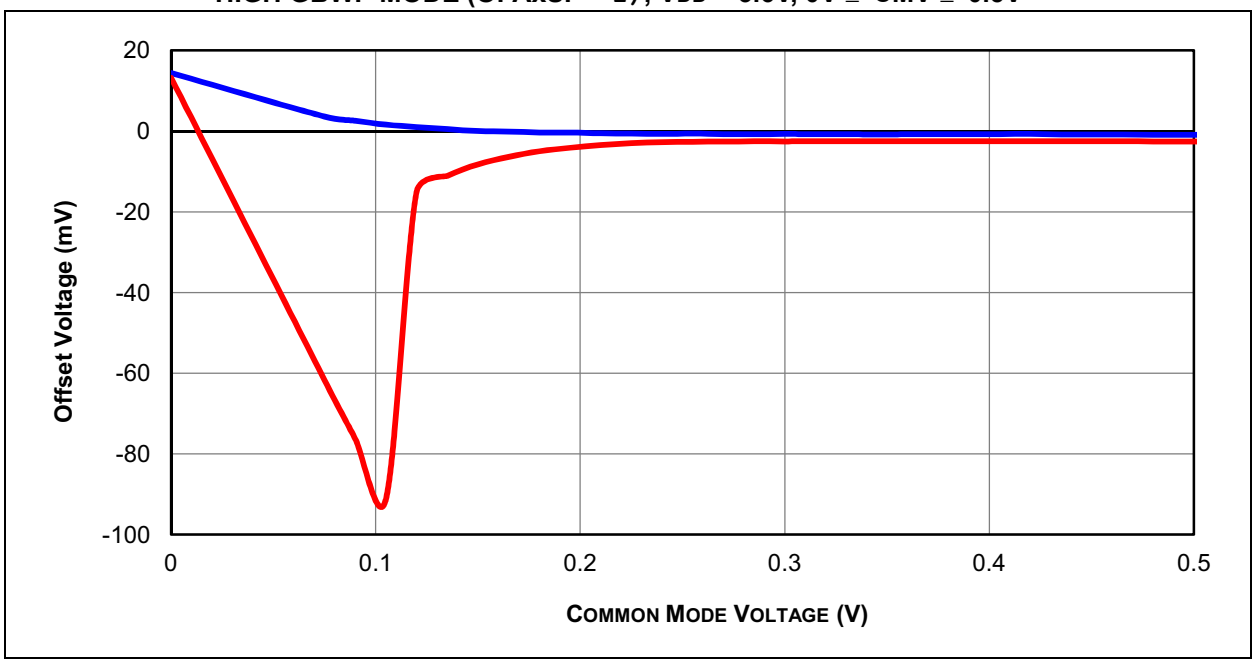
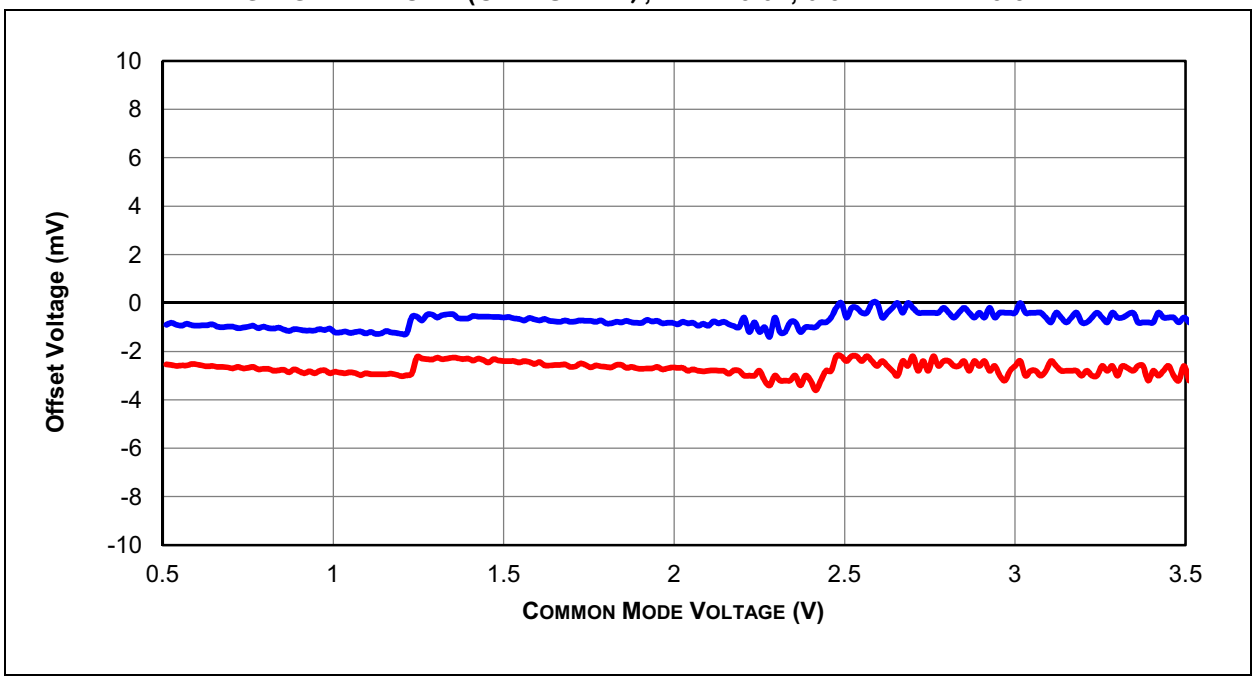


FIGURE 5: **OP AMP TYPICAL OFFSET VOLTAGE AT 85°C, HIGH GBWP MODE (OPAxSP = 1), VDD = 3.6V, 0.5V ≤ CMV ≤ 3.5V**



3. Module: Comparator

3.1 No Low-Power, No Low-Speed Mode

The comparator operation in Low-Power, Low-Speed mode (CxSP = 0) may not perform properly.

Work around

Use the comparator in High Power mode.

Affected Silicon Revisions

B2	B4						
X	X						

3.2 Typical Offset Performance

CMRR performance for the range of VSS + 1V to VDD - 1V is better than specified in the data sheet.

Work around

See Figure 6 and Figure 7.

Affected Silicon Revisions

B2	B4						
X							

FIGURE 6: COMPARATOR INPUT OFFSET, TYPICAL MEASURED VALUES, NORMAL SPEED MODE (CxSP = 1), VDD = 5.5V, PIC16F1782/1783 ONLY

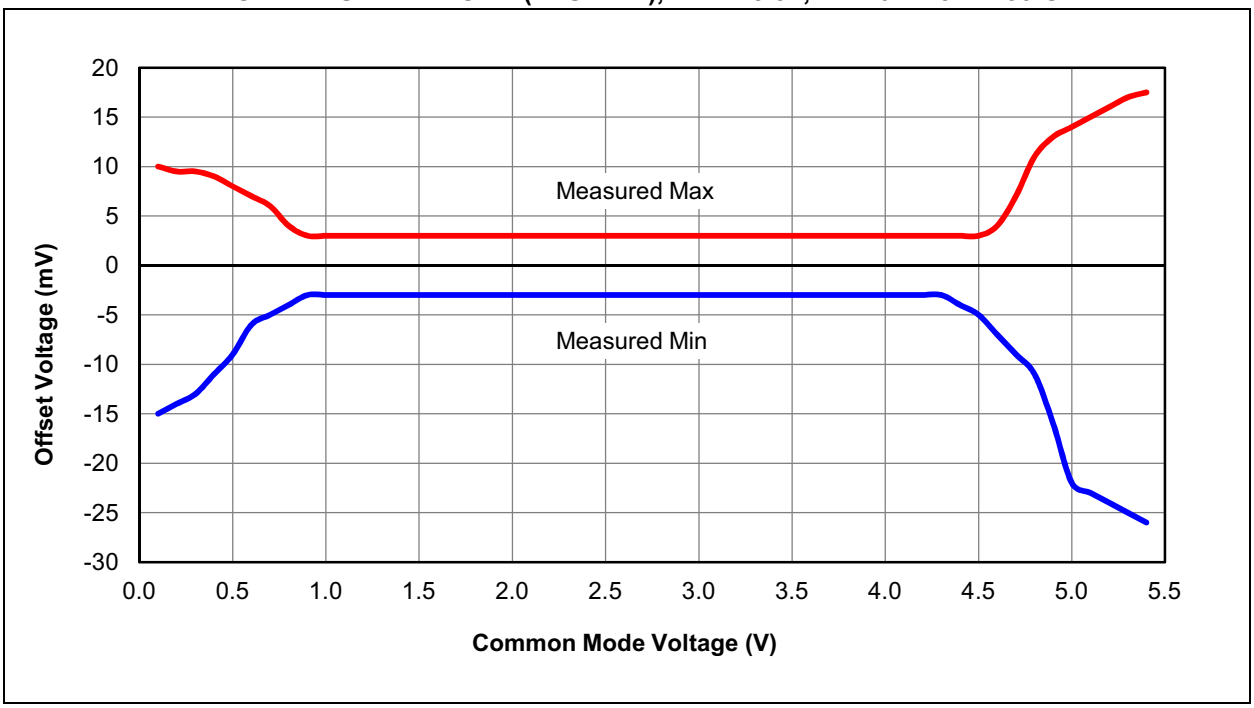
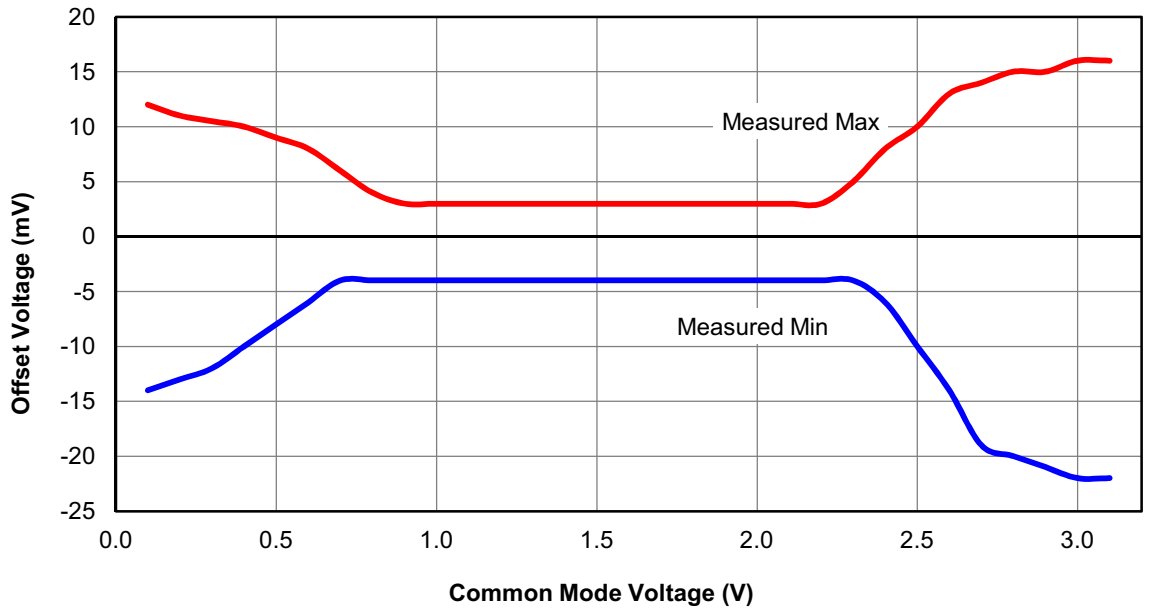


FIGURE 7: COMPARATOR INPUT OFFSET, TYPICAL MEASURED VALUES, NORMAL SPEED MODE (CxSP = 1), VDD = 3.2V



4. Module: Data EEPROM

4.1 Endurance of the Data EEPROM is 10k

The write/erase endurance of the data EE memory is limited to 10k cycles when VDD <2.3V. This errata applies to the PIC16LF1782/1783 only.

Work around

Use an error correction method that stores data in multiple locations.

Affected Silicon Revisions

B2	B4						
X							

5. Module: HF Internal Oscillator

5.1 Clock Switching

When switching clock sources between INTOSC clock source and an external clock source, one corrupted instruction may be executed after the switch occurs.

This issue affects Two-Speed Start-up operation.

Work around

When switching from an external oscillator clock source, first switch to 16 MHz HFINTOSC. Once running at 16 MHz HFINTOSC, configure IRCF to run at desired internal oscillator frequency.

When switching from an internal oscillator (INTOSC) to an external oscillator clock source, first switch to HFINTOSC High-Power mode (8 MHz or 16 MHz). Once running from HFINTOSC, switch to the external oscillator clock source.

Affected Silicon Revisions

B2	B4						
X							

6. Module: PSMC

6.1 Rising Edge Inhibit

When the period and falling edge sources are from the same asynchronous input, then a race condition may occur where the period is detected before the falling edge. When this occurs, then the falling edge properly terminates the cycle but subsequent rising edge inputs are ignored.

Work around

To configure the PSMC for fixed off-time and variable frequency, set the following:

- Period = Asynchronous feedback
- Rising Event = Synchronous @ PSMCxPH = 0
- Falling Event = Synchronous @ PSMCxDC = Off Time
- Output inverted so drive time is from falling event to period event.

Affected Silicon Revisions

B2	B4						
X	X						

6.2 Auto-Restart

When auto-shutdown is configured for auto-restart and the shutdown source is a comparator, then auto-restart may fail to occur after the shutdown condition ceases.

Work around

Enable the zero-latency filter of the comparator used for auto-shutdown.

Affected Silicon Revisions

B2	B4						
X							

7. Module: Low-Dropout (LDO) Voltage Regulator

7.1 Low-Power Sleep mode at ambient temperatures below 0°C

Under the following conditions:

- ambient temperatures below 0°C
- while in Sleep mode
- VREGCON configured for Low-Power Sleep mode (VREGPM = 1)

On very rare occasions, the LDO voltage will drop below the minimum VDD, causing unexpected device Resets.

Work around

For applications that operate at ambient temperatures below 0°C, use the LDO voltage regulator in Normal-Power mode (VREGPM = 0).

Affected Silicon Revisions

B2	B4						
X	X						

8. Module: FVR

8.1 FVR Module

When using the FVR module, if the gain amplifier outputs are set via the CDAFVR or ADFVR bits in FVRCON while the module is disabled (FVREN = 0), the internal oscillator frequency may shift, device current consumption can increase, and a Brown-out Reset may occur. Additionally, after the FVREN is enabled, a switch from 4x to 1x can also cause a Reset.

Work around

Set the FVREN bit of FVRCON to enable the module prior to adjusting the amplifier output selections with the CDAFVR and ADFVR bits. Always set the amplifier output selections to off ('00') before disabling the FVR module.

When switching from 4x to 1x, first switch from 4x to 2x and then from 2x to 1x.

Affected Silicon Revisions

B2	B4						
X	X						

9. Module: PFM Self-Writes

9.1 PFM

Writes to the PFM will not execute if the device's clock source is HS, ECH, or the Internal oscillator is at either 8 MHz or 16 MHz. The DFM is unaffected.

Work around

To write to the PFM, the clock source must be one of the following settings: Internal oscillator set to 4 MHz or lower, ECM, ECL, XT, External RC, LP or T1OSC.

Affected Silicon Revisions

B2	B4						
	X						

Data Sheet Clarifications

The following typographic corrections and clarifications are to be noted for the latest version of the device data sheet (DS41579**D**):

Note:	Corrections are shown in **bold**. Where possible, the original bold text formatting has been removed for clarity.

None.

APPENDIX A: DOCUMENT REVISION HISTORY

Rev A Document (03/2012)

Initial release of this document.

Rev B Document (07/2012)

Added MPLAB X IDE; Added Silicon Revision B4; Updated Module 6.1; Added Modules 6.2, 7, 8 and 9.

Rev C Document (09/2012)

Removed Silicon Revision B4 from Module 4, Data EEPROM.

Rev D Document (05/2014)

Added Module 1.4; Other minor corrections.

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