
8/14/20-Pin, 8-Bit Flash Microcontroller Product Brief

Description:

PIC12/16(L)F161X microcontrollers deliver on-chip features that are unique to the design for embedded control of small motors and general purpose applications in 8/14/20-pin count packages. Features like 10-bit A/D, CCP, 24-bit SMT and Zero-Cross Detection offer an excellent solution to the variety of applications. The product family also has a CRC+ memory scan and Windowed WDT to support safety-critical systems in home appliances, white goods and other end equipment.

Core Features:

- C Compiler Optimized RISC Architecture
- Only 49 Instructions
- Operating Speed:
 - DC – 32 MHz clock input
 - 125 ns minimum instruction cycle
- Interrupt Capability
- 16-Level Deep Hardware Stack
- Up to Four 8-bit Timers
- Up to Three 16-bit Timers
- Low Current Power-on Reset (POR)
- Configurable Power-up Timer (PWRT)
- Brown-out Reset (BOR) with Selectable Trip Point
- Window Watchdog Timer (WWDT):
 - Variable prescaler selection
 - Variable window size selection
 - All sources configurable in hardware or software

Memory:

- Up to 8 KW Flash Program Memory
- Up to 1024 Bytes Data SRAM Memory
- Direct, Indirect and Relative Addressing modes
- High-Endurance Flash Data Memory (HEF):
 - 128 B (nonvolatile), 100K Erase/Write Cycles

Operating Characteristics:

- Operating Voltage Range:
 - 1.8V to 3.6V (PIC16LF161X)
 - 2.3V to 5.5V (PIC16F161X)
- Temperature Range:
 - Industrial: -40°C to 85°C
 - Extended: -40°C to 125°C

eXtreme Low-Power (XLP) Features:

- Sleep mode: 50 nA @ 1.8V, typical
- Watchdog Timer: 500 nA @ 1.8V, typical
- Secondary Oscillator: 500 nA @ 32 kHz
- Operating Current:
 - 8 uA @ 32 kHz, 1.8V, typical
 - 32 uA/MHz @ 1.8V, typical

Digital Peripherals:

- Configurable Logic Cell (CLC):
 - Up to four CLCs
 - Integrated combinational and sequential logic
- Complementary Waveform Generator (CWG):
 - Rising and falling edge dead-band control
 - Full-bridge, half-bridge, 1-channel drive
 - Multiple signal sources
- Two Capture/Compare/PWM (CCP) modules
- PWM: Two 10-bit Pulse-Width Modulators
- Two Signal Measurement Timers (SMT):
 - 24-bit timer/counter with prescaler
 - Multiple gate and clock inputs
- Angular Timer:
 - Single pulse
 - Multiple pulses with missing pulse recovery
- Hardware Limit Timer (HLT):
 - 8-bit timer with prescaler
 - 8-bit period register and postscaler
 - Asynchronous H/W reset sources
- Math Accelerator:
 - Four operation modes
 - Add and multiply
 - Simple multiplier
 - Multiply and Accumulate (MAC)
 - Programmable PID controller
- Cyclic Redundancy Check with Memory Scan (CRC):
 - Software configurable
- Serial Communications:
 - Enhanced USART (EUSART)
 - SPI, I²C™, RS-232, RS-485, LIN compatible
 - Auto-Baud Detect, Auto-Wake-up on start
- Up to 18 I/O Pins:
 - Individually programmable pull-ups
 - Slew rate control
 - Interrupt-on-change with edge-select
- Peripheral Pin Select (PPS):
 - Enables pin mapping of digital I/O

PIC12/16(L)F161X

Intelligent Analog Peripherals:

- 10-Bit Analog-to-Digital Converter (ADC):
 - Up to 12 external channels
 - Conversion available during Sleep
- Two Comparators (CMP):
 - Low-Power/High-Speed mode
 - Up to three external inverting inputs
 - Fixed Voltage Reference at non-inverting input(s)
 - Comparator outputs externally accessible
- 8-Bit Digital-to-Analog Converter (DAC):
 - 8-bit resolution, rail-to-rail
 - Positive Reference Selection
- Voltage Reference:
 - Fixed Voltage Reference (FVR): 1.024V, 2.048V and 4.096V output levels
- Zero-Cross Detect (ZCD):
 - Detect when AC signal on pin crosses ground

Clocking Structure:

- 16 MHz Internal Oscillator:
 - $\pm 1\%$ at calibration
 - Selectable frequency range from 32 MHz to 31 kHz
- 31 kHz Low-Power Internal Oscillator
- 4x Phase-Locked Loop (PLL):
 - For up to 32 MHz internal operation
- External Oscillator Block with:
 - Three external clock modes up to 32 MHz

TABLE 1: PIC12/16(L)F161X FAMILY TYPES

Device	Data Sheet Index	Program Memory Flash (W)	Data SRAM (bytes)	I/O Pins	8-bit/16-bit Timers	Comparators	10-bit ADC (ch)	Zero-Cross Detect	CCP/10-bit PWM	CWG	CLC	SMT/HLT	Angular Timer	Window Watchdog Timer	CRC with Memory Scan	Math Accelerator	PPS	EUSART	I ² C™/SPI	Debug ⁽¹⁾
PIC12(L)F1612	(A)	2048	256	6	1/1	1	4	1	2/0	1	0	2/3	0	Y	Y	0	0	0	0	I/H
PIC16(L)F1613	(A)	2048	256	12	1/1	2	8	1	2/0	1	0	2/3	0	Y	Y	0	0	0	0	I/H
PIC16(L)F1614	(B)	4096	512	12	1/3	2	8	1	2/2	1	2	2/3	1	Y	Y	1	Y	1	1	I/H
PIC16(L)F1615	(C)	8192	1024	12	1/3	2	8	1	2/2	1	4	2/3	1	Y	Y	1	Y	1	1	I/H
PIC16(L)F1618	(B)	4096	512	18	1/3	2	12	1	2/2	1	2	2/3	1	Y	Y	1	Y	1	1	I/H
PIC16(L)F1619	(C)	8192	1024	18	1/3	2	12	1	2/2	1	4	2/3	1	Y	Y	1	Y	1	1	I/H

Note 1: Debugging Methods: (I) – Integrated on Chip; (H) – via ICD Header; E – using Emulation Product.

Data Sheet Index:

- A. DS40001737 [PIC12\(L\)F1612/16\(L\)F1613 Data Sheet, 8/14-Pin, 8-bit Flash Microcontrollers](#)
- B. Future Release [PIC16\(L\)F1614/8 Data Sheet, 14/20-Pin, 8-bit Flash Microcontrollers](#)
- C. Future Release [PIC16\(L\)F1615/9 Data Sheet, 14/20-Pin, 8-bit Flash Microcontrollers](#)

Note: For other small form-factor package availability and marking information, please visit <http://www.microchip.com/packaging> or contact your local sales office.

PIC12/16(L)F161X

TABLE 2: PACKAGES

Packages	PDIP	SOIC	DFN	UDFN	TSSOP	QFN	UQFN	SSOP
PIC12(L)F1612	X	X	X	X				
PIC16(L)F1613	X	X			X	X	X	
PIC16(L)F1614	X	X			X	X		
PIC16(L)F1615	X	X			X	X		
PIC16(L)F1618	X	X				X		X
PIC16(L)F1619	X	X				X		X

Note: Pin details are subject to change.

PIN DIAGRAMS

FIGURE 1: 8-PIN PDIP, SOIC, DFN, UDFN

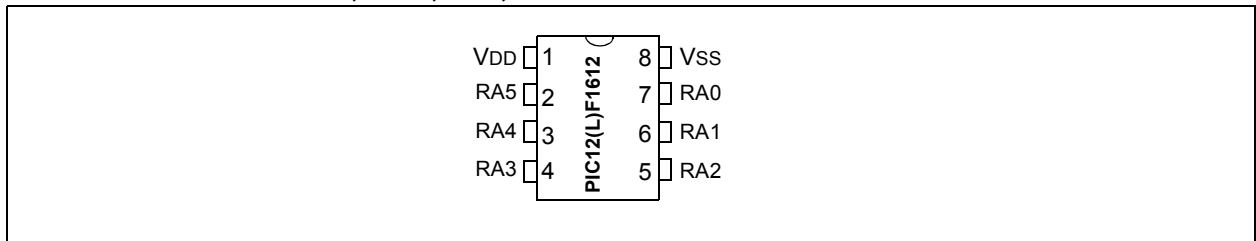


FIGURE 2: 14-PIN PDIP, SOIC, TSSOP

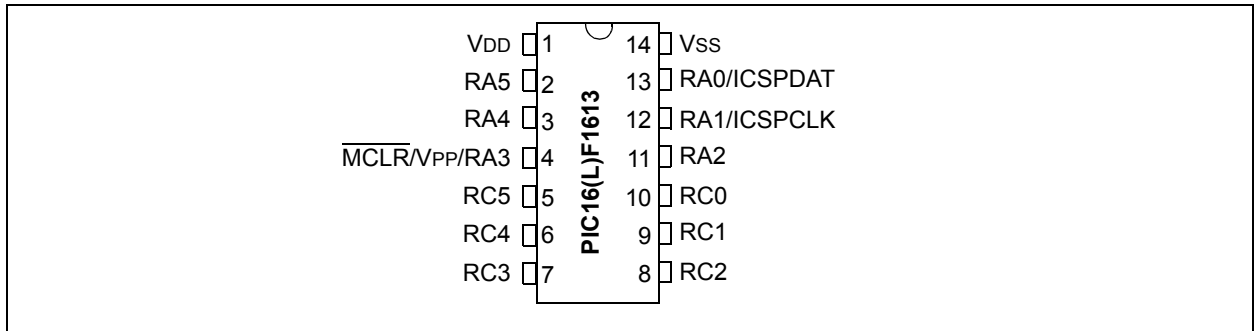
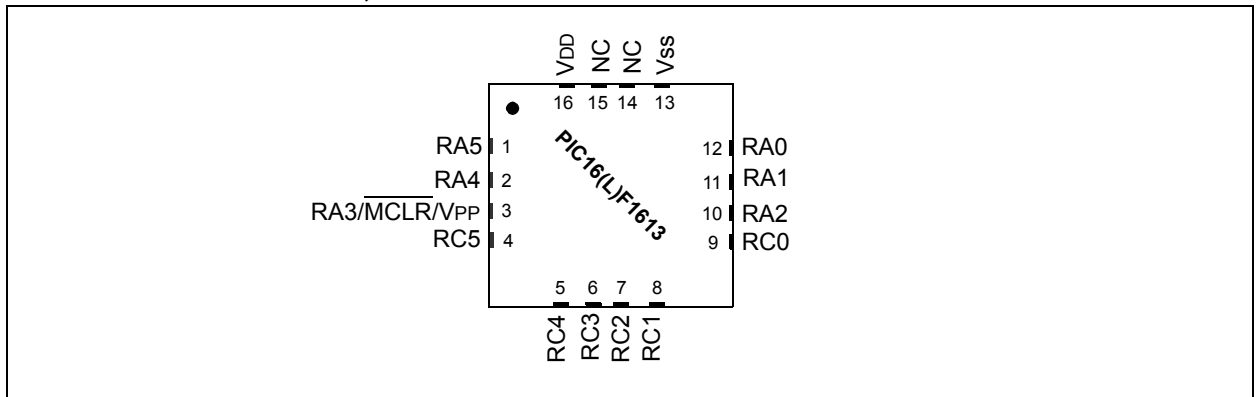


FIGURE 3: 16-PIN QFN, UQFN



PIC12/16(L)F161X

FIGURE 4: 14-PIN PDIP, SOIC, TSSOP

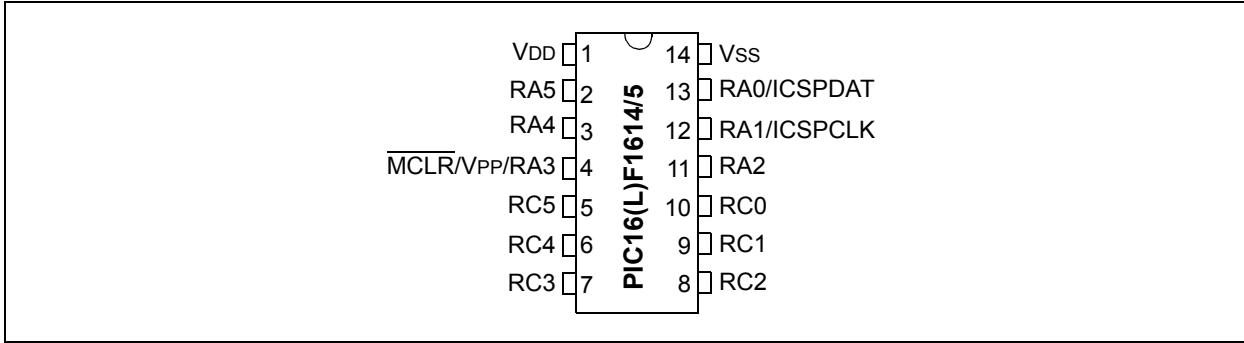


FIGURE 5: 16-PIN QFN

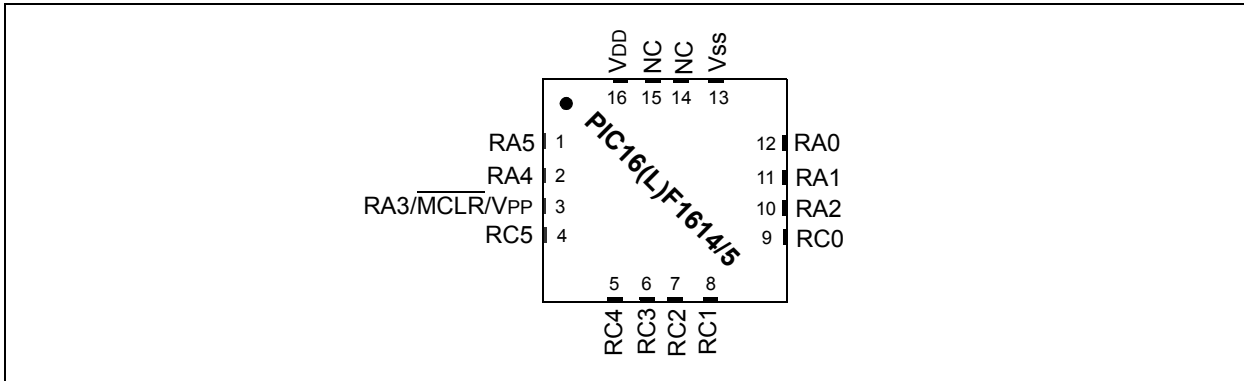


FIGURE 6: 20-PIN PDIP, SOIC, SSOP

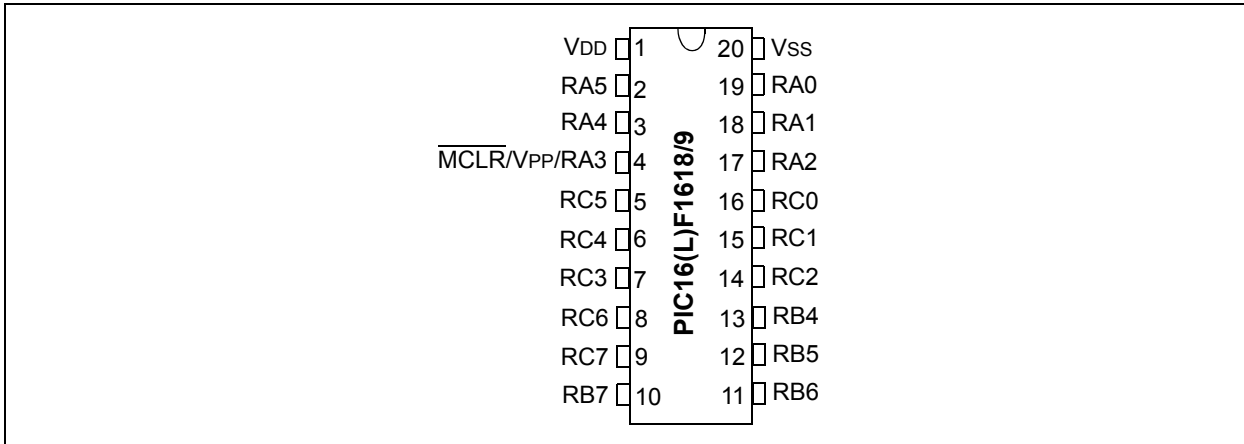
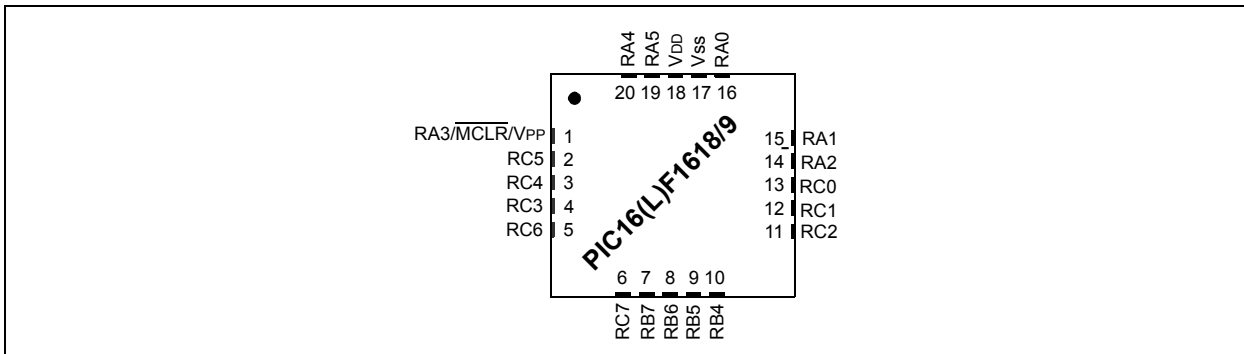


FIGURE 7: 20-PIN QFN



PIN ALLOCATION TABLES

TABLE 3: 8-PIN ALLOCATION TABLE (PIC12(L)F1612)

I/O	8-Pin PDIP, SOIC, DFN, UDFN	A/D	Reference	Comparator	Timers	CCP	CWG	ZCD	Interrupt	SMT	Pull-up	Basic
RA0	7	AN0	DAC1OUT1	C1IN+	—	CCP2	CWG1B	—	IOC	—	Y	ICSPDAT
RA1	6	AN1	VREF+	C1IN0-	—	—	—	ZCD1OUT	IOC	—	Y	ICSPCLK
RA2	5	AN2	—	C1OUT	T0CKI T4IN	CCP1	CWG1A CWG1IN	ZCD1IN	INT IOC	SMTSIG2	Y	—
RA3	4	—	—	—	T1G ⁽¹⁾ T6IN	—	—	—	IOC	SMTWIN2	Y	$\overline{\text{MCLR}}/\text{VPP}$
RA4	3	AN3	—	C1IN1-	T1G	—	CWG1B ⁽¹⁾	—	IOC	SMTSIG1	Y	CLKOUT
RA5	2	—	—	—	T1CKI T2IN	CCP1 ⁽¹⁾	CWG1A ⁽¹⁾	—	IOC	SMTWIN1	Y	CLKIN
VDD	1	—	—	—	—	—	—	—	—	—	—	VDD
VSS	8	—	—	—	—	—	—	—	—	—	—	VSS

Note 1: Alternate pin function selected with the APFCON register.

TABLE 4: 14/16-PIN ALLOCATION TABLE (PIC16(L)F1613)

I/O	14-Pin PDIP, SOIC, TSSOP	16-Pin QFN, UQFN	A/D	Reference	Comparator	Timers	CCP	CWG	ZCD	Interrupt	SMT	Pull-up	Basic
RA0	13	12	AN0	DAC1OUT1	C1IN+	—	—	—	—	IOC	—	Y	ICSPDAT
RA1	12	11	AN1	VREF+	C1IN0- C2IN0-	—	—	—	ZCD1OUT	IOC	—	Y	ICSPCLK
RA2	11	10	AN2	—	C1OUT	T0CKI T4IN	—	CWG1IN	ZCD1IN	INT IOC	—	Y	—
RA3	4	3	—	—	—	T1G ⁽¹⁾ T6IN	—	—	—	IOC	SMTWIN2	Y	$\overline{\text{MCLR}}/\text{VPP}$
RA4	3	2	AN3	—	—	T1G	—	—	—	IOC	SMTSIG1	Y	CLKOUT
RA5	2	1	—	—	—	T1CKI T2IN	CCP2 ⁽¹⁾	—	—	IOC	SMTWIN1	Y	CLKIN
RC0	10	9	AN4	—	C2IN+	—	—	—	—	IOC	—	Y	—
RC1	9	8	AN5	—	C1IN1- C2IN1-	T4IN	—	—	—	IOC	SMTSIG2	Y	—
RC2	8	7	AN6	—	C1IN2- C2IN2-	—	—	CWG1D	—	IOC	—	Y	—
RC3	7	6	AN7	—	C1IN3- C2IN3-	—	CCP2	CWG1C	—	IOC	—	Y	—
RC4	6	5	—	—	C2OUT	—	—	CWG1B	—	IOC	—	Y	—
RC5	5	4	—	—	—	—	CCP1	CWG1A	—	IOC	—	Y	—
VDD	1	16	—	—	—	—	—	—	—	—	—	—	VDD
VSS	14	13	—	—	—	—	—	—	—	—	—	—	VSS

Note 1: Alternate pin function selected with the APFCON register.

TABLE 5: 14/16-PIN ALLOCATION TABLE (PIC16(L)F1614/5)

I/O	14-Pin PDIP, SOIC, TSSOP	16-Pin QFN	A/D	Reference	Comparator	Timers	CCP	CWG	ZCD	CLC	EUSART	SMT	Angular Timer	MSSP	PWM
RA0	13	12	AN0	DAC1OUT1	C1IN+	—	—	—	—	—	—	—	—	—	—
RA1	12	11	AN1	VREF+	C1IN0- C2IN0-	—	—	—	—	—	—	—	—	—	—
RA2	11	10	AN2	—	C2IN+	T0CK1(1)	—	CWG1IN(1)	ZCD1IN	—	—	—	—	—	—
RA3	4	3	—	—	—	T6IN(1)	—	—	—	—	—	SMTWIN2(1)	—	—	—
RA4	3	2	AN3	—	—	T1G(1)	—	—	—	—	—	SMTSIG1(1)	—	—	—
RA5	2	1	—	—	—	T1CK1(1) T2IN(1)	—	—	—	—	—	SMTWIN1(1)	—	—	—
RC0	10	9	AN4	—	C2IN+	T5CK1(1)	—	—	—	—	—	—	—	SCK(1,3)	—
RC1	9	8	AN5	—	C1IN1- C2IN1-	T4IN(1)	—	—	—	—	—	SMTSIG2(1)	—	SDI(1)	—
RC2	8	7	AN6	—	C1IN2- C2IN2-	—	—	—	—	—	—	—	—	—	—
RC3	7	6	AN7	—	C1IN3- C2IN3-	T5G(1)	CCP2(1)	—	—	CLCIN0(1)	—	—	ATCC(1)	SS(1)	—
RC4	6	5	—	—	—	T3G(1)	—	—	—	CLCIN1(1)	CK(1)	—	—	—	—
RC5	5	4	—	—	—	T3CK1(1)	CCP1(1)	—	—	—	RX(1,3)	—	ATIN(1)	—	—
VDD	1	16	—	—	—	—	—	—	—	—	—	—	—	—	—
VSS	14	13	—	—	—	—	—	—	—	—	—	—	—	—	—
OUT(2)	—	—	—	—	C1OUT	—	CCP1	CWG1A	ZCD1OUT	CLC1OUT	DT(3)	—	—	SDO	PWM3OUT
	—	—	—	—	C2OUT	—	CCP1	CWG1B	—	CLC2OUT	CK	—	—	SCK(3)	PWM4OUT
	—	—	—	—	—	—	—	CWG1C	—	—	TX	—	—	—	—

Note 1: Default peripheral input. Input can be moved to any other pin with the PPS input selection registers.

2: All pin outputs default to PORT latch data. Any pin can be selected as a digital peripheral output with the PPS output selection registers.

3: These peripheral functions are bidirectional. The output pin selections must be the same as the input pin selections.

TABLE 6: 20-PIN ALLOCATION TABLE (PIC16(L)F1618/9)

I/O	20-Pin PDIP, SOIC, SSOP	20-Pin QFN	A/D	Reference	Comparator	Timers	CCP	CWG	ZCD	CLC	EUSART	SMT	Angular Timer	MSSP	PWM
RA0	19	16	AN0	DAC1OUT	C1IN+	—	—	—	—	—	—	—	—	—	—
RA1	18	15	AN1	VREF+	C1IN0- C2IN0-	—	—	—	—	—	—	—	—	—	—
RA2	17	14	AN2	—	—	T0CKI(1)	—	CWG1IN(1)	—	—	—	—	—	—	—
RA3	4	1	—	—	—	T6IN(1)	—	—	—	—	—	SMTWIN2(1)	—	—	—
RA4	3	20	AN3	—	—	T1G(1)	—	—	—	—	—	SMTSIG(1)	—	—	—
RA5	2	19	—	—	—	T1CKI(1) T2IN(1)	—	—	—	CLCIN3(1)	—	SMTWIN1(1)	—	—	—
RB4	13	10	AN10	—	—	—	—	—	—	—	—	—	—	SD(1)	—
RB5	12	9	AN11	—	—	—	—	—	—	—	RX(1,3)	—	—	—	—
RB6	11	8	—	—	—	—	—	—	—	—	—	—	—	—	—
RB7	10	7	—	—	—	—	—	—	—	—	—	—	—	—	—
RC0	16	13	AN4	—	C2IN+	T5CKI(1)	—	—	—	—	—	—	—	—	—
RC1	15	12	AN5	—	C1IN1- C2IN1-	T4IN(1)	—	—	—	CLCIN(2)	—	SMTSIG2(1)	—	—	—
RC2	14	11	AN6	—	C1IN2- C2IN2-	—	—	—	—	—	—	—	—	—	—
RC3	7	4	AN7	—	C1IN3- C2IN3-	T5G(1)	CCP2(1)	—	—	CLCIN0(1)	—	—	ATCC(1)	—	—
RC4	6	3	—	—	—	T3G(1)	—	—	—	CLCIN1(1)	—	—	—	—	—
RC5	5	2	—	—	—	T3CKI(1)	CCP2(1)	—	—	—	—	—	ATIN(1)	—	—
RC6	8	5	AN8	—	—	—	—	—	—	—	—	—	—	SS(1)	—
RC7	9	6	AN9	—	—	—	—	—	—	—	—	—	—	—	—
VDD	1	18	—	—	—	—	—	—	—	—	—	—	—	—	—
VSS	20	17	—	—	—	—	—	—	—	—	—	—	—	—	—

Note 1: Default peripheral input. Input can be moved to any other pin with the PPS input selection registers.

2: All pin outputs default to PORT latch data. Any pin can be selected as a digital peripheral output with the PPS output selection registers.

3: These peripheral functions are bidirectional. The output pin selections must be the same as the input pin selections.

TABLE 6: 20-PIN ALLOCATION TABLE (PIC16(L)F1618/9)

I/O	20-Pin PDIP, SOIC, SSOP	20-Pin QFN	A/D	Reference	Comparator	Timers	CCP	CWG	ZCD	CLC	EUSART	SMT	Angular Timer	MSSP	PWM
OUT ⁽²⁾	—	—	—	—	C1OUT	—	CCP1	CWG1A	ZCD1OUT	CLC1OUT	DT ⁽³⁾	—	—	SDO	PWM3OUT
	—	—	—	—	C2OUT	—	CCP2	CWG1B	—	CLC2OUT	CK	—	—	SCK ⁽³⁾	PWM4OUT
—	—	—	—	—	—	—	—	CWG1C	—	CLC3OUT	TX	—	—	—	—
—	—	—	—	—	—	—	—	CWG1D	—	CLC4OUT	—	—	—	—	—

- Note**
- 1: Default peripheral input. Input can be moved to any other pin with the PPS input selection registers.
 - 2: All pin outputs default to PORT latch data. Any pin can be selected as a digital peripheral output with the PPS output selection registers.
 - 3: These peripheral functions are bidirectional. The output pin selections must be the same as the input pin selections.

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