THE DATASHEET OF

PCF2123BS/1,518

PCF2123

SPI Real time clock/calendar

Rev. 6 — 15 July 2013 Product data sheet

1. General description

The PCF2123 is a CMOS[1] Real-Time Clock (RTC) and calendar optimized for low power applications. Data is transferred serially via a Serial Peripheral Interface (SPI-bus) with a maximum data rate of 6.25 Mbit/s. An alarm and timer function is also available providing the possibility to generate a wake-up signal on an interrupt pin. An offset register allows fine tuning of the clock.

2. Features and benefits

- Real time clock provides year, month, day, weekday, hours, minutes, and seconds based on a 32.768 kHz quartz crystal
- Low backup current while running: typical 100 nA at V_{DD} = 2.0 V and T_{amb} = 25 °C
- Resolution: seconds to years
- Watchdog functionality
- Freely programmable timer and alarm with interrupt capability
- Clock operating voltage: 1.1 V to 5.5 V
- 3 line SPI-bus with separate, but combinable data input and output
- Serial interface at V_{DD} = 1.8 V to 5.5 V
- 1 second or 1 minute interrupt output
- Integrated oscillator load capacitors for C_L = 7 pF
- Internal Power-On Reset (POR)
- Open-drain interrupt and clock output pins
- Programmable offset register for frequency adjustment

3. Applications

- Time keeping application
- Battery powered devices
- Metering
- High duration timers
- Daily alarms
- Low standby power applications

1. The definition of the abbreviations and acronyms used in this data sheet can be found in Section 22.

4. Ordering information

Table 1. Ordering information

Type number	Package		
	Name	Description	Version
PCF2123BS	HVQFN16	plastic thermal enhanced very thin quad flat package; no leads; 16 terminals; body 3 × 3 × 0.85 mm	SOT758-1
PCF2123TS	TSSOP14	plastic thin shrink small outline package; 14 leads; body width 4.4 mm	SOT402-1
PCF2123U/10AA	wire bond die	12 bonding pads	PCF2123U/10
PCF2123U/12AA	WLCSP12	wafer level chip size package; 12 bumps	PCF2123U/12
PCF2123U/12HA	WLCSP12	wafer level chip size package; 12 bumps	PCF2123U/12
PCF2123U/5GA	wire bond die	12 bonding pads	PCF2123U/10

4.1 Ordering options

Table 2. Ordering options

Product type number	Sales item (12NC)	Orderable part number	IC revision	Delivery form
PCF2123BS/1	935286382512	PCF2123BS/1,512	1	tube, dry pack
	935286382518	PCF2123BS/1,518	1	tape and reel, 13 inch, dry pack
PCF2123TS/1	935286384112	PCF2123TS/1,112	1	tube
	935286384118	PCF2123TS/1,118	1	tape and reel, 13 inch
PCF2123U/10AA/1	935287542005	PCF2123U/10AA/1,00	1	sawn 6 inch wafer on Film Frame Carrier (FFC) for 6 inch wafer
PCF2123U/12AA/1	935290647005	PCF2123U/12AA/1,00	1	sawn 6 inch wafer on plastic Film Frame Carrier (FFC) for 8 inch wafer
PCF2123U/12HA/1	935292966005	PCF2123U/12HA/1,00	1	sawn 6 inch wafer on plastic Film Frame Carrier (FFC) for 8 inch wafer
PCF2123U/5GA/1	935295429015	PCF2123U/5GA/1,015	1	wafer, unsawn

5. Marking

Table 3. Marking codes

Type number	Marking code
PCF2123BS	123
PCF2123TS	PCF2123
PCF2123U/10AA	PC2123-1
PCF2123U/12AA	PC2123-1
PCF2123U/12HA	PC2123-1
PCF2123U/5GA	PC2123-1

6. Block diagram

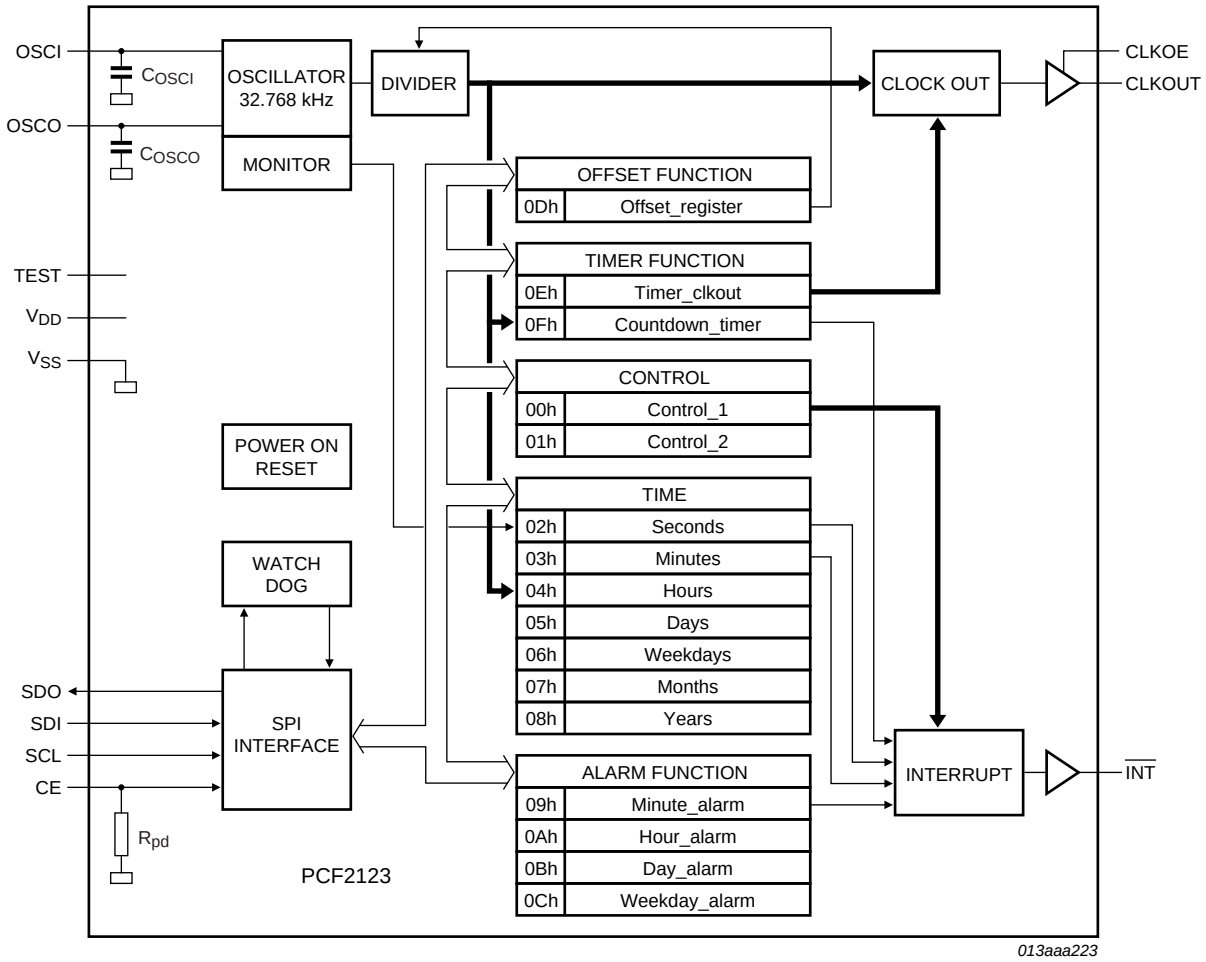
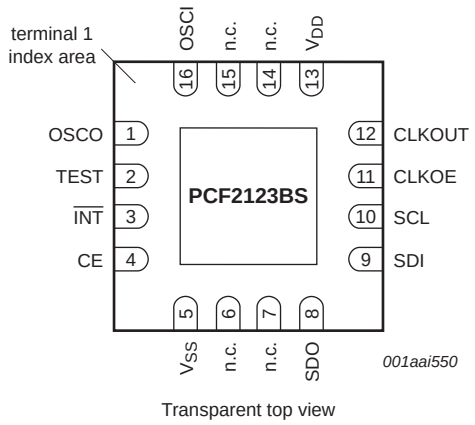


Fig 1. Block diagram of PCF2123

7. Pinning information

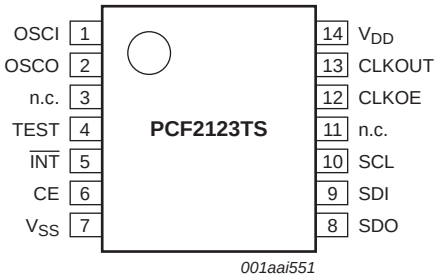
7.1 Pinning



Transparent top view

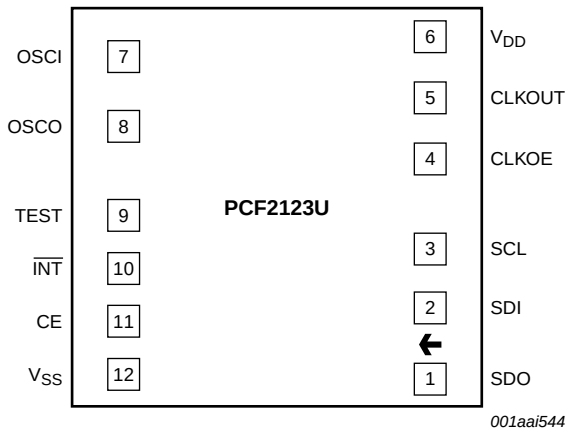
For mechanical details, see Figure 31 on page 45.

Fig 2. Pin configuration for HVQFN16 (PCF2123BS/1)



Top view. For mechanical details, see Figure 32 on page 46.

Fig 3. Pin configuration for TSSOP14 (PCF2123TS/1)



Viewed from active side. For mechanical details, see Figure 33 on page 47 and Figure 34 on page 48.

Fig 4. Pin configuration for PCF2123Ux (bare die)

7.2 Pin description

Table 4. Pin description

Symbol	Pin			Description
	HVQFN16 (PCF2123BS/1)	TSSOP14 (PCF2123TS/1)	PCF2123Ux (bare die)	
OSCI	16	1	7	oscillator input; high-impedance node; minimize wire length between quartz and package
OSCO	1	2	8	oscillator output; high-impedance node; minimize wire length between quartz and package
n.c.	6, 7, 14, 15	3, 11	-	do not connect and do not use as feed through; connect to V_{DD} if floating pins are not allowed
TEST	2	4	9	test pin; not user accessible; connect to V_{SS} or leave floating (internally pulled down)
$\overline{INT}$	3	5	10	interrupt output (open-drain; active LOW)
CE	4	6	11	chip enable input (active HIGH) with internal pull down
V_{SS}	5[1]	7	12[2]	ground
SDO	8	8	1	serial data output, push-pull; high-impedance when not driving; can be connected to SDI for single wire data line
SDI	9	9	2	serial data input; may float when CE is inactive
SCL	10	10	3	serial clock input; may float when CE is inactive
CLKOE	11	12	4	CLKOUT enable or disable pin; enable is active HIGH
CLKOUT	12	13	5	clock output (open-drain)
V_{DD}	13	14	6	supply voltage; positive or negative steps in V_{DD} may affect oscillator performance; recommend 100 nF decoupling close to the device (see Figure 30)

[1] The die paddle (exposed pad) is wired to V_{SS} and should be electrically isolated.

[2] The substrate (rear side of the die) is wired to V_{SS} and should be electrically isolated.

8. Functional description

The PCF2123 contains 16 8-bit registers with an auto-incrementing address counter, an on-chip 32.768 kHz oscillator with two integrated load capacitors, a frequency divider which provides the source clock for the Real Time Clock (RTC), a programmable clock output, and a 6.25 Mbit/s SPI-bus. An offset register allows fine tuning of the clock.

All 16 registers are designed as addressable 8-bit parallel registers although not all bits are implemented.

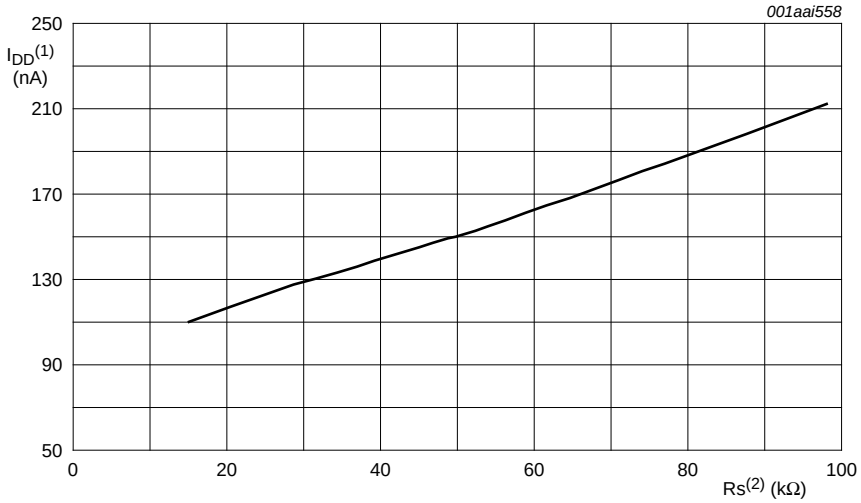
- The first two registers (memory address 00h and 01h) are used as control registers.
- The memory addresses 02h through 08h are used as counters for the clock function (seconds up to years). The registers Seconds, Minutes, Hours, Days, Weekdays, Months, and Years are all coded in Binary Coded Decimal (BCD) format. When one of the RTC registers is written or read the contents of all counters are frozen. Therefore, faulty writing or reading of the clock and calendar during a carry condition is prevented.
- Addresses 09h through 0Ch define the alarm condition.
- Address 0Dh defines the offset calibration.
- Address 0Eh defines the clock out and timer mode.
- Address registers 0Eh and 0Fh are used for the countdown timer function. The countdown timer has four selectable source clocks allowing for countdown periods in the range from 244 μs up to four hours. There are also two pre-defined timers which can be used to generate an interrupt once per second or once per minute. These are defined in register Control_2 (01h).

8.1 Low power operation

Minimum power operation will be achieved by reducing the number and frequency of switching signals inside the IC, i.e., low frequency timer clocks and a low frequency CLKOUT will result in lower operating power. A second prime consideration is the series resistance R_S of the quartz used.

8.1.1 Power consumption with respect to quartz series resistance

The series resistance acts as a loss element. Low R_S will reduce current consumption further.



Configuration: CLKOUT disabled, V_{DD} = 3 V, timer clock set to $\frac{1}{60}$ Hz.

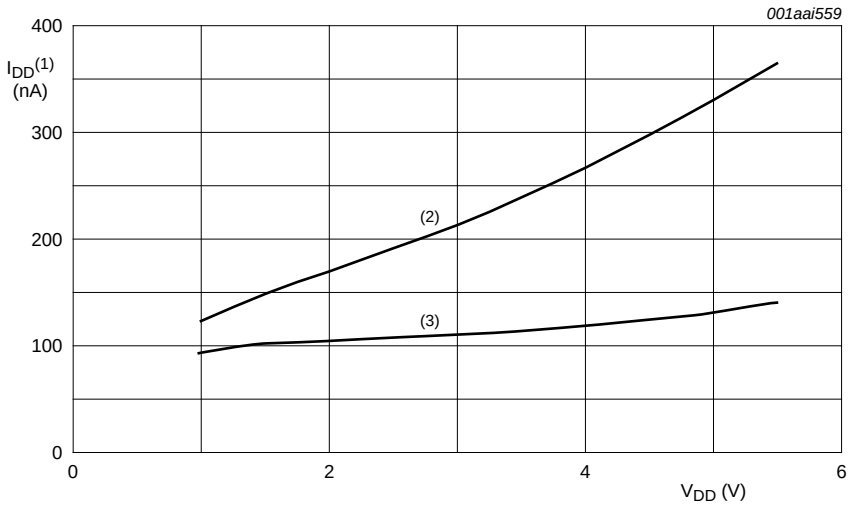
(1) I_{DD} (nA) minimum power mode.

(2) Maximum value for R_S is 100 kΩ.

Fig 5. I_{DD} with respect to quartz R_S

8.1.2 Power consumptions with respect to timer mode

Four source clocks are possible for the timer. The 4.096 kHz source clock will add the greatest part to the power consumption. The selection of 64 Hz, 1 Hz, or $\frac{1}{60}$ Hz will be almost indistinguishable and add very little.



Configuration: CLKOUT disabled, quartz R_S = 15 kΩ.

(1) I_{DD} (nA) minimum power mode.

(2) Timer clock = 4 kHz.

(3) Timer clock = 64 Hz, 1 Hz, $\frac{1}{60}$ Hz.

Fig 6. I_{DD} with respect to timer clock selection

8.2 Register overview

16 registers are available. The time registers are encoded in the Binary Coded Decimal (BCD) format to simplify application use. Other registers are either bit-wise or standard binary.

Table 5. Registers overview

Bit positions labelled as - are not implemented and will return a 0 when read. The bit position labelled as -- is not implemented and will return a 0 or 1 when read. Bit positions labelled with N should always be written with logic 0[1].

Address	Register name	Bit							
		7	6	5	4	3	2	1	0
Control and status registers									
00h	Control_1	EXT_TEST	N	STOP	SR	N	12_24	CIE	N
01h	Control_2	MI	SI	MSF	TI_TP	AF	TF	AIE	TIE
Time and date registers									
02h	Seconds	OS	SECONDS (0 to 59)						
03h	Minutes	--	MINUTES (0 to 59)						
04h	Hours	-	-	AMPM	HOURS (1 to 12) in 12 h mode				
				HOURS (0 to 23) in 24 h mode					
05h	Days	-	-	DAYS (1 to 31)					
06h	Weekdays	-	-	-	-	-	WEEKDAYS (0 to 6)		
07h	Months	-	-	-	MONTHS (1 to 12)				
08h	Years	YEARS (0 to 99)							
Alarm registers									
09h	Minute_alarm	AE_M	MINUTE_ALARM (0 to 59)						
0Ah	Hour_alarm	AE_H	-	AMPM	HOUR_ALARM (1 to 12) in 12 h mode				
				HOUR_ALARM (0 to 23) in 24 h mode					
0Bh	Day_alarm	AE_D	-	DAY_ALARM (1 to 31)					
0Ch	Weekday_alarm	AE_W	-	-	-	-	WEEKDAY_ALARM (0 to 6)		
Offset register									
0Dh	Offset_register	MODE	OFFSET[6:0]						
Timer registers									
0Eh	Timer_clkout	-	COF[2:0]			TE	-	CTD[1:0]	
0Fh	Countdown_timer	COUNTDOWN_TIMER[7:0]							

[1] Except in the case of software reset, see Section 8.3.1.1.

8.3 Control registers

8.3.1 Register Control_1

Table 6. Control_1 - control and status register 1 (address 00h) bit description

Bit	Symbol	Value	Description	Reference
7	EXT_TEST	0[1]	normal mode	Section 8.10
		1	external clock test mode	
6	N	-	unused	-
5	STOP	0[1]	the RTC source clock runs	Section 8.11
		1	the RTC clock is stopped; RTC divider chain flip-flops are asynchronously set to logic 0; CLKOUT at 32.768 kHz, 16.384 kHz or 8.192 kHz is still available	
4	SR	0[1]	no software reset	Section 8.3.1.1
		1	initiate software reset[2]; this register will always return a 0 when read	
3	N	-	unused	-
2	12_24	0[1]	24 hour mode is selected	-
		1	12 hour mode is selected	
1	CIE	0[1]	no correction interrupt generated	Section 8.9
		1	interrupt pulses will be generated at every correction cycle	
0	N	-	unused	-

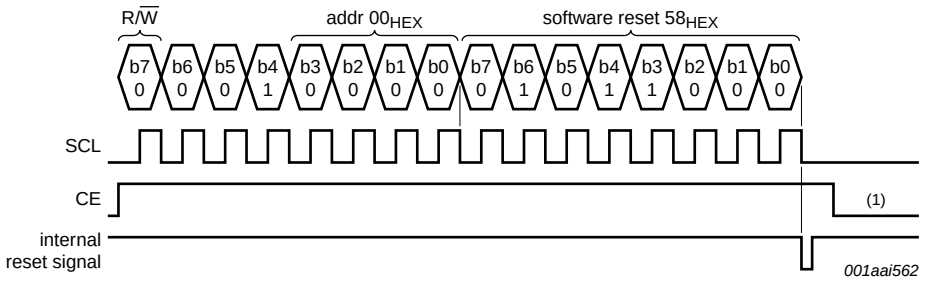
[1] Default value.

[2] For a software reset, 01011000 (58h) must be sent to register Control_1 (see Section 8.3.1.1).

8.3.1.1 Reset

A reset is automatically generated at power-on. A reset can also be initiated with the software reset command. It is generally recommended to make a software reset after power-on.

A software reset can be initiated by setting the bits 6, 4 and 3 in register Control_1 logic 1 and all other bits logic 0 by sending the bit sequence 01011000 (58h), see Figure 7. If this bit sequence is not correct, the software reset instruction will be ignored to protect the device from accidently being reset. When sending the software instruction, the other bits are not written.



(1) When CE is inactive, the interface is reset.

Fig 7. Software reset command

After reset, the following mode is entered:

- 32.768 kHz on pin CLKOUT active
- 24 hour mode is selected
- Offset register is set to 0
- No alarms set
- Timer disabled
- No interrupts enabled

Table 7. Register reset values

Bits labeled as - are not implemented. Bits labeled as X are undefined at power-on and unchanged by subsequent resets.

Address	Register name	Bit							
		7	6	5	4	3	2	1	0
00h	Control_1	0	0	0	0	0	0	0	0
01h	Control_2	0	0	0	0	0	0	0	0
02h	Seconds	1	X	X	X	X	X	X	X
03h	Minutes	-	X	X	X	X	X	X	X
04h	Hours	-	-	X	X	X	X	X	X
05h	Days	-	-	X	X	X	X	X	X
06h	Weekdays	-	-	-	-	-	X	X	X
07h	Months	-	-	-	X	X	X	X	X
08h	Years	X	X	X	X	X	X	X	X
09h	Minute_alarm	1	X	X	X	X	X	X	X
0Ah	Hour_alarm	1	-	X	X	X	X	X	X
0Bh	Day_alarm	1	-	X	X	X	X	X	X
0Ch	Weekday_alarm	1	-	-	-	-	X	X	X
0Dh	Offset_register	0	0	0	0	0	0	0	0
0Eh	Timer_clkout	-	0	0	0	0	-	1	1
0Fh	Countdown_timer	X	X	X	X	X	X	X	X

8.3.2 Register Control_2

Table 8. Control_2 - control and status register 2 (address 01h) bits description

Bit	Symbol	Value	Description	Reference
7	MI	0[1]	minute interrupt is disabled	Section 8.6.3
		1	minute interrupt is enabled	
6	SI	0[1]	second interrupt is disabled	
		1	second interrupt is enabled	
5	MSF	0[1]	no minute or second interrupt generated	
		1	flag set when minute or second interrupt generated; flag must be cleared to clear interrupt when TI_IP = 0	
4	TI_TP	0[1]	interrupt pin follows timer flags	Section 8.7.2
		1	interrupt pin generates a pulse	
3	AF	0[1]	no alarm interrupt generated	Section 8.5.5
		1	flag set when alarm triggered; flag must be cleared to clear interrupt	
2	TF	0[1]	no countdown timer interrupt generated	Section 8.6.4
		1	flag set when countdown timer interrupt generated; flag must be cleared to clear interrupt when TI_IP = 0	
1	AIE	0[1]	no interrupt generated from the alarm flag	Section 8.7.3
		1	interrupt generated when alarm flag set	
0	TIE	0[1]	no interrupt generated from the countdown timer	Section 8.7.2
		1	interrupt generated by the countdown timer	

[1] Default value.

8.4 Time and date function

The majority of the registers are coded in the Binary Coded Decimal (BCD) format. BCD is used to simplify application use. An example is shown for the seconds in Table 10.

8.4.1 Register Seconds

Table 9. Seconds - seconds register (address 02h) bit description

Bit	Symbol	Value	Place value	Description
7	OS	0	-	clock integrity is guaranteed
		1[1]	-	clock integrity is not guaranteed; oscillator has stopped or has been interrupted
6 to 4	SECONDS	0 to 5	ten's place	actual seconds coded in BCD format, see Table 10
3 to 0		0 to 9	unit place	

[1] Default value.

Table 10. Seconds coded in BCD format

Seconds value (decimal)	Upper-digit (ten's place)				Digit (unit place)			
	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
00	0	0	0	0	0	0	0	0
01	0	0	0	0	0	0	0	1
02	0	0	0	0	0	0	1	0
:	:	:	:	:	:	:	:	:
09	0	0	0	0	1	0	0	1
10	0	0	0	1	0	0	0	0
:	:	:	:	:	:	:	:	:
58	0	1	0	1	1	0	0	0
59	0	1	0	1	1	0	0	1

8.4.1.1 OS flag

The PCF2123 includes a flag (OS in register Seconds, see Table 9) which is set whenever the oscillator is stopped (see Figure 8 and Figure 9). The flag will remain set until cleared by software. If the flag cannot be cleared, then the PCF2123 oscillator is not running. This method can be used to monitor the oscillator and to determine if the supply voltage has reduced to the point where oscillation fails.

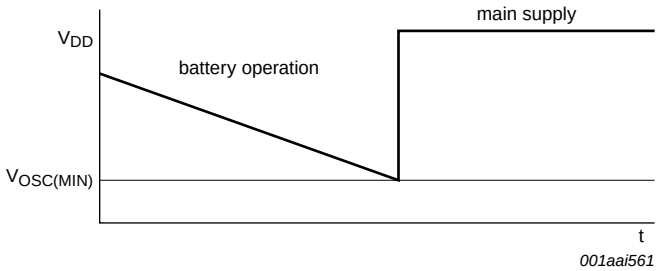


Fig 8. OS set by failing V_{DD}

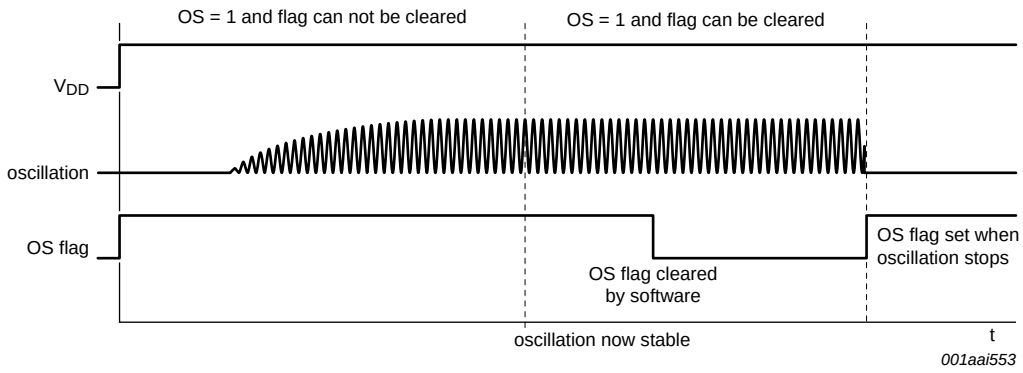


Fig 9. OS flag

The oscillator may be stopped, for example, by grounding one of the oscillator pins, OSCI or OSCO. The oscillator is also considered to be stopped during the time between power-on and stable crystal resonance. This time may be in the range of 200 ms to 2 s depending on crystal type, temperature and supply voltage. At power-on the OS flag is always set.

8.4.2 Register Minutes

Table 11. Minutes - minutes register (address 03h) bit description

Bit	Symbol	Value	Place value	Description
7	-	-	-	unused
6 to 4	MINUTES	0 to 5	ten's place	actual minutes coded in BCD format
3 to 0		0 to 9	unit place	

8.4.3 Register Hours

Table 12. Hours - hours register (address 04h) bit description

Bit	Symbol	Value	Place value	Description
7 to 6	-	-	-	unused
12 hour mode[1]				
5	AMPM	0	-	indicates AM
		1	-	indicates PM
4	HOURS	0 to 1	ten's place	actual hours in 12 hour mode coded in BCD format
3 to 0		0 to 9	unit place	
24 hour mode[1]				
5 to 4	HOURS	0 to 2	ten's place	actual hours in 24 hour mode coded in BCD format
3 to 0		0 to 9	unit place	

[1] Hour mode is set by the 12_24 bit in register Control_1.

8.4.4 Register Days

Table 13. Days - days register (address 05h) bit description

Bit	Symbol	Value	Place value	Description
7 to 6	-	-	-	unused
5 to 4	DAYS[1]	0 to 3	ten's place	actual day coded in BCD format
3 to 0		0 to 9	unit place	

[1] The PCF2123 compensates for leap years by adding a 29th day to February if the year counter contains a value which is exactly divisible by 4, including the year 00.

8.4.5 Register Weekdays

Table 14. Weekdays - weekdays register (address 06h) bit description

Bit	Symbol	Value	Description
7 to 3	-	-	unused
2 to 0	WEEKDAYS	0 to 6	actual weekday values, see Table 15

Table 15. Weekday assignments

Day[1]	Bit		
	2	1	0
Sunday	0	0	0
Monday	0	0	1
Tuesday	0	1	0
Wednesday	0	1	1
Thursday	1	0	0
Friday	1	0	1
Saturday	1	1	0

[1] Definition may be re-assigned by the user.

8.4.6 Register Months

Table 16. Months - months register (address 07h) bit description

Bit	Symbol	Value	Place value	Description
7 to 5	-	-	-	unused
4	MONTHS	0 to 1	ten's place	actual month coded in BCD format, see Table 17
3 to 0		0 to 9	unit place	

Table 17. Month assignments in BCD format

Month	Upper-digit (ten's place)	Digit (unit place)			
	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
January	0	0	0	0	1
February	0	0	0	1	0
March	0	0	0	1	1
April	0	0	1	0	0
May	0	0	1	0	1
June	0	0	1	1	0
July	0	0	1	1	1
August	0	1	0	0	0
September	0	1	0	0	1
October	1	0	0	0	0
November	1	0	0	0	1
December	1	0	0	1	0

8.4.7 Register Years

Table 18. Years - years register (08h) bit description

Bit	Symbol	Value	Place value	Description
7 to 4	YEARS	0 to 9	ten's place	actual year coded in BCD format
3 to 0		0 to 9	unit place	

8.4.8 Setting and reading the time

Figure 10 shows the data flow and data dependencies starting from the 1 Hz clock tick.

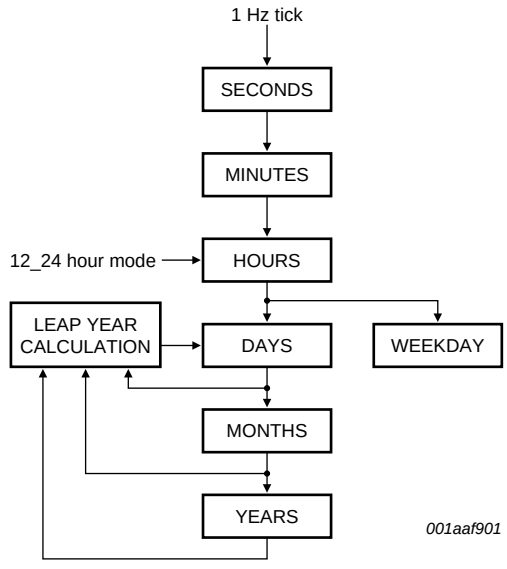


Fig 10. Data flow of the time function

During read/write operations, the time counting circuits (memory locations 02h through 08h) are blocked.

This prevents

- Faulty reading of the clock and calendar during a carry condition
- Incrementing the time registers during the read cycle

After this read/write access is completed, the time circuit is released again and any pending request to increment the time counters that occurred during the read/write access is serviced. A maximum of 1 request can be stored; therefore, all accesses must be completed within 1 second (see Figure 11).

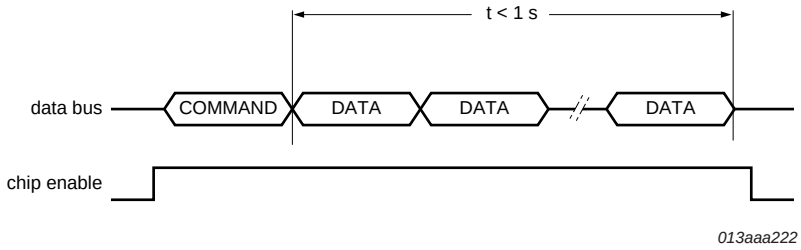


Fig 11. Access time for read/write operations

As a consequence of this method, it is very important to make a read or write access in one go, that is, setting or reading seconds through to years should be made in one single access. Failing to comply with this method could result in the time becoming corrupted.

As an example, if the time (seconds through to hours) is set in one access and then in a second access the date is set, it is possible that the time may increment between the two accesses. A similar problem exists when reading. A roll over may occur between reads thus giving the minutes from one moment and the hours from the next. Therefore it is advised to read all time and date registers in one access.

8.5 Alarm function

When one or more of these registers are loaded with a valid minute, hour, day, or weekday and its corresponding alarm enable bit (AE_x) is logic 0, then that information will be compared with the current minute, hour, day, and weekday.

8.5.1 Register Minute_alarm

Table 19. Minute_alarm - minute alarm register (address 09h) bit description

Bit	Symbol	Value	Place value	Description
7	AE_M	0	-	minute alarm is enabled
		1[1]	-	minute alarm is disabled
6 to 4	MINUTE_ALARM	0 to 5	ten's place	minute alarm information coded in BCD format
3 to 0		0 to 9	unit place	

[1] Default value.

8.5.2 Register Hour_alarm

Table 20. Hour_alarm - hour alarm register (address 0Ah) bit description

Bit	Symbol	Value	Place value	Description
7	AE_H	0	-	hour alarm is enabled
		1[1]	-	hour alarm is disabled
6	-	-	-	unused
12 hour mode[2]				
5	AMPM	0	-	indicates AM
		1	-	indicates PM
4	HOUR_ALARM	0 to 1	ten's place	hour alarm information coded in BCD format when in 12 hour mode
3 to 0		0 to 9	unit place	
24 hour mode[2]				
5 to 4	HOUR_ALARM	0 to 2	ten's place	hour alarm information coded in BCD format when in 24 hour mode
3 to 0		0 to 9	unit place	

[1] Default value.

[2] Hour mode is set by the 12_24 bit in register Control_1.

8.5.3 Register Day_alarm

Table 21. Day_alarm - day alarm register (address 0Bh) bit description

Bit	Symbol	Value	Place value	Description
7	AE_D	0	-	day alarm is enabled
		1[1]	-	day alarm is disabled
6	-	-	-	unused
5 to 4	DAY_ALARM	0 to 3	ten's place	day alarm information coded in BCD format
3 to 0		0 to 9	unit place	

[1] Default value.

8.5.4 Register Weekday_alarm

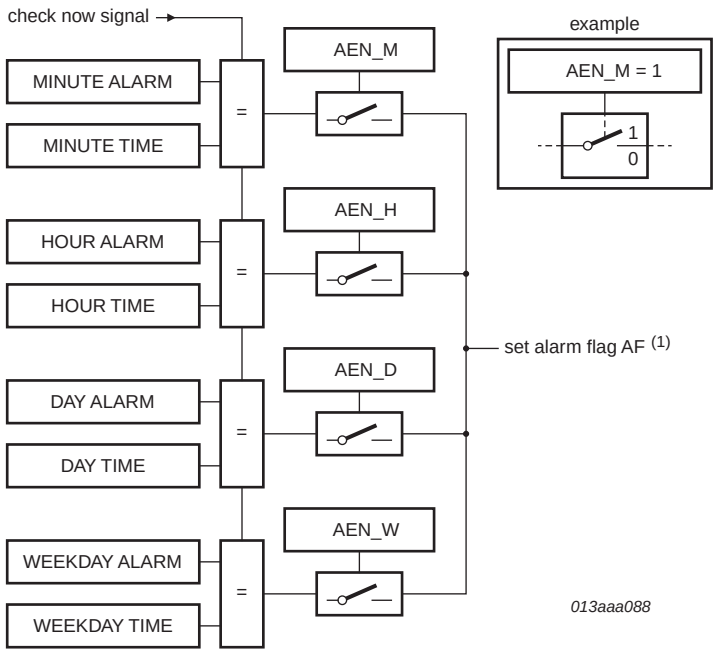
Table 22. Weekday_alarm - weekday alarm register (address 0Ch) bit description

Bit	Symbol	Value	Description
7	AE_W	0	weekday alarm is enabled
		1[1]	weekday alarm is disabled
6 to 3	-	-	unused
2 to 0	WEEKDAY_ALARM	0 to 6	weekday alarm information coded in BCD format

[1] Default value.

8.5.5 Alarm flag

By clearing the MSB, AE_x (Alarm Enable), of one or more of the alarm registers the corresponding alarm condition(s) are active. When an alarm occurs, AF (register Control_2, see Table 8) is set logic 1. The asserted AF can be used to generate an interrupt ($\overline{INT}$). The AF is cleared using the interface.



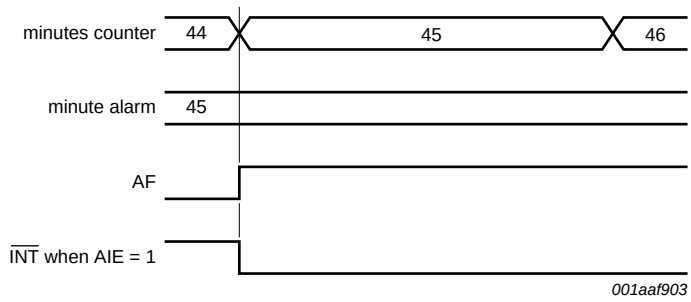
(1) Only when all enabled alarm settings are matching.
It's only on increment to a matched case that the alarm flag is set, see Section 8.5.5.

Fig 12. Alarm function block diagram

The registers at addresses 09h through 0Ch contain alarm information. When one or more of these registers is loaded with minute, hour, day, or weekday, and its corresponding Alarm Enable bit (AE_x) is logic 0, then that information is compared with the current minute, hour, day, and weekday. When all enabled comparisons first match, the Alarm Flag (AF) is set logic 1.

The generation of interrupts from the alarm function is controlled via bit AIE (register Control_2, see Table 8). If bit AIE is enabled, the $\overline{INT}$ pin follows the condition of bit AF. AF will remain set until cleared by the interface. Once AF has been cleared, it will only be set again when the time increments to match the alarm condition once more. Alarm registers which have their AE_x bit logic 1 are ignored.

Generation of interrupts from the alarm function is described in Section 8.7.3.



Example where only the minute alarm is used and no other interrupts are enabled.

Fig 13. Alarm flag timing

Figure 13, Table 23, and Table 24 show an example for clearing bit AF, but leaving bit MSF and bit TF unaffected. The flags are cleared by a write command, therefore bits 7, 6, 4, 1 and 0 must be written with their previous values. Repeatedly re-writing these bits has no influence on the functional behavior.

To prevent the timer flags being overwritten while clearing bit AF, logic AND is performed during a write access. A flag is cleared by writing logic 0 whilst a flag is not cleared by writing logic 1. Writing logic 1 will result in the flag value remaining unchanged.

Table 23. Flag location in register Control_2

Register	Bit							
	7	6	5	4	3	2	1	0
Control_2	-	-	MSF	-	AF	TF	-	-

Table 24 shows what instruction must be sent to clear bit AF. In this example, bit MSF and bit TF are unaffected.

Table 24. Example to clear only AF (bit 3) in register Control_2

Register	Bit							
	7	6	5	4	3	2	1	0
Control_2	-	-	1	-	0	1	-	-

8.6 Timer functions

The countdown timer has four selectable source clocks allowing for countdown periods in the range from 244 μs to 4 h 15 min. There are also two pre-defined timers which can be used to generate an interrupt once per second or once per minute. For periods greater than 4 hours, the alarm function can be used. Registers 01h, 0Eh and 0Fh are used to control the timer function and output.

8.6.1 Register Timer_clkout

Table 25. Timer_clkout - timer control register (address 0Eh) bit description

Bit	Symbol	Value	Description	Reference
7	-	-	unused	-
6 to 4	COF[2:0]	[1]	CLKOUT control	Section 8.8
3	TE	0	countdown timer is disabled	Section 8.6.4
		1	countdown timer is enabled	
2	-	-	unused	
1 to 0	CTD[1:0]	00	4.096 kHz countdown timer source clock	
		01	64 Hz countdown timer source clock	
		10	1 Hz countdown timer source clock	
		11[2]	$1/60$ Hz countdown timer source clock	

[1] Values of COF[2:0] see Table 36.

[2] Default value.

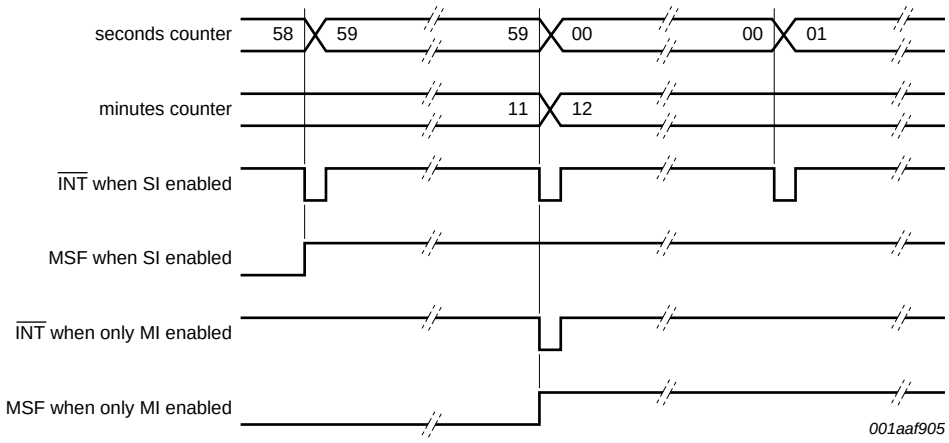
8.6.2 Register Countdown_timer

Table 26. Countdown_timer - countdown timer register (address 0Ah) bit description

Bit	Symbol	Value	Description	Reference
7 to 0	COUNTDOWN_TIMER[7:0]	0h to FFh	countdown period in seconds: $CountdownPeriod = \frac{n}{SourceClockFrequency}$ where n is the countdown value	Section 8.6.4

8.6.3 Minute and second interrupt

The minute and second interrupts (bits MI and SI) are pre-defined timers for generating periodic interrupts. The timers can be enabled independently from one another. However, a minute interrupt enabled on top of a second interrupt will not be distinguishable since it will occur at the same time; see Figure 14.



In this example, TI_TP is set to logic 1 resulting in $1/64$ Hz wide interrupt pulse and the MSF flag is not cleared after an interrupt.

Fig 14. INT example for MI and SI

Table 27. Effect of bits MI and SI on INT generation

Minute interrupt (bit MI)	Second interrupt (bit SI)	Result
0	0	no interrupt generated
1	0	an interrupt once per minute
0	1	an interrupt once per second
1	1	an interrupt once per second

The minute and second flag (bit MSF) is set logic 1 when either the seconds or the minutes counter increments according to the currently enabled interrupt. The flag can be read and cleared by the interface. The status of bit MSF does not affect the INT pulse generation. If the MSF flag is not cleared prior to the next coming interrupt period, an INT pulse will still be generated.

The purpose of the flag is to allow the controlling system to interrogate the PCF2123 and identify the source of the interrupt, i.e., minute or second, countdown timer or alarm.

Table 28. Effect of MI and SI on MSF

Minute interrupt (bit MI)	Second interrupt (bit SI)	Result
0	0	MSF never set
1	0	MSF set when **minutes** counter increments
0	1	MSF set when **seconds** counter increments
1	1	MSF set when **seconds** counter increments

The duration of both of these timers will be affected by the register Offset_register (see Section 8.9). Only when the Offset_register has the value 00h the periods will be consistent.

8.6.4 Countdown timer function

The 8-bit countdown timer at address 0Fh is controlled by the register Timer_clkout at address 0Eh. The register Timer_clkout selects one of 4 source clock frequencies for the timer (4.096 kHz, 64 Hz, 1 Hz, or $1/60$ Hz) and enables or disables the timer.

Table 29. Bits CTD0 and CTD1 for timer frequency selection and countdown timer durations

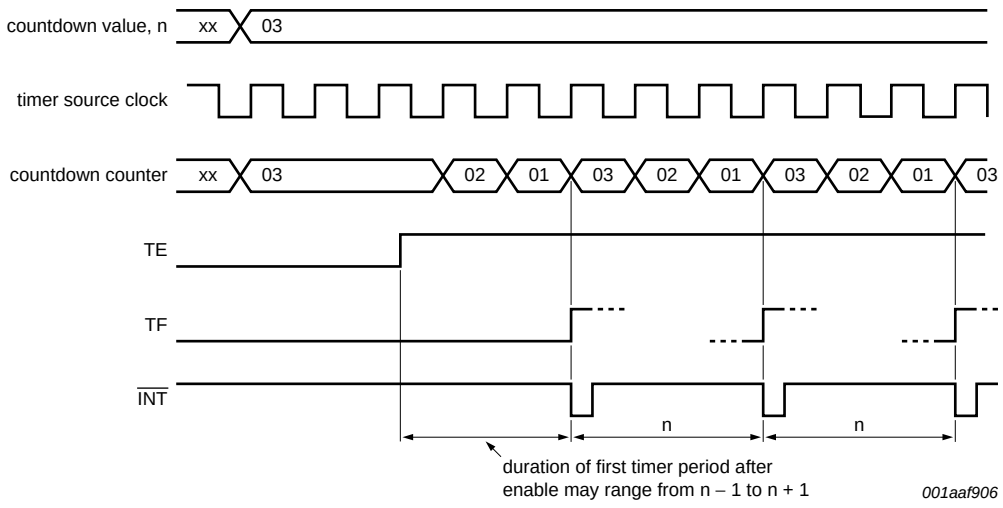
CTD[1:0]	Timer source clock frequency[1]	Delay	
		Minimum timer duration n = 1	Maximum timer duration n = 255
00	4.096 kHz	244 μs	62.256 ms
01	64 Hz	15.625 ms	3.984 s
10	1 Hz[2]	1 s	255 s
11	$1/60$ Hz[2]	60 s	4 h 15 min

[1] When not in use, CTD must be set to $1/60$ Hz for power saving.

[2] Time periods can be affected by correction pulses.

Remark: Note that all timings which are generated from the 32.768 kHz oscillator are based on the assumption that there is 0 ppm deviation. Deviation in oscillator frequency will result in deviation in timings. This is not applicable to interface timing.

The timer counts down from a software-loaded 8-bit binary value, n. Loading the counter with 0 stops the timer. Values from 1 to 255 are valid. When the counter reaches 1, the countdown timer flag (bit TF) will be set and the counter automatically re-loads and starts the next timer period. Reading the timer will return the current value of the countdown counter (see Figure 15).



In this example it is assumed that the timer flag is cleared before the next countdown period expires and that the pin $\overline{INT}$ is set to pulsed mode.

Fig 15. General countdown timer behavior

If a new value of n is written before the end of the current timer period, then this value will take immediate effect. NXP does not recommend changing n without first disabling the counter (by setting bit TE = 0). The update of n is asynchronous to the timer clock,

therefore changing it without setting bit TE = 0 may result in a corrupted value loaded into the countdown counter which results in an undetermined countdown period for the first period. The countdown value n will, however, be correctly stored and correctly loaded on subsequent timer periods.

When the countdown timer flag is set, an interrupt signal on $\overline{INT}$ will be generated provided that this mode is enabled. See Section 8.7.2 for details on how the interrupt can be controlled.

When starting the timer for the first time, the first period will have an uncertainty which is a result of the enable instruction being generated from the interface clock which is asynchronous from the timer source clock. Subsequent timer periods will have no such delay. The amount of delay for the first timer period will depend on the chosen source clock, see Table 30.

Table 30. First period delay for timer counter value n

Timer source clock	Minimum timer period	Maximum timer period
4.096 kHz	n	n + 1
64 Hz	n	n + 1
1 Hz	(n – 1) + $\frac{1}{64}$ Hz	n + $\frac{1}{64}$ Hz
$\frac{1}{60}$ Hz	(n – 1) + $\frac{1}{64}$ Hz	n + $\frac{1}{64}$ Hz

At the end of every countdown, the timer sets the countdown timer flag (bit TF). Bit TF may only be cleared by software. The asserted bit TF can be used to generate an interrupt ($\overline{INT}$). The interrupt may be generated as a pulsed signal every countdown period or as a permanently active signal which follows the condition of bit TF. Bit TI_TP is used to control this mode selection and the interrupt output may be disabled with bit TIE, see Table 8.

When reading the timer, the current countdown value is returned and **not** the initial value n. Since it is not possible to freeze the countdown timer counter during read back, it is recommended to read the register twice and check for consistent results.

Timer source clock frequency selection of 1 Hz and $\frac{1}{60}$ Hz will be affected by the Offset_register. The duration of a program period will vary according to when the offset is initiated. For example, if a 100 s timer is set using the 1 Hz clock as source, then some 100 s periods will contain correction pulses and therefor be longer or shorter depending on the setting of the Offset_register. See Section 8.9 to understand the operation of the Offset_register.

8.6.5 Timer flags

When a minute or second interrupt occurs, bit MSF is set logic 1. Similarly, at the end of a timer countdown or alarm event, bit TF or AF are set logic 1. These bits maintain their value until overwritten by software. If both countdown timer and minute or second interrupts are required in the application, the source of the interrupt can be determined by reading these bits. To prevent one flag being overwritten while clearing another a logical AND is performed during a write access. A flag is cleared by writing logic 0 whilst a flag is not cleared by writing logic 1. Writing logic 1 will result in the flag value remaining unchanged.

Three examples are given for clearing the flags. Clearing the flags is made by a write command, therefore bits 7, 6, 4, 1 and 0 must be written with their previous values. Repeatedly re-writing these bits has no influence on the functional behavior.

Table 31. Flag location in register Control_2

Register	Bit							
	7	6	5	4	3	2	1	0
Control_2	-	-	MSF	-	AF	TF	-	-

Table 32, Table 33, and Table 34 show what instruction must be sent to clear the appropriate flag.

Table 32. Example to clear only TF (bit 2) in register Control_2

Register	Bit							
	7	6	5	4	3	2	1	0
Control_2	-	-	1	-	1	0	-	-

Table 33. Example to clear only MSF (bit 5) in register Control_2

Register	Bit							
	7	6	5	4	3	2	1	0
Control_2	-	-	0	-	1	1	-	-

Table 34. Example to clear both TF and MSF (bit 2 and bit 5) in register Control_2

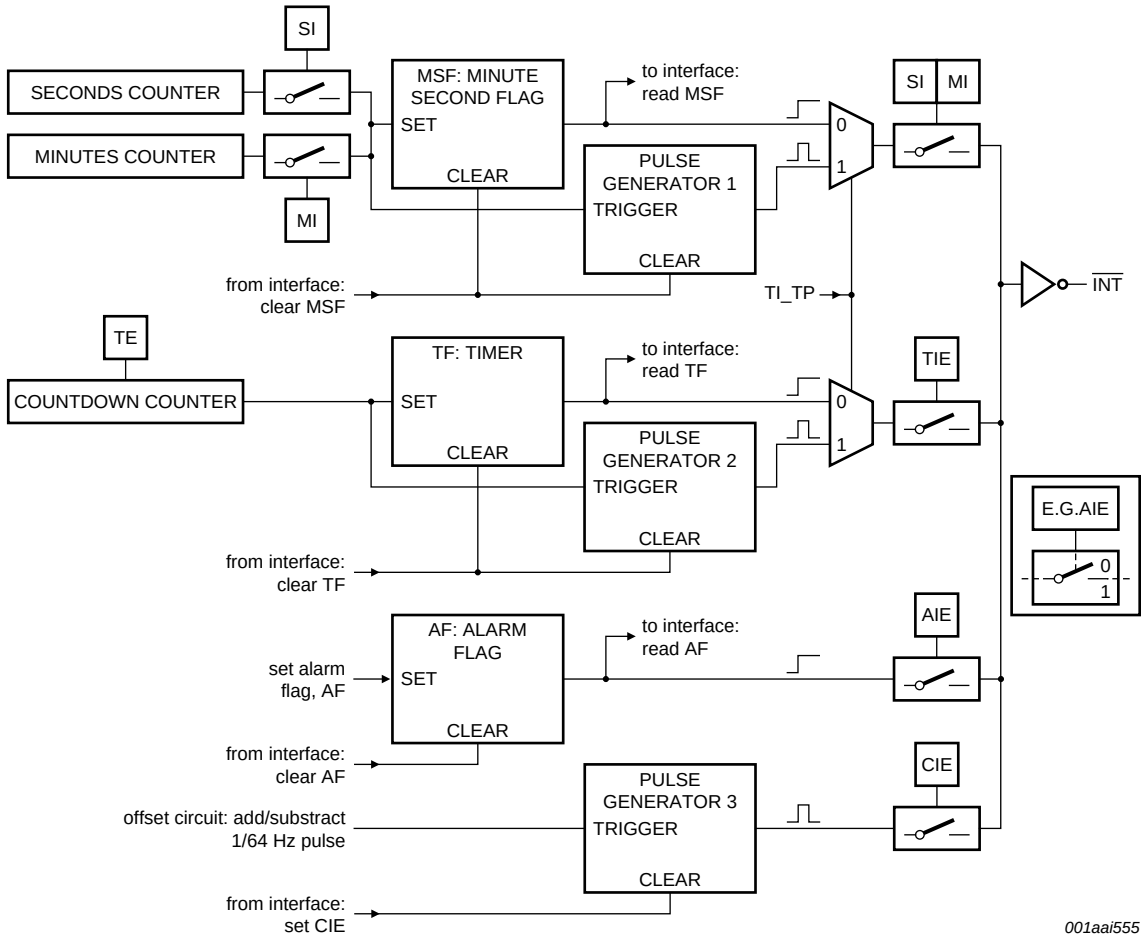
Register	Bit							
	7	6	5	4	3	2	1	0
Control_2	-	-	0	-	1	0	-	-

Clearing the alarm flag (bit AF) operates in exactly the same way, see Section 8.5.5.

8.7 Interrupt output

An active LOW interrupt signal is available at pin $\overline{INT}$. Operation is controlled via the bits of register Control_2. Interrupts may be sourced from four places: second and minute timer, countdown timer, alarm function or offset function.

With bit TI_TP, the timer generated interrupts can be configured to either generate a pulse or to follow the status of the interrupt flags (bits TF and MSF). Correction interrupt pulses are always $^{1}/_{128}$ second long. Alarm interrupts always follow the condition of AF.



When bits SI, MI, TIE, AIE, and CIE are all disabled, pin $\overline{INT}$ will remain high-impedance.

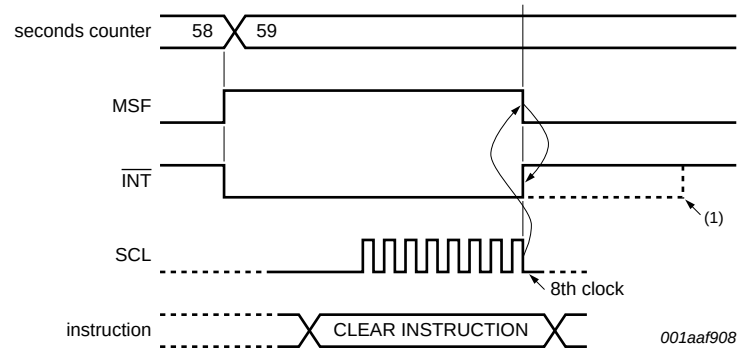
Fig 16. Interrupt scheme

Remark: Note that the interrupts from the four sources are wired-OR, meaning they will mask one another (see Figure 16).

8.7.1 Minute and second interrupts

The pulse generator for the minute and second interrupt operates from an internal 64 Hz clock and consequently generates a pulse of $^1/_{64}$ second in duration.

If the MSF flag is cleared before the end of the $\overline{INT}$ pulse, then the $\overline{INT}$ pulse is shortened. This allows the source of a system interrupt to be cleared immediately it is serviced, i.e., the system does not have to wait for the completion of the pulse before continuing; see Figure 17. Instructions for clearing MSF are given in Section 8.6.5.



(1) Indicates normal duration of $\overline{INT}$ pulse (bit TI_TP = 1)

Fig 17. Example of shortening the $\overline{INT}$ pulse by clearing the MSF flag

The timing shown for clearing bit MSF in Figure 17 is also valid for the non-pulsed interrupt mode i.e. when bit TI_TP = 0, $\overline{INT}$ may be shortened by setting both MI and SI or MSF to logic 0.

8.7.2 Countdown timer interrupts

The generation of interrupts from the countdown timer is controlled via bit TIE.

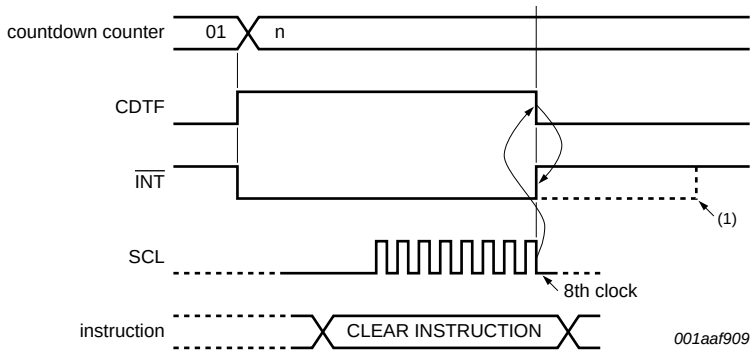
The pulse generator for the countdown timer interrupt also uses an internal clock, but this time it is dependent on the selected source clock for the countdown timer and on the countdown value n. As a consequence, the width of the interrupt pulse varies (see Table 35).

Table 35. $\overline{INT}$ operation (bit TI_TP = 1)

Source clock (Hz)	$\overline{INT}$ period (s)	
	n = 1[1]	n > 1
4096	$^1/_{8192}$	$^1/_{4096}$
64	$^1/_{128}$	$^1/_{64}$
1	$^1/_{64}$	$^1/_{64}$
$^1/_{60}$	$^1/_{64}$	$^1/_{64}$

[1] n = loaded countdown value. Timer stopped when n = 0.

If the TF flag is cleared before the end of the $\overline{INT}$ pulse, then the $\overline{INT}$ pulse is shortened. This allows the source of a system interrupt to be cleared immediately it is serviced, i.e., the system does not have to wait for the completion of the pulse before continuing (see Figure 18). Instructions for clearing MSF can be found in Section 8.6.5.



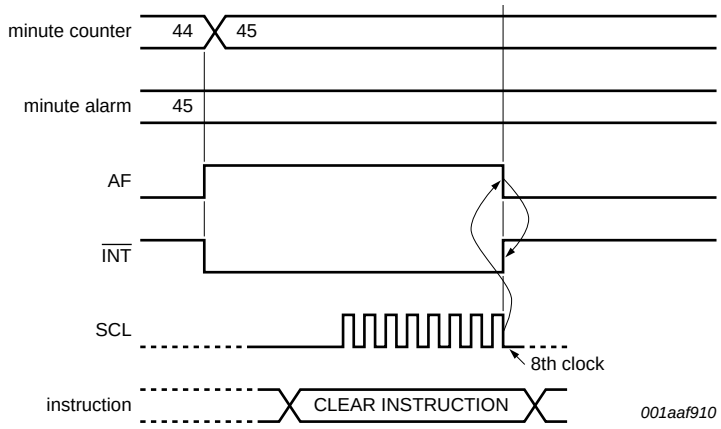
(1) Indicates normal duration of $\overline{INT}$ pulse (bit TI_TP = 1).

Fig 18. Example of shortening the $\overline{INT}$ pulse by clearing the TF flag

The timing shown for clearing bit TF in Figure 18 is also valid for the non-pulsed interrupt mode, i.e., when bit TI_TP = 0; $\overline{INT}$ may be shortened by setting bit TIE to logic 0.

8.7.3 Alarm interrupts

The generation of interrupts from the alarm function is controlled via bit AIE (see Table 8). If bit AIE is enabled, the $\overline{INT}$ pin follows the condition of bit AF. Clearing bit AF will immediately clear $\overline{INT}$. No pulse generation is possible for alarm interrupts (see Figure 19).



Example where only the minute alarm is used and no other interrupts are enabled.

Fig 19. AF timing

8.7.3.1 Correction pulse interrupts

Interrupt pulses generated by correction events can be shortened by writing logic 1 to bit CIE in register Control_1.

8.8 Clock output

A programmable square wave is available at pin CLKOUT. Operation is controlled by the COF[2:0] bits in the register Timer_clkout. Frequencies of 32.768 kHz (default) down to 1 Hz can be generated for use as a system clock, microcontroller clock, input to a charge pump, or for calibration of the oscillator.

Pin CLKOUT is an open-drain output and enabled at power-on. When disabled the output is high-impedance.

The duty cycle of the selected clock is not controlled. However, due to the nature of the clock generation, all will be 50 : 50 except the 32.768 kHz frequencies.

The STOP bit function can also affect the CLKOUT signal, depending on the selected frequency. When the STOP bit is set logic 1, the CLKOUT pin will generate a continuous LOW for those frequencies that can be stopped. For more details of the STOP bit function see Section 8.11.

Table 36. CLKOUT frequency selection

Bits COF[2:0]	CLKOUT frequency (Hz)	Typical duty cycle[1]	Effect of STOP bit
000	32768	60 : 40 to 40 : 60	no effect
001	16384	50 : 50	no effect
010	8192	50 : 50	no effect
011	4096	50 : 50	CLKOUT = LOW
100	2048	50 : 50	CLKOUT = LOW
101	1024	50 : 50	CLKOUT = LOW
110	1[2]	50 : 50	CLKOUT = LOW
111	CLKOUT = high-Z	-	-

[1] Duty cycle definition: % HIGH-level time : % LOW-level time.

[2] 1 Hz clock pulses will be affected by offset correction pulses.

8.8.1 CLKOE pin

The CLKOE pin can be used to block the CLKOUT function and force the CLKOUT pin to a high-impedance state. The effect is the same as setting COF[2:0] = 111.

8.9 Offset register

The PCF2123 incorporates an offset register (address 0Dh) which can be used to implement several functions, such as:

- Ageing adjustment
- Temperature compensation
- Accuracy tuning

The offset is made once every two hours in the normal mode, or once every hour in the course mode. Each LSB will introduce an offset of 2.17 ppm for normal mode and 4.34 ppm for course mode. The values of 2.17 ppm and 4.34 ppm are based on a nominal 32.768 kHz clock. The offset value is coded in two's complement giving a range of +63 LSB to −64 LSB.

Table 37. Register Offset_register

OFFSET[6:0]	Offset value in decimal	Offset value in ppm	
		Normal mode MODE = 0	Course mode MODE = 1
0 1 1 1 1 1 1	+63	+136.71	+273.42
0 1 1 1 1 1 0	+62	+134.54	+269.08
:	:	:	:
0 0 0 0 0 1 0	+2	+4.34	+8.68
0 0 0 0 0 0 1	+1	+2.17	+4.34
0 0 0 0 0 0 0	0[1]	0	0
1 1 1 1 1 1 1	−1	−2.17	−4.34
1 1 1 1 1 1 0	−2	−4.34	−8.68
:	:	:	:
1 0 0 0 0 0 1	−63	−136.71	−273.42
1 0 0 0 0 0 0	−64	−138.88	−277.76

[1] Default mode.

The correction is made by adding or subtracting 64 Hz clock correction pulses, thereby changing the period of a single second.

Table 38. Example of converting the offset in ppm to seconds

Offset in ppm	Seconds per			
	Day	Week	Month	Year
2.17	0.187	1.31	5.69	68.2
4.34	0.375	2.62	11.4	136

In normal mode, the correction is triggered once per two hours and then correction pulses are applied once per minute until the programmed correction values have been implement.

In course mode, the correction is triggered once per hour and then correction pulses are applied once per minute up to a maximum of 60 minutes. When correction values greater than 60 are used, additional correction pulses are made in the 59th minute (see Table 39).

Table 39. Correction pulses for course mode

Correction value	Hour:Minute[1]	Correction pulses on $\overline{INT}$ per minute[2]
+1 or −1	02:00	1
	02:01 to 02:59	0
+2 or −2	02:00	1
	02:01	1
	02:02 to 02:59	0
+3 or −3	02:00	1
	02:01	1
	02:02	1
	02:03 to 02:59	0
:	:	:
+59 or −59	02:00 to 02:58	1
	02:59	0
+60 or −60	02:00 to 02:59	1
+61 or −61	02:00 to 02:58	1
	02:59	2
+62 or −62	02:00 to 02:58	1
	02:59	3
+63 or −63	02:00 to 02:58	1
	02:59	4
−64	02:00 to 02:58	1
	02:59	5

[1] Example is given in a time range from 2:00 to 2:59.

[2] Correction $\overline{INT}$ pulses are $\frac{1}{128}$ s wide. For multiple pulses they are repeated at $\frac{1}{64}$ s interval.

It is possible to monitor when correction pulses are applied. The correction interrupt enable mode (bit CIE) will generate a $\frac{1}{128}$ second pulse on $\overline{INT}$ for every correction applied. In the case where multiple correction pulses are applied, a $\frac{1}{128}$ second interrupt pulse will be generated and repeated every $\frac{1}{64}$ seconds.

Correction is applied to the 1 Hz clock. Any timer or clock output using a frequency of 1 Hz or below will also be affected by the correction pulses.

Table 40. Effect of correction pulses

Frequency (Hz)	Effect of correction
CLKOUT	
32768	no effect
16384	no effect
8192	no effect
4096	no effect
2048	no effect
1024	no effect
1	affected
Time source clock	
4096	no effect
64	no effect
1	affected
$^1/_{60}$	affected

8.9.1 Offset calibration workflow

The calibration offset has to be calculated based on the time. Figure 20 shows the workflow how the offset register values can be calculated:

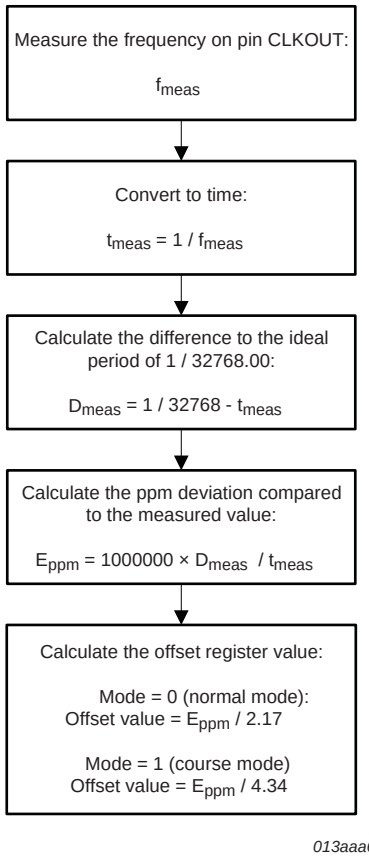


Fig 20. Offset calibration calculation workflow

8.10 External clock test mode

A test mode is available which allows for on-board testing. In this mode it is possible to set up test conditions and control the operation of the RTC.

The test mode is entered by setting bit EXT_TEST in register Control_1. Then pin CLKOUT becomes an input. The test mode replaces the internal clock signal with the signal applied to pin CLKOUT.

The signal applied to pin CLKOUT should have a minimum pulse width of 300 ns and a maximum period of 1000 ns. The internal clock, now sourced from CLKOUT, is divided down to 1 Hz by a 2^6 divide chain called a prescaler. The prescaler can be set into a known state by using bit STOP. When bit STOP is set, the prescaler is reset to 0. (STOP must be cleared before the prescaler can operate again.)

From a stop condition, the first 1 second increment will take place after 32 positive edges on pin CLKOUT. Thereafter, every 64 positive edges will cause a 1 second increment.

Remark: Entry into test mode is not synchronized to the internal 64 Hz clock. When entering the test mode, no assumption as to the state of the prescaler can be made.

Operation example:

1. Set EXT_TEST test mode (register Control_1, bit EXT_TEST = 1).
2. Set STOP (Control_1, bit STOP = 1).
3. Clear STOP (Control_1, bit STOP = 0).
4. Set time registers to desired value.
5. Apply 32 clock pulses to pin CLKOUT.
6. Read time registers to see the first change.
7. Apply 64 clock pulses to pin CLKOUT.
8. Read time registers to see the second change.

Repeat 7 and 8 for additional increments.

8.11 STOP bit function

The function of the STOP bit is to allow for accurate starting of the time circuits. The STOP bit function will cause the upper part of the prescaler (F_2 to F_{14}) to be held in reset and thus no 1 Hz ticks will be generated. The time circuits can then be set and will not increment until the STOP bit is released (see Figure 22 and Table 41).

The STOP bit function will not affect the output of 32.768 kHz, 16.384 kHz, or 8.192 kHz (see Section 8.8).

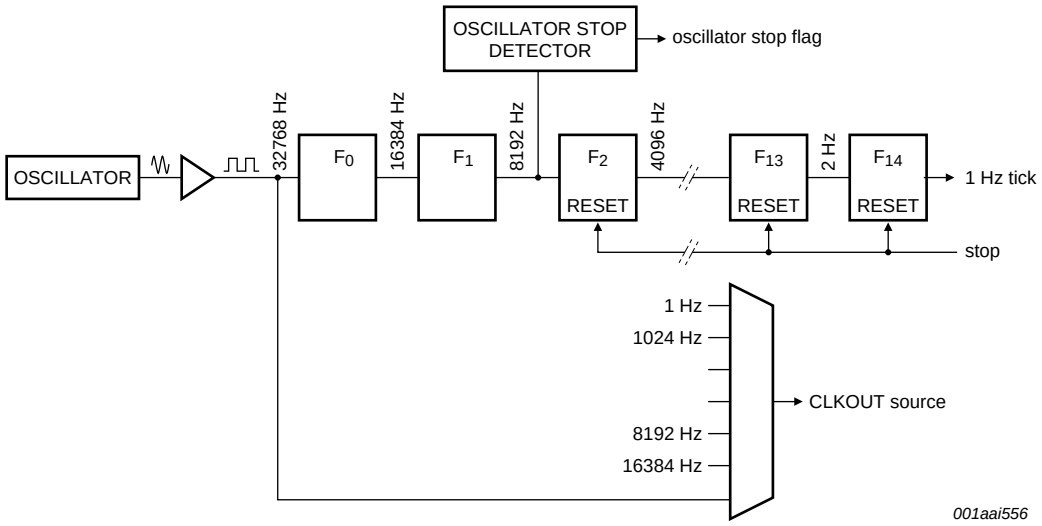


Fig 21. STOP bit functional diagram

The lower two stages of the prescaler (F_0 and F_1) are not reset and because the SPI-bus is asynchronous to the crystal oscillator, the accuracy of re-starting the time circuits will be between 0 and one 8.192 kHz cycle (see Figure 22).

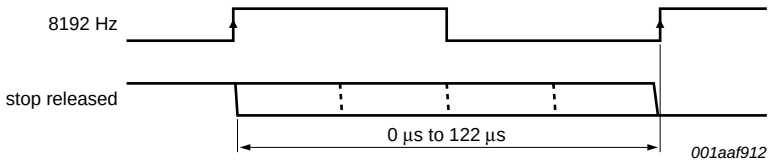
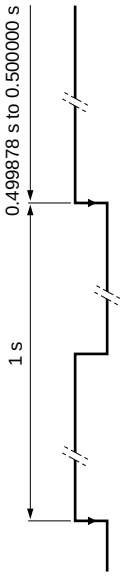


Fig 22. STOP bit release timing

The first increment of the time circuits is between 0.499878 s and 0.500000 s after STOP bit is released. The uncertainty is caused by the prescaler bits F_0 and F_1 not being reset (see Table 41).

Table 41. First increment of time circuits after STOP bit release

Bit	Prescaler bits[1]	1 Hz tick	Time	Comment
STOP	F_0F_1-F_2 to F_{14}		hh:mm:ss	
Clock is running normally				
0	01-0 0001 1101 0100		12:45:12	prescaler counting normally
STOP bit is activated by user. F_0F_1 are not reset and values cannot be predicted externally				
1	XX-0 0000 0000 0000		12:45:12	prescaler is reset; time circuits are frozen
New time is set by user				
1	XX-0 0000 0000 0000		08:00:00	prescaler is reset; time circuits are frozen
STOP bit is released by user				
0	XX-0 0000 0000 0000		08:00:00	prescaler is now running
	XX-1 0000 0000 0000	0.499878 s to 0.500000 s	08:00:00	-
	XX-0 1000 0000 0000		08:00:00	-
	XX-1 1000 0000 0000		08:00:00	-
	:		:	:
	11-1 1111 1111 1110		08:00:00	-
	00-0 0000 0000 0001		08:00:01	0 to 1 transition of F_{14} increments the time circuits
	10-0 0000 0000 0001		08:00:01	-
	:		:	:
	11-1 1111 1111 1111	1 s	08:00:01	-
	00-0 0000 0000 0000		08:00:01	-
	10-0 0000 0000 0000		08:00:01	-
	:		:	:
	11-1 1111 1111 1110		08:00:01	-
	00-0 0000 0000 0001		08:00:02	0 to 1 transition of F_{14} increments the time circuits



[1] F_0 is clocked at 32.768 kHz.

9. 3-line serial interface

Data transfer to and from the device is made via a 3-wire SPI-bus (see Table 42). The data lines for input and output are split. The data input and output lines can be connected together to facilitate a bidirectional data bus. The chip enable signal is used to identify the transmitted data. Each data transfer is a byte, with the Most Significant Bit (MSB) sent first (see Figure 24).

Table 42. Serial interface

Symbol	Function	Description
CE	chip enable input	when LOW, the interface is reset; pull-down resistor included; active input may be higher than V_{DD}, but may not be wired permanently HIGH
SCL	serial clock input	when CE is LOW, this input may float; input may be higher than V_{DD}
SDI	serial data input	when CE is LOW, input may float; input may be higher than V_{DD}; input data is sampled on the rising edge of SCL
SDO	serial data output	push-pull output; drives from V_{SS} to V_{DD}; output data is changed on the falling edge of SCL; will be high-Z when not driving; may be connected directly to SDI

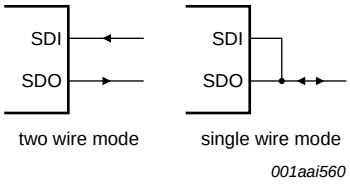


Fig 23. SDI, SDO configurations

The transmission is controlled by the active HIGH chip enable signal CE. The first byte transmitted is the command byte. Subsequent bytes will be either data to be written or data to be read. Data is sampled on the rising edge of the clock and transferred internally on the falling edge.

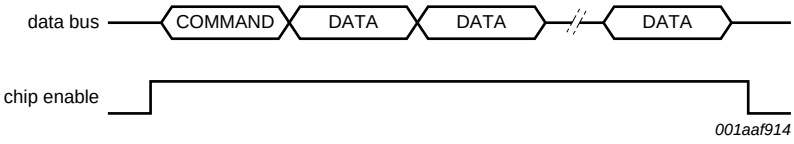


Fig 24. Data transfer overview

The command byte defines the address of the first register to be accessed and the read/write mode. The address counter will auto increment after every access and will rollover to zero after the last register is accessed. The read/write bit (R/W) defines if the following bytes will be read or write information.

Table 43. Command byte definition

Bit	Symbol	Value	Description
7	R/$\overline{W}$		data read or data write selection
		0	write data
		1	read data
6 to 4	SA	001	subaddress; other codes will cause the device to ignore data transfer
3 to 0	RA	0h to Fh	register address range

In Figure 25, the register Seconds is set to 45 seconds and the register Minutes is set to 10 minutes.

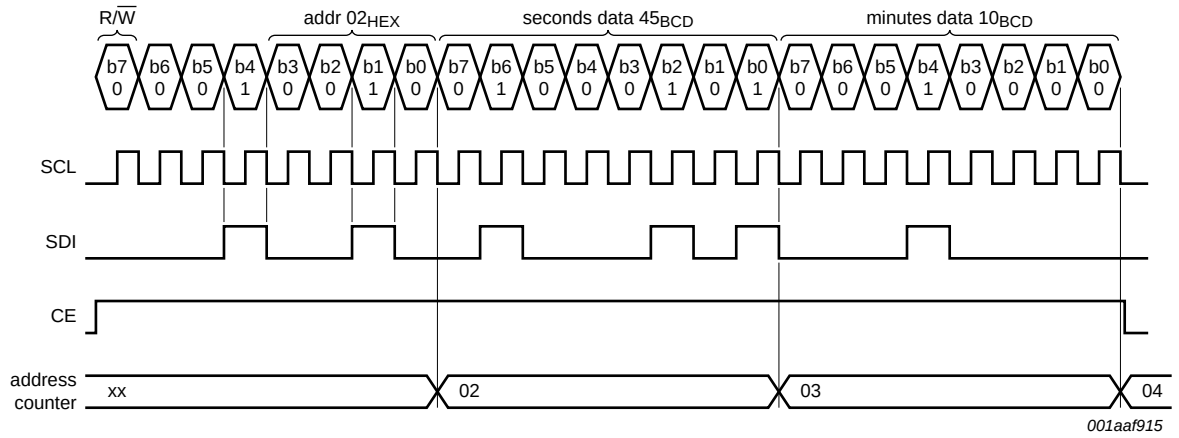


Fig 25. Serial bus write example

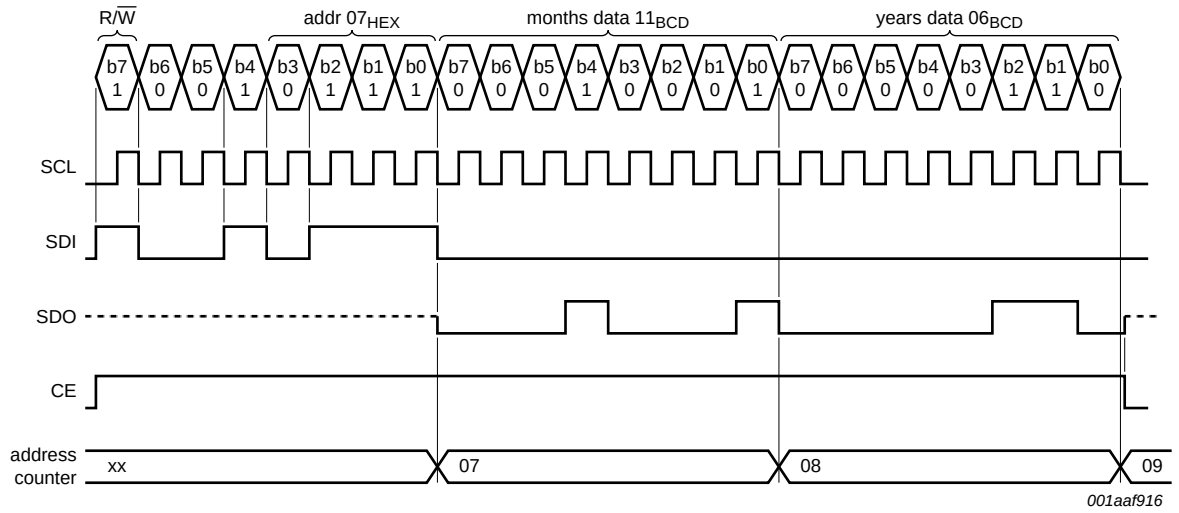
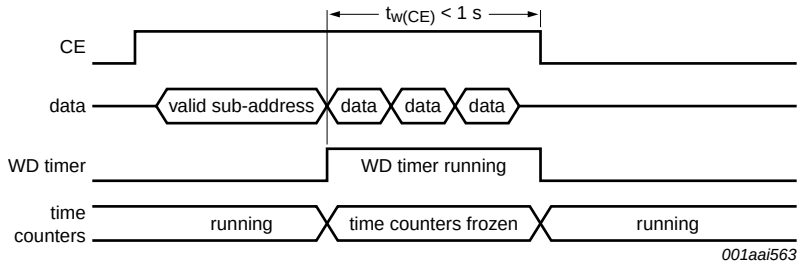


Fig 26. Serial bus read example

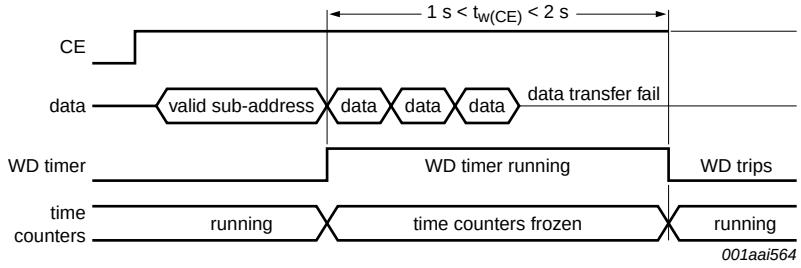
In Figure 26, the Months and Years registers are read. In this example, pins SDI and SDO are not connected together. For this configuration, it is important that pin SDI is never left floating. It must always be driven either HIGH or LOW. If pin SDI is left open, high I_{DD} currents may result. Short transition periods in the order of 200 ns will not cause any problems.

9.1 Interface watchdog timer

During read/write operations, the time counting circuits are frozen. To prevent a situation where the accessing device becomes locked and does not clear the interface by setting pin CE LOW, the PCF2123 has a built in watchdog timer. Should the interface be active for more than 1 s from the time a valid subaddress is transmitted, then the PCF2123 will automatically clear the interface and allow the time counting circuits to continue counting. CE must return LOW once more before a new data transfer can be executed.



a. Correct data transfer: read or write



b. Incorrect data transfer: read or write

Fig 27. Interface watchdog timer

The watchdog is implemented to prevent the excessive loss of time due to interface access failure e.g. if main power is removed from a battery backed-up system during an interface access.

Each time the watchdog period is exceeded, 1 s will be lost from the time counters. The watchdog will trigger between 1 s and 2 s after receiving a valid subaddress.

10. Internal circuitry

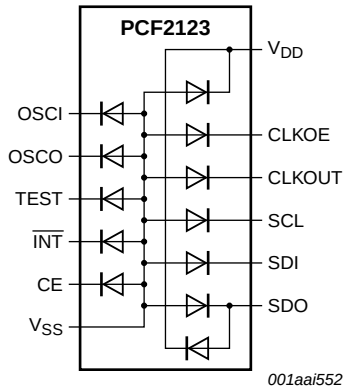


Fig 28. Device diode protection diagram of PCF2123

11. Safety notes

CAUTION

This device is sensitive to ElectroStatic Discharge (ESD). Observe precautions for handling electrostatic sensitive devices.

Such precautions are described in the *ANSI/ESD S20.20*, *IEC/ST 61340-5*, *JESD625-A* or equivalent standards.

CAUTION

Semiconductors are light sensitive. Exposure to light sources can cause the IC to malfunction. The IC must be protected against light. The protection must be applied to all sides of the IC.

12. Limiting values

Table 44. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions		Min	Max	Unit
V_{DD}	supply voltage		[1]	−0.5	+6.5	V
I_{DD}	supply current			−50	+50	mA
V_I	input voltage		[1]	−0.5	+6.5	V
V_O	output voltage		[1]	−0.5	+6.5	V
I_I	input current			−10	+10	mA
I_O	output current			−10	+10	mA
P_{tot}	total power dissipation			-	300	mW
V_{ESD}	electrostatic discharge voltage	HBM	[2]	-	±3000	V
I_{lu}	latch-up current		[3]	-	200	mA
T_{stg}	storage temperature		[4]	−65	+150	°C
T_{amb}	ambient temperature	operating device		−40	+85	°C

[1] With respect to V_{SS}.

[2] Pass level; Human Body Model (HBM) according to Ref. 9 “JESD22-A114”

[3] Pass level; latch-up testing, according to Ref. 10 “JESD78” at maximum ambient temperature ($T_{amb(max)}$).

[4] According to the store and transport requirements (see Ref. 14 “UM10569”) the devices have to be stored at a temperature of +8 °C to +45 °C and a humidity of 25 % to 75 %.

13. Static characteristics

Table 45. Static characteristics

V_{DD} = 1.1 V to 5.5 V; V_{SS} = 0 V; T_{amb} = −40 °C to +85 °C; f_{osc} = 32.768 kHz; quartz R_s = 15 kΩ; C_L = 7 pF; unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
Supplies							
V_{DD}	supply voltage	for clock data integrity; SPI-bus inactive	[1]	1.1	-	5.5	V
		T_{amb} = 25 °C		-	0.9	-	V
		SPI-bus active		1.8	-	5.5	V
I_{DD}	supply current	SPI-bus active					
		f_{SCL} = 4.5 MHz; V_{DD} = 5 V		-	250	400	µA
		f_{SCL} = 1.0 MHz; V_{DD} = 3 V		-	30	80	µA
		SPI-bus inactive; CLKOUT disabled	[2]				
		T_{amb} = 25 °C; V_{DD} = 2.0 V		-	100	-	nA
		T_{amb} = 25 °C; V_{DD} = 3.0 V		-	110	-	nA
		T_{amb} = 25 °C; V_{DD} = 5.0 V		-	120	-	nA
		SPI-bus inactive; CLKOUT disabled; T_{amb} = −40 °C to +85 °C	[2]				
		V_{DD} = 2.0 V		-	-	330	nA
		V_{DD} = 3.0 V		-	-	350	nA
		V_{DD} = 5.0 V		-	-	380	nA
		SPI-bus inactive; CLKOUT enabled at 32 kHz; T_{amb} = 25 °C					
		V_{DD} = 2.0 V		-	260	-	nA
		V_{DD} = 3.0 V		-	340	-	nA
		V_{DD} = 5.0 V		-	520	-	nA
		SPI-bus inactive; CLKOUT enabled at 32 kHz; T_{amb} = −40 °C to +85 °C					
		V_{DD} = 2.0 V		-	-	450	nA
		V_{DD} = 3.0 V		-	-	550	nA
		V_{DD} = 5.0 V		-	-	750	nA

Table 45. Static characteristics *...continued*

V_{DD} = 1.1 V to 5.5 V; V_{SS} = 0 V; T_{amb} = −40 °C to +85 °C; f_{osc} = 32.768 kHz; quartz R_s = 15 kΩ; C_L = 7 pF; unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
Inputs							
V_{IL}	LOW-level input voltage			-	-	$0.3V_{DD}$	V
V_{IH}	HIGH-level input voltage			$0.7V_{DD}$	-	-	V
V_I	input voltage	on pins CE, SDI, SCL, OSCI, CLKOE, CLKOUT		−0.5	-	+5.5	V
I_{LI}	input leakage current	$V_I = V_{DD}$ or V_{SS} on pins SDI, SCL, OSCI, CLKOE, CLKOUT	[3]	-	0	-	µA
		$V_I = V_{SS}$ on pin CE		−1	0	-	µA
R_{pd}	pull-down resistance	on pin CE		-	240	550	kΩ
C_i	input capacitance	on pins SDI, SCL, CLKOE and CE	[4]	-	-	7	pF
Outputs							
V_O	output voltage	on pins CLKOUT and $\overline{INT}$	[5]	−0.5	-	+5.5	V
		on pin OSCO		−0.5	-	+5.5	V
		on pin SDO		−0.5	-	V_{DD} + 0.5	V
V_{OH}	HIGH-level output voltage	on pin SDO		$0.8V_{DD}$	-	V_{DD}	V
V_{OL}	LOW-level output voltage	on pin SDO		V_{SS}	-	$0.2V_{DD}$	V
		on pins CLKOUT and $\overline{INT}$; V_{DD} = 5 V; I_{OL} = 1.5 mA		V_{SS}	-	0.4	V
I_{OH}	HIGH-level output current	output source current; V_{OH} = 4.6 V; V_{DD} = 5 V on pin SDO		1.5	-	-	mA
I_{OL}	LOW-level output current	output sink current; V_{OL} = 0.4 V; V_{DD} = 5 V on pins $\overline{INT}$, SDO and CLKOUT		1.5	-	-	mA
I_{LO}	output leakage current	$V_O = V_{DD}$ or V_{SS}	[3]	-	0	-	µA
$C_{L(itg)}$	integrated load capacitance	on pins OSCO and OSCI	[6]	3.3	7	14	pF
R_s	series resistance			-	-	100	kΩ

[1] For reliable oscillator start at power-on: $V_{DD} = V_{DD(min)} + 0.3$ V.

[2] Timer source clock = $\frac{1}{60}$ Hz, level of pins CE, SDI, and SCL is V_{DD} or V_{SS}.

[3] In case of an ESD event, the value may increase slightly.

[4] Implicit by design.

[5] Refers to external pull-up voltage.

[6] Integrated load capacitance, $C_{L(itg)}$, is a calculation of C_{OSCI} and C_{OSCO} in series: $C_{L(itg)} = \frac{(C_{OSCI} \cdot C_{OSCO})}{(C_{OSCI} + C_{OSCO})}$.

14. Dynamic characteristics

Table 46. SPI-bus characteristics

V_{SS} = 0 V; T_{amb} = −40 °C to +85 °C. All timing values are valid within the operating supply voltage and temperature range and referenced to V_{IL} and V_{IH} with an input voltage swing of V_{SS} to V_{DD}.

Symbol	Parameter	Conditions	V_{DD} = 1.8 V		V_{DD} = 2.4 V		V_{DD} = 3.3 V		V_{DD} = 5.0 V		Unit
			Min	Max	Min	Max	Min	Max	Min	Max	
Timing characteristics (see Figure 29)											
$f_{clk(SCL)}$	SCL clock frequency		-	2.9	-	4.54	-	5.71	-	8.0	MHz
t_{SCL}	SCL time		345	-	220	-	175	-	125	-	ns
$t_{clk(H)}$	clock HIGH time		90	-	50	-	45	-	40	-	ns
$t_{clk(L)}$	clock LOW time		200	-	120	-	95	-	70	-	ns
t_r	rise time	for SCL signal	-	100	-	100	-	100	-	100	ns
t_f	fall time	for SCL signal	-	100	-	100	-	100	-	100	ns
$t_{su(CE)}$	CE set-up time		40	-	35	-	30	-	25	-	ns
$t_{h(CE)}$	CE hold time		40	-	30	-	25	-	15	-	ns
$t_{rec(CE)}$	CE recovery time		30	-	25	-	20	-	15	-	ns
$t_{w(CE)}$	CE pulse width	measured after valid subaddress is received	-	0.99	-	0.99	-	0.99	-	0.99	s
t_{su}	set-up time	set-up time for SDI data	10	-	5	-	3	-	2	-	ns
t_h	hold time	hold time for SDI data	25	-	10	-	8	-	5	-	ns
$t_{d(R)SDO}$	SDO read delay time	bus load = 50 pF	-	190	-	108	-	85	-	60	ns
$t_{dis(SDO)}$	SDO disable time	no load value; bus will be held up by bus capacitance; use RC time constant with application values	-	70	-	45	-	40	-	27	ns
$t_{t(SDI-SDO)}$	transition time from SDI to SDO	to avoid bus conflict	0	-	0	-	0	-	0	-	ns

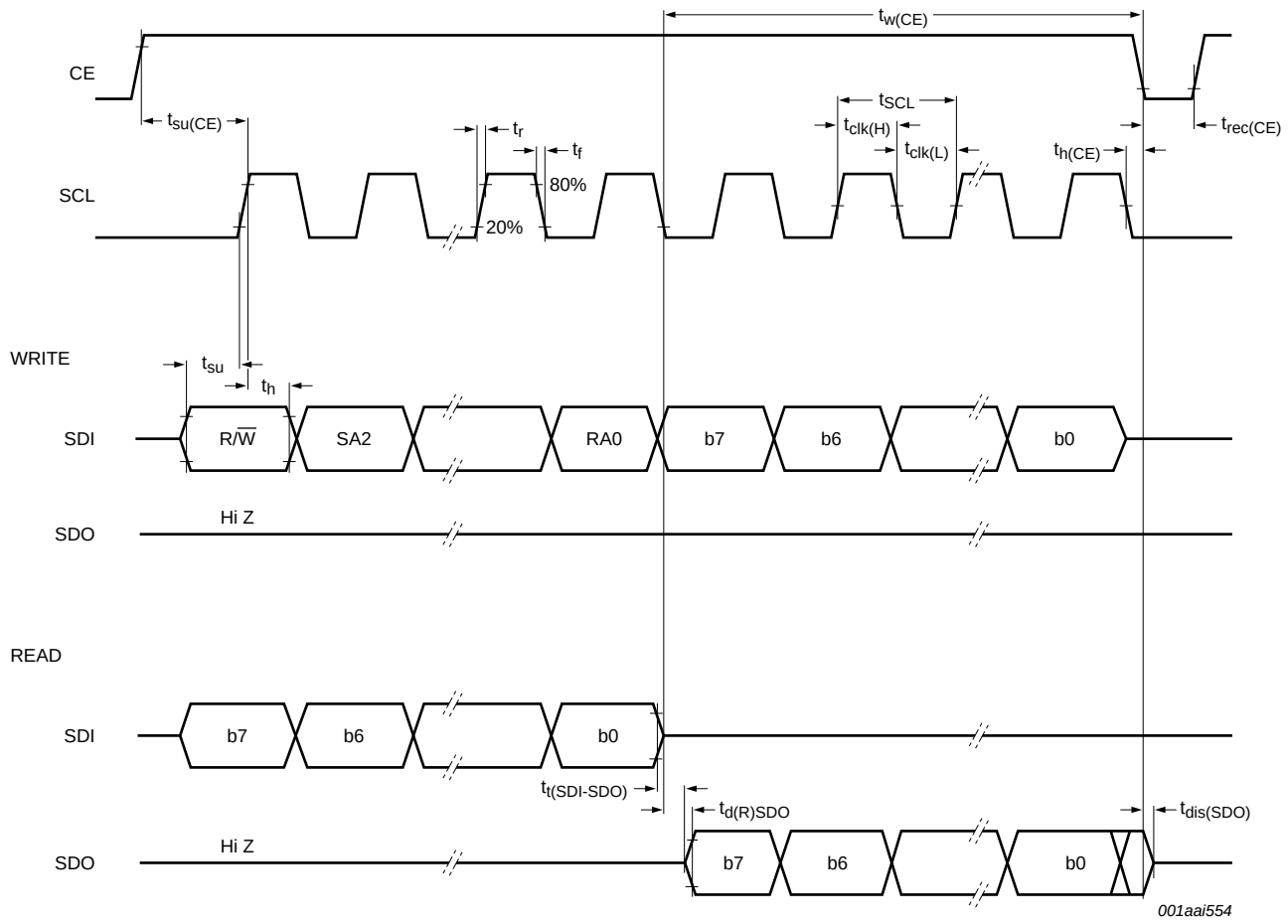
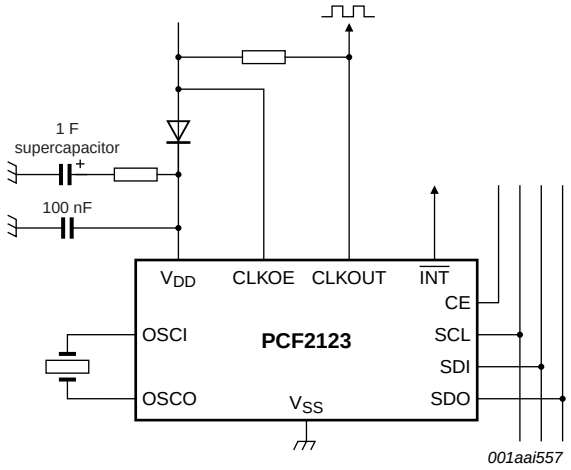


Fig 29. SPI-bus timing

15. Application information

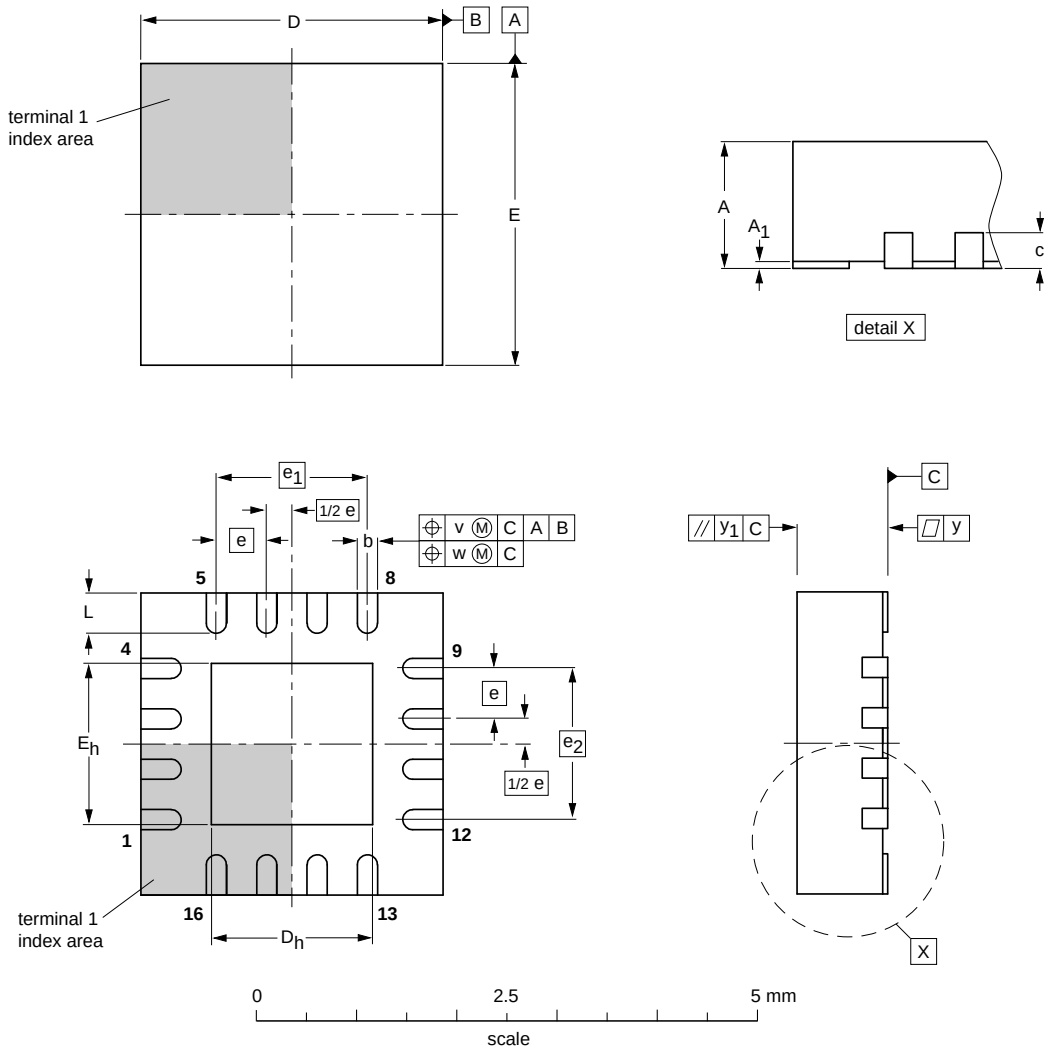


A 1 farad super capacitor combined with a low V_F diode can be used as a standby or back-up supply. With the RTC in its minimum power configuration i.e. timer off and CLKOUT off, the RTC may operate for weeks.

Fig 30. Typical application diagram

16. Package outline

HVQFN16: plastic thermal enhanced very thin quad flat package; no leads; 16 terminals; body 3 x 3 x 0.85 mm **SOT758-1**



DIMENSIONS (mm are the original dimensions)

UNIT	A(1) max.	A_1	b	c	D(1)	D_h	E(1)	E_h	e	e_1	e_2	L	v	w	y	y_1
mm	1	0.05 0.00	0.30 0.18	0.2	3.1 2.9	1.75 1.45	3.1 2.9	1.75 1.45	0.5	1.5	1.5	0.5 0.3	0.1	0.05	0.05	0.1

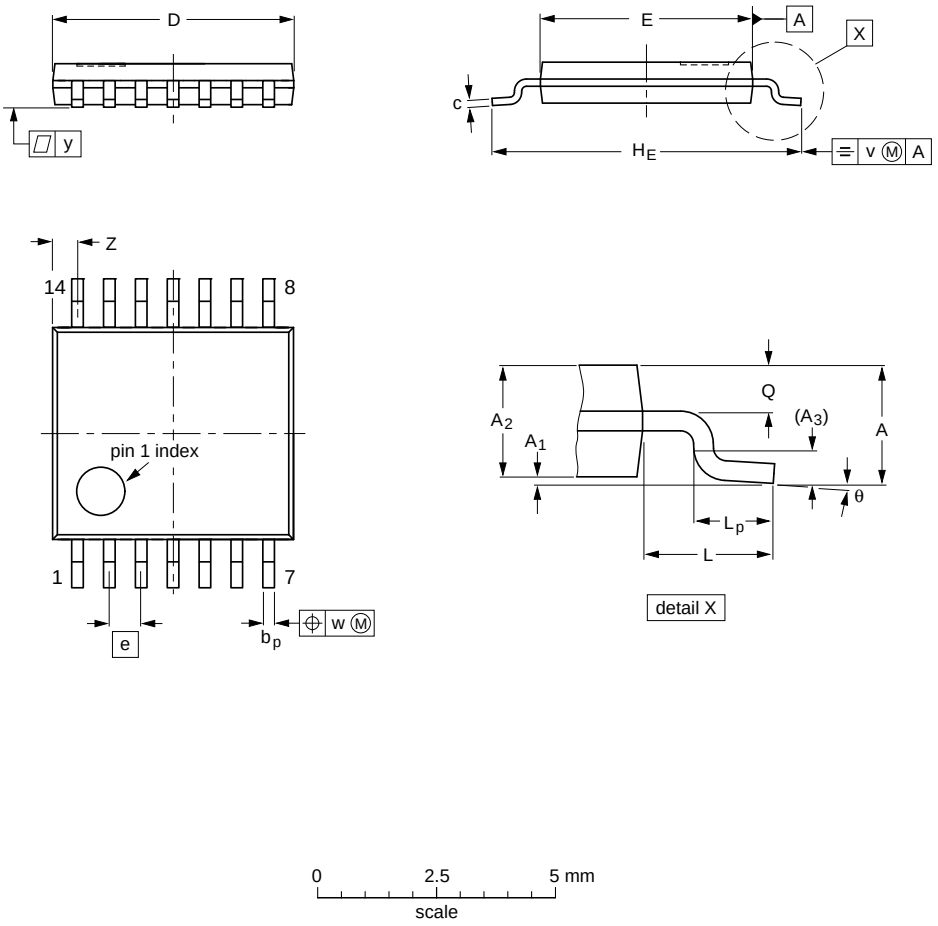
Note

1. Plastic or metal protrusions of 0.075 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT758-1	- - -	MO-220	- - -			~~02-03-25~~ 02-10-21

Fig 31. Package outline SOT758-1 (HVQFN16) of PCF2123BS/1

TSSOP14: plastic thin shrink small outline package; 14 leads; body width 4.4 mm **SOT402-1**



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	D (1)	E (2)	e	H_E	L	L_p	Q	v	w	y	Z (1)	θ
mm	1.1	0.15 0.05	0.95 0.80	0.25	0.30 0.19	0.2 0.1	5.1 4.9	4.5 4.3	0.65	6.6 6.2	1	0.75 0.50	0.4 0.3	0.2	0.13	0.1	0.72 0.38	8^o 0^o

Notes

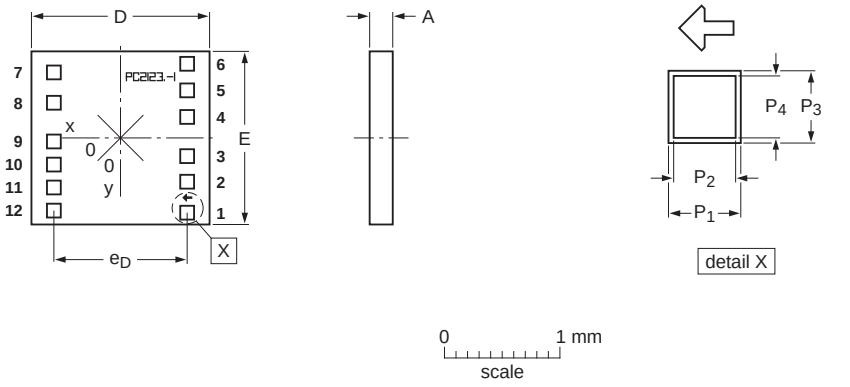
1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.
2. Plastic interlead protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT402-1		MO-153				~~99-12-27~~ 03-02-18

Fig 32. Package outline SOT402-1 (TSSOP14) of PCF2123TS/1

17. Bare die outline

Wire bond die; 12 bonding pads **PCF2123U/10**



OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
PCF2123U/10						~~08-07-24~~ 11-04-06

Fig 33. Bare die outline PCF2123U/10 of PCF2123U/5GA/1 and PCF2123U/10AA/1 (for dimensions see Table 47)

Table 47. Dimensions of PCF2123U/10

Original dimensions are in mm.

Unit (mm)	A[1]	D[2]	E[2]	e_D	P_1[3]	P_2[4]	P_3[3]	P_4[4]
PCF2123U/5GA/1								
nom	0.20	1.492	1.449	1.296	0.09	0.081	0.09	0.081
PCF2123U/10AA/1								
nom	0.20	1.492	1.449	1.296	0.09	0.081	0.09	0.081

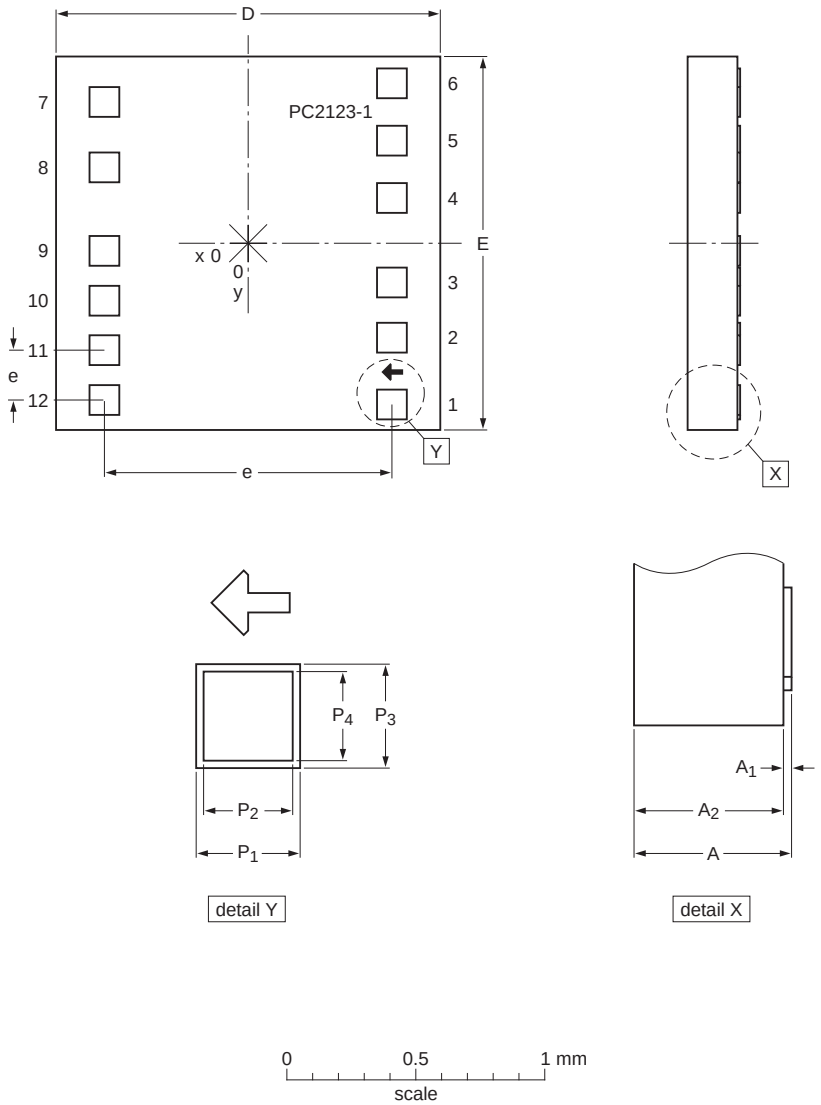
[1] Nominal die thickness. Compare with wafer thickness given in Table 51.

[2] Dimension includes saw lane.

[3] P_1 and P_3: pad size.

[4] P_2 and P_4: passivation opening.

WLCSP12: wafer level chip size package; 12 bumps. **PCF2123U/12**



pcf2123u_12_do

Outline version	References				European projection	Issue date
	IEC	JEDEC	JEITA			
PCF2123U/12	- - -	- - -	- - -			~~10-07-13~~ 11-04-06

Fig 34. Bare die outline PCF2123U/12 of PCF2123U/12AA/1 and PCF2123U/12HA/1 (for dimensions see Table 48)

Table 48. Dimensions of PCF2123U/12

Original dimensions are in mm.

Unit (mm)	A[1]	A_1	A_2[1]	D[2]	E[2]	e	P_1[3]	P_2[4]	P_3[3]	P_4[4]
PCF2123U/12AA										
max	-	0.018	-	-	-	1.296	-	0.084	-	0.084
nom	0.22	0.015	0.2	1.492	1.449	-	0.09	0.081	0.09	0.081
min	-	0.012	-	-	-	0.198	-	0.078	-	0.078
PCF2123U/12HA										
max	-	0.018	-	-	-	1.296	-	0.084	-	0.084
nom	0.17	0.015	0.15	1.492	1.449	-	0.09	0.081	0.09	0.081
min	-	0.012	-	-	-	0.198	-	0.078	-	0.078

[1] Nominal die thickness. Compare with wafer thickness given in Table 51.

[2] Dimension includes saw lane.

[3] P_1 and P_3: pad size.

[4] P_2 and P_4: bump size.

Table 49. Bump locations of all PCF2123U types

All x/y coordinates represent the position of the center of each pad with respect to the center (x/y = 0) of the chip; see Figure 33 and Figure 34.

Symbol	Bump	Coordinates	
		x	y
SDO	1	648.0	−575.0
SDI	2	648.0	−377.0
SCL	3	648.0	−179.0
CLKOE	4	648.0	171.2
CLKOUT	5	648.0	369.2
V_{DD}	6	648.0	625.7
OSCI	7	−648.0	639.0
OSCO	8	−648.0	421.9
TEST	9	−648.0	−25.9
$\overline{INT}$	10	−648.0	−223.9
CE	11	−648.0	−441.0
V_{SS}	12	−648.0	−639.0

Table 50. Alignment mark dimension and location of all PCF2123U types

Coordinates	
x	**y**
Location[1]	
693	−516.2
Dimension[2]	
16 μm	13 μm

[1] The x/y coordinates of the alignment mark location represent the position of the REF point (see Figure 35) with respect to the center (x/y = 0) of the chip; see Figure 33 and Figure 34.

[2] The x/y values of the dimensions represent the extensions of the alignment mark in direction of the coordinate axis (see Figure 35).

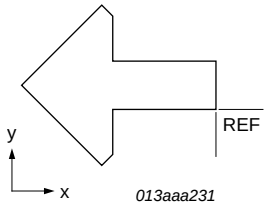
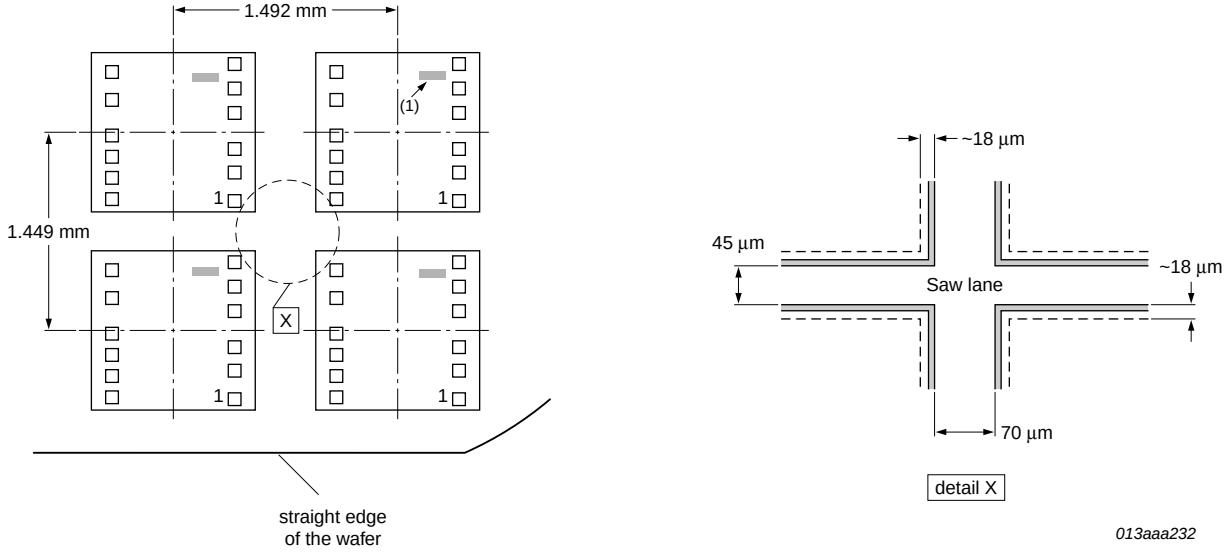


Fig 35. Alignment mark

18. Handling information

All input and output pins are protected against ElectroStatic Discharge (ESD) under normal handling. When handling Metal-Oxide Semiconductor (MOS) devices ensure that all normal precautions are taken as described in *JESD625-A*, *IEC 61340-5* or equivalent standards.

19. Packing information



(1) Die marking code.

Seal ring plus gap to active circuit ~18 µm.

Fig 36. PCF2123Ux wafer information

Table 51. PCF2123Ux wafer information

Type number	Wafer thickness (µm)	Wafer diameter	Marking of bad die
PCF2123U/5GA/1	687	6 inch	wafer mapping[1]
PCF2123U/10AA/1	200	6 inch	inking
PCF2123U/12AA/1	200	6 inch	wafer mapping[1]
PCF2123U/12HA/1	150	6 inch	inking

[1] Wafer mapping information will be distributed to customer's ftp server.

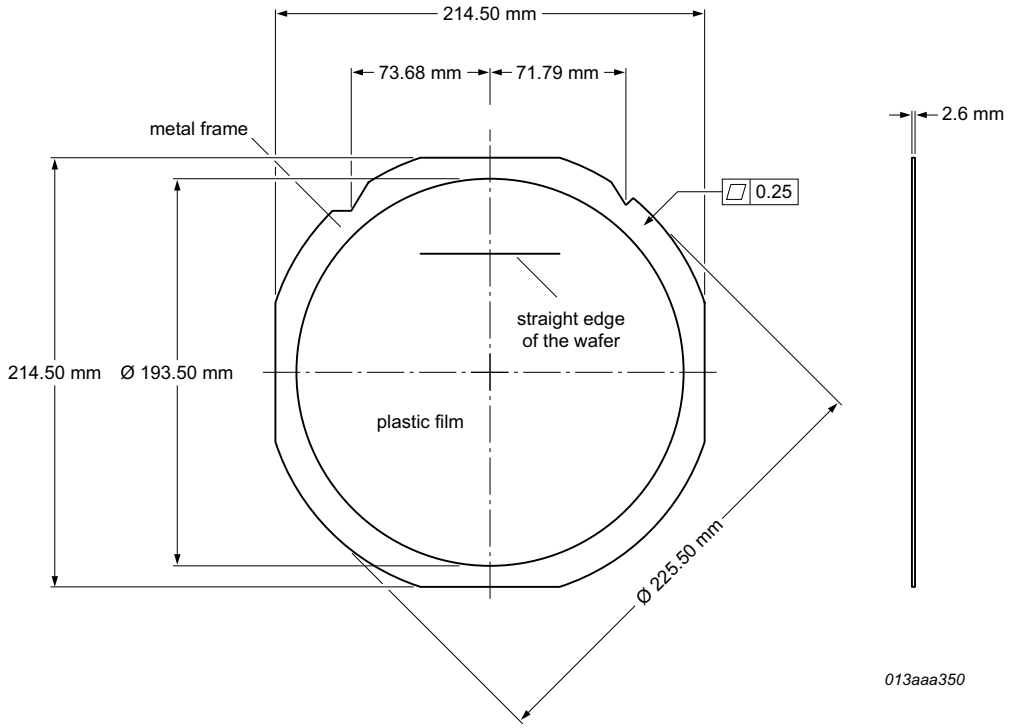


Fig 37. Film Frame Carrier (FFC) for 6 inch wafer (PCF2123U/10AA/1)

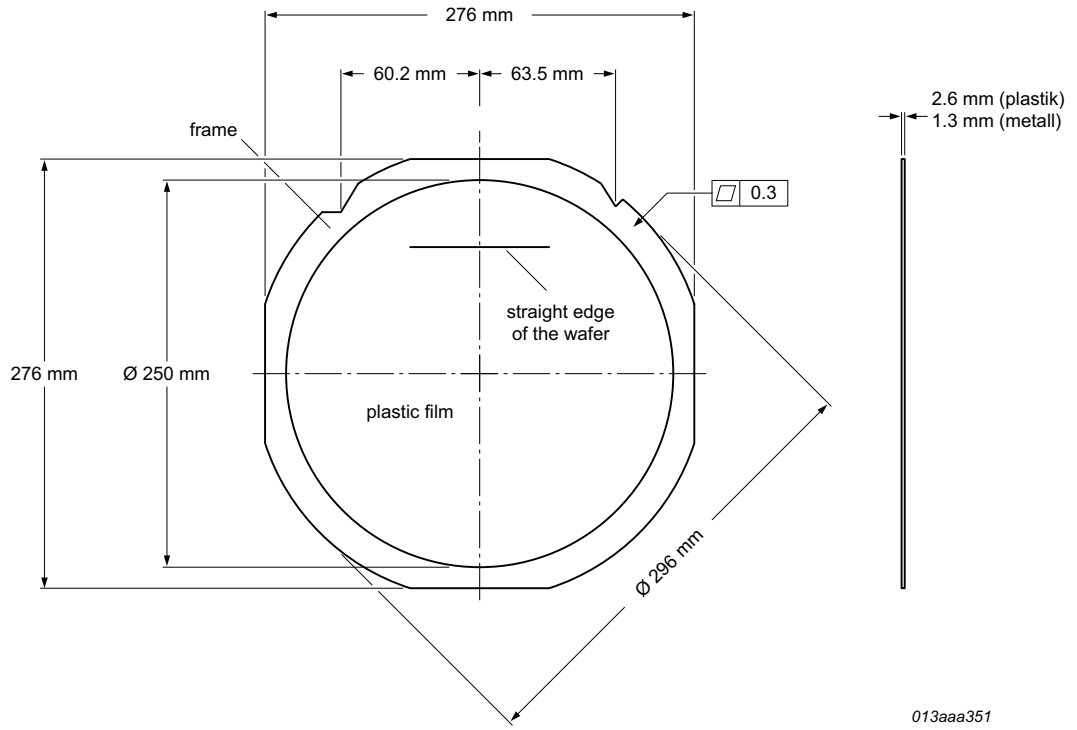


Fig 38. Film Frame Carrier (FFC) for 8 inch wafer (PCF2123U/12AA/1 and PCF2123U/12HA/1)

20. Soldering of SMD packages

This text provides a very brief insight into a complex technology. A more in-depth account of soldering ICs can be found in Application Note *AN10365 "Surface mount reflow soldering description"*.

20.1 Introduction to soldering

Soldering is one of the most common methods through which packages are attached to Printed Circuit Boards (PCBs), to form electrical circuits. The soldered joint provides both the mechanical and the electrical connection. There is no single soldering method that is ideal for all IC packages. Wave soldering is often preferred when through-hole and Surface Mount Devices (SMDs) are mixed on one printed wiring board; however, it is not suitable for fine pitch SMDs. Reflow soldering is ideal for the small pitches and high densities that come with increased miniaturization.

20.2 Wave and reflow soldering

Wave soldering is a joining technology in which the joints are made by solder coming from a standing wave of liquid solder. The wave soldering process is suitable for the following:

- Through-hole components
- Leaded or leadless SMDs, which are glued to the surface of the printed circuit board

Not all SMDs can be wave soldered. Packages with solder balls, and some leadless packages which have solder lands underneath the body, cannot be wave soldered. Also, leaded SMDs with leads having a pitch smaller than ~0.6 mm cannot be wave soldered, due to an increased probability of bridging.

The reflow soldering process involves applying solder paste to a board, followed by component placement and exposure to a temperature profile. Leaded packages, packages with solder balls, and leadless packages are all reflow solderable.

Key characteristics in both wave and reflow soldering are:

- Board specifications, including the board finish, solder masks and vias
- Package footprints, including solder thieves and orientation
- The moisture sensitivity level of the packages
- Package placement
- Inspection and repair
- Lead-free soldering versus SnPb soldering

20.3 Wave soldering

Key characteristics in wave soldering are:

- Process issues, such as application of adhesive and flux, clinching of leads, board transport, the solder wave parameters, and the time during which components are exposed to the wave
- Solder bath specifications, including temperature and impurities

20.4 Reflow soldering

Key characteristics in reflow soldering are:

- Lead-free versus SnPb soldering; note that a lead-free reflow process usually leads to higher minimum peak temperatures (see Figure 39) than a SnPb process, thus reducing the process window
- Solder paste printing issues including smearing, release, and adjusting the process window for a mix of large and small components on one board
- Reflow temperature profile; this profile includes preheat, reflow (in which the board is heated to the peak temperature) and cooling down. It is imperative that the peak temperature is high enough for the solder to make reliable solder joints (a solder paste characteristic). In addition, the peak temperature must be low enough that the packages and/or boards are not damaged. The peak temperature of the package depends on package thickness and volume and is classified in accordance with Table 52 and 53

Table 52. SnPb eutectic process (from J-STD-020D)

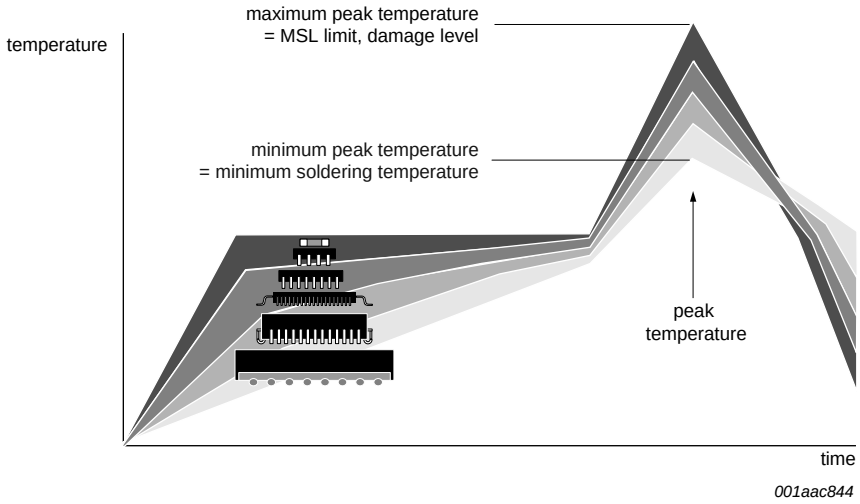
Package thickness (mm)	Package reflow temperature (°C)	
	Volume (mm^3)	
	< 350	≥ 350
< 2.5	235	220
≥ 2.5	220	220

Table 53. Lead-free process (from J-STD-020D)

Package thickness (mm)	Package reflow temperature (°C)		
	Volume (mm^3)		
	< 350	350 to 2000	> 2000
< 1.6	260	260	260
1.6 to 2.5	260	250	245
> 2.5	250	245	245

Moisture sensitivity precautions, as indicated on the packing, must be respected at all times.

Studies have shown that small packages reach higher temperatures during reflow soldering, see Figure 39.



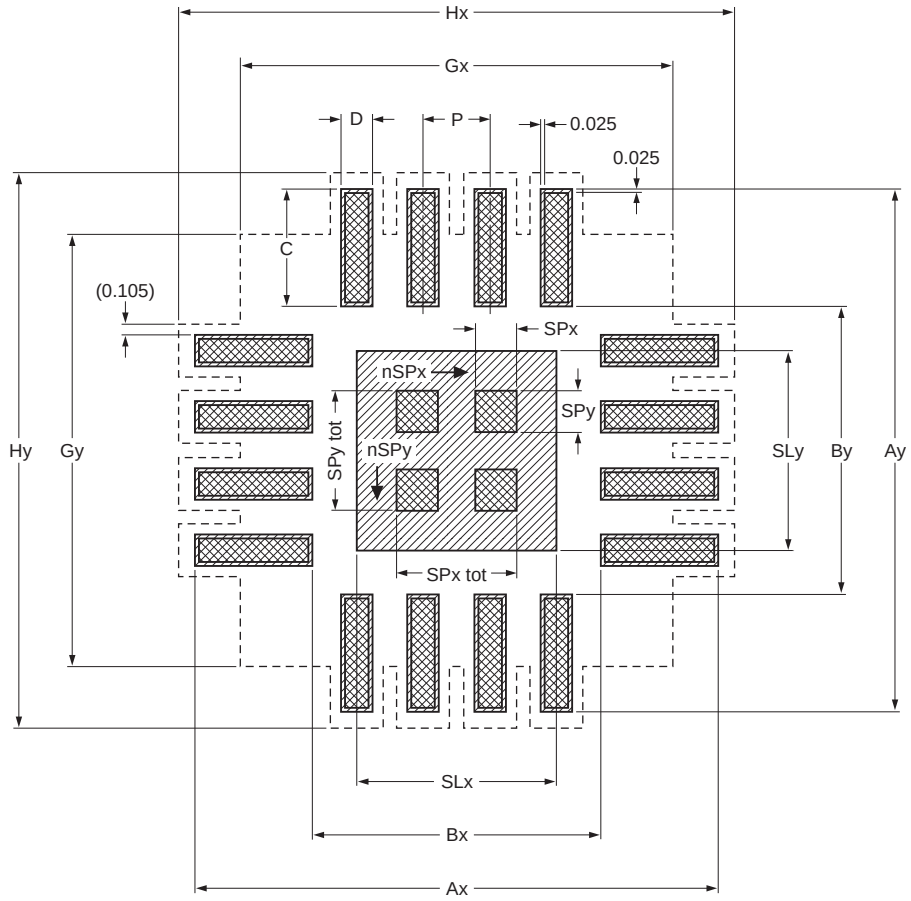
MSL: Moisture Sensitivity Level

Fig 39. Temperature profiles for large and small components

For further information on temperature profiles, refer to Application Note *AN10365 "Surface mount reflow soldering description"*.

21. Footprint information for reflow soldering

Footprint information for reflow soldering of HVQFN16 package **SOT758-1**



solder land

solder paste deposit

solder land plus solder paste

occupied area

nSPx	nSPy
2	2

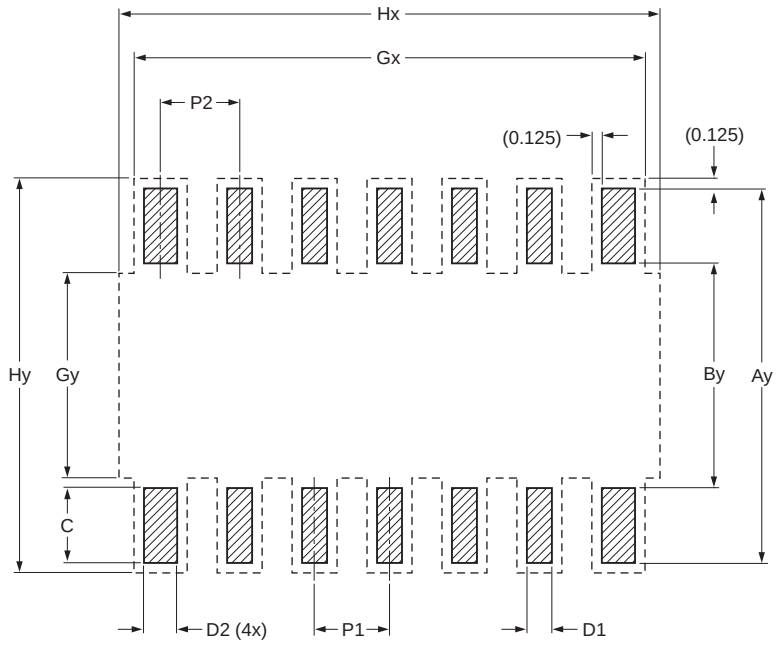
Dimensions in mm

P	Ax	Ay	Bx	By	C	D	SLx	SLy	SPx tot	SPy tot	SPx	SPy	Gx	Gy	Hx	Hy
0.50	4.00	4.00	2.20	2.20	0.90	0.24	1.50	1.50	0.90	0.90	0.30	0.30	3.30	3.30	4.25	4.25

Issue date ~~12-03-07~~ 12-03-08 *sot758-1_fr*

Fig 40. Footprint information for reflow soldering of SOT758-1 (HVQFN16) package of PCF2123BS/1

Footprint information for reflow soldering of TSSOP14 package **SOT402-1**



Generic footprint pattern
Refer to the package outline drawing for actual layout

solder land

occupied area

DIMENSIONS in mm

P1	P2	Ay	By	C	D1	D2	Gx	Gy	Hx	Hy
0.650	0.750	7.200	4.500	1.350	0.400	0.600	4.950	5.300	5.800	7.450

sot402-1_fr

Fig 41. Footprint information for reflow soldering of SOT402-1 (TSSOP14) package of PCF2123TS/1

22. Abbreviations

Table 54. Abbreviations

Acronym	Description
CMOS	Complementary Metal Oxide Semiconductor
BCD	Binary Coded Decimal
ESD	ElectroStatic Discharge
FFC	Film Frame Carrier
HBM	Human Body Model
LSB	Least Significant Bit
MM	Machine Model
MOS	Metal Oxide Semiconductor
MSB	Most Significant Bit
MSL	Moisture Sensitivity Level
PCB	Printed-Circuit Board
RTC	Real Time Clock
SMD	Surface Mount Device
SPI	Serial Peripheral Interface

23. References

[1] **AN10365 —** Surface mount reflow soldering description

[2] **AN10366 —** HVQFN application information

[3] **AN10706 —** Handling bare die

[4] **AN10853 —** Handling precautions of ESD sensitive devices

[5] **AN11247 —** Improved timekeeping accuracy with PCF85063, PCF8523 and PCF2123 using an external temperature sensor

[6] **IEC 60134 —** Rating systems for electronic tubes and valves and analogous semiconductor devices

[7] **IEC 61340-5 —** Protection of electronic devices from electrostatic phenomena

[8] **IPC/JEDEC J-STD-020D —** Moisture/Reflow Sensitivity Classification for Nonhermetic Solid State Surface Mount Devices

[9] **JESD22-A114 —** Electrostatic Discharge (ESD) Sensitivity Testing Human Body Model (HBM)

[10] **JESD78 —** IC Latch-Up Test

[11] **JESD625-A —** Requirements for Handling Electrostatic-Discharge-Sensitive (ESDS) Devices

[12] **SNV-FA-01-02 —** Marking Formats Integrated Circuits

[13] **UM10301 —** User Manual for NXP Real Time Clocks PCF85x3, PCA8565 and PCF2123, PCA2125

[14] **UM10569 —** Store and transport requirements

24. Revision history

Table 55. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
PCF2123 v.6	20130715	Product data sheet	-	PCF2123 v.5
Modifications:	• Changed spec value in Table 45 for SPI-bus active to 1.8 V • Added Section 8.9.1 • Adjusted raise and fall time values of the SPI-bus in Table 46 • Added ordering options in Table 2			
PCF2123 v.5	20110427	Product data sheet	-	PCF2123 v.4
PCF2123 v.4	20101222	Product data sheet	-	PCF2123 v.3
PCF2123 v.3	20101005	Product data sheet	-	PCF2123_2
PCF2123_2	20091204	Product data sheet	-	PCF2123_1
PCF2123_1	20081119	Product data sheet	-	-

25. Legal information

25.1 Data sheet status

Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL http://www.nxp.com.

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27. Tables

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