THE DATASHEET OF

PCA8885TS/Q900/1,1

PCA8885

Capacitive 8-channel touch and proximity sensor with auto-calibration and very low power consumption

Rev. 4 — 13 March 2014 Product data sheet

1. General description

The integrated circuit PCA8885 is a capacitive 8-channel touch and proximity sensor that uses a patented (EDISEN) method to detect a change in capacitance on remote sensing plates. Changes in the static capacitances (as opposed to dynamic capacitance changes) are automatically compensated using continuous auto-calibration. Remote sensing plates (for example, conductive foils) can be connected to the IC[1] using coaxial cable. The eight input channels operate independently of each other. There is also a built-in option for a matrix arrangement of the sensors: interrupt generation only when two channels are activated simultaneously, suppression of additional channel outputs when two channels are already active.

2. Features and benefits

- AEC-Q100 compliant for automotive applications
- Dynamic touch and proximity sensor with 8 sensor channels
- Support for matrix arrangement of sensors
- Sensing plates can be connected remotely
- Adjustable response time
- Adjustable sensitivity
  - Continuous auto-calibration
  - Digital processing method
  - Can cope with up to 6 mm of acrylic glass
- Direct and latching switch modes
- I^2C Fast-mode Plus (Fm+) compatible interface
  - Two I^2C-bus addresses
  - Cascading of two ICs possible
  - Interrupt signaling over I^2C-bus
- Interrupt output
- Large voltage operating range (V_{DD} = 2.5 V to 5.5 V)
- Sleep mode (I_{DD} < 100 nA)
- Low-power battery operation possible (I_{DD} ~ 10 μA)
- Operating temperature range (T_{amb} = −40 °C to +85 °C)

1. The definition of the abbreviations and acronyms used in this data sheet can be found in Section 23 on page 39.

3. Applications

- Replacing mechanical switches
- Hermetically sealed keys on a keyboard
- Switches for medical applications
- Switches for use in explosive environments
- Audio control: on/off, channel, volume
- Vandal proof switches
- Switches in or under the upholstery, leather, handles, mats, carpets, tiles, and glass
- Use of standard metal sanitary parts (for example a tap) as switch
- Portable communication and entertainment units
- White goods control panel

4. Ordering information

Table 1. Ordering information

Type number	Package		
	Name	Description	Version
PCA8885TS	TSSOP28	plastic small outline package; 28 leads; body width 4.4 mm	PCA8885TS

4.1 Ordering options

Table 2. Ordering options

Product type number	Orderable part number	Sales item (12NC)	Delivery form	IC revision
PCA8885TS/Q900/1	PCA8885TS/Q900/1,1	935297377118	tape and reel, 13 inch	1

5. Marking

Table 3. Marking codes

Product type number	Marking code
PCA8885TS/Q900/1	PCA8885TS

6. Block diagram

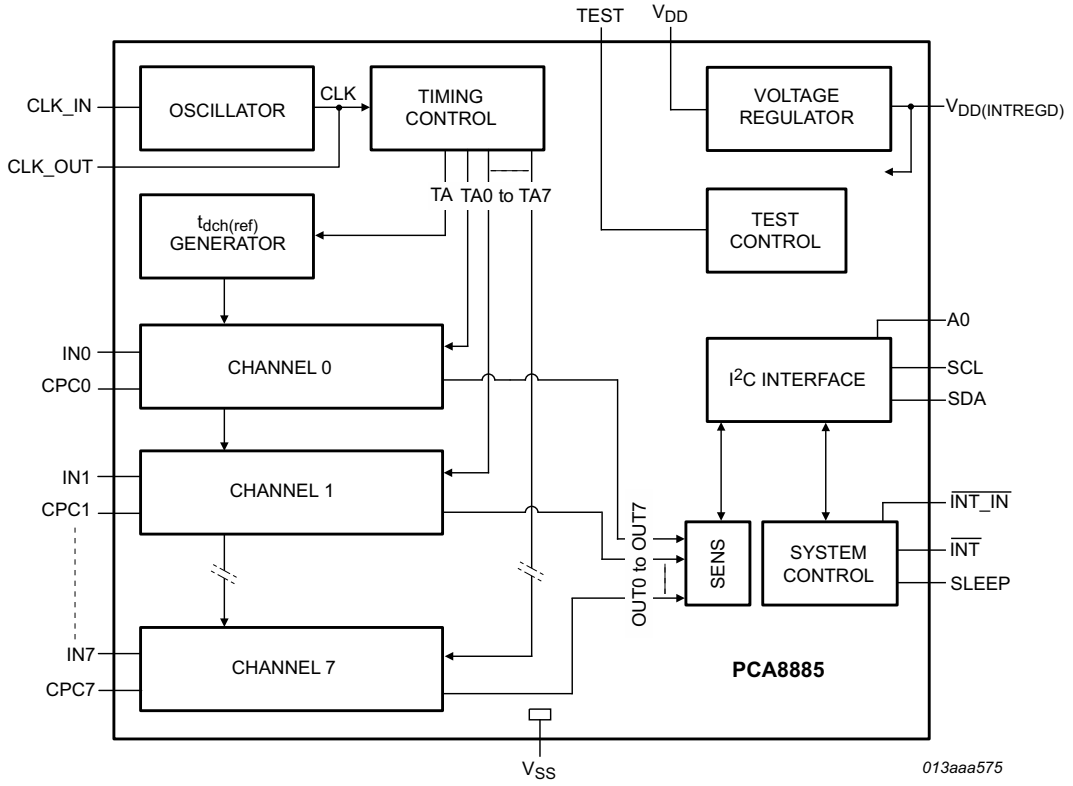
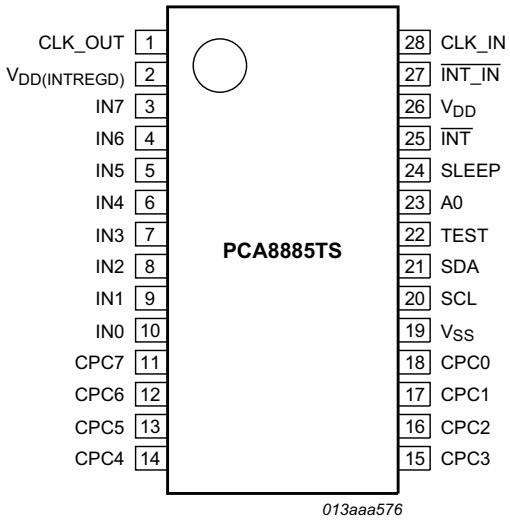


Fig 1. Block diagram of PCA8885

7. Pinning information

7.1 Pinning



Top view. For mechanical details, see Figure 26 on page 36.

Fig 2. Pin configuration for TSSOP28 (PCA8885TS)

7.2 Pin description

Table 4. Pin description

Input or input/output pins must always be at a defined level (V_{SS} or V_{DD}) unless otherwise specified.

Symbol	Pin	Type	Description
	PCA8885TS		
CLK_OUT	1	output	clock output for chip cascading and synchronization
$V_{DD(INTREGD)}$[1]	2	supply	internal regulated supply reference voltage
IN7 to IN0	3 to 10	analog input/output	sensor input, channel 0 to 7[2]
CPC7 to CPC0	11 to 18	analog input/output	reservoir capacitor, channel 0 to 7[2]
V_{SS}	19[3]	supply	ground supply voltage
SCL	20	input	serial clock line
SDA	21	input/output	serial data line
TEST	22	input	test pin; must be connected to V_{SS}
A0	23	input	I^2C subaddress LSB[4]
SLEEP	24	input	sleep mode; connect to V_{DD} to force the circuit into low-power sleep mode
$\overline{INT}$	25	output	interrupt output
V_{DD}	26	supply	supply voltage
$\overline{INT\_IN}$	27	input	interrupt input for chip cascading; connect to V_{DD} if not used
CLK_IN	28	input	clock input; for the secondary chip when the primary chip provides the clock signal

[1] The internal regulated supply voltage output must be decoupled with a decoupling capacitor to V_{SS}.

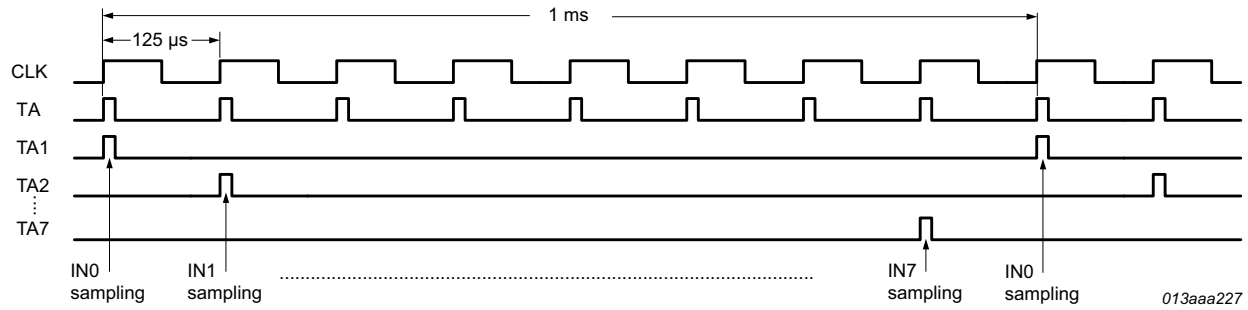
[2] If a channel is not used, the appropriate sensor input line has to be left open, the corresponding CPCn has to be connected to V_{SS} and the channel should be disabled in the MASK register (see Table 11 on page 15).

[3] The die paddle (exposed pad) is connected to V_{SS} and should be electrically isolated.

[4] Used to address two devices, for example: low address 3Ah, high address 3Bh.

8. Functional description

The sensing plates have to be connected to the sensor input pins IN0 to IN7. The discharge times (t_{dch}) on the sensor input pins, are compared to the discharge time ($t_{dch(ref)}$) of an internal RC timing element. The comparison is done sequentially for each sensor input pin. The RC timing circuits are periodically charged from $V_{DD(INTREGD)}$ and then discharged via a resistor to V_{SS}. The charge-discharge cycle for each channel is governed by the sampling rate (f_s). The channels are sampled sequentially, while the reference element is activated at the sampling point of each channel (see timing diagram in Figure 3).



For this example, the oscillator frequency and the clock division factor have been set to result in a 1 kHz sampling frequency.

Fig 3. Timing diagram of sensor sampling

When the voltage of an RC combination falls below the level V_{ref}, the appropriate comparator output changes. The logic following the comparators determines which comparator switched first. If the reference comparator switched first, then a pulse is given on CUP. If the sensor comparator switched first, then a pulse is given on CDN. Figure 4 illustrates the functional principle of the PCA8885.

The pulses control the charge on the external capacitors C_{CPC} on pins CPC0 to CPC7. Every time a pulse is given on CUP, the capacitor C_{CPC} is charged through a current source (I_{source}) from $V_{DD(INTREGD)}$ for a fixed time causing the voltage on C_{CPC} to rise by a small increment. Likewise when a pulse occurs on CDN, capacitor C_{CPC} is discharged through a current sink (I_{sink}) towards ground for a fixed time, causing the voltage on C_{CPC} to fall by a small decrement. The voltage on C_{CPC} controls an additional current sink (I_{CPC}) that causes the capacitance attached to the input pins IN[0:7] to be discharged more quickly. This arrangement constitutes a closed loop control system, that constantly tries to equalize the discharge time (t_{dch}) with the reference discharge time ($t_{dch(ref)}$). In the equilibrium state, the discharge times are nearly equal and the pulses alternate between CUP and CDN.

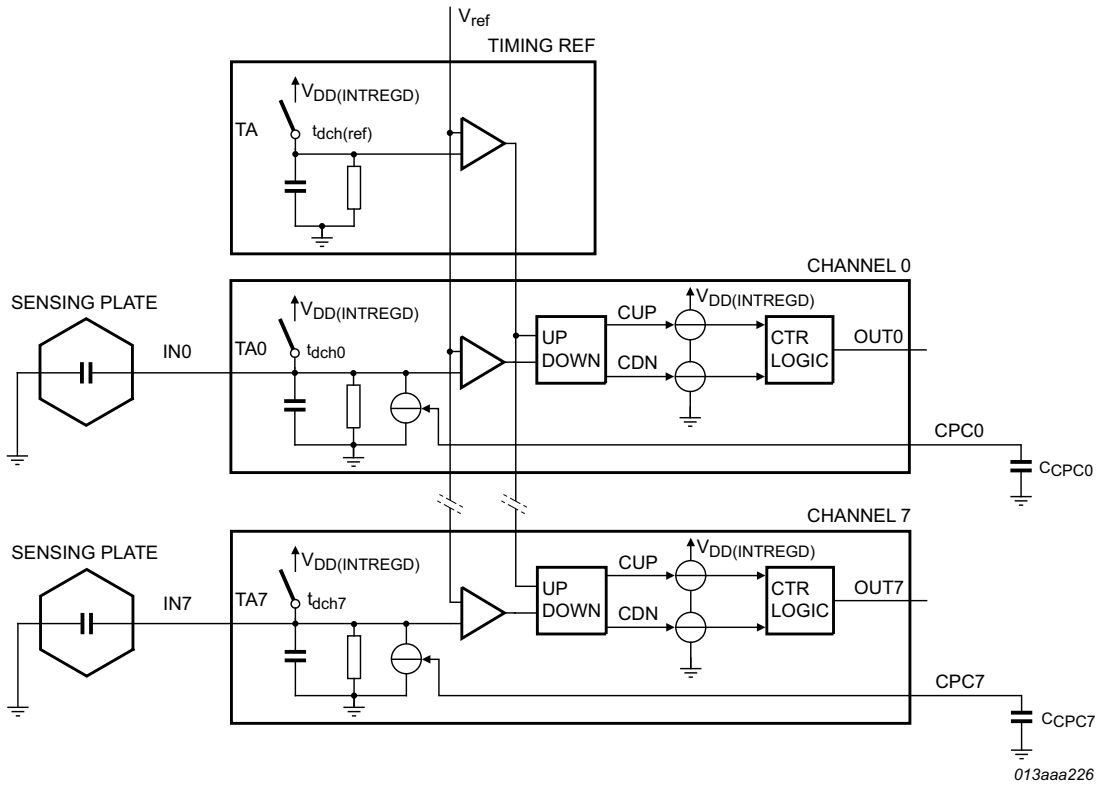


Fig 4. Functional diagram of sensor operation

The counter following this logic counts the pulses CUP or CDN respectively. The counter is reset every time the pulse sequence changes from CUP to CDN or the other way round. The outputs OUT0 to OUT7 are only activated when 64 consecutive pulses occurred on CUP. Low-level interference or slow changes in the input capacitance do not cause the output to switch.

Various measures, such as asymmetrical charge and discharge steps, are taken to ensure that the output switches off correctly. A special start-up circuit ensures that the device reaches equilibrium quickly when the supply is attached.

The sampling rate (f_s) is derived from the internally generated oscillator frequency. The oscillator frequency can be adjusted within a specified range by programming the CLKREG register (see Table 10 on page 14).

The status of the output signals OUT0 to OUT7 is stored in the SENS register (see Table 9 on page 13). An interrupt is generated on changes of the sensor states.

9. Commands

The operation of the PCA8885 can be controlled by 12 commands and 4 configuration- and status-registers (see Section 10 on page 10). Several configuration settings can be programmed using single commands without associated data transfer. The configuration register can however also be written using the write-config command. The clock and mask registers can only be programmed using the write-clock and write-mask commands.

9.1 Command overview

Table 5. Commands of PCA8885

Command	Operation code	Description	Transfer type	Reference
soft-reset	00000000	brings chip to reset state	command	Section 9.2, Section 10.2.2.2
clear-$\overline{INT}$	00000011	deactivates interrupt generation on pin $\overline{INT}$	command	Section 10.2.2.1
sleep	00000101	enter sleep mode	command	Section 9.3
wake-up	00000110	enter active mode	command	
write-config	00110000	write configuration register	write 1 byte	Section 10.2
read-config	00110011	read configuration register	read 1 byte	
write-clock	00110101	write clock setting register	write 1 byte	Section 10.4
read-clock	00110110	read clock setting register	read 1 byte	
write-mask	00111001	write the mask register	write 1 byte	Section 10.5
read-mask	00111010	read the mask register	read 1 byte	
int-over-I^2C	00111100	put the device in int-over-I^2C mode	command	Section 10.2.2.1
read-sensor	-	read sensor state register and clears the $\overline{INT}$ line	direct read	Section 9.4, Section 10.2.2.1

9.2 Command: soft-reset

Reset takes place during power-on of the circuit. There is no external hardware reset input.

During operation, the device can be reset using the soft-reset command. The sensor channels and all registers are reset to the default values and the int-over-I^2C mode is terminated. It does not affect the state of the analog section except for those functions that are controlled by configuration bits.

9.3 Commands: Sleep and wake-up

Sleep mode is implemented to save power during periods where no sensor activity is expected or supported.

In sleep mode, most of the circuit parts are put in power-down mode, in particular all analog blocks consuming static and dynamic power. This includes the oscillator, thus no internal activity remains. Also the voltage regulator is powered down, to reduce its standalone power consumption.

During sleep mode, the register configuration is maintained and the device remains responsive to I^2C commands. The charges in the CPC capacitors however cannot be guaranteed, as there is no limitation on the duration of the sleep mode. Therefore the analog part has to perform a normal start-up phase, including the fast start procedure for the CPC capacitor charging.

Sleep mode is entered when the sleep command is received from the system controller or when the SLEEP pin is set to HIGH. Resume is done by the wake-up command, or by setting the SLEEP pin to LOW.

The hardware sleep mechanism using the SLEEP pin and the software sleep mechanism using the sleep or wake-up commands are independent of each other:

- If the device was put to sleep using the sleep command, a wake-up command resumes the operation. It cannot be resumed by activating the SLEEP pin.
- If the device was put to sleep by setting pin SLEEP to HIGH, then pin SLEEP must be set to LOW to resume operation. It cannot be resumed with the wake-up command.

9.4 Command: read-sensor

The read-sensor command is the main transaction to read the actual state information of the sensor state register SENS.

If the R/$\overline{W}$ bit (LSB of the I^2C slave address byte, see Table 12 on page 19) is set logic 1 the PCA8885 regards the transaction as the read-sensor command. The read-sensor command transaction supports a repeated reading of the SENS register (see Section 10.3 on page 13). When two circuits are used in a cascaded configuration, they alternately return their SENS register content in a single transaction

The protocols for the repeated read mode and the alternating read mode are described in Section 13.7 on page 20.

10. Registers

The PCA8885 has four registers storing the configuration and the status information of the device.

10.1 Register overview

Table 6. Register overview

The bit position labeled as x is not relevant; if read, it can be either logic 0 or logic 1.

Register name	Bit								Default value
	7	6	5	4	3	2	1	0	
CONFIG	OPM[1:0]		SWM	KM[1:0]		VROF	INTM	MSKMODE	00000000
SENS	CH[7:0]								00000000
CLKREG	CLO	CLI	x	FRQC[1:0]		FRQF[2:0]			00x01100
MASK	MSK[7:0]								11111111

10.2 Register: CONFIG

Table 7. CONFIG - configuration register bit description

Bit	Symbol	Value	Description	Reference
7 to 6	OPM[1:0]		main operation mode	Section 10.2.1.1
		00[1]	stand-alone device	
		01	secondary-chip in a cascade	
		10	primary-chip in a cascade	
		11	unused	
5	SWM		switching mode	Section 10.2.1.2
		0[1]	direct switching mode: sensor release clears the corresponding bit in the SENS register	
		1	latching mode: reading SENS register clears bits in the SENS register	
4 to 3	KM[1:0]		key-press mode	Section 10.2.1.3
		00[1]	N-key mode: each sensor activity is reflected in the SENS register	
		01	2-key mode: only first two keys are visible in the SENS register	
		10	1-key mode: only first key-press is visible in the SENS register	
		11	unused	

Table 7. CONFIG - configuration register bit description *...continued*

Bit	Symbol	Value	Description	Reference
2	VROF		voltage regulation	Section 11
		0[1]	voltage regulation on	
		1	voltage regulation off	
1	INTM		interrupt generation mode	Section 10.2.2
		0[1]	an interrupt is generated by each bit changed in the SENS register (press and release)	
		1	an interrupt is generated by each bit set in the SENS register (press only)	
0	MSKMODE		channel masking mode	Section 10.5.1
		0[1]	normal power: masked out channels remain operational	
		1	low power: masked out channels are powered down	

[1] Default value.

All bits in this register can be written and read with the write-config and read-config commands.

10.2.1 Operating modes

10.2.1.1 Main operating modes

The PCA8885 can operate in three operating modes: as a stand-alone device or in a cascade as a primary-chip or a secondary-chip (see Table 8).

Table 8. Main operating modes

	Main operating modes		
Conditions of	**Stand-alone[1]**	**Primary-chip**	**Secondary-chip**
clock source	internal oscillator	internal oscillator	clock input
oscillator	enabled	enabled	disabled
clock output pin CLK_OUT	disabled	enabled	disabled
clock input pin CLK_IN	disabled	disabled	enabled

[1] Default operating mode after power-on.

The operating modes are implemented to support the application of two PCA8885 in the system (see Section 13.8 on page 21).

10.2.1.2 Switching modes

There is a one to one relationship between the channels IN[0:7] and the bits in the SENS register. The indication of the switching status of each channel is controlled by the two switching modes supported:

Direct mode — In direct mode, the sensor state is directly reflected in the SENS register. When the sensor is activated, the corresponding bit in the SENS register is immediately set logic 1. When the sensor is released, the bit is cleared (set logic 0) again. The bits are even cleared if the SENS register has not yet been read by the system controller.

Latching mode — In latching mode, every activated sensor sets the corresponding bit in the SENS register logic 1. When the sensor is released, the SENS register is unaffected. Reading the SENS register clears (set logic 0) those bits, whose sensor is not activated anymore.

After reset, the PCA8885 is set to direct switching mode.

10.2.1.3 Key-press modes

There are three key-press modes implemented in the PCA8885: N-key, 1-key, and 2-key mode.

N-key mode — In N-key mode, each sensor activity is reflected in register SENS according to the configured switching mode. The N-key mode is the default key-press mode after reset.

1-key mode — In 1-key mode, only the first sensor activation sets the corresponding bit in register SENS. All further activations of the other sensors are suppressed at the SENS register boundary. In this way, sensors in a keypad are masked out, which are activated accidentally because they are arranged next to the activated sensor.

The 1-key mode supports sensor matrix arrangements with two PCA8885, where one chip is attached to the columns and one to the rows (primary-chip and secondary-chip). Sensor activation sets 1 bit for the column and 1 bit for the row in the SENS register of the appropriate chip. Each activation of a sensor raises an interrupt. The system controller must handle the situation where the $\overline{\text{INT}}$ is raised before the second sensor in the matrix has been activated.

2-key mode — In 2-key mode, only the two first sensor activations set the corresponding bits in register SENS. All further activations of the other sensors are suppressed at the SENS register boundary. This mode supports in particular the matrix arrangement of sensors using only one PCA8885, as illustrated in Figure 25 on page 33. In this way, sensors in a matrix are masked out, which are activated accidentally because they are arranged next to the intended sensors. This mode properly handles a delay in sensor activation due to unequal sensor capacitance or area (non-centric sensor touching, and so on) as long as the intended sensors react before sensors which are activated accidentally. In 2-key mode, the $\overline{\text{INT}}$ output is only activated after 2 bits have been set in the SENS register.

10.2.2 Interrupt generation

The PCA8885 provides two mechanisms to inform the system controller that a sensor activity has been detected.

10.2.2.1 Interrupt output $\overline{\text{INT}}$

The PCA8885 has an interrupt output, $\overline{\text{INT}}$, to flag to the system controller that a capacitive event has been detected. The controller can then fetch the sensor state by reading the SENS register over the I^2C-bus.

The interrupt generation is controlled by the INTM bit in the CONFIG register (see Table 7 on page 10).

- If INTM is logic 0 (default), then the change (set or clear) of each bit in register SENS activates the $\overline{INT}$ output.
- If INTM is logic 1, then only sensor press events, resulting in bits being set logic 1 in the SENS register, activate the $\overline{INT}$ output. Sensor release events, which cause the corresponding bit in SENS to be cleared (set logic 0), do not activate the $\overline{INT}$ output.

In 2-key mode, the $\overline{INT}$ output is only activated after 2 bits have been set in the SENS register.

The interrupt is automatically cleared when the system controller reads the SENS register. Alternatively the $\overline{INT}$ can be cleared by using the clear-$\overline{INT}$ command, without reading the actual sensor state.

10.2.2.2 Interrupt over the I²C-bus

In applications where the sensing plates are remote from the microcontroller, the interrupt line can be saved by enabling the interrupt over I²C-bus.

The PCA8885 provides the feature of interrupt over the I²C-bus. The PCA8885 then behaves like an I²C master with restricted functionality. The interrupt is signaled by setting a START condition immediately followed by a STOP condition. It is illustrated in Figure 5. No further I²C master capabilities are supported.

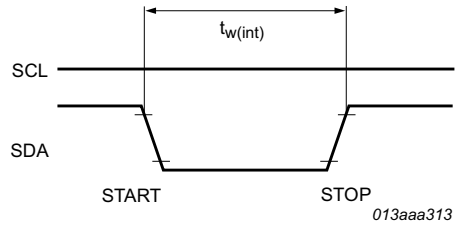


Fig 5. Interrupt over the I²C-bus

The system controller has to detect the START-STOP condition and react accordingly.

The interrupt over the I²C-bus can be enabled with the int-over-I²C command and disabled with the soft-reset command.

In interrupt over the I²C-bus mode, the functionality of the $\overline{INT}$ output continues to work as described in Section 10.2.2.1.

10.3 Register: SENS

Table 9. SENS - sensor state register bit description

Bit	Symbol	Value	Description
7 to 0	CH[7:0]	00000000[1] to 11111111	sensor state of the respective channels IN7 to IN0

[1] Default value.

All bits in this register are read-only and can be read with the read-sensor command (see Section 9.4).

10.4 Register: CLKREG

Table 10. CLKREG - clock setting register bit description

Bit	Symbol	Value	Description
7	CLO		CLK_OUT switch
		0[1]	CLK_OUT disabled (unless IC is in primary-chip mode)
		1	CLK_OUT enabled
6	CLI		CLK_IN switch
		0[1]	CLK_IN disabled (unless IC is in secondary-chip mode)
		1	CLK_IN enabled, internal oscillator is powered down
5	-	-[2]	unused
4 to 3	FRQC[1:0]		clock frequency, coarse setting
		00	$f_{clk} = f_{osc} / 64$
		01[1]	$f_{clk} = f_{osc} / 16$
		10	$f_{clk} = f_{osc} / 4$
		11	$f_{clk} = f_{osc}$
2 to 0	FRQF[2:0]		oscillator tuning
		000	$f_{osc} = 0.5 \times f_{osc(nom)}$
		001	$f_{osc} = 0.625 \times f_{osc(nom)}$
		010	$f_{osc} = 0.75 \times f_{osc(nom)}$
		011	$f_{osc} = 0.875 \times f_{osc(nom)}$
		100[1]	$f_{osc} = 1 \times f_{osc(nom)}$
		101	$f_{osc} = 1.25 \times f_{osc(nom)}$
		110	$f_{osc} = 1.5 \times f_{osc(nom)}$
		111	$f_{osc} = 1.75 \times f_{osc(nom)}$

[1] Default value.

[2] Should always be written with logic 0 and if read, it can be either logic 0 or logic 1.

All bits in this register can be written and read with the write-clock and read-clock commands.

10.4.1 Clock generation and frequency adjustment

The PCA8885 contains an integrated oscillator as main clock source. With the values of FRQF[2:0], the oscillator frequency can be tuned (see Equation 1).

$$f_{osc} = m \times f_{osc(nom)} \quad (1)$$

The values of m can be varied in the range 0.5 ≤ m ≤ 1.75, where m = 1.0 corresponds to the default value of FRQF[2:0] = 100.

The internal clock frequency (f_{clk}) is derived from the oscillator frequency with Equation 2:

$$f_{clk} = f_{osc} / n \quad (2)$$

where the values for n are 1, 4, 16, or 64 and can be selected with FRQC[1:0]. The sensor sampling frequency (f_s) is derived from the internal clock frequency with Equation 3:

$$f_s = f_{clk} / 8 \quad (3)$$

The eight sensors are sampled sequentially, which results in a default sensor sampling rate f_s.

In secondary-chip mode, the internal clock generator is stopped, and the circuit is clocked from the CLK_IN input pin.

The tuning of the oscillator frequency and the programmable clock divider (see Figure 6) allows changing the sensor sampling rate, the adjustment of the reaction time and the power consumption of the PCA8885 over a wide range.

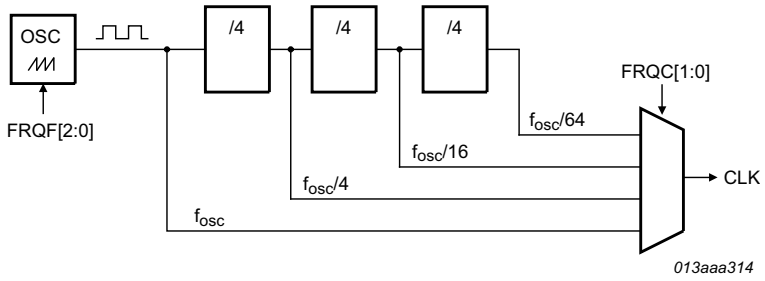


Fig 6. Oscillator block diagram

10.5 Register: MASK

Table 11. MASK - channel enable mask register bit description

Bit	Symbol	Value	Description
7 to 0	MSK[7:0]	00000000 to 11111111[1]	enable or disable the respective sensor channels IN0 to IN7
		0	sensor channel is disabled
		1	sensor channel is enabled

[1] Default value.

All bits in this register can be written and read with the write-mask and read-mask commands.

10.5.1 Channel masking

The channel masking register MASK allows individual sensor channels to be enabled or disabled for particular applications or certain modes (for example only the on/off sensor should be active).

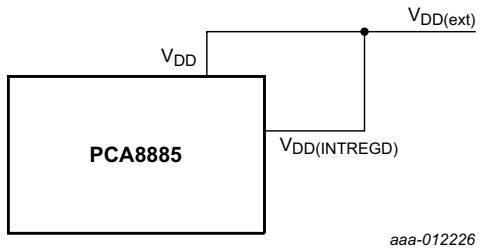
- When bit MSKMODE in register CONFIG (see Table 7) is set logic 0, then the disabled channels are continuously sampled, but switching events are not reflected in register SENS and do not cause interrupts.
- When bit MSKMODE in register CONFIG (see Table 7) is set logic 1, only channels which are enabled are sampled. Reducing the number of sampled channels also reduces the power consumption.

When a channel becomes newly enabled, the fast start-up method (see Section 12) is used to reach the functional state quickly.

11. Power architecture

The circuit has an integrated voltage regulator, supplied by pin V_{DD}. The regulator provides an internal $V_{DD(INTREGD)}$ supply of nominally 2.8 V.

If a stable and noise free external supply voltage with 2.5 V < $V_{DD(ext)}$ < 3.3 V is available in the system, $V_{DD(INTREGD)}$ can be provided from an external source (see Figure 7). In this case V_{DD} and $V_{DD(INTREGD)}$ must both be connected to $V_{DD(ext)}$. To reduce the current consumption, the internal voltage regulator should be shut down by setting bit VROF logic 1 (see Table 7 on page 10).



2.5 V < $V_{DD(ext)}$ < 3.3 V.

Fig 7. Connection of $V_{DD(ext)}$

While the analog part of the circuit is powered from $V_{DD(INTREGD)}$, the I^2C interface and the registers are powered from V_{DD}. Therefore the I^2C interface remains accessible in sleep mode, and the register values are maintained when $V_{DD(INTREGD)}$ is powered off.

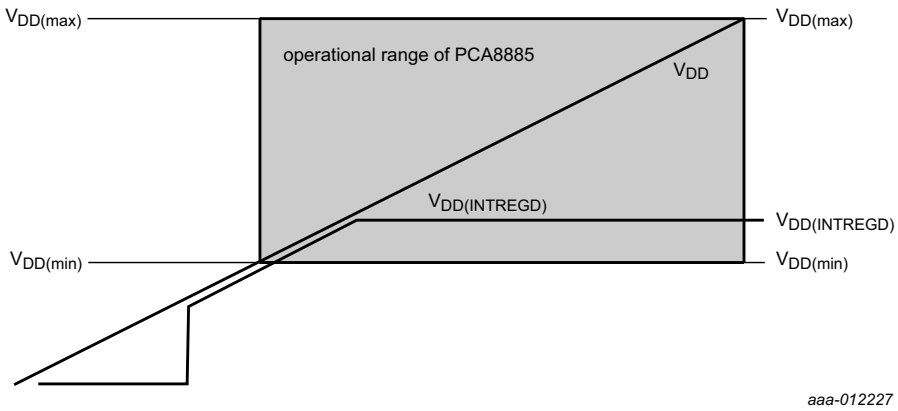


Fig 8. Integrated voltage regulator behavior

Figure 8 illustrates the behavior of the integrated voltage regulator. The gray area covers the operational range of the PCA8885. The analog part of the circuit and the switch logic is powered from $V_{DD(INTREGD)}$. The I^2C interface and the registers are powered from V_{DD}. Therefore the I^2C interface remains accessible in sleep mode, and the register values are maintained when $V_{DD(INTREGD)}$ is powered off.

12. Start-up procedure

After power-on the registers in the V_{DD} domain are reset, which includes the VROF bit controlling the voltage regulator. The regulator is therefore enabled, and the $V_{DD(INTREGD)}$ domain is powered on. As soon as a sufficient $V_{DD(INTREGD)}$ level is reached, the Power-On Reset (POR) is released.

After release of the POR in the $V_{DD(INTREGD)}$ domain, the circuit starts with the sensor sampling in the fast start mode (increased charge-pump currents quickly charge the CPC capacitors close to their target value). As soon as the capacitor voltages are close to the target value, the fast start phase is terminated, and the capacitors are charged in fine steps to the final value. When this state is reached, the logic enables the up and down counters, and the sensors are operational.

This start-up mechanism is executed independently for each channel.

13. Characteristics of the I^2C-bus

The PCA8885 has an I^2C serial interface which operates as a slave receiver or transmitter. SDA and SCL are the data I/O and clock lines for the serial I^2C Interface. SDA is used as an input or as an open-drain output. SDA is actively pulled LOW and is passively held HIGH by the external pull-up resistor on the I^2C-bus.

In order to provide high link robustness, the I^2C interface of the PCA8885 is Fast-mode compatible and provides a robust addressing and command scheme.

13.1 Bit transfer

One data bit is transferred during each clock pulse. The data on the SDA line must remain stable during the HIGH period of the clock pulse as changes in the data line at this time are interpreted as a control signal (see Figure 9).

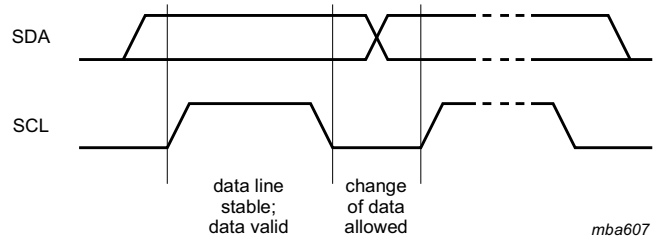


Fig 9. Bit transfer

13.1.1 START and STOP conditions

Both data and clock lines remain HIGH when the bus is not busy.

A HIGH-to-LOW change of the data line, while the clock is HIGH, is defined as the START condition (S).

A LOW-to-HIGH change of the data line, while the clock is HIGH, is defined as the STOP condition (P).

The START and STOP conditions are shown in Figure 10.

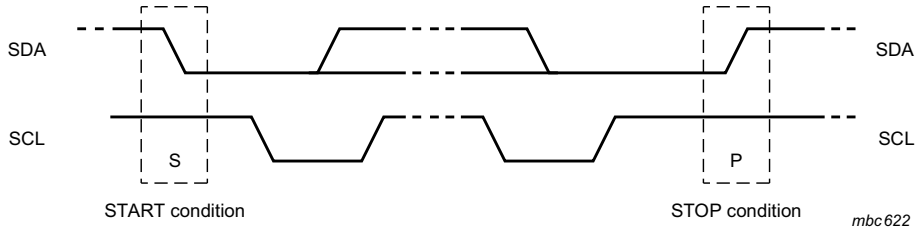


Fig 10. Definition of START and STOP conditions

13.2 System configuration

A device generating a message is a transmitter; a device receiving a message is the receiver. The device that controls the message is the master; and the devices which are controlled by the master are the slaves. The system configuration is shown in Figure 11.

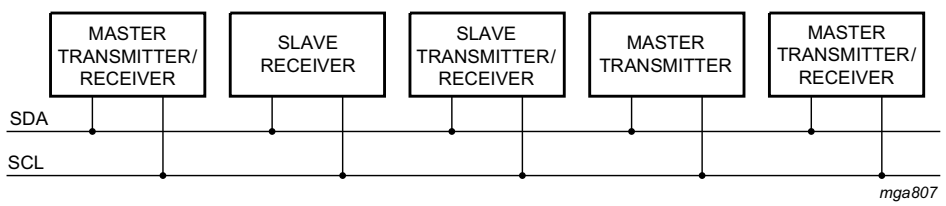


Fig 11. System configuration

13.3 Acknowledge

The number of data bytes transferred between the START and STOP conditions from transmitter to receiver is unlimited. Each byte of 8 bits is followed by an acknowledge cycle.

- A slave receiver, which is addressed, must generate an acknowledge after the reception of each byte.
- A master receiver must generate an acknowledge after the reception of each byte that has been clocked out of the slave transmitter.
- The device that acknowledges must pull-down the SDA line during the acknowledge clock pulse, so that the SDA line is stable LOW during the HIGH period of the acknowledge related clock pulse (set-up and hold times must be considered).
- A master receiver must signal an end of data to the transmitter by not generating an acknowledge on the last byte that has been clocked out of the slave. In this event, the transmitter must leave the data line HIGH to enable the master to generate a STOP condition.

Acknowledgement on the I^{2}C-bus is shown in Figure 12.

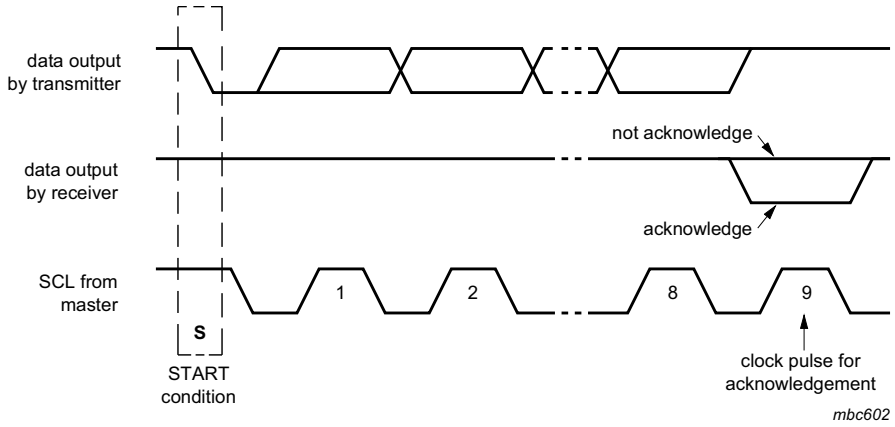


Fig 12. Acknowledgement on the I^{2}C-bus

13.4 I^{2}C-bus subaddress

Device selection depends on the I^{2}C-bus slave address, on the transferred command data, and on the hardware subaddress.

Two I^{2}C-bus slave addresses are used to address the PCA8885 (see Table 12).

Table 12. I^{2}C slave address byte

	Slave address							
Bit	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
	MSB							**LSB**
Slave address	0	1	0	0	0	0	A0	R/$\overline{W}$

The least significant bit of the slave address is bit R/$\overline{W}$ (see Table 13).

Table 13. R/$\overline{W}$-bit description

R/$\overline{W}$	Description
0	write data
1	read data

Bit 1 of the slave address is defined by connecting input A0 to either V_{SS} (logic 0) or V_{DD} (logic 1). Therefore, two instances of PCA8885 can be distinguished on the same I²C-bus.

13.5 I²C-bus protocol

The I²C-bus protocol is shown in Figure 13. The sequence is initiated with a START condition (S) from the I²C-bus master which is followed by the slave address.

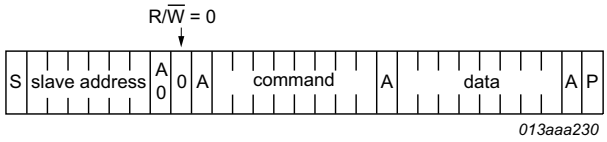


Fig 13. I²C-bus protocol write mode

After acknowledgement, a command is sent, and after a further acknowledge a data byte is transmitted. After the last data byte, the I²C-bus master issues a STOP condition (P). Alternatively a START may be asserted to RESTART an I²C-bus access.

13.6 Fast-mode Plus (Fm+) support

The Fast-mode Plus specification is supported. Besides providing a high transmission speed, the main characteristic of Fast-mode Plus is the increased drive strength, allowing lower impedance buses to be driven, and therefore less noise sensitive. Details on the Fast-mode Plus specification are given in Ref. 14 “UM10204”.

13.7 Reading sensor data

The PCA8885 supports direct reading of the sensor state from the SENS register. If - after sending the address - the R/$\overline{W}$ bit is immediately set to logic 1 without sending a command, the circuit recognizes that it must immediately return the content of the SENS register (see Figure 14)

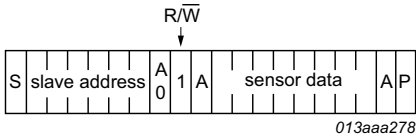


Fig 14. Reading sensor data

When the transaction, after reading the SENS register, is not terminated with a STOP bit, the PCA8885 repeatedly sends the content of SENS again. This provides a facility to observe the sensor activity continuously. This transaction is illustrated in Figure 15.

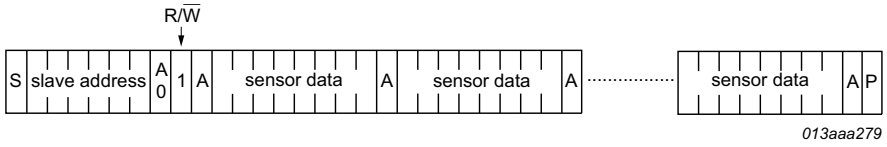


Fig 15. Continuously reading sensor data

Using two PCA8885 in a cascade (see Section 13.8), one has to be the primary-chip and the other the secondary-chip. When the direct read transaction is executed in a cascaded configuration, the primary-chip transmits its SENS content register immediately after the address byte, followed by the secondary-chip transmitting its SENS register content.

If the transaction - after reading the two SENS registers - is not terminated with a STOP bit, the primary-chip and the secondary-chip continue sending the content of the SENS registers alternately. Such a transaction is illustrated in Figure 16.

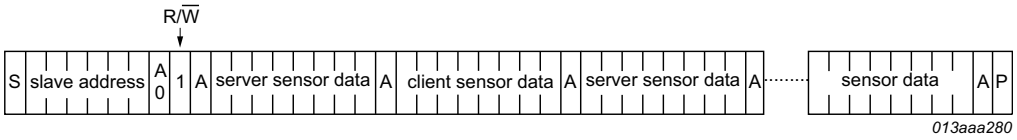


Fig 16. Reading sensor data, alternately from primary-chip and secondary-chip

It must be noted, that for this alternate data transfer only one PCA8885 has to be addressed. By definition the primary-chip must be addressed (A0 bit in the address set to logic 0). In this particular case, the secondary-chip reacts on the address of the primary-chip. For all other transactions targeting the secondary-chip, it must be properly addressed with A0 set to logic 1.

13.8 Device cascading

Two PCA8885 devices can be connected to the same I^2C-bus, which facilitates up to 8×8 keypads.

The device provides the following features to guarantee robust operation and to simplify the system design using two devices:

- The 7-bit I^2C address consists of 6 fixed bits and 1 selectable bit. The level externally applied to pin A0 (V_{DD} or V_{SS}) defines the LSB of the I^2C slave address. In this way, two PCA8885 can be addressed on the same bus without the need for different hard coded I^2C addresses.
- The sensor activity can be synchronized, so that interference between the sensors of the different chips is avoided. One chip is considered to be the primary-chip. It provides the sample clock on pin CLK_OUT. The other chip is considered to be the secondary-chip. It uses the clock provided by the primary-chip instead of the internal clock. The primary-chip samples the sensors on the rising edge of the internal sample clock. The CLK_IN signal is inverted to derive the sample clock in the secondary-chip. Therefore the secondary-chip samples its sensors on the negative edge of the sample clock of the primary-chip. In this way, no simultaneous sensor sampling occurs.

Primary-chip or secondary-chip modes are enabled by programming the configuration register (see Table 7 on page 10).

- The interrupt signal can be cascaded. The $\overline{INT}$ output of the primary-chip can be connected to the $\overline{INT\_IN}$ input of the secondary-chip. The $\overline{INT}$ output of the secondary-chip is then an OR'ed combination of the two interrupts.
- If two devices are cascaded and the int-over-I^2C mode is desired, then it is sufficient to put the secondary-chip in int-over-I^2C mode. The primary-chip still signals an interrupt over the INT output to the $\overline{INT\_IN}$ input of the secondary-chip.

Figure 25 on page 33 illustrates a typical example of an application using two PCA8885 circuits.

14. Internal circuitry

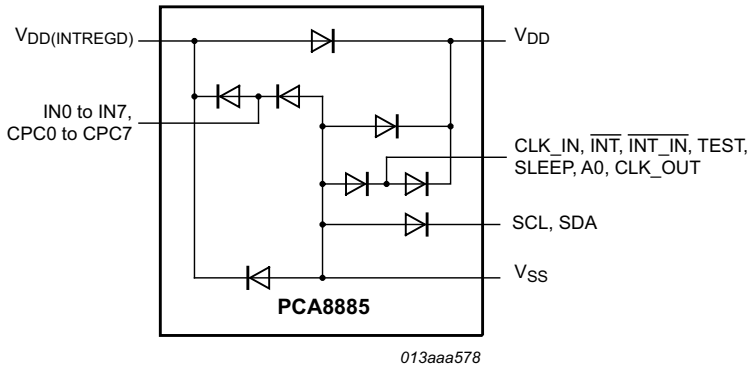


Fig 17. Device protection diagram

15. Safety notes

CAUTION

This device is sensitive to ElectroStatic Discharge (ESD). Observe precautions for handling electrostatic sensitive devices.

Such precautions are described in the *ANSI/ESD S20.20*, *IEC/ST 61340-5*, *JESD625-A* or equivalent standards.

16. Limiting values

Table 14. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
V_{DD}	supply voltage		−0.5	+8.0	V
$V_{DD(INTREGD)}$	internal regulated supply voltage		−0.5	+6.5	V
V_I	input voltage	on all input pins	−0.5	+6.5	V
I_{SS}	ground supply current		−50	+50	mA
I_{SDA}	current on pin SDA		−30	+30	mA
$I_{I/O(n)}$	input/output current on any other pin		−10	+10	mA
P_{tot}	total power dissipation		-	100	mW
V_{ESD}	electrostatic discharge voltage	HBM [1]	-	±2000	V
		CDM [2]	-	±750	V
I_{lu}	latch-up current	[3]	-	100	mA
T_{stg}	storage temperature	[4]	−60	+125	°C
T_{amb}	ambient temperature		−40	+85	°C

[1] Pass level; Human Body Model (HBM) according to Ref. 10 “JESD22-A114”.

[2] Pass level; Charged-Device Model (CDM), according to Ref. 11 “JESD22-C101”.

[3] Pass level; latch-up testing, according to Ref. 12 “JESD78” at maximum ambient temperature ($T_{amb(max)}$).

[4] According to the store and transport requirements (see Ref. 16 “UM10569”) the devices have to be stored at a temperature of +8 °C to +45 °C and a humidity of 25 % to 75 %.

17. Static characteristics

Table 15. Static characteristics

V_{DD} = 2.5 V to 5.5 V, V_{SS} = 0 V, T_{amb} = −40 °C to +85 °C; unless otherwise specified; min and max values are not production tested, but verified on sampling basis.

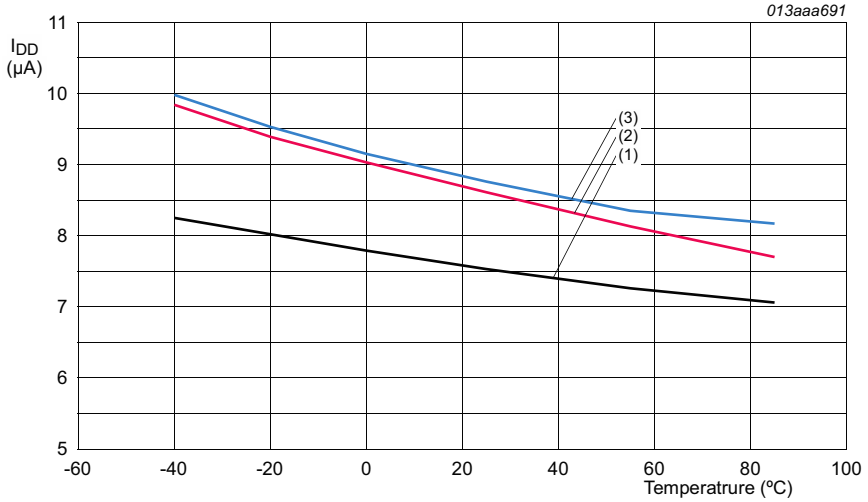
Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{DD}	supply voltage		2.5	-	5.5	V
$V_{DD(ext)}$	external supply voltage	V_{DD} connected to $V_{DD(INTREGD)}$; internal regulator disabled	2.5	-	3.3	V
$V_{DD(INTREGD)}$	internal regulated supply voltage	[1]				
			2.5	2.9	3.3	V
		external supplied	2.5	-	3.3	V
I_{DD}	supply current	idle state; f_s = 1 kHz [2]	-	10	20	µA
$I_{DD(sleep)}$	sleep mode supply current		-	100	500	nA
Digital inputs (CLK_IN, A0, INT_IN, TEST)						
V_{IL}	LOW-level input voltage		V_{SS}	-	$0.3V_{DD}$	V
V_{IH}	HIGH-level input voltage		$0.7V_{DD}$	-	V_{DD}	
Digital outputs (INT, CLK_OUT)						
V_{OL}	LOW-level output voltage	I_O = 0.5 mA	V_{SS}	-	$0.2V_{DD}$	V
V_{OH}	HIGH-level output voltage	I_O = 0.5 mA	$0.8V_{DD}$	-	V_{DD}	V
Analog pins (IN0 to IN7 and CPC0 to CPC7)						
V_{CPC}	voltage on pin CPC	usable control range	V_{SS} + 0.5	-	$V_{DD(INTREGD)}$ − 0.5	V
C_{in}	input capacitance	sensing plate and parasitic	10	-	40	pF
I²C interface pins (SDA, SCL)						
V_{IL}	LOW-level input voltage		−0.5	-	$0.3V_{DD}$	V
V_{IH}	HIGH-level input voltage		$0.7V_{DD}$	-	5.5	V
I_{OL}	LOW-level output current	V_{DD} = 5.0 V; V_{OL} = 0.4 V	20	-	-	mA
I_L	leakage current	[3]	-	0	-	µA
C_i	capacitance for each I/O pin		-	-	10	pF
External components						
C_{CPC}	capacitance on pin CPC	[4]	22	100	470	nF
C_{dec}	decoupling capacitance	on pins $V_{DD(INTREGD)}$ and V_{DD}; ceramic chip capacitor	-	100	-	nF

[1] See Figure 8 for an illustration of the voltage regulation behavior and the related parameters.

[2] Idle state is the steady state after completed power-on, without any mode change and without any activity on the sensor plates, and the voltages on the reservoir capacitors C_{CPC} are settled.

[3] In case of an ESD event, the value may increase slightly.

[4] The insulation resistance of the capacitor should be at least 5 GΩ.



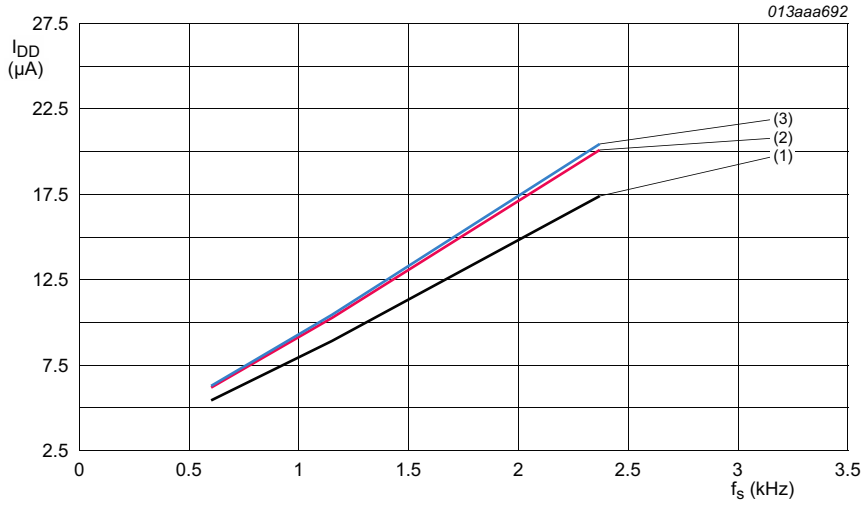
f_s = 1 kHz.

(1) V_{DD} = 2.5 V.

(2) V_{DD} = 3.3 V.

(3) V_{DD} = 5.5 V.

Fig 18. I_{DD} with respect to temperature

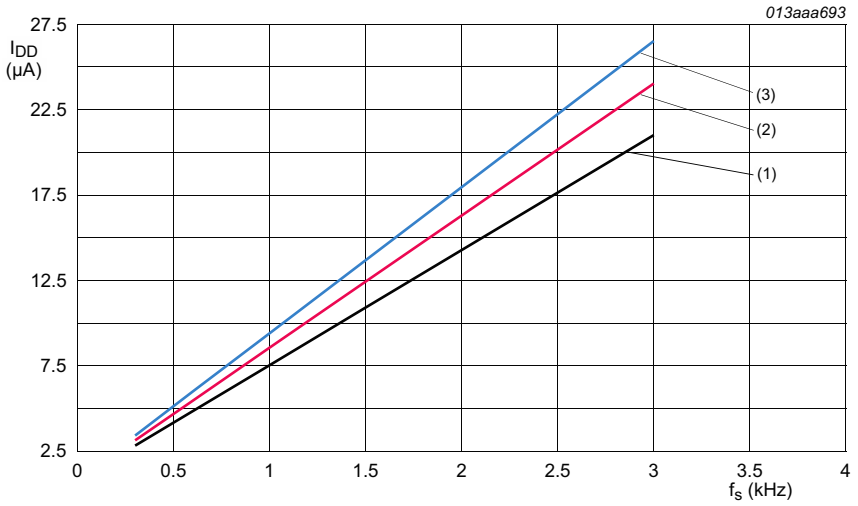


(1) V_{DD} = 2.5 V.

(2) V_{DD} = 3.3 V.

(3) V_{DD} = 5.5 V.

Fig 19. I_{DD} with respect to sampling frequency (internal clock)



(1) V_{DD} = 2.5 V.

(2) V_{DD} = 3.3 V.

(3) V_{DD} = 5.5 V.

Fig 20. I_{DD} with respect to sampling frequency (external clock)

18. Dynamic characteristics

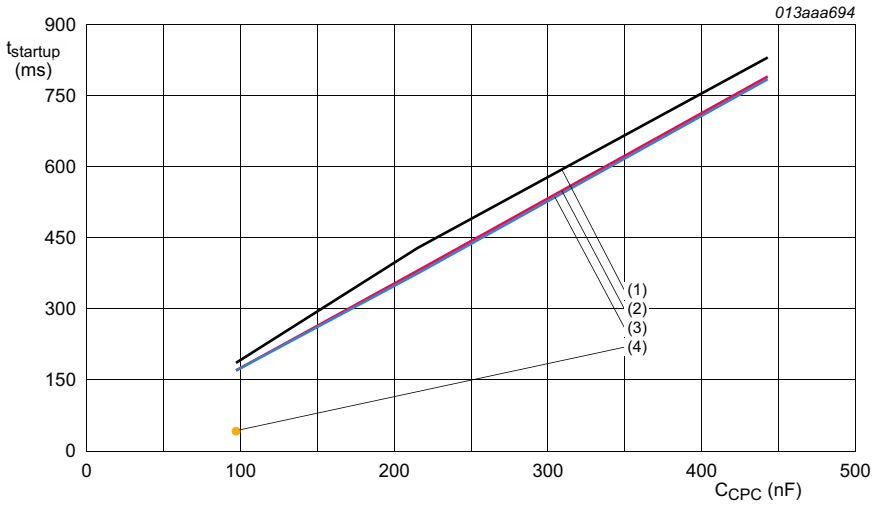
Table 16. Dynamic characteristics

V_{DD} = 2.5 V to 5.5 V, V_{SS} = 0 V, T_{amb} = −40 °C to +85 °C; unless otherwise specified; min and max values are not production tested, but verified on sampling basis.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
System timing						
$t_{startup}$	start-up time	C_{CPC} = 100 nF; f_s = 1 kHz; C_{in} = 40 pF	-	200	-	ms
f_{osc}	oscillator frequency	internal RC oscillator; FRQF[2:0] = 100 [1]	58	80	112	kHz
t_{sw}	switching time	f_s = 1 kHz [2]	-	64	-	ms
I²C interface characteristics (SDA, SCL)						
t_{SP}	pulse width of spikes that must be suppressed by the input filter		0	-	50	ns
f_{SCL}	SCL clock frequency		0	-	1000	kHz
$t_{HD;STA}$	hold time (repeated) START condition		0.26	-	-	µs
$t_{SU;STA}$	set-up time for a repeated START condition		0.26	-	-	µs
t_{LOW}	LOW period of the SCL clock		0.5	-	-	µs
t_{HIGH}	HIGH period of the SCL clock		0.26	-	-	µs
$t_{HD;DAT}$	data hold time		0	-	-	ns
$t_{SU;DAT}$	data set-up time		50	-	-	ns
t_r	rise time of both SDA and SCL signals		-	-	120	ns
t_f	fall time of both SDA and SCL signals		-	-	120	ns
$t_{SU;STO}$	set-up time for STOP condition		0.26	-	-	µs
t_{BUF}	bus free time between a STOP and START condition		0.5	-	-	µs
C_b	capacitive load for each bus line		-	-	550	pF
$t_{VD;DAT}$	data valid time		-	-	0.45	µs
$t_{VD;ACK}$	data valid acknowledge time		-	-	0.45	µs
$t_{w(int)}$	interrupt pulse width	interrupt over I²C	-	2	-	µs

[1] Default value.

[2] For switching, 64 consecutive CUP pulses are needed.



(1) V_{DD} = 2.5 V; C_i = 41 pF.

(2) V_{DD} = 3.3 V; C_i = 41 pF.

(3) V_{DD} = 5.5 V; C_i = 41 pF.

(4) V_{DD} = 3.3 V; C_i = 10 pF.

Fig 21. Start-up time with respect to C_{CPC}

18.1 I²C interface timing

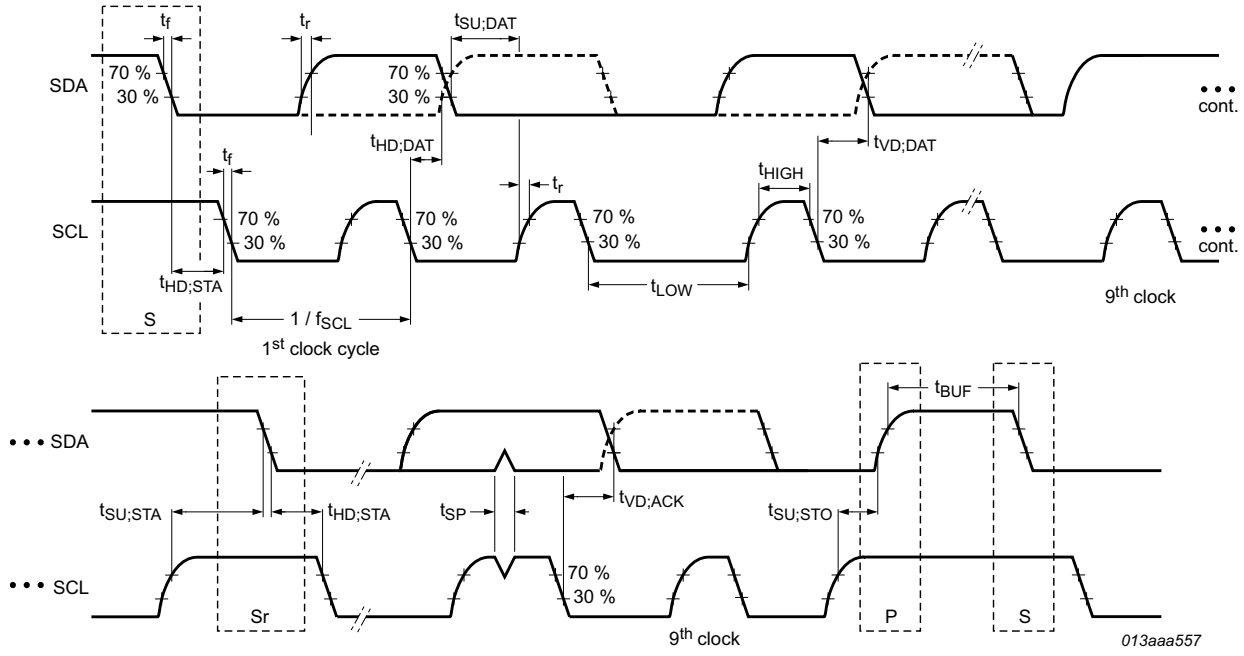
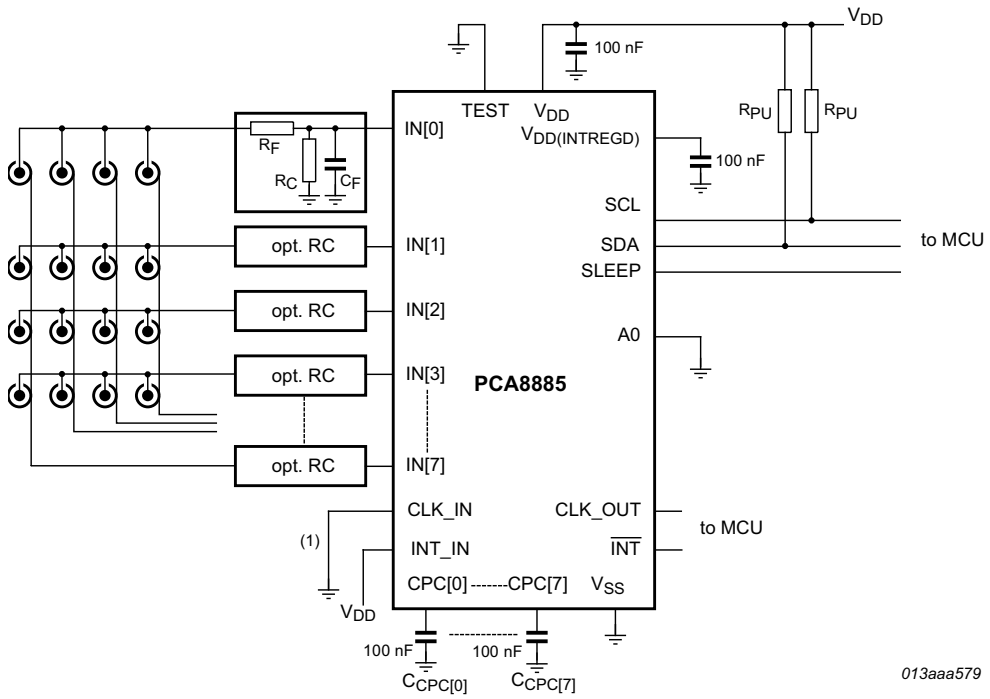


Fig 22. I²C interface timing

19. Application information

19.1 Single device application



(1) Pin CLK_IN can be tied to V_{SS} or left open.

Fig 23. Single device application diagram

19.2 28 sensor grid application in 2-key mode

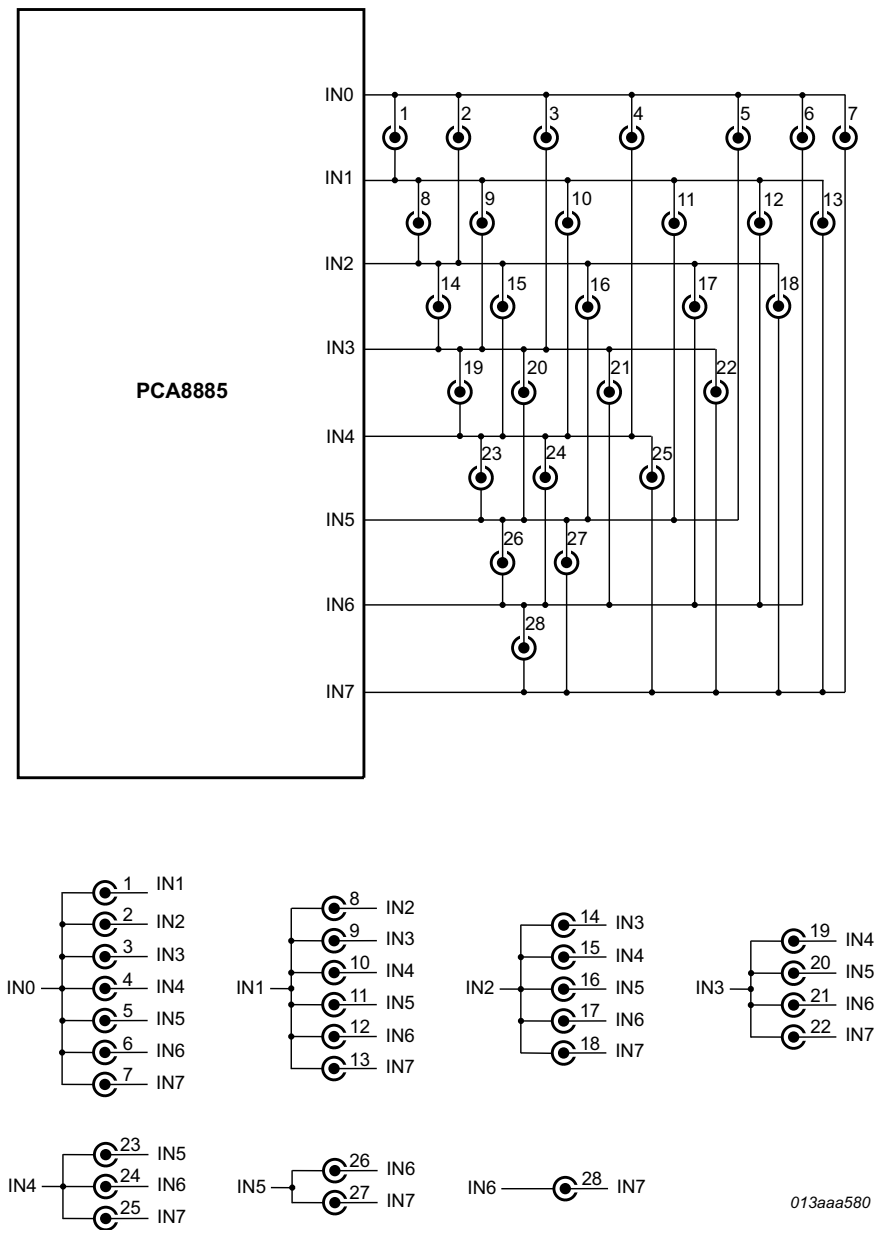
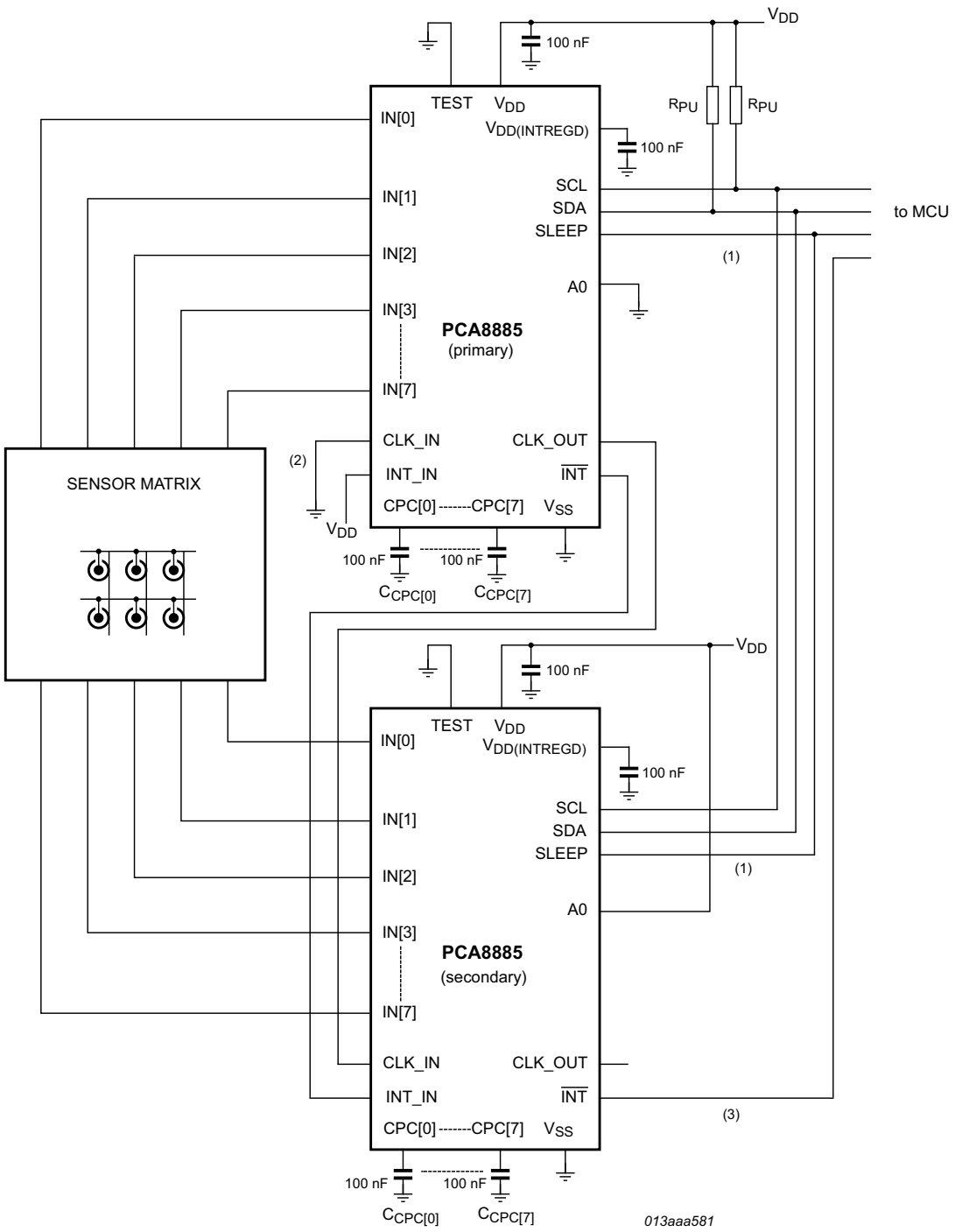


Fig 24. Application diagram for 28 sensors in 2-key mode

Table 17. Input combinations for a 28 sensor grid in 2-key mode

Sensor	Inputs							
	IN7	IN6	IN5	IN4	IN3	IN2	IN1	IN0
1	0	0	0	0	0	0	1	1
2	0	0	0	0	0	1	0	1
3	0	0	0	0	1	0	0	1
4	0	0	0	1	0	0	0	1
5	0	0	1	0	0	0	0	1
6	0	1	0	0	0	0	0	1
7	1	0	0	0	0	0	0	1
8	0	0	0	0	0	1	1	0
9	0	0	0	0	1	0	1	0
10	0	0	0	1	0	0	1	0
11	0	0	1	0	0	0	1	0
12	0	1	0	0	0	0	1	0
13	1	0	0	0	0	0	1	0
14	0	0	0	0	1	1	0	0
15	0	0	0	1	0	1	0	0
16	0	0	1	0	0	1	0	0
17	0	1	0	0	0	1	0	0
18	1	0	0	0	0	1	0	0
19	0	0	0	1	1	0	0	0
20	0	0	1	0	1	0	0	0
21	0	1	0	0	1	0	0	0
22	1	0	0	0	1	0	0	0
23	0	0	1	1	0	0	0	0
24	0	1	0	1	0	0	0	0
25	1	0	0	1	0	0	0	0
26	0	1	1	0	0	0	0	0
27	1	0	1	0	0	0	0	0
28	1	1	0	0	0	0	0	0

19.3 Cascaded application



(1) If the SLEEP pin is not used, it must be connected to V_{SS}.

(2) Pin CLK_IN can be tied to V_{SS} or left open.

(3) Instead of the $\overline{INT}$ pin, interrupt over I^2C-bus can be used. If the $\overline{INT}$ pin is not used, it must be left open.

Fig 25. Cascaded application diagram

Figure 25 shows the typical connections for a general application using two chips. For simplicity, the sensors attached to the secondary-chip are not shown in this diagram. The sensors of the secondary-chip can be arranged independently of the sensors of the primary-chip or combined in a common larger matrix.

Both chips use different I^2C addresses programmed by the voltage level applied to pin A0. The primary-chip has A0 connected to ground; the secondary-chip has A0 connected to $V_{DD(ext)}$. In this way, each circuit is addressed individually.

In this case, the primary-chip is programmed to use the internal oscillator as clock reference. The primary-chip is also programmed to enable the clock output. The secondary-chip is programmed to use the clock output from the primary-chip as input clock. The internal oscillator of the secondary-chip is shut down to save power in this mode.

The interrupt output $\overline{INT}$ of the primary-chip is routed to the $\overline{INT\_IN}$ input of the secondary-chip, where it is OR'ed with the interrupt state of the secondary-chip.

The sensing plate capacitances may consist of a small metal area, for example behind an isolating layer. Illustrated in Figure 25 is a 4 × 4 sensor arrangement. In this configuration, a sensor touch always excites two sensor plates at the same time.

The sensing plates are connected to a coaxial cable (for remote sensors) or a shielded connection, which in turn is connected to the input pin IN. The connection capacitance contributes to the input capacitance and must not be neglected. An internal low pass filter (not shown) is used to reduce RF interference. An additional low pass filter consisting of a resistor RF and capacitor CF can be added to the input to improve RF immunity further than required. For good performance, the total amount of capacitance on the input ($C_S + C_{CABLE} + C_F$) should be in the proper range, the optimum point being around 30 pF. Even if the external filtering is not required, placing C_F can help to bring the input capacitance to an optimal value. These conditions allow the control loop to adapt to the static capacitance on C_S and to compensate for slow changes in the sensing plate capacitance. A higher capacitive input loading is possible, if an additional discharge resistor RC is used. Resistor RC simply reduces the discharge time such that the internal timing requirements can be fulfilled.

The sensitivity of the sensors can be influenced by the sensing plate area and capacitors C_{CPC}. The sensitivity is reduced when C_{CPC} is reduced. When maximum sensitivity is desired, C_{CPC} can be increased, but it also increases sensitivity to interference. The CPC[0:7] pins have high impedance and are sensitive to leakage currents.

Remark: C_{CPC} should be a high-quality foil or ceramic capacitor, for example an X7R type.

For the choice of proper component values for a given application, the component specifications in Section 17 on page 25 must be followed.

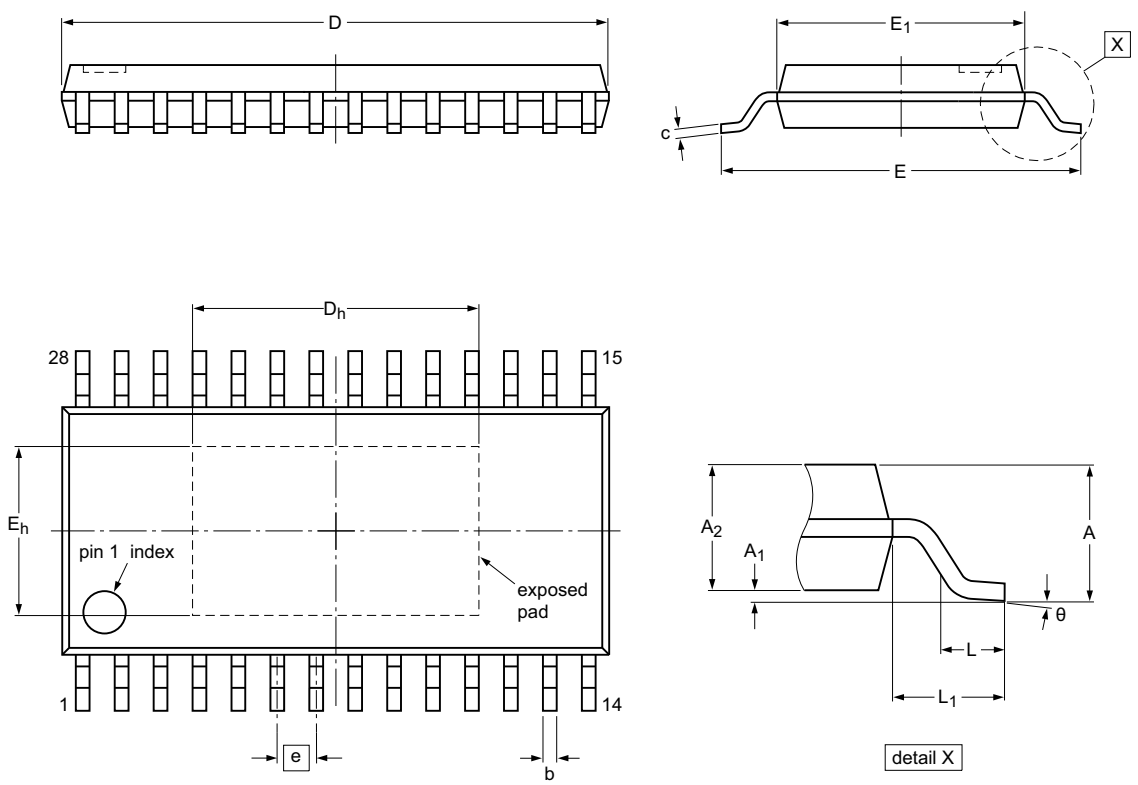
20. Test information

20.1 Quality information

This product has been qualified in accordance with the Automotive Electronics Council (AEC) standard *Q100 - Failure mechanism based stress test qualification for integrated circuits*, and is suitable for use in automotive applications.

21. Package outline

TSSOP28: plastic small outline package; 28 leads; body width 4.4 mm **PCA8885TS**



Dimensions

Unit[1]		A	A_1	A_2	b	c	D[1]	D_h	E	E_1	E_h	e	L	L_1	θ
	max	1.20	0.10	1.05	0.30	0.20	9.80		6.60	4.50			0.75		8°
mm	nom			0.90			9.70	5.08	6.40	4.40	2.997	0.65	0.60	1.00	
	min		0.025	0.80	0.19	0.09	9.60		6.20	4.30			0.45		0°

Note

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.

pca8885ts_po

Outline version	References				European projection	Issue date
	IEC	JEDEC	JEITA			
PCA8885TS		MO-153 ISSUE C				~~11-11-16~~ 12-08-06

Fig 26. Package outline PCA8885TS (TSSOP28)

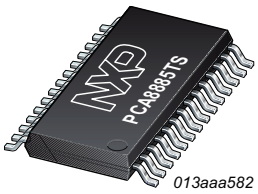


Fig 27. Three-dimensional package drawing of PCA8885

22. Soldering of SMD packages

This text provides a very brief insight into a complex technology. A more in-depth account of soldering ICs can be found in Application Note *AN10365 "Surface mount reflow soldering description"*.

22.1 Introduction to soldering

Soldering is one of the most common methods through which packages are attached to Printed Circuit Boards (PCBs), to form electrical circuits. The soldered joint provides both the mechanical and the electrical connection. There is no single soldering method that is ideal for all IC packages. Wave soldering is often preferred when through-hole and Surface Mount Devices (SMDs) are mixed on one printed wiring board; however, it is not suitable for fine pitch SMDs. Reflow soldering is ideal for the small pitches and high densities that come with increased miniaturization.

22.2 Wave and reflow soldering

Wave soldering is a joining technology in which the joints are made by solder coming from a standing wave of liquid solder. The wave soldering process is suitable for the following:

- Through-hole components
- Leaded or leadless SMDs, which are glued to the surface of the printed circuit board

Not all SMDs can be wave soldered. Packages with solder balls, and some leadless packages which have solder lands underneath the body, cannot be wave soldered. Also, leaded SMDs with leads having a pitch smaller than ~0.6 mm cannot be wave soldered, due to an increased probability of bridging.

The reflow soldering process involves applying solder paste to a board, followed by component placement and exposure to a temperature profile. Leaded packages, packages with solder balls, and leadless packages are all reflow solderable.

Key characteristics in both wave and reflow soldering are:

- Board specifications, including the board finish, solder masks and vias
- Package footprints, including solder thieves and orientation
- The moisture sensitivity level of the packages
- Package placement
- Inspection and repair
- Lead-free soldering versus SnPb soldering

22.3 Wave soldering

Key characteristics in wave soldering are:

- Process issues, such as application of adhesive and flux, clinching of leads, board transport, the solder wave parameters, and the time during which components are exposed to the wave
- Solder bath specifications, including temperature and impurities

22.4 Reflow soldering

Key characteristics in reflow soldering are:

- Lead-free versus SnPb soldering; note that a lead-free reflow process usually leads to higher minimum peak temperatures (see Figure 28) than a SnPb process, thus reducing the process window
- Solder paste printing issues including smearing, release, and adjusting the process window for a mix of large and small components on one board
- Reflow temperature profile; this profile includes preheat, reflow (in which the board is heated to the peak temperature) and cooling down. It is imperative that the peak temperature is high enough for the solder to make reliable solder joints (a solder paste characteristic). In addition, the peak temperature must be low enough that the packages and/or boards are not damaged. The peak temperature of the package depends on package thickness and volume and is classified in accordance with Table 18 and 19

Table 18. SnPb eutectic process (from J-STD-020D)

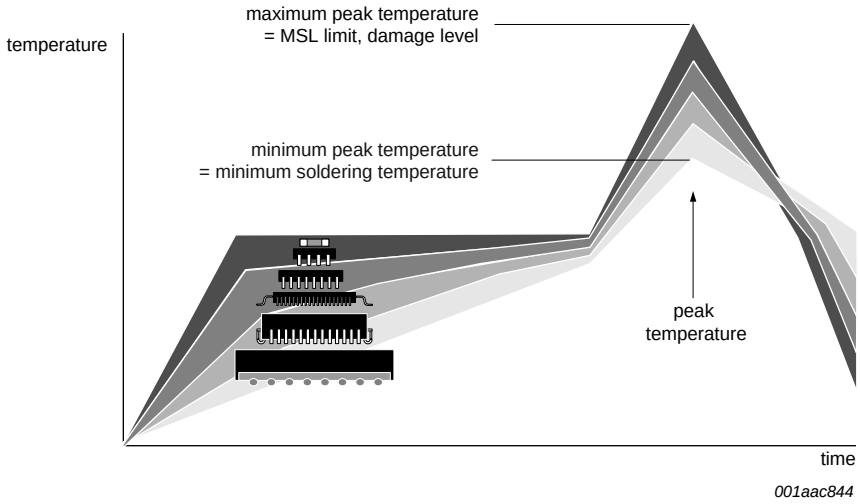
Package thickness (mm)	Package reflow temperature (°C)	
	Volume (mm^3)	
	< 350	≥ 350
< 2.5	235	220
≥ 2.5	220	220

Table 19. Lead-free process (from J-STD-020D)

Package thickness (mm)	Package reflow temperature (°C)		
	Volume (mm^3)		
	< 350	350 to 2000	> 2000
< 1.6	260	260	260
1.6 to 2.5	260	250	245
> 2.5	250	245	245

Moisture sensitivity precautions, as indicated on the packing, must be respected at all times.

Studies have shown that small packages reach higher temperatures during reflow soldering, see Figure 28.



MSL: Moisture Sensitivity Level

Fig 28. Temperature profiles for large and small components

For further information on temperature profiles, refer to Application Note *AN10365 "Surface mount reflow soldering description"*.

23. Abbreviations

Table 20. Abbreviations

Acronym	Description
CMOS	Complementary Metal Oxide Semiconductor
HBM	Human Body Model
IC	Integrated Circuit
MM	Machine Model
MOS	Metal Oxide Semiconductor
MOSFET	Metal–Oxide–Semiconductor Field-Effect Transistor
MSL	Moisture Sensitivity Level
PCB	Printed-Circuit Board
RC	Resistance-Capacitance
RF	Radio Frequency
SMD	Surface Mount Device

24. References

[1] **AN10365 —** Surface mount reflow soldering description

[2] **AN10832 —** PCF8883 - capacitive proximity switch with auto-calibration

[3] **AN10853 —** Handling precautions of ESD sensitive devices

[4] **AN11122 —** Water and condensation safe touch sensing with the NXP capacitive touch sensors

[5] **AN11157 —** Capacitive touch sensing with high EMC performance, Application Note

[6] **AN11155 —** General design guidelines for the NXP capacitive sensors

[7] **IEC 60134 —** Rating systems for electronic tubes and valves and analogous semiconductor devices

[8] **IEC 61340-5 —** Protection of electronic devices from electrostatic phenomena

[9] **IPC/JEDEC J-STD-020D —** Moisture/Reflow Sensitivity Classification for Nonhermetic Solid State Surface Mount Devices

[10] **JESD22-A114 —** Electrostatic Discharge (ESD) Sensitivity Testing Human Body Model (HBM)

[11] **JESD22-C101 —** Field-Induced Charged-Device Model Test Method for Electrostatic-Discharge-Withstand Thresholds of Microelectronic Components

[12] **JESD78 —** IC Latch-Up Test

[13] **JESD625-A —** Requirements for Handling Electrostatic-Discharge-Sensitive (ESDS) Devices

[14] **UM10204 —** I^2C-bus specification and user manual

[15] **UM10505 —** OM11057 quick start guide

[16] **UM10569 —** Store and transport requirements

[17] **UM10664 —** PCA8885 and PCF8885 evaluation board OM11056

[18] **UM10720 —** User manual for the TFT touch demo board OM11058

25. Revision history

Table 21. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
PCA8885 v.4	20140313	Product data sheet	-	PCA8885 v.3
Modifications:	• The format of this data sheet has been redesigned to comply with the new identity guidelines of NXP Semiconductors. • Legal texts have been adapted to the new company name where appropriate. • Emphasized the X7R statement (Section 19.3) • Adjusted Figure 7 and Figure 8 • Adjusted Figure 3, Figure 4, Figure 13, Figure 15 • Added Table 13 • Added Section 15			
PCA8885 v.3	20121002	Product data sheet	-	PCA8885 v.2
PCA8885 v.2	20120524	Product data sheet	-	PCA8885 v.1
PCA8885 v.1	20111124	Objective data sheet	-	-

26. Legal information

26.1 Data sheet status

Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

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