



THE DATASHEET OF DLPDLCR4710EVM



DLPA3005 PMIC and High-Current LED Driver IC

1 Features

- High-Efficiency, High-Current RGB LED Driver
- Drivers for External Buck FETs up to 16 A
- Drivers for External RGB Switches
- 10-Bit Programmable Current per Channel
- Inputs for Selecting Color-Sequential RGB LEDs
- Generation of DMD High Voltage Supplies
- Two High Efficiency Buck Converters to Generate the DLPC343x and DMD Supply
- Three High Efficiency, 8-Bit Programmable Buck Converters for FAN Driver Application or General Power Supply. General Purpose Buck2 (PWR6 currently supported, others may be available in the future)
- Two LDOs Supplying Auxiliary Voltages
- Analog MUX for Measuring internal and external nodes such as a thermistor and reference levels
- Monitoring/Protections: Thermal Shutdown, Hot Die, Low-Battery, and Undervoltage Lockout (UVLO)

2 Applications

Portable DLP® Pico™ Projectors

3 Description

The DLPA3005 is a highly-integrated power management IC optimized for DLP® Pico™ Projector systems. The DLPA3005 supports LED projectors up to 16 A per LED, enabled by an integrated high efficiency buck controller. Additionally, the drivers control the RGB switches, supporting the sequencing of R, G, and B LEDs. The DLPA3005 contains five buck converters, two of which are dedicated for DLPC low voltage supplies. Another dedicated regulating supply generates the three timing-critical DC supplies for the DMD: VBIAS, VRST, and VOFS.

The DLPA3005 contains several auxiliary blocks which can be used in a flexible way. This enables a tailor-made Pico Projector system. Three 8-bit programmable buck converters can be used, for instance, to drive rgb projector FANs or to make auxiliary supply lines. General Purpose Buck2 (PWR6) currently supported, others may be available in the future. Two LDOs can be used for a lower-current supply, up to 200 mA. These LDOs are pre-defined to 2.5 V and 3.3 V.

Through the SPI, all blocks of the DLPA3005 can be addressed. Features included are the generation of the system reset, power sequencing, input signals for sequentially selecting the active LED, IC self-protections, and an analog MUX for routing analog information to an external ADC.

Device Information⁽¹⁾

| PART NUMBER | PACKAGE | BODY SIZE (NOM) |
|-------------|-------------|---------------------|
| DLPA3005 | HTQFP (100) | 14.00 mm x 14.00 mm |

(1) For all available packages, see the orderable addendum at the end of the data sheet.

System Block Diagram

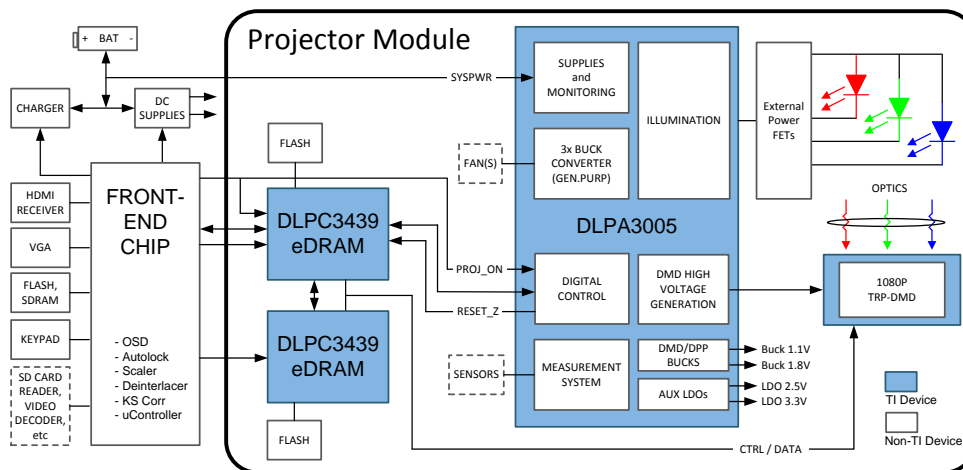


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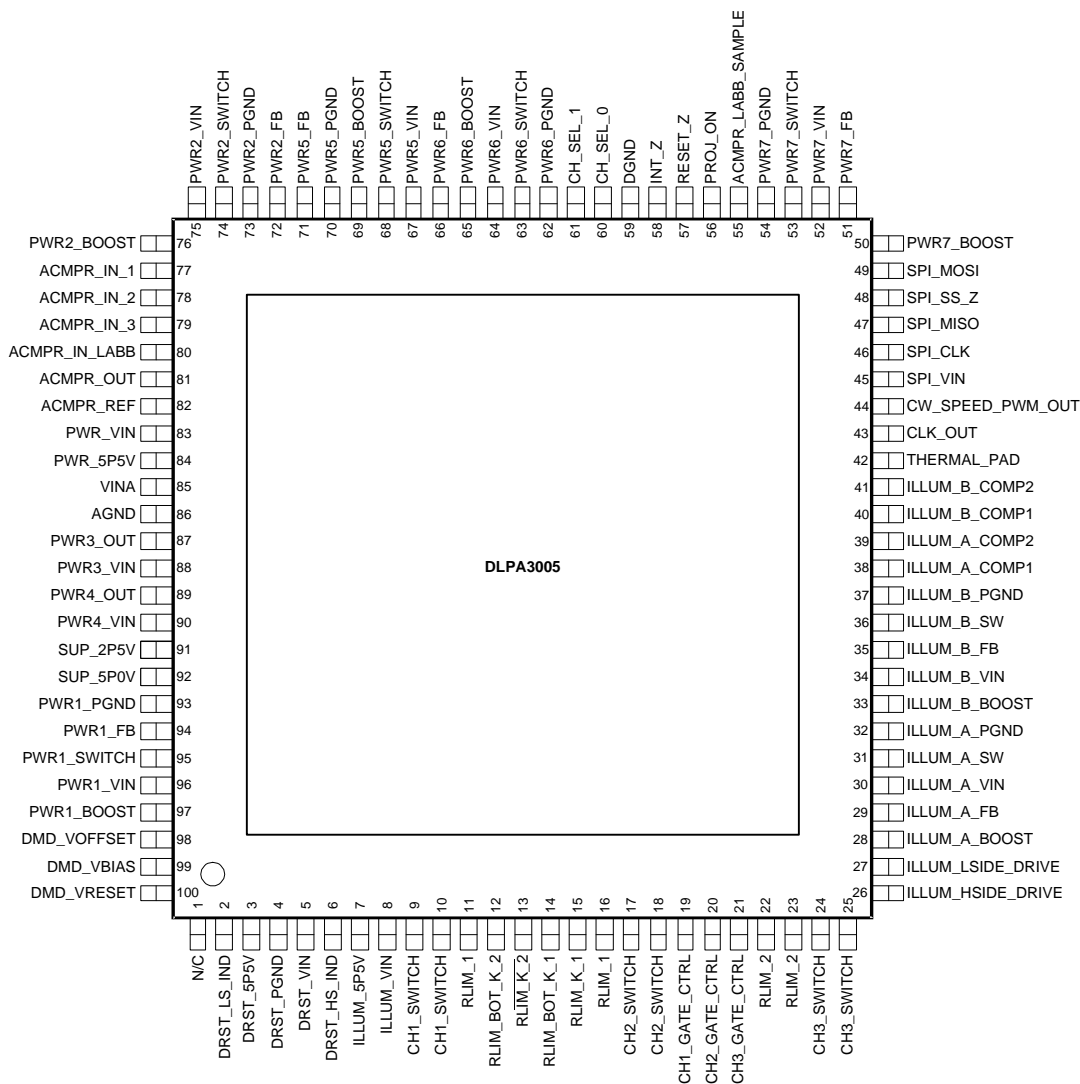
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4 Revision History

| DATE | REVISION | NOTES |
|--------------|----------|------------------|
| October 2015 | * | Initial release. |

5 Pin Configuration and Functions

**PFD Package
100-Pin HTQFP
Top View**



Pin Functions

| PIN | | I/O | DESCRIPTION |
|-------------|-----|-------|---|
| NAME | NO. | | |
| N/C | 1 | — | No connect |
| DRST_LS_IND | 2 | I/O | Connection for the DMD SMPS-inductor (low-side switch). |
| DRST_5P5V | 3 | O | Filter pin for LDO DMD. Power supply for internal DMD reset regulator, typical 5.5 V. |
| DRST_PGND | 4 | GND | Power ground for DMD SMPS. Connect to ground plane. |
| DRST_VIN | 5 | POWER | Power supply input for LDO DMD. Connect to system power. |
| DRST_HS_IND | 6 | I/O | Connection for the DMD SMPS-inductor (high-side switch). |
| ILLUM_5P5 V | 7 | O | Filter pin for LDO ILLUM. Power supply for internal ILLUM block, typical 5.5 V. |
| ILLUM_VIN | 8 | POWER | Supply input of LDO ILLUM. Connect to system power. |
| CH1_SWITCH | 9 | I | Low-side MOSFET switch for LED Cathode. Connect to RGB LED assembly. |
| CH1_SWITCH | 10 | I | Low-side MOSFET switch for LED Cathode. Connect to RGB LED assembly. |

Pin Functions (continued)

| PIN | | I/O | DESCRIPTION |
|-------------------|-----|-------|--|
| NAME | NO. | | |
| RLIM_1 | 11 | O | Connection to LED current sense resistor for CH1 and CH2. |
| RLIM_BOT_K_2 | 12 | I | Kelvin sense connection to ground side of LED current sense resistor. |
| RLIM_K_2 | 13 | I | Kelvin sense connection to top side of current sense resistor. |
| RLIM_BOT_K_1 | 14 | I | Kelvin sense connection to ground side of LED current sense resistor. |
| RLIM_K_1 | 15 | I | Kelvin sense connection to top side of current sense resistor. |
| RLIM_1 | 16 | O | Connection to LED current sense resistor for CH1 and CH2. |
| CH2_SWITCH | 17 | I | Low-side MOSFET switch for LED cathode. Connect to RGB LED assembly. |
| CH2_SWITCH | 18 | I | Low-side MOSFET switch for LED cathode. Connect to RGB LED assembly. |
| CH1_GATE_CTRL | 19 | O | Gate control of CH1 external MOSFET switch for LED cathode. |
| CH2_GATE_CTRL | 20 | O | Gate control of CH2 external MOSFET switch for LED cathode. |
| CH3_GATE_CTRL | 21 | O | Gate control of CH3 external MOSFET switch for LED cathode. |
| RLIM_2 | 22 | O | Connection to LED current sense resistor for CH3. |
| RLIM_2 | 23 | O | Connection to LED current sense resistor for CH3. |
| CH3_SWITCH | 24 | I | Low-side MOSFET switch for LED Cathode. Connect to RGB LED assembly. |
| CH3_SWITCH | 25 | I | Low-side MOSFET switch for LED Cathode. Connect to RGB LED assembly. |
| ILLUM_HSIDE_DRIVE | 26 | O | Gate control for external high-side MOSFET for ILLUM Buck converter. |
| ILLUM_LSIDE_DRIVE | 27 | O | Gate control for external low-side MOSFET for ILLUM Buck converter. |
| ILLUM_A_BOOST | 28 | I | Supply voltage for high-side N-channel MOSFET gate driver. A 100 nF capacitor (typical) must be connected between this pin and ILLUM_A_SW. |
| ILLUM_A_FB | 29 | I | Input to the buck converter loop controlling I_{LED} . |
| ILLUM_A_VIN | 30 | POWER | Power input to the ILLUM Driver A. |
| ILLUM_A_SW | 31 | I/O | Switch node connection between high-side NFET and low-side NFET. Serves as common connection for the flying high side FET driver. |
| ILLUM_A_PGND | 32 | GND | Ground connection to the ILLUM Driver A. |
| ILLUM_B_BOOST | 33 | I | Supply voltage for high-side N-channel MOSFET gate driver. |
| ILLUM_B_VIN | 34 | POWER | Power input to the ILLUM driver B. |
| ILLUM_B_FB | 35 | I | Input to the buck converter loop controlling I_{LED} . |
| ILLUM_B_SW | 36 | I/O | Switch node connection between high-side NFET and low-side NFET. |
| ILLUM_B_PGND | 37 | GND | Ground connection to the ILLUM driver B. |
| ILLUM_A_COMP1 | 38 | I/O | Connection node for feedback loop components |
| ILLUM_A_COMP2 | 39 | I/O | Connection node for feedback loop components |
| ILLUM_B_COMP1 | 40 | I/O | Connection node for feedback loop components |
| ILLUM_B_COMP2 | 41 | I/O | Connection node for feedback loop components |
| THERMAL_PAD | 42 | GND | Thermal pad. Connect to clean system ground. |
| CLK_OUT | 43 | O | Color wheel clock output |
| CW_SPEED_PWM_OUT | 44 | O | Color wheel PWM output |
| SPI_VIN | 45 | I | Supply for SPI interface |
| SPI_CLK | 46 | I | SPI clock input |
| SPI_MISO | 47 | O | SPI data output |
| SPI_SS_Z | 48 | I | SPI chip select (active low) |
| SPI_MOSI | 49 | I | SPI data input |
| PWR7_BOOST | 50 | I | Charge-pump-supply input for the high-side FET gate drive circuit. Connect 100 nF capacitor between PWR7_BOOST and PWR7_SWITCH pins. |
| PWR7_FB | 51 | I | Converter feedback input. Connect to converter output voltage. |
| PWR7_VIN | 52 | POWER | Power supply input for converter. |
| PWR7_SWITCH | 53 | I/O | Switch node connection between high-side NFET and low-side NFET. |
| PWR7_PGND | 54 | GND | Ground pin. Power ground return for switching circuit. |

Pin Functions (continued)

| PIN | | I/O | DESCRIPTION |
|-------------------|-----|-------|--|
| NAME | NO. | | |
| ACMPR_LABB_SAMPLE | 55 | I | Control signal to sample voltage at ACMPR_IN_LABB. |
| PROJ_ON | 56 | I | Input signal to enable/disable the IC and DLP projector. |
| RESET_Z | 57 | O | Reset output to the DLP system (active low). Pin is held low to reset DLP system. |
| INT_Z | 58 | O | Interrupt output signal (open drain, active low). Connect to pull-up resistor. |
| DGND | 59 | GND | Digital ground. Connect to ground plane. |
| CH_SEL_0 | 60 | I | Control signal to enable either of CH1,2,3. |
| CH_SEL_1 | 61 | I | Control signal to enable either of CH1,2,3. |
| PWR6_PGND | 62 | GND | Ground pin. Power ground return for switching circuit. |
| PWR6_SWITCH | 63 | I/O | Switch node connection between high-side NFET and low-side NFET. |
| PWR6_VIN | 64 | POWER | Power supply input for converter. |
| PWR6_BOOST | 65 | I | Charge-pump-supply input for the high-side FET gate drive circuit. Connect 100 nF capacitor between PWR6_BOOST and PWR6_SWITCH pins. |
| PWR6_FB | 66 | I | Converter feedback input. Connect to output voltage. |
| PWR5_VIN | 67 | POWER | Power supply input for converter. |
| PWR5_SWITCH | 68 | I/O | Switch node connection between high-side NFET and low-side NFET. |
| PWR5_BOOST | 69 | I | Charge-pump-supply input for the high-side FET gate drive circuit. Connect 100nF capacitor between PWR5_BOOST and PWR5_SWITCH pins. |
| PWR5_PGND | 70 | GND | Ground pin. Power ground return for switching circuit. |
| PWR5_FB | 71 | I | Converter feedback input. Connect to output voltage. |
| PWR2_FB | 72 | I | Converter feedback input. Connect to output voltage. |
| PWR2_PGND | 73 | GND | Ground pin. Power ground return for switching circuit. |
| PWR2_SWITCH | 74 | I/O | Switch node connection between high-side NFET and low-side NFET. |
| PWR2_VIN | 75 | POWER | Power supply input for converter. |
| PWR2_BOOST | 76 | I | Charge-pump-supply input for the high-side FET gate drive circuit. Connect 100 nF capacitor between PWR2_BOOST and PWR2_SWITCH pins. |
| ACMPR_IN_1 | 77 | I | Input for analog sensor signal. |
| ACMPR_IN_2 | 78 | I | Input for analog sensor signal. |
| ACMPR_IN_3 | 79 | I | Input for analog sensor signal. |
| ACMPR_IN_LABB | 80 | I | Input for ambient light sensor, sampled input |
| ACMPR_OUT | 81 | O | Analog comparator out |
| ACMPR_REF | 82 | I | Reference voltage input for analog comparator |
| PWR_VIN | 83 | POWER | Power supply input for LDO_Bucks. Connect to system power. |
| PWR_5P5V | 84 | O | Filter pin for LDO_BUCKS. Internal analog supply for buck converters, typical 5.5 V. |
| VINA | 85 | POWER | Input voltage supply pin for Reference system. |
| AGND | 86 | GND | Analog ground pin. |
| PWR3_OUT | 87 | O | Filter pin for LDO_2 DMD/DLPC/AUX, typical 2.5 V. |
| PWR3_VIN | 88 | POWER | Power supply input for LDO_2. Connect to system power. |
| PWR4_OUT | 89 | O | Filter pin for LDO_1 DMD/DLPC/AUX, typical 3.3 V. |
| PWR4_VIN | 90 | POWER | Power supply input for LDO_1. Connect to system power. |
| SUP_2P5V | 91 | O | Filter pin for LDO_V2V5. Internal supply voltage, typical 2.5 V. |
| SUP_5P0V | 92 | O | Filter pin for LDO_V5V. Internal supply voltage, typical 5 V. |
| PWR1_PGND | 93 | GND | Ground pin. Power ground return for switching circuit. |
| PWR1_FB | 94 | I | Converter feedback input. Connect to output voltage. |
| PWR1_SWITCH | 95 | I/O | Switch node connection between high-side NFET and low-side NFET. |
| PWR1_VIN | 96 | POWER | Power supply input for converter. |
| PWR1_BOOST | 97 | I | Charge-pump-supply input for the high-side FET gate drive circuit. Connect 100nF capacitor between PWR1_BOOST and PWR1_SWITCH pins. |

Pin Functions (continued)

| PIN | | I/O | DESCRIPTION |
|-------------|-----|-----|---|
| NAME | NO. | | |
| DMD_VOFFSET | 98 | O | VOFS output rail. Connect to ceramic capacitor. |
| DMD_VBIAS | 99 | O | VBIAS output rail. Connect to ceramic capacitor. |
| DMD_VRESET | 100 | O | VRESET output rail. Connect to ceramic capacitor. |

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature (unless otherwise noted) ⁽¹⁾

| | | MIN | MAX | UNIT |
|------------------|--|------|-----|------|
| Voltage | ILLUM_A,B_BOOST | -0.3 | 28 | V |
| | ILLUM_A,B_BOOST (10 ns transient) | -0.3 | 30 | |
| | ILLUM_A,B_BOOST vs ILLUM_A,B_SWITCH | -0.3 | 7 | |
| | ILLUM_LSIDE_DRIVE | -0.3 | 7 | |
| | ILLUM_HSIDE_DRIVE | -2 | 28 | |
| | ILLUM_A_BOOST vs ILLUM_HSIDE_DRIVE | -0.3 | 7 | |
| | ILLUM_A,B_SW | -2 | 22 | |
| | ILLUM_A,B_SW (10 ns transient) | -3 | 27 | |
| | PWR_VIN, PWR1,2,3,4,5,6,7_VIN, VINA, ILLUM_VIN, ILLUM_A,B_VIN, DRST_VIN | -0.3 | 22 | |
| | PWR1,2,5,6,7_BOOST | -0.3 | 28 | |
| | PWR1,2,5,6,7_BOOST (10 ns transient) | -0.3 | 30 | |
| | PWR1,2,5,6,7_SWITCH | -2 | 22 | |
| | PWR1,2,5,6,7_SWITCH (10 ns transient) | -3 | 27 | |
| | PWR1,2,5,6,7_FB | -0.3 | 6.5 | |
| | PWR1,2,5,6,7_BOOST vs PWR1,2,5,6,7_SWITCH | -0.3 | 6.5 | |
| | CH1,2,3_SWITCH, DRST_LS_IND, ILLUM_A,B_FB | -0.3 | 20 | |
| | ILLUM_A,B_COMP1,2, INT_Z, PROJ_ON | -0.3 | 7 | |
| | DRST_HS_IND | -18 | 7 | |
| | ACMPR_IN_1,2,3, ACMPR_REF, ACMPR_IN_LABB, ACMPR_LABB_SAMPLE, ACMPR_OUT | -0.3 | 3.6 | |
| | SPI_VIN, SPI_CLK, SPI_MOSI, SPI_SS_Z, SPI_MISO, CH_SEL_0,1, RESET_Z | -0.3 | 3.6 | |
| | RLIM_K_1,2, RLIM_1,2 | -0.3 | 3.6 | |
| | DGND, AGND, DRST_PGND, ILLUM_A,B_PGND, PWR1,2,5,6,7_PGND, RLIM_BOT_K_1,2 | -0.3 | 0.3 | |
| | DRST_5P5V, ILLUM_5P5V, PWR_5P5, PWR3,4_OUT, SUP_5P0V | -0.3 | 7 | |
| | CH1,2,3_GATE_CTRL | -0.3 | 7 | |
| | CLK_OUT | -0.3 | 3.6 | |
| | CW_SPEED_PWM | -0.3 | 7 | |
| | SUP_2P5V | -0.3 | 3.6 | |
| | DMD_VOFFSET | -0.3 | 12 | |
| | DMD_VBIAS | -0.3 | 20 | |
| | DMD_VRESET | -18 | 7 | |
| Source current | RESET_Z, ACMPR_OUT | | 1 | mA |
| | SPI_DOUT | | 5.5 | |
| Sink current | RESET_Z, ACMPR_OUT | | 1 | mA |
| | SPI_DOUT, INT_Z | | 5.5 | |
| T _{stg} | Storage temperature | -65 | 150 | °C |

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

6.2 ESD Ratings

| | | VALUE | UNIT |
|----------------------------|-------------------------|--|-------|
| $V_{(ESD)}$ ⁽¹⁾ | Electrostatic discharge | Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins ⁽²⁾ | ±2000 |
| | | Charged device model (CDM), per JEDEC specification JESD22-C101, all pins ⁽³⁾ | ±500 |

- (1) Electrostatic discharge (ESD) to measure device sensitivity and immunity to damage caused by assembly line electrostatic discharges in to the device.
- (2) JEDEC document JEP155 states that 500 V HBM allows safe manufacturing with a standard ESD control process.
- (3) JEDEC document JEP157 states that 250 V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

| | | MIN | MAX | UNIT |
|--------------------------------|---|------|------|------|
| Input voltage range | PWR_VIN, PWR1,2,3,4,5,6,7_VIN, VINA, ILLUM_VIN, ILLUM_A,B_VIN, DRST_VIN | 6 | 20 | V |
| | CH1,2,3_SWITCH, ILLUM_A,B_FB, | -0.1 | 6.3 | |
| | INT_Z, PROJ_ON | -0.1 | 6 | |
| | PWR1,2,5,6,7_FB | -0.1 | 5 | |
| | ACMPR_REF, CH_SEL_0,1, SPI_CLK, SPI_MOSI, SPI_SS_Z | -0.1 | 3.6 | |
| | RLIM_BOT_K_1,2 | -0.1 | 0.1 | |
| | ACMPR_IN_1,2,3, LABB_IN_LABB | -0.1 | 1.5 | |
| | SPI_VIN | 1.7 | 3.6 | |
| | RLIM_K_1,2 | -0.1 | 0.25 | |
| | ILLUM_A,B_COMP1,2 | -0.1 | 5.7 | |
| Ambient temperature range | | 0 | 70 | °C |
| Operating junction temperature | | 0 | 120 | °C |

6.4 Thermal Information

| THERMAL METRIC ⁽¹⁾ | | DLPA3005 | UNIT |
|-------------------------------|---|-------------|------|
| | | PFD (HTQFP) | |
| | | 100 PINS | |
| $R_{\theta JA}$ | Junction-to-ambient thermal resistance ⁽²⁾ | 7.0 | °C/W |
| $R_{\theta JC(top)}$ | Junction-to-case (top) thermal resistance ⁽³⁾ | 0.7 | °C/W |
| $R_{\theta JB}$ | Junction-to-board thermal resistance | N/A | °C/W |
| Ψ_{JT} | Junction-to-top characterization parameter ⁽⁴⁾ | 0.6 | °C/W |
| Ψ_{JB} | Junction-to-board characterization parameter ⁽⁵⁾ | 3.4 | °C/W |
| $R_{\theta JC(bot)}$ | Junction-to-case (bottom) thermal resistance | N/A | °C/W |

- (1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, [SPRA953](#).
- (2) The junction-to-ambient thermal resistance under natural convection is obtained in a simulation on a JEDEC-standard, high-K board, but since the device is intended to be cooled with a heatsink from the top case of the package, the simulation includes a fan and heatsink attached to the DLPA3005. The heatsink is a 22 mm × 22 mm × 12 mm aluminum pin fin heatsink with a 12 × 12 × 3 mm stud. Base thickness is 2 mm and pin diameter is 1.5 mm with an array of 6 × 6 pins. The heatsink is attached to the DLPA3005 with 100 um thick thermal grease with 3 W/m-K thermal conductivity. The fan is 20 × 20 × 8 mm with 1.6 cfm open volume flow rate and 0.22 in. water pressure at stagnation.
- (3) The junction-to-case (top) thermal resistance is obtained by simulating a cold plate test on the package top. No specific JEDEC standard test exists, but a close description can be found in the ANSI SEMI standard G30-88.
- (4) The junction-to-top characterization parameter, Ψ_{JT} , estimates the junction temperature of a device in a real system and is extracted from the simulation data for obtaining $R_{\theta JA}$, using a procedure described in JESD51-2a (sections 6 and 7), but modified to include the fan and heatsink described in note 2.
- (5) The junction-to-board characterization parameter, Ψ_{JB} , estimates the junction temperature of a device in a real system and is extracted from the simulation data for obtaining $R_{\theta JA}$, using a procedure described in JESD51-2a (sections 6 and 7), but modified to include the fan and heatsink described in note 2.

6.5 Electrical Characteristics

Over operating free-air temperature range. $V_{IN} = 12\text{ V}$, $T_A = 0$ to $+70^\circ\text{C}$, typical values are at $T_A = 25^\circ\text{C}$, Configuration according to *Typical Application* ($V_{IN} = 12\text{ V}$, $I_{OUT} = 16\text{ A}$, LED, external FETs) (unless otherwise noted).

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|--------------------------|-------------------------------|--|------------------|------|------|---------------|
| SUPPLIES | | | | | | |
| INPUT VOLTAGE | | | | | | |
| V_{IN} | Input voltage range | VINA – pin | 6 ⁽¹⁾ | 12 | 20 | V |
| V_{LOW_BAT} | Low battery warning threshold | VINA falling (via 5 bit trim function, 0.5 V steps) | 3.9 | | 18.4 | V |
| | Hysteresis | VINA rising | | 90 | | mV |
| V_{UVLO} | UVLO threshold | VINA falling (via 5 bit trim function, 0.5 V steps) | 3.9 | | 18.4 | V |
| | Hysteresis | VINA rising | | 90 | | mV |
| $V_{STARTUP}$ | Startup voltage | DMD_VBIAS, DMD_VOFFSET, DMD_VRESET loaded with 10 mA | 6 | | | V |
| INPUT CURRENT | | | | | | |
| I_{IDLE} | Idle current | IDLE mode, all VIN pins combined | | 15 | | μA |
| I_{STD} | Standby current | STANDBY mode, analog, internal supplies and LDOs enabled, DMD, ILLUMINATION and BUCK CONVERTERS disabled. | | 3.7 | | mA |
| I_{Q_DMD} | Quiescent current (DMD) | Quiescent current DMD block (in addition to I_{STD}) with DMD type TRP, VINA + DRST_VIN | | 0.49 | | mA |
| I_{Q_ILLUM} | Quiescent current (ILLUM) | Quiescent current ILLUM block (in addition to I_{STD}), $V_{openloop} = 3\text{ V}$ (0x18, ILLUM_OLV_SEL), VINA + ILLUM_VIN + ILLUM_A_VIN + ILLUM_B_VIN | | 21 | | mA |
| I_{Q_BUCK} | Quiescent current (per BUCK) | Quiescent current per BUCK converter (in addition to I_{STD}), Normal mode, VINA + PWR_VIN + PWR1,2,5,6,7_VIN, PWR1,2,5,6,7_VOUT = 1 V | | 4.3 | | mA |
| | | Quiescent current per BUCK converter (in addition to I_{STD}), Normal mode, VINA + PWR_VIN + PWR1,2,5,6,7_VIN, PWR1,2,5,6,7_VOUT = 5 V | | 15 | | |
| | | Quiescent current per BUCK converter (in addition to I_{STD}), Cycle-skipping mode, VINA + PWR_VIN + PWR1,2,5,6,7_VIN = 1 V | | 0.41 | | |
| | | Quiescent current per BUCK converter (in addition to I_{STD}), Cycle-skipping mode, VINA + PWR_VIN + PWR1,2,5,6,7_VIN = 5 V | | 0.46 | | |
| I_{Q_TOTAL} | Quiescent current (Total) | Typical Application: ACTIVE mode, all VIN pins combined, DMD, ILLUMINATION and PWR1,2 enabled, PWR3,4,5,6,7 disabled. | | 38 | | mA |
| INTERNAL SUPPLIES | | | | | | |
| V_{SUP_5P0V} | Internal supply, analog | | | 5 | | V |
| V_{SUP_2P5V} | Internal supply, logic | | | 2.5 | | V |
| DMD - LDO DMD | | | | | | |
| V_{DRST_VIN} | | | 6 | 12 | 20 | V |
| V_{DRST_5P5V} | | | | 5.5 | | V |

- (1) V_{IN} must be higher than the UVLO voltage setting, including after accounting for AC noise on V_{IN} , for the DLPA3005 to fully operate. While 6.0V is the min V_{IN} voltage supported, TI recommends that the UVLO is never set below 6.21V. 6.21V gives margin above 6.0V to protect against the case where someone suddenly removes V_{IN} 's power supply which causes the V_{IN} voltage to drop rapidly. Failure to keep V_{IN} above 6.0V before the mirrors are parked and VOFS, VRST, and VBIAS supplies are properly shut down can result in permanent damage to the DMD. Since 6.21V is .21V above 6.0V, when UVLO trips there is time for the DLPA3005 and DLPC343x to park the DMD mirrors and do a fast shut down of supplies VOFS, VRST, and VBIAS. For whatever UVLO setting is used, if V_{IN} 's power supply is suddenly removed enough bulk capacitance should be included on V_{IN} inside the projector to keep V_{IN} above 6.0V for at least 100us after UVLO trips.

Electrical Characteristics (continued)

Over operating free-air temperature range. $V_{IN} = 12\text{ V}$, $T_A = 0\text{ to }+70^\circ\text{C}$, typical values are at $T_A = 25^\circ\text{C}$, Configuration according to [Typical Application](#) ($V_{IN} = 12\text{ V}$, $I_{OUT} = 16\text{ A}$, LED, external FETs) (unless otherwise noted).

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|--------------------------|---|--|------|------|-----|------|
| PGOOD | Power good DRST_5P5V | Rising | | 80% | | |
| | | Faling | | 60% | | |
| OVP | Overvoltage protection DRST_5P5V | | | 7.2 | | V |
| | Regulator dropout | At 25 mA, VDRST_VIN= 5.5 V | | 56 | | mV |
| | Regulator current limit ⁽²⁾ | | 300 | 340 | 400 | mA |
| DMD - REGULATOR | | | | | | |
| R _{DS(ON)} | MOSFET ON-resistance | Switch A (from DRST_5P5V to DRST_HS_IND) | | 920 | | mΩ |
| | | Switch B (from DRST_LS_IND to DRST_PGND) | | 450 | | |
| V _{FW} | Forward voltage drop | Switch C (from DRST_LS_IND to DRST_VBIAS ⁽³⁾), VDRST_LS_IND = 2 V, I _F = 100 mA | | 1.21 | | V |
| | | Switch D (from DRST_LS_IND to DRST_VOFFSET ⁽³⁾), VDRST_LS_IND = 2 V, I _F = 100 mA | | 1.22 | | |
| t _{DIS} | Rail Discharge time | C _{OUT} = 1 μF | | | 40 | μs |
| t _{PG} | Power-good timeout | not tested in production | | 15 | | ms |
| I _{LIMIT} | Switch current limit | DMD type TRP | | 610 | | mA |
| VOFFSET REGULATOR | | | | | | |
| V _{OFFSET} | Output voltage | DMD type TRP | | 10 | | V |
| | DC output voltage accuracy | DMD type TRP, I _{OUT} = 10 mA | -0.3 | | 0.3 | V |
| | DC Load regulation | DMD type TRP, I _{OUT} = 0 to 10 mA | | -10 | | V/A |
| | DC Line regulation | DMD type TRP, I _{OUT} = 10 mA, DRST_VIN = 8 V to 20 V | | -5 | | mV/V |
| V _{RIPPLE} | Output ripple | DMD type TRP, I _{OUT} = 10 mA, C _{OUT} = 1 μF | | 200 | | mVpp |
| I _{OUT} | Output current | DMD type TRP | 0.1 | | 10 | mA |
| PGOOD | Power-good threshold (fraction of nominal output voltage) | VOFFSET rising | | 86% | | |
| | | VOFFSET falling | | 66% | | |
| C | Output capacitor | DMD type TRP, Recommended value ⁽⁴⁾ (use same value as output capacitor on VRESET) | 1 | | | μF |
| | | t _{DISCHARGE} <40 μs at VIN = 8 V | | | 1 | |
| VBIAS REGULATOR | | | | | | |
| V _{BIAS} | Output voltage | DMD type TRP | | 18 | | V |
| | DC output voltage accuracy | DMD type TRP, I _{OUT} = 10 mA | -0.3 | | 0.3 | V |
| | DC Load regulation | DMD type TRP, I _{OUT} = 0 to 10 mA | | -18 | | V/A |
| | DC Line regulation | DMD type TRP, I _{OUT} = 10 mA, DRST_VIN = 8 V to 20 V | | -3 | | mV/V |
| V _{RIPPLE} | Output ripple | DMD type TRP, I _{OUT} = 10 mA, C _{OUT} = 470 nF | | 200 | | mVpp |
| I _{OUT} | Output current | DMD type TRP | 0.1 | | 10 | mA |
| PGOOD | Power-good threshold (fraction of nominal output voltage) | VBIAS rising | | 86% | | |
| | | VBIAS falling | | 66% | | |

(2) Not production tested.

(3) Including rectifying diode.

(4) Take care that the capacitor has the specified capacitance at the related voltage, that is V_{OFFSET}, V_{BIAS} or V_{RESET}

Electrical Characteristics (continued)

Over operating free-air temperature range. $V_{IN} = 12\text{ V}$, $T_A = 0\text{ to }+70^\circ\text{C}$, typical values are at $T_A = 25^\circ\text{C}$, Configuration according to [Typical Application](#) ($V_{IN} = 12\text{ V}$, $I_{OUT} = 16\text{ A}$, LED, external FETs) (unless otherwise noted).

| PARAMETER | TEST CONDITIONS | MIN | TYP | MAX | UNIT | | | |
|----------------------------------|---|--|-----|-----|------|---------------|------------|----|
| C | Output capacitor | DMD type TRP, recommended value ⁽⁴⁾ (use same or smaller value as output capacitors VOFFSET / VRESET) | | | 470 | nF | | |
| | | $t_{DISCHARGE} < 40\ \mu\text{s}$ at $V_{IN} = 8\text{ V}$ | | | 470 | | | |
| VRESET REGULATOR | | | | | | | | |
| V_{RST} | Output voltage | DMD type TRP | | | -14 | V | | |
| | DC output voltage accuracy | DMD type TRP, $I_{OUT} = 10\text{ mA}$ | | | -0.3 | 0.3 | V | |
| | DC Load regulation | DMD type TRP, $I_{OUT} = 0\text{ to }10\text{ mA}$ | | | -4 | | V/A | |
| | DC Line regulation | DMD type TRP, $I_{OUT} = 10\text{ mA}$, $DRST_VIN = 8\text{ to }20\text{ V}$ | | | -2 | | mV/V | |
| V_{RIPPLE} | Output ripple | DMD type TRP, $I_{OUT} = 10\text{ mA}$, $C_{OUT} = 1\ \mu\text{F}$ | | | 120 | | mVpp | |
| I_{OUT} | Output current | DMD type TRP | | | 0.1 | 10 | mA | |
| PGOOD | Power-good threshold | | | | 90% | | | |
| C | Output capacitor | DMD type TRP, Recommended value ⁽⁴⁾ (use same value as output capacitor on VOFFSET) | | | 1 | μF | | |
| | | $t_{DISCHARGE} < 40\ \mu\text{s}$ at $V_{IN} = 8\text{ V}$ | | | 1 | | | |
| DMD - BUCK CONVERTERS | | | | | | | | |
| OUTPUT VOLTAGE | | | | | | | | |
| $V_{PWR_1_VOUT}$ | Output Voltage | DMD type TRP | | | 1.1 | | V | |
| $V_{PWR_2_VOUT}$ | Output Voltage | DMD type TRP | | | 1.8 | | V | |
| | DC output voltage accuracy | DMD type TRP, $I_{OUT} = 0\text{ mA}$ | | | -3% | 3% | | |
| MOSFET | | | | | | | | |
| $R_{ON,H}$ | High side switch resistance | 25°C , $V_{PWR_1,2_Boost} - V_{PWR1,2_SWITCH} = 5.5\text{ V}$ | | | 150 | | m Ω | |
| $R_{ON,L}$ | Low side switch resistance ⁽²⁾ | 25°C | | | 85 | | m Ω | |
| LOAD CURRENT | | | | | | | | |
| | Allowed Load Current ⁽⁵⁾ | | | | 3 | | A | |
| I_{OCL} | Current limit ⁽²⁾ | $L_{OUT} = 3.3\ \mu\text{H}$ | | | 3.2 | 3.6 | 4.2 | A |
| ON-TIME TIMER CONTROL | | | | | | | | |
| t_{ON} | On time | $V_{IN} = 12\text{ V}$, $V_O = 5\text{ V}$ | | | 120 | | ns | |
| $t_{OFF(MIN)}$ | Minimum off time ⁽²⁾ | $T_A = 25^\circ\text{C}$, $V_{FB} = 0\text{ V}$ | | | 270 | | ns | |
| START-UP | | | | | | | | |
| | Soft start | | | | 1 | 2.5 | 4 | ms |
| PGOOD | | | | | | | | |
| Ratio _{OV} | Overvoltage protection | | | | 120% | | | |
| Ratio _{PG} | Relative power good level | Low to High | | | 72% | | | |
| ILLUMINATION - LDO ILLUM | | | | | | | | |
| V_{ILLUM_VIN} | | | | | 6 | 12 | 20 | V |
| V_{ILLUM_5P5V} | | | | | 5.5 | | | V |
| PGOOD | Power good ILLUM_5P5V | Rising | | | 80% | | | |
| | | Falling | | | 60% | | | |
| OVP | Overvoltage protection ILLUM_5P5V | | | | 7.2 | | V | |
| | Regulator dropout | At 25 mA, $V_{ILLUM_VIN} = 5.5\text{ V}$ | | | 53 | | mV | |
| | Regulator current limit ⁽²⁾ | | | | 300 | 340 | 400 | mA |
| ILLUMINATION - DRIVER A,B | | | | | | | | |
| V_{ILLUM_A,B_IN} | Input supply voltage range | | | | 6 | 12 | 20 | V |

(5) Care should be taken not to exceed the max power dissipation. Refer to [Thermal Considerations](#).

Electrical Characteristics (continued)

Over operating free-air temperature range. $V_{IN} = 12\text{ V}$, $T_A = 0$ to $+70^\circ\text{C}$, typical values are at $T_A = 25^\circ\text{C}$, Configuration according to [Typical Application](#) ($V_{IN} = 12\text{ V}$, $I_{OUT} = 16\text{ A}$, LED, external FETs) (unless otherwise noted).

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|--|---|--|-------|------|-----|---------------|
| PWM | | | | | | |
| f_{SW} | Oscillator frequency | $3\text{ V} < V_{IN} < 20\text{ V}$ | | 600 | | kHz |
| t_{DEAD} | Output driver dead time | HDRV off to LDRV on, TRDLY = 0 | | 28 | | ns |
| | | HDRV off to LDRV on, TRDLY = 1 | | 40 | | |
| | | LDRV off to HDRV on, TRDLY = 0 | | 35 | | |
| OUTPUT DRIVERS | | | | | | |
| R_{HDHI} | High-side driver pull-up resistance | $V_{ILLUM_A,B_BOOT} - V_{ILLUM_A,B_SW} = 5\text{ V}$, $I_{HDRV} = -100\text{ mA}$ | | 4.9 | | Ω |
| R_{HDLO} | High-side driver pull-down resistance | $V_{ILLUM_A,B_BOOT} - V_{ILLUM_A,B_SW} = 5\text{ V}$, $I_{HDRV} = 100\text{ mA}$ | | 3 | | Ω |
| R_{LDHI} | Low-side driver pull-up resistance | $I_{LDRV} = -100\text{ mA}$ | | 3.1 | | Ω |
| R_{LDLO} | Low-side driver pull-down resistance | $I_{LDRV} = 100\text{ mA}$ | | 2.4 | | Ω |
| t_{HRISE} | High-side driver rise time ⁽²⁾ | $C_{LOAD} = 5\text{ nF}$ | | 23 | | ns |
| t_{HFALL} | High-side driver fall time ⁽²⁾ | $C_{LOAD} = 5\text{ nF}$ | | 19 | | ns |
| t_{LRISE} | Low-side driver rise time ⁽²⁾ | $C_{LOAD} = 5\text{ nF}$ | | 23 | | ns |
| t_{LFALL} | Low-side driver fall time ⁽²⁾ | $C_{LOAD} = 5\text{ nF}$ | | 17 | | ns |
| OVERCURRENT PROTECTION | | | | | | |
| HSD OC | High-Side Drive Over Current threshold | External switches, V_{DS} threshold ⁽²⁾ . | | 185 | | mV |
| BOOT DIODE | | | | | | |
| V_{DFWD} | Bootstrap diode forward voltage | $I_{BOOT} = 5\text{ mA}$ | | 0.75 | | V |
| PGOOD | | | | | | |
| RatioUV | Undervoltage protection | | | 89% | | |
| INTERNAL RGB STROBE CONTROLLER SWITCHES | | | | | | |
| R_{ON} | ON-resistance | CH1,2,3_SWITCH | | 30 | 45 | m Ω |
| I_{LEAK} | OFF-state leakage current | $V_{DS} = 5.0\text{ V}$ | | | 0.1 | μA |
| I_{MAX} | Maximum current | | | 6 | | A |
| DRIVERS EXTERNAL RGB STROBE CONTROLLER SWITCHES | | | | | | |
| CHx_GATE_CN TR_HIGH | Gate control high level | ILLUM_SW_ILIM_EN[2:0] = 7, register 0x02, $I_{SINK} = 400\text{ }\mu\text{A}$ | | 4.35 | | V |
| | | ILLUM_SW_ILIM_EN[2:0] = 0, register 0x02, $I_{SINK} = 400\text{ }\mu\text{A}$ | | 5.25 | | |
| CHx_GATE_CN TR_LOW | Gate control low level | ILLUM_SW_ILIM_EN[2:0] = 7, register 0x02, $I_{SINK} = 400\text{ }\mu\text{A}$ | | 55 | | mV |
| | | ILLUM_SW_ILIM_EN[2:0] = 0, register 0x02, $I_{SINK} = 400\text{ }\mu\text{A}$ | | 55 | | |
| LED CURRENT CONTROL | | | | | | |
| V_{LED_ANODE} | LED Anode voltage ⁽²⁾ | Ratio with respect to V_{ILLUM_A,B_VIN} (Duty cycle limitation). | 0.85x | | | |
| | | | | | 6.3 | V |
| I_{LED} | LED currents | $V_{ILLUM_A,B_VIN} \geq 8\text{ V}$. See register SWx_IDAC[9:0] for settings. | 1 | | 16 | A |
| | DC current offset, CH1,2,3_SWITCH | $R_{LIM} = 12.5\text{ m}\Omega$ | -150 | 0 | 150 | mA |

Electrical Characteristics (continued)

Over operating free-air temperature range. $V_{IN} = 12\text{ V}$, $T_A = 0\text{ to }+70^\circ\text{C}$, typical values are at $T_A = 25^\circ\text{C}$, Configuration according to [Typical Application](#) ($V_{IN} = 12\text{ V}$, $I_{OUT} = 16\text{ A}$, LED, external FETs) (unless otherwise noted).

| PARAMETER | TEST CONDITIONS | MIN | TYP | MAX | UNIT | | |
|---|---|--|------|-------|---------------|------------|---|
| Transient LED current limit range (programmable) | 20% higher than I_{LED} . Min-setting, $R_{LIM} = 12.5\text{ m}\Omega$. | | 11% | | | | |
| | 20% higher than I_{LED} . Max-setting, $R_{LIM} = 12.5\text{ m}\Omega$. Percentage of max current. | | 133% | | | | |
| t_{RISE} | Current rise time | | | 50 | μs | | |
| BUCK CONVERTERS - LDO_BUCKS | | | | | | | |
| V_{PWR_VIN} | Input voltage range PWR1,2,5,6,7_VIN | 6 | 12 | 20 | V | | |
| V_{PWR_5P5V} | PWR_5P5V | | 5.5 | | V | | |
| PGOOD | Power good PWR_5P5V | Rising | 80% | | | | |
| | | Falling | 60% | | | | |
| OVP | Overvoltage Protection PWR_5P5V | | 7.2 | | V | | |
| | Regulator dropout | At 25 mA, $V_{PWR_VIN} = 5.5\text{ V}$ | | 41 | mV | | |
| | Regulator current limit ⁽²⁾ | 300 | 340 | 400 | mA | | |
| BUCK CONVERTERS - GENERAL PURPOSE BUCK CONVERTERS ⁽⁶⁾ | | | | | | | |
| OUTPUT VOLTAGE | | | | | | | |
| $V_{PWR_5,6,7_VOUT}$ | Output Voltage (General Purpose Buck1,2,3) | 8-bit programmable | | 1 | 5 | V | |
| | DC output voltage accuracy | $I_{OUT} = 0\text{ mA}$ | | -3.5% | 3.5% | | |
| MOSFET | | | | | | | |
| $R_{ON,H}$ | High side switch resistance | 25°C, $V_{PWR5,6,7_Boost} - V_{PWR5,6,7_SWITCH} = 5.5\text{ V}$ | | 150 | | m Ω | |
| $R_{ON,L}$ | Low side switch resistance ⁽²⁾ | 25°C | | 85 | | m Ω | |
| LOAD CURRENT | | | | | | | |
| | Allowed Load Current PWR6 ⁽⁵⁾ . | | | 2 | | A | |
| | Allowed Load Current PWR5, PWR7 ⁽⁵⁾ . | Buck converters should not be used at this time. May become available in the future. | | | | A | |
| I_{OCL} | Current limit ⁽²⁾⁽⁵⁾ | $L_{OUT} = 3.3\text{ }\mu\text{H}$ | | 3.2 | 3.6 | 4.2 | A |
| ON-TIME TIMER CONTROL | | | | | | | |
| t_{ON} | On time | $V_{IN} = 12\text{ V}$, $V_O = 5\text{ V}$ | | 120 | | ns | |
| $t_{OFF(MIN)}$ | Minimum off time ⁽²⁾ | $T_A = 25^\circ\text{C}$, $V_{FB} = 0\text{ V}$ | | 270 | 310 | ns | |
| START-UP | | | | | | | |
| | Soft start | 1 | 2.5 | 4 | | ms | |
| PGOOD | | | | | | | |
| Ratio _{OV} | Overvoltage protection | | | 120% | | | |
| Ratio _{PG} | Relative power good level | Low to High | | 72% | | | |
| AUXILIARY LDOs | | | | | | | |
| $V_{PWR3,4_VIN}$ | Input voltage range | LDO1 (PWR4), LDO2 (PWR3) | | 3.3 | 12 | 20 | V |
| PGOOD | Power good PWR3,4_VOUT | PWR3,4_VOUT rising | | 80% | | | |
| | | PWR3,4_VOUT falling | | 60% | | | |
| OVP | Overvoltage Protection PWR3,4_VOUT | | | 7 | | V | |

(6) General Purpose Buck2 (PWR6) currently supported, others may be available in the future.

Electrical Characteristics (continued)

Over operating free-air temperature range. $V_{IN} = 12\text{ V}$, $T_A = 0$ to $+70^\circ\text{C}$, typical values are at $T_A = 25^\circ\text{C}$, Configuration according to [Typical Application](#) ($V_{IN} = 12\text{ V}$, $I_{OUT} = 16\text{ A}$, LED, external FETs) (unless otherwise noted).

| PARAMETER | TEST CONDITIONS | MIN | TYP | MAX | UNIT | |
|--|---------------------------------------|--|------|------|-----------------|---------------|
| DC output voltage accuracy PWR3,4_VOUT | $I_{OUT} = 0\text{ mA}$ | -3% | | 3% | | |
| Regulator current limit ⁽²⁾ | | 300 | 340 | 400 | mA | |
| t_{ON} | Turn-on time | to 80% of $V_{OUT} = \text{PWR3}$ and PWR4 , $C = 1\ \mu\text{F}$ | | 40 | μs | |
| LDO2 (PWR3) | | | | | | |
| V_{PWR3_VOUT} | Output Voltage PWR3_VOUT | | 2.5 | | V | |
| | Load Current capability | | 200 | | mA | |
| | DC Load regulation PWR3_VOUT | $V_{OUT} = 2.5\text{ V}$, $I_{OUT} = 5$ to 200 mA | | -70 | mV/A | |
| | DC Line regulation PWR3_VOUT | $V_{OUT} = 2.5\text{ V}$, $I_{OUT} = 5\text{ mA}$, $\text{PWR3_VIN} = 3.3$ to 20 V | | 30 | $\mu\text{V/V}$ | |
| LDO1 (PWR4) | | | | | | |
| V_{PWR4_VOUT} | Output Voltage PWR4_VOUT | | 3.3 | | V | |
| | Load Current capability | | 200 | | mA | |
| | DC Load regulation PWR4_VOUT | $V_{OUT} = 3.3\text{ V}$, $I_{OUT} = 5$ to 200 mA | | -70 | mV/A | |
| | DC Line regulation PWR4_VOUT | $V_{OUT} = 3.3\text{ V}$, $I_{OUT} = 5\text{ mA}$, $\text{PWR4_VIN} = 4$ to 20 V | | 30 | $\mu\text{V/V}$ | |
| | Regulator dropout | At 25 mA , $V_{OUT} = 3.3\text{ V}$, $V_{PWR4_VIN} = 3.3\text{ V}$ | | 48 | mV | |
| MEASUREMENT SYSTEM | | | | | | |
| AFE | | | | | | |
| G | Amplifier gain (PGA) | AFE_GAIN[1:0] = 01 | | 1 | V/V | |
| | | AFE_GAIN[1:0] = 10 | | 9.5 | | |
| | | AFE_GAIN[1:0] = 11 | | 18 | | |
| V_{OFS} | Input referred offset voltage | PGA, AFE_CAL_DIS = 1 ⁽²⁾ | | -1 | 1 | mV |
| | | Comparator ⁽²⁾ | | -1.5 | +1.5 | |
| τ_{RC} | Settling time | To 1% of final value ⁽²⁾ . | | 46 | 67 | μs |
| | | To 0.1% of final value ⁽²⁾ . | | 69 | 100 | |
| $V_{ACMPR_IN_1,2,3}$ | Input voltage Range ACMPR_IN_1,2,3 | | 0 | 1.5 | V | |
| LABB | | | | | | |
| τ_{RC} | Settling time | To 1% of final value ⁽²⁾ . | | 4.6 | 6.6 | μs |
| | | To 0.1% of final value ⁽²⁾ . | | 7 | 10 | |
| $V_{ACMPR_IN_LABB}$ | Input voltage range ACMPR_IN_LABB | | 0 | 1.5 | V | |
| | Sampling window ACMPR_IN_LABB | Programmable per $7\ \mu\text{s}$ | | 7 | 28 | μs |
| COLOR WHEEL PWM | | | | | | |
| CLK_OUT | Clock output frequency | | 2.25 | | MHz | |
| $V_{CW_SPEED_PWM_OUT}$ | Voltage range CW_SPEED_PWM_OUT | Average value programmable in 16 bits | | 0 | 5 | V |
| DIGITAL CONTROL - LOGIC LEVELS AND TIMING CHARACTERISTICS | | | | | | |
| V_{SPI} | SPI supply voltage range | SPI_VIN | | 1.7 | 3.6 | V |

Electrical Characteristics (continued)

Over operating free-air temperature range. $V_{IN} = 12\text{ V}$, $T_A = 0\text{ to }+70^\circ\text{C}$, typical values are at $T_A = 25^\circ\text{C}$, Configuration according to [Typical Application](#) ($V_{IN} = 12\text{ V}$, $I_{OUT} = 16\text{ A}$, LED, external FETs) (unless otherwise noted).

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|----------------------------|------------------------------------|--|----------------------|-----|----------------------|------------------|
| V_{OL} | Output low-level | RESETZ, CMP_OUT, CLK_OUT. $I_O = 0.3\text{ mA}$ sink current | 0 | | 0.3 | V |
| | | SPI_DOUT. $I_O = 5\text{ mA}$ sink current | 0 | | $0.3 \times V_{SPI}$ | |
| | | INTZ. $I_O = 1.5\text{ mA}$ sink current | 0 | | $0.3 \times V_{SPI}$ | |
| V_{OH} | Output high-level | RESETZ, CMP_OUT, CLK_OUT. $I_O = 0.3\text{ mA}$ source current | 1.3 | | 2.5 | V |
| | | SPI_DOUT. $I_O = 5\text{ mA}$ source current | $0.7 \times V_{SPI}$ | | V_{SPI} | |
| V_{IL} | Input low-level | PROJ_ON, LED_SEL0, LED_SEL1 | 0 | | 0.4 | V |
| | | SPI_CSZ, SPI_CLK, SPI_DIN | 0 | | $0.3 \times V_{SPI}$ | |
| V_{IH} | Input high-level | PROJ_ON, LED_SEL0, LED_SEL1 | 1.2 | | | V |
| | | SPI_CSZ, SPI_CLK, SPI_DIN | $0.7 \times V_{SPI}$ | | V_{SPI} | |
| I_{BIAS} | Input bias current | $V_{IO} = 3.3\text{ V}$, any digital input pin | | | 0.1 | μA |
| SPI_CLK | SPI clock frequency ⁽⁷⁾ | Normal SPI mode, DIG_SPI_FAST_SEL = 0, $f_{OSC} = 9\text{ MHz}$ | 0 | | 36 | MHz |
| | | Fast SPI mode, DIG_SPI_FAST_SEL = 1, $V_{SPI} > 2.3\text{ V}$, $f_{OSC} = 9\text{ MHz}$ | 20 | | 40 | |
| $t_{DEGLITCH}$ | Deglintch time | LED_SEL0, LED_SEL1 ⁽²⁾ . | | 300 | | ns |
| INTERNAL OSCILLATOR | | | | | | |
| f_{OSC} | Oscillator frequency | | | 9 | | MHz |
| | Frequency accuracy | $T_A = 0\text{ to }70^\circ\text{C}$ | -5% | | 5% | |
| THERMAL SHUTDOWN | | | | | | |
| T_{WARN} | Thermal warning (HOT threshold) | | | 120 | | $^\circ\text{C}$ |
| | Hysteresis | | | 10 | | |
| T_{SHTDWN} | Thermal shutdown (TSD threshold) | | | 150 | | $^\circ\text{C}$ |
| | Hysteresis | | | 15 | | |

(7) Maximum depends linearly on oscillator frequency f_{OSC} .

6.6 SPI Timing Parameters

$SPI_VIN = 3.6\text{ V} \pm 5\%$, $T_A = 0\text{ to }70^\circ\text{C}$, $C_L = 10\text{ pF}$ (unless otherwise noted).

| | | MIN | NOM | MAX | UNIT |
|------------|---|-----|-----|-----|------|
| f_{CLK} | Serial clock frequency | 0 | | 40 | MHz |
| t_{CLKL} | Pulse width low, SPI_CLK, 50% level | 10 | | | ns |
| t_{CLKH} | Pulse width high, SPI_CLK, 50% level | 10 | | | ns |
| t_t | Transition time, 20% to 80% level, all signals | 0.2 | | 4 | ns |
| t_{CSCR} | SPI_SS_Z falling to SPI_CLK rising, 50% level | 8 | | | ns |
| t_{CFCS} | SPI_CLK falling to SPI_CSZ rising, 50% level | | | 1 | ns |
| t_{CDS} | SPI_MOSI data setup time, 50% level | 7 | | | ns |
| t_{CDH} | SPI_MOSI data hold time, 50% level | 6 | | | ns |
| t_S | SPI_MISO data setup time, 50% level | 10 | | | ns |
| t_H | SPI_MISO data hold time, 50% level | 0 | | | ns |
| t_{CFDO} | SPI_CLK falling to SPI_MISO data valid, 50% level | | 13 | | ns |
| t_{CSZ} | SPI_CSZ rising to SPI_MISO HiZ | | 6 | | ns |

7 Detailed Description

7.1 Overview

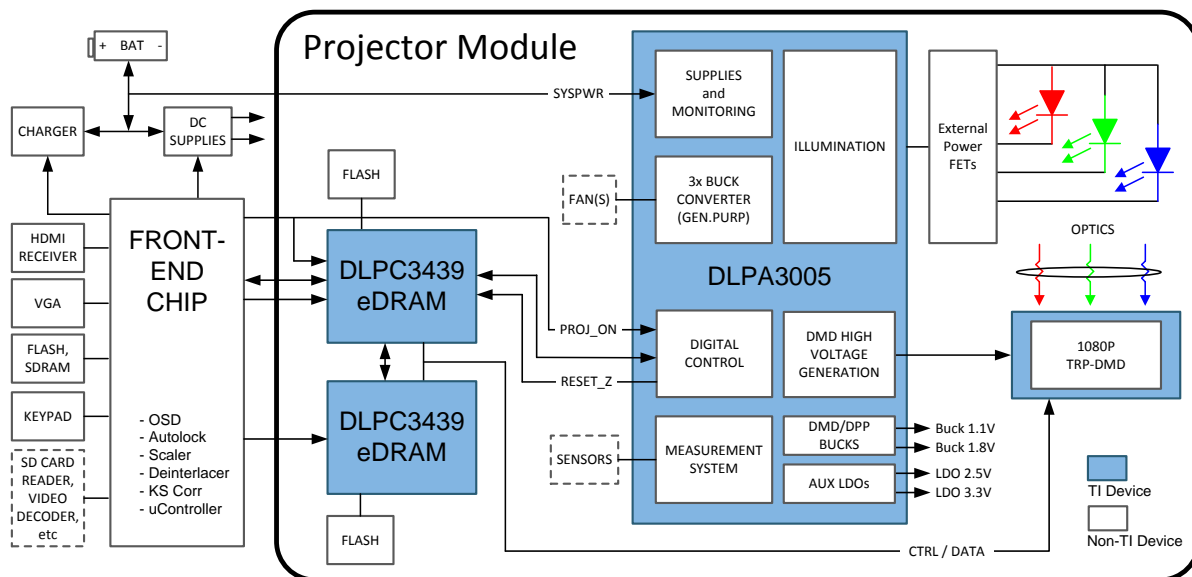
The DLPA3005 is a highly integrated power management IC optimized for DLP Pico Projector systems. It targets accessory applications up to several hundreds of lumen and is designed to support a wide variety of high-current LEDs. The Projector system supports the TRP type of digital mirror device (DMD). [Functional Block Description](#) shows a typical DLP Pico Projector implementation using the DLPA3005.

Part of the projector is the projector module, which is an optimized combination of components consisting of, for instance, DLPA3005, LEDs, DMD, DLPC chip, memory, and optional sensors and fans. The front-end chip controls the projector module. More information about the system and projector module configuration can be found in a separate application note.

Within the DLPA3005, several blocks can be distinguished. The blocks are listed below and subsequently discussed in detail:

- Supply and monitoring: Creates internal supply and reference voltages and has functions such as thermal protection and low battery warning
- Illumination: Block to control the light. Contains drivers, strobe decoder for the LEDs and power conversion
- External Power FETs: Capable for 16 A
- DMD: Generates voltages and their specific timing for the DMD. Contains regulators and DMD/DLPC buck converters
- Buck converters: General purpose buck converters
- Auxiliary LDOs: Fixed voltage LDOs for customer usage
- Measurement system: Analog front end to measure internal and external signals
- Digital control: SPI interface, digital control

7.2 Functional Block Description



7.3 Feature Description

7.3.1 Supply and Monitoring

This block takes care of creating several internal supply voltages and monitors correct behavior of the device.

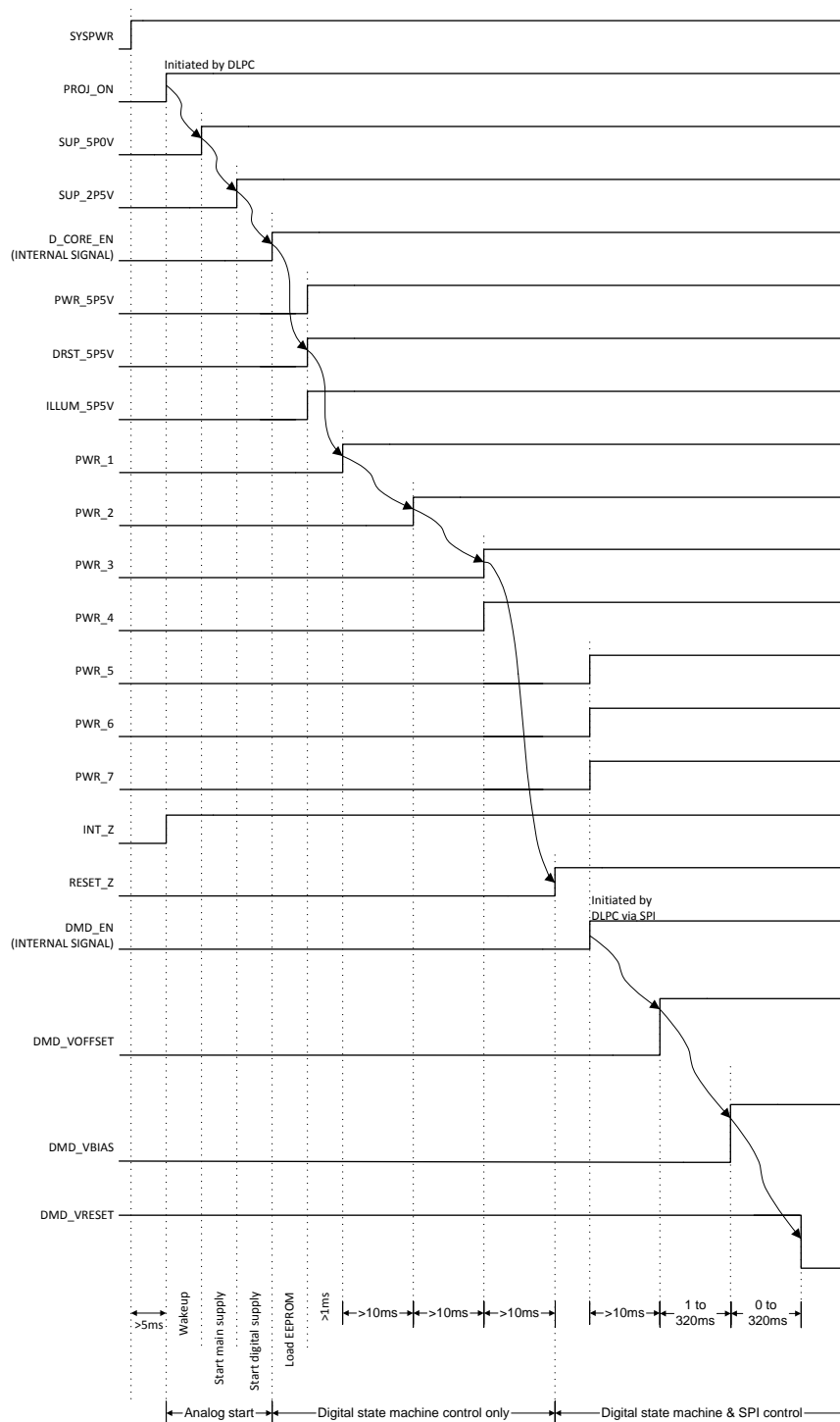
7.3.1.1 Supply

SYSPWR is the main supply of the DLPA3005. It can range from 6 V to 20 V, where the typical is 12 V. At power-up, several (internal) power supplies are started one after the other in order to make the system work correctly (Figure 1). A sequential startup ensures that all the different blocks start in a certain order and prevent excessive startup currents. The main control to start the DLPA3005 is the control pin *PROJ_ON*. Once set high the *basic* analog circuitry is started that is needed to operate the digital and SPI interface. This circuitry is supplied by two LDO regulators that generate 2.5 V (SUP_2P5V) and 5 V (SUP_5P0V). These regulator voltages are for internal use only and should not be loaded by an external application. The output capacitors of those LDOs should be 2.2 μ F for the 2.5-V LDO, and 4.7 μ F for the 5-V LDO, pin 91 and 92 respectively. Once these are up the digital core is started, and the DLPA3005 Digital State Machine (DSM) takes over.

Subsequently, the 5.5-V LDOs for various blocks are started: PWR_5V5V, DRST_5P5V and ILLUM_5P5V. Next, the buck converters and DMD LDOs are started (PWR_1 to PWR_4). The DLPA3005 is now awake and ready to be controlled by the DLPC (indicated by RESET_Z going high).

The general purpose buck converters (PWR_5 to 7) can be started (if used) as well as the regulator that supplies the DMD. The DMD regulator generates the timing critical VOFFSET, VBIAS, and VRESET supplies.

Feature Description (continued)



Note: Arrows indicate sequence of events automatically controlled by digital state machine. Other events are initiated under SPI control.

Figure 1. Powerup Timing

Feature Description (continued)

7.3.1.2 Monitoring

Several possible faults are monitored by the DLPA3005. If a fault has occurred and what kind of fault it is can be read in register 0x0C. Subsequently, an interrupt can be generated if such a fault occurs. The fault conditions for which an interrupt is generated can be configured individually in register 0x0D.

7.3.1.2.1 Block Faults

Fault conditions for several supplies can be observed such as the low voltage supplies (SUPPLY_FAULT). ILLUM_FAULT monitors correct supply and voltage levels in the illumination block and DMD_FAULT monitors a correct functioning DMD block. The PROJ_ON_INT bit indicates if PROJ_ON was asserted.

7.3.1.2.2 Low Battery and UVLO

Monitoring is also done on the battery voltage (input supply) by the low battery warning (BAT_LOW_WARN) and battery low shutdown (BAT_LOW_SHUT), [Figure 2](#). They warn for a low VIN supply voltage or automatically shutdown the DLPA3005 when the VIN supply drops below a predefined level respectively. The threshold levels for these fault conditions can be set from 3.9 V to 18.4 V by writing to registers 0x10<4:0> (LOWBATT) and 0x11<4:0> (BAT_LOW_SHUT_UVLO). These threshold levels have hysteresis. This hysteresis depends on the selected threshold voltage and is depicted in [Figure 3](#). It is recommended to set the low battery voltage higher than the under voltage lock out such that a warning is generated before the device goes into shutdown.

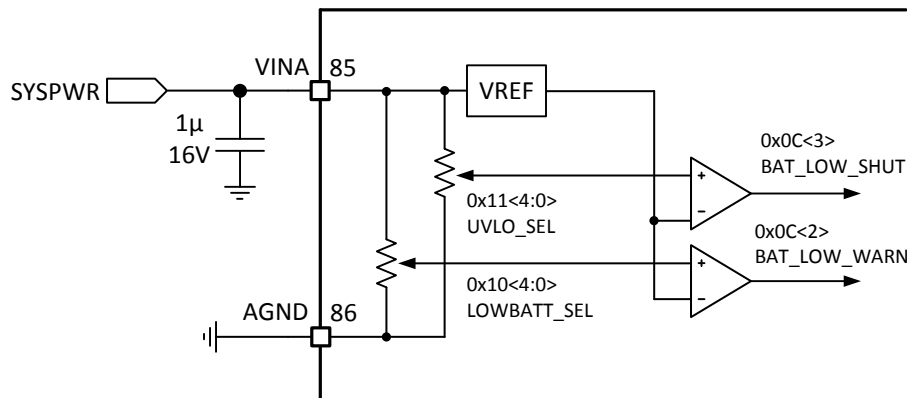


Figure 2. Battery Voltage Monitoring

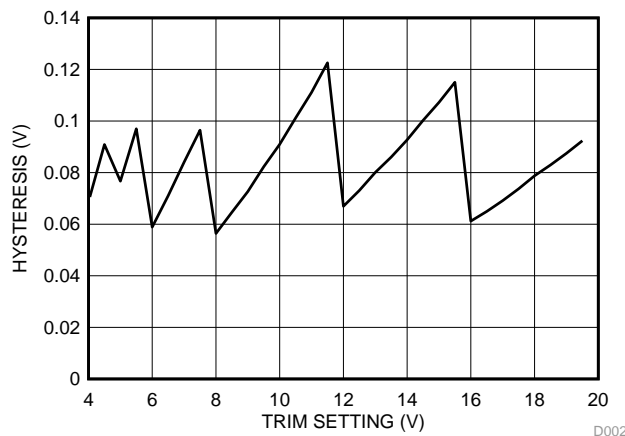


Figure 3. Hysteresis on V_{LOW_BAT} and V_{UVLO}

Feature Description (continued)

7.3.1.2.3 Auto LED Turn Off Functionality

The PAD devices can be supplied from either a battery pack or an adapter. The PAD devices use several warning and detection levels, as indicated in the previous paragraphs, to prevent system damage in case the supply voltage becomes too low or even interrupted.

Interruption of the supply voltage occurs when, for example, the adapter is switched to another mains outlet. In case a battery pack is installed, the system power control should switch at that moment to the battery pack. A change of supply voltage from, for example, 20 V to 8 V can occur, and thus the OVP level (which is ratio metric, see section [Ratio Metric Overvoltage Protection](#)) could become lower than V_{LED} . An OVP fault will be triggered and the system switches off.

The `Auto_LED_Turn_Off` functionality can be used to prevent the system from turning off in these circumstances. This function disables the LEDs when the supply voltage drops below `LED_AUTO_OFF_LEVEL` (reg 0x18h). It is advisable to have this level the same as the `BAT_LOW_WARN` level. When the `Auto_LED_Turn_Off` functionality is enabled (reg 0x01h), once a supply voltage drop is detected to below `LED_AUTO_OFF_LEVEL`, the LEDs will be switched off and the system should start sending lower current levels to have a lower V_{LED} . After start using lower currents, the LEDs can be switched on again by disabling `AUTO_LED_TURN_OFF` function. As a result the system can continue working at the lower supply voltage using a lower intensity. The system has to monitor the `BAT_LOW_WARN` status and once the mains adapter is plugged in again (seen by `BAT_LOW_WARN` being low), the `Auto_LED_Turn_Off` functionality can be enabled again. Now the LED currents can be restored to their original levels from before the supply voltage drop.

7.3.1.2.4 Thermal Protection

The chip temperature is monitored constantly to prevent overheating of the device. There are two levels of fault condition (register 0x0C). The first is to warn for overheating (`TS_WARN`). This is an indication that the chip temperature raises to a critical temperature. The next level of warning is `TS_SHUT`. This occurs at a higher temperature than `TS_WARN` and will shutdown the chip to prevent permanent damage. Both temperature faults have hysteresis on their levels to prevent rapid switching around the temperature threshold.

7.3.2 Illumination

The illumination function includes all blocks needed to generate light for the DLP system. In order to accurately set the current through the LEDs, a control loop is used ([Figure 4](#)). The intended LED current is set through `IDAC[9:0]`. The Illumination driver controls the LED anode voltage V_{LED} and as a result a current will flow through one of the LEDs. The LED current is measured via the voltage across sense resistor R_{LIM} . Based on the difference between the actual and intended current, the loop controls the output of the buck converter (V_{LED}) higher or lower. The LED which conducts the current is controlled by switches P, Q, and R. The *Openloop feedback circuitry* ensures that the control loop can be closed for cases when there is no path via the LED (for instance, when $I_{LED} = 0$).

Feature Description (continued)

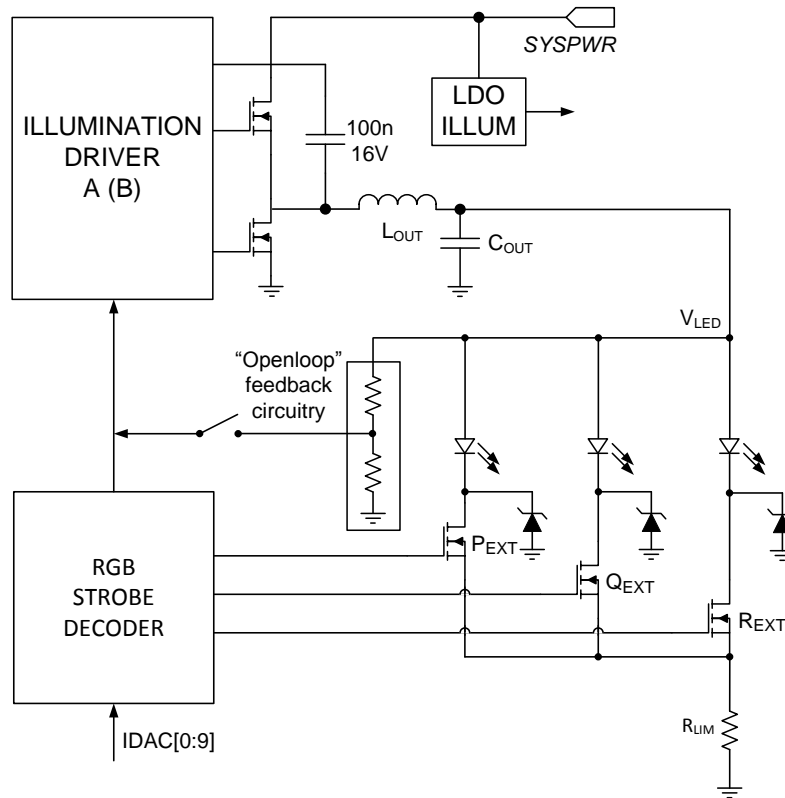


Figure 4. Illumination Control Loop

Within the illumination block, the following blocks can be distinguished:

- Programmable Gain Block
- LDO illum, analog supply voltage for internal illumination blocks
- Illumination driver A, primary driver for the external FETs
- Illumination driver B, secondary driver – for future purpose. Will not be discussed
- RGB stobe decoder, driver for external switches to control the on-off rhythm of the LEDs and measures the LED current

7.3.2.1 Programmable Gain Block

The current through the LEDs is determined by a digital number stored in the respective IDAC registers 0x03h to 0x08h. These registers determine the LED current which is measured through the sense resistor R_{LIM} . The voltage across R_{LIM} is compared with the current setting from the IDAC registers and the loop regulates the current to its set value.

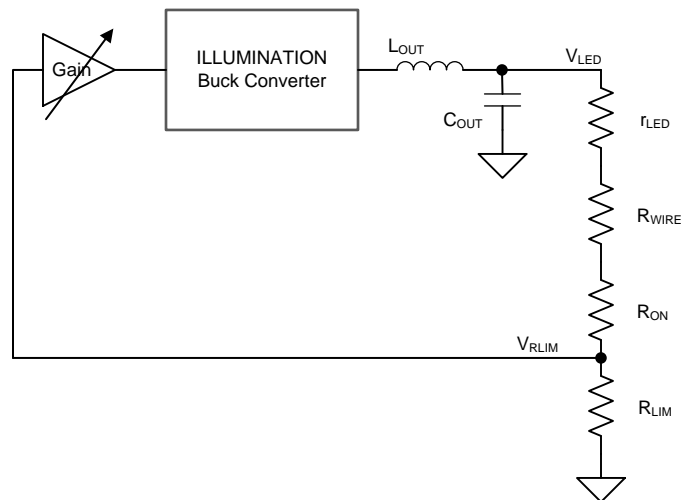
Feature Description (continued)


Figure 5. Programmable Gain Block in the Illumination Control Loop

When current is flowing through an LED, a forward voltage is built up over the LED. The LED also represents a (low) differential resistance which is part of the load circuit for V_{LED} . Together with the wire resistance (R_{WIRE}) and the R_{ON} resistance of the FET switch a voltage divider is created with R_{LIM} that is a factor in the loop gain of the ILED control. Under normal conditions, the loop is able to produce a well regulated LED current up to 16 Amps.

Since this voltage divider is part of the control loop, care must be taken while designing the system.

When, for instance, two LEDs in series are connected, or when a relatively high wiring resistance is present in the loop, the loop gain will reduce due to the extra attenuation caused by the increased series resistances of $r_{LED} + R_{WIRE} + R_{ON}$. As a result, the loop response time lowers. To compensate for this increased attenuation, the loop gain can be increased by selecting a higher gain for the programmable gain block. The gain increase can be set through register 0x25h [3:0].

Under normal circumstances the default gain setting (00h) is sufficient. In case of a series connection of two LEDs setting 01h or 02h might suffice.

As discussed before, wiring resistance also impacts the control-loop performance. It is advisable to prevent unnecessary large wire length in the loop. Keeping wiring resistance as low as possible is good for efficiency reasons. In case wiring resistance still impacts the response time of the loop, an appropriate setting of the gain block can be selected. The same goes for connector resistance and PCB tracks. Keep in mind that basically every milliohm counts. Following these precautions will help get a proper functioning of the I_{LED} current loop.

7.3.2.2 LDO Illumination

This regulator is dedicated to the illumination block and provides an analog supply of 5.5 V to the internal circuitry. It is recommended to use 1- μ F capacitors on both the input and output of the LDO.

7.3.2.3 Illumination Driver A

The illumination driver of the DLPA3005 is a buck controller for driving two external low-ohmic N-channel FETs (Figure 6). The theory of operation of a buck converter is explained in the application note *Understanding Buck Power Stages in Switchmode Power Supplies (SLVA057)*. For proper operation, selection of the external components is very important, especially the inductor L_{OUT} and the output capacitor C_{OUT} . For best efficiency and ripple performance, an inductor and capacitor should be chosen with low equivalent series resistance (ESR).

Feature Description (continued)

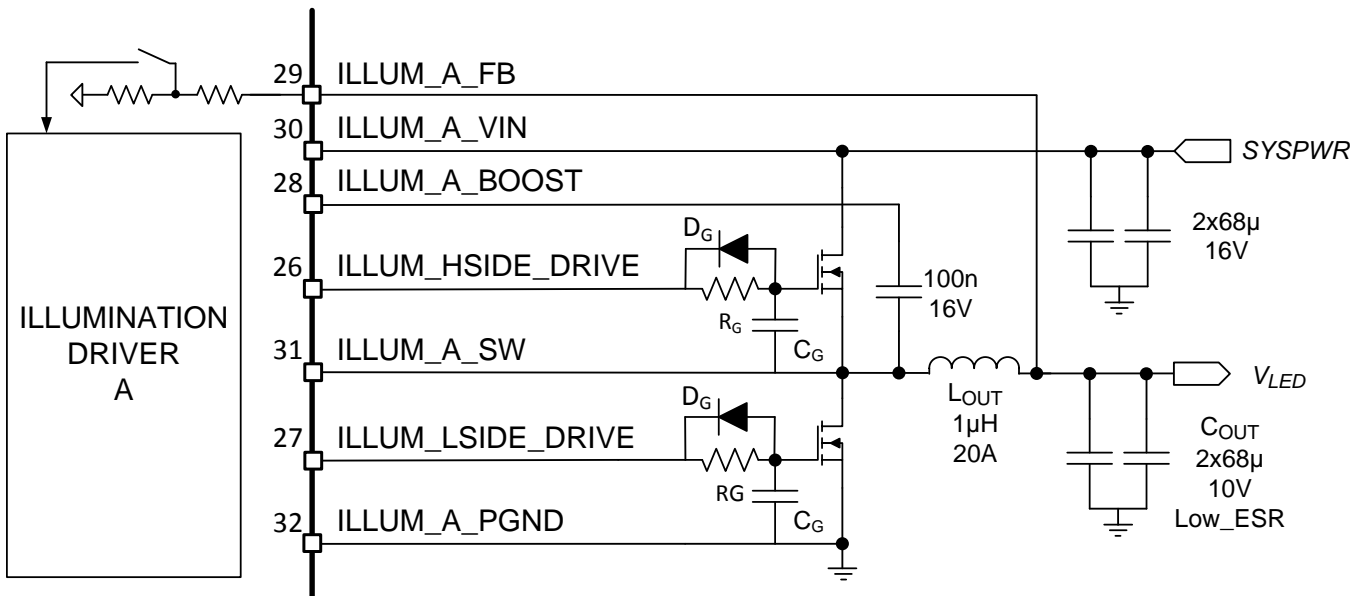


Figure 6. Typical Illumination Driver Configuration

Several factors determine the component selection of the buck converter, such as input voltage (SYSPWR), desired output voltage (V_{LED}) and the allowed output current ripple. Configuration starts with selecting the inductor L_{OUT} .

The value of the inductance of a buck power stage is selected such that the peak-to-peak ripple current flowing in the inductor stays within a certain range. Here, the target is set to have an inductor current ripple, k_{I_RIPPLE} , less than 0.3 (30%). The minimum inductor value can be calculated given the input and output voltage, output current, switching frequency of the buck converter ($f_{SWITCH} = 600$ kHz), and inductor ripple of 0.3 (30%):

$$L_{OUT} = \frac{V_{OUT}}{k_{I_RIPPLE} \cdot I_{OUT} \cdot f_{SWITCH}} \cdot (V_{IN} - V_{OUT}) \quad (1)$$

Example: $V_{IN} = 12$ V, $V_{OUT} = 4.3$ V, $I_{OUT} = 16$ A results in an inductor value of $L_{OUT} = 1$ μ H

Once the inductor is selected, the output capacitor C_{OUT} can be determined. The value is calculated using the fact that the frequency compensation of the illumination loop has been designed for an LC-tank resonance frequency of 15 kHz:

$$f_{RES} = \frac{1}{2 \cdot \pi \cdot \sqrt{L_{OUT} \cdot C_{OUT}}} = 15\text{kHz} \quad (2)$$

Example: $C_{OUT} = 110$ μ F given that $L_{OUT} = 1$ μ H. A practical value is 2×68 μ F. Here, a parallel connection of two capacitors is chosen to lower the ESR even further.

The selected inductor and capacitor determine the output voltage ripple. The resulting output voltage ripple V_{LED_RIPPLE} is a function of the inductor ripple k_{I_RIPPLE} , output current I_{OUT} , switching frequency f_{SWITCH} and the capacitor value C_{OUT} :

$$V_{LED_RIPPLE} = \frac{k_{I_RIPPLE} \cdot I_{OUT}}{8 \cdot f_{SWITCH} \cdot C_{OUT}} \quad (3)$$

Example: $k_{I_RIPPLE} = 0.3$, $I_{OUT} = 16$ A, $f_{SWITCH} = 600$ kHz and $C_{OUT} = 2 \times 68$ μ F results in an output voltage ripple of $V_{LED_RIPPLE} = 7$ mVpp

As can be seen, this is a relative small ripple.

Feature Description (continued)

It is strongly advised to keep the capacitance value low. The larger the capacitor value the more energy is stored. In case of a V_{LED} going down stored energy needs to be dissipated. This might result in a large discharge current. For a V_{LED} step down from V_1 to V_2 , while the LED current was I_1 . The theoretical peak reverse current is:

$$I_{2,MAX} = \sqrt{\frac{C_{OUT}}{L_{OUT}} \times (V_1^2 - V_2^2) + I_1^2} \quad (4)$$

Depending on the selected external FETs, the following three components might need to be added for each power FET:

- Gate series resistor (R_G)
- Gate series diode (D_G)
- Gate parallel capacitance (C_G)

It is advisable to have placeholders for these components in the board design.

The gate series resistors can be used to slow down the enable transient of the power FET. Since large currents are being switched, a fast transient implies a potential risk on ringing. Slowing down the turn-on transient reduces the edge steepness of the drain current and thus reduces the induced inductive ringing. A resistance of a few Ohm typically is sufficient.

The gate series resistance is also present in the turn-off transient of the power FET. This might have a negative effect on the non-overlap timing. In order to keep the turn-off transient of the power FET fast, a parallel diode with the gate series resistance can be used. The cathode of the diode should be directed to the DLPA3005 device in order have fast gate pull-down.

A third component that might be needed, depending on the specific configuration and FET selection, is an extra gate-source filter capacitance. Specifically for the higher supply voltages this capacitance is advisable. Due to a large drain voltage swing and the drain-gate capacitance, the gate of a disabled power FET might be pulled high parasitically.

For the low-side FET this can happen at the end of the non-overlap time while the power converter is supplying current. For that case the switch node is low at the end of the non-overlap time. Enabling the high-side FET pulls high the switch node. Due to the large and steep switch node edge, charge is being injected via the drain-gate capacitance of the low-side FET into the gate of the low-side FET. As a result the low-side FET can be enabled for a short period of time causing a shoot-through current.

For the high-side FET a dual case exists. If the power converter is discharging V_{LED} , the power converter current is directed inward and thus at the end of the non-overlap time the switch node is high. If at that moment the low-side FET is enabled, via the gate-drain capacitance of the high-side FET charge is being injected into the gate of the high-side FET potentially causing the device to switch on for a short amount of time. That will cause a shoot through current as well.

To reduce the effect of the charge injection via the drain-gate capacitance, an extra gate-source filter capacitance can be used. Assuming a linear voltage division between gate-source capacitance and gate-drain capacitance, for a 20V supply voltage the ratio of gate-source capacitance and gate-drain capacitance should be kept to about 1:10 or larger. It is advised to carefully test the gate-drive signals and the switch node for potential cross conduction.

Sometimes dual FETs are being used in order to spread out power dissipation (heat). In order to prevent parasitic gate-oscillation a structure as shown in [Figure 7](#) is suggested. Each gate is being isolated with R_{ISO} to damp potential oscillations. A resistance of 1 Ohm is typically sufficient.

Feature Description (continued)

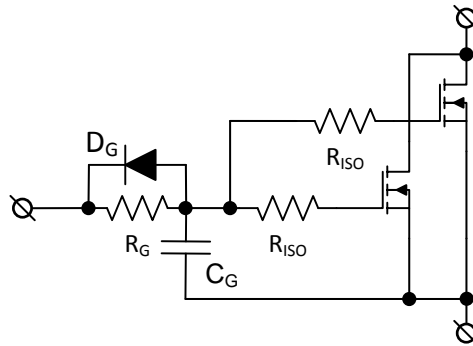


Figure 7. Using R_{ISO} to Prevent Gate Oscillations When Using Power FETs in Parallel

Finally two other components need to be selected in the buck converter. The value of the input-capacitor (pin ILLUM_A_VIN) should be equal or greater than the selected output capacitance C_{OUT} , in this case $\geq 2 \times 68 \mu F$. The capacitor between ILLUM_A_SWITCH and ILLUM_A_BOOST is a charge pump capacitor to drive the high side FET. The recommended value is 100 nF.

7.3.2.4 RGB Strobe Decoder

The DLPA3005 contains circuitry to sequentially control the three color-LEDs (red, green and blue). This circuitry consists of three drivers to control external switches, the actual strobe decoder and the LED current control (Figure 8). The NMOS switches are connected to the cathode terminals of the external LED package and turn the currents through the LEDs on and off.

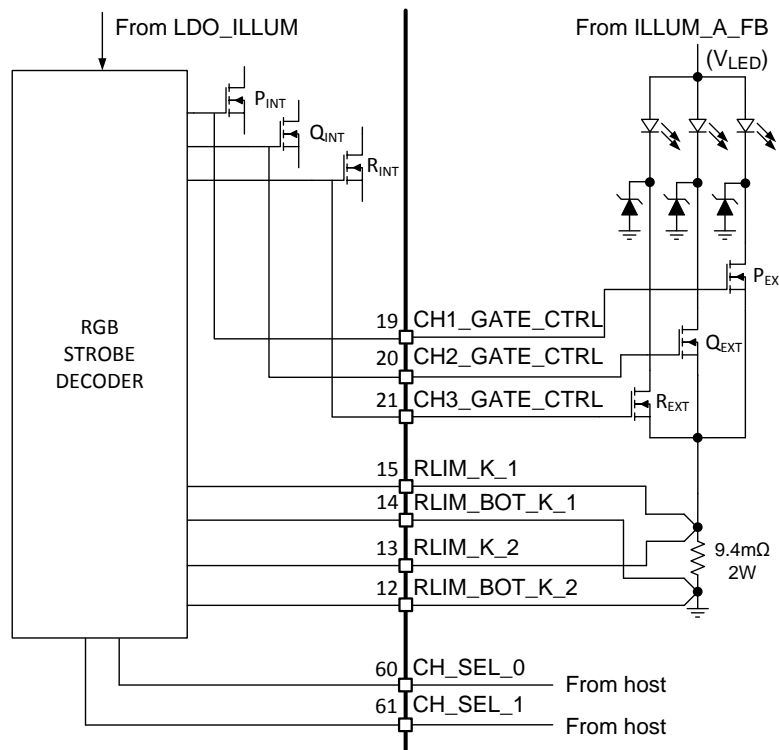


Figure 8. Switch Connection for a Common-Anode LED Assembly

The NMOS FET's P, Q, and R are controlled by the CH_SEL_0 and CH_SEL_1 pins. CH_SEL[1:0] typically receive a rotating code switching from RED to GREEN to BLUE and then back to RED. The relation between CH_SEL[0:1] and which switch is closed is indicated in Table 1.

Feature Description (continued)
Table 1. Switch Positions for Common Anode RGB LEDs

| PINS CH_SEL[1:0] | SWITCH | | | IDAC REGISTER |
|------------------|--------|--------|--------|-----------------------------|
| | P | Q | R | |
| 00 | Open | Open | Open | N/A |
| 01 | Closed | Open | Open | 0x03 and 0x04 SW1_IDAC[9:0] |
| 10 | Open | Closed | Open | 0x05 and 0x06 SW2_IDAC[9:0] |
| 11 | Open | Open | Closed | 0x07 and 0x08 SW3_IDAC[9:0] |

Besides enabling one of the switches, CH_SEL[1:0] also selects a 10-bit current setting for the control IDAC that is used as the set current for the LED. This set current together with the measured current through R_{LIM} is used to control the illumination driver to the appropriate V_{LED} . The current through the 3 LEDs can be set independently by registers 0x03 to 0x08 (Table 1).

Each current level can be set from *off* to $150mV/R_{LIM}$ in 1023 steps:

Led current(A) = 0 for bit value = 0

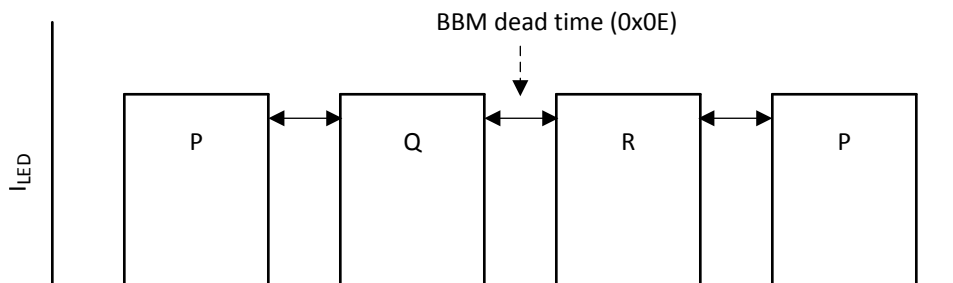
$$\text{Led current(A)} = \frac{\text{Bit value} + 1}{1024} \cdot \frac{150mV}{R_{LIM}} \text{ for bit value} = 1 \text{ to } 1023 \quad (5)$$

The maximum current for $R_{LIM} = 9.4 \text{ m}\Omega$ is thus 16 A.

For proper operation a minimum LED current of 5% of I_{LED_MAX} is required.

7.3.2.4.1 Break Before Make (BBM)

The switching of the three LED NMOS switches (P, Q, R) is controlled such that a switch is returned to the OPEN position first before the subsequent switch is set to the CLOSED position (BBM), Figure 9. The dead time between opening and closing switches is controlled through the BBM register (0x0E). Switches that already are in the CLOSED position and are to remain in the CLOSED state, are not opened during the BBM delay time.


Figure 9. BBM Timing
7.3.2.4.2 Openloop Voltage

Several situations exist in which the control loop for the buck converter through the LED is not present. In order to prevent the output voltage of the buck converter to “run-away”, the loop is closed by means of an internal resistive divider (see Figure 4 - Openloop feedback circuitry). Situations in which the openloop voltage control is active:

- During the BBM period. Transitions from one LED to another implies that during the BBM time all LEDs are off.
- Current setting for all three LEDs is 0.

It's advised to set the openloop voltage to about the lowest LED forward voltage. The openloop voltage can be set between 3 V and 18 V in steps of 1 V through register 0x18.

7.3.2.4.3 Transient Current Limit

Typically the forward voltages of the GREEN and BLUE diodes are close to each other (about 3 V to 5 V) however the forward voltage of the red diode is significantly lower (2 V to 4 V). This can lead to a current spike in the RED diode when the strobe controller switches from green or blue to red. This happens because V_{LED} is initially at a higher voltage than required to drive the red diode. DLPA3005 provides transient current limiting for each switch to limit the current in the LEDs during the transition. The transient current limit value is controlled via register 0x02 (ILLUM_ILIM). In a typical application it is required only for the RED diode. The value for ILLUM_ILIM should be set at least 20% higher than the DC regulation current. Register 0x02 (ILLUM_SW_ILIM_EN) contains three bits to select which switch employs the transient current limiting feature. The effect of the transient current limit on the LED current is shown in Figure 10.

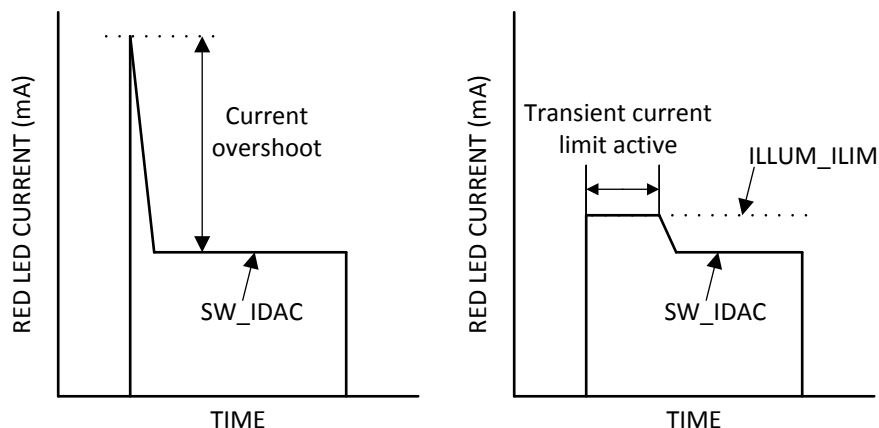


Figure 10. LED Current Without (Left) and With (Right) Transient Current Limit

7.3.2.5 Illumination Monitoring

The illumination block is continuously monitored for system failures to prevent damage to the DLPA3005 and LEDs. Several possible failures are monitored such as a broken control loop and a too high or too low output voltage V_{LED} . The overall illumination fault bit is in register 0x0C (ILLUM_FAULT). If any of the below failures occur, the ILLUM_FAULT bit may be set high:

- ILLUM_BC1_PG_FAULT
- ILLUM_BC1_OV_FAULT

Where, PG= Power Good and OV= Over Voltage

7.3.2.5.1 Power Good

Both the Illumination driver and the Illumination LDO have a power good indication. The power good for the driver indicates if the output voltage (V_{LED}) is within a defined window indicating that the LED current has reached the set point. If for some reason the LED current cannot be controlled to the intended value, this fault occurs. Subsequently, bit ILLUM_BC1_PG_FAULT in register 0x27 is set high. The illumination LDO output voltage is also monitored. When the power good of the LDO is asserted it implies that the LDO voltage is below a pre-defined minimum of 80% (rising) or 60% (falling) edge. The power good indication for the LDO is in register 0x27 (V5V5_LDO_ILLUM_PG_FAULT).

7.3.2.5.2 Ratio Metric Overvoltage Protection

The DLPA3005 illumination driver LED outputs are protected against open circuit use. In case no LED is connected and the PAD device is instructed to set the LED current to a specific level, the LED voltage (ILLUM_A_FB) will quickly rise and potentially rail to V_{IN} . This should be prevented. The OVP protection circuit triggers once V_{LED} crosses a predefined level. As a result the DLPA3005 will be switched off.

The same protection circuit is triggered in case the supply voltage (V_{INA}) will become too low to have the DLPA3005 work properly given the V_{LED} level. This protection circuit is constructed around a comparator that will sense both the LED voltage and the V_{INA} supply voltage. The fraction of the V_{INA} is connected to the minus input of the comparator while the fraction of the V_{LED} voltage is connected to the plus input. Triggering occurs when the plus input rises above the minus input and an OVP fault is set. The fraction of the V_{INA} must be set between 1 V and 4 V to ensure proper operation of the comparator.

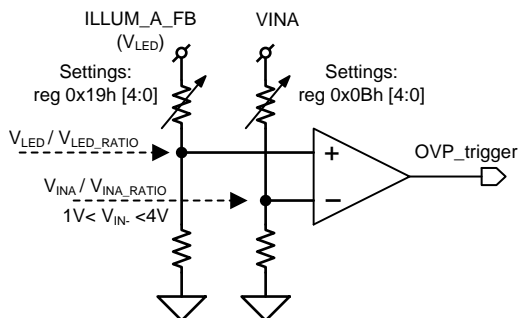


Figure 11. Ratio Metric OVP

The fraction of the ILLUM_A_FB voltage is set by the register 0x19h bits [4:0], while the setting of the fraction of the V_{INA} voltage is done by register 0x0Bh bits [4:0]. In general an OVP fault is set when

$$V_{LED}/V_{LED_RATIO} \geq V_{INA}/V_{INA_RATIO}$$

thus when:

$$V_{LED} \geq V_{INA} * V_{LED_RATIO}/V_{INA_RATIO}$$

Clearly, the OVP level is ratio-metric, i.e. can be set to a fixed fraction of V_{INA} .

For example: V_{LED} should stay below 85% of V_{INA} . The settings for the respective registers are:

reg 0x19h [4:0] = 01h (4.98)

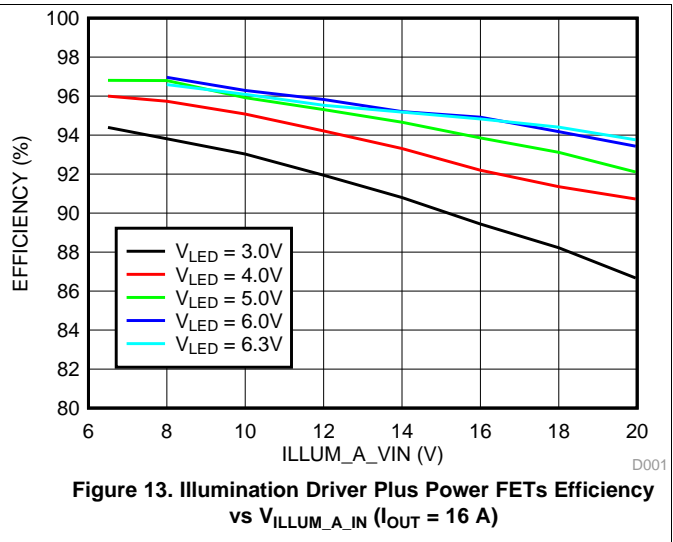
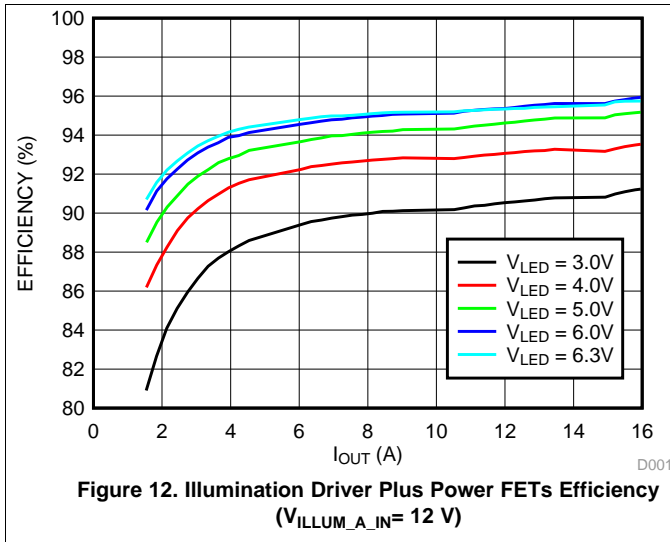
reg 0x0Bh [4:0] = 07h (5.85)

Resulting in: OVP triggers if $V_{LED} \geq V_{INA} * 4.98/5.85 = 0.85 V_{INA}$. Additionally for $V_{IN_RATIO} = 5.85$ the V_{IN-} input voltage for the comparator is between 1 V and 3.4 V for a supply voltage between 6 V and 20 V.

7.3.2.6 Illumination Driver plus Power FETs Efficiency

Below (Figure 12) an overview is given of the efficiency of the illumination driver plus power FETs for an input voltage of 12 V. Used external components (Figure 6): High-side FET (L) CDS17506Q5A, Low-side FET (M) CDS17501Q5A, $L_{OUT} = 2 \times 2.2 \mu H$ parallel, $C_{OUT} = 88 \mu F$. The efficiency is shown for several output voltage levels (V_{LED}) versus output current.

Figure 13 depict the efficiency versus input voltage ($V_{ILLUM_A_VIN}$) at various output voltage levels (V_{LED}) for an output current of 16 A.



7.3.3 External Power FET Selection

The DLPA3005 requires five external N-type Power FETs for proper operation. Two Power FETs are required for the illumination buck converter section (FETs L_{EXT} and M_{EXT} Figure 26) and three power FETs are required for the LED selection switches (FETs P_{EXT} , Q_{EXT} and R_{EXT} in Figure 26). This section discusses the selection criteria for these FETs to be taken into account:

- Threshold voltage
- Gate charge and gate timing
- $R_{DS(ON)}$

7.3.3.1 Threshold Voltage

The DLPA3005 has five drive outputs for the respective five power FETs. The signal swing at these outputs is about 5 V. Thus FETs should be selected that are turned on adequately with a gate-source voltage of 5 V. For the three LED selection outputs (CHx_GATE_CTRL) and the low-side drive ($ILLUM_LSIDE_DRIVE$), the drive signal is ground referred. For the $ILLUM_HSIDE_DRIVE$ output the signal swing is referred to the switch node of the converter, $ILLUM_A_SW$. All five power FETs should be N-type.

7.3.3.2 Gate Charge and Gate Timing

For power FETs a typically specified parameter is the total gate charge required to turn-on or turn-off the FET. The selection of the illumination buck-converter FETs with respect to their total gate charge is mainly relative to gate-source rise and fall times. For proper operation it is advised to have the gate-source rise and fall times maximum on the order of 20-30 ns. Given the typical high-side driver pull-up resistance of about 5 Ohm, an equivalent maximum gate capacitance of 4-6nF is appropriate. Since the gate-source swing is about 5 V, a total turn-on/off gate charge of maximum 20-30 nC is therefore advised.

The DPLA3005 has built-in non-overlap timing to prevent that both the high-side and low-side FET of the illumination buck converter are turned-on simultaneously. The typical non-overlap timing is about 35 ns. In most applications this should give sufficient margins. On top of this non-overlap timing the DLPA3005 measures the gate-source voltage of the external FETs to determine whether a FET is actually on or off. This measurement is done at the pins of the DLPA3005. For the low-side FET this measurement is done between $ILLUM_LSIDE_DRIVE$ and $ILLUM_A_GND$. Similarly, for the high-side FET the gate-source voltage is measured between $ILLUM_HSIDE_DRIVE$ and $ILLUM_A_SW$. The location of these measurement nodes imply that at all times no additional drivers or circuitry should be inserted between the DLPA3005 and the external power FETs of the buck converter. Inserting circuitry (delays) could potentially lead to incorrect on-off detection of the FETs and cause shoot-through currents. These shoot-through currents are negatively affecting the efficiency, but more seriously can potentially damage the power FETs.

For the LED selection switches no specific selection criteria are present on gate charge / timing. This is because the timing of the LED selection signals is in the microsecond range rather than nanosecond range.

7.3.3.3 $R_{DS(ON)}$

The selection of the FET relative to its drain-source on-resistance, $R_{DS(ON)}$, has two aspects. Firstly, for the high-side FET of the illumination buck-converter the $R_{DS(ON)}$ is a factor in the over-current detection. Secondly, for the other four FETs the power dissipation drives the choice of the FETs $R_{DS(ON)}$.

In order to detect an over-current situation, the DLPA3005 measures the drain-source voltage drop of the high-side FET when turned on. The over-current detection circuit triggers, and switches off the high-side FET, when the threshold $V_{DC-Th} = 185$ mV (typical) is reached. Therefore, the actual current, I_{OC} , at which this over-current detection triggers is given by:

$$I_{OC} = \frac{V_{DC-Th}}{R_{DS(ON)}} = \frac{185 \text{ mV}}{R_{DS(ON)}} \quad (6)$$

Note that the $R_{DS(ON)}$ should be taken from the FET datasheet at high-temp, i.e. at over-current the FETs will likely be hot.

For example, the CSD17510Q5A NexFET has an $R_{DS(ON)}$ of 7 mOhm at 125 °C. Using this FET will result in an over-current level of 26 A. This FET would be a good choice for a 16 A application.

For the low-side FET and the three LED selection FETs the $R_{DS(ON)}$ selection is mainly governed by the power dissipation due to conduction losses. The power dissipated in these FETs is given by:

$$P_{DISS} = \int_t I_{DS}^2(t) R_{DS(ON)} \quad (7)$$

In which I_{DS} is the current running through the respective FET. Clearly, the lower the $R_{DS(ON)}$ the lower the dissipation is.

For example, the CSD17501Q5A has $R_{DS(ON)} = 3$ mOhm. For a drain-source current of 16 A with a duty cycle of 25% (assuming the FET is used as LED selection switch) the dissipation is about 0.2 W in this FET.

7.3.4 DMD Supplies

This block contains all the supplies needed for the DMD and DLPC (Figure 14). The block comprises:

- LDO_DMD: for internal supply
- DMD_HV: regulator generates high voltage supplies
- Two buck converters: for DLPC/DMD voltages

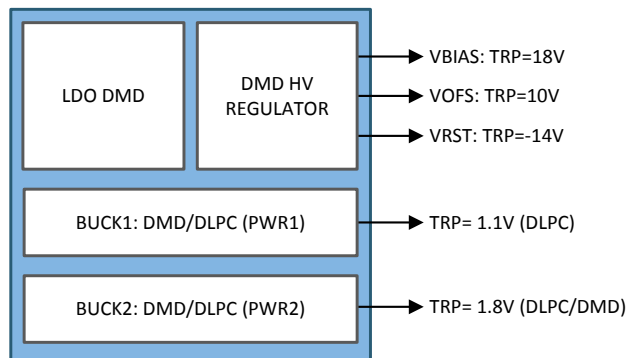


Figure 14. DMD Supplies Blocks

The DMD supplies block is designed to work with the TRP-type DMD and the related DLPC. The TRP-type DMD has its own set of supply voltage requirements. Besides the three high voltages, two supplies are needed for the DMD and the related DLPC (DLPC343x-family for instance). These supplies are made by two buck converters.

The EEPROM of the DLPA3005 is factory programmed for a certain configuration, such as which buck converters are used. Which configuration is programmed in EEPROM can be read in the capability register 0x26. It concerns the following bits:

- DMD_BUCK1_USE
- DMD_BUCK2_USE

A description of the function of these capability bits can be found in the register map, register 0x26.

7.3.4.1 LDO DMD

This regulator is dedicated to the DMD supplies block and provides an analog supply voltage of 5.5 V to the internal circuitry.

7.3.4.2 DMD HV Regulator

The DMD HV regulator generates three high voltage supplies: DMD_VRESET, DMD_VBIAS, and DMD_VOFFSET (Figure 15). The DMD HV regulator uses a switching regulator (switch A-D), where the inductor is time shared between all three supplies. The inductor is charged up to a certain current value (current limit) and then discharged into one of the three supplies. If not all supplies need charging the time available will be equally shared between those that do need charging.

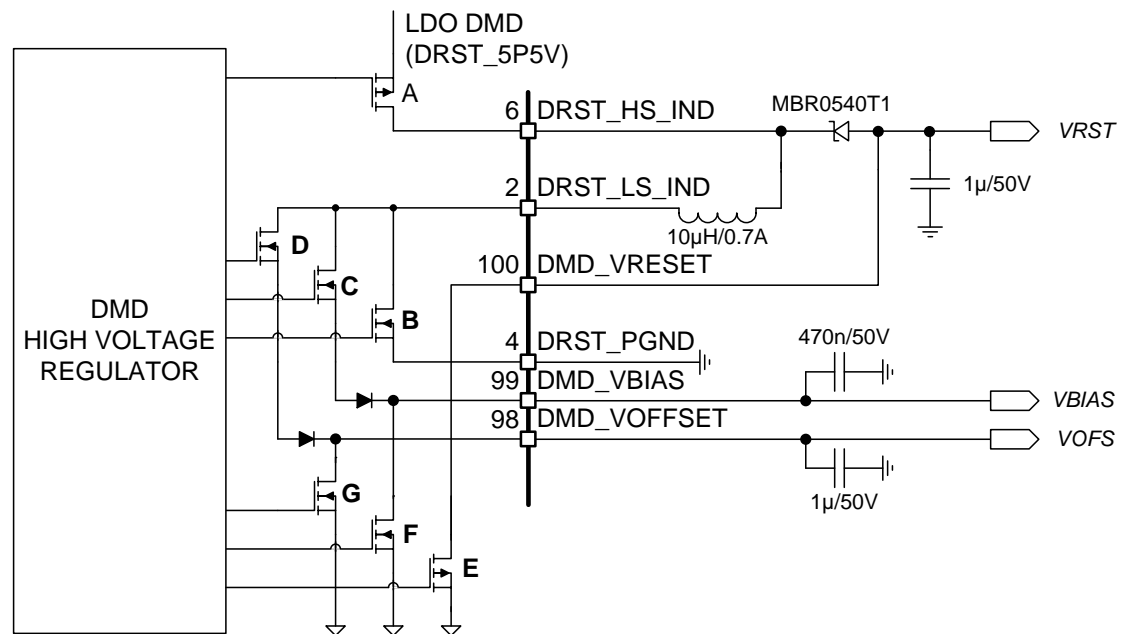


Figure 15. DMD High Voltage Regulator

7.3.4.3 DMD/DLPC Buck Converters

Each of the 2 DMD buck converters creates a supply voltage for the DMD and/ or DLPC. The values of the voltages for the TRP-type of DMD and DLPC used, for instance:

- TRP DMD+DLPC3439: 1.1 V (DLPC) and 1.8 V (DLPC/DMD)

The topology of the buck converters is the same as the general purpose buck converters discussed later in this document. How to configure the inductor and capacitor will be discussed in [Buck Converters](#).

A typical configuration is 3.3 µH for the inductor and 2x 22 µF for the output capacitor.

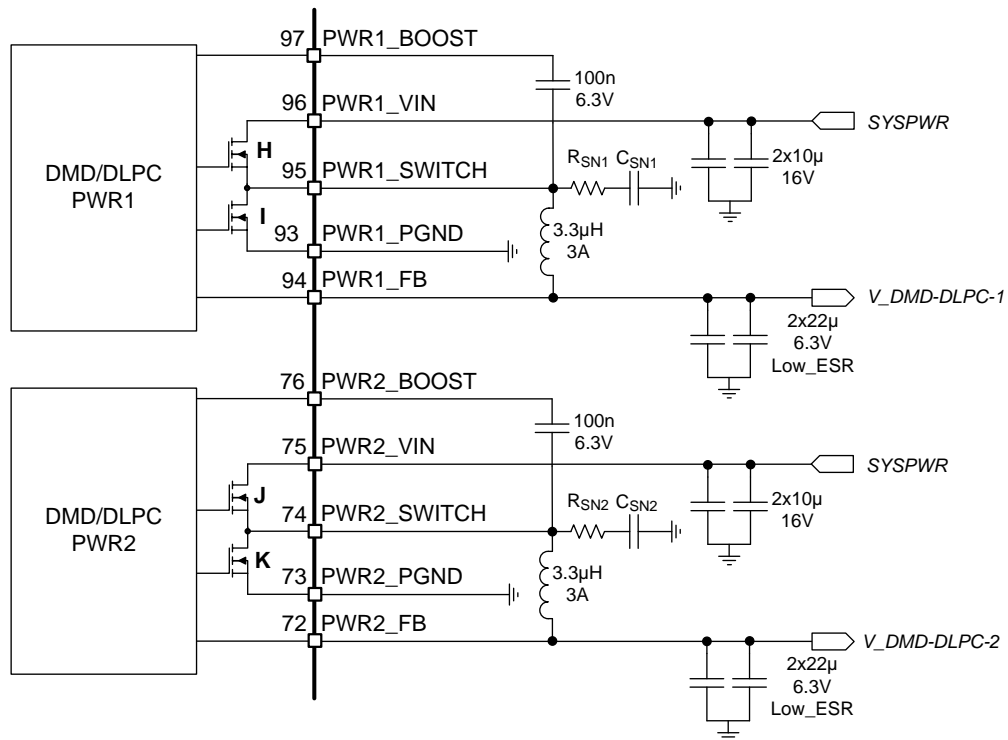


Figure 16. DMD/DLPC Buck Converters

7.3.4.4 DMD Monitoring

The DMD block is continuously monitored for failures to prevent damage to the DLPA3005 and/ or the DMD. Several possible failures are monitored such that the DMD voltages can be ensured. Failures could be for instance a broken control loop or a too high or too low converter output voltage. The overall DMD fault bit is in register 0x0C, DMD_FAULT. If any of the failures in [Table 2](#) occur, the DMD_FAULT bit will be set high.

Table 2. DMD FAULT Indication

| POWER GOOD (REGISTER 0x29) | | |
|------------------------------|---|--|
| BLOCK | REGISTER BIT | THRESHOLD |
| HV Regulator | DMD_PG_FAULT | DMD_RESET: 90%, DMD_OFFSET and DMD_VBIAS: 86% rising, 66% falling |
| PWR1 | BUCK_DMD1_PG_FAULT | Ratio: 72% |
| PWR2 | BUCK_DMD2_PG_FAULT | Ratio: 72% |
| PWR3 (LDO_2) | LDO_GP2_PG_FAULT / LDO_DMD1_PG_FAULT | 80% rising, 60% falling |
| PWR4 (LDO_1) | LDO_GP1_PG_FAULT / LDO_DMD1_PG_FAULT | 80% rising, 60% falling |
| OVER-VOLTAGE (REGISTER 0x2A) | | |
| BLOCK | REGISTER BIT | THRESHOLD (V) |
| PWR1 | BUCK_DMD1_OV_FAULT | Ratio: 120% |
| PWR2 | BUCK_DMD2_OV_FAULT | Ratio: 120% |
| PWR3 (LDO_2) | LDO_GP2_OV_FAULT / LDO_DMD1_OV_FAULT | 7 |
| PWR4 (LDO_1) | LDO_GP1_OV_FAULT / LDO_DMD1_OV_FAULT | 7 |

7.3.4.4.1 Power Good

The DMD HV regulator, DMD buck converters, DMD LDOs, and the LDO_DMD that supports the HV regulator, all have a power good indication.

The DMD HV regulator is continuously monitored to check if the output rails DMD_RESET, DMD_VOFFSET and DMD_VBIAS are in regulation. If either one of the output rails drops out of regulation (e.g due to a shorted output or overloading) the DMD_PG_FAULT bit in register 0x29 is set. Threshold for DMD_RESET is 90% and the thresholds for DMD_OFFSET/ DMD_VBIAS are 86% (rising edge) and 66% (falling edge).

The power good signal for the two DMD buck converters indicate if their output voltage (PWR1_FB and PWR2_FB) are within a defined window. The relative power good ratio is 72%. This means that if the output voltage is below 72% of the set output voltage the power good bit is asserted. The power good bits are in register 0x29, BUCK_DMD1_PG_FAULT and BUCK_DMD2_PG_FAULT.

DMD_LDO1 and DMD_LDO2 output voltages are also monitored. When the power good fault of the LDO is asserted it implies that the LDO voltage is below 80% (rising edge) or 60% (falling edge) of its intended value. The power good indication for the LDOs is in register 0x29, LDO_GP1_PG_FAULT / LDO_DMD1_PG_FAULT and LDO_GP2_PG_FAULT / LDO_DMD2_PG_FAULT.

The LDO_DMD used for the DMD HV regulator has its own power good signaling. The power good fault of the LDO_DMD is asserted if the LDO voltage is below 80% (rising edge) or 60% (falling edge) of its intended value. The power good indication for this LDO is in register 0x29, V5V5_LDO_DMD_PG_FAULT.

7.3.4.4.2 Overvoltage Fault

An overvoltage fault occurs when an output voltage rises above a pre-defined threshold. Overvoltage faults are indicated for the DMD buck converters, DMD LDOs and the LDO_DMD supporting the DMD HV regulator. The overvoltage fault of LDO1 and LDO2 are not incorporated in the overall DMD_FAULT when the LDOs are used as general purpose LDOs. [Table 2](#) provides an overview of the possible DMD overvoltage faults and their threshold levels.

7.3.5 Buck Converters

The DLPA3005 contains three general purpose buck converters and a supporting LDO (LDO_BUCKS). The three programmable 8-bit buck converters can generate a voltage between 1 V and 5 V and have an output current limit of 3 A. General Purpose Buck2 (PWR6) currently supported, others may be available in the future. One of the buck converters and the LDO_BUCKS is depicted in [Figure 17](#)

The two DMD/DLPC buck converters discussed earlier in [DMD Supplies](#) have the same architecture as these three buck converters and can be configured in the same way.

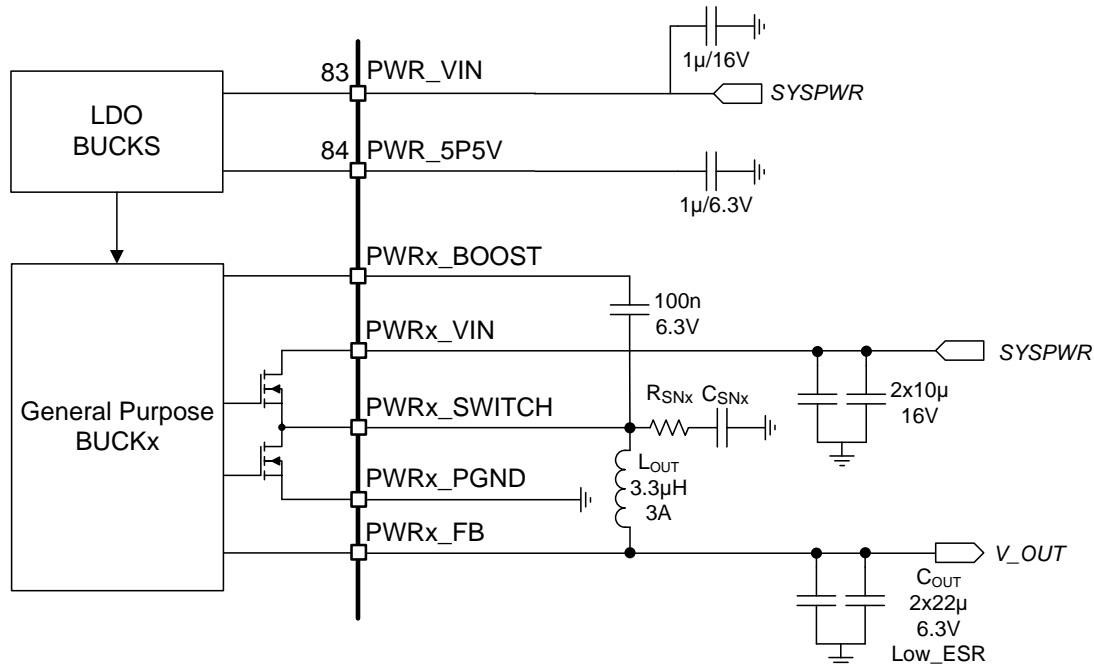


Figure 17. Buck Converter

7.3.5.1 LDO Bucks

This regulator supports the 3 general purpose buck converters and the 2 DMD/DLPC buck converters and provides an analog voltage of 5.5 V to the internal circuitry.

7.3.5.2 General Purpose Buck Converters

The 3 Buck converters are for general purpose usage ([Figure 17](#)). Each of the converters can be enabled or disabled via register 0x01 bit:

- BUCK_GP1_EN
- BUCK_GP2_EN
- BUCK_GP3_EN

The output voltages of the converters are configurable between 1 V and 5 V with an 8-bit resolution. This can be done via register 0x13, 0x14 and 0x15.

General Purpose Buck2 (PWR6) has a current capability of 2 A. Other General Purpose Buck converters (PWR5,7) are not supported at this time, they may become available in the future.

The buck converters can operate in two switching modes: Normal, 600 kHz switching frequency, mode and the skip mode. The skip mode is designed to increase light load efficiency. As the output current decreases from heavy load condition, the inductor current is also reduced and eventually comes to point that its rippled valley touches zero level, which is the boundary between continuous conduction and discontinuous conduction modes. The rectifying MOSFET is turned off when its zero inductor current is detected. As the load current further decreases the converter run into discontinuous conduction mode. The on-time is kept almost the same as it was in the continuous conduction mode so that it takes longer time to discharge the output capacitor with smaller load current to the level of the reference voltage. The skip mode can be enabled/disabled per buck converter in register 0x16.

7.3.5.3 Buck Converter Monitoring

The buck converter block is continuously monitored for system failures to prevent damage to the DLPA3005 and peripherals. Several possible failures are monitored such as a too high or too low output voltage. The possible faults are summarized in [Table 3](#).

Table 3. Buck Converter Fault Indication

| POWER GOOD (REGISTER 0X27) | | |
|-----------------------------|-------------------|-------------------------|
| BLOCK | REGISTER BIT | THRESHOLD (RISING EDGE) |
| Gen.Buck1 | BUCK_GP1_PG_FAULT | Ratio 72% |
| Gen.Buck2 | BUCK_GP2_PG_FAULT | Ratio 72% |
| Gen.Buck3 | BUCK_GP3_PG_FAULT | Ratio 72% |
| OVERVOLTAGE (REGISTER 0X28) | | |
| Gen.Buck1 | BUCK_GP1_OV_FAULT | Ratio 120% |
| Gen.Buck2 | BUCK_GP2_OV_FAULT | Ratio 120% |
| Gen.Buck3 | BUCK_GP3_OV_FAULT | Ratio 120% |

7.3.5.3.1 Power Good

The buck converters as well as the supporting LDO_BUCK have a power good indication. Each buck converter has a separate indication.

The power good for the three buck converters indicate if their output voltage (PWR5,6,7_FB) is within a defined window. The relative power good ratio is 72%. This means that if the output voltage is below 72% of the set voltage the PG_fault bit is set high. The power good bits of the buck converters are in register 0x27 bit:

- BUCK_GP1_PG_FAULT for BUCK1 (PWR5)
- BUCK_GP2_PG_FAULT for BUCK2 (PWR6)
- BUCK_GP3_PG_FAULT for BUCK3 (PWR7)

The LDO_BUCKS that supports the buck converters has its own power good indication. The power good of the LDO_BUCKS is asserted if the LDO voltage is below 80% (rising edge) or 60% (falling edge) of its intended value. The power good indication for the LDO_BUCKS is in register 0x29, V5V5_LDO_BUCK_PG_FAULT.

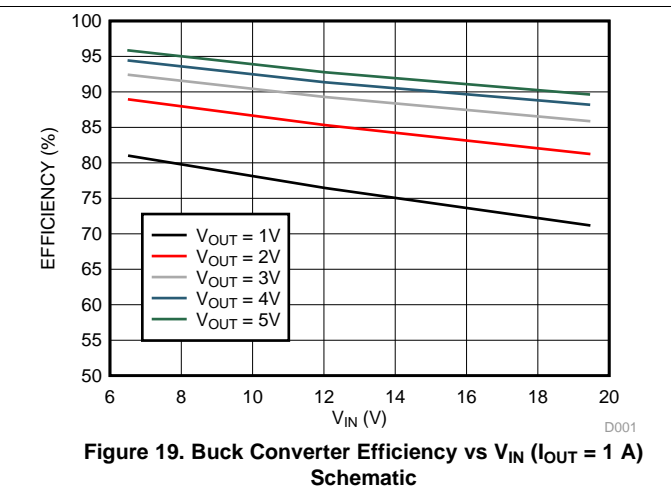
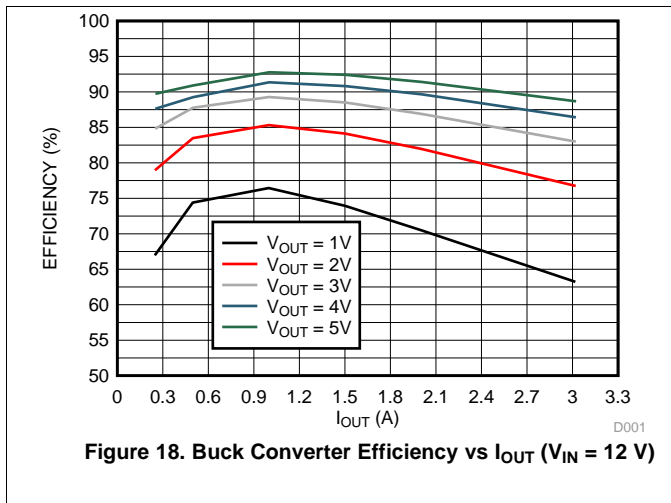
7.3.5.3.2 Overvoltage Fault

An over-voltage fault occurs when an output voltage rises above a pre-defined threshold. Over-voltage faults are indicated for the buck converters, and LDO_BUCKS. The over-voltage fault of the LDO_BUCKS is asserted if the LDO voltage is above 7.2 V and can be found in register 0x2A, V5V5_LDO_BUCK_OV_FAULT. The over-voltage of the general purpose buck converters is 120% of the set value and can be read via register 0x28, BUCK_GP1,2,3_OV_FAULT.

7.3.5.4 Buck Converter Efficiency

[Figure 18](#) shows an overview of the efficiency of the buck converter for an input voltage of 12 V. The efficiency is shown for several output voltage levels where the load current is swept.

[Figure 19](#) depicts the buck converter efficiency versus input voltage (V_{IN}) for a load current (I_{OUT}) of 1 A for various output voltage levels (V_{OUT}).



7.3.6 Auxiliary LDOs

LDO_1 and LDO_2 are the two auxiliary LDOs that can freely be used by an additional external application. All other LDOs are for internal usage only and should not be loaded. LDO1 (PWR4) is a fixed voltage of 3.3 V, while LDO2 (PWR3) is a fixed voltage of 2.5 V. Both LDOs are capable to deliver 200 mA.

7.3.7 Measurement System

The measurement system (Figure 20) is designed to sense internal and external nodes and convert them to digital by the implemented AFE comparator. The AFE can be enabled via register 0x0A, AFE_EN. The reference signal for this comparator, ACMPR_REF, is a low pass filtered PWM signal coming from the DLPC. To be able to cover a wide range of input signals a variable gain amplifier (VGA) is added with 3 gain settings (1x, 9.5x, and 18x). The gain of the VGA can be set via register 0x0A, AFE_GAIN. The maximum input voltage of the VGA is 1.5 V. Some of the internal voltage are too large though to be handled by the VGA and are divided down first.

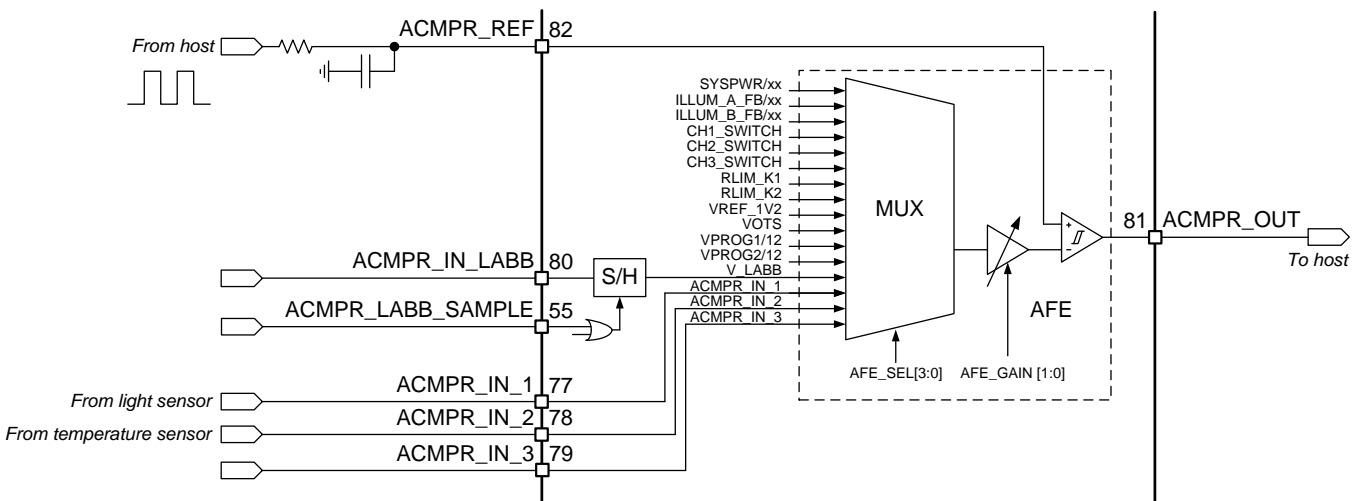


Figure 20. Measurement System Schematic

The multiplexer (MUX) connects to a wide range of nodes. Selection of the MUX input can be done via register 0X0A, AFE_SEL. Signals that can be selected:

- System input voltage, SYSPWR
- LED anode cathode voltage, ILLUM_A_FB
- LED cathode voltage, CHx_SWITCH
- $V_{R_{LIM}}$ to measure LED current

- Internal reference, VREF_1V2
- Die Temperature represented by voltage VOTS
- EEPROM programming voltage, VPROG1,2/12
- LABB sensor, V_LABB
- External sense pins, ACMPR_IN_1,2,3

The system input voltage SYSPWR can be measured by selecting the SYSPWR/xx input of the MUX. Before the system input voltage is supplied to the MUX the voltage needs to be divided. This is because the variable gain amplifier (VGA) can handle voltages up-to 1.5 V whereas the system voltage can be as high as 20 V. The division is done internally in the DLPA3005. The division factor selection (VIN division factor) is combined with the auto LED turn off functionality of the illumination driver and can be set via register 0x18, ILLUM_LED_AUTO_OFF_SEL.

The LED voltages can be monitored by measuring both the common anode of the LEDs as well as the cathode of each LED individually. The LED anode voltage (V_{LED}) is measured by sensing the feedback pin of the illumination driver (ILLUM_A_FB). Likewise the SYSPWR, the LED anode voltage needs to be divided before feeding it to the MUX. The division factor is combined with the over-voltage fault level of the illumination driver and can be set via register 0x19, VLED_OVP_VLED_RATIO. The cathode voltages CH1,2,3_SWITCH are fed directly to the MUX without division factor.

The LED current can be determined knowing the value of sense resistor R_{LIM} and the voltage across the resistor. The voltage at the top-side of the sense resistor can be measured via selecting MUX-input RLIM_K1. The bottom-side of the resistor is connected to GND.

VOTS is connected to an on-chip temperature sensor. The voltage is a measure for the chip's junction temperature: $Temperature (^{\circ}C) = 300 \times VOTS (V) - 270$

For storage of trim bits, but also for the USER EEPROM bytes (0x30 to 0x35), the DLPA3005 has two EEPROM blocks. The programming voltage of EEPROM block 1 and 2 can be measured via MUX input VPROG1/12 and VPROG2/12 respectively. The EEPROM programming voltage is divided by 12 before it is supplied to the MUX to prevent a too large voltage on the MUX input. The EEPROM programming voltage is ~12 V.

LABB is a feature that stands for Local Area Brightness Boost. LABB locally increases the brightness while maintaining good contrast and saturation. The sensor needed for this feature should be connected to pin ACMPR_IN_LABB. The light sensor signal is sampled and held such that it can be read independently of the sensor timing. To use this feature it should be ensured that:

- The AFE block is enabled (0x0A, AFE_EN = 1)
- The LABB input is selected (0x0A, AFE_SEL<3:0>=3h)
- The AFE gain is set appropriately to have $AFE_Gain \times VLABB < 1.5 V$ (0x0A, AFE_GAIN<1:0>)

Sampling of the signal can be done via one of the following methods:

1. Writing to register 0x0B by specifying the sample time window (TSAMPLE_SEL) and set bit SAMPLE_LABB=1 to start sampling. The SAMPLE_LABB bit in register 0x0B is automatically reset to 0 at the end of the sample period to be ready for a next sample request.
2. Use the input ACMPR_LABB_SAMPLE-pin as a sample signal. As long as this signal is high the signal on ACMPR_IN_LABB is tracked. Once the ACMPR_LABB_SAMPLE is set low again the value at that moment will be held.

ACMPR_IN_1,2,3 can measure external signals from for instance a light sensor or a temperature sensor. It should be ensured that the voltage on the input doesn't exceed 1.5 V.

7.4 Device Functional Modes

Table 4. Modes of Operation

| MODE | DESCRIPTION |
|------|--|
| OFF | This is the lowest-power mode of operation. All power functions are turned off, registers are reset to their default values, and the IC does not respond to SPI commands. RESET_Z pin is pulled low. The IC will enter OFF mode whenever the PROJ_ON pin is low. |

Device Functional Modes (continued)
Table 4. Modes of Operation (continued)

| MODE | DESCRIPTION |
|---------|--|
| WAIT | The DMD regulators and LED power (V_{LED}) are turned off, but the IC does respond to the SPI. The device enters WAIT mode whenever PROJ_ON is set high, DMD_EN ⁽¹⁾ bit is set to 0 or a FAULT is resolved. |
| STANDBY | The device also enters STANDBY mode when a fault condition is detected ⁽²⁾ . (See also section Interrupt). Once the fault condition is resolved, WAIT mode is entered. |
| ACTIVE1 | The DMD supplies are enabled but LED power (V_{LED}) is disabled. PROJ_ON pin must be high, DMD_EN bit must be set to 1, and ILLUM_EN ⁽³⁾ bit is set to 0. |
| ACTIVE2 | DMD supplies and LED power are enabled. PROJ_ON pin must be high and DMD_EN and ILLUM_EN bits must both be set to 1. |

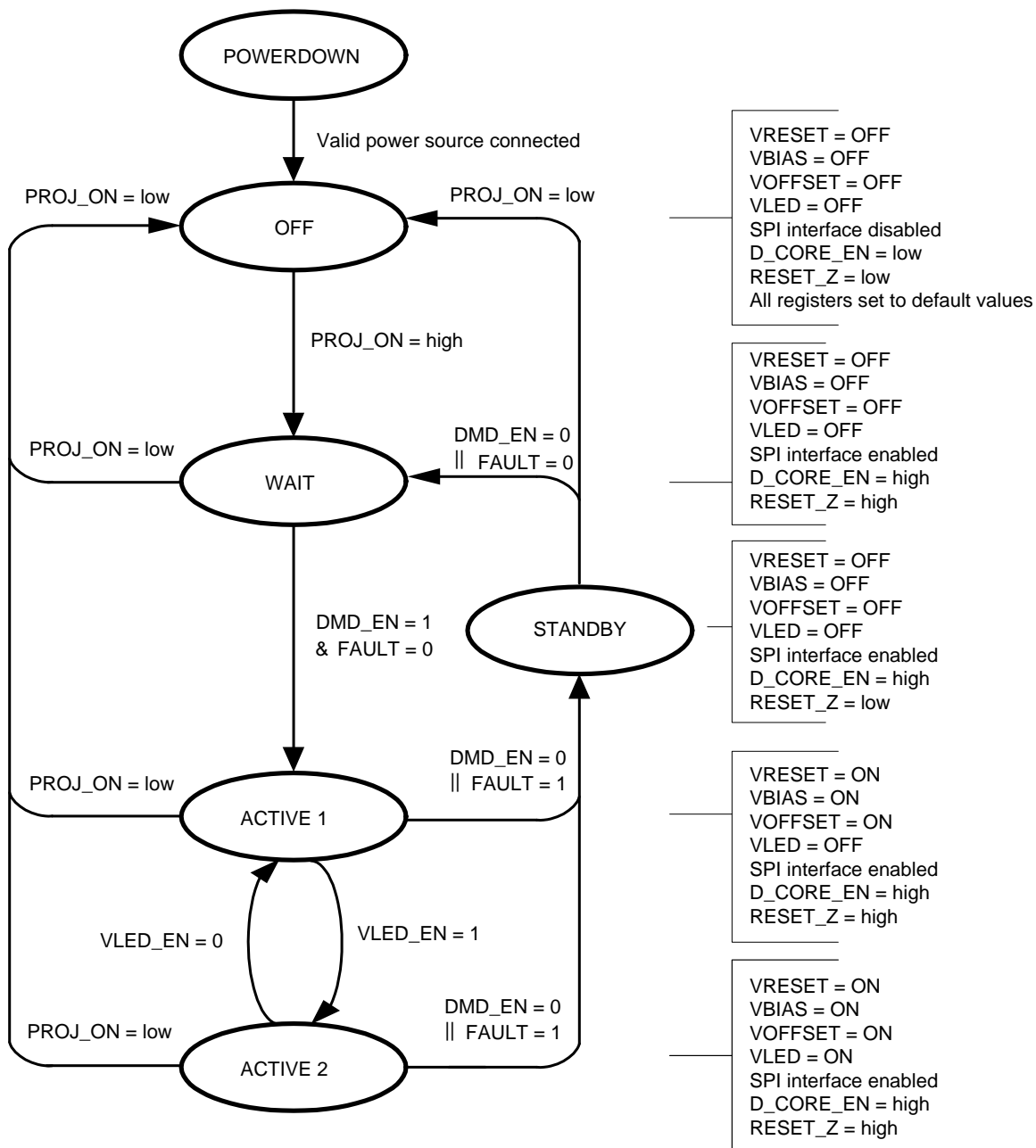
(1) Settings can be done through register 0x01

(2) Power-good faults, over-voltage, over-temperature shutdown, and undervoltage lockout

(3) Settings can be done through register 0x01, bit is named ILLUM_EN

Table 5. Device State as a Function of Control-Pin Status

| PROJ_ON Pin | STATE |
|-------------|---|
| LOW | OFF |
| HIGH | WAIT STANDBY ACTIVE1 ACTIVE2 (Device state depends on DMD_EN and ILLUM_EN bits and whether there are any fault conditions.) |



- A. || = OR, & = AND
- B. FAULT = Undervoltage on any supply, thermal shutdown, or UVLO detection
- C. UVLO detection, per the diagram, causes the DLPA3005 to go into the standby state. This is not the lowest power state. If lower power is desired, PROJ_ON should be set low.
- D. DMD_EN register bit can be reset or set by SPI writes. DMD_EN defaults to 0 when PROJ_ON goes from low to high and then the DLPC ASIC software automatically sets it to 1. Also, FAULT = 1 causes the DMD_EN register bit to be reset.
- E. D_CORE_EN is a signal internal to the DLPA3005. This signal turns on the VCORE regulator.

Figure 21. State Diagram

7.5 Programming

This section discusses the serial protocol interface (SPI) of the DLPA3005 as well as the interrupt handling, device shutdown and register protection.

7.5.1 SPI

The DLPA3005 provides a 4-wire SPI port that supports two SPI clock frequency modes: 0 MHz to 36 MHz and 20 MHz to 40MHz. The clock frequency mode can be set in register 0x17, DIG_SPI_FAST_SEL. The interface supports both read and write operations. The SPI_SS_Z input serves as the active low chip select for the SPI port. The SPI_SS_Z input must be forced low for writing to or reading from registers. When SPI_SS_Z is forced high, the data at the SPI_MOSI input is ignored, and the SPI_MISO output is forced to a high-impedance state. The SPI_MOSI input serves as the serial data input for the port; the SPI_MISO output serves as the serial data output. The SPI_CLK input serves as the serial data clock for both the input and output data. Data at the SPI_MOSI input is latched on the rising edge of SPI_CLK, while data is clocked out of the SPI_MISO output on the falling edge of SPI_CLK. [Figure 22](#) illustrates the SPI port protocol. Byte 0 is referred to as the command byte, where the most significant bit is the write/not-read bit. For the W/nR bit, a 1 indicates a write operation, while a 0 indicates a read operation. The remaining seven bits of the command byte are the register address targeted by the write or read operation. The SPI port supports write and read operations for multiple sequential register addresses through the implementation of an auto-increment mode. As shown in [Figure 22](#), the auto-increment mode is invoked by simply holding the SPI_SS_Z input low for multiple data bytes. The register address is automatically incremented after each data byte transferred, starting with the address specified by the command byte. After reaching address 0x7Fh the address pointer jumps back to 0x00h.

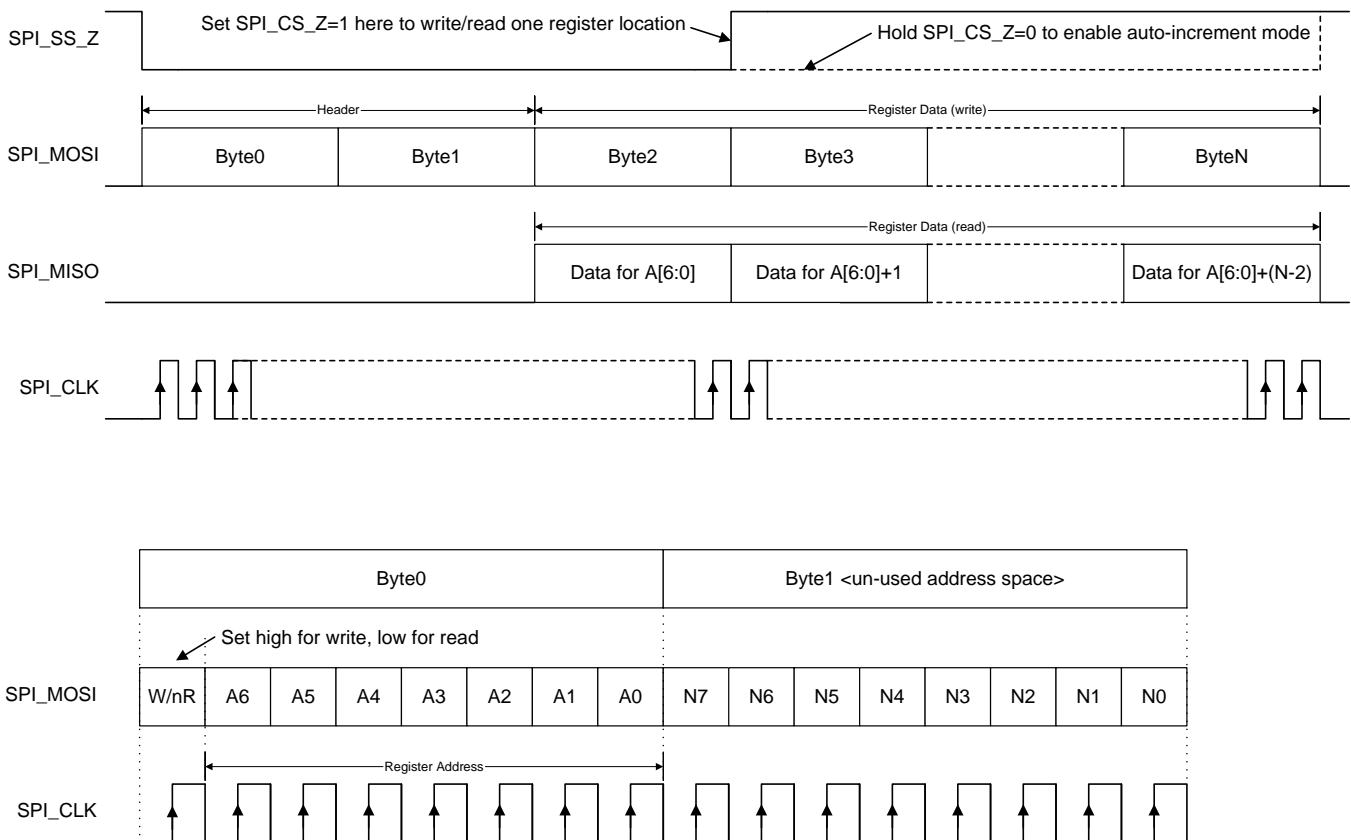


Figure 22. SPI Protocol

Programming (continued)

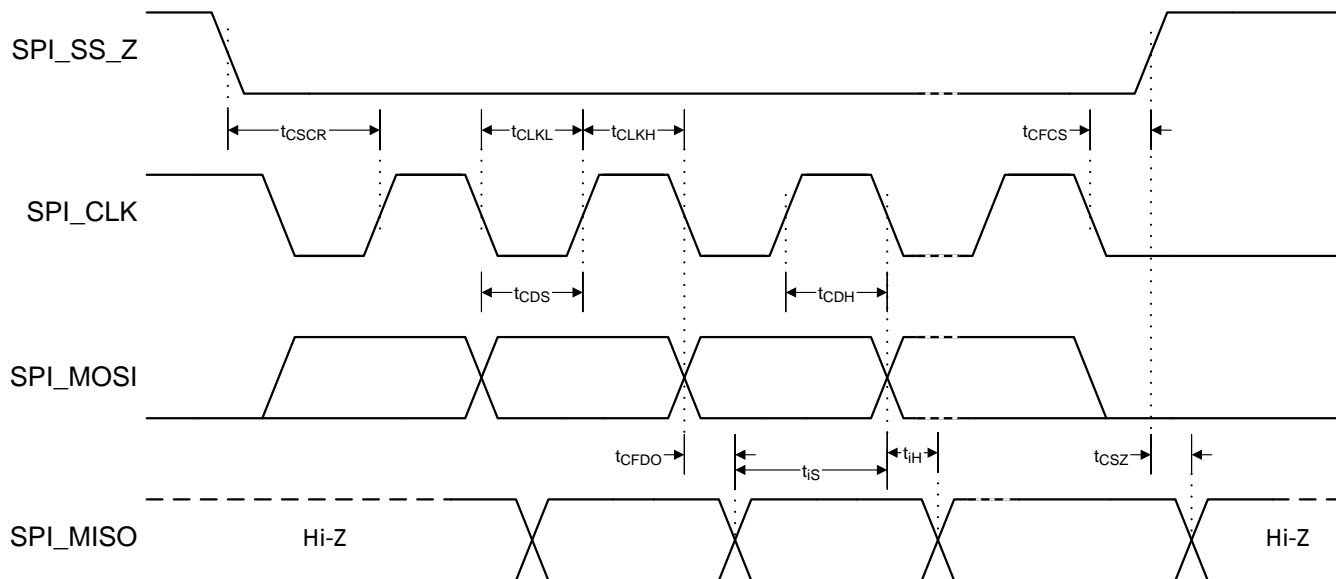


Figure 23. SPI Timing Diagram

7.5.2 Interrupt

The DLPA3005 has the capability to flag for several faults in the system, such as overheating, low battery, power good and over voltage faults. If a certain fault condition occurs one or more bits in the interrupt register (0x0C) will be set. The setting of a bit in register 0x0C will trigger an interrupt event, which will pull down the INT_Z pin. Interrupts can be masked by setting the respective MASK bits in register 0x0D. Setting a MASK bit will prevent that the INT_Z is pulled low for the particular fault condition. Some high-level faults are composed of multiple low-level faults. The high-level faults can be read in register 0x0C, while the lower-level faults can be read in register 0x027 through 0x2A. An overview of the faults and how they are related is given in Table 6.

Table 6. Interrupt Registers

| HIGH-LEVEL | MID-LEVEL | LOW-LEVEL |
|--------------|--------------------------------------|--------------------------------------|
| SUPPLY_FAULT | DMD_FAULT | DMD_PG_FAULT |
| | | BUCK_DMD1_PG_FAULT |
| | | BUCK_DMD1_OV_FAULT |
| | | BUCK_DMD2_PG_FAULT |
| | | BUCK_DMD2_OV_FAULT |
| | | LDO_GP1_PG_FAULT / LDO_DMD1_PG_FAULT |
| | | LDO_GP1_OV_FAULT / LDO_DMD1_OV_FAULT |
| | | LDO_GP2_PG_FAULT / LDO_DMD2_PG_FAULT |
| | LDO_GP2_OV_FAULT / LDO_DMD2_OV_FAULT | |
| | BUCK_GP1_PG_FAULT | |
| | BUCK_GP1_OV_FAULT | |
| | BUCK_GP2_PG_FAULT | |
| | BUCK_GP2_OV_FAULT | |
| | BUCK_GP3_PG_FAULT | |
| | BUCK_GP3_OV_FAULT | |

Programming (continued)
Table 6. Interrupt Registers (continued)

| HIGH-LEVEL | MID-LEVEL | LOW-LEVEL |
|--------------|--------------------|-----------|
| ILLUM_FAULT | ILLUM_BC1_PG_FAULT | |
| | ILLUM_BC1_OV_FAULT | |
| | ILLUM_BC2_PG_FAULT | |
| | ILLUM_BC2_OV_FAULT | |
| PROJ_ON_INT | | |
| BAT_LOW_SHUT | | |
| BAT_LOW_WARN | | |
| TS_SHUT | | |
| TS_WARN | | |

7.5.3 Fast-Shutdown in Case of Fault

The DLPA3005 has 2 shutdown-down modes: a normal shutdown initiated after pulling PROJ_ON level low and a fast power-down mode. The fast power down feature can be enabled/disabled via register 0x01, FAST_SHUTDOWN_EN. By default the mode is enabled.

When the fast power-down feature is enabled, a fast shutdown is initiated for specific faults. This shutdown happens autonomously from the DLPC. The DLPA3005 enters the fast-shutdown mode only for specific faults, thus not for all the faults flagged by the DLPA3005. The faults for which the DLPA3005 goes into fast-shutdown are listed in [Table 7](#).

Table 7. Faults that Trigger a Fast-Shutdown

| HIGH-LEVEL | LOW-LEVEL |
|--------------------------------------|--------------------------------------|
| BAT_LOW_SHUT | |
| TS_SHUT | |
| DMD_FAULT | DMD_PG_FAULT |
| | BUCK_DMD1_PG_FAULT |
| | BUCK_DMD1_OV_FAULT |
| | BUCK_DMD2_PG_FAULT |
| | BUCK_DMD2_OV_FAULT |
| | LDO_GP1_PG_FAULT / LDO_DMD1_PG_FAULT |
| | LDO_GP1_OV_FAULT / LDO_DMD1_OV_FAULT |
| | LDO_GP2_PG_FAULT / LDO_DMD2_PG_FAULT |
| LDO_GP2_OV_FAULT / LDO_DMD2_OV_FAULT | |
| ILLUM_FAULT | ILLUM_BC1_OV_FAULT |
| | ILLUM_BC2_OV_FAULT |

7.5.4 Protected Registers

By default all regular USER registers are writable, except for the READ ONLY registers. Registers can be protected though to prevent accidental write operations. By enabling the protecting, only USER registers 0x02 through 0x09 are writable. Protection can be enabled/ disabled via register 0x2F, PROTECT_USER_REG.

7.5.5 Writing to EEPROM

The DLPA3005 has an EEPROM mainly intended for default settings and factory trimming parameters. Registers 0x30 through 0x35 can freely be used for customer convenience though, to write a serial number or version information for instance. Writing to EEPROM requires a couple of steps. First the EEPROM needs to be unlocked. Unlock the EEPROM by writing 0xBAh to register 0x2E followed by writing 0xBE to the same register. Both writes must be consecutive, that is, there must be no other read or write operation in between sending

these two bytes. Once the password has been successfully written, register 0x30h through 0x35h are unlocked and can be write accessed using the regular SPI protocol. They remain unlocked until any byte other than 0xBABE is written to PASSWORD register 0x2E or the part is power cycled. To permanently store the written data in EEPROM write a 1 to register 0x2F, EEPROM_PROGRAM, > 250 ms later followed by writing a 0 to the same register.

To check if the registers are unlocked, read back the PASSWORD register 0x2E. If the data returned is 0x00h, the registers are locked. If the PASSWORD register returns 0x01h, the registers are unlocked.

7.6 Register Maps

Register Address, Default, R/W, Register name. **Boldface** settings are the hardwired defaults.

Table 8. Register Map

| NAME | BITS | DESCRIPTION | |
|---|-----------|--|------------------|
| 0x00, E3, R/W, Chip Identification | | | |
| CHIPID | [7:4] | Chip identification number: E (hex) | |
| REVID | [3:0] | Revision number, 3 (hex) | |
| 0x01, 82, R/W, Enable Register | | | |
| FAST_SHUTDOWN_EN | [7] | 0: Fast shutdown disabled 1: Fast shutdown enabled | |
| CW_EN | [6] | 0: Color wheel circuitry disabled 1: Color wheel circuitry enabled | |
| BUCK_GP3_EN | [5] | 0: General purpose buck3 disabled 1: General purpose buck3 enabled | |
| BUCK_GP2_EN | [4] | 0: General purpose buck2 disabled 1: General purpose buck2 enabled | |
| BUCK_GP1_EN | [3] | 0: General purpose buck1 disabled 1: General purpose buck1 enabled | |
| ILLUM_LED_AUTO_OFF_EN | [2] | 0: Illum_led_auto_off_en disabled 1: Illum_led_auto_off_en enabled | |
| ILLUM_EN | [1] | 0: Illum regulators disabled 1: Illum regulators enabled | |
| DMD_EN | [0] | 0: DMD regulators disabled 1: DMD regulators enabled | |
| 0x02, 70, R/W, IREG Switch Control | | | |
| | [7] | Reserved, values don't care | |
| ILLUM_ILIM | [6:3] | Rlim voltage top-side (mV). Illum current limit = Rlim voltage / Rlim | |
| | | 0000: 17 | 1000: 73 |
| | | 0001: 20 | 1001: 88 |
| | | 0010: 23 | 1010: 102 |
| | | 0011: 25 | 1011: 117 |
| | | 0100: 29 | 1100: 133 |
| | | 0101: 37 | 1101: 154 |
| | | 0110: 44 | 1110: 176 |
| 0111: 59 | 1111: 197 | | |
| ILLUM_SW_ILIM_EN | [2:0] | Bit2: CH3, MOSFET R transient current limit (0:disabled , 1:enabled) Bit1: CH2, MOSFET Q transient current limit (0:disabled , 1:enabled) Bit0: CH1, MOSFET P transient current limit (0:disabled , 1:enabled) | |
| 0x03, 00, R/W, SW1_IDAC(1) | | | |
| | [7:2] | Reserved, values don't care | |
| SW1_IDAC<9:8> | [1:0] | Led current of CH1(A) = ((Bit value + 1)/1024) × (150 mV / Rlim), Most significant bits of 10 bits register (register 0x03 and 0x04). 00 0000 0000 [OFF] 00 0011 0011 [(52/1024) × (150mV/Rlim)], Minimum code. 11 1111 1111 [150mV/Rlim] | |

Register Maps (continued)
Table 8. Register Map (continued)

| NAME | BITS | DESCRIPTION |
|---|-------|---|
| 0x04, 00, R/W, SW1_IDAC(2) | | |
| SW1_IDAC<7:0> | [7:0] | Led current of CH1(A) = ((Bit value + 1)/1024) × (150 mV / Rlim), Least significant bits of 10 bits register (register 0x03 and 0x04). 00 0000 0000 [OFF] 00 0011 0011 [(52/1024) × (150mV/Rlim)], Minimum code. 11 1111 1111 [150mV/Rlim] |
| 0x05, 00, R/W, SW2_IDAC(1) | | |
| | [7:2] | Reserved, value don't care. |
| SW2_IDAC<9:8> | [1:0] | Led current of CH2(A) = ((Bit value + 1)/1024) × (150 mV / Rlim), Most significant bits of 10 bits register (register 0x05 and 0x06). 00 0000 0000 [OFF] 00 0011 0011 [(52/1024) × (150mV/Rlim)], Minimum code. 11 1111 1111 [150mV/Rlim] |
| 0x06, 00, R/W, SW2_IDAC(2) | | |
| SW2_IDAC<7:0> | [7:0] | Led current of CH2(A) = ((Bit value + 1)/1024) × (150 mV / Rlim), Least significant bits of 10 bits register (register 0x05 and 0x06). 00 0000 0000 [OFF] 00 0011 0011 [(52/1024) × (150mV/Rlim)], Minimum code. 11 1111 1111 [150mV/Rlim] |
| 0x07, 00, R/W, SW3_IDAC(1) | | |
| | [7:2] | Reserved, value don't care. |
| SW3_IDAC<9:8> | [1:0] | Led current of CH3(A) = ((Bit value + 1)/1024) × (150 mV / Rlim), Most significant bits of 10 bits register (register 0x07 and 0x08). 00 0000 0000 [OFF] 00 0011 0011 [(52/1024) × (150mV/Rlim)], Minimum code. 11 1111 1111 [150mV/Rlim] |
| 0x08, 00, R/W, SW3_IDAC(2) | | |
| SW3_IDAC<7:0> | [7:0] | Led current of CH3(A) = ((Bit value + 1)/1024) × (150 mV / Rlim), Least significant bits of 10 bits register (register 0x07 and 0x08). 00 0000 0000 [OFF] 00 0011 0011 [(52/1024) × (150mV/Rlim)], Minimum code. 11 1111 1111 [150mV/Rlim] |
| 0x09, 00, R/W, Switch ON/OFF Control | | |
| SW3 | [7] | Only used if DIRECT MODE is enabled (see register 0x2F) 0: SW3 disabled 1: SW3 enabled |
| SW2 | [6] | Only used if DIRECT MODE is enabled (see register 0x2F) 0: SW2 disabled 1: SW2 enabled |
| SW1 | [5] | Only used if DIRECT MODE is enabled (see register 0x2F) 0: SW1 disabled 1: SW1 enabled |
| | [4:0] | Reserved, value don't care. |
| 0x0A, 00, R/W, Analog Front End (1) | | |
| AFE_EN | [7] | 0: Analog front end disabled 1: Analog front end enabled |
| AFE_CAL_DIS | [6] | 0: Calibrated 18x AFE_VGA 1: Uncalibrated 18x AFE_VGA |
| AFE_GAIN | [5:4] | Gain analog front end gain 00: Off 01: 1x 10: 9.5x 11: 18x |

Register Maps (continued)
Table 8. Register Map (continued)

| NAME | BITS | DESCRIPTION | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
|--|-------------|---|--------------------|-------------|-------------|--------------|-------------|-------------|-------------|--------------|-------------|-------------|-------------|--------------|-------------|-------------|--------------|--------------|-------------|-------------|--------------|--------------|-------------|-------------|--------------|--------------|-------------|-------------|--------------|--------------|-------------|-------------|--------------|--------------|
| AFE_SEL | [3:0] | Selected analog multiplexer input 0000: ILLUM_A_FB/xx, where xx is controlled by VLED_OVP_VLED_RATIO <4:0> (reg0x19) 0001: ILLUM_B_FB/xx, where xx is controlled by VLED_OVP_VLED_RATIO <4:0> (reg0x19) 0010: VIN/xx, where xx is controlled by ILLUM_LED_AUTO_OFF_SEL <3:0> (reg0x18) 0011: V_LABB 0100: RLIM_K1 0101: RLIM_K2 0110: CH1_SWITCH 0111: CH2_SWITCH 1000: CH3_SWITCH 1001: VREF_1V2 1010: VOTS (Main temperature sense block output voltage) 1011: VPROG1/12 (EEPROM block1 programming voltage divided by 12) 1100: VPROG2/12 (EEPROM block2 programming voltage divided by 12) 1101: ACMPR_IN_1 1110: ACMPR_IN_2 1111: ACMPR_IN_3 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 0x0B, 00, R/W, Analog Front End (2) | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| TSAMPLE_SEL | [7:6] | Samples time LABB Sensor (µs) 00: 7 01: 14 10: 21 11: 28 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| SAMPLE_LABB | [5] | 0: LABB SAMPLING disabled 1: START LABB SAMPLING (auto reset to 0 after TSAMPLE_SEL time). | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| VLED_OVP_VIN_RATIO | [4:0] | OVP_VIN Division factor. <table border="1"> <tr> <td>00000: 3.33</td> <td>01000: 6.10</td> <td>10000: 9.16</td> <td>11000: 12.51</td> </tr> <tr> <td>00001: 4.98</td> <td>01001: 6.23</td> <td>10001: 9.60</td> <td>11001: 12.94</td> </tr> <tr> <td>00010: 5.23</td> <td>01010: 6.67</td> <td>10010: 9.99</td> <td>11010: 13.31</td> </tr> <tr> <td>00011: 5.32</td> <td>01011: 7.11</td> <td>10011: 10.41</td> <td>11011: 13.70</td> </tr> <tr> <td>00100: 5.42</td> <td>01100: 7.50</td> <td>10100: 10.88</td> <td>11100: 14.11</td> </tr> <tr> <td>00101: 5.52</td> <td>01101: 7.96</td> <td>10101: 11.26</td> <td>11101: 14.56</td> </tr> <tr> <td>00110: 5.62</td> <td>01110: 8.34</td> <td>10110: 11.67</td> <td>11110: 15.04</td> </tr> <tr> <td>00111: 5.85</td> <td>01111: 8.77</td> <td>10111: 12.11</td> <td>11111: 15.41</td> </tr> </table> | 00000: 3.33 | 01000: 6.10 | 10000: 9.16 | 11000: 12.51 | 00001: 4.98 | 01001: 6.23 | 10001: 9.60 | 11001: 12.94 | 00010: 5.23 | 01010: 6.67 | 10010: 9.99 | 11010: 13.31 | 00011: 5.32 | 01011: 7.11 | 10011: 10.41 | 11011: 13.70 | 00100: 5.42 | 01100: 7.50 | 10100: 10.88 | 11100: 14.11 | 00101: 5.52 | 01101: 7.96 | 10101: 11.26 | 11101: 14.56 | 00110: 5.62 | 01110: 8.34 | 10110: 11.67 | 11110: 15.04 | 00111: 5.85 | 01111: 8.77 | 10111: 12.11 | 11111: 15.41 |
| 00000: 3.33 | 01000: 6.10 | 10000: 9.16 | 11000: 12.51 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 00001: 4.98 | 01001: 6.23 | 10001: 9.60 | 11001: 12.94 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 00010: 5.23 | 01010: 6.67 | 10010: 9.99 | 11010: 13.31 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 00011: 5.32 | 01011: 7.11 | 10011: 10.41 | 11011: 13.70 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 00100: 5.42 | 01100: 7.50 | 10100: 10.88 | 11100: 14.11 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 00101: 5.52 | 01101: 7.96 | 10101: 11.26 | 11101: 14.56 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 00110: 5.62 | 01110: 8.34 | 10110: 11.67 | 11110: 15.04 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 00111: 5.85 | 01111: 8.77 | 10111: 12.11 | 11111: 15.41 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 0x0C, 00, R, Main Status Register | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| SUPPLY_FAULT | [7] | 0: No PG or OV failures for any of the LV Supplies 1: PG failures for a LV Supplies | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| ILLUM_FAULT | [6] | 0: ILLUM_FAULT = LOW 1: ILLUM_FAULT = HIGH | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| PROJ_ON_INT | [5] | 0: PROJ_ON = HIGH 1: PROJ_ON = LOW | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| DMD_FAULT | [4] | 0: DMD_FAULT = LOW 1: DMD_FAULT = HIGH | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| BAT_LOW_SHUT | [3] | 0: VIN > UVLO_SEL<4:0> 1: VIN < UVLO_SEL<4:0> | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| BAT_LOW_WARN | [2] | 0: VIN > LOWBATT_SEL<4:0> 1: VIN < LOWBATT_SEL<4:0> | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| TS_SHUT | [1] | 0: Chip temperature < 132.5°C and no violation in V5V0 1: Chip temperature > 156.5°C, or violation in V5V0 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| TS_WARN | [0] | 0: Chip temperature < 121.4°C 1: Chip temperature > 123.4°C | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 0x0D, F5, Interrupt Mask Register | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| SUPPLY_FAULT_MASK | [7] | 0: Not masked for SUPPLY_FAULT interrupt 1: Masked for SUPPLY_FAULT interrupt | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |

Register Maps (continued)
Table 8. Register Map (continued)

| NAME | BITS | DESCRIPTION |
|--|-------|---|
| ILLUM_FAULT_MASK | [6] | 0: Not masked for ILLUM_FAULT interrupt 1: Masked for ILLUM_FAULT interrupt |
| PROJ_ON_INT_MASK | [5] | 0: Not masked for PROJ_ON_INT interrupt 1: Masked for PROJ_ON_INT interrupt |
| DMD_FAULT_MASK | [4] | 0: Not masked for DMD_FAULT interrupt 1: Masked for DMD_FAULT interrupt |
| BAT_LOW_SHUT_MASK | [3] | 0: Not masked for BAT_LOW_SHUT interrupt 1: Masked for BAT_LOW_SHUT interrupt |
| BAT_LOW_WARN_MASK | [2] | 0: Not masked for BAT_LOW_WARN interrupt 1: Masked for BAT_LOW_WARN interrupt |
| TS_SHUT_MASK | [1] | 0: Not masked for TS_SHUT interrupt 1: Masked for TS_SHUT interrupt |
| TS_WARN_MASK | [0] | 0: Not masked for TS_WARN interrupt 1: Masked for TS_WARN interrupt |
| 0x0E, 00, R/W, Break-Before-Make Delay | | |
| BBM_DELAY | [7:0] | Break before make delay register (ns), step size is 111 ns 0000 0000: 0 0000 0001: 333 0000 0010: 444 0000 0011: 555 1111 1101: 28305 1111 1110: 28416 1111 1111: 28527 |
| 0x0F, 07, R/W, Fast Shutdown Timing | | |
| VOFS/RESETZ_DELAY | [7:4] | VOFS/RESETZ_DELAY (μs) |
| | | 0000: 4.000 – 4.445 1000: 6.230 – 7.120 |
| | | 0001: 8.010 – 8.900 1001: 12.46 – 14.24 |
| | | 0010: 16.02 – 17.80 1010: 24.89 – 28.44 |
| | | 0011: 32.00 – 35.55 1011: 49.77 – 56.88 |
| | | 0100: 63.99 – 71.10 1100: 99.5 – 113.8 |
| | | 0101: 128.0 – 142.2 1101: 199.1 – 227.6 |
| | | 0110: 256.0 – 284.5 1110: 398.3 – 455.2 |
| 0111: 512.1 – 569.0 1111: 1024.2 – 1138.0 | | |
| VBIAS/VRST_DELAY | [3:0] | VBIAS/VRST_DELAY (μs) |
| | | 0000: 4.000 – 4.445 1000: 6.230 – 7.120 |
| | | 0001: 8.010 – 8.900 1001: 12.46 – 14.24 |
| | | 0010: 16.02 – 17.80 1010: 24.89 – 28.44 |
| | | 0011: 32.00 – 35.55 1011: 49.77 – 56.88 |
| | | 0100: 63.99 – 71.10 1100: 99.5 – 113.8 |
| | | 0101: 128.0 – 142.2 1101: 199.1 – 227.6 |
| | | 0110: 256.0 – 284.5 1110: 398.3 – 455.2 |
| 0111: 512.1 – 569.0 1111: 1024.2 – 1138.0 | | |
| 0x10, C0, R/W, VOFS State Duration | | |

Register Maps (continued)
Table 8. Register Map (continued)

| NAME | BITS | DESCRIPTION | | | |
|--|--------------|---|--------------|--------------|--------------|
| VOFS_STATE_DURATION | [7:5] | Duration of VOFS state (ms) 000: 1 001: 5 010: 10 011: 20 100: 40 101: 80 110: 160 111: 320 | | | |
| LOWBATT_SEL | [4:0] | Low Battery level Selection | | | |
| | | 00000: 3.93 | 01000: 7.27 | 10000: 10.94 | 11000: 14.96 |
| | | 00001: 5.92 | 01001: 7.43 | 10001: 11.46 | 11001: 15.47 |
| | | 00010: 6.21 | 01010: 7.95 | 10010: 11.92 | 11010: 15.91 |
| | | 00011: 6.32 | 01011: 8.46 | 10011: 12.42 | 11011: 16.37 |
| | | 00100: 6.43 | 01100: 8.93 | 10100: 12.97 | 11100: 16.87 |
| | | 00101: 6.55 | 01101: 9.47 | 10101: 13.42 | 11101: 17.40 |
| | | 00110: 6.67 | 01110: 9.92 | 10110: 13.91 | 11110: 17.96 |
| 00111: 6.93 | 01111: 10.42 | 10111: 14.43 | 11111: 18.41 | | |
| 0x11, 00, R/W, VBIAS State Duration | | | | | |
| VBIAS_STATE_DURATION | [7:5] | Duration of VBIAS state (ms) 000: bypass 001: 5 010: 10 011: 20 100: 40 101: 80 110: 160 111: 320 | | | |
| UVLO_SEL | [4:0] | Under Voltage Lockout level Selection | | | |
| | | 00000: 3.93 | 01000: 7.27 | 10000: 10.94 | 11000: 14.96 |
| | | 00001: 5.92 | 01001: 7.43 | 10001: 11.46 | 11001: 15.47 |
| | | 00010: 6.21 | 01010: 7.95 | 10010: 11.92 | 11010: 15.91 |
| | | 00011: 6.32 | 01011: 8.46 | 10011: 12.42 | 11011: 16.37 |
| | | 00100: 6.43 | 01100: 8.93 | 10100: 12.97 | 11100: 16.87 |
| | | 00101: 6.55 | 01101: 9.47 | 10101: 13.42 | 11101: 17.40 |
| | | 00110: 6.67 | 01110: 9.92 | 10110: 13.91 | 11110: 17.96 |
| 00111: 6.93 | 01111: 10.42 | 10111: 14.43 | 11111: 18.41 | | |
| 0x13, 00, R/W, GP1 Buck Converter Voltage Selection | | | | | |
| BUCK_GP1_TRIM | [7:0] | General purpose1 buck output voltage = 1+ bit value * 15.69 (stepsize = 15.69 mV) 00000000 1 V 11111111 5 V | | | |

Register Maps (continued)
Table 8. Register Map (continued)

| NAME | BITS | DESCRIPTION |
|---|-------|---|
| 0x14, 00, R/W, GP2 Buck Converter voltage Selection | | |
| BUCK_GP2_TRIM | [7:0] | General purpose2 buck output voltage = 1+ bit value * 15.69 (stepsize = 15.69 mV) 00000000 1 V 11111111 5 V |
| 0x15, 00, R/W, GP3 Buck Converter Voltage Selection | | |
| BUCK_GP3_TRIM | [7:0] | General purpose3 driver output voltage = 1+ bit value * 15.69 (stepsize = 15.69 mV) 00000000 1 V 11111111 5 V |
| 0x16, 00, R/W, Buck Skip Mode | | |
| | [7:5] | Reserved, value don't care. |
| BUCK_SKIP_ON | [4:0] | Skip Mode: Bit4: Buck_GP3 (0:disabled , 1:enabled) Bit3: Buck_GP1 (0:disabled , 1:enabled) Bit2: Buck_GP2 (0:disabled , 1:enabled) Bit1: Buck_DMD1 (0:disabled , 1:enabled) Bit0: Buck_DMD2 (0:disabled , 1:enabled) |
| 0x17, 02, R/W, User Configuration Selection Register | | |
| DIG_SPI_FAST_SEL | [7] | 0: SPI Clock from 0 to 36 MHz 1: SPI Clock from 20 to 40 MHz |
| | [6] | Reserved, value don't care. |
| ILLUM_EXT_LSD_CUR_LIM_EN | [5] | 0: Current limiting disabled (External FETs mode) 1: Current limiting enabled (External FETs mode) |
| Reserved | [4] | |
| ILLUM_3A_INT_SWITCH_SEL | [3] | Illum Configuration: most significant bit is ILLUM_EXT_SWITCH_CAP<6> (Reg0x26). Other 4 bits are <3:0> of this register. "x" is don't care. x xx00: Off x x110: 2 x 3 A Internal FETs x 0010: 1 x 6 A Internal FETs x 1010: 1 x 3 A Internal FETs 0 xx0x: Off 0 x11x: 2 x 3 A Internal FETs 0 001x: 1 x 6 A Internal FETs 0 101x: 1 x 3 A Internal FETs 0 xxx1: External FETs |
| ILLUM_DUAL_OUTPUT_CNTR_SEL | [2] | |
| ILLUM_INT_SWITCH_SEL | [1] | |
| ILLUM_EXT_SWITCH_SEL | [0] | |
| 0x18, 00, R/W, OLV -ILLUM_LED_AUTO_OFF_SEL | | |
| ILLUM_OLV_SEL | [7:4] | Illum openloop voltage (V) = 3 + bit value * 1 (stepsize = 1 V) 0000: 3 V 0001: 4 V ... 1110: 17 V 1111: 18 V |

Register Maps (continued)
Table 8. Register Map (continued)

| NAME | BITS | DESCRIPTION | | | |
|---|-------|--|------------------------|---------------------|---------------------|
| ILLUM_LED_AUTO_OFF_SEL | [3:0] | Bit value | Led Auto Off Level (V) | VIN division factor | |
| | | 0000 | 3.93 | 3.33 | |
| | | 0001 | 5.92 | 4.98 | |
| | | 0010 | 6.21 | 5.23 | |
| | | 0011 | 6.32 | 5.32 | |
| | | 0100 | 6.43 | 5.42 | |
| | | 0101 | 6.55 | 5.52 | |
| | | 0110 | 6.67 | 5.62 | |
| | | 0111 | 6.93 | 5.85 | |
| | | 1000 | 7.27 | 6.10 | |
| | | 1001 | 7.95 | 6.67 | |
| | | 1010 | 8.93 | 7.50 | |
| | | 1011 | 9.92 | 8.34 | |
| | | 1100 | 10.94 | 9.16 | |
| | | 1101 | 11.92 | 9.99 | |
| | | 1110 | 12.97 | 10.88 | |
| 1111 | 13.91 | 11.67 | | | |
| 0x19, 1F, R/W, Illumination Buck Converter Overvoltage Fault Level | | | | | |
| Reserved | [7:5] | | | | |
| VLED_OVP_VLED_RATIO | [4:0] | Bit value / OVP VLED Division factor | | | |
| | | 00000: 3.33 | 01000: 6.10 | 10000: 9.16 | 11000: 12.51 |
| | | 00001: 4.98 | 01001: 6.23 | 10001: 9.60 | 11001: 12.94 |
| | | 00010: 5.23 | 01010: 6.67 | 10010: 9.99 | 11010: 13.31 |
| | | 00011: 5.32 | 01011: 7.11 | 10011: 10.41 | 11011: 13.70 |
| | | 00100: 5.42 | 01100: 7.50 | 10100: 10.88 | 11100: 14.11 |
| | | 00101: 5.52 | 01101: 7.96 | 10101: 11.26 | 11101: 14.56 |
| | | 00110: 5.62 | 01110: 8.34 | 10110: 11.67 | 11110: 15.04 |
| | | 00111: 5.85 | 01111: 8.77 | 10111: 12.11 | 11111: 15.41 |
| 0x1B, 00, R/W, Color Wheel PWM Voltage(1) | | | | | |
| CW_PWM <7:0> | [7:0] | Least significant 8 bits of 16 bits register (register 0x1B and 0x1C) Average color wheel PWM voltage (V), step size = 76.294 μ V 0x0000 0 V 0xFFFF 5 V | | | |

Register Maps (continued)
Table 8. Register Map (continued)

| NAME | BITS | DESCRIPTION |
|---|-------|---|
| 0x1C, 00, R/W, Color Wheel PWM Voltage(2) | | |
| CW_PWM <15:8> | [7:0] | Most significant 8 bits of 16 bits register (register 0x1B and 0x1C) Average color wheel PWM voltage (V), step size = 76.294 μ V 0x0000 0 V 0xFFFF 5 V |
| 0x25, 00, R/W, ILLUM BUCK CONVERTER BANDWIDTH SELECTION | | |
| reserved | [7:4] | |
| ILLUM_BW_BC1 | [3,2] | ILED CONTROL LOOP BANDWIDTH INCREASE (dB) 00: 0 |
| | | 01: 1.9 |
| | | 10: 4.7 |
| | | 11: 9.3 |
| ILLUM_BW_BC2 | [1,0] | ILED CONTROL LOOP BANDWIDTH INCREASE (dB) 00: 0 |
| | | 01: 1.9 |
| | | 10: 4.7 |
| | | 11: 9.3 |
| 0x26, DF, R, Capability register | | |
| LED_AUTO_TURN_OFF_CAP | [7] | 0: LED_AUTO_TURN_OFF_CAP disabled 1: LED_AUTO_TURN_OFF_CAP enabled |
| ILLUM_EXT_SWITCH_CAP | [6] | 0: No external switch control capability 1: External switch control capability included |
| CW_CAP | [5] | 0: No color wheel capability 1: Color wheel capability included |
| DMD type | [4] | 0: VSP 1: TRP |
| DMD_LDO1_USE | [3] | 0: LDO1 not used for DMD, voltage set by user register 1: LDO1 used for DMD, voltage set by EEPROM |
| DMD_LDO2_USE | [2] | 0: LDO2 not used for DMD, voltage set by user register 1: LDO2 used for DMD, voltage set by EEPROM |
| DMD_BUCK1_USE | [1] | 0: DMD Buck1 disabled 1: DMD Buck1 used |
| DMD_BUCK2_USE | [0] | 0: DMD Buck2 disabled 1: DMD Buck2 used |
| 0x27, 00, R, Detailed status register1 (Power good failures for general purpose and illumination blocks) | | |
| BUCK_GP3_PG_FAULT | [7] | 0: No fault 1: Focus motor buck power good failure. Does not initiate a fast shutdown. |
| BUCK_GP1_PG_FAULT | [6] | 0: No fault 1: General purpose buck1 power good failure. Does not initiate a fast shutdown. |
| BUCK_GP2_PG_FAULT | [5] | 0: No fault 1: General purpose buck2 power good failure. Does not initiate a fast shutdown. |
| Reserved | [4] | |
| ILLUM_BC1_PG_FAULT | [3] | 0: No fault 1: Illum buck converter1 power good failure. Does not initiate a fast shutdown. |
| ILLUM_BC2_PG_FAULT | [2] | 0: No fault 1: Illum buck converter2 power good failure. Does not initiate a fast shutdown. |
| | [1] | Reserved, value always 0 |
| | [0] | Reserved, value always 0 |
| 0x28, 00, R, Detailed status register2 (Overvoltage failures for general purpose and illum blocks) | | |
| BUCK_GP3_OV_FAULT | [7] | 0: No fault 1: Focus motor buck overvoltage failure. Does not initiate a fast shutdown. |

Register Maps (continued)
Table 8. Register Map (continued)

| NAME | BITS | DESCRIPTION |
|---|------|--|
| BUCK_GP1_OV_FAULT | [6] | 0: No fault 1: General purpose buck1 overvoltage failure. Does not initiate a fast shutdown. |
| BUCK_GP2_OV_FAULT | [5] | 0: No fault 1: General purpose buck2 overvoltage failure. Does not initiate a fast shutdown. |
| | [4] | Reserved, value always 0 |
| ILLUM_BC1_OV_FAULT | [3] | 0: No fault 1: Illum buck converter1 overvoltage failure. Does not initiate a fast shutdown. |
| ILLUM_BC2_OV_FAULT | [2] | 0: No fault 1: Illum buck converter2 overvoltage failure. Does not initiate a fast shutdown. |
| | [1] | Reserved, value always 0 |
| | [0] | Reserved, value always 0 |
| 0x29, 00, R, Detailed status register3 (Power good failure for DMD related blocks) | | |
| | [7] | Reserved, value always 0 |
| DMD_PG_FAULT | [6] | 0: No fault 1: VBIAS, VOFS and/or VRST power good failure. Initiates a fast shutdown. |
| BUCK_DMD1_PG_FAULT | [5] | 0: No fault 1: Buck1 (used to create DMD voltages) power good failure. Initiates a fast shutdown. |
| BUCK_DMD2_PG_FAULT | [4] | 0: No fault 1: Buck2 (used to create DMD voltages) power good failure. Initiates a fast shutdown. |
| | [3] | Reserved, value always 0 |
| | [2] | Reserved, value always 0 |
| LDO_GP1_PG_FAULT / LDO_DMD1_PG_FAULT | [1] | 0: No fault 1: LDO1 (used as general purpose or DMD specific LDO) power good failure. Initiates a fast shutdown. |
| LDO_GP2_PG_FAULT / LDO_DMD2_PG_FAULT | [0] | 0: No fault 1: LDO2 (used as general purpose or DMD specific LDO) power good failure. Initiates a fast shutdown. |

Register Maps (continued)
Table 8. Register Map (continued)

| NAME | BITS | DESCRIPTION |
|---|-------|---|
| 0x2A, 00, R, Detailed status register4 (Overvoltage failures for DMD related blocks and Color Wheel) | | |
| | [7] | Reserved, value always 0 |
| | [6] | Reserved, value always 0 |
| BUCK_DMD1_OV_FAULT | [5] | 0: No fault 1: Buck1 (used to create DMD voltage) overvoltage failure |
| BUCK_DMD2_OV_FAULT | [4] | 0: No fault 1: Buck2 (used to create DMD voltage) overvoltage failure |
| | [3] | Reserved, value always 0 |
| | [2] | Reserved, value always 0 |
| LDO_GP1_OV_FAULT / LDO_DMD1_OV_FAULT | [1] | 0: No fault 1: LDO1 (used as general purpose or DMD specific LDO) overvoltage failure |
| LDO_GP2_OV_FAULT / LDO_DMD2_OV_FAULT | [0] | 0: No fault 1: LDO2 (used as general purpose or DMD specific LDO) overvoltage failure |
| 0x2B, 00, R, Chip ID extension | | |
| CHIP_ID_EXTENTION | [7:0] | ID extension to distinguish between various configuration options. |
| 0x2C, 00, R/W, ILLUM_LED_AUTO_TURN_OFF_DELAY SETTINGS | | |
| Reserved | [7:4] | TBD |
| ILLUM_LED_AUTO_TURN_OFF_D ELAY | [3:0] | ILLUM_LED_AUTO_TURN_OFF_DELAY (µsec) |
| | | 0000: 4.000-4.445 0100: 63.99-71.10 1000: 6.230-7.120 1100: 99.5-113.8 |
| | | 0001: 8.010-8.900 0101: 128.0-142.2 1001: 12.46-14.24 1101: 199.1-227.6 |
| | | 0010: 16.02-17.80 0110: 256.0-284.5 1010: 24.89-28.44 1110: 398.3-455.2 |
| 0011: 32.00-35.55 0111: 512.1-569.0 1011: 49.77-56.88 1111: 1024.2-1138.0 | | |
| 0x2E, 00, R/W, User Password | | |
| USER_PASSWORD (0xBABE) | [7:0] | Write Consecutively 0xBA and 0xBE to unlock. |
| 0x2F, 00, R/W, User Protection Register | | |
| | [7:3] | Reserved, value don't care. |
| EEPROM_PROGRAM | [2] | 0: EEPROM programming disabled 1: Shadow register values programmed to EEPROM |
| DIRECT_MODE | [1] | 0: Direct mode disabled 1: Direct mode enabled (register 0x09 to control switched) |
| PROTECT_USER_REG | [0] | 0: ALL regular USER registers are WRITABLE, except for READ ONLY registers 1: ONLY USER registers 0x02, 0x03, 0x04, 0x05, 0x06, 0x07, 0x08, and 0x09 are WRITABLE |
| 0x30, 00, R/W, User EEPROM Register | | |
| USER_REGISTER1 | [7:0] | User EEPROM Register1 |
| 0x31, 00, R/W, User EEPROM Register | | |
| USER_REGISTER2 | [7:0] | User EEPROM Register2 |
| 0x32, 00, R/W, User EEPROM Register | | |
| USER_REGISTER3 | [7:0] | User EEPROM Register3 |
| 0x33, 00, R/W, User EEPROM Register | | |
| USER_REGISTER4 | [7:0] | User EEPROM Register4 |
| 0x34, 00, R/W, User EEPROM Register | | |
| USER_REGISTER5 | [7:0] | User EEPROM Register5 |
| 0x35, 00, R/W, User EEPROM Register | | |
| USER_REGISTER6 | [7:0] | User EEPROM Register6 |

8 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

In display applications, using the DLPA3005 provides all needed analog functions including all analog power supplies and the RGB LED driver (up to 16A per LED) to provide a robust and efficient display solution. Each DLP application is derived primarily from the optical architecture of the system and the format of the data coming into the DLPC3439 DLP controller chips.

8.2 Typical Application

A common application when using DLPA3005 is to use it with a 0.47 1080 DMD (DLP4710) and two DLPC3439 controllers for creating a small, ultra-portable projector. The DLPC3439s in the projector typically receive images from a PC or video player using HDMI or VGA analog as shown in Figure 24. Card readers and Wi-Fi can also be used to receive images if the appropriate peripheral chips are added. The DLPA3005 provides power supply sequencing and control of the RGB LED currents as required by the application.

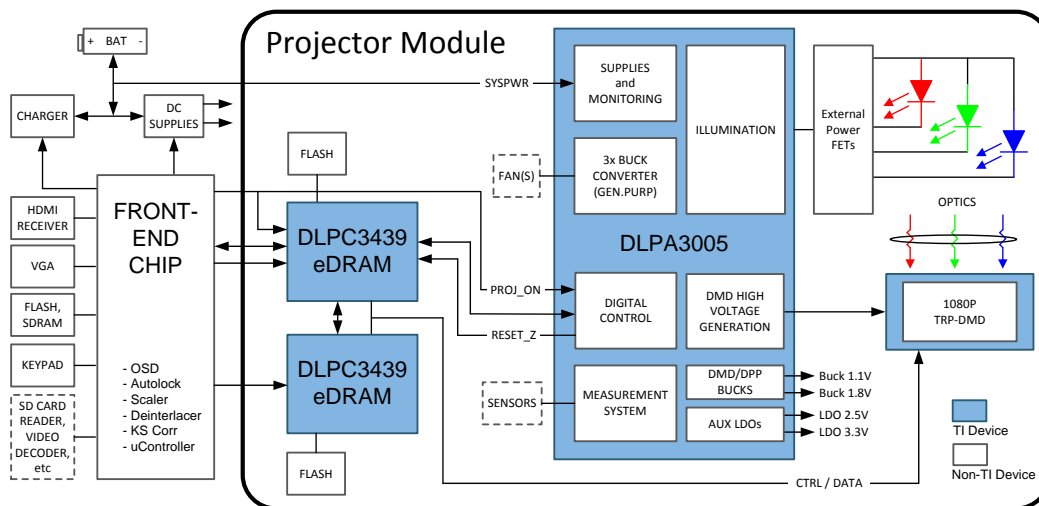


Figure 24. Typical Setup Using DLPA3005

8.2.1 Design Requirements

An ultra-portable projector can be created by using a DLP chip set comprised of a 0.47 1080 DMD (DLP4710), two DLPC3439s controllers, and the DLPA3005 PMIC/LED Driver. The two DLPC3439s do the digital image processing, the DLPA3005 provides the needed analog functions for the projector, and DMD is the display device for producing the projected image. In addition to the three DLP chips in the chip set, other chips may be needed. At a minimum a Flash part is needed to store the software and firmware to control the two DLPC3439s. The illumination light that is applied to the DMD is typically from red, green, and blue LEDs. These are often contained in three separate packages, but sometimes more than one color of LED die may be in the same package to reduce the overall size of the projector. Power FETs are needed external to the DLPA3005 so that high LED currents can be supported. For connecting the two DLPC3439s to the front end chip for receiving images the parallel interface is typically used. While using the parallel interface, I²C should be connected to the front end chip for inputting commands to the two DLPC3439s.

Typical Application (continued)

The DLPA3005 has five built-in buck switching regulators to serve as projector system power supplies. Two of the regulators are fixed to 1.1 V and 1.8 V for powering the DLP chip set. The remaining three buck regulators are available for general purpose use and their voltages are programmable. These three regulators can be used to drive variable-speed fans or to power other projector chips such as the front-end chip. The only power supply needed at the DLPA3005 input is SYSPWR from an external DC power supply or internal battery. The entire projector can be turned on and off by using a single signal called PROJ_ON. When PROJ_ON is high, the projector turns on and begins displaying images. When PROJ_ON is set low, the projector turns off and draws just microamps of current on SYSPWR.

8.2.2 Detailed Design Procedure

To connect the 0.47 1080 DMD (DLP4710), two DLPC3439s and DLPA3005, see the reference design schematic. When a circuit board layout is created from this schematic a very small circuit board is possible. An example small board layout is included in the reference design data base. Layout guidelines should be followed to achieve reliable projector operation. The optical engine that has the LED packages and the DMD mounted to it is typically supplied by an optical OEM who specializes in designing optics for DLP projectors.

The component selection of the buck converter is mainly determined by the output voltage. [Table 9](#) shows the recommended value for inductor L_{OUT} and capacitor C_{OUT} for a given output voltage.

Table 9. Recommended Buck Converter L_{OUT} and C_{OUT}

| V_{OUT} (V) | L_{OUT} (μ H) | | | C_{OUT} (μ F) | |
|---------------|----------------------|-----|-----|----------------------|-----|
| | MIN | TYP | MAX | MIN | MAX |
| 1 - 1.5 | 1.5 | 2.2 | 4.7 | 22 | 68 |
| 1.5 - 3.3 | 2.2 | 3.3 | 4.7 | 22 | 68 |
| 3.3 - 5 | 3.3 | | 4.7 | 22 | 68 |

The inductor peak-to-peak ripple current, peak current and RMS current can be calculated using [Equation 8](#), [Equation 9](#) and [Equation 10](#) respectively. The inductor saturation current rating must be greater than the calculated peak current. Likewise, the RMS or heating current rating of the inductor must be greater than the calculated RMS current. The switching frequency of the buck converter is approximately 600 kHz (f_{SWITCH}).

$$I_{L_OUT_RIPPLE_P-P} = \frac{V_{OUT}}{V_{IN_MAX}} \cdot (V_{IN_MAX} - V_{OUT})$$

$$L_{OUT} \cdot f_{SWITCH} \tag{8}$$

$$I_{L_OUT_PEAK} = I_{L_OUT} + \frac{I_{L_OUT_RIPPLE_P-P}}{2} \tag{9}$$

$$I_{L_OUT(RMS)} = \sqrt{I_{L_OUT}^2 + \frac{1}{12} \cdot I_{L_OUT_RIPPLE_P-P}^2} \tag{10}$$

The capacitor value and ESR determines the level of output voltage ripple. The buck converter is intended for use with ceramic or other low ESR capacitors. Recommended values range from 22 to 68 μ F. [Equation 11](#) can be used to determine the required RMS current rating for the output capacitor.

$$I_{C_OUT(RMS)} = \frac{V_{OUT} \cdot (V_{IN} - V_{OUT})}{\sqrt{12} \cdot V_{IN} \cdot L_{OUT} \cdot f_{SWITCH}} \tag{11}$$

Two other components need to be selected in the buck converter configuration. The value of the input-capacitor (pin PWRx_VIN) should be equal or greater than half the selected output capacitance C_{OUT} . In this case $C_{IN} 2 \times 10 \mu$ F is sufficient. The capacitor between PWRx_SWITCH and PWRx_BOOST is a charge pump capacitor to drive the high side FET. The recommended value is 100 nF.

Since the switching edges of the buck converter are relatively fast, voltage overshoot and ringing can become a problem. To overcome this problem a snubber network is used. The snubber circuit consists of a resistor and capacitor that are connected in series from the switch node to ground. The snubber circuit is used to damp the parasitic inductances and capacitances during the switching transitions. This circuit reduces the ringing voltage and also reduces the number of ringing cycles. The snubber network is formed by RSNx and CSNx. More information on controlling switch-node ringing in synchronous buck converters and configuring the snubber can be found in [Analog Applications Journal](#).

8.2.2.1 Component Selection for General-Purpose Buck Converters

The theory of operation of a buck converter is explained in application note, *Understanding Buck Power Stages in Switchmode Power Supplies*, [SLVA057](#). This section is limited to the component selection. For proper operation, selection of the external components is very important, especially the inductor L_{OUT} and the output capacitor C_{OUT} . For best efficiency and ripple performance, an inductor and capacitor should be chosen with low equivalent series resistance (ESR).

8.2.3 Application Curve

As the LED currents that are driven time-sequentially through the red, green, and blue LEDs are increased, the brightness of the projector increases. This increase is somewhat non-linear, and the curve for typical white screen lumens changes with LED currents as shown in [Figure 25](#). For the LED currents shown, it's assumed that the same current amplitude is applied to the red, green, and blue LEDs. The thermal solution used to heatsink the red, green, and blue LEDs can significantly alter the curve shape shown.

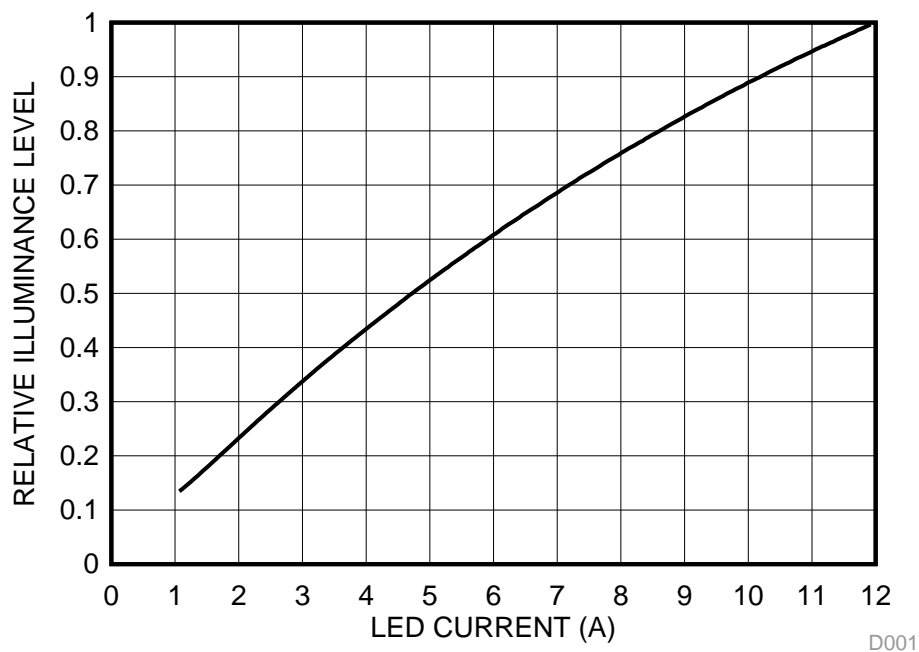


Figure 25. Luminescence vs LED Current

8.3 System Example With DLPA3005 Internal Block Diagram

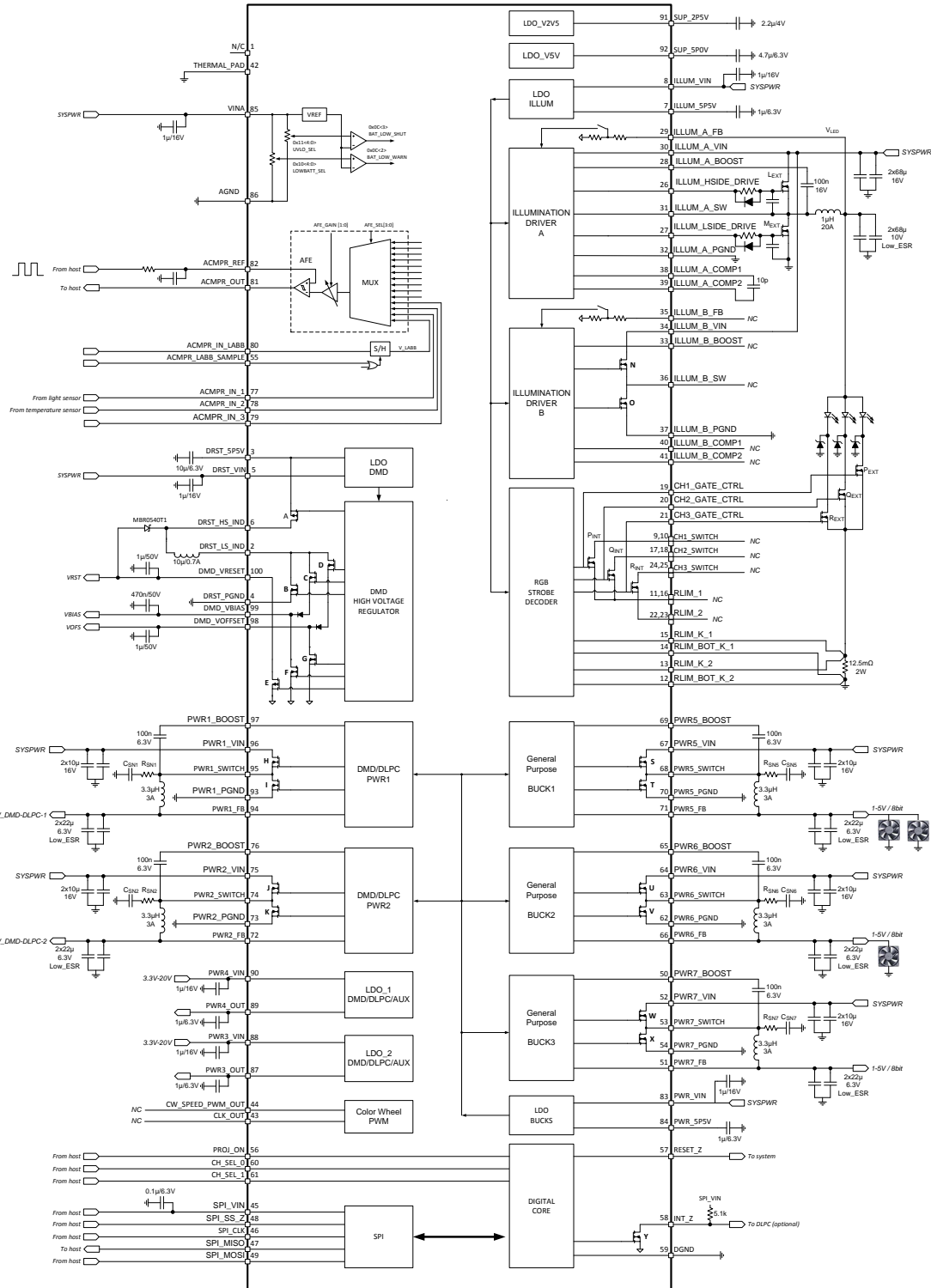


Figure 26. Typical Application: $V_{IN} = 12\text{ V}$, $I_{OUT} = 16\text{ A}$, LED, Internal FETs

9 Power Supply Recommendations

The DLPA3005 is designed to operate from a 6 V to 20 V input voltage supply or battery. To avoid insufficient supply current due to line drop, ringing due to trace inductance at the VIN terminals, or supply peak current limitations, additional bulk capacitance may be required. In the case ringing that is caused by the interaction with the ceramic input capacitors, an electrolytic or tantalum type capacitor may be needed for damping.

The amount of bulk capacitance required should be evaluated such that the input voltage can remain in spec long enough for a proper fast shutdown to occur for the VOFFSET, VRESET, and VBIAS supplies. The shutdown begins when the input voltage drops below the programmable UVLO threshold such as when the external power supply or battery supply is suddenly removed from the system.

9.1 Power-Up and Power-Down Timing

The power-up and power-down sequence is important to ensure a correct operation of the DLPA3005 and to prevent damage to the DMD. The DLPA3005 controls the correct sequencing of the DMD_VRESET, DMD_VBIAS, and DMD_VOFFSET to ensure a reliable operation of the DMD.

The general startup sequence of the supplies is described earlier in [Supply and Monitoring](#). The power-up sequence of the high voltage DMD lines is especially important in order not to damage the DMD. A too large delta voltage between DMD_VBIAS and DMD_VOFFSET could cause the damage and should therefore be prevented.

After PROJ_ON is pulled high, the DMD buck converters and LDOs are powered (PWR1-4) the DMD high voltage lines (HV) are sequentially enabled. First DMD_VOFFSET is enabled. After a delay VOFS_STATE_DURATION (register 0x10) DMD_VBIAS is enabled. Finally, again after a delay VBIAS_STATE_DURATION (register 0x11) DMD_VRESET is enabled. Now the DLPA3005 is fully powered and ready for starting projection.

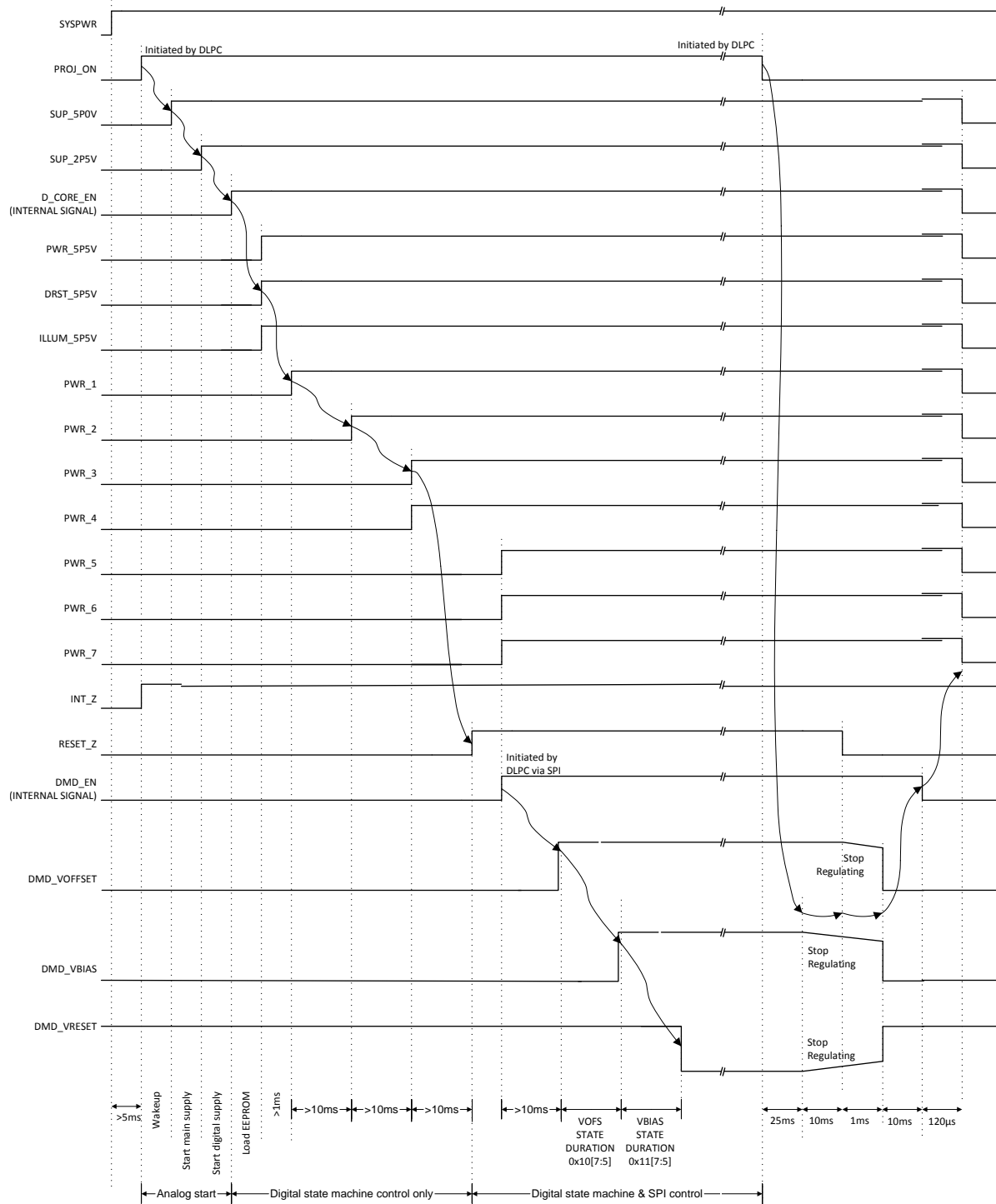
For power down there are two sequences, normal power down ([Figure 27](#)) and a fault fast power down used in case a fault occurs ([Figure 28](#)).

In normal power down mode, the power down is initiated after pulling PROJ_ON pin low. 25 ms after PROJ_ON is pulled low, first DMD_VBIAS and DMD_VRESET stop regulating, 10 ms later followed by DMD_OFFSET. When DMD_OFFSET stopped regulating, RESET_Z is pulled low. 1 ms after the DMD_OFFSET stopped regulating, all three voltages are discharged. Finally, all other supplies are turned off. INT_Z remains high during the power down sequence since no fault occurred. During power down it is ensured that the HV levels do not violate the DMD specifications on these three lines. For this it is important to select the capacitors such that $C_{V\text{OFFSET}}$ is equal to $C_{V\text{RESET}}$ and $C_{V\text{BIAS}}$ is $\leq C_{V\text{OFFSET}}$, $C_{V\text{BIAS}}$.

The fast power down mode ([Figure 28](#)) is started in case a fault occurs (INT_Z will be pulled low), for instance due to overheating. The fast power down mode can be enabled/ disabled via register 0x01, FAST_SHUTDOWN_EN. By default the mode is enabled. After the fault occurs, regulation of DMD_VBIAS and DMD_VRESET is stopped. The time (delay) between fault and stop of regulation can be controlled via register 0x0F (VBIAS/VRST_DELAY). The delay can be selected between 4 μs and ~1.1 ms, where the default is ~540 μs . A defined delay-time after the regulation stopped, all three high voltages lines are discharged and RESET_Z is pulled low. The delay can be controlled via register 0x0F (VOFS/VRESETZ_DELAY). Delay can be selected between 4 μs and ~1.1ms. The default is ~4 μs . Finally the internal DMD_EN signal is pulled low.

Power-Up and Power-Down Timing (continued)

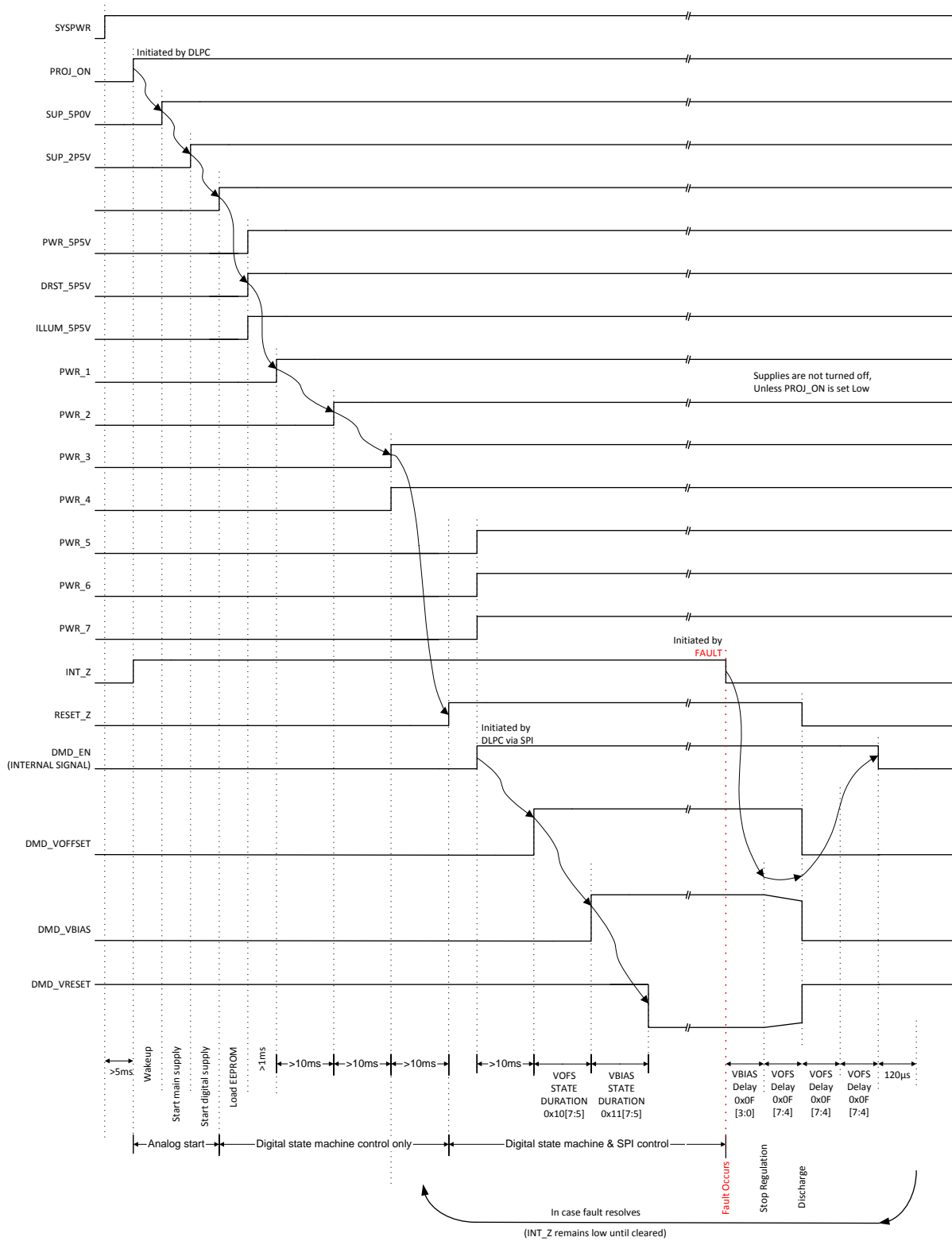
Now the DLPA3005 is in a standby state. It remains in standby state until the fault resolves. In case the fault resolves a restart is initiated. It starts then by powering-up PWR_3 and follows the regular power up as depicted in Figure 28. Again, for proper discharge timing/levels the capacitors should be select such that $C_{V\text{OFFSET}}$ is equal to $C_{V\text{RESET}}$ and $C_{V\text{BIAS}}$ is $\leq C_{V\text{OFFSET}}$.



Note: Arrows indicate sequence of events automatically controlled by digital state machine. Other events are initiated under SPI control.

Figure 27. Power Sequence Normal Shutdown Mode

Power-Up and Power-Down Timing (continued)



Note: Arrows indicate sequence of events automatically controlled by digital state machine. Other events are initiated under SPI control.

Figure 28. Power Sequence Fault Fast Shutdown Mode

10 Layout

10.1 Layout Guidelines

For switching power supplies, the layout is an important step in the design, especially when it concerns high peak currents and high switching frequencies. If the layout is not carefully done, the regulator could show stability issues and/or EMI problems. Therefore, it is recommended to use wide and short traces for high current paths and for their return power ground paths. For the DMD HV regulator, the input capacitor, output capacitor, and the inductor should be placed as close as possible to the IC. In order to minimize ground noise coupling between different buck converters it is advised to separate their grounds and connect them together at a central point under the part. For the DMD HV regulator, the recommended value for the capacitors is 1 μF for VRST and VOFS, 470 nF for VBIAS. The inductor value is 10 μH .

The high currents of the buck converters concentrate around pins VIN, SWITCH and PGND (Figure 29). The voltage at the pins VIN, PGND and FB are DC voltages while the pin SWITCH has a switching voltage between VIN and PGND. In case the FET between pins 52 – 53 is closed the red line indicates the current flow while the blue line indicates the current flow when the FET between pins 53 – 54 is closed.

These paths carry the highest currents and must be kept as short as possible.

For the LDO DMD, it is recommended to use a 1 $\mu\text{F}/16\text{ V}$ capacitor on the input and a 10 $\mu\text{F}/6.3\text{ V}$ capacitor on the output of the LDO assuming a battery voltage of 12 V.

For LDO bucks, it is recommended to use a 1 $\mu\text{F}/16\text{ V}$ capacitor on the input and a 1 $\mu\text{F}/6.3\text{ V}$ capacitor on the output of the LDO.

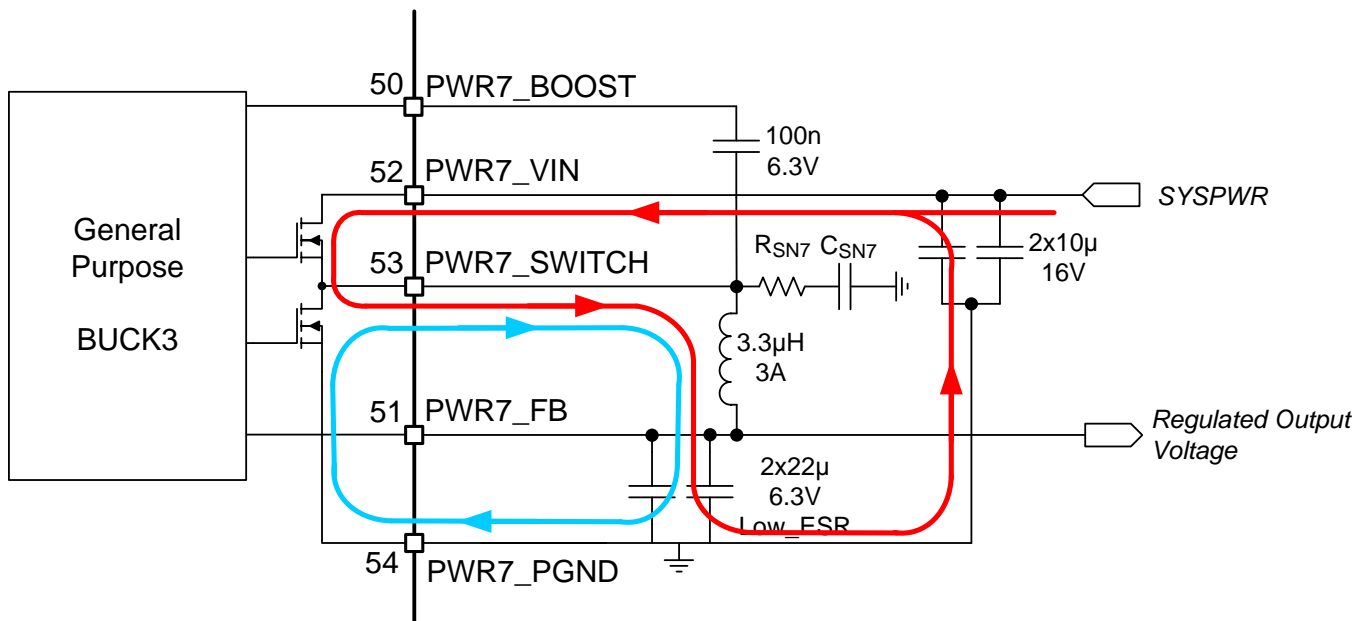


Figure 29. High AC Current Paths in a Buck Converter

The trace to the VIN pin carries high AC currents. Therefore the trace should be low resistive to prevent voltage drop across the trace. Additionally the decoupling capacitors should be placed as close to the VIN pin as possible.

The SWITCH pin is connected alternately to the VIN or GND. This means a square wave voltage is present on the SWITCH pin with an amplitude of VIN, and containing high frequencies. This can lead to EMI problems if not properly handled. To reduce EMI problems a snubber network (RSN7 & CSN7) is placed at the SWITCH pin to prevent and/or suppress unwanted high frequency ringing at the moment of switching.

The PGND pin sinks high current and should be connected to a star ground point such that it does not interfere with other ground connections.

Layout Guidelines (continued)

The FB pin is the sense connection for the regulated output voltage which is a DC voltage; no current is flowing through this pin. The voltage on the FB pin is compared with the internal reference voltage in order to control the loop. The FB connection should be made at the load such that $I \cdot R$ drop is not affecting the sensed voltage.

10.1.1 SPI Connections

The SPI interface consists of several digital lines and the SPI supply. If routing of the interface lines is not done properly, communication errors can occur. It should be prevented that SPI lines can pickup noise and possible interfering sources should be kept away from the interface.

Pickup of noise can be prevented by ensuring that the SPI ground line is routed together with the digital lines as much as possible to the respective pins. The SPI interface should be connected by a separate own ground connection to the DGND of the DLPA3005 (Figure 30). This prevents ground noise between SPI ground references of DLPA3005 and DLPC due to the high current in the system.

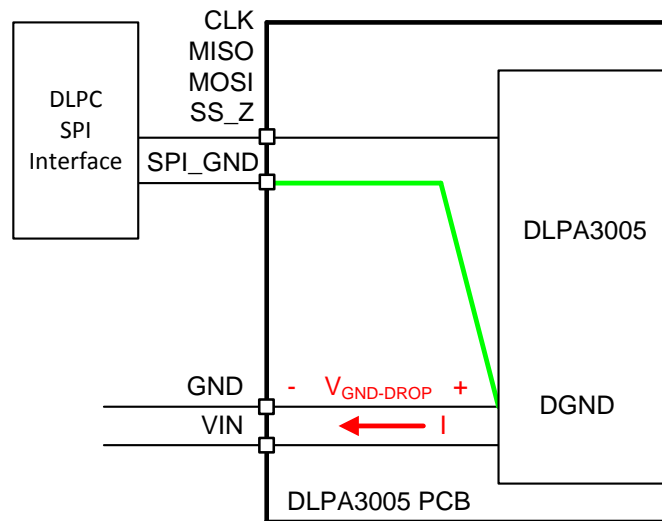


Figure 30. SPI Connections

Interfering sources should be kept away from the interface lines as much as possible. Especially high current lines such as neighboring PWR_7 should be routed carefully. If PWR 7 is routed too close to for instance the SPI_CLK it could lead to false clock pulses and thus communication errors.

10.1.2 R_{LIM} Routing

RLIM is used to sense the LED current. To accurately measure the LED current, the RLIM_K_1,2 lines should be connected close to the top-side of measurement resistor RLIM, while RLIM_BOT_K_1,2 should be connected close to the bottom-side of RLIM.

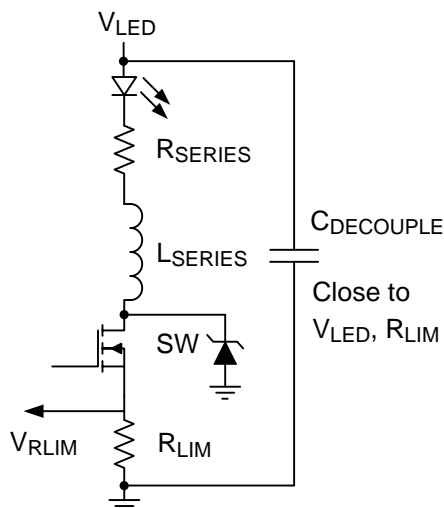
The switched LED current is running through RLIM. Therefore a low-ohmic ground connection for RLIM is strongly advised.

10.1.3 LED Connection

Through the wiring from the external RGB switches to the LEDs switched large currents are running. Therefore special attention needs to be paid here. Two perspectives apply to the LED-to-RGB switches wiring:

1. The resistance of the wiring, R_{series}
2. The inductance of the wiring, L_{series}

The location of the parasitic series impedances are depicted in Figure 31.

Layout Guidelines (continued)

Figure 31. Parasitic Inductance (L_{series}) and Resistance (R_{series}) in Series with LED

Currents up to 16 A can run through the wires connecting the LEDs to the RGB switches. Easily some noticeable dissipation can be caused. Every 10 m Ω of series resistances implies for 16 A average LED current a parasitic power dissipation of 2.5 W. This might cause PCB heating, but more important overall system efficiency is deteriorated.

Additionally the resistance of the wiring might impact the control dynamics of the LED current. It should be noted that the routing resistance is part of the LED current control loop. The LED current is controlled by V_{LED} . For a small change in V_{LED} (ΔV_{LED}) the resulting LED current variation (ΔI_{LED}) is given by the total differential resistance in that path, as:

$$\Delta I_{LED} = \frac{\Delta V_{LED}}{r_{LED} + R_{series} + R_{on_SW_Q3,Q4,Q5} + R_{LIM}}$$

where

- r_{LED} is the differential resistance of the LED
- $R_{on_SW_P,Q,R}$ the on resistance of the strobe decoder switch. (12)

In this expression L_{series} is ignored since realistic values are usually sufficiently low to cause any noticeable impact on the dynamics.

All the comprising differential resistances are in the range of 12.5 m Ω to several 100's m Ω . Without paying special attention a series resistance of 100 m Ω can easily be obtained. It is advised to keep this series resistance sufficiently low, i.e. <10 m Ω .

The series inductance plays an important role when considering the switched nature of the LED current. While cycling through R,G and B LEDs, the current through these branches is turned-on and turned-off in short time duration. Specifically turning off is fast. A current of 16 A goes to 0 A in a matter of 50 ns. This implies a voltage spike of about 1 V for every 5 nH of parasitic inductance. It is recommended to minimize the series inductance of the LED wiring by:

- Short wires
- Thick wires / Multiple parallel wires
- Small enclosed area of the forward and return current path

If the inductance cannot be made sufficiently low, a Zener diode needs to be used to clamp the drain voltage of the RGB switch such it does not surpass the absolute maximum rating. The clamping voltage need to be chosen between the maximum expected V_{LED} and the absolute maximum rating. Take care of sufficient margin of the clamping voltage relative to the mentioned minimum and maximum voltage.

10.2 Layout Example

As an example of a proper layout one of the buck converters layout is shown in [Figure 32](#). It shows the routing and placing of the components around the DLPA3005 for optimal performance. The output voltage of the converters used by the DLPA3005 is set via a register. The DLPA3005 uses the feedback pin to compare the output voltage with an internal setpoint.

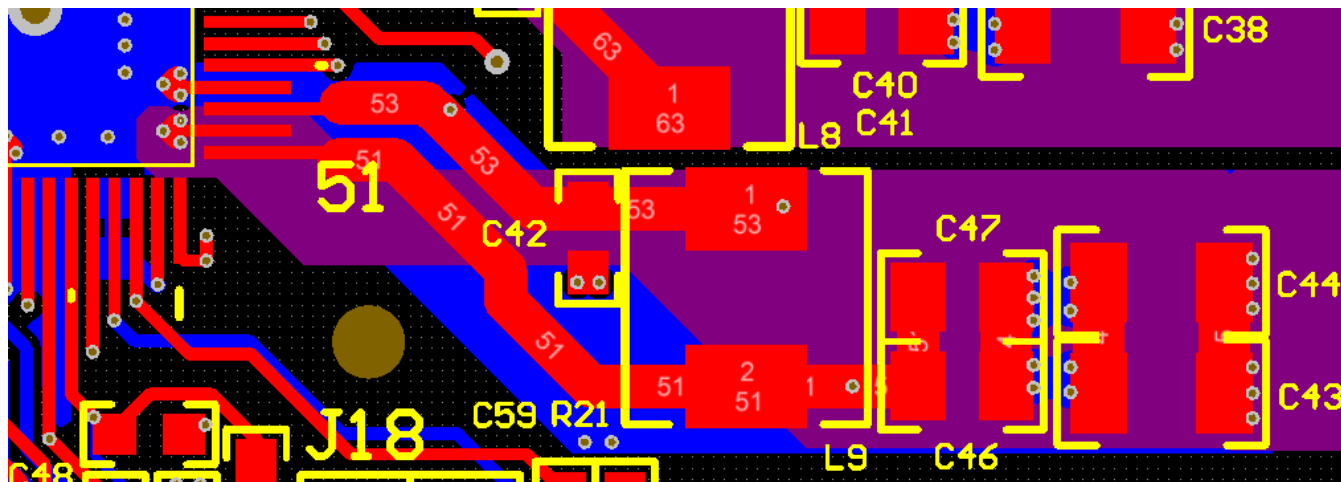


Figure 32. Practical Layout

For a proper layout short traces are required, and power grounds should be separated from each other. This avoids ground shift problems, which can occur due to interference of the ground currents of different buck converters. High currents are flowing through the inductor (L9) and the output capacitors (C46, C47). Therefore it is important to keep the traces to and from inductor and capacitors as short as possible to avoid losses due to trace resistance. It is strongly recommended to use high quality capacitors with a low ESR value to keep the losses in the capacitors as low as possible, and to keep the voltage ripple on the output acceptable.

In order to prevent problems with switching high currents at high frequencies the layout is very critical and snubber networks are advisable. The switching frequency can vary from several hundreds of kHz to frequencies in the MHz range. Keep in mind that it takes only nanoseconds to switch currents from zero to several amperes which is equivalent to even much higher frequencies. Those switching moments will cause EMI problems if not properly handled, especially when ringing occurs on the edges, which can have higher amplitude and frequency as the switching voltage itself. To prevent this ringing the DLPA3005 buck converters all need a snubber network, consisting of a resistor and a capacitor in series implemented on the board to reduce this unwanted behavior. The snubber network is in this case placed on the bottom-side of the PCB (thus not visible here) connected to the trace of L9 routing to the switch node.

In order to make more clear what plays a role when laying out a buck converter, this paragraph explains the connections and placing of the parts around the buck converter connected to the pins 50-54. The supply voltage is connected to pin 52 which is laid out on a mid layer (purple colored) and is connected to this pin using 3 via's to make sure a stable and low resistance connection is made. The decoupling is done by capacitor C43 & C44 visible on the bottom right of [Figure 32](#) and the connection to the supply and the ground layer is done using multiple vias. The ground connection on pin 54 is also done using multiple via's to the ground layer which is visible as the blue areas in [Figure 32](#). By using different layers it is possible to create low resistive paths. Ideally the ground connection of the output capacitors and the ground connection of the part (pin54) should be close together. The layout connects both points together using a wide trace on the bottom layer (blue colored area) which is also suitable to bring both connections together. All buck converters in the layout have the same layout structure and use a separated ground trace to their respective ground connection on the part. All these ground connections are connected together on the ground plane below the DLPA3005 itself. [Figure 32](#) shows the position of the converter inductor and its accompanying capacitors (L9 & C46, C47) as close as possible positioned to the pins 51 and 53 using traces as thick as possible. The ground connections of these capacitors is done using multiple via's to the ground layer to ensure a low resistance path.

10.3 Thermal Considerations

Implementation of integrated circuits in low-profile and fine-pitch surface-mount packages typically requires special attention to power dissipation. Many system-dependent issues such as thermal coupling, airflow, added heat sinks and convection surfaces, and the presence of other heat-generating components affect the power dissipation limits of a given component. In general three basic approaches for enhancing thermal performance can be used; these are listed below:

- Improving the heat sinking capability of the PCB.
- Reducing the thermal resistance to the environment of the chip by adding / increasing heat sink capability on top of the package.
- Adding / increasing airflow in the system.

The DLPA3005 is a device with efficient power converters. Nevertheless, since the power delivered to the LEDs can be quite large, i.e. more than 50 W in some cases, the power dissipated in the DLPA3005 device can still be considerable. In order to have proper operation of the DLPA3005, below guidance is given on the thermal dimensioning of the DLPA3005 application.

Target of the dimensioning is to keep the junction temperature during operation below the maximum recommended of 120°C. In order to determine the junction temperature of the DLPA3005 a summation of all power dissipation terms, P_{diss} , needs to be made. The junction temperature, $T_{junction}$, is then given by:

$$T_{junction} = T_{ambient} + P_{diss} \times R_{\theta JA} \quad (13)$$

in which $T_{ambient}$ is the ambient temperature and $R_{\theta JA}$ is the thermal resistance from junction to ambient.

Depending on the application of the DLPA3005 the total power dissipation can vary. The main contributors in the DLPA3005 will typically be the:

- Buck converters
- LDOs

Below it is shown how to calculate the dissipation for these blocks.

For a buck converter the dissipated power is given by:

$$P_{diss_buck} = P_{in} - P_{out} = P_{out} \left(\frac{1}{\eta_{buck}} - 1 \right) \quad (14)$$

in which η_{buck} is the efficiency of the buck converter, P_{in} the power delivered at the input of the buck converter and P_{out} the power delivered to the load of the buck converter. For buck converter PWR1,2,5,6,7 the efficiency can be determined use curves in [Figure 18](#)

The buck converters potentially handle the highest power levels, that's why they need to be power efficient. In contrast, linear regulator, i.e. LDOs, handle less power. However, since the efficiency of an LDO can be relative low, the related power dissipation can be significant. To calculate the power dissipation of an LDO, P_{diss_LDO} , the following equation can be used:

$$P_{diss_LDO} = (V_{in} - V_{out}) \times I_{load} \quad (15)$$

V_{in} is the input supply voltage, V_{out} is the output voltage of the LDO, and I_{load} is the load current of the LDO. Since the voltage drop over the LDO ($V_{in} - V_{out}$) can be relative large, a relatively small load current can yield significant DLPA3005 dissipation. If this situation occurs, one might consider using one of the general purpose bucks to have a more power efficient, i.e. less dissipation, solution.

One LDO needs some special attention since it is used as the power supply of a boost power converter, i.e. the LDO DMD. The boost converter is used to supply the high voltages for the DMD, i.e. V_{BIAS} , V_{OFS} , V_{RST} . The loading on these lines can be up to $I_{load,max}=10$ mA simultaneously. So, the maximum related power level is moderate. Assuming an efficiency on the order of 80% for the boost converter, η_{boost} , this implies a maximum boost converter dissipation, $P_{diss_DMD_boost,max}$ of:

$$P_{diss_DMD_boost,max} = I_{load,max} (V_{BIAS} + V_{OFS} + |V_{RST}|) \times \left(\frac{1}{\eta_{boost}} - 1 \right) \approx 0.1W \quad (16)$$

Thermal Considerations (continued)

In perspective of the dissipation of the illumination buck converter this is likely negligible. The term that might count to the total power dissipation is $P_{\text{diss_LDO_DMD}}$. The input current of the DMD boost converter is supplied by this LDO. In case of an high supply voltage, a non negligible dissipation term is obtained. The worst case load current for the LDO is given by:

$$I_{\text{load_LDO,max}} = \frac{1}{\eta_{\text{boost}}} \frac{(V_{\text{BIAS}} + V_{\text{OFS}} + |V_{\text{RST}}|)}{V_{\text{DRST_5P5V}}} I_{\text{load,max}} \approx 100\text{mA} \quad (17)$$

In which the output voltage of the LDO is $V_{\text{DRST_5P5V}} = 5.5\text{ V}$.

Thus the dissipation of the LDO, worst case, can be on the order of 1.5 W for an input supply voltage of 19.5 V. This is however, a worst case scenario. In most cases the load current of the LDO DMD is significantly less. It is advised though to check this LDO current level for the specific application.

Finally, the DLPA3005 will draw a quiescent current. This quiescent current is relatively independent of the power supply voltage. For the buck converters the quiescent current is comprised in the efficiency numbers. For the LDOs a quiescent current on the order of 0.5 mA can be used. For the rest of the DLPA3005 circuitry, not included in the buck converters or LDOs, a quiescent current on the order of 3 mA applies. So, overall, when the power dissipation of the buck converters and the LDOs are summed, a good estimate of the DLPA3005 dissipation, $P_{\text{diss_DLPA3005}}$, is obtained. Given as an equation:

$$P_{\text{diss_DLPA3005}} = \sum P_{\text{buck_converter}} + \sum P_{\text{LDOs}} \quad (18)$$

Once this total power dissipation is known, the thermal design can be done. A few examples are given. Assume the total $P_{\text{diss_DLPA3005}} = 2.5\text{ W}$ and the heat sink and airflow is as given in [Thermal Information](#). What is the maximum ambient temperature that can be allowed?

Known parameters: $T_{\text{junction,max}} = 120\text{ }^{\circ}\text{C}$, $R_{\theta\text{JA}} = 7\text{ }^{\circ}\text{C/W}$, $P_{\text{diss_DLPA3005}} = 2.5\text{ W}$.

Using [Equation 13](#) the maximum ambient temperature can be calculated as:

$$T_{\text{ambient,max}} = T_{\text{junction,max}} - P_{\text{diss}} \times R_{\theta\text{JA}} = 120^{\circ}\text{C} - 2.5\text{W} \times 7^{\circ}\text{C/W} = 102.5^{\circ}\text{C} \quad (19)$$

In the same way, the junction temperature of the DLPA3005 can be calculated once the dissipated power and the ambient temperature is known. For instance:

$$T_{\text{ambient}} = 50\text{ }^{\circ}\text{C}, R_{\theta\text{JA}} = 7\text{ }^{\circ}\text{C/W}, P_{\text{diss_DLPA3005}} = 4\text{ W}. \quad (20)$$

For the heat sink configuration and airflow as indicated in [Thermal Information](#), the junction temperature can be calculated to be:

$$T_{\text{junction}} = T_{\text{ambient}} + P_{\text{diss}} \times R_{\theta\text{JA}} = 50^{\circ}\text{C} + 4\text{W} \times 7^{\circ}\text{C/W} = 78^{\circ}\text{C} \quad (21)$$

In case the combination of ambient temperature and DLPA3005 power dissipation does not yield an acceptable junction temperature, that is $<120^{\circ}\text{C}$, basically two approaches can be used:

1. Using larger heat sink / more airflow to reduced $R_{\theta\text{JA}}$
2. Reduce power dissipation in DLPA3005 by for instance not using an internal general purpose buck converter, but an external one. Or lowering loading currents of the bucks.

11 Device and Documentation Support

11.1 Device Support

11.1.1 Device Nomenclature

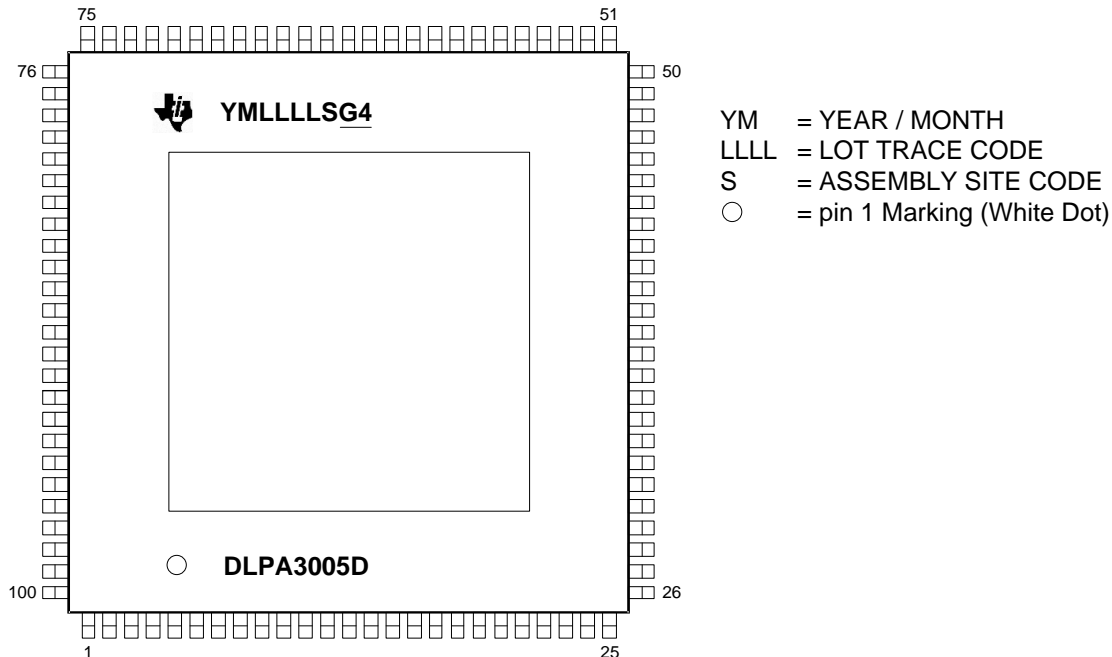


Figure 33. Package Marking DLPA3005 (Top View)

11.2 Related Links

The table below lists quick access links. Categories include technical documents, support and community resources, tools and software, and quick access to sample or buy.

Table 10. Related Links

| PARTS | PRODUCT FOLDER | SAMPLE & BUY | TECHNICAL DOCUMENTS | TOOLS & SOFTWARE | SUPPORT & COMMUNITY |
|----------|----------------------------|----------------------------|----------------------------|----------------------------|----------------------------|
| DLPA3005 | Click here | Click here | Click here | Click here | Click here |
| DLPC3439 | Click here | Click here | Click here | Click here | Click here |

11.3 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's [Terms of Use](#).

TI E2E™ Online Community *TI's Engineer-to-Engineer (E2E) Community*. Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support *TI's Design Support* Quickly find helpful E2E forums along with design support tools and contact information for technical support.

11.4 Trademarks

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 DLP is a registered trademark of Texas Instruments.
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11.5 Electrostatic Discharge Caution



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

11.6 Glossary

[SLYZ022](#) — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

12.1 Package Option Addendum

12.1.1 Packaging Information

| Orderable Device | Status ⁽¹⁾ | Package Type | Package Drawing | Pins | Package Qty | Eco Plan ⁽²⁾ | Lead/Ball Finish | MSL Peak Temp ⁽³⁾ | Op Temp (°C) | Device Marking ⁽⁴⁾⁽⁵⁾ |
|------------------|-----------------------|--------------|-----------------|------|-------------|-------------------------|------------------|------------------------------|--------------|----------------------------------|
| DLPA3005CPFD | LIFEBUY | HTQFP | PFD | 100 | | TBD | Call TI | Level-2-260C-1 YEAR | 0 to 70 | DLPA3005C |
| DLPA3005CPFDR | LIFEBUY | HTQFP | PFD | 100 | | TBD | Call TI | Level-2-260C-1 YEAR | 0 to 70 | DLPA3005C |
| DLPA3005DPFD | ACTIVE | HTQFP | PFD | 100 | 90 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-2-260C-1 YEAR | 0 to 70 | DLPA3005D |
| DLPA3005DPFDR | ACTIVE | HTQFP | PFD | 100 | 1000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-2-260C-1 YEAR | 0 to 70 | DLPA3005D |

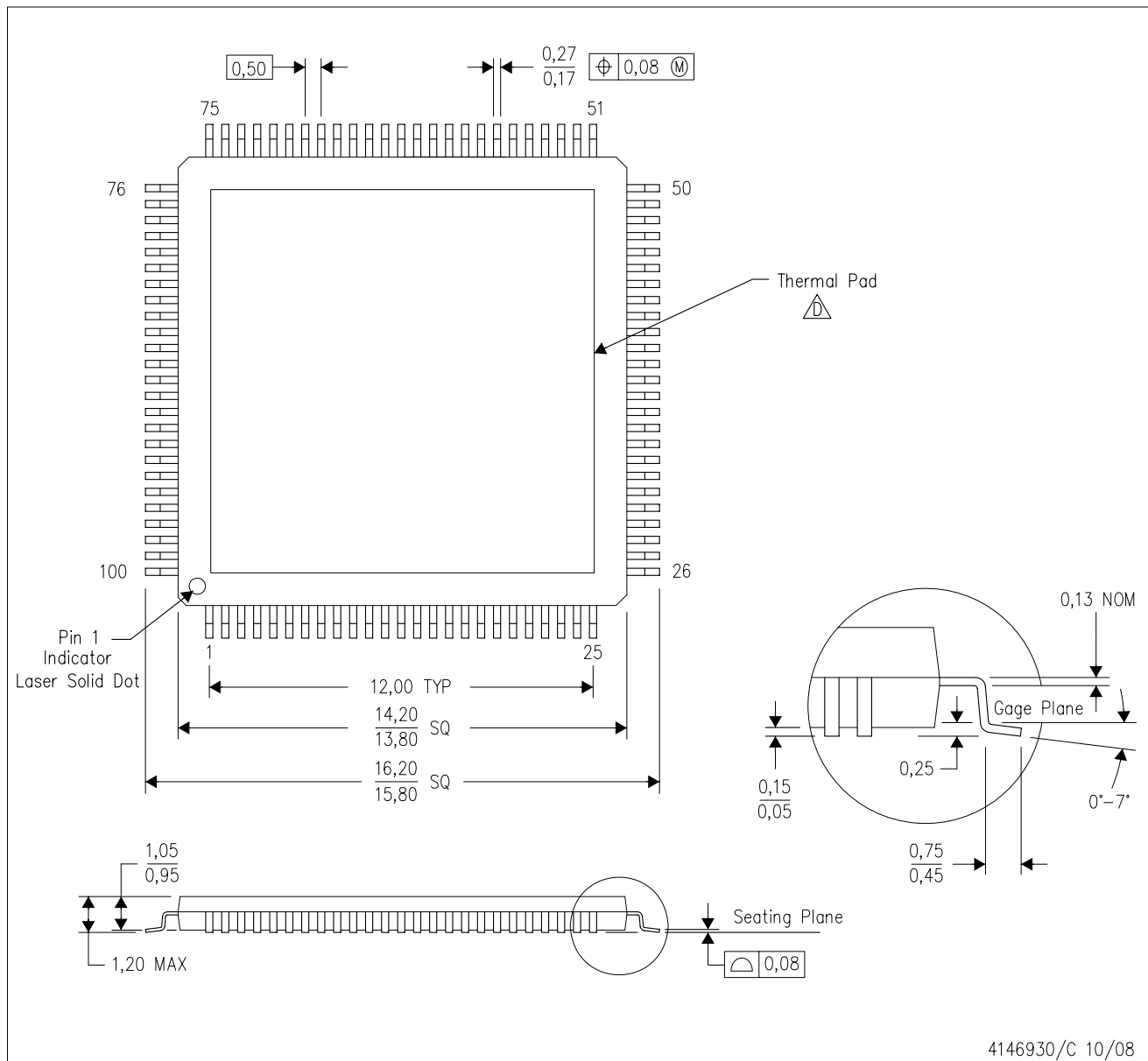
- (1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PRE_PROD Unannounced device, not in production, not available for mass market, nor on the web, samples not available.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.
- (2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
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Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)
- (3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.
- (4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device
- (5) Multiple Device markings will be inside parentheses. Only on Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.


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MECHANICAL DATA

PFD (S-PQFP-G100) PowerPAD™ PLASTIC QUAD FLATPACK (DIE DOWN)



- NOTES:
- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
 - B. This drawing is subject to change without notice.
 - C. Body dimensions do not include mold flash or protrusion.
 -  This package is designed to be attached directly to an external heatsink. Refer to Technical Brief, PowerPAD Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 for information regarding recommended board layout. This document is available at www.ti.com <<http://www.ti.com>>. See the product data sheet for details regarding the exposed thermal pad dimensions.
 - E. Falls within JEDEC MS-026

PowerPAD is a trademark of Texas Instruments.

THERMAL PAD MECHANICAL DATA

PFD (S-PQFP-G100)

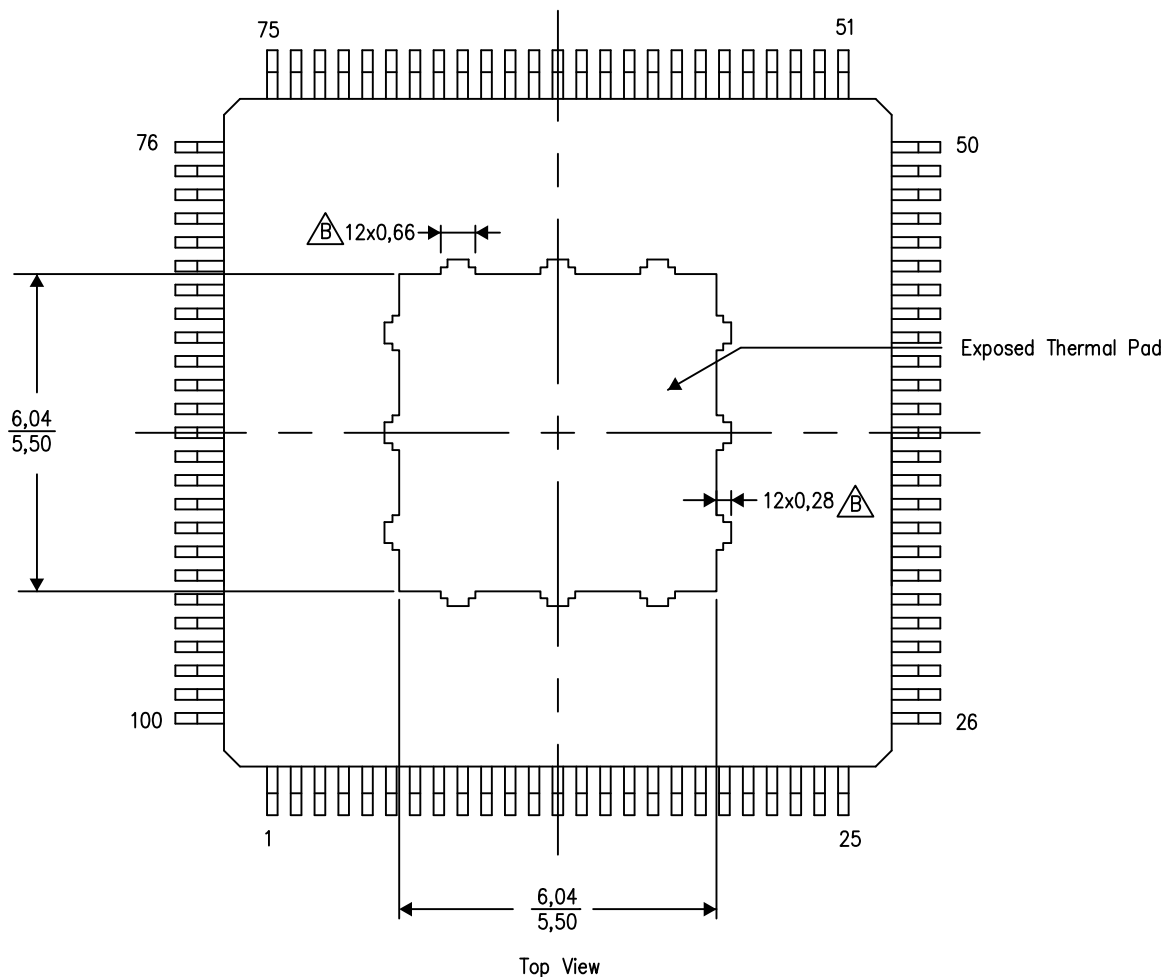
PowerPAD™ PLASTIC QUAD FLATPACK

THERMAL INFORMATION

This PowerPAD™ package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. This design optimizes the heat transfer from the integrated circuit (IC).

For additional information on the PowerPAD package and how to take advantage of its heat dissipating abilities, refer to Technical Brief, PowerPAD Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 and Application Brief, PowerPAD Made Easy, Texas Instruments Literature No. SLMA004. Both documents are available at www.ti.com.


The exposed thermal pad dimensions for this package are shown in the following illustration.



Exposed Thermal Pad Dimensions

4211595-3/B 06/14

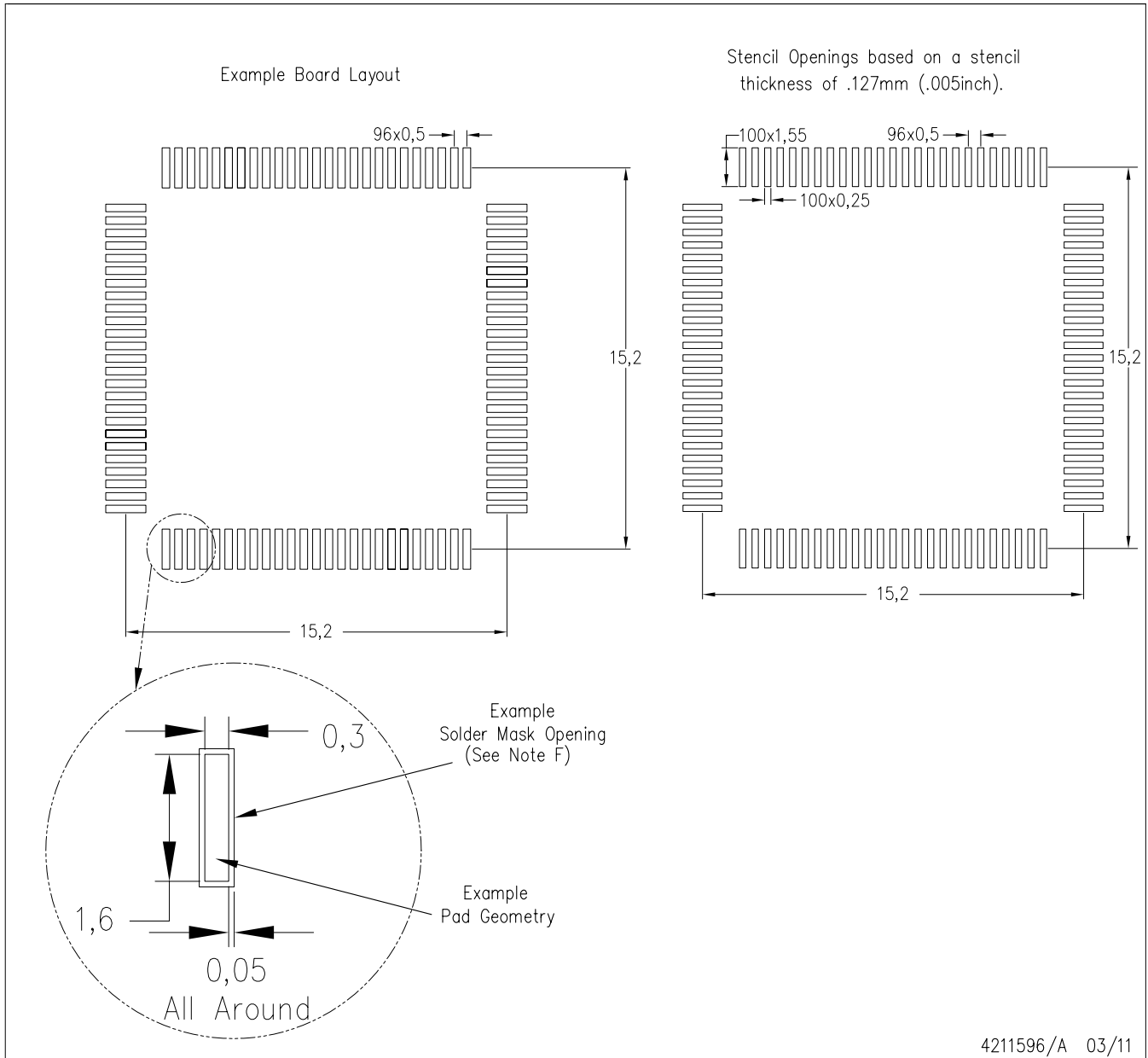
NOTE: A. All linear dimensions are in millimeters

 Tie strap features may not be present.

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PFD (S-PQFP-G100)

PowerPAD™ PLASTIC QUAD FLATPACK



- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC-7525 for other stencil recommendations.
 - D. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

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