P89LPC9102/9103/9107

8-bit microcontrollers with two-clock accelerated 80C51 core 1 kB 3 V byte-erasable flash with 8-bit A/D converter

Rev. 03 — 10 July 2007 Product data sheet

1. General description

The P89LPC9102/9103/9107 are single-chip microcontrollers in low-cost 10-pin and 14-pin packages based on a high performance processor architecture that executes instructions in two to four clocks, six times the rate of standard 80C51 devices. Many system-level functions have been incorporated into the P89LPC9102/9103/9107 in order to reduce component count, board space, and system cost.

2. Features

2.1 Principal features

- 1 kB byte-erasable flash code memory organized into 256-byte sectors and 16-byte pages. Single-byte erasing allows any byte(s) to be used as non-volatile data storage.
- 128-byte RAM data memory.
- Two 16-bit timer/counters (P89LPC9102/9107). Two 16-bit timers (P89LPC9103)
- 23-bit system timer that can also be used as a RTC.
- Four input multiplexed 8-bit A/D converter/single DAC output. One analog comparator with selectable reference.
- Enhanced UART with fractional baud rate generator, break detect, framing error detection, automatic address detection and versatile interrupt capabilities (P89LPC9103/9107).
- High-accuracy internal RC oscillator option, factory calibrated to 1 %, allows operation without external oscillator components. The RC oscillator option is selectable and fine tunable.
- V_{DD} operating range of 2.4 V to 3.6 V with 5 V tolerant I/O pins (may be pulled up or driven to 5.5 V).
- Up to 10 (P89LPC9107) or eight (P89LPC9102/9103) I/O pins when using internal oscillator and reset options.
- Ultra-small 10-pin HVSON package (P89LPC9102/9103). 14-pin TSSOP and DIP packages (P89LPC9107).

2.2 Additional features

- A high performance 80C51 CPU provides instruction cycle times of 136 ns to 272 ns for all instructions except multiply and divide when using the internal 7.3728 MHz RC oscillator in clock doubling mode (111 ns to 222 ns when using an external 18 MHz clock). A lower clock frequency for the same performance results in power savings and reduced EMI.

- In-Application Programming (IAP-Lite) and byte erase allows code memory to be used for non-volatile data storage.
- Serial flash ICP allows simple production coding with commercial EPROM programmers. Flash security bits prevent reading of sensitive application programs.
- Watchdog timer with separate on-chip oscillator, requiring no external components. The watchdog prescaler is selectable from eight values.
- Low voltage reset (Brownout detect) allows a graceful system shutdown when power fails. May optionally be configured as an interrupt.
- Idle mode and two different reduced power Power-down modes. Improved wake-up from Power-down mode (a LOW interrupt input starts execution). Typical Power-down mode current is **less than 1 μA** (total Power-down mode with voltage comparators disabled).
- Active-LOW reset. On-chip power-on reset allows operation without external reset components. A reset counter and reset glitch suppression circuitry prevent spurious and incomplete resets. A software reset function is also available.
- Programmable port output configuration options: quasi-bidirectional, open drain, push-pull, input-only.
- Port ‘input pattern match’ detect. Port 0 may generate an interrupt when the value of the pins match or do not match a programmable pattern.
- LED drive capability (20 mA) on all port pins. A maximum limit is specified for the entire chip.
- Controlled slew rate port outputs to reduce EMI. Outputs have approximately 10 ns minimum ramp times.
- Only power and ground connections are required to operate the P89LPC9102/9103/9107 when internal reset option is selected.
- Four interrupt priority levels.
- Two keypad interrupt inputs.
- Second data pointer.
- External clock input.
- Clock output (P89LPC9102/9107).
- Schmitt trigger port inputs.
- Emulation support.

3. Product comparison overview

Table 1 highlights the differences between these two devices. For a complete list of device features, please see Section 2 “Features”.

Table 1. Product comparison overview

Type number	UART	T0 toggle/PWM	T1 toggle/PWM	CLKOUT
P89LPC9102	-	X	X	X
P89LPC9103	X	-	-	-
P89LPC9107	X	X	X	X

4. Ordering information

Table 2. Ordering information

Type number	Package		
	Name	Description	Version
P89LPC9102FTK	HVSON10	plastic thermal enhanced very thin small outline package; no leads; 10 terminals; body 3 × 3 × 0.85 mm	SOT650-1
P89LPC9103FTK			
P89LPC9107FDH	TSSOP14	plastic thin shrink small outline package; 14 leads; body width 4.4 mm	SOT402-1
P89LPC9107FN	DIP14	plastic dual in-line package; 14 leads (300 mil)	SOT27-1

4.1 Ordering options

Table 3. Ordering options

Type number	Temperature range	Frequency
P89LPC9102FTK	–40 °C to +85 °C	internal RC or watchdog timer
P89LPC9103FTK		
P89LPC9107FDH		
P89LPC9107FN		

5. Block diagram

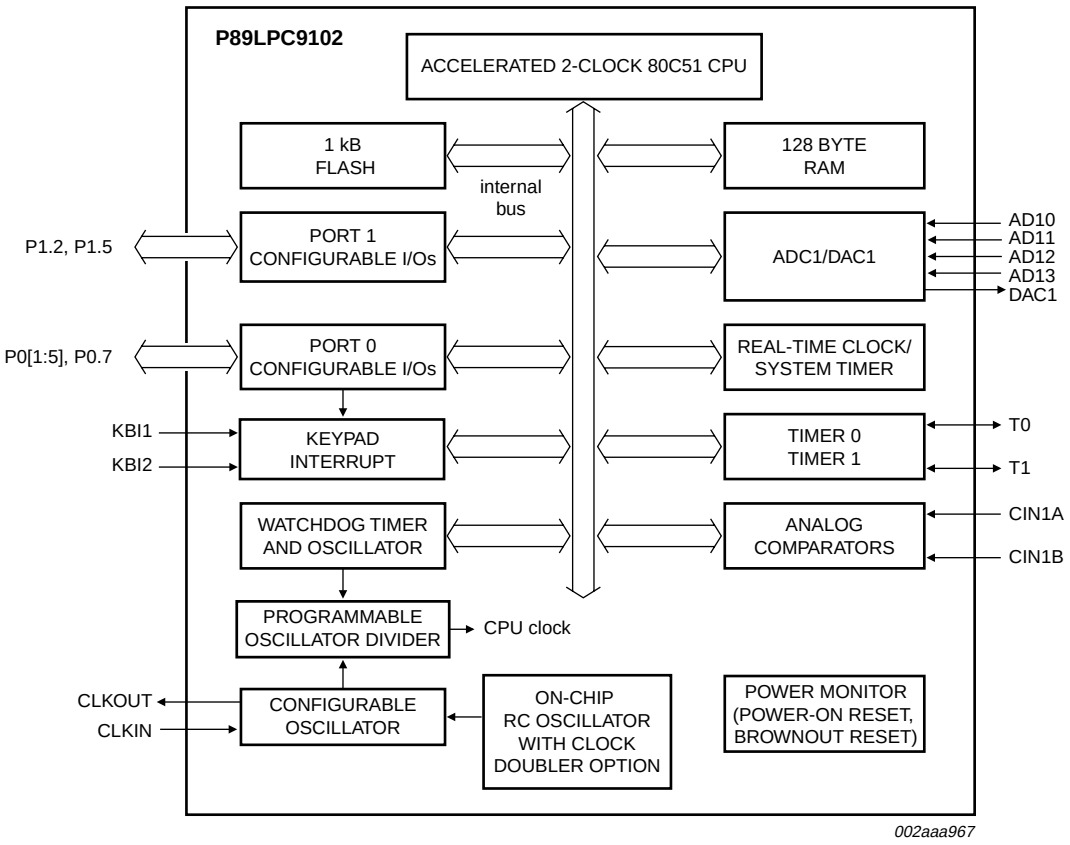


Fig 1. Block diagram of P89LPC9102

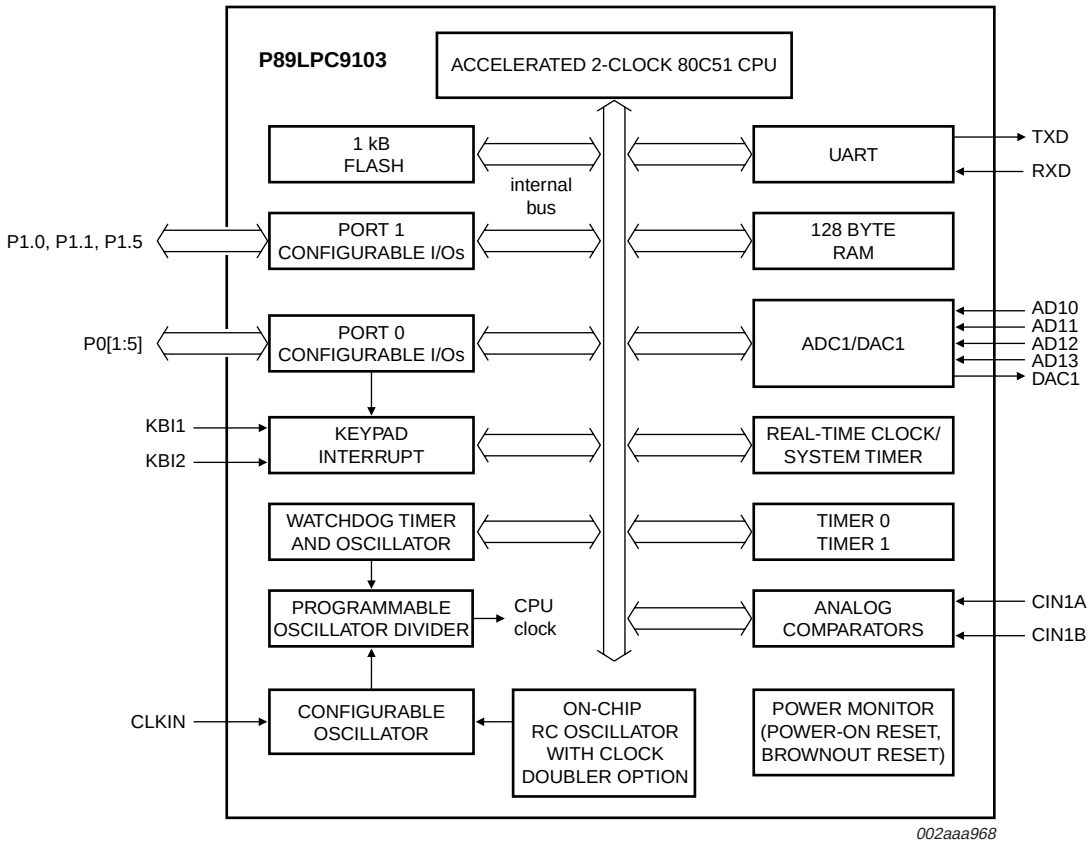


Fig 2. Block diagram of P89LPC9103

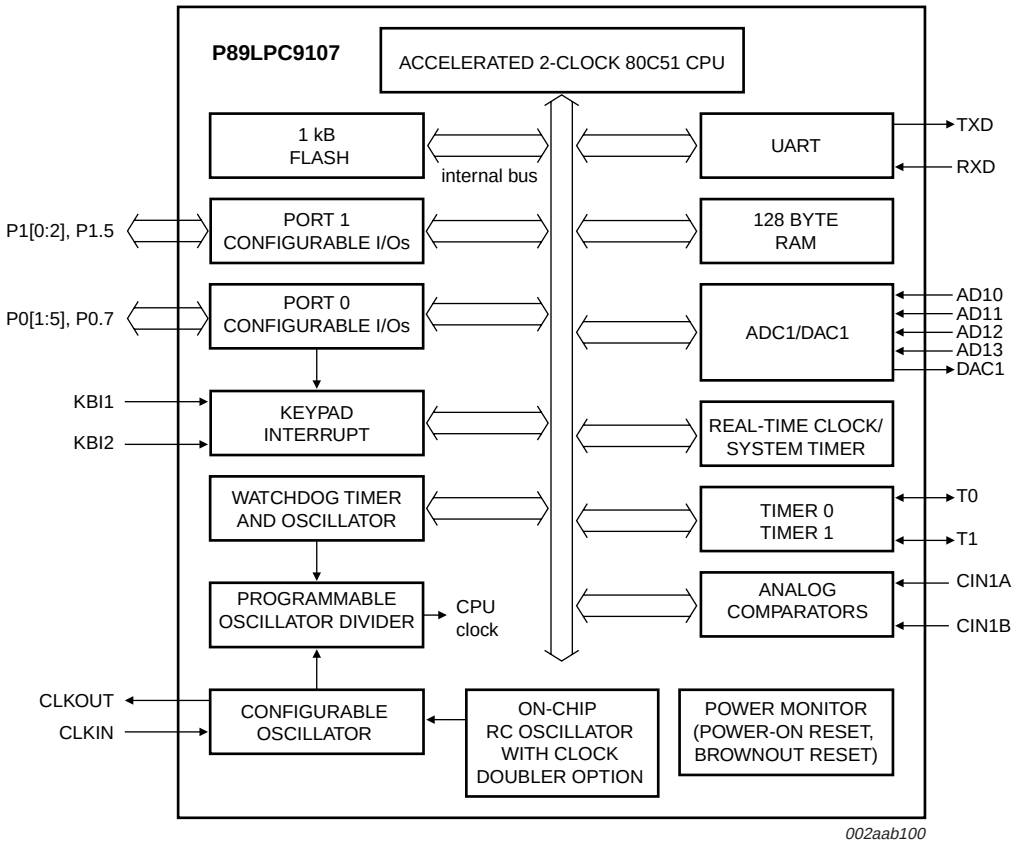


Fig 3. Block diagram of P89LPC9107

6. Functional diagram

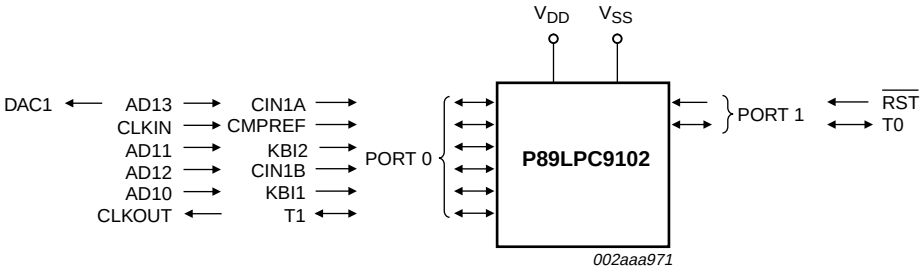


Fig 4. Functional diagram of P89LPC9102

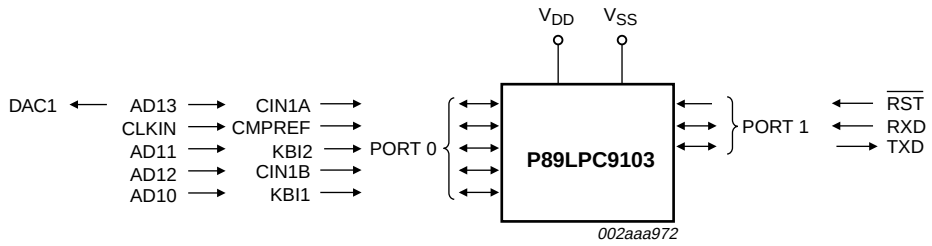


Fig 5. Functional diagram of P89LPC9103

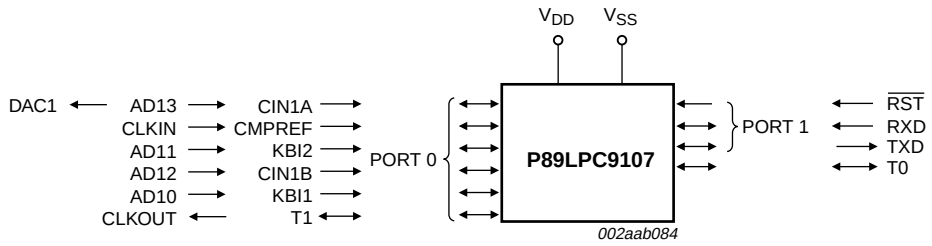
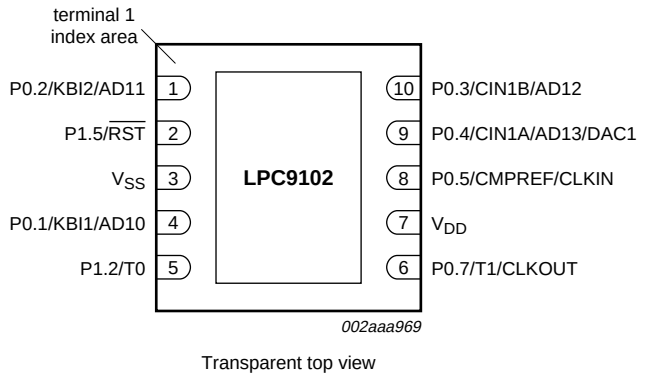


Fig 6. Functional diagram of P89LPC9107

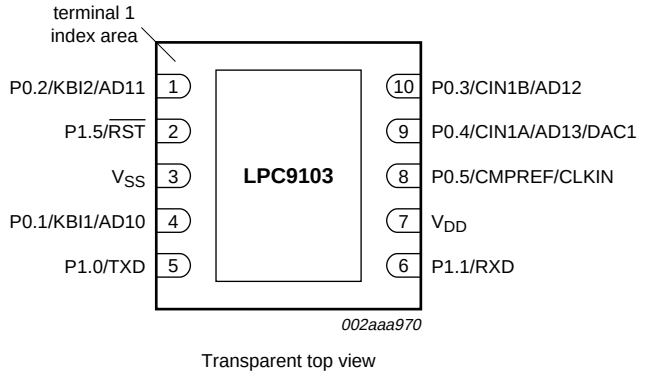
7. Pinning information

7.1 Pinning



Transparent top view

Fig 7. P89LPC9102 pinning (HVSON10)



Transparent top view

Fig 8. P89LPC9103 pinning (HVSON10)

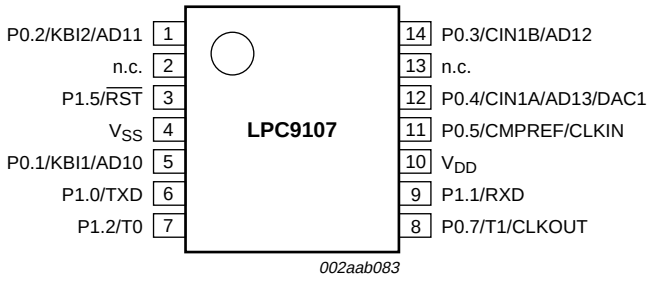


Fig 9. P89LPC9107 pinning (TSSOP14)

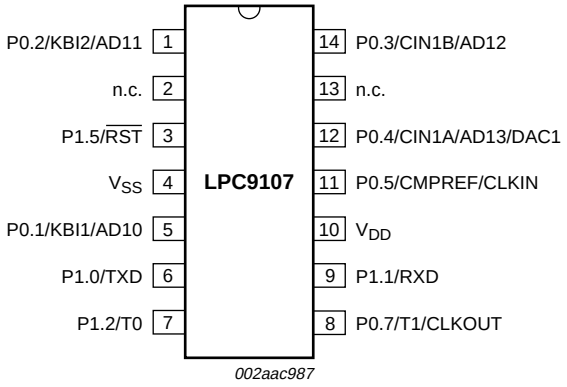


Fig 10. P89LPC9107 pinning (DIP14)

7.2 Pin description

Table 4. P89LPC9102 pin description

Symbol	Pin	Type	Description
P0.1 to P0.5, P0.7		I/O	**Port 0:** Port 0 is an I/O port with a user-configurable output type. During reset Port 0 latches are configured in the input-only mode with the internal pull-up disabled. The operation of Port 0 pins as inputs and outputs depends upon the port configuration selected. Each port pin is configured independently. Refer to Section 8.12.1 “Port configurations” and Table 12 “Static characteristics” for details. The Keypad Interrupt feature operates with Port 0 pins. All pins have Schmitt triggered inputs. Port 0 also provides various special functions as described below:
P0.1/KBI1/ AD10	4	I/O	**P0.1 —** Port 0 bit 1.
		I	**KBI1 —** Keyboard input 1.
		I	**AD10 —** ADC1 channel 0 analog input.
P0.2/KBI2/ AD11	1	I/O	**P0.2 —** Port 0 bit 2.
		I	**KBI2 —** Keyboard input 2.
		I	**AD11 —** ADC1 channel 1 analog input.
P0.3/CIN1B/ AD12	10	I/O	**P0.3 —** Port 0 bit 3.
		I	**CIN1B —** Comparator 1 positive input.
		I	**AD12 —** ADC1 channel 2 analog input.
P0.4/CIN1A/ AD13/DAC1	9	I/O	**P0.4 —** Port 0 bit 4.
		I	**CIN1A —** Comparator 1 positive input.
		I	**AD13 —** ADC1 channel 3 analog input.
		O	**DAC1 —** Digital to analog converter output.
P0.5/CMPREF/CLKIN	8	I/O	**P0.5 —** Port 0 bit 5.
		I	**CMPREF —** Comparator reference (negative) input.
		I	**CLKIN —** External clock input.
P0.7/T1/ CLKOUT	6	I/O	**P0.7 —** Port 0 bit 7.
		I/O	**T1 —** Timer/counter 1 external count input or overflow/PWM output.
		I	**CLKOUT —** Clock output.
P1.2, P1.5		I/O	**Port 1:** Port 1 is an I/O port with a user-configurable output type. During reset Port 1 latches are configured in the input-only mode with the internal pull-up disabled. The operation of the configurable Port 1 pins as inputs and outputs depends upon the port configuration selected. Each of the configurable port pins are programmed independently. Refer to Section 8.12.1 “Port configurations” and Table 12 “Static characteristics” for details. P1.5 is input-only. All pins have Schmitt triggered inputs. Port 1 also provides various special functions as described below:
P1.2/T0	5	I/O	**P1.2 —** Port 1 bit 2.
		I/O	**T0 —** Timer/counter 0 external count input or overflow/PWM output.

Table 4. P89LPC9102 pin description *…continued*

Symbol	Pin	Type	Description
P1.5/$\overline{\text{RST}}$	2	I	**P1.5 —** Port 1 bit 5 (input-only).
		I	**$\overline{\text{RST}}$ —** External Reset input during power-on or if selected via User Configuration Register 1 (UCFG1). When functioning as a reset input a LOW on this pin resets the microcontroller, causing I/O ports and peripherals to take on their default states, and the processor begins execution at address 0. **When using an oscillator frequency above 12 MHz, the reset input function of P1.5 must be enabled. An external circuit is required to hold the device in reset at power-up until V_{DD} has reached its specified level. When system power is removed V_{DD} will fall below the minimum specified operating voltage. When using an oscillator frequency above 12 MHz, in some applications, an external brownout detect circuit may be required to hold the device in reset when V_{DD} falls below the minimum specified operating voltage.**
V_{SS}	3	I	**Ground:** 0 V reference.
V_{DD}	7	I	**Power supply:** This is the power supply voltage for normal operation as well as Idle mode and Power-down mode.

Table 5. P89LPC9103 pin description

Symbol	Pin	Type	Description
P0.1 to P0.5		I/O	**Port 0:** Port 0 is an I/O port with a user-configurable output type. During reset Port 0 latches are configured in the input-only mode with the internal pull-up disabled. The operation of Port 0 pins as inputs and outputs depends upon the port configuration selected. Each port pin is configured independently. Refer to Section 8.12.1 "Port configurations" and Table 12 "Static characteristics" for details. The Keypad Interrupt feature operates with Port 0 pins. All pins have Schmitt triggered inputs. Port 0 also provides various special functions as described below:
P0.1/KBI1/ AD10	4	I/O	**P0.1 —** Port 0 bit 1.
		I	**KBI1 —** Keyboard input 1.
		I	**AD10 —** ADC1 channel 0 analog input.
P0.2/KBI2/ AD11	1	I/O	**P0.2 —** Port 0 bit 2.
		I	**KBI2 —** Keyboard input 2.
		I	**AD11 —** ADC1 channel 1 analog input.
P0.3/CIN1B/ AD12	10	I/O	**P0.3 —** Port 0 bit 3.
		I	**CIN1B —** Comparator 1 positive input.
		I	**AD12 —** ADC1 channel 2 analog input.
P0.4/CIN1A/ AD13/DAC1	9	I/O	**P0.4 —** Port 0 bit 4.
		I	**CIN1A —** Comparator 1 positive input.
		I	**AD13 —** ADC1 channel 3 analog input.
		O	**DAC1 —** Digital to analog converter output.
P0.5/CMPREF/ CLKIN	6	I/O	**P0.5 —** Port 0 bit 5.
		I	**CMPREF —** Comparator reference (negative) input.
		I	**CLKIN —** External clock input.
P1.0 to P1.5		I/O	**Port 1:** Port 1 is an I/O port with a user-configurable output type. During reset Port 1 latches are configured in the input-only mode with the internal pull-up disabled. The operation of the configurable Port 1 pins as inputs and outputs depends upon the port configuration selected. Each of the configurable port pins are programmed independently. Refer to Section 8.12.1 "Port configurations" and Table 12 "Static characteristics" for details. P1.5 is input-only. All pins have Schmitt triggered inputs. Port 1 also provides various special functions as described below:
P1.0/TXD	5	I/O	**P1.0 —** Port 1 bit 0.
		O	**TXD —** Serial port transmitter data.
P1.1/RXD	6	I/O	**P1.1 —** Port 1 bit 1.
		I	**RXD —** Serial port receiver data.

Table 5. P89LPC9103 pin description *…continued*

Symbol	Pin	Type	Description
P1.5/$\overline{\text{RST}}$	2	I	**P1.5 —** Port 1 bit 5 (input-only).
		I	**$\overline{\text{RST}}$ —** External Reset input during Power-on or if selected via UCFG1. When functioning as a reset input a LOW on this pin resets the microcontroller, causing I/O ports and peripherals to take on their default states, and the processor begins execution at address 0. **When using an oscillator frequency above 12 MHz, the reset input function of P1.5 must be enabled. An external circuit is required to hold the device in reset at power-up until V_{DD} has reached its specified level. When system power is removed V_{DD} will fall below the minimum specified operating voltage. When using an oscillator frequency above 12 MHz, in some applications, an external brownout detect circuit may be required to hold the device in reset when V_{DD} falls below the minimum specified operating voltage.**
V_{SS}	3	I	**Ground:** 0 V reference.
V_{DD}	7	I	**Power supply:** This is the power supply voltage for normal operation as well as Idle mode and Power-down mode.

Table 6. P89LPC9107 pin description

Symbol	Pin	Type	Description
P0.1 to P0.5, P0.7		I/O	**Port 0:** Port 0 is an I/O port with a user-configurable output type. During reset Port 0 latches are configured in the input-only mode with the internal pull-up disabled. The operation of Port 0 pins as inputs and outputs depends upon the port configuration selected. Each port pin is configured independently. Refer to Section 8.12.1 “Port configurations” and Table 12 “Static characteristics” for details. The Keypad Interrupt feature operates with Port 0 pins. All pins have Schmitt triggered inputs. Port 0 also provides various special functions as described below:
P0.1/KBI1/ AD10	5	I/O	**P0.1 —** Port 0 bit 1.
		I	**KBI1 —** Keyboard input 1.
		I	**AD10 —** ADC1 channel 0 analog input.
P0.2/KBI2/ AD11	1	I/O	**P0.2 —** Port 0 bit 2.
		I	**KBI2 —** Keyboard input 2.
		I	**AD11 —** ADC1 channel 1 analog input.
P0.3/CIN1B/ AD12	14	I/O	**P0.3 —** Port 0 bit 3.
		I	**CIN1B —** Comparator 1 positive input.
		I	**AD12 —** ADC1 channel 2 analog input.
P0.4/CIN1A/ AD13/DAC1	12	I/O	**P0.4 —** Port 0 bit 4.
		I	**CIN1A —** Comparator 1 positive input.
		I	**AD13 —** ADC1 channel 3 analog input.
		O	**DAC1 —** Digital to analog converter output.
P0.5/CMPREF/ CLKIN	11	I/O	**P0.5 —** Port 0 bit 5.
		I	**CMPREF —** Comparator reference (negative) input.
		I	**CLKIN —** External clock input.
P0.7/T1/ CLKOUT	8	I/O	**P0.7 —** Port 0 bit 7.
		I/O	**T1 —** Timer/counter 1 external count input or overflow/PWM output.
		I	**CLKOUT —** Clock output.

Table 6. P89LPC9107 pin description *…continued*

Symbol	Pin	Type	Description
P1.0 to P1.2, P1.5		I/O	**Port 1:** Port 1 is an I/O port with a user-configurable output type. During reset Port 1 latches are configured in the input-only mode with the internal pull-up disabled. The operation of the configurable Port 1 pins as inputs and outputs depends upon the port configuration selected. Each of the configurable port pins are programmed independently. Refer to Section 8.12.1 "Port configurations" and Table 12 "Static characteristics" for details. P1.5 is input-only. All pins have Schmitt triggered inputs. Port 1 also provides various special functions as described below:
P1.0/TXD	6	I/O	**P1.0 —** Port 1 bit 0.
		O	**TXD —** Serial port transmitter data.
P1.1/RXD	9	I/O	**P1.1 —** Port 1 bit 1.
		I	**RXD —** Serial port receiver data.
P1.2/T0	7	I/O	**P1.2 —** Port 1 bit 2.
		I/O	**T0 —** Timer/counter 0 external count input or overflow/PWM output.
P1.5/$\overline{\text{RST}}$	3	I	**P1.5 —** Port 1 bit 5 (input-only).
		I	**$\overline{\text{RST}}$ —** External Reset input during Power-on or if selected via UCFG1. When functioning as a reset input a LOW on this pin resets the microcontroller, causing I/O ports and peripherals to take on their default states, and the processor begins execution at address 0. **When using an oscillator frequency above 12 MHz, the reset input function of P1.5 must be enabled. An external circuit is required to hold the device in reset at power-up until V_{DD} has reached its specified level. When system power is removed V_{DD} will fall below the minimum specified operating voltage. When using an oscillator frequency above 12 MHz, in some applications, an external brownout detect circuit may be required to hold the device in reset when V_{DD} falls below the minimum specified operating voltage.**
V_{SS}	4	I	**Ground:** 0 V reference.
V_{DD}	10	I	**Power supply:** This is the power supply voltage for normal operation as well as Idle mode and Power-down mode.

8. Functional description

Remark: Please refer to the *P89LPC9102/9103/9107 User manual UM10112* for a more detailed functional description.

8.1 Special function registers

Remark: Special Function Registers (SFRs) accesses are restricted in the following ways:

- User must **not** attempt to access any SFR locations not defined.
- Accesses to any defined SFR locations must be strictly for the functions for the SFRs.
- SFR bits labeled '-', '0' or '1' can **only** be written and read as follows:
  - '-' Unless otherwise specified, **must** be written with '0', but can return any value when read (even if it was written with '0'). It is a reserved bit and may be used in future derivatives.
  - '0' **must** be written with '0', and will return a '0' when read.
  - '1' **must** be written with '1', and will return a '1' when read.

Table 7. P89LPC9102 special function registers

** indicates SFRs that are bit addressable.*

Name	Description	SFR addr.	Bit functions and addresses						
			MSB						
	Bit address		E7	E6	E5	E4	E3	E2	E1
ACC*	Accumulator	E0H							
ADCON1	A/D control register 1	97H	ENBI1	ENADCI 1	TMM1	-	ADCI1	ENADC1	ADCS11
ADINS	A/D input select	A3H	AD13	AD12	AD11	AD10	-	-	-
ADMODA	A/D mode register A	C0H	BNDI1	BURST1	SCC1	SCAN1	-	-	-
ADMODB	A/D mode register B	A1H	CLK2	CLK1	CLK0	-	ENDAC1	-	BSA1
AD1BH	A/D_1 boundary high register	C4H							
AD1BL	A/D_1 boundary low register	BCH							
AD1DAT0	A/D_1 data register 0	D5H							
AD1DAT1	A/D_1 data register 1	D6H							
AD1DAT2	A/D_1 data register 2	D7H							
AD1DAT3	A/D_1 data register 3	F5H							
AUXR1	Auxiliary function register	A2H	CLKLP	EBRR	ENT1	ENT0	SRST	0	-
	Bit address		F7	F6	F5	F4	F3	F2	F1
B*	B register	F0H							
CMP1	Comparator 1 control register	ACH	-	-	CE1	CP1	CN1	-	CO1
DIVM	CPU clock divide-by-M control	95H							
DPTR	Data pointer (2 bytes)								
DPH	Data pointer high	83H							
DPL	Data pointer low	82H							
FMADRH	Program flash address high	E7H							
FMADRL	Program flash address low	E6H							
FMCON	Program flash Control (Read)	E4H	BUSY	-	-	-	HVA	HVE	SV
	Program flash Control (Write)		FMCMD. 7	FMCMD. 6	FMCMD. 5	FMCMD. 4	FMCMD. 3	FMCMD. 2	FMCMD. 1
FMDATA	Program flash data	E5H							
IEN0*	Interrupt enable 0	A8H	EA	EWDRT	EBO	-	ET1	-	ET0

Table 7. P89LPC9102 special function registers *...continued*

** indicates SFRs that are bit addressable.*

Name	Description	SFR addr.	Bit functions and addresses						
			MSB						
		Bit address	EF	EE	ED	EC	EB	EA	E9
IEN1*	Interrupt enable 1	E8H	EAD	-	-	-	-	EC	EKBI
		Bit address	BF	BE	BD	BC	BB	BA	B9
IP0*	Interrupt priority 0	B8H	-	PWDRT	PBO	-	PT1	-	PT0
IP0H	Interrupt priority 0 high	B7H	-	PWDRTH	PBOH	-	PT1H	-	PT0H
		Bit address	FF	FE	FD	FC	FB	FA	F9
IP1*	Interrupt priority 1	F8H	PAD	-	-	-	-	PC	PKBI
IP1H	Interrupt priority 1 high	F7H	PADH	-	-	-	-	PCH	PKBIH
KBCON	Keypad control register	94H	-	-	-	-	-	-	PATN_SEL
KBMASK	Keypad interrupt mask register	86H		-	-	-	KBMASK.2	KBMASK.1	-
KBPATN	Keypad pattern register	93H	-	-	-	-	KBPATN.2	KBPATN.1	-
		Bit address	87	86	85	84	83	82	81
P0*	Port 0	80H	CLKOUT/T1	-	CMPREF/CLKIN	CIN1A	CIN1B	CIN2A/KBI2	KBI1
		Bit address	97	96	95	94	93	92	91
P1*	Port 1	90H	-	-	$\overline{\text{RST}}$	-	-	T0	-
P0M1	Port 0 output mode 1	84H	(P0M1.7)	-	(P0M1.5)	(P0M1.4)	(P0M1.3)	(P0M1.2)	(P0M1.1)
P0M2	Port 0 output mode 2	85H	(P0M2.7)	-	(P0M2.5)	(P0M2.4)	(P0M2.3)	(P0M2.2)	(P0M2.1)
P1M1	Port 1 output mode 1	91H	-	-	-	-	-	(P1M1.2)	-
P1M2	Port 1 output mode 2	92H	-	-	-	-	-	(P1M2.2)	-
PCON	Power control register	87H	-	-	BOPD	BOI	GF1	GF0	PMOD1
PCONA	Power control register A	B5H	RTCPD		VCPD	ADPD		-	-
PCONB	reserved for Power control register B	B6H	-	-	-	-	-	-	-
		Bit address	D7	D6	D5	D4	D3	D2	D1
PSW*	Program status word	D0H	CY	AC	F0	RS1	RS0	OV	F1
PT0AD	Port 0 digital input disable	F6H	-	-	PT0AD.5	PT0AD.4	PT0AD.3	PT0AD.2	PT0AD.1

Table 7. P89LPC9102 special function registers *...continued*

** indicates SFRs that are bit addressable.*

Name	Description	SFR addr.	Bit functions and addresses						
			MSB						
RSTSRC	Reset source register	DFH	-	-	BOF	POF	-	R_WD	R_SF
RTCCON	Real-time clock control	D1H	RTCF	RTCS1	RTCS0	-	-	-	ERTC
RTCH	Real-time clock register high	D2H							
RTCL	Real-time clock register low	D3H							
SP	Stack pointer	81H							
TAMOD	Timer 0 and 1 auxiliary mode	8FH	-	-	-	T1M2	-	-	-
	Bit address		**8F**	**8E**	**8D**	**8C**	**8B**	**8A**	**89**
TCON*	Timer 0 and 1 control	88H	TF1	TR1	TF0	TR0	-	-	-
TH0	Timer 0 high	8CH							
TH1	Timer 1 high	8DH							
TL0	Timer 0 low	8AH							
TL1	Timer 1 low	8BH							
TMOD	Timer 0 and 1 mode	89H	-	-	T1M1	T1M0	-	-	T0M1
TRIM	Internal oscillator trim register	96H	RCCLK	ENCLK	TRIM.5	TRIM.4	TRIM.3	TRIM.2	TRIM.1
WDCON	Watchdog control register	A7H	PRE2	PRE1	PRE0	-	-	WDRUN	WDTOF
WDL	Watchdog load	C1H							
WFEED1	Watchdog feed 1	C2H							
WFEED2	Watchdog feed 2	C3H							

[1] Unimplemented bits in SFRs (labeled '-') are X (unknown) at all times. Unless otherwise specified, ones should not be written to these bits sin purposes in future derivatives. The reset values shown for these bits are logic 0s although they are unknown when read.

[2] All ports are in input-only (high-impedance) state after power-up.

[3] The RSTSRC register reflects the cause of the P89LPC9102/9103/9107 reset. Upon a power-up reset, all reset source flags are cleared excep value is xx11 0000.

[4] The only reset source that affects these SFRs is power-on reset.

[5] On power-on reset, the TRIM SFR is initialized with a factory preprogrammed value. Other resets will not cause initialization of the TRIM regis

[6] After reset, the value is 1110 01x1, i.e., PRE2 to PRE0 are all logic 1s, WDRUN = 1 and WDCLK = 1. WDTOF bit is logic 1 after watchdog time reset. Other resets will not affect WDTOF.

Table 8. P89LPC9103 special function registers

** indicates SFRs that are bit addressable.*

Name	Description	SFR addr.	Bit functions and addresses						
			MSB						
	Bit address		E7	E6	E5	E4	E3	E2	E1
ACC*	Accumulator	E0H							
ADCON1	A/D control register 1	97H	ENBI1	ENADCI 1	TMM1	-	ADCI1	ENADC1	ADCS11
ADINS	A/D input select	A3H	AD13	AD12	AD11	AD10	-	-	-
ADMODA	A/D mode register A	C0H	BNDI1	BURST1	SCC1	SCAN1	-	-	-
ADMODB	A/D mode register B	A1H	CLK2	CLK1	CLK0	-	ENDAC1	-	BSA1
AD1BH	A/D_1 boundary high register	C4H							
AD1BL	A/D_1 boundary low register	BCH							
AD1DAT0	A/D_1 data register 0	D5H							
AD1DAT1	A/D_1 data register 1	D6H							
AD1DAT2	A/D_1 data register 2	D7H							
AD1DAT3	A/D_1 data register 3	F5H							
AUXR1	Auxiliary function register	A2H	CLKLP	EBRR	-	-	SRST	0	-
	Bit address		F7	F6	F5	F4	F3	F2	F1
B*	B register	F0H							
BRGR0[2]	Baud rate generator rate low	BEH							
BRGR1[2]	Baud rate generator rate high	BFH							
BRGCON	Baud rate generator control	BDH	-	-	-	-	-	-	SBRGS
CMP1	Comparator 1 control register	ACH	-	-	CE1	CP1	CN1	-	CO1
DIVM	CPU clock divide-by-M control	95H							
DPTR	Data pointer (2 bytes)								
DPH	Data pointer high	83H							
DPL	Data pointer low	82H							
FMADRH	Program flash address high	E7H							
FMADRL	Program flash address low	E6H							
FMCON	Program flash Control (Read)	E4H	BUSY	-	-	-	HVA	HVE	SV
	Program flash Control (Write)		FMCMD. 7	FMCMD. 6	FMCMD. 5	FMCMD. 4	FMCMD. 3	FMCMD. 2	FMCMD. 1

Table 8. P89LPC9103 special function registers *...continued*

** indicates SFRs that are bit addressable.*

Name	Description	SFR addr.	Bit functions and addresses						
			MSB						
FMDATA	Program flash data	E5H							
IEN0*	Interrupt enable 0	A8H	EA	EWDRT	EBO	ES/ESR	ET1	-	ET0
		Bit address	**EF**	**EE**	**ED**	**EC**	**EB**	**EA**	**E9**
IEN1*	Interrupt enable 1	E8H	EAD	EST	-	-	-	EC	EKBI
		Bit address	**BF**	**BE**	**BD**	**BC**	**BB**	**BA**	**B9**
IP0*	Interrupt priority 0	B8H	-	PWDRT	PBO	PS/PSR	PT1	-	PT0
IP0H	Interrupt priority 0 high	B7H	-	PWDRTH	PBOH	PSH /PSRH	PT1H	-	PT0H
		Bit address	**FF**	**FE**	**FD**	**FC**	**FB**	**FA**	**F9**
IP1*	Interrupt priority 1	F8H	PAD	PST	-	-	-	PC	PKBI
IP1H	Interrupt priority 1 high	F7H	PADH	PSTH	-	-	-	PCH	PKBIH
KBCON	Keypad control register	94H	-	-	-	-	-	-	PATN_SEL
KBMASK	Keypad interrupt mask register	86H		-	-	-	-	KBMASK.2	KBMASK.1
KBPATN	Keypad pattern register	93H	-	-	-	-	-	KBPATN.2	KBPATN.1
		Bit address	**87**	**86**	**85**	**84**	**83**	**82**	**81**
P0*	Port 0	80H	-	-	CMPREF /CLKIN	CIN1A	CIN1B	KBI2	KBI1
		Bit address	**97**	**96**	**95**	**94**	**93**	**92**	**91**
P1*	Port 1	90H	-	-	$\overline{\text{RST}}$	-	-	-	RXD
P0M1	Port 0 output mode 1	84H	-	-	(P0M1.5)	(P0M1.4)	(P0M1.3)	(P0M1.2)	(P0M1.1)
P0M2	Port 0 output mode 2	85H	-	-	(P0M2.5)	(P0M2.4)	(P0M2.3)	(P0M2.2)	(P0M2.1)
P1M1	Port 1 output mode 1	91H	-	-	-	-	-	-	(P1M1.1)
P1M2	Port 1 output mode 2	92H	-	-	-	-	-	-	(P1M2.1)
PCON	Power control register	87H	SMOD1	SMOD0	BOPD	BOI	GF1	GF0	PMOD1
PCONA	Power control register A	B5H	RTCPD		VCPD	ADPD		-	SPD
PCONB	reserved for Power control register B	B6H	-	-	-	-	-	-	-

Table 8. P89LPC9103 special function registers *...continued*

** indicates SFRs that are bit addressable.*

Name	Description	SFR addr.	Bit functions and addresses						
			MSB						
	Bit address		**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**
PSW*	Program status word	D0H	CY	AC	F0	RS1	RS0	OV	F1
PT0AD	Port 0 digital input disable	F6H	-	-	PT0AD.5	PT0AD.4	PT0AD.3	PT0AD.2	PT0AD.1
RSTSRC	Reset source register	DFH	-	-	BOF	POF	R_BK	R_WD	R_SF
RTCCON	Real-time clock control	D1H	RTCF	RTCS1	RTCS0	-	-	-	ERTC
RTCH	Real-time clock register high	D2H							
RTCL	Real-time clock register low	D3H							
SADDR	Serial port address register	A9H							
SADEN	Serial port address enable	B9H							
SBUF	Serial port data buffer register	99H							
	Bit address		**9F**	**9E**	**9D**	**9C**	**9B**	**9A**	**99**
SCON*	Serial port control	98H	SM0/FE	SM1	SM2	REN	TB8	RB8	TI
SSTAT	Serial port extended status register	BAH	DBMOD	INTLO	CIDIS	DBISEL	FE	BR	OE
SP	Stack pointer	81H							
	Bit address		**8F**	**8E**	**8D**	**8C**	**8B**	**8A**	**89**
TCON*	Timer 0 and 1 control	88H	TF1	TR1	TF0	TR0	-	-	-
TH0	Timer 0 high	8CH							
TH1	Timer 1 high	8DH							
TL0	Timer 0 low	8AH							
TL1	Timer 1 low	8BH							
TMOD	Timer 0 and 1 mode	89H	-	-	T1M1	T1M0	-	-	T0M1
TRIM	Internal oscillator trim register	96H	RCCLK	-	TRIM.5	TRIM.4	TRIM.3	TRIM.2	TRIM.1
WDCON	Watchdog control register	A7H	PRE2	PRE1	PRE0	-	-	WDRUN	WDTOF
WDL	Watchdog load	C1H							
WFEED1	Watchdog feed 1	C2H							
WFEED2	Watchdog feed 2	C3H							

[1] Unimplemented bits in SFRs (labeled '-') are X (unknown) at all times. Unless otherwise specified, ones should not be written to these bits sin purposes in future derivatives. The reset values shown for these bits are logic 0s although they are unknown when read.

[2] BRGR1 and BRGR0 must only be written if BRGEN in BRGCON SFR is logic 0. If any are written while BRGEN = 1, the result is unpredictabl

[3] All ports are in input-only (high-impedance) state after power-up.

[4] The RSTSRC register reflects the cause of the P89LPC9102/9103/9107 reset. Upon a power-up reset, all reset source flags are cleared except POF; their value is xx11 0000.

[5] The only reset source that affects these SFRs is power-on reset.

[6] On power-on reset, the TRIM SFR is initialized with a factory preprogrammed value. Other resets will not cause initialization of the TRIM register.

[7] After reset, the value is 1110 01x1, i.e., PRE2 to PRE0 are all logic 1s, WDRUN = 1 and WDCLK = 1. WDTOF bit is logic 1 after watchdog time-out reset. Other resets will not affect WDTOF.

Table 9. P89LPC9107 special function registers

** indicates SFRs that are bit addressable.*

Name	Description	SFR addr.	Bit functions and addresses						
			MSB						
	Bit address		E7	E6	E5	E4	E3	E2	E1
ACC*	Accumulator	E0H							
ADCON1	A/D control register 1	97H	ENBI1	ENADCI 1	TMM1	-	ADCI1	ENADC1	ADCS11
ADINS	A/D input select	A3H	AD13	AD12	AD11	AD10	-	-	-
ADMODA	A/D mode register A	C0H	BNDI1	BURST1	SCC1	SCAN1	-	-	-
ADMODB	A/D mode register B	A1H	CLK2	CLK1	CLK0	-	ENDAC1	-	BSA1
AD1BH	A/D_1 boundary high register	C4H							
AD1BL	A/D_1 boundary low register	BCH							
AD1DAT0	A/D_1 data register 0	D5H							
AD1DAT1	A/D_1 data register 1	D6H							
AD1DAT2	A/D_1 data register 2	D7H							
AD1DAT3	A/D_1 data register 3	F5H							
AUXR1	Auxiliary function register	A2H	CLKLP	EBRR	ENT1	ENT0	SRST	0	-
	Bit address		F7	F6	F5	F4	F3	F2	F1
B*	B register	F0H							
BRGR0[2]	Baud rate generator rate low	BEH							
BRGR1[2]	Baud rate generator rate high	BFH							
BRGCON	Baud rate generator control	BDH	-	-	-	-	-	-	SBRGS
CMP1	Comparator 1 control register	ACH	-	-	CE1	CP1	CN1	-	CO1
DIVM	CPU clock divide-by-M control	95H							
DPTR	Data pointer (2 bytes)								
DPH	Data pointer high	83H							
DPL	Data pointer low	82H							
FMADRH	Program flash address high	E7H							
FMADRL	Program flash address low	E6H							
FMCON	Program flash Control (Read)	E4H	BUSY	-	-	-	HVA	HVE	SV
	Program flash Control (Write)		FMCMD.7	FMCMD.6	FMCMD.5	FMCMD.4	FMCMD.3	FMCMD.2	FMCMD.1

Table 9. P89LPC9107 special function registers *...continued*

** indicates SFRs that are bit addressable.*

Name	Description	SFR addr.	Bit functions and addresses						
			MSB						
FMDATA	Program flash data	E5H							
IEN0*	Interrupt enable 0	A8H	EA	EWDRT	EBO	ES/ESR	ET1	-	ET0
		Bit address	**EF**	**EE**	**ED**	**EC**	**EB**	**EA**	**E9**
IEN1*	Interrupt enable 1	E8H	EAD	EST	-	-	-	EC	EKBI
		Bit address	**BF**	**BE**	**BD**	**BC**	**BB**	**BA**	**B9**
IP0*	Interrupt priority 0	B8H	-	PWDRT	PBO	PS/PSR	PT1	-	PT0
IP0H	Interrupt priority 0 high	B7H	-	PWDRTH	PBOH	PSH /PSRH	PT1H	-	PT0H
		Bit address	**FF**	**FE**	**FD**	**FC**	**FB**	**FA**	**F9**
IP1*	Interrupt priority 1	F8H	PAD	PST	-	-	-	PC	PKBI
IP1H	Interrupt priority 1 high	F7H	PADH	PSTH	-	-	-	PCH	PKBIH
KBCON	Keypad control register	94H	-	-	-	-	-	-	PATN_SEL
KBMASK	Keypad interrupt mask register	86H		-	-	-	-	KBMASK.2	KBMASK.1
KBPATN	Keypad pattern register	93H	-	-	-	-	-	KBPATN.2	KBPATN.1
		Bit address	**87**	**86**	**85**	**84**	**83**	**82**	**81**
P0*	Port 0	80H	-	-	CMPREF /CLKIN	CIN1A	CIN1B	KBI2	KBI1
		Bit address	**97**	**96**	**95**	**94**	**93**	**92**	**91**
P1*	Port 1	90H	-	-	$\overline{\text{RST}}$	-	-	-	RXD
P0M1	Port 0 output mode 1	84H	-	-	(P0M1.5)	(P0M1.4)	(P0M1.3)	(P0M1.2)	(P0M1.1)
P0M2	Port 0 output mode 2	85H	-	-	(P0M2.5)	(P0M2.4)	(P0M2.3)	(P0M2.2)	(P0M2.1)
P1M1	Port 1 output mode 1	91H	-	-	-	-	-	-	(P1M1.1)
P1M2	Port 1 output mode 2	92H	-	-	-	-	-	-	(P1M2.1)
PCON	Power control register	87H	SMOD1	SMOD0	BOPD	BOI	GF1	GF0	PMOD1
PCONA	Power control register A	B5H	RTCPD		VCPD	ADPD		-	SPD
PCONB	reserved for Power control register B	B6H	-	-	-	-	-	-	-

Table 9. P89LPC9107 special function registers *...continued*

** indicates SFRs that are bit addressable.*

Name	Description	SFR addr.	Bit functions and addresses						
			MSB						
	Bit address		**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**
PSW*	Program status word	D0H	CY	AC	F0	RS1	RS0	OV	F1
PT0AD	Port 0 digital input disable	F6H	-	-	PT0AD.5	PT0AD.4	PT0AD.3	PT0AD.2	PT0AD.1
RSTSRC	Reset source register	DFH	-	-	BOF	POF	R_BK	R_WD	R_SF
RTCCON	Real-time clock control	D1H	RTCF	RTCS1	RTCS0	-	-	-	ERTC
RTCH	Real-time clock register high	D2H							
RTCL	Real-time clock register low	D3H							
SADDR	Serial port address register	A9H							
SADEN	Serial port address enable	B9H							
SBUF	Serial port data buffer register	99H							
	Bit address		**9F**	**9E**	**9D**	**9C**	**9B**	**9A**	**99**
SCON*	Serial port control	98H	SM0/FE	SM1	SM2	REN	TB8	RB8	TI
SSTAT	Serial port extended status register	BAH	DBMOD	INTLO	CIDIS	DBISEL	FE	BR	OE
SP	Stack pointer	81H							

Table 9. P89LPC9107 special function registers *...continued*

** indicates SFRs that are bit addressable.*

Name	Description	SFR addr.	Bit functions and addresses						
			MSB						
	Bit address		8F	8E	8D	8C	8B	8A	89
TCON*	Timer 0 and 1 control	88H	TF1	TR1	TF0	TR0	-	-	-
TH0	Timer 0 high	8CH							
TH1	Timer 1 high	8DH							
TL0	Timer 0 low	8AH							
TL1	Timer 1 low	8BH							
TMOD	Timer 0 and 1 mode	89H	-	-	T1M1	T1M0	-	-	T0M1
TRIM	Internal oscillator trim register	96H	RCCLK	ENCLK	TRIM.5	TRIM.4	TRIM.3	TRIM.2	TRIM.1
WDCON	Watchdog control register	A7H	PRE2	PRE1	PRE0	-	-	WDRUN	WDTOF
WDL	Watchdog load	C1H							
WFEED1	Watchdog feed 1	C2H							
WFEED2	Watchdog feed 2	C3H							

[1] Unimplemented bits in SFRs (labeled '-') are X (unknown) at all times. Unless otherwise specified, ones should not be written to these bits sin purposes in future derivatives. The reset values shown for these bits are logic 0s although they are unknown when read.

[2] BRGR1 and BRGR0 must only be written if BRGEN in BRGCON SFR is logic 0. If any are written while BRGEN = 1, the result is unpredictabl

[3] All ports are in input-only (high-impedance) state after power-up.

[4] The RSTSRC register reflects the cause of the P89LPC9102/9103/9107 reset. Upon a power-up reset, all reset source flags are cleared excep value is xx11 0000.

[5] The only reset source that affects these SFRs is power-on reset.

[6] On power-on reset, the TRIM SFR is initialized with a factory preprogrammed value. Other resets will not cause initialization of the TRIM regis

[7] After reset, the value is 1110 01x1, i.e., PRE2 to PRE0 are all logic 1s, WDRUN = 1 and WDCLK = 1. WDTOF bit is logic 1 after watchdog time reset. Other resets will not affect WDTOF.

8.2 Enhanced CPU

The P89LPC9102/9103/9107 uses an enhanced 80C51 CPU which runs at six times the speed of standard 80C51 devices. A machine cycle consists of two CPU clock cycles, and most instructions execute in one or two machine cycles.

8.3 Clocks

8.3.1 Clock definitions

The P89LPC9102/9103/9107 device has internal clocks as defined below:

OSCCLK — Input to the DIVM clock divider. OSCCLK is selected from one of the clock sources (see Figure 11 “Block diagram of P89LPC9102 oscillator control”) and can also be optionally divided to a slower frequency (see Section 8.8 “CCLK modification: DIVM register”).

Note: f_{osc} is defined as the OSCCLK frequency.

CCLK — CPU clock; output of the clock divider. There are two CCLK cycles per machine cycle, and most instructions are executed in one to two machine cycles (two or four CCLK cycles).

RCCLK — The internal 7.373 MHz RC oscillator output. The clock doubler option, when enabled, provides an output frequency of 14.746 MHz.

PCLK — Clock for the various peripheral devices and is $^{CCLK}/_{2}$.

8.3.2 CPU clock (CCLK)

The P89LPC9102/9103/9107 provides user-selectable oscillator options in generating the CPU clock. This allows optimization for a range of needs from high precision to lowest possible cost. These options are configured when the flash memory is programmed and include an on-chip watchdog oscillator, an on-chip RC oscillator, and an external clock input.

8.4 On-chip RC oscillator option

The P89LPC9102/9103/9107 has a 6-bit TRIM register that can be used to tune the frequency of the RC oscillator. During reset, the TRIM value is initialized to a factory pre-programmed value to adjust the oscillator frequency to 7.373 MHz ± 1 % at room temperature. End-user applications can write to the Trim register to adjust the on-chip RC oscillator to other frequencies. When the clock doubler option is enabled (UCFG1.3 = 1) the output frequency is 14.746 MHz. If CCLK is 8 MHz or slower, the CLKLP SFR bit (AUXR1.7) can be set to logic 1 to reduce power consumption. On reset, CLKLP is logic 0 allowing highest performance access. This bit can then be set in software if CCLK is running at 8 MHz or slower.

The RCCLK bit (TRIM.7) can be used to switch between the clock source selected by UCFG1 and the internal RC oscillator. This allows a low frequency source such as the WDT or low speed external source to clock the device in order to save power and then switch to the higher speed internal RC oscillator to perform processing.

8.5 Watchdog oscillator option

The watchdog timer has a separate oscillator which has a frequency of 400 kHz. This oscillator can be used to save power when a high clock frequency is not needed.

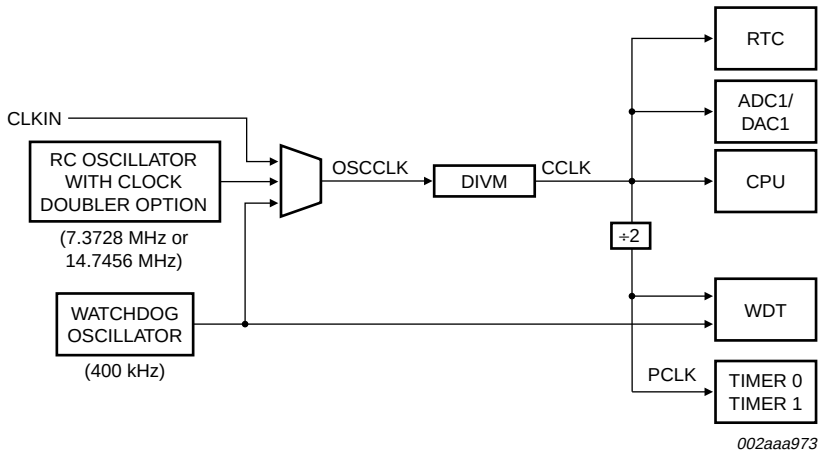


Fig 11. Block diagram of P89LPC9102 oscillator control

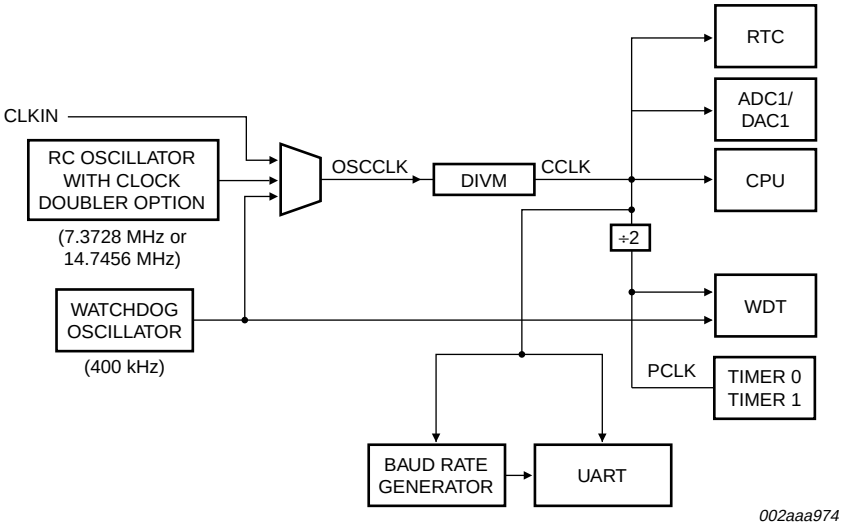


Fig 12. Block diagram of P89LPC9103/9107 oscillator control

8.6 External clock input option

In this configuration, the processor clock is derived from an external source driving the P0.5/CMPREF/CLKIN pin. The rate may be from 0 Hz up to 18 MHz. The P0.5/CMPREF/CLKIN pin may also be used as a standard port pin. **When using an oscillator frequency above 12 MHz, the reset input function of P1.5 must be enabled. An external circuit is required to hold the device in reset at power-up until V_{DD} has reached its specified level. When system power is removed V_{DD} will fall below the minimum specified operating voltage. When using an oscillator**

frequency above 12 MHz, in some applications, an external brownout detect circuit may be required to hold the device in reset when V_{DD} falls below the minimum specified operating voltage.

8.7 CCLK wake-up delay

The P89LPC9102/9103/9107 has an internal wake-up timer that delays the clock until it stabilizes depending to the clock source used.

8.8 CCLK modification: DIVM register

The OSCCLK frequency can be divided down up to 510 times by configuring a dividing register, DIVM, to generate CCLK. This feature makes it possible to temporarily run the CPU at a lower rate, reducing power consumption. By dividing the clock, the CPU can retain the ability to respond to events that would not exit Idle mode by executing its normal program at a lower rate. This can also allow bypassing the oscillator start-up time in cases where Power-down mode would otherwise be used. The value of DIVM may be changed by the program at any time without interrupting code execution.

8.9 Low power select

If CCLK is 8 MHz or slower, the CLKLP SFR bit (AUXR1.7) can be set to logic 1 to lower the power consumption further. On any reset, CLKLP is logic 0.

8.10 Memory organization

The various P89LPC9102/9103/9107 memory spaces are as follows:

- DATA

  128 bytes of internal data memory space (00H:7FH) accessed via direct or indirect addressing, using instruction other than MOVX and MOVC. All or part of the stack may be in this area.

- SFR

  Special Function Registers. Selected CPU registers and peripheral control and status registers, accessible only via direct addressing.

- CODE

  1 kB of Code memory space, accessed as part of program execution and via the MOVC instruction.

8.11 Interrupts

The P89LPC9102 supports nine interrupt sources: timers 0 and 1, brownout detect, watchdog timer/RTC, keyboard, comparator 1, and the A/D converter.

The P89LPC9103/9107 support nine interrupt sources: timers 0 and 1, serial port Tx, serial port Rx, combined serial port Rx/Tx, brownout detect, watchdog timer/RTC, keyboard, comparator, and the A/D converter.

Each interrupt source can be individually enabled or disabled by setting or clearing a bit in the interrupt enable registers IEN0 or IEN1. The IEN0 register also contains a global disable bit, EA, which disables all interrupts.

Each interrupt source can be individually programmed to one of four priority levels by setting or clearing bits in the interrupt priority registers IP0, IP0H, IP1, and IP1H. An interrupt service routine in progress can be interrupted by a higher priority interrupt, but not by another interrupt of the same or lower priority. The highest priority interrupt service cannot be interrupted by any other interrupt source. If two requests of different priority levels are pending at the start of an instruction, the request of higher priority level is serviced.

If requests of the same priority level are pending at the start of an instruction, an internal polling sequence determines which request is serviced. This is called the arbitration ranking. Note that the arbitration ranking is only used to resolve pending requests of the same priority level.

8.11.1 External interrupt inputs

The P89LPC9102/9103/9107 has a Keypad Interrupt function. This can be used as an external interrupt input.

If enabled when the P89LPC9102/9103/9107 is put into Power-down mode or Idle mode, the interrupt will cause the processor to wake-up and resume operation. Refer to Section 8.14 “Power reduction modes” for details.

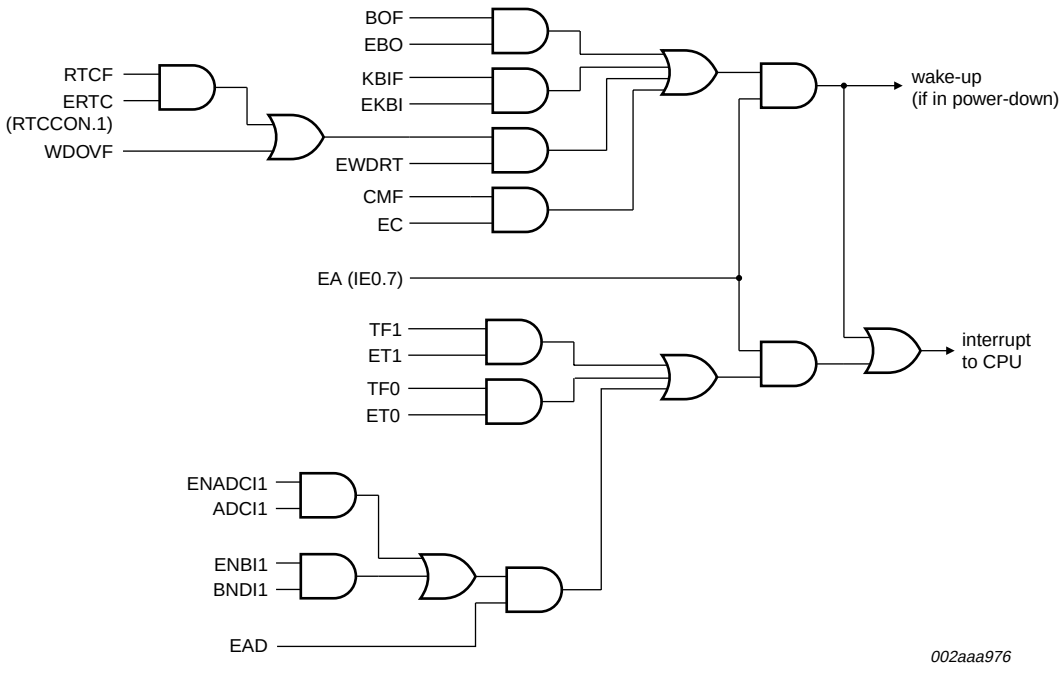


Fig 13. Interrupt sources, interrupt enables, and power-down wake-up sources (P89LPC9102)

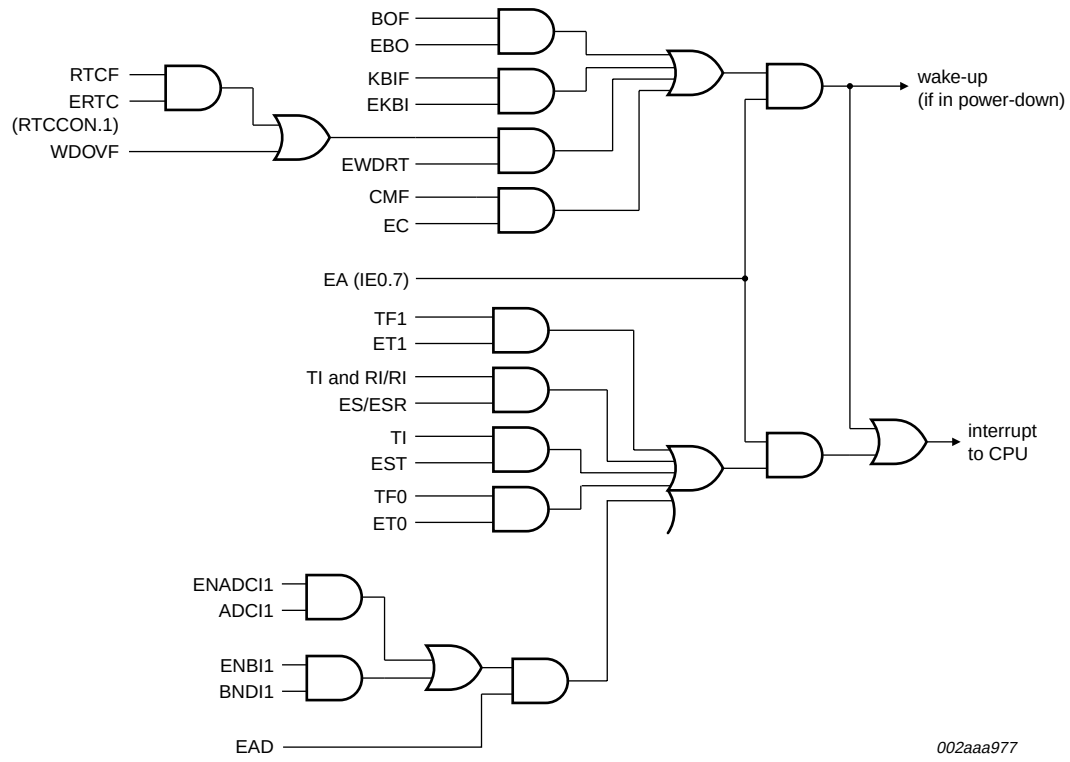


Fig 14. Interrupt sources, interrupt enables, and power-down wake-up sources (P89LPC9103/9107)

8.12 I/O ports

The P89LPC9102/9103/9107 has either 6, 7, or 8 I/O pins depending on the reset pin option and clock source option chosen. Refer to Table 10.

Table 10. Number of I/O pins available

Clock source	Reset option	Number of I/O pins (10-pin package)	Number of I/O pins (14-pin package)
On-chip oscillator or watchdog oscillator	No external reset (except during power-up)	8	10
	External $\overline{\text{RST}}$ pin supported	7	9
External clock input	No external reset (except during power-up)	7	9
	External $\overline{\text{RST}}$ pin supported[1]	6	8

[1] Required for operation above 12 MHz.

8.12.1 Port configurations

All but one I/O port pin on the P89LPC9102/9103/9107 may be configured by software to one of four types on a bit-by-bit basis. These are: quasi-bidirectional (standard 80C51 port outputs), push-pull, open drain, and input-only. Two configuration registers for each port select the output type for each port pin.

P1.5 ($\overline{\text{RST}}$) can only be an input and cannot be configured.

8.12.2 Quasi-bidirectional output configuration

Quasi-bidirectional output type can be used as both an input and output without the need to reconfigure the port. This is possible because when the port outputs a logic HIGH, it is weakly driven, allowing an external device to pull the pin LOW. When the pin is driven LOW, it is driven strongly and able to sink a fairly large current. These features are somewhat similar to an open-drain output except that there are three pull-up transistors in the quasi-bidirectional output that serve different purposes.

The P89LPC9102/9103/9107 is a 3 V device, however, the pins are 5 V-tolerant. In quasi-bidirectional mode, if a user applies 5 V on the pin, there will be a current flowing from the pin to V_{DD}, causing extra power consumption. Therefore, applying 5 V in quasi-bidirectional mode is discouraged.

A quasi-bidirectional port pin has a Schmitt triggered input that also has a glitch suppression circuit.

8.12.3 Open-drain output configuration

The open-drain output configuration turns off all pull-ups and only drives the pull-down transistor of the port driver when the port latch contains a logic 0. To be used as a logic output, a port configured in this manner must have an external pull-up, typically a resistor tied to V_{DD}.

An open-drain port pin has a Schmitt triggered input that also has a glitch suppression circuit.

8.12.4 Input-only configuration

The input-only port configuration has no output drivers. It is a Schmitt triggered input that also has a glitch suppression circuit.

8.12.5 Push-pull output configuration

The push-pull output configuration has the same pull-down structure as both the open-drain and the quasi-bidirectional output modes, but provides a continuous strong pull-up when the port latch contains a logic 1. The push-pull mode may be used when more source current is needed from a port output. A push-pull port pin has a Schmitt triggered input that also has a glitch suppression circuit.

8.12.6 Port 0 analog functions

The P89LPC9102/9103/9107 incorporates an Analog Comparator. In order to give the best analog function performance and to minimize power consumption, pins that are being used for analog functions must have the digital outputs and digital inputs disabled.

Digital outputs are disabled by putting the port output into the Input-only (high-impedance) mode as described in Section 8.12.4 “Input-only configuration”.

Digital inputs on Port 0 may be disabled through the use of the PT0AD register. On any reset, the PT0AD bits default to logic 0s to enable digital functions.

8.12.7 Additional port features

After power-up, all pins are in Input-only mode. **Please note that this is different from the LPC76x series of devices.**

- After power-up all I/O pins, except P1.5, may be configured by software.
- Pin P1.5 is input-only.

Every output on the P89LPC9102/9103/9107 has been designed to sink typical LED drive current. However, there is a maximum total output current for all ports which must not be exceeded. Please refer to Table 12 “Static characteristics” for detailed specifications.

All ports pins that can function as an output have slew rate controlled outputs to limit noise generated by quickly switching output signals. The slew rate is factory-set to approximately 10 ns rise and fall times.

8.13 Power monitoring functions

The P89LPC9102/9103/9107 incorporates power monitoring functions designed to prevent incorrect operation during initial power-up and power loss or reduction during operation. This is accomplished with two hardware functions: Power-on Detect and Brownout detect.

8.13.1 Brownout detection

The Brownout detect function determines if the power supply voltage drops below a certain level. The default operation is for a Brownout detection to cause a processor reset, however, it may alternatively be configured to generate an interrupt.

Brownout detection may be enabled or disabled in software.

If Brownout detection is enabled, the brownout condition occurs when V_{DD} falls below the brownout trip voltage, V_{bo} (see Table 12 “Static characteristics”), and is negated when V_{DD} rises above V_{bo}. If the P89LPC9102/9103/9107 device is to operate with a power supply that can be below 2.7 V, Brownout detect Enable (BOE) should be left in the unprogrammed state so that the device can operate at 2.4 V, otherwise continuous brownout reset may prevent the device from operating.

For correct activation of Brownout detect, the V_{DD} rise and fall times must be observed. Please see Table 12 “Static characteristics” for specifications.

8.13.2 Power-on detection

The Power-on Detect has a function similar to the Brownout detect, but is designed to work as power comes up initially, before the power supply voltage reaches a level where Brownout detect can work. The Power-on detect flag (POF) in the RSTSRC register is set to indicate an initial power-up condition. The POF flag will remain set until cleared by software.

8.14 Power reduction modes

The P89LPC9102/9103/9107 supports three different power reduction modes. These modes are Idle mode, Power-down mode, and Total Power-down mode.

8.14.1 Idle mode

Idle mode leaves peripherals running in order to allow them to activate the processor when an interrupt is generated. Any enabled interrupt source or reset may terminate Idle mode.

8.14.2 Slow-down mode using the DIVM register

Slow-down mode is achieved by dividing down the OSCCLK frequency to generate CCLK. This division is accomplished by configuring the DIVM register to divide OSCCLK by up to 510 times. This feature makes it possible to temporarily run the CPU at a lower rate, reducing power consumption. By dividing the clock, the CPU can retain the ability to respond to events that would not exit Idle mode by executing its normal program at a lower rate. This can also allow bypassing the oscillator start-up time in cases where Power-down mode would otherwise be used. The value of DIVM may be changed by the program at any time without interrupting code execution.

8.14.3 Power-down mode

The Power-down mode stops the oscillator in order to minimize power consumption. The P89LPC9102/9103/9107 exits Power-down mode via any reset, or certain interrupts. In Power-down mode, the power supply voltage may be reduced to the data retention voltage V_{DDR}. This retains the RAM contents at the point where Power-down mode was entered. SFR contents are not guaranteed after V_{DD} has been lowered to V_{DDR}, therefore it is highly recommended to wake-up the processor via reset in this case. V_{DD} must be raised to within the operating range before the Power-down mode is exited.

Some chip functions continue to operate and draw power during Power-down mode, increasing the total power used during Power-down mode. These include: Brownout detect, watchdog timer, comparators (note that comparator can be powered-down separately), and RTC/system timer. The internal RC oscillator is disabled unless both the RC oscillator has been selected as the system clock **and** the RTC is enabled.

8.14.4 Total Power-down mode

This is the same as Power-down mode except that the brownout detection circuitry and the voltage comparators are also disabled to conserve additional power. The internal RC oscillator is disabled unless both the RC oscillator has been selected as the system clock **and** the RTC is enabled. If the internal RC oscillator is used to clock the RTC during Power-down mode, there will be high power consumption. Please use an external low frequency clock to achieve low power with the RTC running during Power-down mode.

8.15 Reset

The P1.5/$\overline{\text{RST}}$ pin can function as either an active-LOW reset input or as a digital input, P1.5. The RPE (Reset Pin Enable) bit in UCFG1, when set to logic 1, enables the external reset input function on P1.5. When cleared, P1.5 may be used as an input pin.

Remark: During a power-up sequence, the RPE selection is overridden and this pin will always function as a reset input. **An external circuit connected to this pin should not hold this pin LOW during a power-on sequence as this will keep the device in reset.** After power-up this input will function either as an external reset input or as a digital input as defined by the RPE bit. Only a power-up reset will temporarily override the selection defined by RPE bit. Other sources of reset will not override the RPE bit.

Remark: During a power cycle, V_{DD} must fall below V_{POR} (see Table 12 “Static characteristics”) before power is reapplied, in order to ensure a power-on reset.

Reset can be triggered from the following sources:

- External reset pin (during power-up or if user configured via UCFG1)

- Power-on detect
- Brownout detect
- Watchdog timer
- Software reset
- UART break character detect reset (P89LPC9103/9107).

For every reset source, there is a flag in the Reset Register, RSTSRC. The user can read this register to determine the most recent reset source. These flag bits can be cleared in software by writing a logic 0 to the corresponding bit. More than one flag bit may be set:

- During a power-on reset, both POF and BOF are set but the other flag bits are cleared.
- For any other reset, previously set flag bits that have not been cleared will remain set.

8.16 Timers 0 and 1

The P89LPC9102 has two general purpose timer/counters which are similar to the standard 80C51 Timer 0 and Timer 1. These timers have five operating modes (modes 0, 1, 2, 3, and 6). Modes 0, 1, and 2 are the same for both Timers. Mode 3 is different.

The P89LPC9103/9107 has two general purpose timers which are similar to the standard 80C51 Timer 0 and Timer 1. These timers have four operating modes (modes 0, 1, 2, and 3). Modes 0, 1, and 2 are the same for both Timers. Mode 3 is different.

8.16.1 Mode 0

Putting either Timer into Mode 0 makes it look like an 8048 Timer, which is an 8-bit Counter with a divide-by-32 prescaler. In this mode, the Timer register is configured as a 13-bit register. Mode 0 operation is the same for Timer 0 and Timer 1.

8.16.2 Mode 1

Mode 1 is the same as Mode 0, except that all 16 bits of the timer register are used.

8.16.3 Mode 2

Mode 2 configures the Timer register as an 8-bit counter with automatic reload. Mode 2 operation is the same for Timer 0 and Timer 1.

8.16.4 Mode 3

When Timer 1 is in Mode 3 it is stopped. Timer 0 in Mode 3 forms two separate 8-bit counters and is provided for applications that require an extra 8-bit timer. When Timer 1 is in Mode 3 it can still be used by the serial port as a baud rate generator.

8.16.5 Mode 6 (P89LPC9102/9107)

In this mode, the corresponding timer can be changed to a PWM with a full period of 256 timer clocks.

8.16.6 Timer overflow toggle output (P89LPC9102/9107)

Timers 0 and 1 can be configured to automatically toggle a port output whenever a timer overflow occurs. The same device pins that are used for the T0 and T1 count inputs are also used for the timer toggle outputs. The port outputs will be a logic 1 prior to the first timer overflow when this mode is turned on.

8.17 RTC/system timer

The P89LPC9102/9103/9107 has a simple RTC that allows a user to continue running an accurate timer while the rest of the device is powered-down. The RTC can be a wake-up or an interrupt source. The RTC is a 23-bit down counter comprised of a 7-bit prescaler and a 16-bit loadable down counter. When it reaches all logic 0s, the counter will be reloaded again and the RTCF flag will be set. The clock source for this counter is the CCLK. Only power-on reset will reset the RTC and its associated SFRs to the default state.

8.18 UART (P89LPC9103/9107)

The P89LPC9103/9107 has an enhanced UART that is compatible with the conventional 80C51 UART except that Timer 2 overflow cannot be used as a baud rate source. The P89LPC9103/9107 does include an independent Baud Rate Generator. The baud rate can be selected from CCLK (divided by a constant), Timer 1 overflow, or the independent Baud Rate Generator. In addition to the baud rate generation, enhancements over the standard 80C51 UART include Framing Error detection, automatic address recognition, selectable double buffering and several interrupt options. The UART can be operated in four modes: shift register, 8-bit UART, 9-bit UART, and $^{CCLK}/_{32}$ or $^{CCLK}/_{16}$.

8.18.1 Mode 0

Serial data enters and exits through RXD. TXD outputs the shift clock. Eight bits are transmitted or received, LSB first. The baud rate is fixed at $^1/_{16}$ of the CPU clock frequency.

8.18.2 Mode 1

10 bits are transmitted (through TXD) or received (through RXD): a start bit (logic 0), 8 data bits (LSB first), and a stop bit (logic 1). When data is received, the stop bit is stored in RB8 in Special Function Register SCON. The baud rate is variable and is determined by the Timer 1 overflow rate or the Baud Rate Generator (described in Section 8.18.5 “Baud rate generator and selection”).

8.18.3 Mode 2

11 bits are transmitted (through TXD) or received (through RXD): start bit (logic 0), 8 data bits (LSB first), a programmable 9th data bit, and a stop bit (logic 1). When data is transmitted, the 9th data bit (TB8 in SCON) can be assigned the value of logic 0 or logic 1. Or, for example, the parity bit (P, in the PSW) could be moved into TB8. When data is received, the 9th data bit goes into RB8 in Special Function Register SCON, while the stop bit is not saved. The baud rate is programmable to either $^1/_{16}$ or $^1/_{32}$ of the CPU clock frequency, as determined by the SMOD1 bit in PCON.

8.18.4 Mode 3

11 bits are transmitted (through TXD) or received (through RXD): a start bit (logic 0), 8 data bits (LSB first), a programmable 9th data bit, and a stop bit (logic 1). In fact, Mode 3 is the same as Mode 2 in all respects except baud rate. The baud rate in Mode 3 is variable and is determined by the Timer 1 overflow rate or the Baud Rate Generator (described in section Section 8.18.5 “Baud rate generator and selection”).

8.18.5 Baud rate generator and selection

The P89LPC9103/9107 enhanced UART has an independent Baud Rate Generator. The baud rate is determined by a baud-rate preprogrammed into the BRGR1 and BRGR0 SFRs which together form a 16-bit baud rate divisor value that works in a similar manner as Timer 1. If the baud rate generator is used, Timer 1 can be used for other timing functions.

The UART can use either Timer 1 or the baud rate generator output (see Figure 15). Note that Timer T1 is further divided by 2 if the SMOD1 bit (PCON.7) is cleared. The independent Baud Rate Generator uses CCLK.

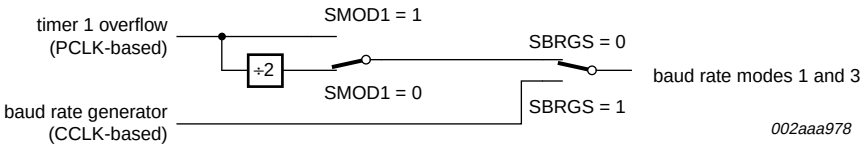


Fig 15. Baud rate sources for UART (Modes 1, 3)

8.18.6 Framing error

Framing error is reported in the status register (SSTAT). In addition, if SMOD0 (PCON.6) is logic 1, framing errors can be made available in SCON.7, respectively. If SMOD0 is logic 0, SCON.7 is SM0. It is recommended that SM0 and SM1 (SCON[7:6]) are set up when SMOD0 is logic 0.

8.18.7 Break detect

Break detect is reported in the status register (SSTAT). A break is detected when 11 consecutive bits are sensed LOW. The break detect can be used to reset the device.

8.18.8 Double buffering

The UART has a transmit double buffer that allows buffering of the next character to be written to SBUF while the first character is being transmitted. Double buffering allows transmission of a string of characters with only one stop bit between any two characters, as long as the next character is written between the start bit and the stop bit of the previous character.

Double buffering can be disabled. If disabled (DBMOD, i.e., SSTAT.7 = 0), the UART is compatible with the conventional 80C51 UART. If enabled, the UART allows writing to SnBUF while the previous data is being shifted out. Double buffering is only allowed in Modes 1, 2 and 3. When operated in Mode 0, double buffering must be disabled (DBMOD = 0).

8.18.9 Transmit interrupts with double buffering enabled (Modes 1, 2 and 3)

Unlike the conventional UART, in double buffering mode, the Tx interrupt is generated when the double buffer is ready to receive new data.

8.18.10 The 9th bit (bit 8) in double buffering (Modes 1, 2 and 3)

If double buffering is disabled TB8 can be written before or after SBUF is written, as long as TB8 is updated some time before that bit is shifted out. TB8 must not be changed until the bit is shifted out, as indicated by the Tx interrupt.

If double buffering is enabled, TB8 **must** be updated before SBUF is written, as TB8 will be double-buffered together with SBUF data.

8.19 Analog comparators

One analog comparator is provided on the P89LPC9102/9103/9107. Comparator operation is such that the output is a logic 1 (which may be read in a register) when the positive input is greater than the negative input (selectable from a pin or an internal reference voltage). Otherwise the output is a zero. The comparator may be configured to cause an interrupt when the output value changes.

The connections to the comparator are shown in Figure 16. The comparator functions to V_{DD} = 2.4 V.

When the comparator is first enabled, the comparator's interrupt flag is not guaranteed to be stable for 10 microseconds. The comparator interrupt should not be enabled during that time, and the comparator interrupt flag must be cleared before the interrupt is enabled in order to prevent an immediate interrupt service.

When a comparator is disabled the comparator's output, COx, goes HIGH. If the comparator output was LOW and then is disabled, the resulting transition of the comparator output from a LOW to HIGH state will set the comparator flag, CMFx. This will cause an interrupt if the comparator interrupt is enabled. The user should therefore disable the comparator interrupt prior to disabling the comparator. Additionally, the user should clear the comparator flag, CMFx, after disabling the comparator.

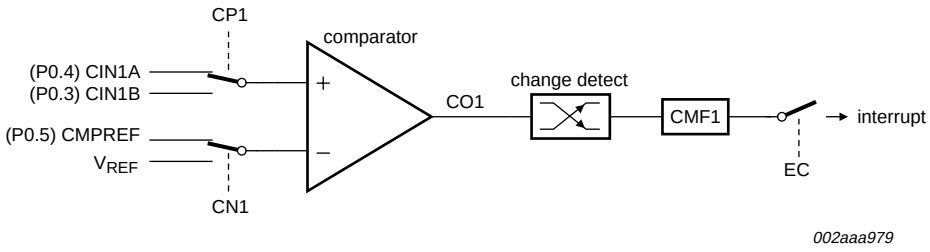


Fig 16. Comparator input and output connections

8.20 Internal reference voltage

An internal reference voltage generator may supply a default reference when a single comparator input pin is used. The value of the internal reference voltage, referred to as $V_{ref(bg)}$, is 1.23 V ± 3 %.

8.21 Comparator interrupt

The comparator has an interrupt flag contained in its configuration register. This flag is set whenever the comparator output changes state. The flag may be polled by software or may be used to generate an interrupt.

8.22 Comparator and power reduction modes

The comparator may remain enabled when Power-down mode or Idle mode is activated, but the comparator is disabled automatically in Total Power-down mode.

If the comparator interrupt is enabled (except in Total Power-down mode), a change of the comparator output state will generate an interrupt and wake-up the processor. If the comparator output to a pin is enabled, the pin should be configured in the push-pull mode in order to obtain fast switching times while in Power-down mode. The reason is that with the oscillator stopped, the temporary strong pull-up that normally occurs during switching on a quasi-bidirectional port pin does not take place.

The comparator consumes power in Power-down mode and Idle mode, as well as in the normal operating mode. This fact should be taken into account when system power consumption is an issue. To minimize power consumption, the user can disable the comparator via PCONA.5 or put the device in Total Power-down mode.

8.23 Keypad interrupt (KBI)

The Keypad Interrupt function is intended primarily to allow a single interrupt to be generated when Port 0 is equal to or not equal to a certain pattern. This function can be used for bus address recognition or keypad recognition. The user can configure the port via SFRs for different tasks.

The Keypad Interrupt Mask Register (KBMASK) is used to define which input pins connected to Port 0 can trigger the interrupt. The Keypad Pattern Register (KBPATN) is used to define a pattern that is compared to the value of Port 0. The Keypad Interrupt Flag (KBIF) in the Keypad Interrupt Control Register (KBCON) is set when the condition is matched while the Keypad Interrupt function is active. An interrupt will be generated if enabled. The PATN_SEL bit in the Keypad Interrupt Control Register (KBCON) is used to define equal or not-equal for the comparison.

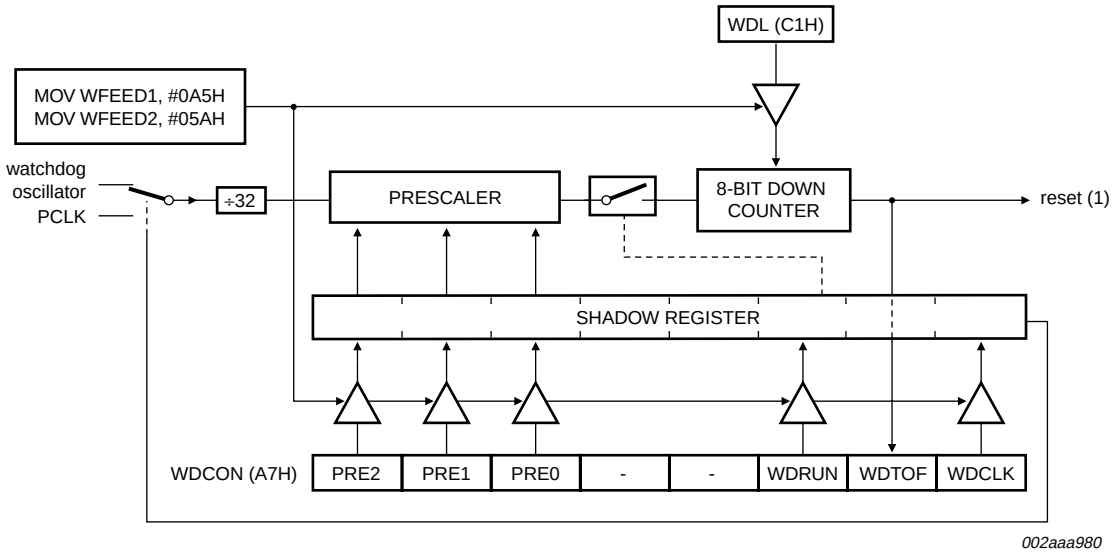
In order to use the Keypad Interrupt as an original KBI function like in 87LPC76x series, the user needs to set KBPATN = 0FFH and PATN_SEL = 1 (not equal), then any key connected to Port 0 which is enabled by the KBMASK register will cause the hardware to set KBIF and generate an interrupt if it has been enabled. The interrupt may be used to wake-up the CPU from Idle mode or Power-down mode. This feature is particularly useful in handheld, battery powered systems that need to carefully manage power consumption yet also need to be convenient to use.

In order to set the flag and cause an interrupt, the pattern on Port 0 must be held longer than six CCLKs.

8.24 Watchdog timer

The watchdog timer causes a system reset when it underflows as a result of a failure to feed the timer prior to the timer reaching its terminal count. It consists of a programmable 12-bit prescaler, and an 8-bit down counter. The down counter is decremented by a tap

taken from the prescaler. The clock source for the prescaler is either the PCLK or the nominal 400 kHz watchdog oscillator. The watchdog timer can only be reset by a power-on reset. When the watchdog timer feature is disabled, it can be used as an interval timer and may generate an interrupt. Figure 17 shows the watchdog timer in Watchdog mode. Feeding the watchdog timer requires a two-byte sequence. If PCLK is selected as the watchdog timer clock and the CPU is powered-down, the watchdog timer is disabled. The watchdog timer has a time-out period that ranges from a few μs to a few seconds. Please refer to the *P89LPC9102/9103/9107 User manual UM10112* for more details.



(1) Watchdog timer reset can also be caused by an invalid feed sequence, or by writing to WDCON not immediately followed by a feed sequence.

Fig 17. Watchdog timer in Watchdog mode (WDTE = 1)

8.25 Additional features

8.25.1 Software reset

The SRST bit in AUXR1 gives software the opportunity to reset the processor completely, as if an external reset or watchdog timer reset had occurred. Care should be taken when writing to AUXR1 to avoid accidental software resets.

8.25.2 Dual data pointers

The dual Data Pointers (DPTR) provides two different Data Pointers to specify the address used with certain instructions. The DPS bit in the AUXR1 register selects one of the two Data Pointers. Bit 2 of AUXR1 is permanently wired as a logic 0 so that the DPS bit may be toggled (thereby switching Data Pointers) simply by incrementing the AUXR1 register, without the possibility of inadvertently altering other bits in the register.

8.26 Flash program memory

8.26.1 General description

The P89LPC9102/9103/9107 flash memory provides in-circuit electrical erasure and programming. The flash can be erased, read, and written as bytes. The Sector and Page Erase functions can erase any flash sector (256 bytes) or page (16 bytes). The Chip Erase operation will erase the entire program memory. In-Circuit Programming using standard commercial programmers is available. In addition, In-Application Programming Lite (IAP-Lite) and byte erase allows code memory to be used for non-volatile data storage. On-chip erase and write timing generation contribute to a user-friendly programming interface. The P89LPC9102/9103/9107 flash reliably stores memory contents even after more than 400000 erase and program cycles. The cell is designed to optimize the erase and programming mechanisms. The P89LPC9102/9103/9107 uses V_{DD} as the supply voltage to perform the Program/Erase algorithms.

8.26.2 Features

- Programming and erase over the full operating voltage range.
- Byte-erase allowing code memory to be used for data storage.
- Read/Programming/Erase using ICP.
- Any flash program/erase operation in 2 ms.
- Programming with industry-standard commercial programmers.
- Programmable security for the code in the flash for each sector.
- More than 400000 minimum erase/program cycles for each byte.
- 20-year minimum data retention.

8.26.3 Flash organization

The P89LPC9102/9103/9107 program memory consists of four 256 byte sectors. Each sector can be further divided into 16-byte pages. In addition to sector erase, page erase, and byte erase, a 16-byte page register is included which allows from 1 byte to 16 bytes of a given page to be programmed at the same time, substantially reducing overall programming time. In addition, erasing and reprogramming of user-programmable configuration bytes including UCFG1, the Boot Status Bit, and the Boot Vector is supported.

8.26.4 Flash programming and erasing

Different methods of erasing or programming of the flash are available. The flash may be programmed or erased in the end-user application (IAP-Lite) under control of the application's firmware. Another option is to use the ICP mechanism. This ICP system provides for programming through a serial clock- serial data interface. Third, the flash may be programmed or erased using a commercially available EPROM programmer which supports this device. This device does not provide for direct verification of code memory contents. Instead this device provides a 32-bit CRC result on either a sector or the entire 1 kB of user code space.

8.26.5 In-circuit programming

In-Circuit Programming is performed without removing the microcontroller from the system. The In-Circuit Programming facility consists of internal hardware resources to facilitate remote programming of the P89LPC9102/9103/9107 through a two-wire serial interface. The NXP In-Circuit Programming facility has made in-circuit programming in an embedded application, using commercially available programmers, possible with a minimum of additional expense in components and circuit board area. The ICP function uses five pins. Only a small connector needs to be available to interface your application to a commercial programmer in order to use this feature. Additional details may be found in the *P89LPC9102/9103/9107 User manual UM10112*.

8.26.6 In-application programming (IAP-Lite)

In-Application Programming is performed in the application under the control of the microcontroller's firmware. The IAP facility consists of internal hardware resources to facilitate programming and erasing. The NXP In-Application Programming (IAP-Lite) has made in-application programming in an embedded application possible without additional components. This is accomplished through the use of four SFRs consisting of a control/status register, a data register, and two address registers. Additional details may be found in the *P89LPC9102/9103/9107 User manual UM10112*.

8.26.7 Using flash as data storage

The flash code memory array of this device supports individual byte erasing and programming. Any byte in the code memory array may be read using the MOVC instruction, provided that the sector containing the byte has not been secured (a MOVC instruction is not allowed to read code memory contents of a secured sector). Thus any byte in a non-secured sector may be used for non-volatile data storage.

8.26.8 User configuration bytes

Some user-configurable features of the P89LPC9102/9103/9107 must be defined at power-up and therefore cannot be set by the program after start of execution. These features are configured through the use of the flash byte UCFG1. Please see the *P89LPC9102/9103/9107 User manual UM10112* for additional details.

8.26.9 User sector security bytes

There are four user sector security bytes, each corresponding to one sector. Please see the *P89LPC9102/9103/9107 User manual UM10112* for additional details.

9. A/D Converter

9.1 General description

The P89LPC9102/9103/9107 has an 8-bit, 4-channel multiplexed successive approximation analog-to-digital converter. The A/D consists of a 4-input multiplexer which feeds a sample-and-hold circuit providing an input signal to one of two comparator inputs. The control logic in combination with the Successive Approximation Register (SAR) drives a digital-to-analog converter which provides the other input to the comparator. The output of the comparator is fed to the SAR. A block diagram of the A/D converter is shown in Figure 18.

9.2 Features

- 8-bit, 4-channel multiplexed input, successive approximation A/D converter
- Four result registers
- Six operating modes
  - Fixed channel, single conversion mode
  - Fixed channel, continuous conversion mode
  - Auto scan, single conversion mode
  - Auto scan, continuous conversion mode
  - Dual channel, continuous conversion mode
  - Single step mode
- Two conversion start modes
  - Timer triggered start
  - Start immediately
- 8-bit conversion time of ≥ 3.9 µs at an ADC clock of 3.3 MHz
- Interrupt or polled operation
- Boundary limits interrupt
- DAC output to a port pin with high output impedance
- Clock divider
- Power-down mode

9.3 Block diagram

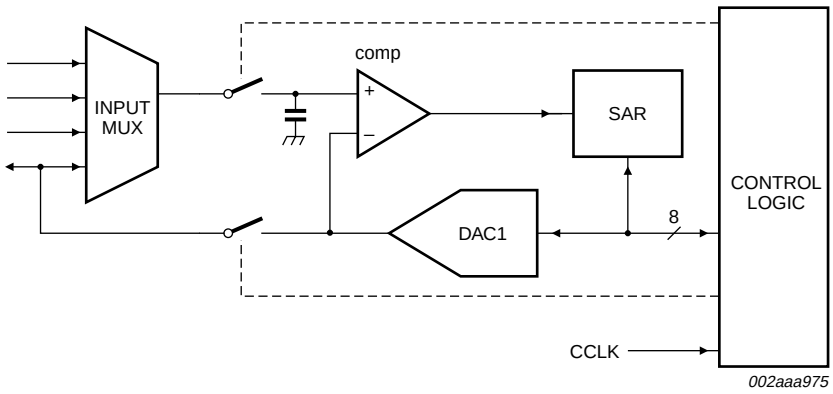


Fig 18. ADC block diagram

9.4 A/D operating modes

9.4.1 Fixed channel, single conversion mode

A single input channel can be selected for conversion. A single conversion will be performed and the result placed in the result register which corresponds to the selected input channel. An interrupt, if enabled, will be generated after the conversion completes.

9.4.2 Fixed channel, continuous conversion mode

A single input channel can be selected for continuous conversion. The results of the conversions will be sequentially placed in the four result registers. An interrupt, if enabled, will be generated after every four conversions. Additional conversion results will again cycle through the four result registers, overwriting the previous results. Continuous conversions continue until terminated by the user.

9.4.3 Auto scan, single conversion mode

Any combination of the four input channels can be selected for conversion. A single conversion of each selected input will be performed and the result placed in the result register which corresponds to the selected input channel. An interrupt, if enabled, will be generated after all selected channels have been converted. If only a single channel is selected this is equivalent to single channel, single conversion mode.

9.4.4 Auto scan, continuous conversion mode

Any combination of the four input channels can be selected for conversion. A conversion of each selected input will be performed and the result placed in the result register which corresponds to the selected input channel. An interrupt, if enabled, will be generated after all selected channels have been converted. The process will repeat starting with the first selected channel. Additional conversion results will again cycle through the four result registers, overwriting the previous results. Continuous conversions continue until terminated by the user.

9.4.5 Dual channel, continuous conversion mode

This is a variation of the auto scan continuous conversion mode where conversion occurs on two user-selectable inputs. The result of the conversion of the first channel is placed in result register, AD1DAT0. The result of the conversion of the second channel is placed in result register, AD1DAT1. The first channel is again converted and its result stored in AD1DAT2. The second channel is again converted and its result placed in AD1DAT3. An interrupt is generated, if enabled, after every set of four conversions (two conversions per channel).

9.4.6 Single step mode

This special mode allows ‘single-stepping’ in an auto scan conversion mode. Any combination of the four input channels can be selected for conversion. After each channel is converted, an interrupt is generated, if enabled, and the A/D waits for the next start condition. May be used with any of the start modes.

9.5 Conversion start modes

9.5.1 Timer triggered start

An A/D conversion is started by the overflow of Timer 0. Once a conversion has started, additional Timer 0 triggers are ignored until the conversion has completed. The Timer triggered start mode is available in all A/D operating modes.

9.5.2 Start immediately

Programming this mode immediately starts a conversion. This start mode is available in all A/D operating modes.

9.6 Boundary limits interrupt

The A/D converter has both a high and low boundary limit register. After the four MSBs have been converted, these four bits are compared with the four MSBs of the boundary high and low registers. If the four MSBs of the conversion are outside the limit an interrupt will be generated, if enabled. If the conversion result is within the limits, the boundary limits will again be compared after all 8 bits have been converted. An interrupt will be generated, if enabled, if the result is outside the boundary limits. The boundary limit may be disabled by clearing the boundary limit interrupt enable.

9.7 DAC output to a port pin with high output impedance

The A/D converter’s DAC block can be output to a port pin. In this mode, the AD1DAT3 register is used to hold the value fed to the DAC. After a value has been written to the DAC (written to AD1DAT3), the DAC output will appear on the channel 3 pin.

9.8 Clock divider

The A/D converter requires that its internal clock source be in the range of 500 kHz to 3.3 MHz to maintain accuracy. A programmable clock divider that divides the clock from 1 to 8 is provided for this purpose.

9.9 Power-down and Idle mode

In Idle mode the A/D converter, if enabled, will continue to function and can cause the device to exit Idle mode when the conversion is completed if the A/D interrupt is enabled. In Power-down mode or Total Power-down mode, the A/D does not function. If the A/D is enabled, it will consume power. Power can be reduced by disabling the A/D.

10. Limiting values

Table 11. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).[1]

Symbol	Parameter	Conditions	Min	Max	Unit
$T_{amb(bias)}$	bias ambient temperature		–55	+125	°C
T_{stg}	storage temperature		–65	+150	°C
$I_{OH(I/O)}$	HIGH-level output current per input/output pin		-	8	mA
$I_{OL(I/O)}$	LOW-level output current per input/output pin		-	20	mA
$I_{I/Otot(max)}$	maximum total input/output current		-	120	mA
V_n	voltage on any other pin	except V_{SS}, with respect to V_{DD}	–0.5	+5.5	V
$P_{tot(pack)}$	total power dissipation per package	based on package heat transfer, not device power consumption	-	1.5	W

[1] The following applies to Table 11 “Limiting values”:

a) Stresses above those listed may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any conditions other than those described in Table 12 “Static characteristics” and Table 13 “Dynamic characteristics (12 MHz)” section of this specification are not implied.

b) This product includes circuitry specifically designed for the protection of its internal devices from the damaging effects of excessive static charge. Nonetheless, it is suggested that conventional precautions be taken to avoid applying greater than the rated maximum.

c) Parameters are valid over operating temperature range unless otherwise specified. All voltages are with respect to V_{SS} unless otherwise noted.

11. Static characteristics

Table 12. Static characteristics

V_{DD} = 2.4 V to 3.6 V unless otherwise specified.
T_{amb} = −40 °C to +85 °C for industrial applications, unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typ[1]	Max	Unit
$I_{DD(oper)}$	operating supply current	3.6 V; 12 MHz	[2]	-	7	11	mA
		3.6 V; 7.373 MHz	[3]	-	4	7	mA
$I_{DD(idle)}$	Idle mode supply current	3.6 V; 12 MHz	[2]	-	3	5	mA
		3.6 V; 7.373 MHz	[3]	-	2	4	mA
$I_{DD(pd)}$	Power-down mode supply current	3.6 V; voltage comparators powered-down	[2]	-	55	80	µA
$I_{DD(tpd)}$	total Power-down mode supply current	3.6 V	[4]	-	0.5	5	µA
$(dV/dt)_r$	rise rate	of V_{DD}		-	-	2	mV/µs
$(dV/dt)_f$	fall rate	of V_{DD}		-	-	50	mV/µs
V_{POR}	power-on reset voltage			-	-	0.2	V
V_{DDR}	data retention supply voltage			1.5	-	-	V
$V_{th(HL)}$	HIGH-LOW threshold voltage			$0.22V_{DD}$	$0.4V_{DD}$	-	V
$V_{th(LH)}$	LOW-HIGH threshold voltage			-	$0.6V_{DD}$	$0.7V_{DD}$	V
V_{hys}	hysteresis voltage			-	$0.2V_{DD}$	-	V
V_{OL}	LOW-level output voltage	I_{OL} = 20 mA	[5]	-	0.6	1.0	V
		I_{OL} = 10 mA	[5]	-	0.3	0.5	V
		I_{OL} = 3.2 mA	[5]	-	0.2	0.3	V
V_{OH}	HIGH-level output voltage	I_{OH} = −8 mA; push-pull mode, all ports		$V_{DD} - 1.0$	-	-	V
		I_{OH} = −3.2 mA; push-pull mode, all ports		$V_{DD} - 0.7$	$V_{DD} - 0.4$	-	V
		I_{OH} = −20 µA; quasi-bidirectional mode, all ports		$V_{DD} - 0.3$	$V_{DD} - 0.2$	-	V
C_{iss}	input capacitance		[6]	-	-	15	pF
I_{IL}	LOW-level input current	V_I = 0.4 V; all ports	[7]	-	-	−80	µA
I_{LI}	input leakage current	$V_I = V_{IL}$ or V_{IH}; all ports	[8]	-	-	±1	µA
I_{THL}	HIGH-LOW transition current	V_I = 2.0 V at V_{DD} = 3.6 V; all ports	[9][10]	−30	-	−450	µA
$R_{RST\_N(int)}$	internal pull-up resistance on pin $\overline{RST}$			10	-	30	kΩ

Table 12. Static characteristics *…continued*

V_{DD} = 2.4 V to 3.6 V unless otherwise specified.
T_{amb} = −40 °C to +85 °C for industrial applications, unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ[1]	Max	Unit
V_{bo}	brownout trip voltage	2.4 V < V_{DD} < 3.6 V; with BOV = 1, BOPD = 0	2.40	-	2.70	V
$V_{ref(bg)}$	band gap reference voltage		1.19	1.23	1.27	V
TC_{bg}	band gap temperature coefficient		-	10	20	ppm/°C

[1] Typical ratings are not guaranteed. The values listed are at room temperature, 3 V.

[2] The $I_{DD(oper)}$, $I_{DD(idle)}$, and $I_{DD(pd)}$ specifications are measured using an external clock with the following functions disabled: comparators, real-time clock, and watchdog timer.

[3] The $I_{DD(oper)}$ and $I_{DD(idle)}$ specifications are measured using with the following functions disabled: comparators, real-time clock, and watchdog timer.

[4] The $I_{DD(tpd)}$ specification is measured using an external clock with the following functions disabled: comparators, real-time clock, brownout detect, and watchdog timer.

[5] Applies to all ports, in all modes except Hi-Z.

[6] Pin capacitance is characterized but not tested.

[7] Measured with port in quasi-bidirectional mode.

[8] Measured with port in high-impedance mode.

[9] Ports in quasi-bidirectional mode with weak pull-up (applies to all port pins with pull-ups)

[10] Port pins source a transition current when used in quasi-bidirectional mode and externally driven from logic 1 to logic 0. This current is highest when V_I is approximately 2 V.

12. Dynamic characteristics

Table 13. Dynamic characteristics (12 MHz)

V_{DD} = 2.4 V to 3.6 V unless otherwise specified.
T_{amb} = −40 °C to +85 °C for industrial applications, unless otherwise specified.[1]

Symbol	Parameter	Conditions	Variable clock		f_{ext} = 12 MHz		Unit
			Min	Max	Min	Max	
$f_{osc(RC)}$	internal RC oscillator frequency	clock doubler option = OFF (default); nominal f = 7.3728 MHz; trimmed to ±1 % at T_{amb} = 25 °C	7.189	7.557	7.189	7.557	MHz
		clock doubler option = ON; nominal f = 14.7456 MHz; V_{DD} = 2.7 V to 3.6 V	14.378	15.114	14.378	15.114	MHz
$f_{osc(WD)}$	internal watchdog oscillator frequency	nominal f = 400 kHz	320	520	320	520	kHz
$T_{cy(clk)}$	clock cycle time	see Figure 20	83	-	-	-	ns
f_{CLKLP}	low-power select clock frequency		0	8	-	-	MHz
External clock							
f_{ext}	external clock frequency		-	-	0	12	MHz
t_{CHCX}	clock HIGH time	V_{DD} = 2.7 V to 3.6 V; see Figure 20	33	$T_{cy(clk)} - t_{CLCX}$	33	-	ns
t_{CLCX}	clock LOW time		33	$T_{cy(clk)} - t_{CHCX}$	33	-	ns
t_{CLCH}	clock rise time		-	8	-	8	ns
t_{CHCL}	clock fall time		-	8	-	8	ns
Glitch filter							
t_{gr}	glitch rejection	P1.5/$\overline{RST}$ pin	-	50	-	50	ns
		any pin except P1.5/$\overline{RST}$	-	15	-	15	ns
t_{sa}	signal acceptance	P1.5/$\overline{RST}$ pin	125	-	125	-	ns
		any pin except P1.5/$\overline{RST}$	50	-	50	-	ns
Shift register (UART mode 0 - P89LPC9103)							
T_{XLXL}	serial port clock cycle time	see Figure 19	$16T_{cy(clk)}$	-	1333	-	ns
t_{QVXH}	output data set-up to clock rising edge	see Figure 19	$13T_{cy(clk)}$	-	1083	-	ns
t_{XHQX}	output data hold after clock rising edge	see Figure 19	-	$T_{cy(clk)}$ + 20	-	103	ns
t_{XHDX}	input data hold after clock rising edge	see Figure 19	-	0	-	0	ns
t_{XHDV}	input data valid to clock rising edge	see Figure 19	150	-	150	-	ns

[1] Parameters are valid over operating temperature range unless otherwise specified. Parts are tested to 2 MHz, but are guaranteed to operate down to 0 Hz.

Table 14. Dynamic characteristics (18 MHz)

V_{DD} = 3.0 V to 3.6 V unless otherwise specified.
T_{amb} = −40 °C to +85 °C for industrial applications, unless otherwise specified.[1]

Symbol	Parameter	Conditions	Variable clock		f_{ext} = 18 MHz		Unit
			Min	Max	Min	Max	
$f_{osc(RC)}$	internal RC oscillator frequency	clock doubler option = OFF (default); nominal f = 7.3728 MHz; trimmed to ±1 % at T_{amb} = 25 °C	7.189	7.557	7.189	7.557	MHz
		clock doubler option = ON; nominal f = 14.7456 MHz	14.378	15.114	14.378	15.114	MHz
$f_{osc(WD)}$	internal watchdog oscillator frequency	nominal f = 400 kHz	320	520	320	520	kHz
$T_{cy(clk)}$	clock cycle time	see Figure 20	83	-	-	-	ns
f_{CLKLP}	low-power select clock frequency		0	8	-	-	MHz
External clock							
f_{ext}	external clock frequency		-	-	0	18	MHz
t_{CHCX}	clock HIGH time	see Figure 20	22	$T_{cy(clk)} - t_{CLCX}$	22	-	ns
t_{CLCX}	clock LOW time		22	$T_{cy(clk)} - t_{CHCX}$	22	-	ns
t_{CLCH}	clock rise time		-	5	-	5	ns
t_{CHCL}	clock fall time		-	5	-	5	ns
Glitch filter							
t_{gr}	glitch rejection	P1.5/$\overline{RST}$ pin	-	50	-	50	ns
		any pin except P1.5/$\overline{RST}$	-	15	-	15	ns
t_{sa}	signal acceptance	P1.5/$\overline{RST}$ pin	125	-	125	-	ns
		any pin except P1.5/$\overline{RST}$	50	-	50	-	ns
Shift register (UART mode 0 - P89LPC9103)							
T_{XLXL}	serial port clock cycle time	see Figure 19	$16T_{cy(clk)}$	-	888	-	ns
t_{QVXH}	output data set-up to clock rising edge	see Figure 19	$13T_{cy(clk)}$	-	722	-	ns
t_{XHQX}	output data hold after clock rising edge	see Figure 19	-	$T_{cy(clk)}$ + 20	-	75	ns
t_{XHDX}	input data hold after clock rising edge	see Figure 19	-	0	-	0	ns
t_{XHDV}	input data valid to clock rising edge	see Figure 19	150	-	150	-	ns

[1] Parameters are valid over operating temperature range unless otherwise specified. Parts are tested to 2 MHz, but are guaranteed to operate down to 0 Hz.

12.1 Waveforms

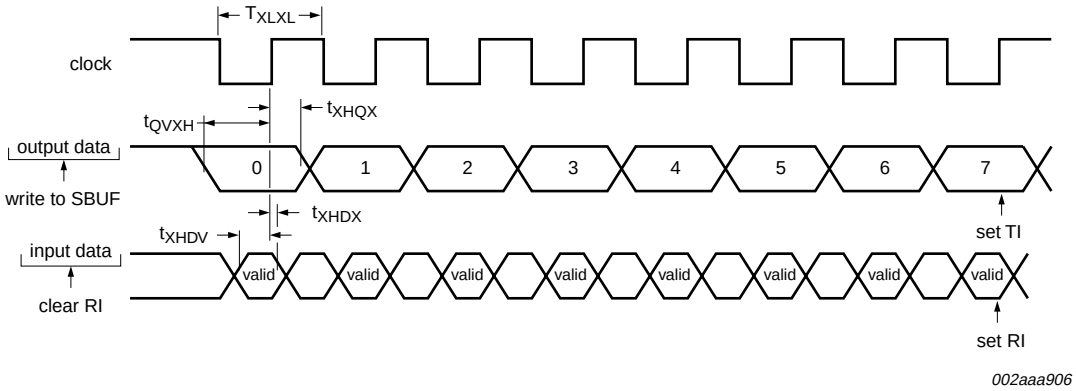


Fig 19. Shift register mode timing (P89LPC9103/9107)

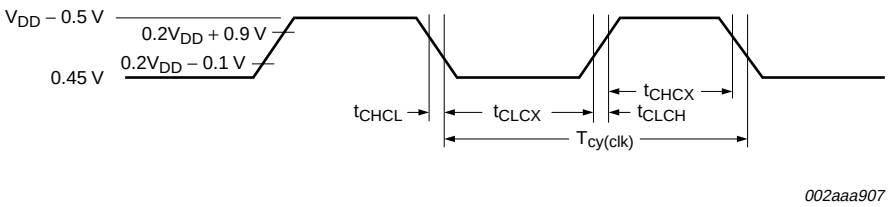


Fig 20. External clock timing

13. Other characteristics

13.1 Comparator electrical characteristics

Table 15. Comparator electrical characteristics

V_{DD} = 2.4 V to 3.6 V, unless otherwise specified.
T_{amb} = −40 °C to +85 °C for industrial applications, unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{IO}	input offset voltage		-	-	±10	mV
V_{IC}	common-mode input voltage		0	-	V_{DD} − 0.3	V
CMRR	common-mode rejection ratio	[1]	-	-	−50	dB
$t_{res(tot)}$	total response time		-	250	500	ns
$t_{(CE-OV)}$	chip enable to output valid time		-	-	10	µs
I_{LI}	input leakage current	0 V < V_I < V_{DD}	-	-	±1	µA

[1] This parameter is characterized, but not tested in production.

13.2 A/D converter electrical characteristics

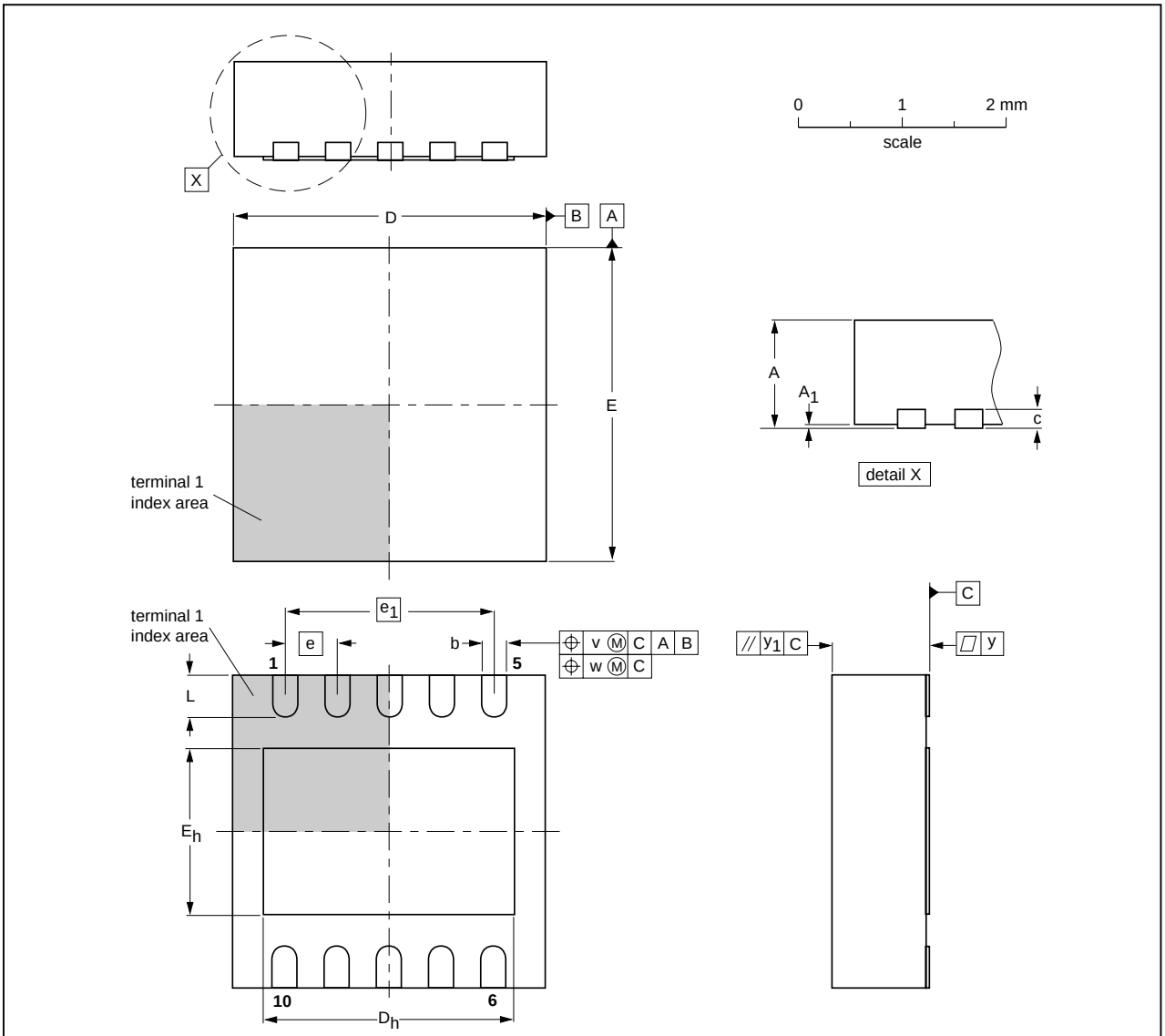
Table 16. A/D converter electrical characteristics

V_{DD} = 2.4 V to 3.6 V, unless otherwise specified.
T_{amb} = −40 °C to +85 °C for industrial applications, unless otherwise specified.
All limits valid for an external source impedance of less than 10 kΩ.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{IA}	analog input voltage		V_{SS} − 0.2	-	V_{SS} + 0.2	V
C_{iss}	input capacitance		-	-	15	pF
E_D	differential linearity error		-	-	±1	LSB
$E_{L(adj)}$	integral non-linearity		-	-	±1	LSB
E_O	offset error		-	-	±2	LSB
E_G	gain error		-	-	±1	%
$E_{u(tot)}$	total unadjusted error		-	-	±2	LSB
M_{CTC}	channel-to-channel matching		-	-	±1	LSB
$\alpha_{ct(port)}$	crosstalk between port inputs	0 kHz to 100 kHz	-	-	−60	dB
SR_{in}	input slew rate		-	-	100	V/ms
$T_{cy(ADC)}$	ADC clock cycle		111	-	2000	ns
t_{ADC}	ADC conversion time	A/D enabled	-	-	$13t_{CLK(ADC)}$	µs

14. Package outline

HVSON10: plastic thermal enhanced very thin small outline package; no leads; 10 terminals; body 3 x 3 x 0.85 mm **SOT650-1**



DIMENSIONS (mm are the original dimensions)

UNIT	$A^{(1)}$ max.	A_1	b	c	$D^{(1)}$	D_h	$E^{(1)}$	E_h	e	e_1	L	v	w	y	y_1
mm	1	0.05 0.00	0.30 0.18	0.2	3.1 2.9	2.55 2.15	3.1 2.9	1.75 1.45	0.5	2	0.55 0.30	0.1	0.05	0.05	0.1

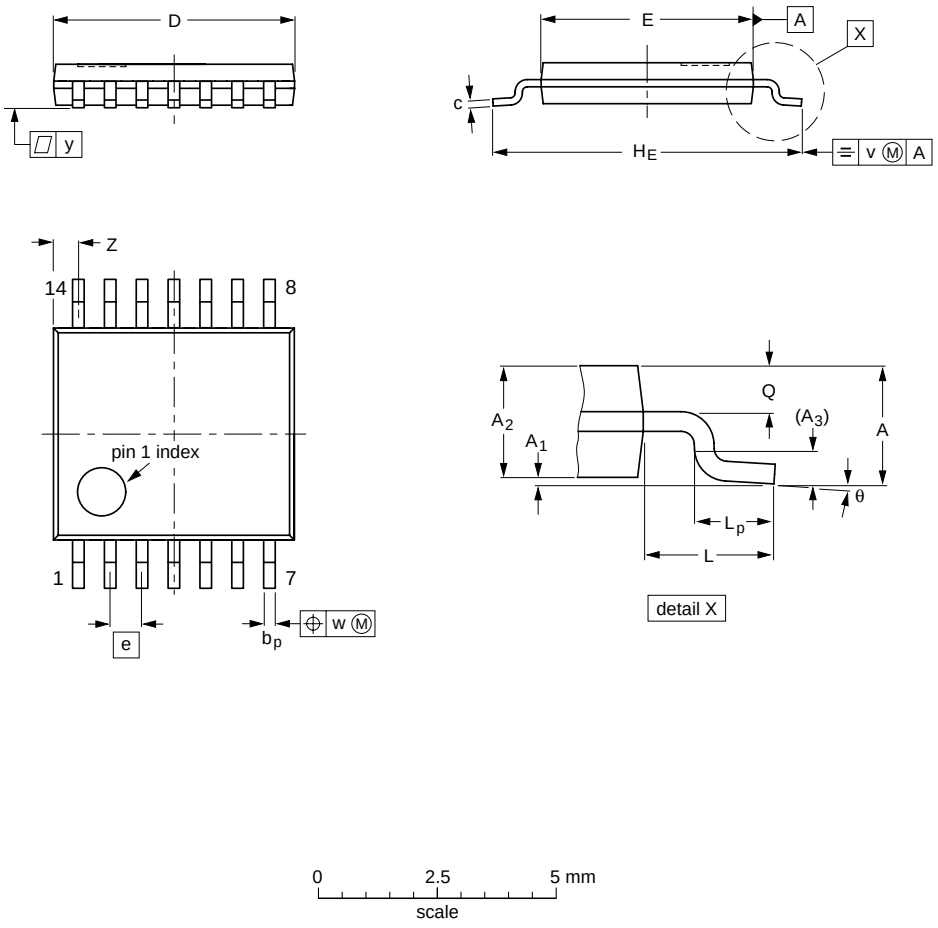
Note

1. Plastic or metal protrusions of 0.075 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT650-1	- - -	MO-229	- - -			~~01-01-22~~ 02-02-08

Fig 21. Package outline SOT650-1 (HVSON10)

TSSOP14: plastic thin shrink small outline package; 14 leads; body width 4.4 mm **SOT402-1**



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	D (1)	E (2)	e	H_E	L	L_p	Q	v	w	y	Z (1)	θ
mm	1.1	0.15 0.05	0.95 0.80	0.25	0.30 0.19	0.2 0.1	5.1 4.9	4.5 4.3	0.65	6.6 6.2	1	0.75 0.50	0.4 0.3	0.2	0.13	0.1	0.72 0.38	8^o 0^o

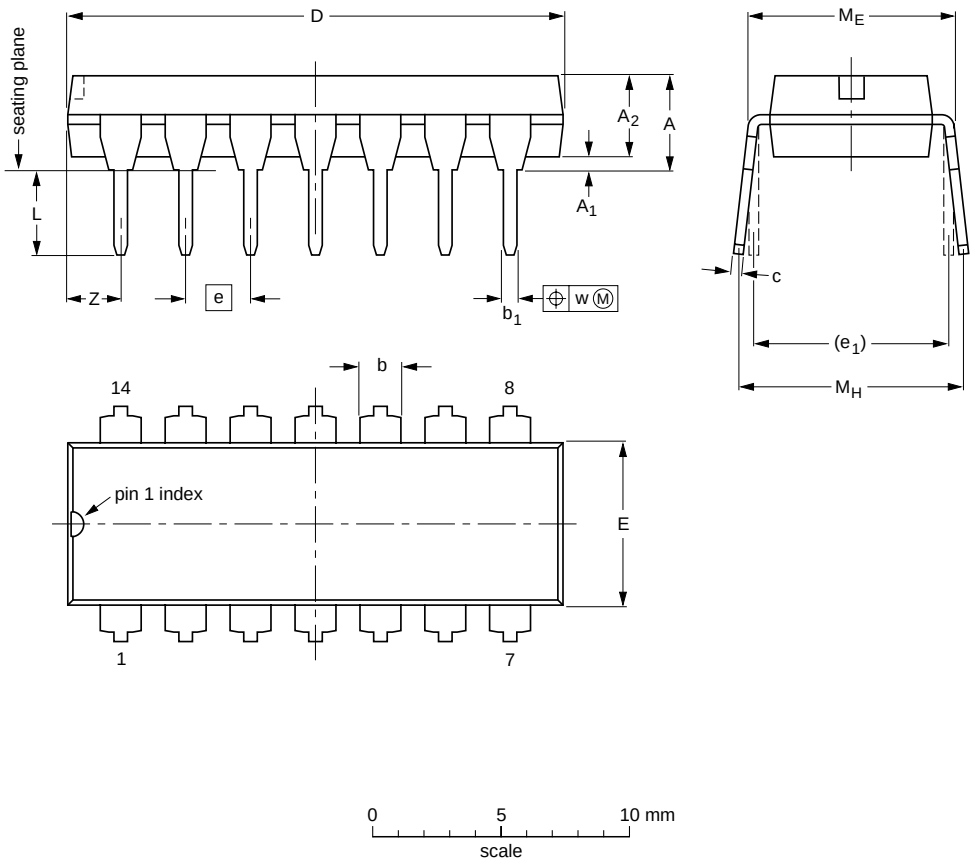
Notes

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.
2. Plastic interlead protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT402-1		MO-153				~~99-12-27~~ 03-02-18

Fig 22. Package outline SOT402-1 (TSSOP14)

DIP14: plastic dual in-line package; 14 leads (300 mil) **SOT27-1**



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A_1 min.	A_2 max.	b	b_1	c	D (1)	E (1)	e	e_1	L	M_E	M_H	w	Z (1) max.
mm	4.2	0.51	3.2	1.73 1.13	0.53 0.38	0.36 0.23	19.50 18.55	6.48 6.20	2.54	7.62	3.60 3.05	8.25 7.80	10.0 8.3	0.254	2.2
inches	0.17	0.02	0.13	0.068 0.044	0.021 0.015	0.014 0.009	0.77 0.73	0.26 0.24	0.1	0.3	0.14 0.12	0.32 0.31	0.39 0.33	0.01	0.087

Note

1. Plastic or metal protrusions of 0.25 mm (0.01 inch) maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT27-1	050G04	MO-001	SC-501-14			~~99-12-27~~ 03-02-13

Fig 23. Package outline SOT27-1 (DIP14)

15. Abbreviations

Table 17. Acronym list

Acronym	Description
A/D	Analog-to-Digital
BOE	Brownout Enable
CMRR	Common-Mode Rejection Ratio
DAC	Digital-to-Analog Converter
EMI	Electromagnetic Interference
IAP	In-Application Programming
ICP	In-Circuit Programming
LSB	Least Significant Bit
MSB	Most Significant Bit
PWM	Pulse Width Modulator
RTC	Real-Time Clock
SAR	Successive Approximation Register
UART	Universal Asynchronous Receiver/Transmitter

16. Revision history

Table 18. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
P89LPC9102_9103_ 9107_3	20070710	Product data sheet	-	P89LPC9102_9103_9107_2
Modifications:	• The format of this data sheet has been redesigned to comply with the new identity guidelines of NXP Semiconductors. • Legal texts have been adapted to the new company name where appropriate. • Added new device P89LPC9107FN.			
P89LPC9102_9103_ 9107_2	20050411	Product data sheet	-	P89LPC9102_9103_9107_1
P89LPC9102_9103_ 9107_1	20050111	Product data sheet	-	-

17. Legal information

17.1 Data sheet status

Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL http://www.nxp.com.

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