ELECTRONICS

THE DATASHEET OF

ONET2804TY

ONET2804T 28 Gbps 4-Channel Limiting TIA

1 Features

- 4-Channel Multi-Rate operation up to 28 Gbps
- 10 kΩ Differential Transimpedance
- 21 GHz Bandwidth
- 1.8 µA_{rms} Input Referred Noise
- 2.9 mA_{PP} Input Overload Current
- Programmable Output Voltage
- Adjustable Gain and Bandwidth
- Received Signal Strength Indicator (RSSI) for each Channel
- 40 dB Isolation Between Channels (Die only)
- Single 3.3 V Supply
- 139 mW per Channel
- Pad Control or 2-Wire Control
- On Chip Filter Capacitors
- –40°C to 100°C Operation
- Die Size: 3250 µm × 1450 µm, 750 µm Channel Pitch

2 Applications

- 100 Gigabit Ethernet Optical Receivers
- ITU OTL4.4
- CFP2, CFP4, and QSFP28 Modules with Internal Retiming

3 Description

The ONET2804T is a high gain limiting transimpedance amplifier for parallel optical interconnects with data rates up to 28 Gbps. The device is used in conjunction with a 750 µm pitch photodiode array to convert an optical signal into a differential output voltage. An internal circuit provides the photodiode reverse bias voltage and senses the average photocurrent supplied to each photodiode.

The device can be used with pin control or a two-wire serial interface to allow control of the output amplitude, gain, bandwidth and input threshold.

The ONET2804T provides 21 GHz bandwidth, a gain of 10 kΩ, an input referred noise of 1.8 µA_{rms} and a received signal strength indicator (RSSI) for each channel. 40 dB isolation between channels results in low crosstalk penalty in the receiver.

The part requires a single 3.3 V supply and typically dissipates 139 mW per channel with a differential output amplitude of 500 mV_{PP}. It is characterized for operation from –40°C to 100°C temperatures and is available in die form with a 750 µm channel pitch.

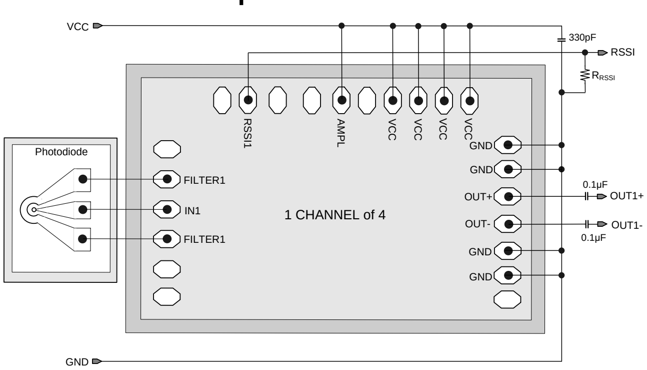
To request a full data sheet, please send an email to: onet2804t_request@ti.com.

Device Information(1)

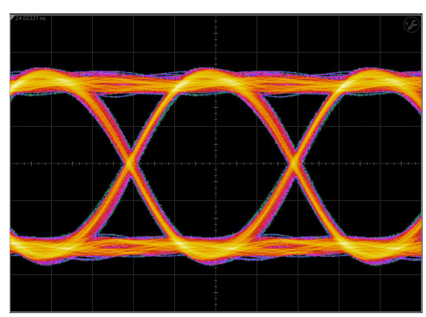
PART NUMBER	PACKAGE	BODY SIZE (NOM)
ONET2804T	Base die in Waffle Pack	3250 µm × 1450 µm

(1) For all available packages, see the orderable addendum at the end of the datasheet.

Simplified Schematic



Eye Diagram



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Changes from Revision A (April 2015) to Revision B **Page**

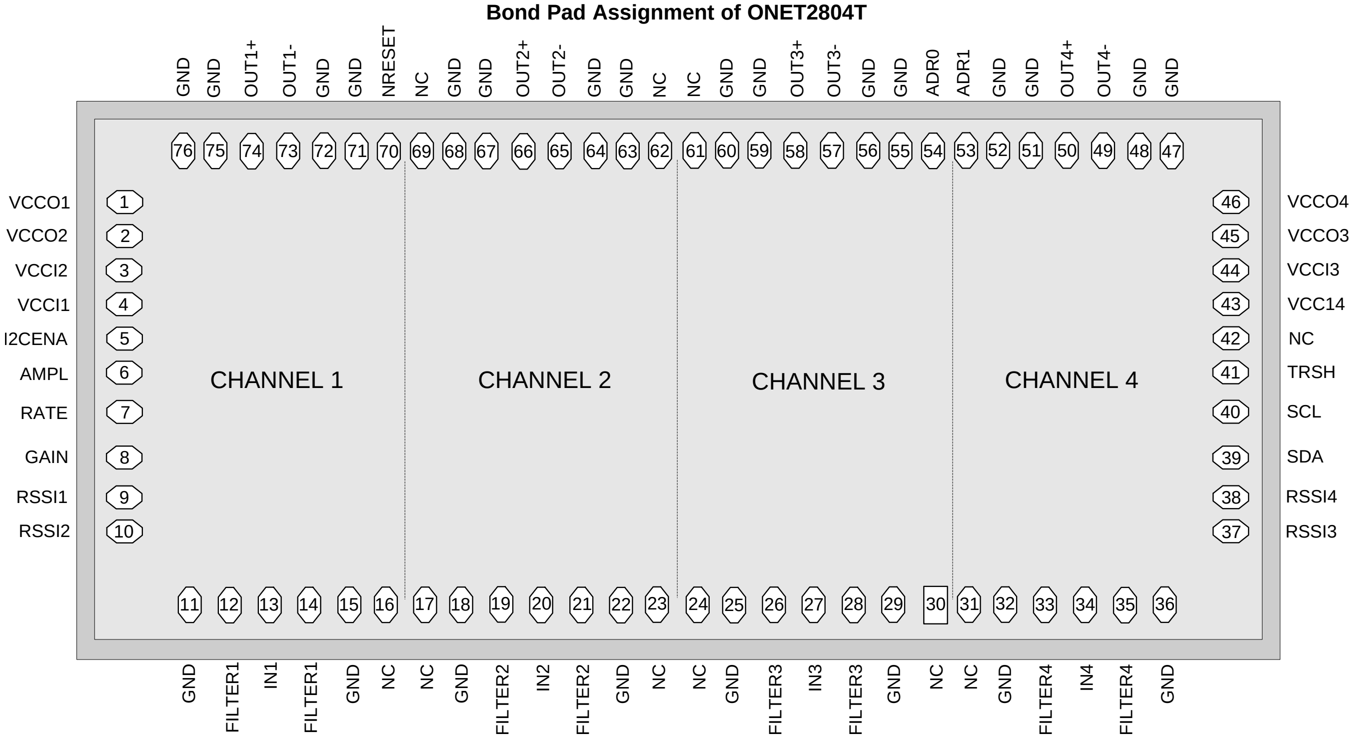
- First public release of data sheet ... 1
- Added *Receiving Notification of Documentation Updates* and *Community Resources* sections ... 31

Changes from Original (July 2014) to Revision A **Page**

- Changed text in the *Description* From: "differential output amplitude of 450 mV_{PP}" To: "differential output amplitude of 500 mV_{PP}" ... 1
- Changed PAD 6, AMPL Description From: "VCC: 450 mVpp differential output swing To: "VCC: 500 mVpp differential output swing" in *Bond Pad Functions* ... 4
- Changed From: *Handling Ratings* To: *ESD Ratings* ... 6
- Changed the Average Input current MAX value in the *Recommended Operating Conditions* From: 3 mA to: 2.7 mA ... 6
- Changed From: V_{OD} = 450 mV_{PP} To: V_{OD} = 500 mV_{PP} in the *DC Electrical Characteristics* condition statement ... 7
- Changed From: V_{OD} = 450 mV_{PP} To: V_{OD} = 500 mV_{PP} in the *AC Electrical Characteristics* condition statement ... 7
- Changed V_{OD} test conditions in the *AC Electrical Characteristics* From: 450 mV_{PP} To: V_{OD} = 500 mV_{PP} ... 7
- Changed V_{OD} values in the *AC Electrical Characteristics* , TYP From: 450 To: 500, MAX From: 650 To: 700 mV_{PP} ... 7
- Changed From: V_{OD} = 450 mV_{PP} To: V_{OD} = 500 mV_{PP} in the *Typical Characteristics* condition statement ... 8
- Changed text in *Amplitude Adjustment* From: "450 mVpp if the pad is tied to VCC" To: "500 mVpp if the pad is tied to VCC" ... 12
- Changed From: [reset = 9h] To: [reset = 0h] in *Register 1 (0x01) – Amplitude and Rate for Channel 1 (offset = 1h) [reset = 0h]* ... 17
- Changed Table 3, Reset value 9h To: 0h. Moved (default) From 10010 To: 0000 ... 17
- Changed From: [reset = 9h] To: [reset = 0h] in *Register 7 (0x07) – Amplitude and Rate for Channel 2 (offset = 7h) [reset = 0h]* ... 18
- Changed Table 9, Reset value 9h To: 0h. Moved (default) From 10010 To: 0000 ... 18
- Changed From: [reset = 9h] To: [reset = 0h] in *Register 13 (0x0D) – Amplitude and Rate for Channel 3 (offset = Dh) [reset = 0h]* ... 20
- Changed Table 15, Moved (default) From 10010 To: 0000 ... 20
- Changed From: [reset = 9h] To: [reset = 0h] in *Register 19 (0x13) – Amplitude and Rate for Channel 4 (offset =*

5 Pin Configuration and Functions

Bond Pad Assignment of ONET2804T



Bond Pad Functions

PAD	SYMBOL	TYPE	DESCRIPTION
6	AMPL	Digital input	3-state input for amplitude control of all 4 channels. VCC: 500 mVpp differential output swing Open: 300 mVpp differential output swing (default) GND: 250 mVpp differential output swing.
53	ADR1	Digital input	2-wire interface address programming pin. Leave this pad open for a default address of 0001100. Grounding this pad changes the 2nd address bit to a 1 (0001110).
54	ADR0	Digital input	2-wire interface address programming pin. Leave this pad open for a default address of 0001100. Grounding this pad changes the 1st address bit to a 1 (0001101).
12, 14, 19, 21, 26, 28, 33, 35	FILTERx	Analog output	Bias voltage for photodiode cathode. These pads are biased to VCC - 100 mV.
8	GAIN	Digital input	3-state input for gain control of all 4 channels. VCC: Minimum transimpedance Open: Default transimpedance GND: Medium transimpedance
11, 15, 18, 22, 25, 29, 32, 36, 47, 48, 51, 52, 55, 56, 59, 60, 63, 64, 67, 68, 71, 72, 75, 76	GND	Supply	Circuit ground. All GND pads are connected on die. Bonding all pads is recommended, except for 11, 15, 18, 22, 25,29,32, and 36.
5	I2CENA	Digital input	2-wire control option. Leave the pad unconnected for pad control of the IC. Two-wire control can be enabled by applying a high signal to the pad.
13, 20, 27, 34	INx	Analog input	Data input to TIAx (connect to photodiode anode).
16, 17, 23, 24, 30, 31, 42, 61, 62, 69	NC	No Connect	Do not connect
70	NRESET	Digital input	Used to reset the 2-wire state machine and registers. Leave open for normal operation and set low to reset the 2-wire interface.
49, 57, 65, 73	OUTx–	Analog output	Inverted CML data output for channel x. On-chip 50 Ω back-terminated to V_{CC}.

Bond Pad Functions (continued)

PAD	SYMBOL	TYPE	DESCRIPTION
50, 58, 66, 74	OUTx+	Analog output	Non-inverted CML data output for channel x. On-chip 50 Ω back-terminated to V_{CC}.
7	RATE	Digital input	3-state input for bandwidth control of all 4 channels. VCC: Increase the bandwidth Open: 21 GHz bandwidth (default) GND: reduce the bandwidth
9, 10, 37, 38	RSSIx	Analog output	Indicates the strength of the received signal (RSSI) for channel x if the photo diode is biased from FILTERx. The analog output current is proportional to the input data amplitude. Connect to an external resistor to ground (GND). For proper operation, ensure that the voltage at the RSSI pad does not exceed V_{CC} - 0.65 V. If the RSSI feature is not used these pads should be left open.
40	SCL	Digital input	2-wire interface serial clock input. Includes a 10 kΩ pull-up resistor to V_{CC}.
39	SDA	Digital –in/out	2-wire interface serial data input. Includes a 10 kΩ pull-up resistor to V_{CC}.
41	TRSH	Digital input	3-state input for threshold control. VCC: Crossing point shifted down Open: No threshold adjustment (default) GND: Crossing point shifted up
1, 2, 45, 46	VCCOx	Supply	2.97 V – 3.47 V supply voltage for AGCx and CMLx amplifiers.
3, 4, 43, 44	VCCIx	Supply	2.97 V – 3.47 V supply voltage for input TIAx stage.

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
Supply voltage(1)	VCCIx, VCCOx	–0.3	4	V
Voltage(1)	FILTERx, OUTx+, OUTx–, RSSIx, SCL, SDA, I2CENA, AMPL, RATE, GAIN, TRSH, ADR1, ADR0 and NRESET	–0.3	4	V
Average Input current	INx	–0.7	5	mA
	FILTERx	–8	8	mA
Continuous current at outputs	OUTx+, OUTx–	–8	8	mA
Maximum junction temperature, T_J			125	°C
Storage temperature, T_{stg}		–65	150	°C

(1) All voltage values are with respect to network ground terminal.

6.2 ESD Ratings

				VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001 (1)	All pins except input INx	±1000	V
			Pin INx	±500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

			MIN	TYP	MAX	UNIT
V_{CC}	Supply voltage		2.97	3.3	3.47	V
$I_{(INx)}$	Average Input current				2.7	mA
T_A	Operating backside die temperature		–40		100	°C
$L_{(FILTER)}$, $L_{(IN)}$	Wire-bond inductance at pins FILTERx and INx			0.3		nH
$C_{(PD)}$	Photodiode Capacitance			0.1		pF
V_{IH}	Digital input high voltage	SDA, SCL	2			V
V_{IL}	Digital input low voltage	SDA, SCL			0.8	V
	3-state input high voltage		V_{CC} - 0.4			V
	3-state input low voltage				0.4	V

6.4 DC Electrical Characteristics

Over recommended operating conditions with V_{OD} = 500 mV_{PP} unless otherwise noted. Typical values are at V_{CC} = 3.3 V and T_A = 25°C

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{CC}	Supply voltage		2.97	3.3	3.47	V
I_{CC}	Supply current	Per channel, 30 μA_{PP} input, maximum 85°C		42	57(1)	mA
		Per channel, 30 μA_{PP} input, maximum 100°C			60(1)	
$P_{(RX)}$	Receiver power dissipation	Per channel, 30 μA_{PP} input, maximum 85°C		139	198	mW
		Per channel, 30 μA_{PP} input, maximum 100°C			208	
V_{IN}	Input bias voltage		0.75	0.85	0.98	V
R_{OUT}	Output resistance	Single-ended to V_{CC}	40	50	60	Ω
$V_{(FILTER)}$	Photodiode bias voltage(2)		2.8	3.2		V
$A_{(RSSI\_IB)}$	RSSI gain	Resistive load to GND(3)	0.49	0.5	0.54	A/A
	RSSI output offset current (no light)		0		2.5	µA

(1) Including RSSI current
(2) Regulated voltage typically 100mV lower than V_{CC}.
(3) The RSSI output is a current output, which requires a resistive load to ground (GND). The voltage gain can be adjusted for the intended application by choosing the external resistor; however, for proper operation, ensure that the voltage at RSSI does not exceed VCC-0.65V.

6.5 AC Electrical Characteristics

Over recommended operating conditions with V_{OD} = 500 mV_{PP} unless otherwise noted. Typical values are at V_{CC} = 3.3 V and T_A = 25°C

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
Z_{21}	Small signal transimpedance	25 μA_{PP} input signal	7	10		kΩ
$f_{(3dB-H)}$	–3dB bandwidth	25 μA_{PP} input signal(1)	18.5	21		GHz
$f_{(3dB-L)}$	Low frequency –3dB bandwidth			30	100	kHz
$i_{N(IN)}$	Input referred RMS noise	CPD = 0.1 pF, 28 GHz BT4 filter(2)		1.8	2.5	µA
DJ	Deterministic jitter	35 μA_{pp} < i_{IN} < 250 μA_{pp} (27.95 Gbps, PRBS9 pattern)		2		ps_{pp}
		250 μA_{pp} < i_{IN} < 500 μA_{pp} (27.95 Gbps, PRBS9 pattern)		2		
		500 μA_{pp} < i_{IN} < 2900 μA_{pp} (27.95 Gbps, PRBS9 pattern)		4		
V_{OD}	Differential output voltage	500 mV_{PP} setting	250	500	700	mV_{PP}
	Crosstalk	Between adjacent channels, up to 20 GHz(3)		–40		dB
	RSSI response time			1		µs
PSRR	Power supply rejection ratio	F < 10 MHz(4)		–15		dB

(1) The small signal bandwidth is specified over process corners, temperature, and supply voltage variation. The assumed photodiode capacitance is 0.1pF and the bond-wire inductance is 0.3nH. The small signal bandwidth strongly depends on environmental parasitics. Careful attention to layout parasitics and external components is necessary to achieve optimal performance.
(2) Input referred RMS noise is (RMS output noise)/ (gain at 100 MHz).
(3) Die only, no wire bonds
(4) PSRR is the differential output amplitude divided by the voltage ripple on the supply. No input current at IN.

6.6 Typical Characteristics

Typical operating condition is at V_{CC} = 3.3 V, T_A = 25°C and V_{OD} = 500 mVpp (unless otherwise noted).

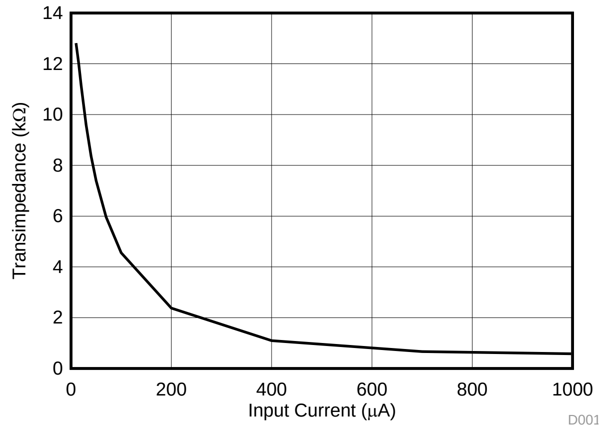


Figure 1. Transimpedance vs Input Current

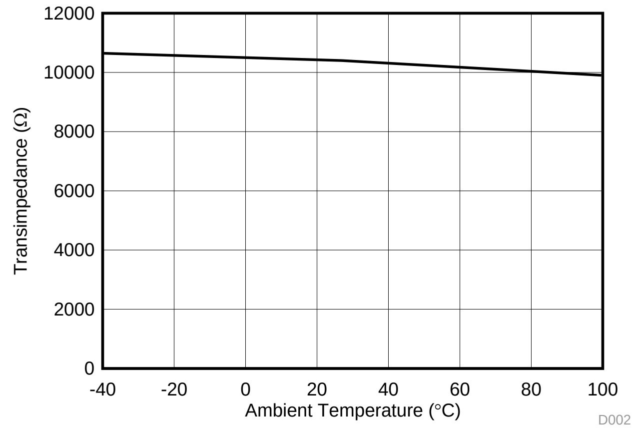


Figure 2. Small Signal Transimpedance vs Ambient Temperature

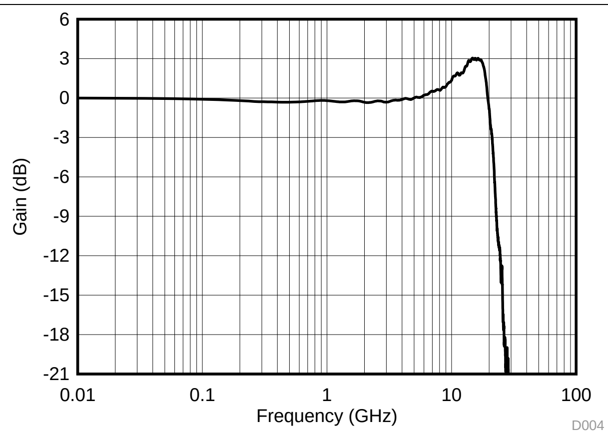


Figure 3. Gain vs Frequency (Test Fixture loss De-embedded)

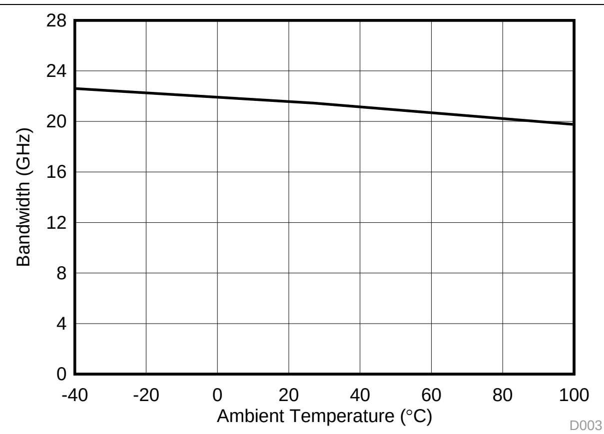


Figure 4. Small Signal Bandwidth vs Ambient Temperature (Test Fixture loss De-embedded)

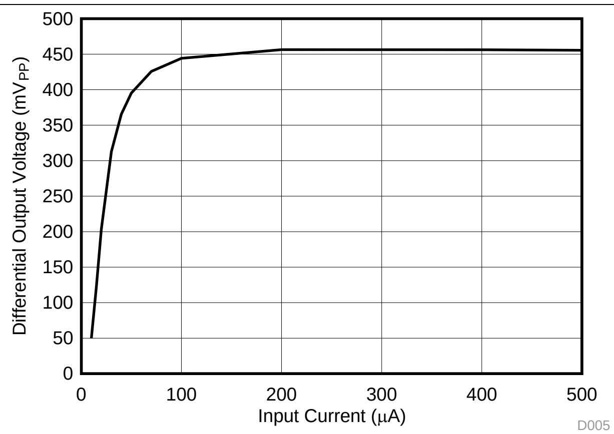


Figure 5. Output Voltage vs Input Current

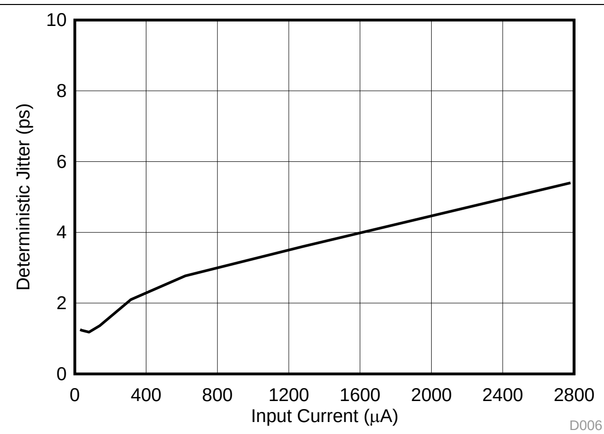


Figure 6. Deterministic Jitter vs Input Current

Typical Characteristics (continued)

Typical operating condition is at V_{CC} = 3.3 V, T_A = 25°C and V_{OD} = 500 mVpp (unless otherwise noted).

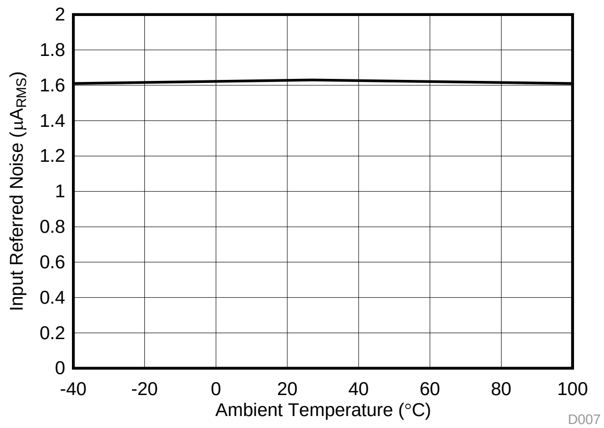


Figure 7. Input Referred Noise vs Temperature

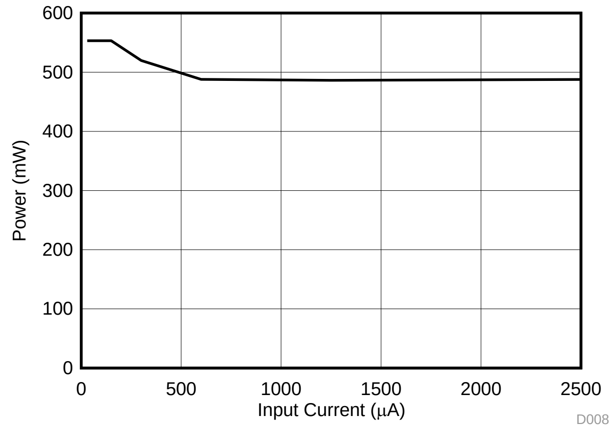


Figure 8. Power vs Input Current

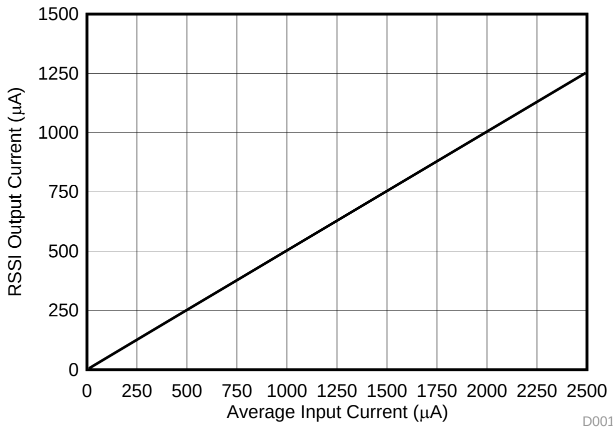
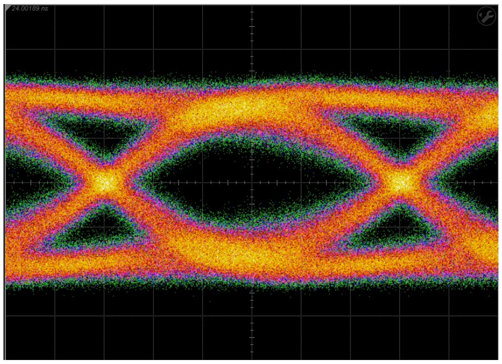


Figure 9. RSSI Output Current vs Average Input Current

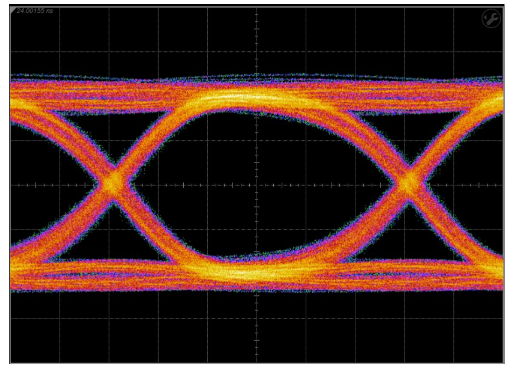
Typical Characteristics (continued)

Typical operating condition is at V_{CC} = 3.3 V, T_A = 25°C and V_{OD} = 500 mVpp (unless otherwise noted).



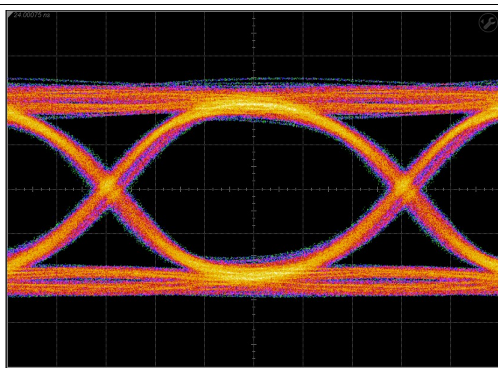
27.95 GBPS

Figure 10. Output Eye-Diagram, 30 μA$_{P-P}$ Input Current



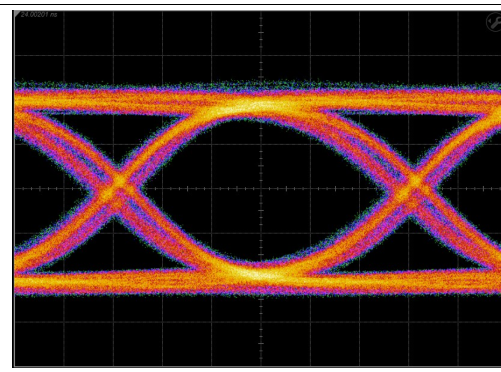
27.95 GBPS

Figure 11. Output Eye-Diagram, 500 μA$_{P-P}$ Input Current



27.95 GBPS

Figure 12. Output Eye-Diagram, 1.5 mA$_{P-P}$ Input Current



27.95 GBPS

Figure 13. Output Eye-Diagram, 2.5 mA$_{P-P}$ Input Current

7 Detailed Description

7.1 Overview

A simplified block diagram of one channel of the ONET2804T is shown in *Functional Block Diagram*.

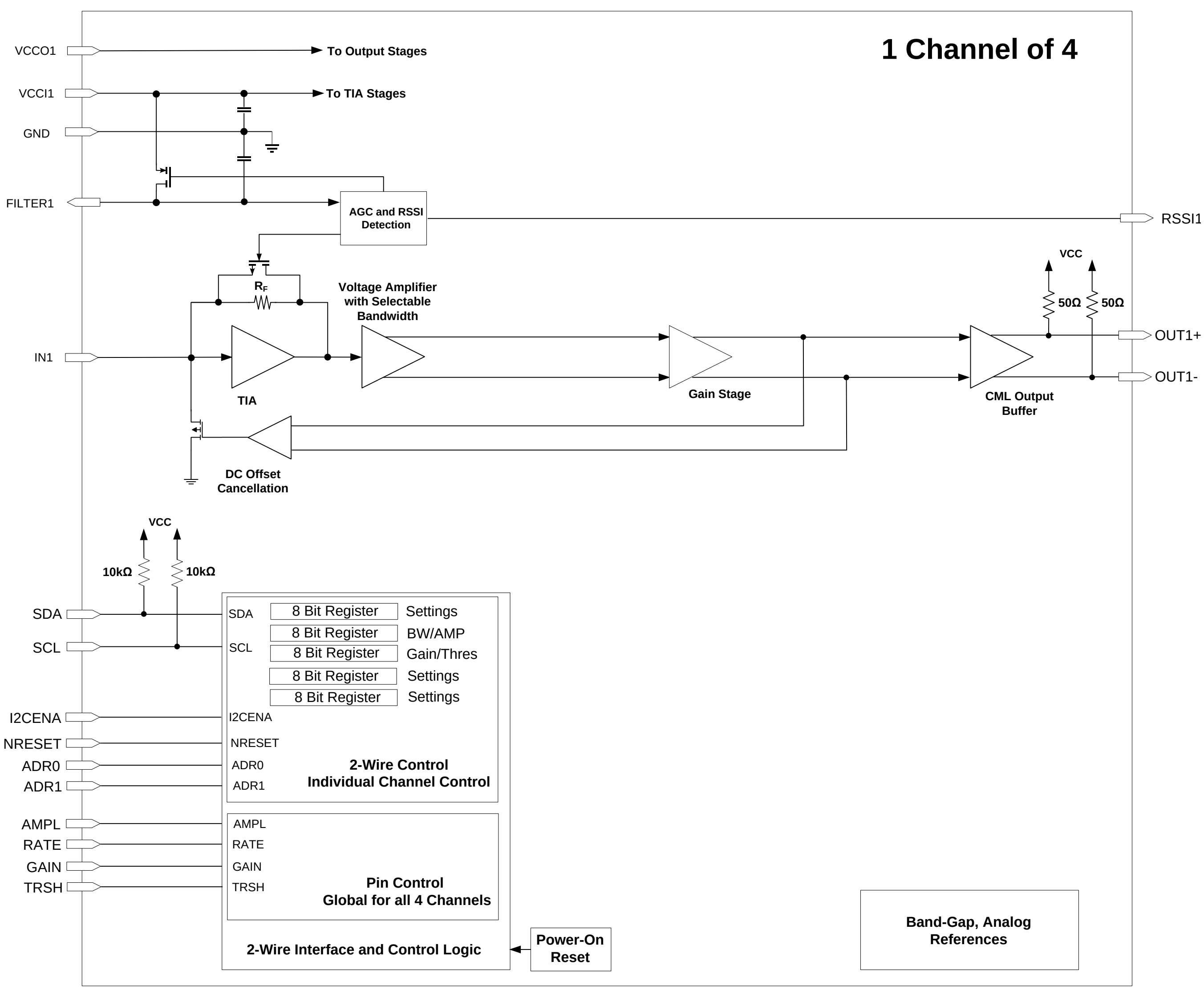
The ONET2804T consists of the signal path, supply filters, a control block for DC input bias, automatic gain control (AGC) and received signal strength indication (RSSI), an analog reference block and a 2-wire serial interface and control logic block.

The signal path consists of a transimpedance amplifier stage, a voltage amplifier, and a CML output buffer. The on-chip filter circuit provides a filtered V_{CC} for the PIN photodiode and for the transimpedance amplifier. The RSSI provides the bias for the TIA stage and the control for the AGC.

The DC input bias circuit and automatic gain control use internal low pass filters to cancel the DC current on the input and to adjust the transimpedance amplifier gain. Furthermore, circuitry is provided to monitor the received signal strength.

The output amplitude, gain, bandwidth and input threshold can be globally controlled through pin settings or each channel can be individually controlled through the 2-wire interface.

7.2 Functional Block Diagram



7.3 Feature Description

7.3.1 Signal Path

The first stage of the signal path is a transimpedance amplifier which converts the photodiode current into a voltage. If the input signal current exceeds a certain value, the transimpedance gain is reduced by means of a nonlinear AGC circuit to limit the signal amplitude.

The second stage is a limiting voltage amplifier that provides additional limiting gain and converts the single ended input voltage into a differential data signal. The output stage provides CML outputs with an on-chip 50Ω back-termination to V_{CC}.

The TIA has adjustable gain, amplitude, bandwidth and input threshold and they can be globally controlled through pad settings or each channel can be individually controlled through the 2-wire interface. The default mode of operation is pad control where the state (OPEN, HI or LO) of the AMPL, BW, GAIN and TRSH pads sets the respective parameter. To enable 2-wire control, the I2CENA pad should be set HIGH and the functionality of each channel can be controlled individually through the 2-wire interface.

7.3.2 Gain Adjustment

The gain of all TIAs can be adjusted using the GAIN pad (pad 8) in pad control mode. The gain is set to default if the pad is left open. The gain is reduced approximately 4 dB if the pad is tied to ground, and reduced approximately 8 dB if the pad is tied to VCC. In 2-wire control mode, the gain of each channel can be adjusted from minimum to default. The gain is controlled with the GAIN[0..1] bits in registers 2, 8, 14 and 20 respectively for channels 1, 2, 3 and 4.

7.3.3 Amplitude Adjustment

The output amplifier of all buffers can be adjusted using the AMPL pad (pad 6) in pad control mode. The amplitude is set to 300 mVpp differential if the pad is left open, 250 mVpp if the pad is tied to ground and 500 mVpp if the pad is tied to VCC (recommended mode of operation). In 2-wire control mode, the amplitude of each channel can be adjusted from 0mVpp to 600 mVpp. The amplitude is controlled with the AMPL[0..3] bits in registers 1, 7, 13 and 19 respectively for channels 1, 2, 3 and 4.

7.3.4 Rate Select

The small signal bandwidth can be adjusted using the RATE pad (pad 7) in pad control mode. The bandwidth is typically 21 GHz if the pad is left open. The bandwidth is reduced approximately 0.4 GHz if the pad is tied to ground, and increased by approximately 0.4 GHz if the pad is tied to VCC. In 2-wire control mode, the bandwidth of each channel can be adjusted up or down using the register settings RATE[0..3] in registers 1, 7, 13 and 19 respectively for channels 1, 2, 3 and 4.

7.3.5 Threshold Adjustment

The TIAs have DC offset cancellation to maintain a 50% crossing point; however, the crossing point can be adjusted using the TRSH pad (pad 41) in pad control mode. No threshold adjustment is applied if the pad is left open. The crossing point is shifted up approximately 12% if the pad is tied to ground, and it is shifted down approximately 12% if the pad is tied to VCC. In 2-wire control mode, the crossing point can be adjusted up or down using register settings TH[0..3] in registers 2, 8, 14 and 20 for channels 1, 2, 3 and 4.

7.3.6 Filter Circuitry

The FILTER pins provide a regulated and filtered VCC for a PIN photodiode bias. The supply voltages for the transimpedance amplifier have on-chip capacitors but it is recommended to use external filter capacitors as well for best performance. The input stage has a separate VCC supply (VCCI) which is not connected on chip to the supply of the limiting and CML stages (VCCO).

7.3.7 AGC and RSSI

The voltage drop across the regulated photodiode FET is monitored by the bias and RSSI control circuit block in the case where a PIN diode is biased using the FILTER pins.

If the DC input current exceeds a certain level then it is partially cancelled by means of a controlled current source. This keeps the transimpedance amplifier stage within sufficient operating limits for optimum performance.

Feature Description (continued)

The automatic gain control circuitry adjusts the voltage gain of the AGC amplifier to ensure limiting behavior of the complete amplifier.

Finally this circuit block senses the current through the FILTER FET and generates a mirrored current that is proportional to the input signal strength. The mirrored currents are available at the RSSI outputs and can be sunk to ground (GND) using an external resistor. For proper operation, ensure that the voltage at the RSSI pad does not exceed VCC - 0.65 V.

7.4 Device Functional Modes

The device has two functional modes of operation: pad control mode and 2-wire interface control mode.

7.4.1 Pad Control

The default mode of operation is pad control and it is recommended that the amplitude be increased to the 500 mVpp setting by bonding AMPL (pad 6) to VCC. If further adjustment is desired as described above, then the control pads RATE (pad 7), GAIN (pad 8) and TRSH (pad 41) and can be bonded to either ground or VCC.

7.4.2 2-Wire Interface Control

To enable 2-wire interface control I2CENA (pad 5) must be bonded to VCC. In this mode of operation pad control is not functional and all control is initiated through the 2-wire interface as described in the *2-Wire Interface and Control Logic* section.

7.4.3 2-Wire Interface and Control Logic

The ONET2804T uses a 2-wire serial interface for digital control. For example, the two circuit inputs, SDA and SCK, are driven by the serial data and serial clock from a microcontroller. Both inputs include 10 kΩ pull-up resistors to VCC. For driving these inputs, an open drain output is recommended. The 2-wire interface allows write access to the internal memory map to modify control registers and read access to read out control and status signals. The ONET2804T is a slave device only which means that it cannot initiate a transmission itself; it always relies on the availability of the SCK signal for the duration of the transmission. The master device provides the clock signal as well as the START and STOP commands. It is recommended that the device be used on a bus with only one master. The protocol for a data transmission is as follows:

1. START command
2. 7 bit slave address (0001100) followed by an eighth bit which is the data direction bit (R/W). A zero indicates a WRITE and a 1 indicates a READ.
3. 8 bit register address
4. 8 bit register data word
5. STOP command

Regarding timing, the ONET2804T is I^2C compatible. The typical timing is shown in Figure 14 and a complete data transfer is shown in Figure 15. Parameters for Figure 14 are defined in Table 1.

7.4.4 Bus Idle

Both SDA and SCK lines remain HIGH

7.4.5 Start Data Transfer

A change in the state of the SDA line, from HIGH to LOW, while the SCK line is HIGH, defines a START condition (S). Each data transfer is initiated with a START condition.

7.4.6 Stop Data Transfer

A change in the state of the SDA line from LOW to HIGH while the SCK line is HIGH defines a STOP condition (P). Each data transfer is terminated with a STOP condition; however, if the master still wishes to communicate on the bus, it can generate a repeated START condition and address another slave without first generating a STOP condition.

Device Functional Modes (continued)

7.4.7 Data Transfer

Only one data byte can be transferred between a START and a STOP condition. The receiver acknowledges the transfer of data.

7.4.8 Acknowledge

Each receiving device, when addressed, is obliged to generate an acknowledge bit. The transmitter releases the SDA line and a device that acknowledges must pull down the SDA line during the acknowledge clock pulse in such a way that the SDA line is stable LOW during the HIGH period of the acknowledge clock pulse. Setup and hold times must be taken into account. When a slave-receiver does not acknowledge the slave address, the data line must be left HIGH by the slave. The master can then generate a STOP condition to abort the transfer. If the slave-receiver does acknowledge the slave address but some time later in the transfer cannot receive any more data bytes, the master must abort the transfer. This is indicated by the slave generating the not acknowledge on the first byte to follow. The slave leaves the data line HIGH and the master generates the STOP condition.

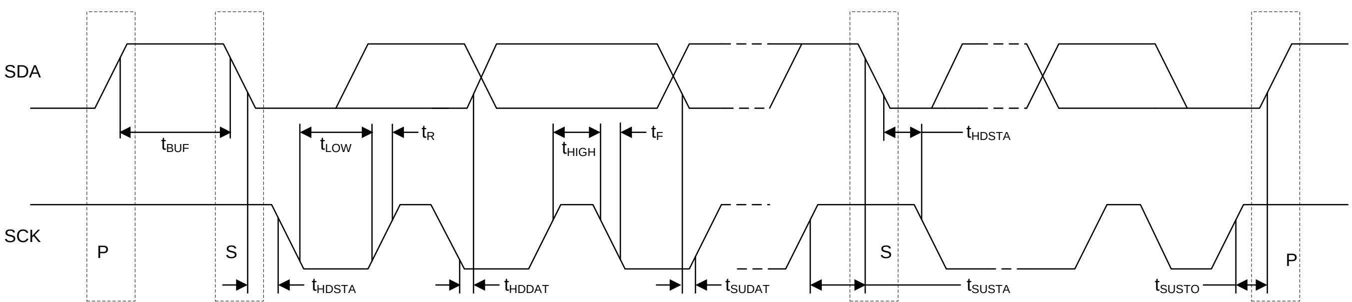


Figure 14. I²C Timing Diagram

Table 1. Timing Diagram Definitions

		MIN	MAX	UNIT
f_{SCK}	SCK clock frequency		400	kHz
t_{BUF}	Bus free time between START and STOP conditions	1.3		µs
t_{HDSTA}	Hold time after repeated START condition. After this period, the first clock pulse is generated	0.6		µs
t_{LOW}	Low period of the SCK clock	1.3		µs
t_{HIGH}	High period of the SCK clock	0.6		µs
t_{SUSTA}	Setup time for a repeated START condition	0.6		µs
t_{HDDAT}	Data HOLD time	0		µs
t_{SUDAT}	Data setup time	100		ns
t_R	Rise time of both SDA and SCK signals		300	ns
t_F	Fall time of both SDA and SCK signals		300	ns
t_{SUSTO}	Setup time for STOP condition	0.6		µs

Write Sequence

1	7	1	1	8	1	8	1	1
S	Slave Address	Wr	A	Register Address	A	Data Byte	A	P

Read Sequence

1	7	1	1	8	1	1	7	1	1	8	1	1
S	Slave Address	Wr	A	Register Address	A	S	Slave Address	Rd	A	Data Byte	N	P

Legend

S	Start Condition
Wr	Write Bit (bit value = 0)
Rd	Read Bit (bit value = 1)
A	Acknowledge
N	Not Acknowledge
P	Stop Condition

Figure 15. Data Transfer

7.5 Register Maps

The register mapping for register addresses 0 (0x00) through 15 (0x0F) are shown in Table 2 through Table 27. Figure 16 through Figure 41 describes the circuit functionality based on the register settings.

7.5.1 Register 0 (0x00) – Control Settings (offset = 0h) [reset = 0h]

Figure 16. Register 0 (0x00) – Control Settings

bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
RESET	PD	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	PWRITE

Table 2. Register 0 (0x00) – Control Settings Field Descriptions

Bit	Field	Type	Reset	Description
7	RESET	W	0h	**Reset registers bit** 1 = Resets all registers to default values 0 = Normal operation
6	PD	R/W	0h	**Power down bit** 1 = Power down all channels (I_{CC} ≈ 4 mA) 0 = Normal operation
5	Reserved			
4	Reserved			
3	Reserved			
2	Reserved			
1	Reserved			
0	PWRITE	R/W	0h	**Parallel write mode bit** 1 = Parallel write enabled (write register value to all channels) 0 = Serial write

7.5.2 Register 1 (0x01) – Amplitude and Rate for Channel 1 (offset = 1h) [reset = 0h]

Figure 17. Register 1 (0x01) – Amplitude and Rate for Channel 1

bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
RATE3	RATE2	RATE1	RATE0	AMP3	AMP2	AMP1	AMP0

Table 3. Register 1 (0x01) – Amplitude and Rate for Channel 1 Field Descriptions

Bit	Field	Type	Reset	Description
7 6 5 4	RATE3 RATE2 RATE1 RATE0	R/W	0h	**Rate adjustments bits for channel 1** 0000 – 21 GHz (default) 0111 – BW decrease of approximately 0.4 GHz 1111 – BW increase of approximately 0.4 GHz
3 2 1 0	AMP3 AMP2 AMP1 AMP0	R/W	0h	**Amplitude adjustment bits for channel 1** 0000 – 0mVpp (default) 1000 – 250mVpp 0001 – 50mVpp 1001 – 300mVpp 0010 – 100mVpp 1010 – 350mVpp 0011 – 150mVpp 1011 – 400mVpp 0100 – 200mVpp 1100 – 450mVpp 0101 – 250mVpp 1101 – 500mVpp 0110 – 300mVpp 1110 – 550mVpp 0111 – 350mVpp 1111 – 600mVpp

7.5.3 Register 2 (0x02) Mapping – Threshold and Gain for Channel 1 (offset = 2h) [reset = 0h]

Figure 18. Register 2 (0x02) – Threshold and Gain for Channel 1

bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
PD	DIS	GAIN1	GAIN0	TH3	TH2	TH1	TH0

Table 4. Register 2 (0x02) – Threshold and Gain for Channel 1

Bit	Field	Type	Reset	Description
7	PD	R/W	0h	**Power down bit for channel 1** 1 = Power down channel 1 0 = Normal operation
6	DIS	R/W	0h	**Disable output buffer for channel 1** 1 = Disable channel 1 output buffer 0 = Normal operation
5 4	GAIN1 GAIN0	R/W	0h	**Gain adjustment bits for channel 1** 00 – default 10 – medium (–4 dB) 01 – NA 11 – minimum (–8 dB)
3 2 1 0	TH3 TH2 TH1 TH0	R/W	0h	**Threshold adjustment bits for channel 1** Minimum positive shift for 0001 Maximum positive shift for 0111 Zero shift for 0000 or 1000 Minimum negative shift for 1001 Maximum negative shift for 1111

7.5.4 Register 3 (0x03) – Reserved

Figure 19. Register 3 (0x03) – Reserved

bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
–	–	–	–	–	–	–	–

Table 5. Register 3 (0x03) – Reserved Field Descriptions

Bit	Field	Type	Reset	Description
0-7	–			Reserved

7.5.5 Register 4 (0x04) – Reserved

Figure 20. Register 4 (0x04) – Reserved

bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
–	–	–	–	–	–	–	–

Table 6. Register 4 (0x04) – Reserved Field Descriptions

Bit	Field	Type	Reset	Description
0-7	–			Reserved

7.5.6 Register 5 (0x05) – Reserved

Figure 21. Register 5 (0x05) – Reserved

bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
–	–	–	–	–	–	–	–

Table 7. Register 5 (0x05) – Reserved Field Descriptions

Bit	Field	Type	Reset	Description
0-7	–			Reserved

7.5.7 Register 6 (0x06) – Reserved

Figure 22. Register 6 (0x06) – Reserved

bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
–	–	–	–	–	–	–	–

Table 8. Register 6 (0x06) – Reserved Field Descriptions

Bit	Field	Type	Reset	Description
0-7	–			Reserved

7.5.8 Register 7 (0x07) – Amplitude and Rate for Channel 2 (offset = 7h) [reset = 0h]

Figure 23. Register 7 (0x07) – Amplitude and Rate for Channel 2

bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
RATE3	RATE2	RATE1	RATE0	AMP3	AMP2	AMP1	AMP0

Table 9. Register 7 (0x07) – Amplitude and Rate for Channel 2 Field Descriptions

Bit	Field	Type	Reset	Description
7 6 5 4	RATE3 RATE2 RATE1 RATE0	R/W	0h	**Rate adjustments bits for channel 2** 0000 – 21 GHz (default) 0111 – BW decrease of approximately 0.4 GHz 1111 – BW increase of approximately 0.4 GHz
3 2 1 0	AMP3 AMP2 AMP1 AMP0	R/W	0h	**Amplitude adjustment bits for channel 2** 0000 – 0mVpp (default) 1000 – 250mVpp 0001 – 50mVpp 1001 – 300mVpp 0010 – 100mVpp 1010 – 350mVpp 0011 – 150mVpp 1011 – 400mVpp 0100 – 200mVpp 1100 – 450mVpp 0101 – 250mVpp 1101 – 500mVpp 0110 – 300mVpp 1110 – 550mVpp 0111 – 350mVpp 1111 – 600mVpp

7.5.9 Register 8 (0x08) Mapping – Threshold and Gain for Channel 1 (offset = 8h) [reset = 0h]

Figure 24. Register 8 (0x08) – Threshold and Gain for Channel 2

bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
PD	DIS	GAIN1	GAIN0	TH3	TH2	TH1	TH0

Table 10. Register 8 (0x08) – Threshold and Gain for Channel 2

Bit	Field	Type	Reset	Description
7	PD	R/W	0h	**Power down bit for channel 2** 1 = Power down channel 2 0 = Normal operation
6	DIS	R/W	0h	**Disable output buffer for channel 2** 1 = Disable channel 2 output buffer 0 = Normal operation
5 4	GAIN1 GAIN0	R/W	0h	**Gain adjustment bits for channel 2** 00 – default 10 – medium (–4 dB) 01 – NA 11 – minimum (–8 dB)
3 2 1 0	TH3 TH2 TH1 TH0	R/W	0h	**Threshold adjustment bits for channel 2** Minimum positive shift for 0001 Maximum positive shift for 0111 Zero shift for 0000 or 1000 Minimum negative shift for 1001 Maximum negative shift for 1111

7.5.10 Register 9 (0x09) – Reserved

Figure 25. Register 9 (0x09) – Reserved

bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
–	–	–	–	–	–	–	–

Table 11. Register 9 (0x09) – Reserved Field Descriptions

Bit	Field	Type	Reset	Description
0-7	–			Reserved

7.5.11 Register 10 (0x0A) – Reserved

Figure 26. Register 10 (0x0A) – Reserved

bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
–	–	–	–	–	–	–	–

Table 12. Register 10 (0x0A) – Reserved Field Descriptions

Bit	Field	Type	Reset	Description
0-7	–			Reserved

7.5.12 Register 11 (0x0B) – Reserved

Figure 27. Register 11 (0x0B) – Reserved

bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
–	–	–	–	–	–	–	–

Table 13. Register 11 (0x0B) – Reserved Field Descriptions

Bit	Field	Type	Reset	Description
0-7	–			Reserved

7.5.13 Register 12 (0x0C) – Reserved

Figure 28. Register 12 (0x0C) – Reserved

bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
–	–	–	–	–	–	–	–

Table 14. Register 12 (0x0C) – Reserved Field Descriptions

Bit	Field	Type	Reset	Description
0-7	–			Reserved

7.5.14 Register 13 (0x0D) – Amplitude and Rate for Channel 3 (offset = Dh) [reset = 0h]

Figure 29. Register 13 (0x0D) – Amplitude and Rate for Channel 3

bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
RATE3	RATE2	RATE1	RATE0	AMP3	AMP2	AMP1	AMP0

Table 15. Register 13 (0x0D) – Amplitude and Rate for Channel 3 Field Descriptions

Bit	Field	Type	Reset	Description	
7 6 5 4	RATE3 RATE2 RATE1 RATE0	R/W	0h	**Rate adjustments bits for channel 3** 0000 – 21 GHz (default) 0111 – BW decrease of approximately 0.4 GHz 1111 – BW increase of approximately 0.4 GHz	
3 2 1 0	AMP3 AMP2 AMP1 AMP0	R/W	0h	**Amplitude adjustment bits for channel 3**	
				0000 – 0mVpp (default) 0001 – 50mVpp 0010 – 100mVpp 0011 – 150mVpp 0100 – 200mVpp 0101 – 250mVpp 0110 – 300mVpp 0111 – 350mVpp	1000 – 250mVpp 1001 – 300mVpp 1010 – 350mVpp 1011 – 400mVpp 1100 – 450mVpp 1101 – 500mVpp 1110 – 550mVpp 1111 – 600mVpp

7.5.15 Register 14 (0x0E) Mapping – Threshold and Gain for Channel 3 (offset = Eh) [reset = 0h]

Figure 30. Register 14 (0x0E) – Threshold and Gain for Channel 3

bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
PD	DIS	GAIN1	GAIN0	TH3	TH2	TH1	TH0

Table 16. Register 14 (0x0E) – Threshold and Gain for Channel 3

Bit	Field	Type	Reset	Description
7	PD	R/W	0h	**Power down bit for channel 3** 1 = Power down channel 3 0 = Normal operation
6	DIS	R/W	0h	**Disable output buffer for channel 3** 1 = Disable channel 3 output buffer 0 = Normal operation
5 4	GAIN1 GAIN0	R/W	0h	**Gain adjustment bits for channel 3** 00 – default 10 – medium (–4 dB) 01 – NA 11 – minimum (–8 dB)
3 2 1 0	TH3 TH2 TH1 TH0	R/W	0h	**Threshold adjustment bits for channel 3** Minimum positive shift for 0001 Maximum positive shift for 0111 Zero shift for 0000 or 1000 Minimum negative shift for 1001 Maximum negative shift for 1111

7.5.16 Register 15 (0x0F) – Reserved

Figure 31. Register 15 (0x0F) – Reserved

bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
–	–	–	–	–	–	–	–

Table 17. Register 15 (0x0F) – Reserved Field Descriptions

Bit	Field	Type	Reset	Description
0-7	–			Reserved

7.5.17 Register 16 (0x10) – Reserved

Figure 32. Register 16 (0x10) – Reserved

bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
–	–	–	–	–	–	–	–

Table 18. Register 16 (0x10) – Reserved Field Descriptions

Bit	Field	Type	Reset	Description
0-7	–			Reserved

7.5.18 Register 17 (0x11) – Reserved

Figure 33. Register 17 (0x11) – Reserved

bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
–	–	–	–	–	–	–	–

Table 19. Register 17 (0x11) – Reserved Field Descriptions

Bit	Field	Type	Reset	Description
0-7	–			Reserved

7.5.19 Register 18 (0x12) – Reserved

Figure 34. Register 18 (0x12) – Reserved

bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
–	–	–	–	–	–	–	–

Table 20. Register 18 (0x12) – Reserved Field Descriptions

Bit	Field	Type	Reset	Description
0-7	–			Reserved

7.5.20 Register 19 (0x13) – Amplitude and Rate for Channel 4 (offset = 13h) [reset = 0h]

Figure 35. Register 19 (0x13) – Amplitude and Rate for Channel 4

bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
RATE3	RATE2	RATE1	RATE0	AMP3	AMP2	AMP1	AMP0

Table 21. Register 19 (0x13) – Amplitude and Rate for Channel 4 Field Descriptions

Bit	Field	Type	Reset	Description
7 6 5 4	RATE3 RATE2 RATE1 RATE0	R/W	0h	**Rate adjustments bits for channel 4** 0000 – 21 GHz (default) 0111 – BW decrease of approximately 0.4 GHz 1111 – BW increase of approximately 0.4 GHz
3 2 1 0	AMP3 AMP2 AMP1 AMP0	R/W	0h	**Amplitude adjustment bits for channel 4** 0000 – 0mVpp (default) 1000 – 250mVpp 0001 – 50mVpp 1001 – 300mVpp 0010 – 100mVpp 1010 – 350mVpp 0011 – 150mVpp 1011 – 400mVpp 0100 – 200mVpp 1100 – 450mVpp 0101 – 250mVpp 1101 – 500mVpp 0110 – 300mVpp 1110 – 550mVpp 0111 – 350mVpp 1111 – 600mVpp

7.5.21 Register 20 (0x14) Mapping – Threshold and Gain for Channel 4 (offset =14h) [reset = 0h]

Figure 36. Register 20 (0x14) – Threshold and Gain for Channel 4

bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
PD	DIS	GAIN1	GAIN0	TH3	TH2	TH1	TH0

Table 22. Register 20 (0x14) – Threshold and Gain for Channel 4

Bit	Field	Type	Reset	Description
7	PD	R/W	0h	**Power down bit for channel 4** 1 = Power down channel 4 0 = Normal operation
6	DIS	R/W	0h	**Disable output buffer for channel 4** 1 = Disable channel 4 output buffer 0 = Normal operation
5 4	GAIN1 GAIN0	R/W	0h	**Gain adjustment bits for channel 4** 00 – default 10 – medium (–4 dB) 01 – NA 11 – minimum (–8 dB)
3 2 1 0	TH3 TH2 TH1 TH0	R/W	0h	**Threshold adjustment bits for channel 4** Minimum positive shift for 0001 Maximum positive shift for 0111 Zero shift for 0000 or 1000 Minimum negative shift for 1001 Maximum negative shift for 1111

7.5.22 Register 21 (0x15) – Reserved

Figure 37. Register 21 (0x15) – Reserved

bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
–	–	–	–	–	–	–	–

Table 23. Register 21 (0x15) – Reserved Field Descriptions

Bit	Field	Type	Reset	Description
0-7	–			Reserved

7.5.23 Register 22 (0x10) – Reserved

Figure 38. Register 21 (0x10) – Reserved

bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
–	–	–	–	–	–	–	–

Table 24. Register 21 (0x10) – Reserved Field Descriptions

Bit	Field	Type	Reset	Description
0-7	–			Reserved

7.5.24 Register 23 (0x17) – Reserved

Figure 39. Register 23 (0x17) – Reserved

bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
–	–	–	–	–	–	–	–

Table 25. Register 23 (0x17) – Reserved Field Descriptions

Bit	Field	Type	Reset	Description
0-7	–			Reserved

7.5.25 Register 24 (0x18) – Reserved

Figure 40. Register 24 (0x18) – Reserved

bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
–	–	–	–	–	–	–	–

Table 26. Register 24 (0x18) – Reserved Field Descriptions

Bit	Field	Type	Reset	Description
0-7	–			Reserved

7.5.26 Register 25 (0x19) – Reserved

Figure 41. Register 25 (0x19) – Reserved

bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
–	–	–	–	–	–	–	–

Table 27. Register 25 (0x19) – Reserved Field Descriptions

Bit	Field	Type	Reset	Description
0-7	–			Reserved

8 Application and Implementation

8.1 Application Information

Figure 42 shows the ONET2804T being used in a 4 x 25 Gbps fiber optic receiver with pin control and Figure 45 shows the device being used with 2-wire control. The ONET2804T converts the electrical current generated by the PIN photodiode into a differential output voltage. The FILTER inputs provide a DC bias voltage for the PIN that is low pass filtered. Because the voltage drop across the photodiode FET is sensed and used by the bias circuit, the photodiode must be connected to the FILTER pads for the bias to function correctly.

The RSSI outputs are used to mirror the photodiode output current and can be connected via resistors to GND. The voltage gain can be adjusted for the intended application by choosing the external resistor; however, for proper operation of the ONET2804T, ensure that the voltage at RSSI never exceeds V_{CC} - 0.65 V. If the RSSI outputs are not used while operating with internal PD bias they should be left open.

The OUT+ and OUT– pins are internally terminated by 50 Ω pull-up resisters to VCC. The outputs must be AC coupled, for example by using 0.1 µF capacitors, to the succeeding device.

8.2 Typical Applications

8.2.1 Typical Application, Pad Control

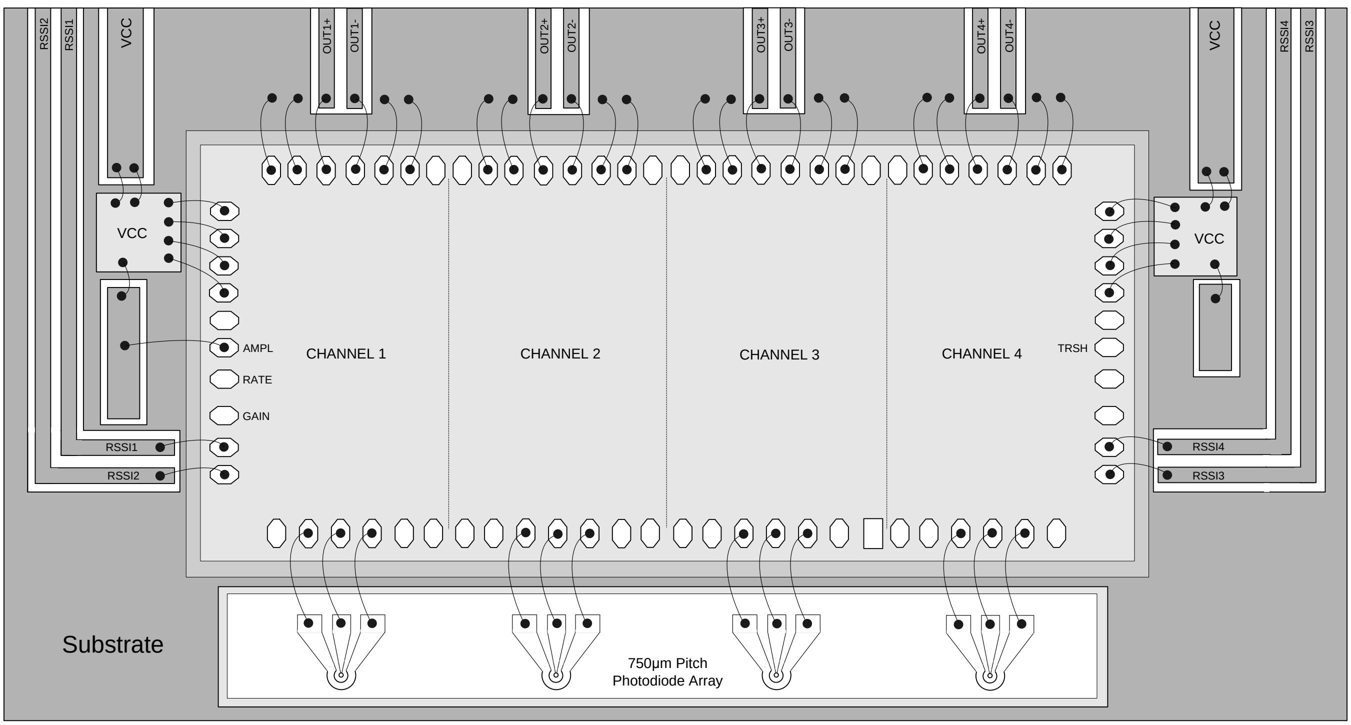


Figure 42. Basic Application Circuit with Pad Control

8.2.1.1 Design Requirements

Table 28. Design Parameters

PARAMETER	VALUE
Input voltage	3.3 V
Output voltage	500 mV_{PP}

8.2.1.2 Detailed Design Procedure

The ONET2804T is designed to be used in conjunction with a 750 μm pitch photodiode array or individual photodiodes and assembled into a receiver optical sub-assembly (ROSA). The TIA will typically be mounted on a ceramic substrate with etched connections for VCC, RSSI and 100 Ω differential transmission lines for the output voltage. The photodiode converts the optical input signal into a current that is supplied to the TIA through wire bonds. The TIA then converts the input current into a voltage and further amplifies the signal. It is recommended to set the output amplitude to the 500 mV_{PP} level by bonding AMPL (pad 6) to VCC.

The ROSA is typically mounted on a printed circuit board (PCB) with 100 Ω differential transmission lines and RF connectors such as GPPO or 2.4 mm SMA. When measuring the output from the ROSA mounted on the PCB, the frequency dependent loss of the transmission lines will impact the frequency response. The loss can be de-embedded from the measurement to determine the actual frequency response at the output of the ROSA. Figure 43 shows a typical frequency response without the loss de-embedded and Figure 44 shows a typical frequency response with the loss de-embedded.

8.2.1.3 Application Curves

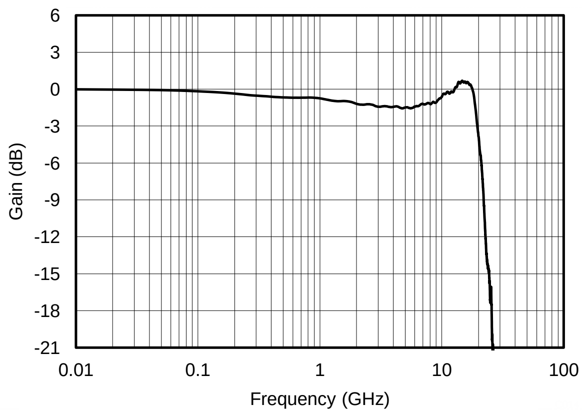


Figure 43. Gain vs Frequency (Without De-embedding)

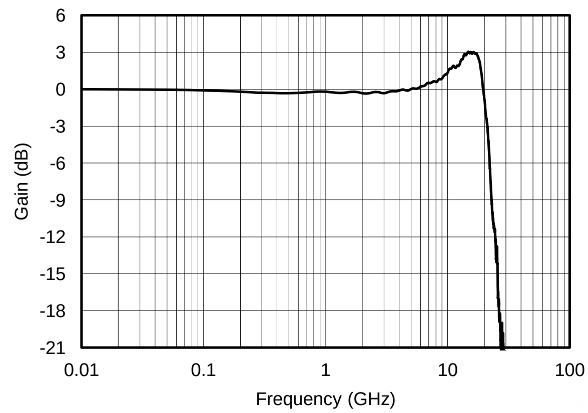


Figure 44. Gain vs Frequency (With De-embedding)

8.2.2 Typical Application, 2-Wire Control

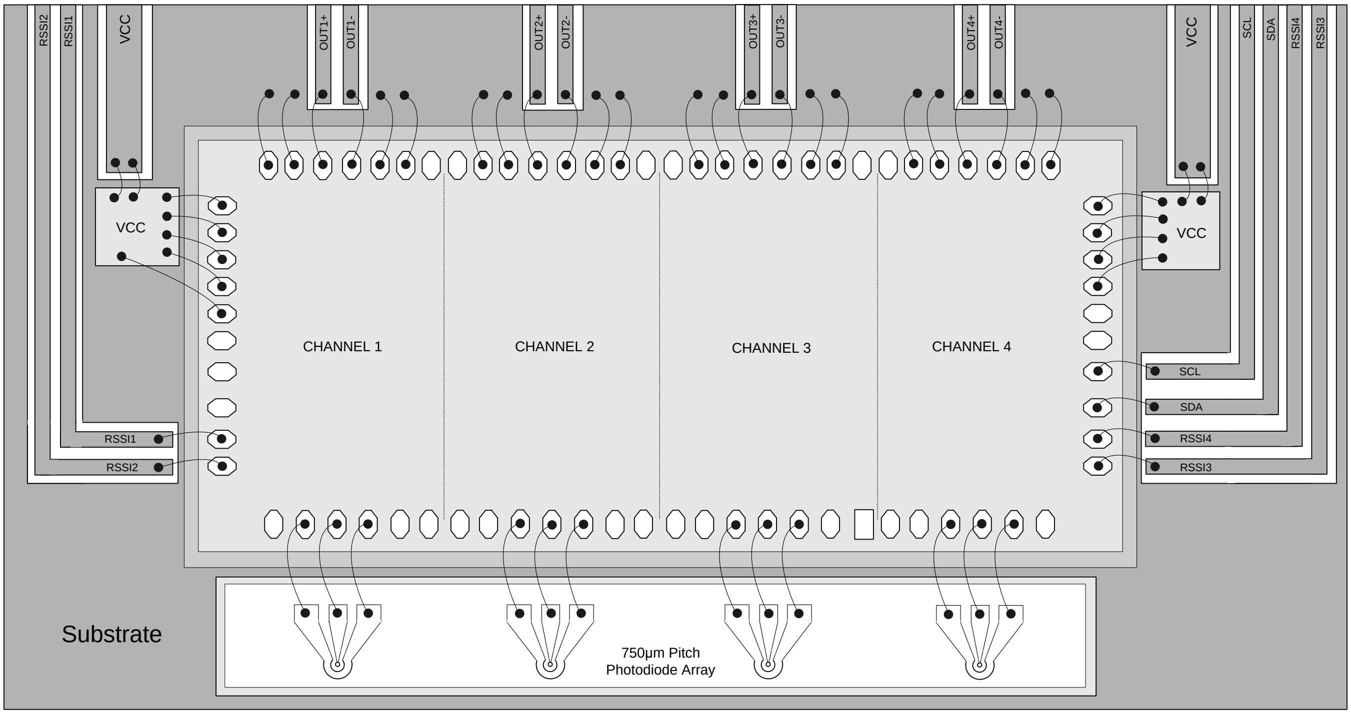


Figure 45. Basic Application Circuit with 2-Wire Control

8.2.2.1 Design Requirements

Refer to *Typical Application, Pad Control* for the Design Requirements.

8.2.2.2 Detailed Design Procedure

Refer to *Typical Application, Pad Control* for the Detailed Design Procedure.

8.2.2.3 Application Curves

Refer to *Typical Application, Pad Control* for the Application Curves.

9 Power Supply Recommendations

The ONET2804T is designed to operate from an input supply voltage range between 2.97 V and 3.47 V. There are a total of 8 power supply pads that must be connected for proper operation. VCCI1-4 are used to supply power to the input transimpedance amplifier stages and VCCO1-4 are used to supply power to the voltage amplifiers and output buffers. Each amplifier is powered up separately but there are some common internal connections for support circuitry such as the 2-wire interface. Therefore, if only one channel is being evaluated, all 8 supply pads must be connected. It is recommended to use two single layer ceramic (SLC) capacitors in the range of 270 pF to 680 pF for power supply decoupling. VCCI1, VCCI2, VCCO1 and VCCO2 should be bonded to one capacitor and VCCI3, VCCI4, VCCO3 and VCCO4 should be bonded to the other capacitor. Refer to Figure 42 and Figure 45 for reference.

10 Layout

10.1 Layout Guidelines

Careful attention to assembly parasitics and external components is necessary to achieve optimal performance.

- Minimize the total capacitance on the IN pad by using a low capacitance photodiode (100fF) and paying attention to stray capacitances. Place the photodiode close to the ONET2804T die and keep the wire bond inductance in the range of 300 to 400pH.
- Use identical termination and symmetrical transmission lines at the AC coupled differential output pins OUT+ and OUT–.
- Use short bond wire connections for the supply terminals VCCIx, VCCOx and GND. Supply voltage filtering is provided on chip but filtering may be improved by using an additional external capacitor.
- The die has backside metal and conductive epoxy must be used to attach the die to ground.

10.2 Layout Example

The IC dimensions are shown in Figure 46, and the pad locations are provided in Table 29. The device is designed for wire bonding not flip chip.

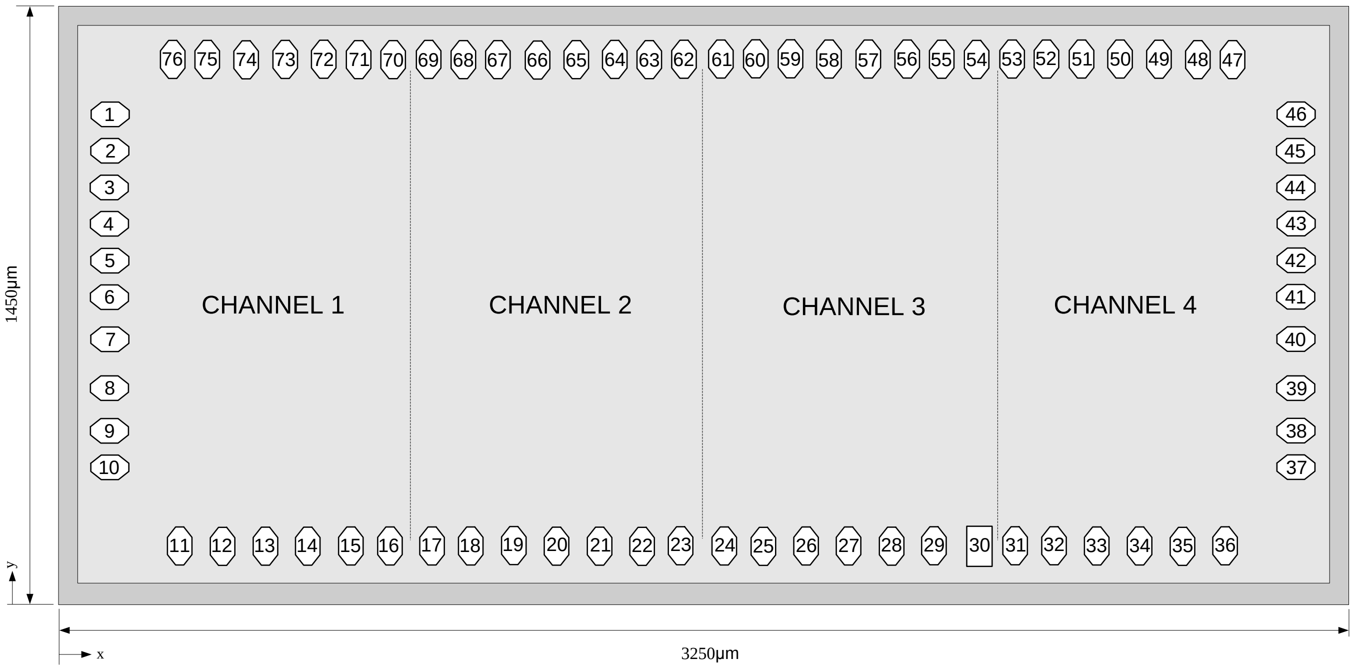


Figure 46. Chip Dimensions and Pad Locations

Die Thickness: 203 ± 13 µm
Pad Dimensions: 105 µm x 65 µm
Die Size: 3250 µm ±40µm x 1450 µm ±40µm

Layout Example (continued)

Table 29. Bond Pad Co-ordinates

PAD	COORDINATES (Referenced to Pad 1)		SYMBOL	TYPE	DESCRIPTION
	x (µm)	y (µm)			
1	0	0	VCCO1	Supply	3.3V supply voltage
2	0	–94	VCCO2	Supply	3.3V supply voltage
3	0	–188	VCCI2	Supply	3.3V supply voltage
4	0	–282	VCCI1	Supply	3.3V supply voltage
5	0	–376	I2CENA	Digital input	I2C Enable
6	0	–470	AMPL	Digital input	Amplitude control
7	0	–580	RATE	Digital input	Rate selection
8	0	–704	GAIN	Digital input	Gain control
9	0	–814	RSSI1	Analog output	Receive signal strength indicator for channel 1
10	0	–908	RSSI2	Analog output	Receive signal strength indicator for channel 2
11	180	–1110	GND	Supply	Circuit ground
12	290	–1110	FILTER1	Analog output	Bias voltage for photodiode 1
13	400	–1110	IN1	Analog input	TIA input for channel 1
14	510	–1110	FILTER1	Analog output	Bias voltage for photodiode 1
15	620	–1110	GND	Supply	Circuit ground
16	720	–1110	NC	No connect	Do not connect
17	829	–1110	NC	No connect	Do not connect
18	929	–1110	GND	Supply	Circuit ground
19	1039	–1110	FILTER2	Analog output	Bias voltage for photodiode 2
20	1149	–1110	IN2	Analog input	TIA input for channel 2
21	1259	–1110	FILTER2	Analog output	Bias voltage for photodiode 2
22	1369	–1110	GND	Supply	Circuit ground
23	1469	–1110	NC	No connect	Do not connect
24	1580	–1110	NC	No connect	Do not connect
25	1680	–1110	GND	Supply	Circuit ground
26	1790	–1110	FILTER3	Analog output	Bias voltage for photodiode 3
27	1900	–1110	IN3	Analog input	TIA input for channel 3
28	2010	–1110	FILTER3	Analog output	Bias voltage for photodiode 3
29	2120	–1110	GND	Supply	Circuit ground
30	2239	–1110	NC	No connect	Do not connect
31	2329	–1110	NC	No connect	Do not connect
32	2429	–1110	GND	Supply	Circuit ground
33	2539	–1110	FILTER4	Analog output	Bias voltage for photodiode 4
34	2649	–1110	IN4	Analog input	TIA input for channel 4
35	2759	–1110	FILTER4	Analog output	Bias voltage for photodiode 4
36	2869	–1110	GND	Supply	Circuit ground
37	3051	–908	RSSI3	Analog output	Receive signal strength indicator for channel 3
38	3051	–814	RSSI4	Analog output	Receive signal strength indicator for channel 4
39	3051	–704	SDA	Digital in/out	2-wire data
40	3051	–579	SCL	Digital input	2-wire clock
41	3051	–470	TRSH	Digital input	Input threshold control (cross-point)
42	3051	–376	NC	No connect	Do not connect
43	3051	–282	VCCI4	Supply	3.3V supply voltage
44	3051	–188	VCCI3	Supply	3.3V supply voltage

Layout Example (continued)

Table 29. Bond Pad Co-ordinates (continued)

PAD	COORDINATES (Referenced to Pad 1)		SYMBOL	TYPE	DESCRIPTION
	x (µm)	y (µm)			
45	3051	–94	VCCO3	Supply	3.3V supply voltage
46	3051	0	VCCO4	Supply	3.3V supply voltage
47	2888	140	GND	Supply	Circuit ground
48	2799	140	GND	Supply	Circuit ground
49	2699	140	OUT4–	Analog output	Inverted data output for channel 4
50	2599	140	OUT4+	Analog output	Non-inverted data output for channel 4
51	2499	140	GND	Supply	Circuit ground
52	2410	140	GND	Supply	Circuit ground
53	2322	140	ADR1	Digital input	2-wire address bit 1 control
54	2228	140	ADR0	Digital input	2-wire address bit 0 control
55	2139	140	GND	Supply	Circuit ground
56	2050	140	GND	Supply	Circuit ground
57	1950	140	OUT3-	Analog output	Inverted data output for channel 3
58	1850	140	OUT3+	Analog output	Non-inverted data output for channel 3
59	1750	140	GND	Supply	Circuit ground
60	1661	140	GND	Supply	Circuit ground
61	1572	140	NC	No connect	Do not connect
62	1477	140	NC	No connect	Do not connect
63	1388	140	GND	Supply	Circuit ground
64	1299	140	GND	Supply	Circuit ground
65	1199	140	OUT2–	Analog output	Inverted data output for channel 2
66	1099	140	OUT2+	Analog output	Non-inverted data output for channel 2
67	999	140	GND	Supply	Circuit ground
68	910	140	GND	Supply	Circuit ground
69	821	140	NC	No connect	Do not connect
70	728	140	NRESET	Digital input	2-wire negative reset
71	639	140	GND	Supply	Circuit ground
72	550	140	GND	Supply	Circuit ground
73	450	140	OUT1–	Analog output	Inverted data output for channel 1
74	350	140	OUT1+	Analog output	Non-inverted data output for channel 1
75	250	140	GND	Supply	Circuit ground
76	161	140	GND	Supply	Circuit ground

11 Device and Documentation Support

11.1 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

11.2 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

11.3 Trademarks

E2E is a trademark of Texas Instruments.
All other trademarks are the property of their respective owners.

11.4 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

11.5 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
ONET2804TY	ACTIVE	DIESALE	Y	0	675	TBD	Call TI	Call TI	-40 to 100		Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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