WINSOURCE ELECTRONICS

THE DATASHEET OF

NCR100W-12LX

NCR100W-12L

SCR

27 June 2016 Product data sheet

1. General description

Planar passivated SCR with sensitive gate in a SOT223 surface mountable plastic package. This SCR is designed to be interfaced directly to microcontrollers, logic integrated circuits and other low power gate trigger circuits.

2. Features and benefits

- Sensitive gate
- Planar passivated for voltage ruggedness and reliability
- Direct triggering from low power drivers and logic ICs
- Surface mountable package

3. Applications

- Ground Fault Circuit Interrupters (GFCI)
- General purpose switching and phase control
- Ignition circuits, CDI for 2- and 3-wheelers
- Motor control - e.g. small kitchen appliances

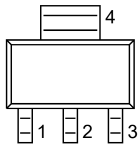
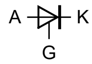
4. Quick reference data

Table 1. Quick reference data

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
V_{DRM}	repetitive peak off-state voltage			-	-	1000	V
V_{RRM}	repetitive peak reverse voltage			-	-	1000	V
$I_{T(AV)}$	average on-state current	half sine wave; $T_{sp} \leq$ 100 °C		-	-	0.8	A
$I_{T(RMS)}$	RMS on-state current	half sine wave; $T_{sp} \leq$ 100 °C; Fig. 1; Fig. 2; Fig. 3		-	-	1.1	A
I_{TSM}	non-repetitive peak on-state current	half sine wave; $T_{j(init)}$ = 25 °C; t_p = 10 ms; Fig. 4; Fig. 5		-	-	11	A
Static characteristics							
I_{GT}	gate trigger current	V_D = 12 V; I_T = 10 mA; T_j = 25 °C; Fig. 7		15	-	50	µA

5. Pinning information

Table 2. Pinning information

Pin	Symbol	Description	Simplified outline	Graphic symbol
1	K	cathode	 SC-73 (SOT223)	 *sym037*
2	A	anode		
3	G	gate		
4	A	mb; connected to anode		

6. Ordering information

Table 3. Ordering information

Type number	Package		
	Name	Description	Version
NCR100W-12L	SC-73	plastic surface-mounted package with increased heatsink; 4 leads	SOT223

7. Marking

Table 4. Marking codes

Type number	Marking code
NCR100W-12L	10012L

8. Limiting values

Table 5. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions		Min	Max	Unit
V_{DRM}	repetitive peak off-state voltage			-	1000	V
V_{RRM}	repetitive peak reverse voltage			-	1000	V
$I_{T(AV)}$	average on-state current	half sine wave; $T_{sp} \leq$ 100 °C		-	0.8	A
$I_{T(RMS)}$	RMS on-state current	half sine wave; $T_{sp} \leq$ 100 °C; Fig. 1; Fig. 2; Fig. 3		-	1.1	A
I_{TSM}	non-repetitive peak on-state current	half sine wave; $T_{j(init)}$ = 25 °C; t_p = 10 ms; Fig. 4; Fig. 5		-	11	A
		half sine wave; $T_{j(init)}$ = 25 °C; t_p = 8.3 ms		-	12.1	A
I^2t	I^2t for fusing	t_p = 10 ms; SIN		-	0.605	A²s
dI_T/dt	rate of rise of on-state current	I_G = 0.1 mA		-	50	A/µs
I_{GM}	peak gate current			-	1	A
V_{RGM}	peak reverse gate voltage			-	5	V
P_{GM}	peak gate power			-	2	W
$P_{G(AV)}$	average gate power	over any 20 ms period		-	0.1	W
T_{stg}	storage temperature			-40	150	°C
T_j	junction temperature			-	125	°C

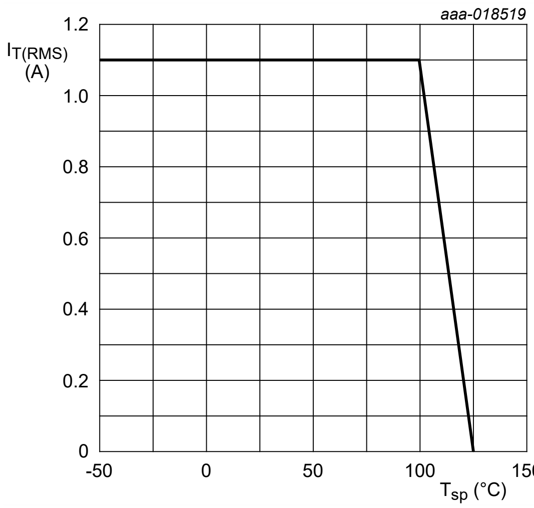
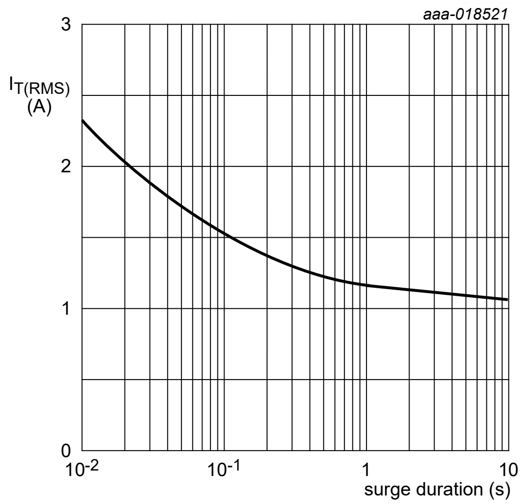
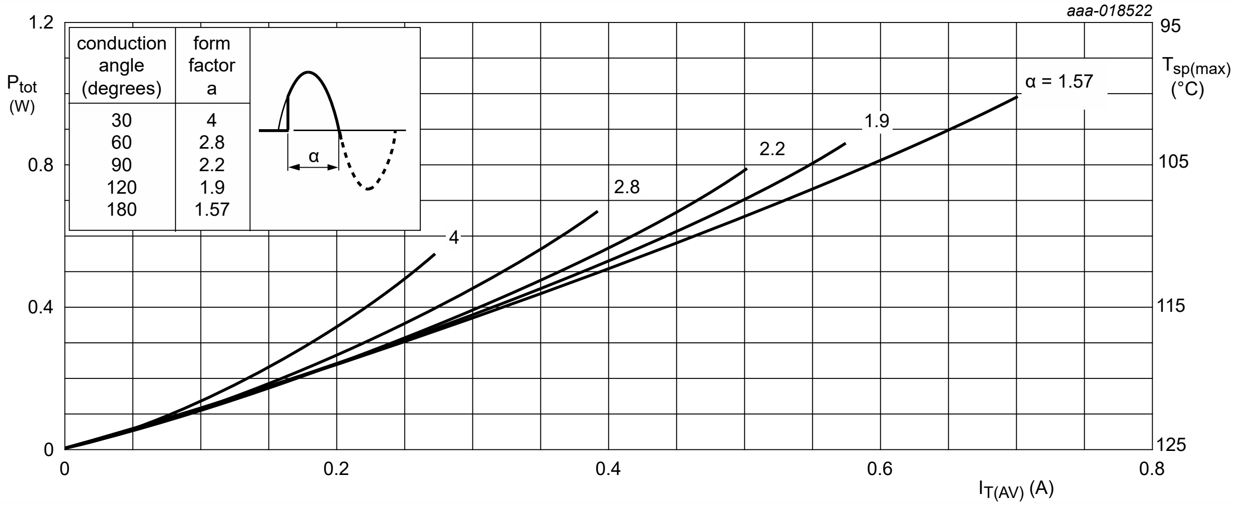


Fig. 1. RMS on-state current as a function of solder point temperature; maximum values



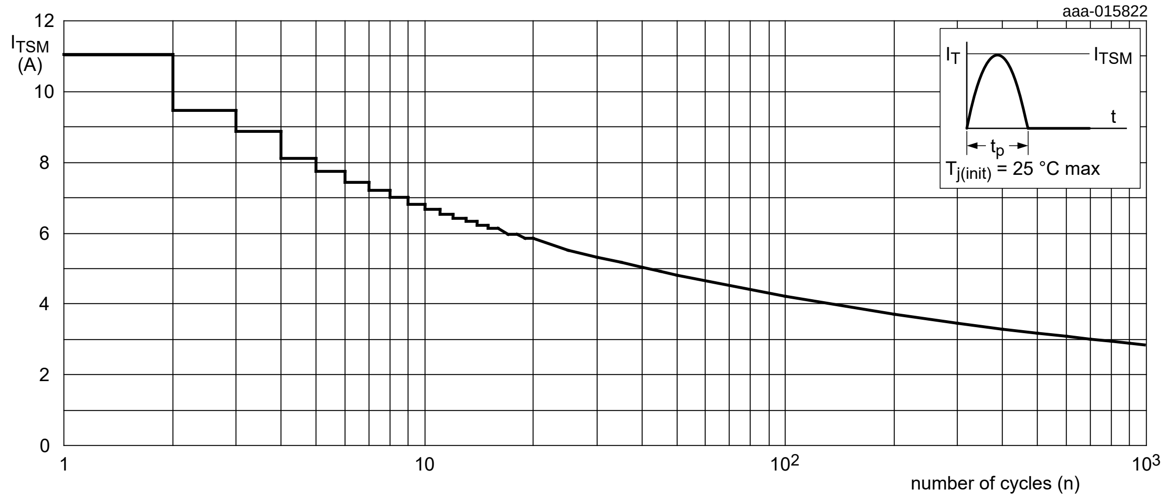
f = 50 Hz; T_{sp} = 100 °C

Fig. 2. RMS on-state current as a function of surge duration; maximum values



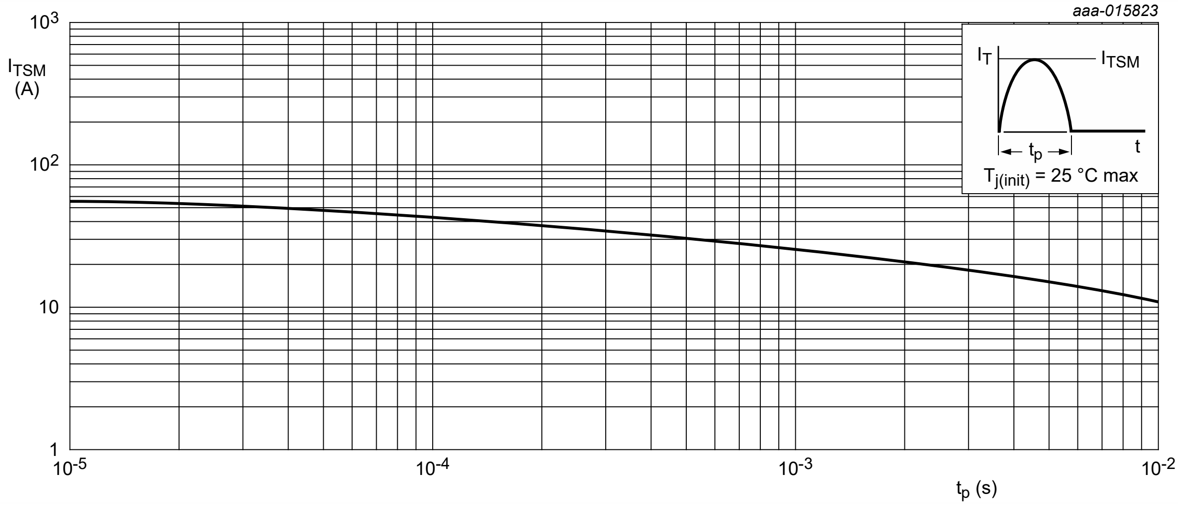
α = conduction angle
a = form factor = $I_{T(RMS)}$ / $I_{T(AV)}$

Fig. 3. Total power dissipation as a function of average on-state current; maximum values



f = 50 Hz

Fig. 4. Non-repetitive peak on-state current as a function of the number of sinusoidal current cycles; maximum values



$t_p \leq 20$ ms

Fig. 5. Non-repetitive peak on-state current as a function of pulse width; maximum values

9. Thermal characteristics

Table 6. Thermal characteristics

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
$R_{th(j-sp)}$	thermal resistance from junction to solder point	half cycle; Fig. 6		-	-	25	K/W
$R_{th(j-a)}$	thermal resistance from junction to ambient free air	printed circuit board mounted; minimum footprint; in free air		-	130	-	K/W

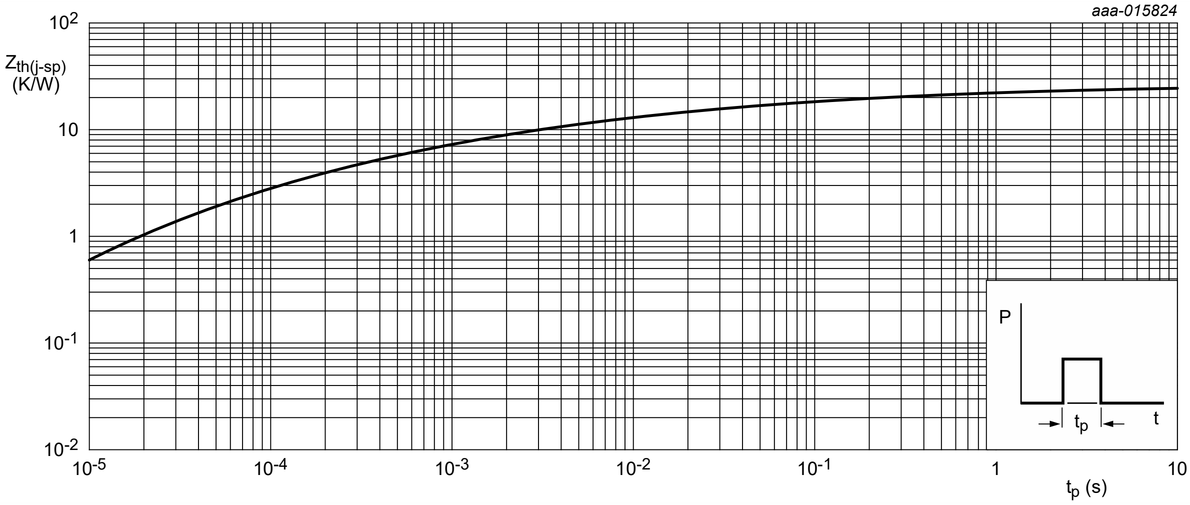


Fig. 6. Transient thermal impedance from junction to solder point as a function of pulse width

10. Characteristics

Table 7. Characteristics

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
Static characteristics							
I_{GT}	gate trigger current	V_D = 12 V; I_T = 10 mA; T_j = 25 °C; Fig. 7		15	-	50	µA
I_L	latching current	V_D = 12 V; I_G = 0.5 mA; T_j = 25 °C; $R_{GK(ext)}$ = 1 kΩ; Fig. 8		-	-	6	mA
I_H	holding current	V_D = 12 V; T_j = 25 °C; $R_{GK(ext)}$ = 1 kΩ; Fig. 9		-	-	3	mA
V_T	on-state voltage	I_T = 1.2 A; T_j = 25 °C; Fig. 10		-	1.25	1.7	V
V_{GT}	gate trigger voltage	V_D = 12 V; I_T = 10 mA; T_j = 25 °C; Fig. 11		-	0.5	0.8	V
		V_D = 1000 V; I_T = 0.1 A; T_j = 125 °C; Fig. 11		0.3	0.5	-	V
I_D	off-state current	V_D = 1000 V; $R_{GK(ext)}$ = 1 kΩ; T_j = 125 °C		-	0.05	1	mA
I_R	reverse current	V_R = 1000 V; T_j = 125 °C; $R_{GK(ext)}$ = 1 kΩ		-	0.05	1	mA
Dynamic characteristics							
dV_D/dt	rate of rise of off-state voltage	V_{DM} = 670 V; T_j = 125 °C; R_{GK} = 1 kΩ; exponential waveform; (V_{DM} = 67% of V_{DRM})		100	-	-	V/µs
t_{gt}	gate-controlled turn-on time	I_{TM} = 2 A; V_D = 1000 V; I_G = 10 mA; dI_G/dt = 0.1 A/µs; T_j = 25 °C		-	2	-	µs
t_q	commutated turn-off time	V_{DM} = 670 V; T_j = 125 °C; I_{TM} = 1.6 A; V_R = 35 V; $(dI_T/dt)_M$ = 30 A/µs; dV_D/dt = 2 V/µs; $R_{GK(ext)}$ = 1 kΩ; (V_{DM} = 67% of V_{DRM})		-	100	-	µs

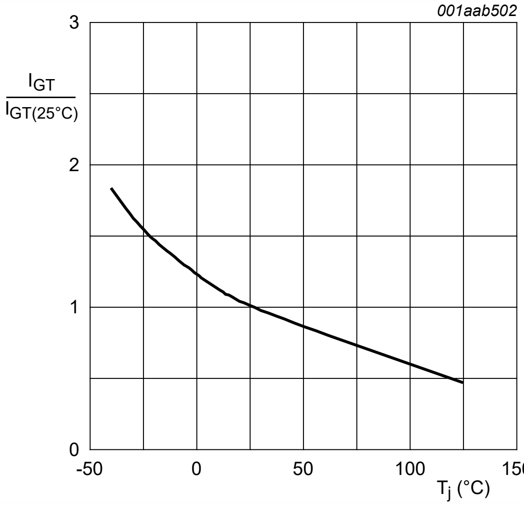
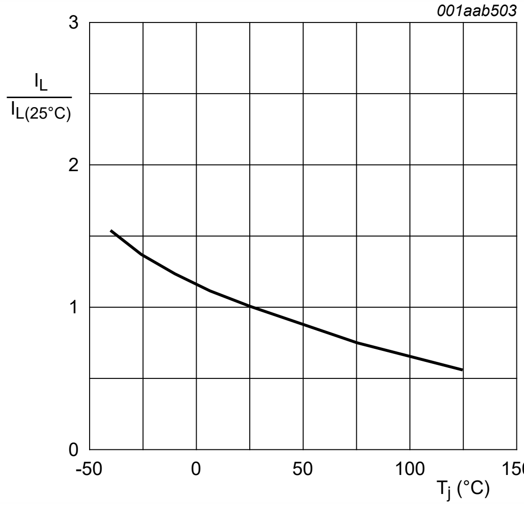
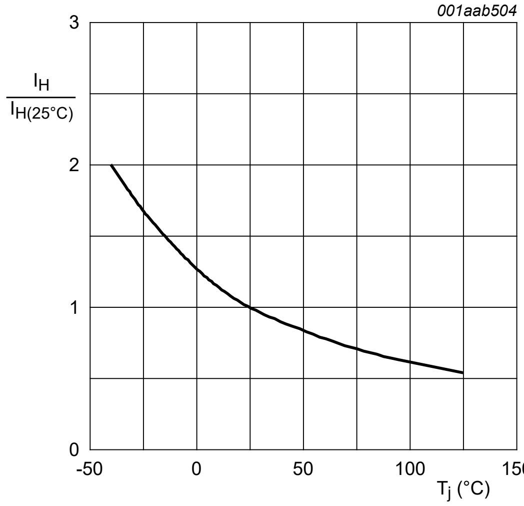


Fig. 7. Normalized gate trigger current as a function of junction temperature



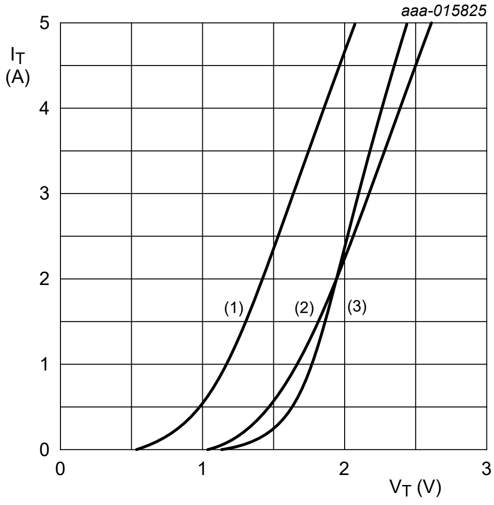
R_{GK} = 1 kΩ

Fig. 8. Normalized latching current as a function of junction temperature



R_{GK} = 1 kΩ

Fig. 9. Normalized holding current as a function of junction temperature



V_o = 1.289 V; R_s = 0.292 Ω

(1) T_j = 125 °C; typical values

(2) T_j = 125 °C; maximum values

(3) T_j = 25 °C; maximum values

Fig. 10. On-state current as a function of on-state voltage

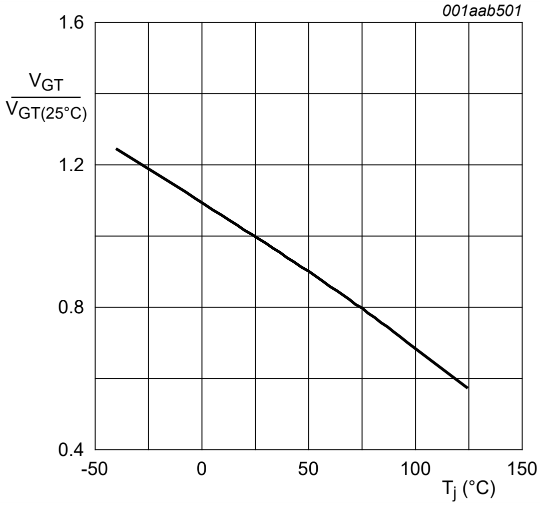
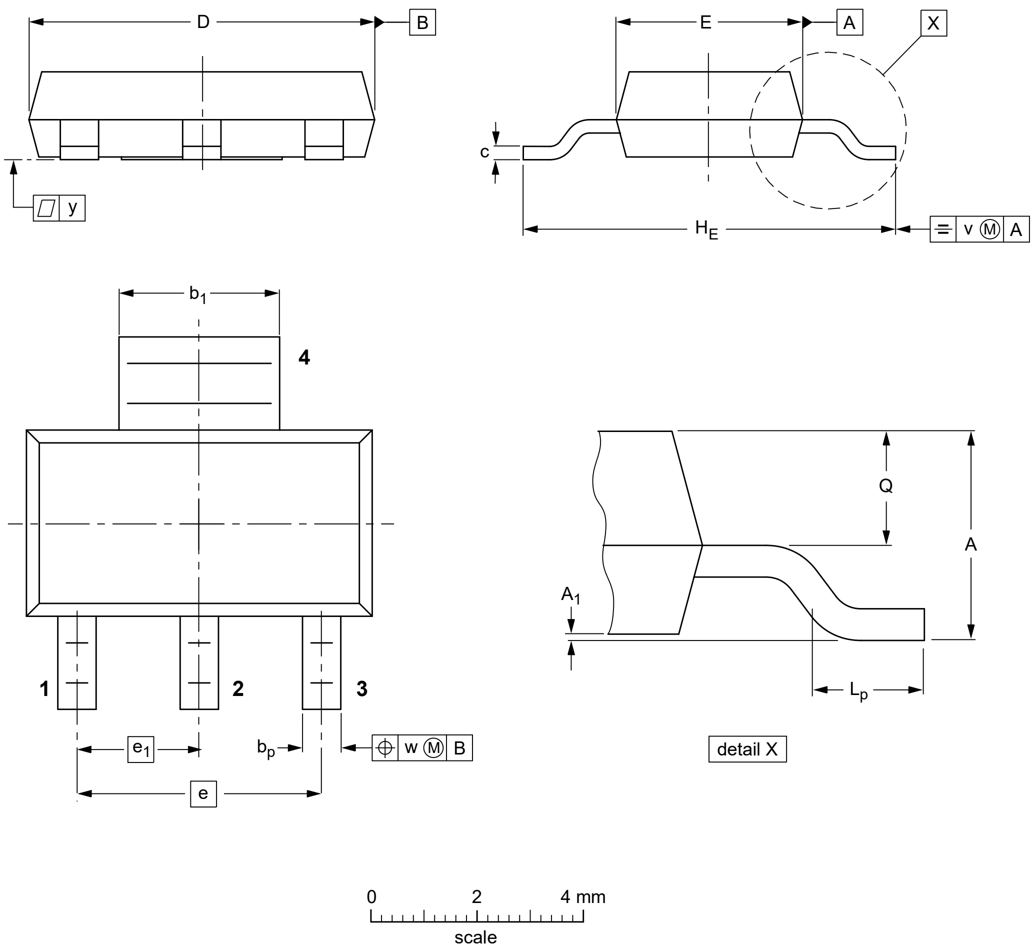


Fig. 11. Normalized gate trigger voltage as a function of junction temperature

11. Package outline

Plastic surface-mounted package with increased heatsink; 4 leads **SOT223**



DIMENSIONS (mm are the original dimensions)

UNIT	A	A_1	b_p	b_1	c	D	E	e	e_1	H_E	L_p	Q	v	w	y
mm	1.8 1.5	0.10 0.01	0.80 0.60	3.1 2.9	0.32 0.22	6.7 6.3	3.7 3.3	4.6	2.3	7.3 6.7	1.1 0.7	0.95 0.85	0.2	0.1	0.1

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT223			SC-73			~~04-11-10~~ 06-03-16

Fig. 12. Package outline SC-73 (SOT223)

12. Package outline (minimized)

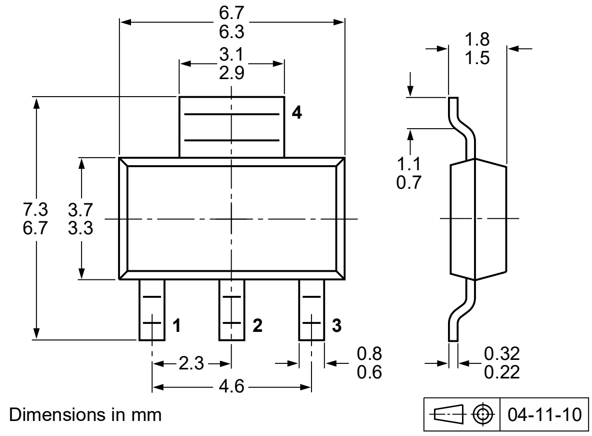


Fig. 13. Package outline SC-73 (SOT223)

13. Soldering

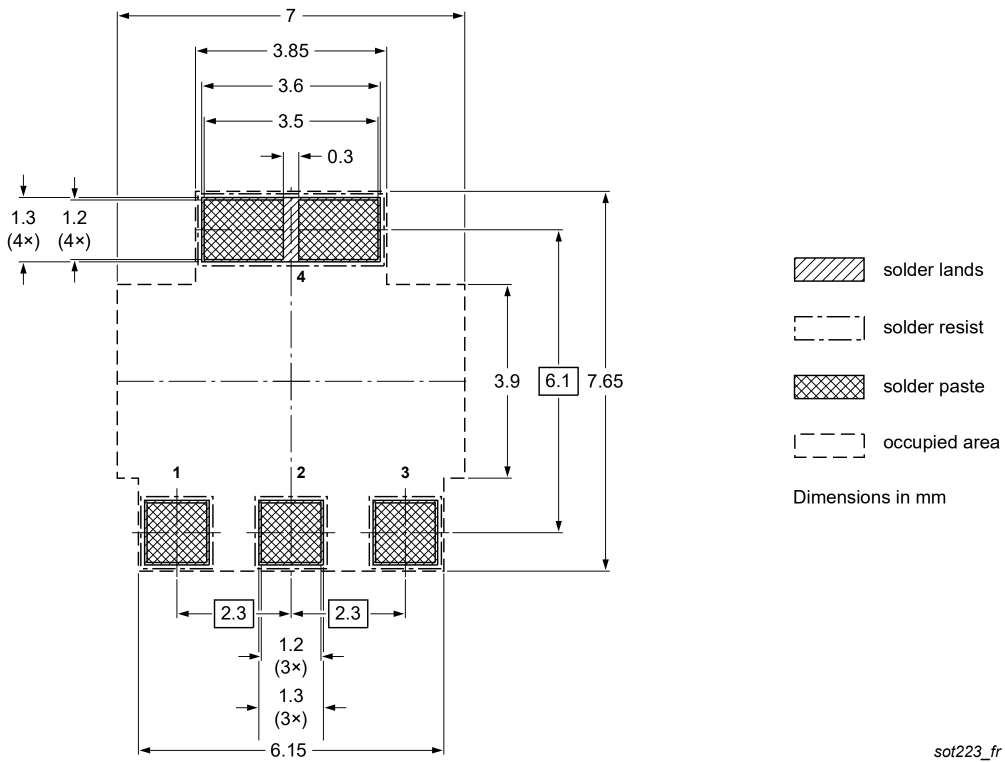


Fig. 14. Reflow soldering footprint for SC-73 (SOT223)

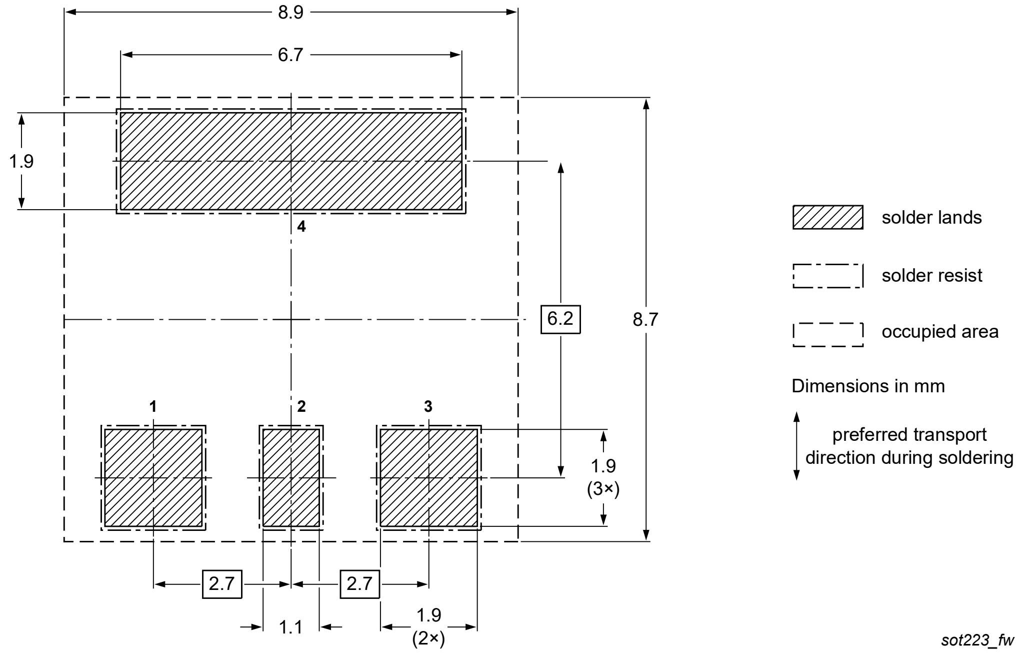


Fig. 15. Wave soldering footprint for SC-73 (SOT223)

14. Legal information

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Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

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[2] The term 'short data sheet' is explained in section "Definitions".
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