THE DATASHEET OF

MX7533JN+

MX7533

CMOS Low Cost 10 Bit Multiplying D/A Converter

General Description

The MX7533 is a low cost CMOS 4-quadrant multiplying digital-to-analog converter (DAC). An advanced silicon gate CMOS process combines 10 bit linearity, low power consumption, and excellent long term stability. Thin-film resistors provide 1.4% untrimmed gain error and less than 0.1% gain change with temperature over all operating ranges.

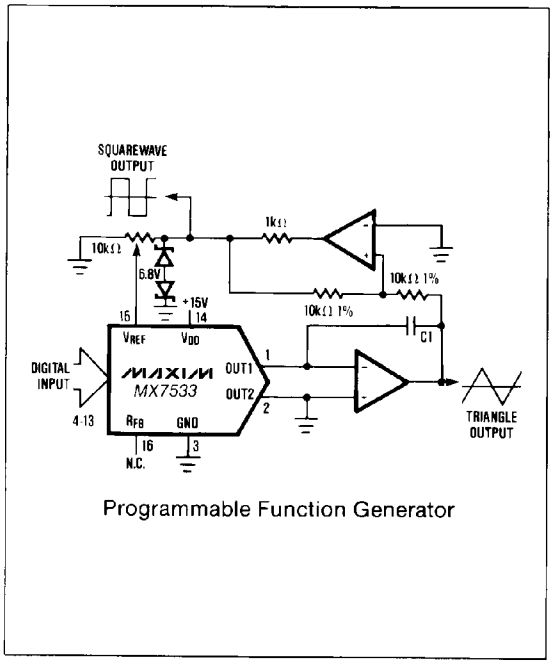
The device operates from a single +5V to +15V supply. All digital inputs are compatible with both CMOS and TTL logic levels.

Maxim's MX7533 is pin and functionally compatible with Analog Devices' AD7533 as well as the AD7520. It is packaged in 16-lead DIP and small outline packages.

Applications

Machine and Motion Control Systems
Automatic Test Equipment
μP Controlled Calibration Circuitry
Programmable Gain Amplifiers
Digitally Controlled Filters
Programmable Power Supplies

Typical Operating Circuit



Programmable Function Generator

Features

- 10 Bit Resolution
- 8, 9, and 10 Bit End Point Linearity
- Low Power Consumption - 20mW
- Four-Quadrant Multiplication
- TTL and CMOS Compatible
- Pin-For-Pin Second Source

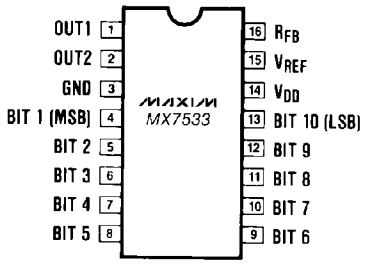
Ordering Information

PART	TEMP. RANGE	PACKAGE*	ERROR
MX7533JN	0°C to +70°C	Plastic DIP	0.2%
MX7533KN	0°C to +70°C	Plastic DIP	0.1%
MX7533LN	0°C to +70°C	Plastic DIP	0.05%
MX7533JCWE	0°C to +70°C	Small Outline	0.2%
MX7533KCWE	0°C to +70°C	Small Outline	0.1%
MX7533LCWE	0°C to +70°C	Small Outline	0.05%
MX7533J/D	0°C to +70°C	Dice	0.2%
MX7533AQ	-25°C to +85°C	CERDIP**	0.2%
MX7533BQ	-25°C to +85°C	CERDIP**	0.1%
MX7533CQ	-25°C to +85°C	CERDIP**	0.05%
MX7533AD	-25°C to +85°C	Ceramic	0.2%
MX7533BD	-25°C to +85°C	Ceramic	0.1%
MX7533CD	-25°C to +85°C	Ceramic	0.05%
MX7533SQ	-55°C to +125°C	CERDIP**	0.2%
MX7533TQ	-55°C to +125°C	CERDIP**	0.1%
MX7533UQ	-55°C to +125°C	CERDIP**	0.05%
MX7533SD	-55°C to +125°C	Ceramic	0.2%
MX7533TD	-55°C to +125°C	Ceramic	0.1%
MX7533UD	-55°C to +125°C	Ceramic	0.05%

* *All devices — 16 lead packages.*
** *Maxim reserves the right to ship Ceramic packages in lieu of CERDIP packages.*

Pin Configuration

Top View



For pricing, delivery, and ordering information, please contact Maxim Direct at 1-888-629-4642, or visit Maxim's website at www.maximintegrated.com.

19-0939; Rev 1a; 7/95

MX7533
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ABSOLUTE MAXIMUM RATINGS

V_{DD} to GND ..... -0.3V, +17V
V_{REF} to GND ..... ±25V
R_{FB} to GND ..... ±25V
Digital Input Voltage to GND ..... -0.3V, V_{DD}
Output Voltage (OUT1, OUT2) (Note 1) ..... -0.3V, V_{DD}
Power Dissipation
  Plastic DIP (Derate 8.3mW/° C above +70° C) 670mW
  Ceramic, CERDIP, Small Outline
    (Derate 6mW/° C above +75° C) 450mW

Operating Temperature Range
  Commercial J/K/L ..... 0° C to +70° C
  Industrial A/B/C ..... -25° C to +85° C
  Military S/T/U ..... -55° C to +125° C
Storage Temperature ..... -65° C to +150° C
Lead Temperature (Soldering 10 secs) ..... +300° C

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(T_A = T_{MIN} to T_{MAX}, V_{DD} = +15V, V_{REF} = +10V, V_{OUT1} = V_{OUT2} = GND, unless otherwise specified)

PARAMETER	SYMBOL	CONDITIONS		MIN.	TYP.	MAX.	UNITS
DC ACCURACY							
Resolution				10			Bits
Relative Accuracy (Note 2)		MX7533J/A/S MX7533K/B/T MX7533L/C/U				±0.2 ±0.1 ±0.05	% FSR
Gain Error (Note 2,3)		Digital Inputs = V_{INH}	T_A = +25°C T_{MIN} to T_{MAX}			±1.4 ±1.5	% FSR
Power Supply Rejection (Note 4) $\Delta Gain/\Delta V_{DD}$	PSRR	V_{DD} = +14V to +17V	T_A = +25°C T_{MIN} to T_{MAX}			0.005 0.008	%/%V_{DD}
Output Leakage Current		OUT1, Digital Inputs = V_{INL}, V_{REF} = ±10V	T_A = +25°C T_{MIN} to T_{MAX}			±50 ±200	nA
		OUT2, Digital Inputs = V_{INH}, V_{REF} = ±10V	T_A = +25°C T_{MIN} to T_{MAX}			±50 ±200	
V_{REF} Input Resistance	R_{REF}	T_A = +25°C		5	10	20	kΩ
V_{REF} Resistance Tempco					-300		ppm/° C
DYNAMIC PERFORMANCE							
Output Current Settling Time (Note 5)		To 0.05% of FSR, R_L = 100Ω, Digital Inputs = V_{INH} to V_{INL} and V_{INL} to V_{INH}.	T_A = +25° C T_{MIN} to T_{MAX}			600 800	ns
Feedthrough Error (Note 4)		Digital Inputs = V_{INL}, V_{REF} = ±10V, 100KHz Sinewave	T_A = +25° C T_{MIN} to T_{MAX}			±0.05 ±0.1	% FSR
Output Capacitance (Note 4)	C_{OUT}	Digital Inputs = V_{INH}	OUT1 OUT2			100 35	pF
		Digital Inputs = V_{INL}	OUT1 OUT2			35 100	
DIGITAL INPUTS							
Logic HIGH Threshold	V_{INH}			+2.4			V
Logic LOW Threshold	V_{INL}					+0.8	V
Input Leakage Current		Digital Inputs = 0V or V_{DD}				±1	μA
Input Capacitance (Note 4)						5	pF
POWER REQUIREMENTS							
Operating Supply Range	V_{DD}	+15V ±10% for Rated Accuracy		+13.5		+16.5	V
		Accuracy Not Guaranteed (Note 4)		+5		+16.5	
Power Supply Current	I_{DD}	Digital Inputs = V_{INH} or V_{INL}				2	mA

Note 1: $V_{OUT1,2}$ may exceed the Absolute Maximum voltage rating if the current is limited to 30mA or less.
Note 2: Using internal feedback resistor (R_{FB}). Full scale range (FSR) = -(V_{REF} - 1LSB) in unipolar mode.
Note 3: Maximum gain change from +25°C to T_{MIN} or T_{MAX} is ±0.1% FSR.
Note 4: Guaranteed by design but not 100% tested.
Note 5: Guaranteed by design and sample tested at +25°C to ensure compliance.

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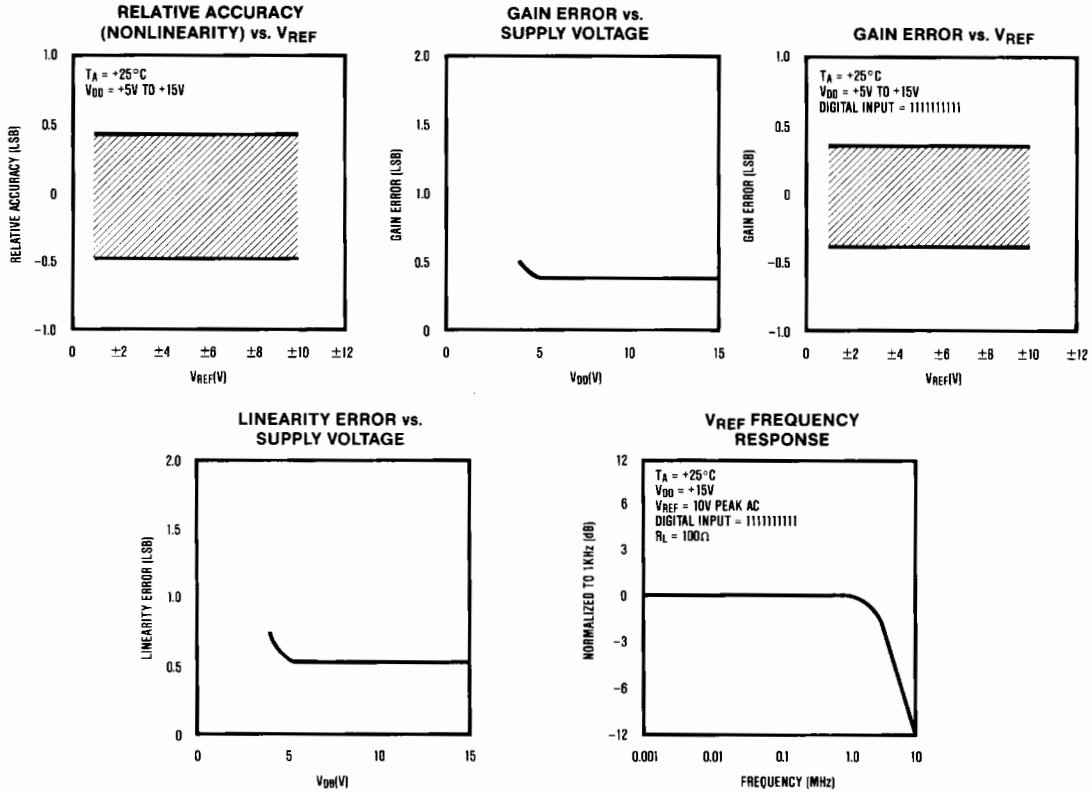
Typical Operating Characteristics



Detailed Description

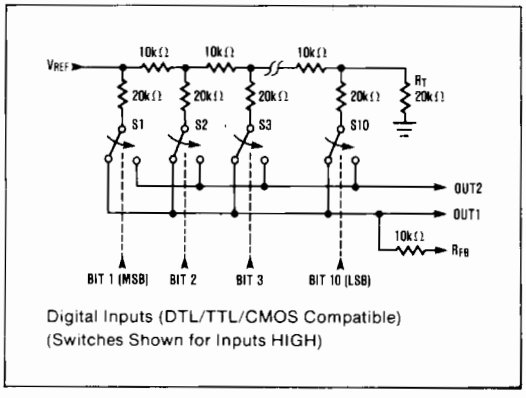


Figure 1. MX7533 Functional Diagram

The basic MX7533 DAC circuit consists of a thin-film R-2R resistor array with CMOS current switches as shown in Figure 1. Binarily weighted currents are switched to either OUT1 or OUT2 depending on the status of each input bit. Most applications require only an output op-amp and an external reference. The V_{REF} input accepts a wide range of reference signals including fixed and time-varying voltage or current inputs.

Equivalent Circuit Analysis

Figures 2 and 3 show the equivalent circuits for the R-2R ladder when all digital inputs are LOW and HIGH respectively. The input resistance at V_{REF} is nominally 10kΩ and does not change with digital input code. The $I_{REF}/1024$ current source, which is actually the ladder termination resistor (R_T, Figure 1), results in an intentional 1-bit current loss to GND. The $I_{LEAKAGE}$ current sources represent junction and surface leakage currents.

Capacitors COUT1 and COUT2 represent the switches' ON and OFF capacitances respectively. When all inputs are switched from LOW to HIGH, the capacitance at OUT1 changes from 35pF to 100pF. This capacitance is code-dependent and is a function of the number of ON switches that are connected to a specific output.

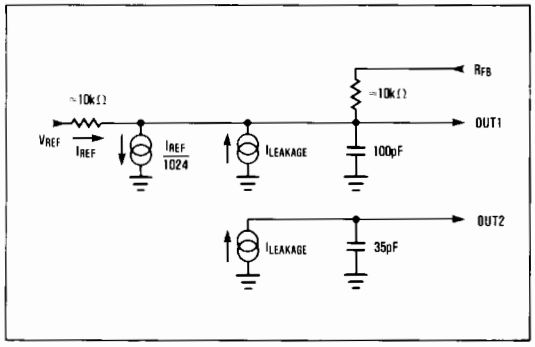


Figure 2. Equivalent DAC Circuit (All digital inputs HIGH)

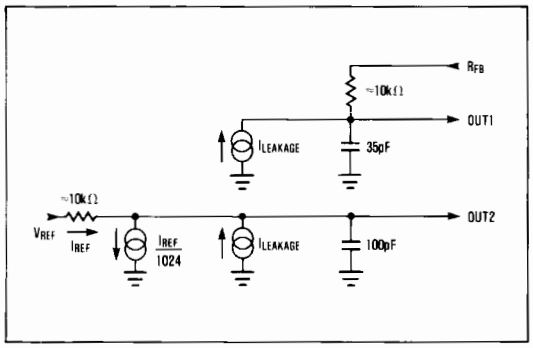


Figure 3. Equivalent DAC Circuit (All digital inputs LOW)

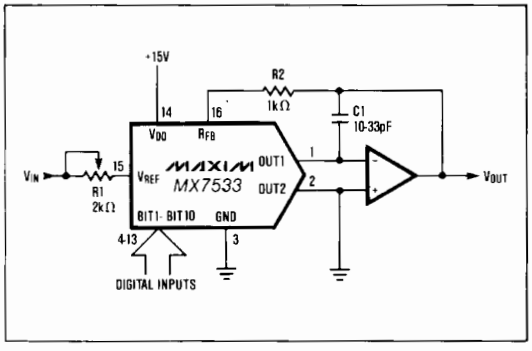


Figure 4. Unipolar Binary Operation (2-Quadrant Multiplication)

Application Information

Unipolar Operation

The most common configuration for the MX7533 is shown in Figure 4. The circuit is used for unipolar binary operation and/or 2-quadrant multiplication. R1 is used for gain adjustment. If no adjustment is desired, R1 and R2 can be omitted. The code table for unipolar operation is given in Table 1. Note that the output polarity is the inverse of the reference input.

A compensation capacitor, C1, may be needed when the DAC is used with a high speed amplifier. The purpose of the capacitor is to cancel the pole formed by the DAC's output capacitance and internal feedback resistance. The correct compensation value depends on the type of op-amp used but typically ranges from 10 to 33pF.

The output op-amp's offset voltage can degrade DAC linearity by causing OUT1 to be terminated at a non-zero voltage. The resulting linearity error is typically $2/3V_{OS}$. For best performance, a low-offset amplifier such as the MAX400 should be used or the amplifier offset must be trimmed to typically more than 1/10 of an LSB's value. The op-amp's input bias current (I_B) can also limit performance since $I_B \times R_{FB}$ generates an offset error as well. I_B should therefore be much less than the DAC's output current for 1 LSB, which is typically 1μA for the MX7533.

Bipolar Operation

Bipolar, or four-quadrant, operation is shown in Figure 5. A second amplifier and three matched resistors are required. R3, R4, and R5 should be matched or trimmed to 0.05% to maintain 10 bit performance. The output vs. code table is listed in Table 2. In multiplying applications, the MSB determines output polarity while the remaining bits control amplitude.

To adjust the circuit, load the DAC with a code of 10000 00000 and trim R1 for a 0V output. With R1 and R2 omitted, an alternative zero trim is to adjust the ratio of R3 and R4 for 0V out. Full scale can be trimmed by loading the DAC with all "zeros" or all "ones" and adjusting the amplitude of V_{REF} or varying R5 until the desired positive or negative output is obtained. The op-amp recommendations made in the Unipolar Operation section apply for bipolar operation as well.

Voltage Mode (Single Supply)

The MX7533 is connected as a voltage output DAC in Figure 6. OUT1 is connected to the external reference and OUT2 is grounded. V_{REF}, now the DAC output, is a voltage source with a constant output resistance of R_{ladder} (nominally 10kΩ). In most circuits this output is buffered with an op-amp.

An advantage of voltage mode operation is single supply operation for the complete circuit, i.e. a negative reference is not required for a positive output. It is important to note that the range of the reference is restricted. The reference input (voltage at OUT1) must

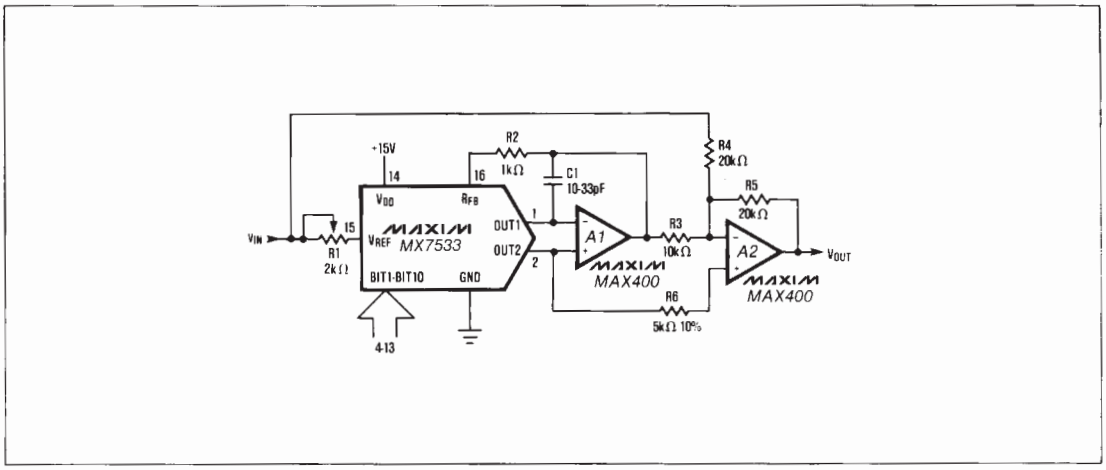


Figure 5. Bipolar Operation (4-Quadrant Multiplication)

always be positive and is limited to no more than 3.5V when V_{DD} is 15V. If the reference voltage is greater than 3.5V, or V_{DD} is reduced, linearity is degraded.

Dynamic Considerations

In static or DC applications, the AC characteristics of the output amplifier are not critical. In higher speed applications, where either the reference input is an AC signal or the DAC output must quickly settle to a new programmed value, the AC parameters of the output op-amp must be considered.

Another error source in dymamic applications is parasitic coupling of signal from the V_{REF} terminal to OUT1 or OUT2. This is normally a function of board layout and package lead-to-lead capacitance. Signals can also be injected into the DAC outputs when the digital inputs are switched. This digital feedthrough is mostly dependent on circuit board layout and on-chip capacitive coupling. Layout induced feedthrough can be minimized with guard traces between digital inputs, V_{REF}, and the DAC outputs.

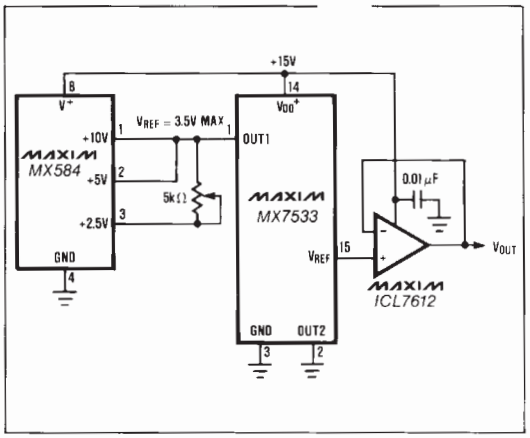


Figure 6. Voltage Mode Operation

Table 1: Code Table — Unipolar Binary Operation

DIGITAL INPUT	ANALOG OUTPUT
1 1 1 1 1 1 1 1 1 1	$-V_{REF}(1 - 2^{-10})$
1 0 0 0 0 0 0 0 0 1	$-V_{REF}(\frac{1}{2} + 2^{-10})$
1 0 0 0 0 0 0 0 0 0	$-V_{REF}/2$
0 1 1 1 1 1 1 1 1 1	$-V_{REF}(\frac{1}{2} - 2^{-10})$
0 0 0 0 0 0 0 0 0 1	$-V_{REF}(2^{-10})$
0 0 0 0 0 0 0 0 0 0	0

Table 2: Code Table — Bipolar (Offset Binary) Operation

DIGITAL INPUT	ANALOG OUTPUT
1 1 1 1 1 1 1 1 1 1	$-V_{REF}(1 - 2^{-9})$
1 0 0 0 0 0 0 0 0 1	$-V_{REF}(2^{-9})$
1 0 0 0 0 0 0 0 0 0	0
0 1 1 1 1 1 1 1 1 1	$V_{REF}(2^{-9})$
0 0 0 0 0 0 0 0 0 1	$V_{REF}(1 - 2^{-9})$
0 0 0 0 0 0 0 0 0 0	V_{REF}

MX7533
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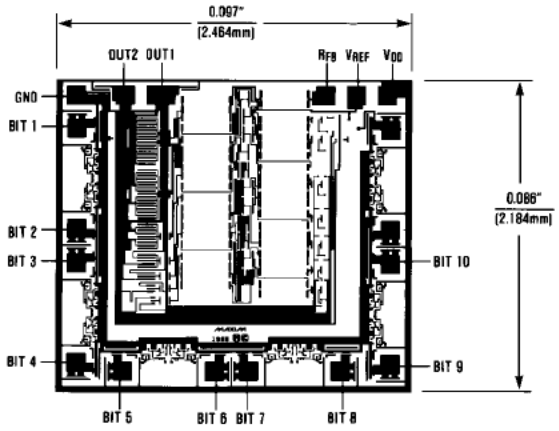
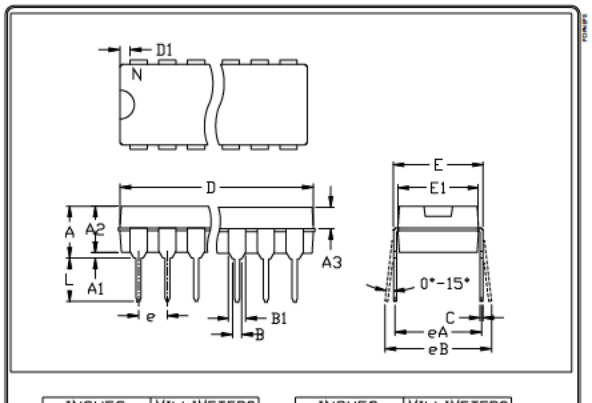
Chip Topography



Package Information



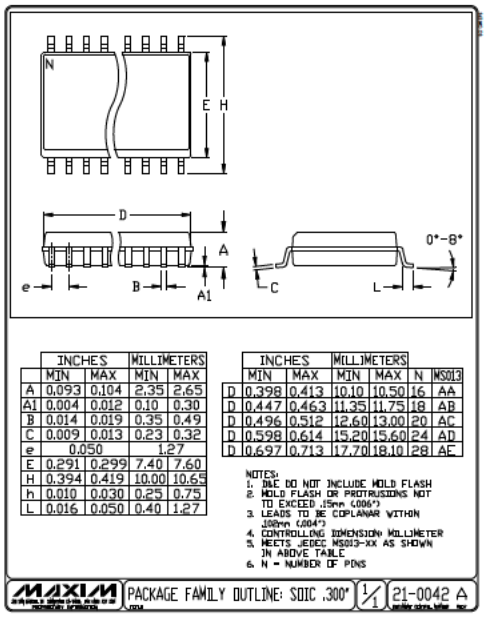
	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	---	0.200	---	5.08
A1	0.015	---	0.38	---
A2	0.125	0.175	3.18	4.45
A3	0.055	0.080	1.40	2.03
B	0.016	0.022	0.41	0.56
B1	0.045	0.065	1.14	1.65
C	0.008	0.012	0.20	0.30
D1	0.005	0.080	0.13	2.03
E	0.300	0.325	7.62	8.26
E1	0.240	0.310	6.10	7.87
e	0.100	---	2.54	---
eA	0.300	---	7.62	---
eB	---	0.400	---	10.16
L	0.115	0.150	2.92	3.81

	INCHES		MILLIMETERS			
	MIN	MAX	MIN	MAX	N	MS001
D	0.348	0.390	8.84	9.91	8	AB
D	0.735	0.765	18.67	19.43	14	AC
D	0.745	0.765	18.92	19.43	16	AA
D	0.885	0.915	22.48	23.24	18	AD
D	1.015	1.045	25.78	26.54	20	AE
D	1.14	1.265	28.96	32.13	24	AF
D	1.360	1.380	34.54	35.05	28	✱5

NOTES:
1. D&E DO NOT INCLUDE MOLD FLASH
2. MOLD FLASH OR PROTRUSIONS NOT TO EXCEED .15mm (.006")
3. CONTROLLING DIMENSION: MILLIMETER
4. MEETS JEDEC MS001-XX AS SHOWN IN ABOVE TABLE
5. SIMILIAR TO JEDEC MO-058AB
6. N = NUMBER OF PINS

MAXIM | PACKAGE FAMILY OUTLINE: PDIP .300" | 1/1 | 21-0043 A

Package Information (continued)

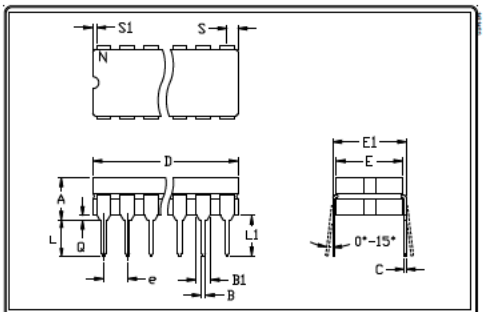


	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.093	0.104	2.35	2.65
A1	0.004	0.012	0.10	0.30
B	0.014	0.019	0.35	0.49
C	0.009	0.013	0.23	0.32
e	0.050		1.27	
E	0.291	0.299	7.40	7.60
H	0.394	0.419	10.00	10.65
h	0.010	0.030	0.25	0.75
L	0.016	0.050	0.40	1.27

	INCHES		MILLIMETERS			
	MIN	MAX	MIN	MAX	N	MS013
D	0.398	0.413	10.10	10.50	16	AA
D	0.447	0.463	11.35	11.75	18	AB
D	0.496	0.512	12.60	13.00	20	AC
D	0.598	0.614	15.20	15.60	24	AD
D	0.697	0.713	17.70	18.10	28	AE

NOTES:
1. DIE DO NOT INCLUDE MOLD FLASH
2. MOLD FLASH OR PROTRUSIONS NOT TO EXCEED .15mm (.006")
3. LEADS TO BE COPLANAR WITHIN .102mm (.004")
4. CONTROLLING DIMENSION: MILLIMETER
5. MEETS JEDEC MS013-XX AS SHOWN IN ABOVE TABLE
6. N = NUMBER OF PINS

MAXIM | PACKAGE FAMILY OUTLINE: SOIC .300" | 1/1 | 21-0042 A



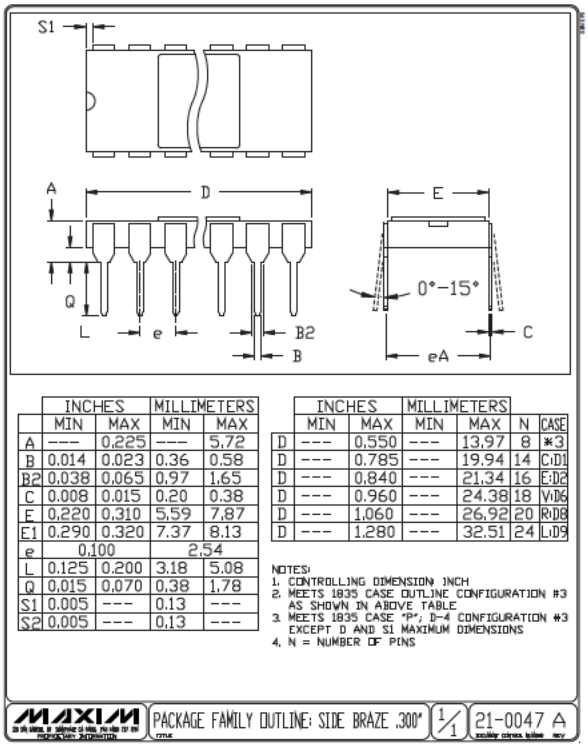
	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	---	0.200	---	5.08
B	0.014	0.023	0.36	0.58
B1	0.038	0.065	0.97	1.65
C	0.008	0.015	0.20	0.38
E	0.220	0.310	5.59	7.87
E1	0.290	0.320	7.37	8.13
e	0.100		2.54	
L	0.125	0.200	3.18	5.08
L1	0.150	---	0.00	---
Q	0.015	0.070	0.38	1.78
S	---	0.098	---	2.49
S1	0.005	---	0.13	---

	INCHES		MILLIMETERS			
	MIN	MAX	MIN	MAX	N	CASE
D	---	0.405	---	10.29	8	P:04
D	---	0.785	---	19.94	14	C:01
D	---	0.840	---	21.34	16	E:02
D	---	0.960	---	24.38	18	V:06
D	---	1.060	---	26.92	20	R:08
D	---	1.280	---	32.51	24	L:09

NOTES:
1. CONTROLLING DIMENSION: INCH
2. MEETS JEDEC CASE OUTLINE CONFIGURATION #1 AS SHOWN IN ABOVE TABLE
3. N = NUMBER OF PINS

MAXIM | PACKAGE FAMILY OUTLINE: CDIP .300" | 1/1 | 21-0045 A

Package Information (continued)



	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	---	0.225	---	5.72
B	0.014	0.023	0.36	0.58
B2	0.038	0.065	0.97	1.65
C	0.008	0.015	0.20	0.38
E	0.220	0.310	5.59	7.87
E1	0.290	0.320	7.37	8.13
e	0.100		2.54	
L	0.125	0.200	3.18	5.08
Q	0.015	0.070	0.38	1.78
S1	0.005	---	0.13	---
S2	0.005	---	0.13	---

	INCHES		MILLIMETERS			
	MIN	MAX	MIN	MAX	N	CASE
D	---	0.550	---	13.97	8	*3
D	---	0.785	---	19.94	14	C-D1
D	---	0.840	---	21.34	16	E-D2
D	---	0.960	---	24.38	18	V-D6
D	---	1.060	---	26.92	20	R-D8
D	---	1.280	---	32.51	24	L-D9

NOTES:
1. CONTROLLING DIMENSION INCH
2. MEETS 1835 CASE OUTLINE CONFIGURATION #3 AS SHOWN IN ABOVE TABLE
3. MEETS 1835 CASE "P"; D-4 CONFIGURATION #3 EXCEPT D AND S1 MAXIMUM DIMENSIONS
4. N = NUMBER OF PINS

MAXIM | PACKAGE FAMILY OUTLINE: SIDE BRAZE .300" | 1/1 | 21-0047 A

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