THE DATASHEET OF

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MPC8544E PowerQUICC III Processor

Overview

The MPC8544E PowerQUICC III processor offers the unique combination of high performance, exceptional integration and lower overall power consumption for networking, communications and industrial control applications.

The MPC8544E includes a high-performance e500 processor core, built on Power Architecture® technology, enhanced peripherals and high-speed interconnect technology to balance processor performance with I/O system throughput, enabling clock speeds scaling from 667 MHz up to 1.067 GHz.

Third-generation PowerQUICC III processors are based on Freescale's 90 nm silicon-on-insulator (SOI) copper interconnect process technology, which is designed to enable the processors to deliver higher performance with lower power dissipation. The predecessors of the MPC8544E—the MPC8548E family—were one of the first generation of PowerQUICC III processors to use this core set of technology. These 90 nm processors are designed to deliver a significant performance increase over 130 nm PowerQUICC devices, providing a higher level of performance and exceptional integration to the PowerQUICC family.

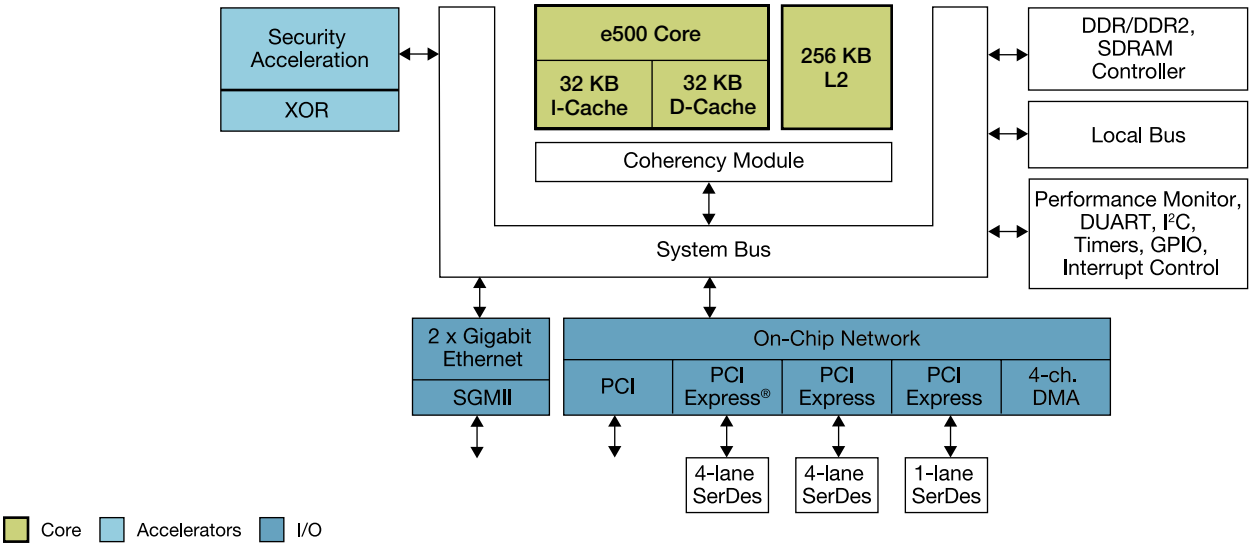
The MPC8544E processor offers a wide range of high-speed connectivity options, including Gigabit Ethernet (GbE) interfaces with SGMII support and multiple PCI Express® connections. Support for these high-speed interfaces enables scalable connectivity to network processors and/or ASICs in the data plane while the PowerQUICC III is designed to handle complex, computationally demanding control plane processing tasks.

The MPC8544E is also designed to provide support for legacy PowerQUICC III interfaces such as PCI, I²C, dual universal asynchronous receiver/transmitters (DUART) and local bus connections. These processors feature a DDR2 memory controller, enhanced GbE support, v2 e500 double precision floating point and the field-proven 90 nm PowerQUICC III integrated security engine.

Key Advantages

- High level of integration and performance
- Consistent programming model across the PowerQUICC III family
- Flexible SoC platform for fast time to market
- Simplified board design
- 256 KB L2 cache memory
- High internal processing bandwidth
- Integrated DDR and DDR2 memory controller
- Two integrated Ethernet controllers (enhanced TSEC) with SGMII support
- Flexible, high-speed interconnection interfaces/multiple PCI Express connections
- 32-bit PCI support
- Integrated security engine

MPC8544E Block Diagram



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MPC8544E Technical Specifications

- Embedded e500 core, initial offerings from 667 MHz up to 1.067 GHz
  - Dual dispatch superscalar, seven-stage pipeline design with out-of-order issue and execution
  - 2,240 MIPS at 1.0 GHz (estimated Dhrystone 2.1)
  - 36-bit physical addressing
- Enhanced hardware and software debug support
- Double-precision embedded scalar and vector floating point APUs
- Memory management unit (MMU)
- Integrated L1/L2 cache
  - L1 cache—32 KB data and 32 KB instruction cache with line-locking support
  - L2 cache—256 KB (8-way set associative) 256/128/64/32 KB can be used as SRAM
  - L1 and L2 hardware coherency
  - L2 cache and I/O transactions can be stashed into L2 cache regions
- Integrated DDR memory controller with full ECC support, offering:
  - 200 MHz clock rate (400 MHz data rate), 64-bit, 2.5V/2.6V I/O, DDR SDRAM
  - 267 MHz clock rate (up to 533 MHz data rate), 64-bit, 1.8V I/O, DDR2 SDRAM
- Integrated security engine supporting DES, 3DES, MD-5, SHA-1/2, AES, RSA, RNG, Kasumi F8/F9 and ARC-4 encryption algorithms (MPC8544E)
- Two on-chip, three-speed Ethernet controllers (eTSECs) supporting 10 Mbps, 100 Mbps and 1 Gbps Ethernet/IEEE® 802.3 networks with MII, RMII, GMII, RGMII TBI and RTBI physical interfaces, as well as SGMII interfaces through a dedicated SerDes
  - TCP/UDP/IP checksum acceleration
  - Advanced QoS features
- General-purpose input/output (GPIO)
- PCI Express high-speed interconnect interfaces, supporting combinations of dual x4 and single x1 PCI Express
- On-chip network (OCeaN) switch fabric
- PCI interface support
  - 32-bit PCI 2.2 bus controller (up to 66 MHz, 3.3V I/O)
- Local bus
  - 133 MHz, 32-bit, 3.3V I/O, local bus with memory controller
- Integrated four-channel DMA controller
- Dual I^2C and DUART support
- Programmable interrupt controller (PIC)
- IEEE 1149.1 JTAG test access port
- 1.0V core voltage with 3.3V and 2.5V I/O
- 783-pin FC-PBGA package
- Operating junction temperature range: T_J = 0°C to +105°C, extended temperature range: T_J = -40°C to +105°C

Development System

The MPCEVAL-DS-8544 development system includes Linux® 2.6.19 + BSP with optimized drivers to support all peripherals and a limited CodeWarrior development tools evaluation license.

Learn More: For current information about Freescale products and documentation, please visit **freescale.com/PowerQUICC**.

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