THE DATASHEET OF

MP8005DF-LF-Z

MP8005

13W 802.3af PoE Powered Device (PD) Interface and PWM Controller

The Future of Analog IC Technology

DESCRIPTION

The MP8005 is a complete integrated IEEE 802.3af POE compliant Powered Device (PD) power supply solution. It includes the PD control function and an isolated/non isolated synchronous regulator controller. Thermal protection is built in to accommodate both transient and/or overload conditions, shutting the part down and protecting the input source as well as the output load depending on the particular fault conditions. Inrush current limiting is included to slowly charge the input capacitor without interruption due to die heating, a problem encountered without the current limit foldback feature. The desired output voltage is user programmable through the selection of an external resistor divider.

FEATURES

- Meets IEEE 802.3af Specifications
- 100V, 1Ω Integrated switch
- 460mA max, Temperature Compensated Current Limit
- Isolated Synchronous Controller
- 20 pin TSSOP Package

APPLICATIONS

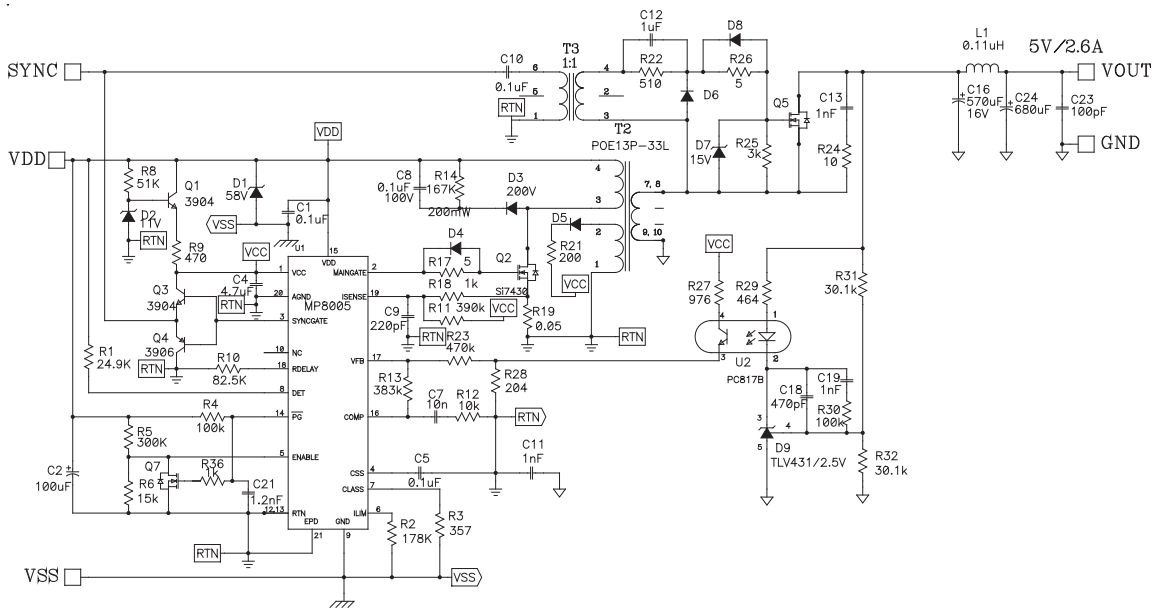
- VoIP Telephones
- Network Cards
- Security Camera Systems
- Safety Backup Power
- Remote Internet Power

All MPS parts are lead-free and adhere to the RoHS directive. For MPS green status, please visit MPS website under Quality Assurance. "MPS" and "The Future of Analog IC Technology" are Registered Trademarks of Monolithic Power Systems, Inc.

EVALUATION BOARD REFERENCE

Board Number	Dimensions
EV8005DF-00A	5.33"x1.75"x0.8" (LxWxH)

TYPICAL ISOLATED APPLICATION

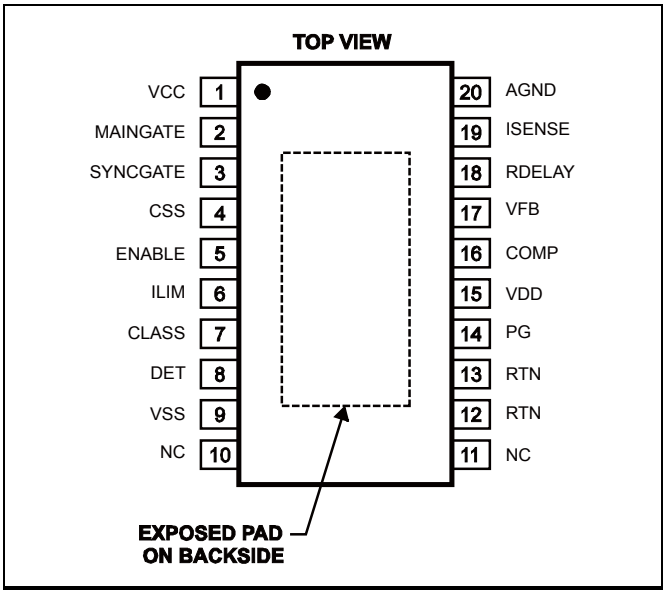


ORDERING INFORMATION

Part Number*	Package	Top Marking	Temperature
MP8005DF	TSSOP-20-EP	MP8005DF	–40°C to +85°C

For Tape & Reel, add suffix –Z (e.g. MP8005DF–Z).
For Lead Free, add suffix –LF (e.g. MP8005DF–LF–Z)

PACKAGE REFERENCE



ABSOLUTE MAXIMUM RATINGS (1)

V_{DD}, RTN.....–0.3V to +100V
PG, DET .....–0.3V to +57V
V_{CC}, CLASS .....–0.3V to +10V
I_{LIM}, CSS, ENABLE. .....–0.3V to +5V
I_{SENSE}. .....–0.3V to +28V
COMP. .....–0.3V to +3V
FB . .....–0.3V to +1.3V
Continuous Power Dissipation (T_A = +25°C) (2)
. ..... 1.2W
Junction Temperature.....150°C
Lead Temperature .....260°C
Storage Temperature..... –65°C to +150°C

Recommended Operating Conditions (3)

Supply Voltage V_{DD} .....0V to 57V
Output Current I_{OUT} ..... 0 to 0.4A
Junction Temperature T_J..... –40°C to +125°C

Thermal Resistance (4)

	θ_{JA}	θ_{JC}	
TSSOP-20-EP	105	50	°C/W

Notes:

1) Exceeding "Absolute Maximum Ratings" may cause permanent damage to the device. Functional operation at or above these conditions is not implied
Exposure to these conditions for extended periods may affect device reliability.
2) The maximum allowable power dissipation is a function of the maximum junction temperature. T_J(MAX) the junction-to-ambient thermal resistance. θ_{JA} and the ambient temperature, T_A the maximum allowable power dissipation at any ambient temperature is calculated using: $P_D(MAX)=(T_J(MAX)-T_A)/\theta_{JA}$. Exceeding the maximum allowable power dissipation will cause excessive die temperature, and the regulator will go into thermal shutdown. Internal thermal shutdown circuitry protects the device from permanent damage.
3) The device is not guaranteed to function outside of its operating conditions.
4) Measured on JESD51-7, 4-layer PCB.

ELECTRICAL CHARACTERISTICS

V_{DD} = 48V, all voltages with respect to V_{SS}, V_{SS} = 0V; R_{DET} = 26.1kΩ, R_{CLASS} = 4.42KΩ, R_{ILIM} = 178kΩ, T_A = 25°C, unless otherwise noted.

Parameters	Symbol	Condition	Min	Typ	Max	Units
VCC Undervoltage Lockout		Internal Divider (I_Q)		4.5	4.7	V
VCC On/Off Voltage Hysteresis				1		V
Shutdown Current	I_S	EN/SS =0V, V_{IN}=9V		50		µA
Quiescent Current	I_Q	Output not switching, no load, V_{FB}=1V, V_{CC}=9V		270	320	µA
Main Gate Driver Impedance (Sourcing)		V_{CC}=9V, V_{GATE}=5V		16		Ω
Main Gate Driver Impedance (Sinking)		V_{CC}=9V, I_{GATE}=5mA		5.0		Ω
Synchronous Gate Driver Impedance (Sourcing)		V_{CC}=9V, $V_{SYNCGATE}$=5V		16		Ω
Synchronous Gate Driver Impedance (Sinking)		V_{CC}=9V, I_{GATE}=5mA		5.0		Ω
Delay after Synchronous Gate		R_{DELAY}=100KΩ		50		ns
Error Amplifier Transconductance		V_{FB} connected to $V_{COMP/RUN}$. Force ± ± 10µA to $V_{COMP/RUN}$.	0.26	0.38	0.46	mA/V
Maximum comp Current		Sourcing and Sinking		40		µA
Error Amplifier Translator Gain (5)	A_{ET}		0.28	0.32	0.36	V/V
Switching Frequency	f_S		220	260	300	kHz
Thermal Shutdown				150		°C
Maximum Duty Cycle			76	81	86	%
Minimum On Time	t_{ON}			200		ns
ISENSE Limit			165	190	215	mV
FB Voltage	V_{FB}		0.794	0.818	0.847	V
FB Bias Current	I_{FB}	Current flowing out of part		50		nA
ISENSE Bias Current	I_{SENSE}	Current flowing out of part		50		nA
Enable On Threshold	V_{EN}	High-to-Low	1.15	1.25	1.35	V
Enable Hystersis	V_{EN}			50		mA
Soft Start Current	I_{SS}			4		µA

ELECTRICAL CHARACTERISTICS (*continued*)

V_{DD} = 48V, all voltages with respect to V_{SS}, V_{SS} = 0V; R_{DET} = 26.1kΩ, R_{CLASS} = 4.42KΩ, R_{ILIM} = 178kΩ, T_A = 25°C, unless otherwise noted.

Parameter	Symbol	Condition		Min	Typ	Max	Units
Detection							
Detection on	V_{DET_ON}	V_{DD}=V_{RTN}=V_{PG}=1.9V			1.9		V
Detection off	V_{DET_OFF}	V_{DD}=V_{RTN}=V_{PG}=11V			11		V
Detection on/off Hysteresis	V_{DET_H}	Falling below 11V on Threshold			0.2		V
DET Leakage Current	**V_{DET_LK}**	**V_{DET}=V_{VDD}=57V, Measure IDET**			**0.1**	**5**	**µA**
Detection Current	I_{DET}	V_{VDD}=V_{RTN} R_{DET}=26.1kΩ, Measure I_{VDD}+I_{RTN}+I_{DET}	V_{DD}= 3V	135	140	145	µA
			V_{DD}= 10.1V	405	420	435	µA
Classification							
V_{CLASS} Output Voltage	V_{CL}	Over a Load Range of 1mA to 41.2 mA		9.6	10	10.3	V
Classification Current	I_{CLASS}	R_{CLASS}=4420Ω, 13≤V_{VDD}≤21V (guar by V_{CL})		2.2.	2.4	2.8	mA
		R_{CLASS}=953Ω, 13≤V_{VDD}≤21V (guar by V_{CL})		10.3	10.6	11.3	
		R_{CLASS}=549Ω, 13≤V_{VDD}≤21V (guar by V_{CL})		17.7	18.3	19.5	
		R_{CLASS}=357Ω, 13≤V_{VDD}≤21V (guar by V_{CL})		27.1	28	29.5	
		R_{CLASS}=255Ω, 13≤V_{VDD}≤21V (guar by V_{CL})		38	39.4	41.2	
Classification Lower Threshold	V_{CL_ON}	Regulator Turns on, V_{VDD} Rising		10.2	11.3	13	V
Classification Upper Threshold	V_{CU_OFF}	Regulator Turns off, V_{VDD} Rising		21	21.9	23	V
	V_{CU_H}	Hysteresis			0.4		V
IC Supply Current during Classification	I_{IN_CLASS}	V_{DD} = 17.5V, CLASS Floating, RTN Tied to VSS			300	500	µA
Leakage Current	$I_{LEAKAGE}$	V_{CLASS} = 0 V, V_{VDD} = 57V				1	µA
Pass Device							
On Resistance	$R_{DS(ON)}$	I_{RTN}=300mA			1.0	1.2	Ω
Leakage Current	I_{SW_LK}	V_{VDD}=V_{RTN}=57V			1	15	µA
Current Limit	I_{LIMIT}	V_{RTN}=1V		360	400	460	mA
Inrush Limit	I_{INRUSH}	V_{RTN}=2V, R_{ILM}=178kΩ		120	150	180	mA
Inrush Current Termination		V_{RTN} Falling, R_{IPEAK} = 178kΩ, Inrush State→Normal Operation		85	90	100	%

ELECTRICAL CHARACTERISTICS (*continued*)

V_{DD} = 48V, all voltages with respect to V_{SS}, V_{SS} = 0V; R_{DET} = 26.1kΩ, R_{CLASS} = 4.42KΩ, R_{ILIM} = 178kΩ, T_A = 25°C, unless otherwise noted.

Parameter	Symbol	Condition	Min	Typ	Max	Units
PG						
Latchoff Voltage Threshold Rising		V_{RTN} Rising (5)	9.5	10	10.5	V
Latchoff Voltage Threshold Falling		V_{RTN} Falling		1.2		V
PG Deglitch		Delay Rising and Falling PDG (5)	75	150	225	µs
Output Low Voltage		I_{PG} = 400 µA		0.12	0.4	V
Leakage Current		V_{PG} = 57 V, V_{RTN} = 0 V		0.1	1	µA
UVLO						
Voltage at V_{VDD}		V_{VDD} Rising (including 1.4V Diode drop)	38	40	42	V
		V_{VDD} Falling (including 1.4V Diode drop)	30.2	31.5	32.8	
Thermal Shutdown						
Thermal Counter Reset Voltage	VCRST	Must Drop below Classification Range		10.8		V
Bias Current						
Operating Current	I_Q (VDD)	VDD = 48V, Pins 5, 6 Floating Measure IVDD		240	450	µA

Notes:

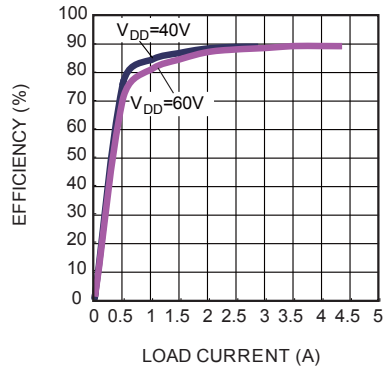
5) Guaranteed by Design.

PIN FUNCTIONS

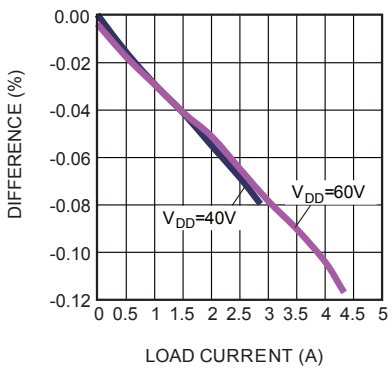
Pin #	Name	Description
1	VCC	10V Shunt Supply Voltage used for the switching regulator controller
2	MAINGATE	Output drive to the Main Gate
3	SYNCGATE	Output drive to the Synchronous Gate
4	CSS	Soft-start ramping capacitor
5	ENABLE	On/Off control input to the switching regulator
6	ILIM	Startup I_{LIM} Value Setting Resistor terminal (optional at this point).
7	CLASS	Classification Resistor terminal.
8	DET	26.1kΩ Detection Resistor terminal
9	VSS	Ground return to the Ethernet negative supply.
10		No Connection
11		No Connection
12	RTN	Powered Device Negative Power Terminal.
13	RTN	Powered Device Negative Power Terminal.
14	PG	Active low power good indication.
15	VDD	Positive Power Supply Terminal for the Ethernet PD control function.
16	COMP	Switching regulator compensation terminal.
17	VFB	Switching regulator voltage feedback terminal.
18	RDELAY	Resistor programming for setting the delay from the Sync gate going low to the Main gate going high.
19	ISENSE	Main Switch current sensing terminal.
20	AGND	Switching regulator controller ground return; Returns to the RTN pin.

TYPICAL PERFORMANCE CHARACTERISTICS

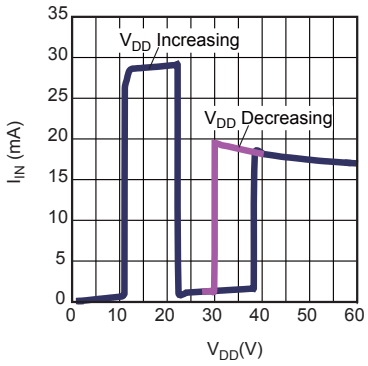
Efficiency vs. Load Current



Output Voltage vs. Load Current

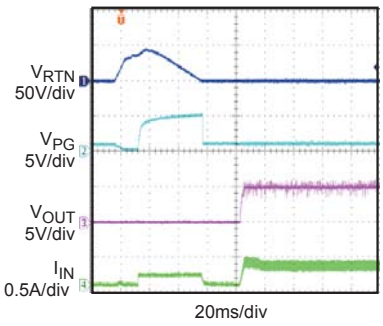


V_{CC} Regulator Line Regulation



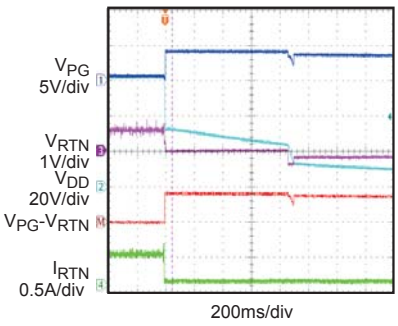
Start Up

V_{DD}=48V, I_{LOAD}=2.6A



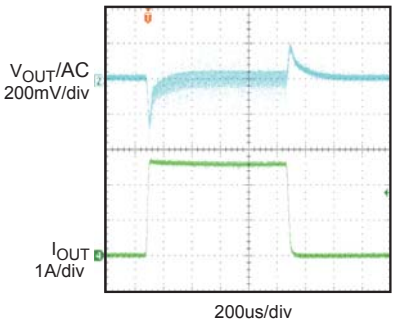
Shut Down

V_{DD}=48V, I_{LOAD}



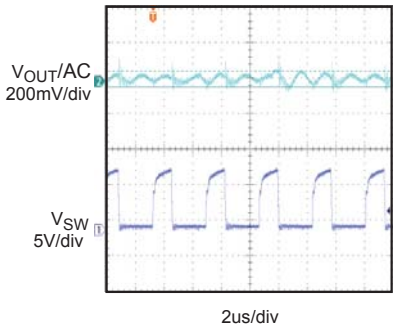
Transient Response

V_{DD}=48V, I_{LOAD}=2.6A, 0 to 2.6A
Load Slew:1.0A/1uS



Output Ripple

V_{DD}=60V, I_{LOAD}=4A



BLOCK DIAGRAM

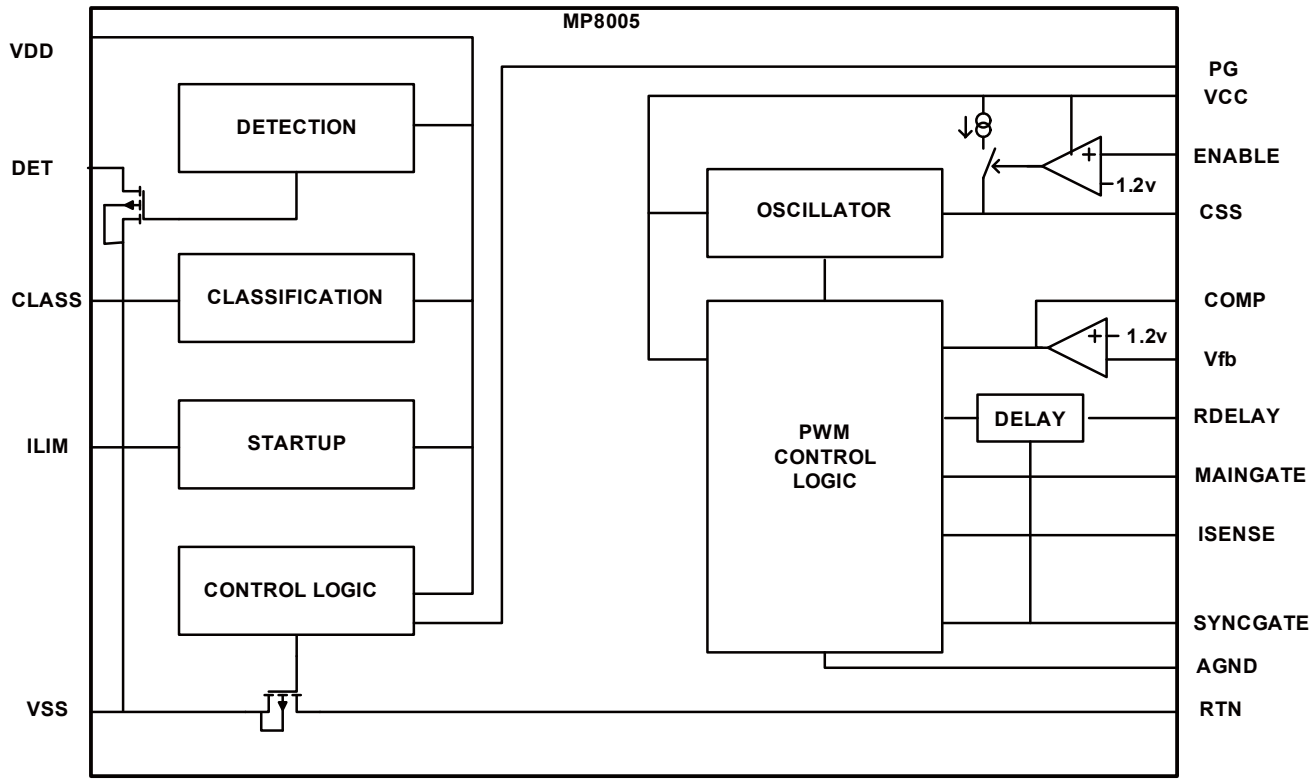


Figure 1— Block Diagram

OPERATION

The MP8005 operates in the manner described here and in the IEEE 802.3af Powered Device (PD) Specification. This device (along with the power sourcing element (PSE)) operates as a safety device to supply potentially lethal voltages only when the power sourcing element recognizes a unique, tightly specified resistance at the end of an unknown length of Ethernet cable.

A 25kΩ resistance is presented as a load to the PSE in Detection Mode, when the PSE applies two “safe” voltages of less than 10.1V each while measuring the change in current drawn in order to determine the load resistance. If the PSE “sees” the correct load, then it may either further increase the applied voltage to enter the “classification” range of operation or switch on the nominal 48V power to the load.

The classification mode can further specify to the PSE the expected load range of the device under power so that the PSE can intelligently distribute power to as many loads as possible (within its maximum current capabilities). If a classification resistance is not present, the PD load is assumed to be the maximum of approximately 13 Watts. The classification mode is active between 14.5V and 20.5V.

The main power switch will pass a limited current above 31V, charging the external DC-to-DC converter’s input capacitor in a controlled manner. The charging will continue until the controlled current drops below either an externally programmed limiting level or 450mA, depending upon the Rlim current setting resistor. The main power switch is internally thermally protected to 100V by reducing the output current using a foldback technique. The required power dissipation of the IC drops from the allowed peak value of 26W (450mA x 57V) to 0.16W ($(450mA)^2$ x R_{ON}) during the normal operation at turn-on. The minimum allowed capacitance of 5µF will charge in 500µs. A larger capacitor will take a proportionally longer time to charge due to the constant current charging method. A capacitor that is too large will overheat the part and force it into thermal shutdown. The IC will reattempt charging for a number of cycles but ultimately will be shut down until the input voltage from the PSE is recycled. This is the way the IC protects itself under overload and/or shorted conditions.

Once the capacitor tied between Vdd, Ethernet input positive supply and the RTN pin is charged to within a volt of the applied Ethernet input supply potential, the PG output is driven low to enable the switching regulator controller. This delay prior to turning on the switching regulator is required in order to minimize the power dissipation incurred during the startup of the controller. The capacitance tied across the Vdd and RTN lines provide the inductor ripple current while maintaining a small voltage differential such that the average current flowing in the RTN line is under the current limit level. Without a storage capacitance at this point, instantaneous current peaks, required by the switching regulator during normal operation, would send the main PD switch (at the RTN pin) in and out of current limit resulting in high power dissipation due to the resultant voltage across the “switch”. A current greater than the current limit value would increase the voltage on the RTN pin to the Ehternet Input supply voltage immediately resulting in power dissipation levels that would immediately shut down the PD switch without the required storage capacitor.

The soft-start capacitor, CSS, slows the rate of current delivery to the switching regulator to a value that can be delivered by the storage capacitor/PD switch.

A resistor tied between the Rdelay pin and AGND sets a time delay between the falling edge of the synchronous gate and the rising edge of the main gate. This delay can be set to compensate for system delays caused by architectural structures of the circuit being used. An isolated secondary type power supply having a transformer in the feedback loop may require extra time due to the electrical path incurred. The delay time is adjustable from as little as 40nSec to over 200nSec through the choice of resistance value. A smaller resistance will result in a shorter delay. Nominal values range from 0 - 200 kΩ for time delays from 40nSec to 200nSec. The delay

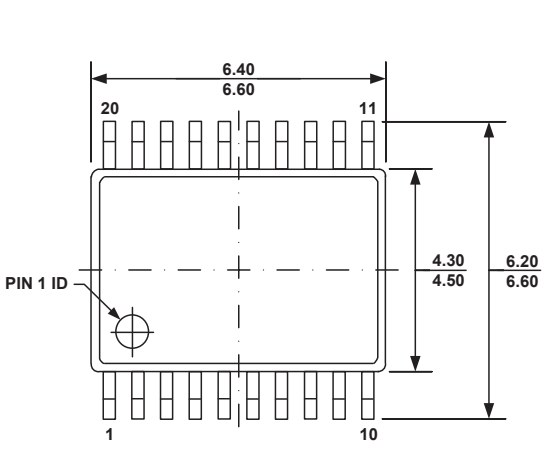
is very important in that it prevents cross conduction of the switching MOSFETS that either severely reduces efficiency or even worse, a switching MOSFET failure.

The output drive levels of the main and synchronous gate are in the hundreds of mA through a 0 to 10V voltage potential. A “normal” threshold MOSFET (Vth typ. 3.5V) having low gate charge (less than 10 nano-Coulombs @ 10V drive) is recommended.

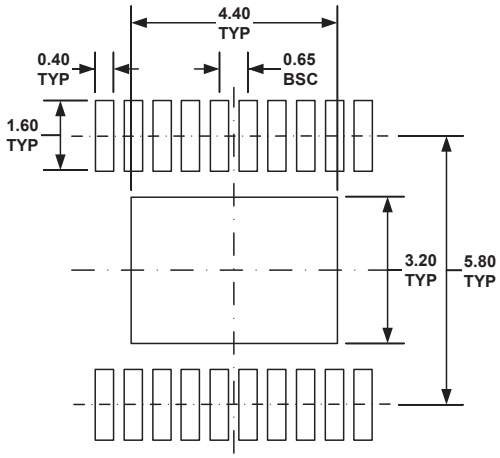
The nominal range of the ISENSE pin is set to a maximum of 200mV but should be designed such that 100mV across the sense resistor provides the maximum current that is expected for the nominal load. This will provide enough “headroom” for typical applications.

PACKAGE INFORMATION

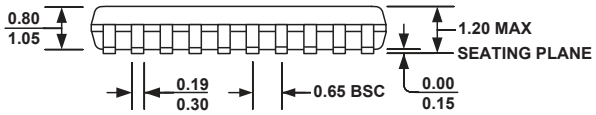
TSSOP-20F
(EXPOSED PAD)



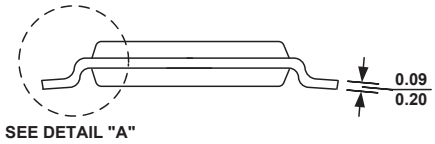
TOP VIEW



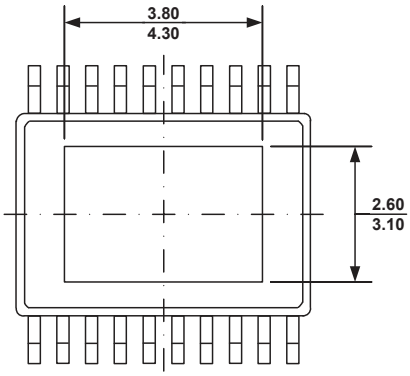
RECOMMENDED LAND PATTERN



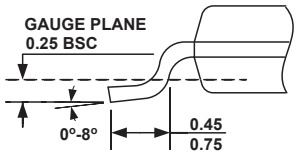
FRONT VIEW



SIDE VIEW



BOTTOM VIEW



DETAIL "A"

NOTE:

1) ALL DIMENSIONS ARE IN MILLIMETERS.
2) PACKAGE LENGTH DOES NOT INCLUDE MOLD FLASH, PROTRUSION OR GATE BURR.
3) PACKAGE WIDTH DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION.
4) LEAD COPLANARITY (BOTTOM OF LEADS AFTER FORMING) SHALL BE 0.10 MILLIMETERS MAX.
5) DRAWING CONFORMS TO JEDEC MO-153, VARIATION ACT.
6) DRAWING IS NOT TO SCALE.

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