



THE DATASHEET OF MCF52223CVM80

MCF52223

MCF52223 ColdFire Microcontroller

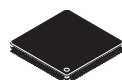
Supports MCF52223 and
MCF52221

The MCF52223 microcontroller family is a member of the ColdFire® family of reduced instruction set computing (RISC) microprocessors.

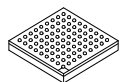
This document provides an overview of the 32-bit MCF52223 microcontroller, focusing on its highly integrated and diverse feature set.

This 32-bit device is based on the Version 2 ColdFire core operating at a frequency up to 80 MHz, offering high performance and low power consumption. On-chip memories connected tightly to the processor core include up to 256 Kbytes of flash memory and 32 Kbytes of static random access memory (SRAM). On-chip modules include:

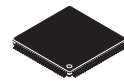
- V2 ColdFire core delivering 76 MIPS (Dhrystone 2.1) at 80 MHz running from internal flash memory with Multiply Accumulate (MAC) Unit and hardware divider
- Universal Serial Bus On-The-Go (USBOTG)
- USB Transceiver
- Three universal asynchronous/synchronous receiver/transmitters (UARTs)
- Inter-integrated circuit (I2C™) bus interface module
- Queued serial peripheral interface (QSPI) module
- Eight-channel 12-bit fast analog-to-digital converter (ADC)
- Four-channel direct memory access (DMA) controller
- Four 32-bit input capture/output compare timers with DMA support (DTIM)
- Four-channel general-purpose timer (GPT) capable of input capture/output compare, pulse width modulation (PWM), and pulse accumulation
- Eight-channel/Four-channel, 8-bit/16-bit pulse width modulation timer
- Two 16-bit periodic interrupt timers (PITs)
- Real-time clock (RTC) module
- Programmable software watchdog timer
- Interrupt controller capable of handling 57 sources



LQFP-64
10 mm x 10 mm



MAPBGA-81
10 mm x 10 mm



LQFP-100
14 mm x 14 mm

- Clock module with 8 MHz on-chip relaxation oscillator and integrated phase-locked loop (PLL)
- Test access/debug port (JTAG, BDM)

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1 Family Configurations

Table 1. MCF52223 Family Configurations

Module	52221	52223
ColdFire Version 2 Core with MAC (Multiply-Accumulate Unit)	•	•
System Clock	66, 80 MHz	
Performance (Dhrystone 2.1 MIPS)	up to 76	
Flash / Static RAM (SRAM)	128/16 Kbytes	256/32 Kbytes
Interrupt Controller (INTC)	•	•
Fast Analog-to-Digital Converter (ADC)	•	•
USB On-The-Go (USB OTG)	•	•
Four-channel Direct-Memory Access (DMA)	•	•
Software Watchdog Timer (WDT)	•	•
Programmable Interrupt Timer	2	2
Four-Channel General Purpose Timer	•	•
32-bit DMA Timers	4	4
QSPI	•	•
UART(s)	3	3
I ² C	•	•
Eight/Four-channel 8/16-bit PWM Timer	•	•
General Purpose I/O Module (GPIO)	•	•
Chip Configuration and Reset Controller Module	•	•
Background Debug Mode (BDM)	•	•
JTAG - IEEE 1149.1 Test Access Port ¹	•	•
Package	64 LQFP 81 MAPBGA 100 LQFP	81 MAPBGA 100 LQFP

¹ The full debug/trace interface is available only on the 100-pin packages. A reduced debug interface is bonded on smaller packages.

1.1 Block Diagram

Figure 1 shows a top-level block diagram of the device. Package options for this family are described later in this document.

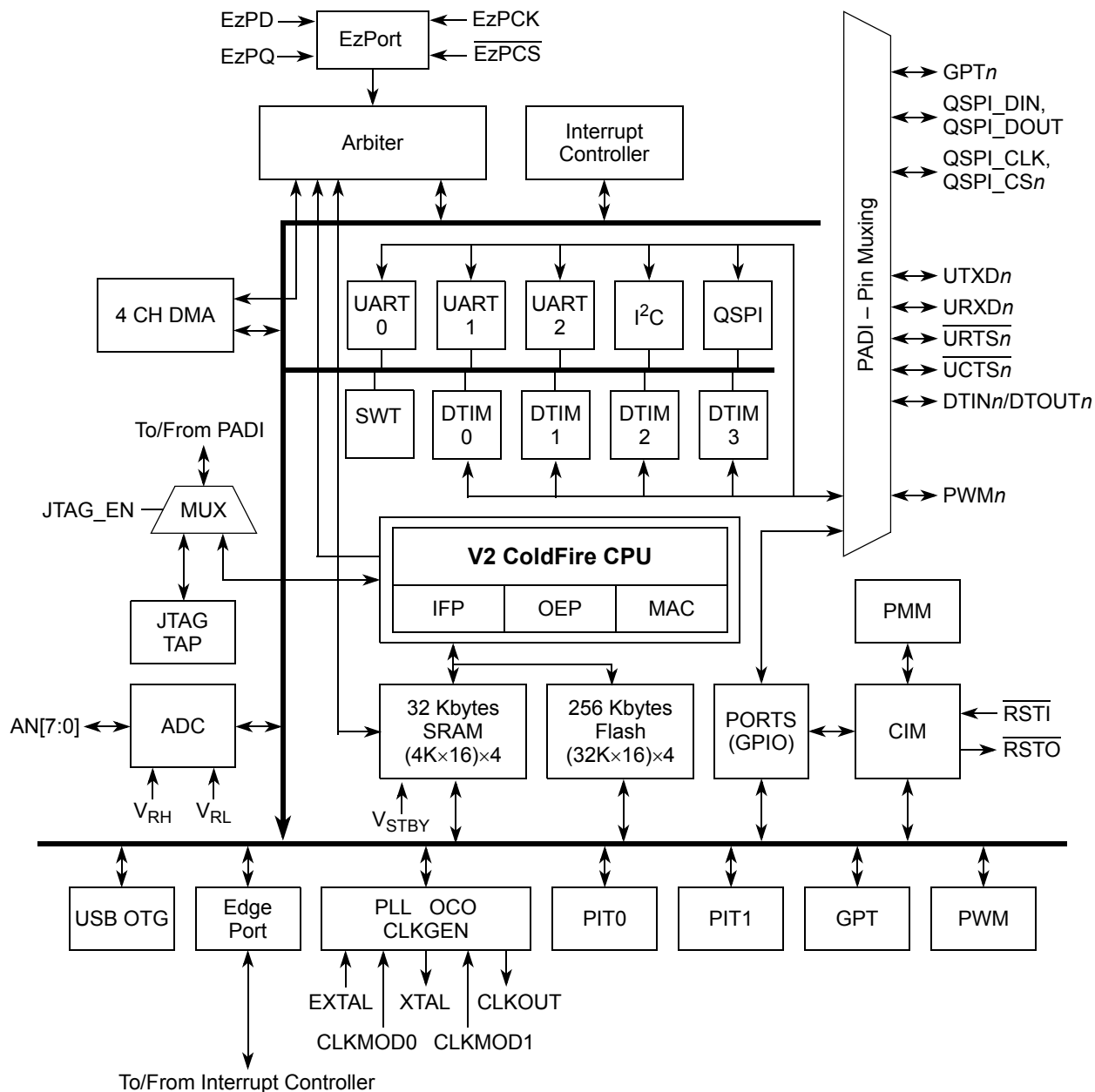


Figure 1. Block Diagram

1.2 Features

1.2.1 Feature Overview

The MCF52223 family includes the following features:

- Version 2 ColdFire variable-length RISC processor core
 - Static operation
 - 32-bit address and data paths on-chip
 - Up to 80 MHz processor core frequency
 - Sixteen general-purpose, 32-bit data and address registers
 - Implements ColdFire ISA_A with extensions to support the user stack pointer register and four new instructions for improved bit processing (ISA_A+)
 - Multiply-Accumulate (MAC) unit with 32-bit accumulator to support $16 \times 16 \rightarrow 32$ or $32 \times 32 \rightarrow 32$ operations
 - Illegal instruction decode that allows for 68-Kbyte emulation support
- System debug support
 - Real-time trace for determining dynamic execution path
 - Background debug mode (BDM) for in-circuit debugging (DEBUG_B+)
 - Real-time debug support, with six hardware breakpoints (4 PC, 1 address and 1 data) configurable into a 1- or 2-level trigger
- On-chip memories
 - 32-Kbyte dual-ported SRAM on CPU internal bus, supporting core and DMA access with standby power supply support
 - 256 Kbytes of interleaved flash memory supporting 2-1-1-1 accesses
- Power management
 - Fully static operation with processor sleep and whole chip stop modes
 - Rapid response to interrupts from the low-power sleep mode (wake-up feature)
 - Clock enable/disable for each peripheral when not used
 - Software controlled disable of external clock output for low-power consumption
- Universal Serial Bus On-The-Go (USB OTG) dual-mode host and device controller
 - Full-speed / low-speed host controller
 - USB 1.1 and 2.0 compliant full-speed / low speed device controller
 - 16 bidirectional end points
 - DMA or FIFO data stream interfaces
 - Low power consumption
 - OTG protocol logic
- Three universal asynchronous/synchronous receiver transmitters (UARTs)
 - 16-bit divider for clock generation
 - Interrupt control logic with maskable interrupts
 - DMA support
 - Data formats can be 5, 6, 7 or 8 bits with even, odd, or no parity
 - Up to two stop bits in 1/16 increments
 - Error-detection capabilities
 - Modem support includes request-to-send (RTS) and clear-to-send (CTS) lines for two UARTs
 - Transmit and receive FIFO buffers
- I²C module

- Interchip bus interface for EEPROMs, LCD controllers, A/D converters, and keypads
- Fully compatible with industry-standard I²C bus
- Master and slave modes support multiple masters
- Automatic interrupt generation with programmable level
- Queued serial peripheral interface (QSPI)
 - Full-duplex, three-wire synchronous transfers
 - Up to four chip selects available
 - Master mode operation only
 - Programmable bit rates up to half the CPU clock frequency
 - Up to 16 pre-programmed transfers
- Fast analog-to-digital converter (ADC)
 - Eight analog input channels
 - 12-bit resolution
 - Minimum 1.125 μ s conversion time
 - Simultaneous sampling of two channels for motor control applications
 - Single-scan or continuous operation
 - Optional interrupts on conversion complete, zero crossing (sign change), or under/over low/high limit
 - Unused analog channels can be used as digital I/O
- Four 32-bit timers with DMA support
 - 12.5 ns resolution at 80 MHz
 - Programmable sources for clock input, including an external clock option
 - Programmable prescaler
 - Input capture capability with programmable trigger edge on input pin
 - Output compare with programmable mode for the output pin
 - Free run and restart modes
 - Maskable interrupts on input capture or output compare
 - DMA trigger capability on input capture or output compare
- Four-channel general purpose timer
 - 16-bit architecture
 - Programmable prescaler
 - Output pulse-widths variable from microseconds to seconds
 - Single 16-bit input pulse accumulator
 - Toggle-on-overflow feature for pulse-width modulator (PWM) generation
 - One dual-mode pulse accumulation channel
- Pulse-width modulation timer
 - Operates as eight channels with 8-bit resolution or four channels with 16-bit resolution
 - Programmable period and duty cycle
 - Programmable enable/disable for each channel
 - Software selectable polarity for each channel
 - Period and duty cycle are double buffered. Change takes effect when the end of the current period is reached (PWM counter reaches zero) or when the channel is disabled.
 - Programmable center or left aligned outputs on individual channels
 - Four clock sources (A, B, SA, and SB) provide for a wide range of frequencies
 - Emergency shutdown
- Two periodic interrupt timers (PITs)

Family Configurations

- 16-bit counter
- Selectable as free running or count down
- Real-Time Clock (RTC)
 - Maintains system time-of-day clock
 - Provides stopwatch and alarm interrupt functions
- Software watchdog timer
 - 32-bit counter
 - Low-power mode support
- Clock generation features
 - Crystal, on-chip trimmed relaxation oscillator, or external oscillator reference options
 - Trimmed relaxation oscillator
 - Pre-divider capable of dividing the clock source frequency into the PLL reference frequency range
 - System can be clocked from PLL or directly from crystal oscillator or relaxation oscillator
 - Low power modes supported
 - 2^n ($0 \leq n \leq 15$) low-power divider for extremely low frequency operation
- Interrupt controller
 - Uniquely programmable vectors for all interrupt sources
 - Fully programmable level and priority for all peripheral interrupt sources
 - Seven external interrupt signals with fixed level and priority
 - Unique vector number for each interrupt source
 - Ability to mask any individual interrupt source or all interrupt sources (global mask-all)
 - Support for hardware and software interrupt acknowledge (IACK) cycles
 - Combinatorial path to provide wake-up from low-power modes
- DMA controller
 - Four fully programmable channels
 - Dual-address transfer support with 8-, 16-, and 32-bit data capability, along with support for 16-byte (4×32-bit) burst transfers
 - Source/destination address pointers that can increment or remain constant
 - 24-bit byte transfer counter per channel
 - Auto-alignment transfers supported for efficient block movement
 - Bursting and cycle-steal support
 - Software-programmable DMA requests for the UARTs (3) and 32-bit timers (4)
- Reset
 - Separate reset in and reset out signals
 - Seven sources of reset:
 - Power-on reset (POR)
 - External
 - Software
 - Watchdog
 - Loss of clock
 - Loss of lock
 - Low-voltage detection (LVD)
 - Status flag indication of source of last reset
- Chip configuration module (CCM)
 - System configuration during reset

- Selects one of six clock modes
- Configures output pad drive strength
- Unique part identification number and part revision number
- General purpose I/O interface
 - Up to 56 bits of general purpose I/O
 - Bit manipulation supported via set/clear functions
 - Programmable drive strengths
 - Unused peripheral pins may be used as extra GPIO
- JTAG support for system level board testing

1.2.2 V2 Core Overview

The version 2 ColdFire processor core is comprised of two separate pipelines decoupled by an instruction buffer. The two-stage instruction fetch pipeline (IFP) is responsible for instruction-address generation and instruction fetch. The instruction buffer is a first-in-first-out (FIFO) buffer that holds prefetched instructions awaiting execution in the operand execution pipeline (OEP). The OEP includes two pipeline stages. The first stage decodes instructions and selects operands (DSOC); the second stage (AGEX) performs instruction execution and calculates operand effective addresses, if needed.

The V2 core implements the ColdFire instruction set architecture revision A+ with support for a separate user stack pointer register and four new instructions to assist in bit processing. Additionally, the core includes the multiply-accumulate (MAC) unit for improved signal processing capabilities. The MAC implements a three-stage arithmetic pipeline, optimized for 16x16 bit operations, with support for one 32-bit accumulator. Supported operands include 16- and 32-bit signed and unsigned integers, signed fractional operands, and a complete set of instructions to process these data types. The MAC provides support for execution of DSP operations within the context of a single processor at a minimal hardware cost.

1.2.3 Integrated Debug Module

The ColdFire processor core debug interface is provided to support system debugging with low-cost debug and emulator development tools. Through a standard debug interface, access to debug information and real-time tracing capability is provided on 100-lead packages. This allows the processor and system to be debugged at full speed without the need for costly in-circuit emulators.

The on-chip breakpoint resources include a total of nine programmable 32-bit registers: an address and an address mask register, a data and a data mask register, four PC registers, and one PC mask register. These registers can be accessed through the dedicated debug serial communication channel or from the processor's supervisor mode programming model. The breakpoint registers can be configured to generate triggers by combining the address, data, and PC conditions in a variety of single- or dual-level definitions. The trigger event can be programmed to generate a processor halt or initiate a debug interrupt exception. This device implements revision B+ of the ColdFire Debug Architecture.

The processor's interrupt servicing options during emulator mode allow real-time critical interrupt service routines to be serviced while processing a debug interrupt event. This ensures the system continues to operate even during debugging.

To support program trace, the V2 debug module provides processor status (PST[3:0]) and debug data (DDATA[3:0]) ports. These buses and the PSTCLK output provide execution status, captured operand data, and branch target addresses defining processor activity at the CPU's clock rate. The device includes a new debug signal, ALLPST. This signal is the logical AND of the processor status (PST[3:0]) signals and is useful for detecting when the processor is in a halted state (PST[3:0] = 1111).

The full debug/trace interface is available only on the 100-pin packages. However, every product features the dedicated debug serial communication channel (DSI, DSO, DSCLK) and the ALLPST signal.

1.2.4 JTAG

The processor supports circuit board test strategies based on the Test Technology Committee of IEEE and the Joint Test Action Group (JTAG). The test logic includes a test access port (TAP) consisting of a 16-state controller, an instruction register, and three test registers (a 1-bit bypass register, a 112-bit boundary-scan register, and a 32-bit ID register). The boundary scan register links the device's pins into one shift register. Test logic, implemented using static logic design, is independent of the device system logic.

The device implementation can:

- Perform boundary-scan operations to test circuit board electrical continuity
- Sample system pins during operation and transparently shift out the result in the boundary scan register
- Bypass the device for a given circuit board test by effectively reducing the boundary-scan register to a single bit
- Disable the output drive to pins during circuit-board testing
- Drive output pins to stable levels

1.2.5 On-Chip Memories

1.2.5.1 SRAM

The dual-ported SRAM module provides a general-purpose 32-Kbyte memory block that the ColdFire core can access in a single cycle. The location of the memory block can be set to any 32-Kbyte boundary within the 4-Gbyte address space. This memory is ideal for storing critical code or data structures and for use as the system stack. Because the SRAM module is physically connected to the processor's high-speed local bus, it can quickly service core-initiated accesses or memory-referencing commands from the debug module.

The SRAM module is also accessible by the DMA. The dual-ported nature of the SRAM makes it ideal for implementing applications with double-buffer schemes, where the processor and a DMA device operate in alternate regions of the SRAM to maximize system performance.

1.2.5.2 Flash Memory

The ColdFire flash module (CFM) is a non-volatile memory (NVM) module that connects to the processor's high-speed local bus. The CFM is constructed with four banks of 32-Kbyte×16-bit flash memory arrays to generate 256 Kbytes of 32-bit flash memory. These electrically erasable and programmable arrays serve as non-volatile program and data memory. The flash memory is ideal for program and data storage for single-chip applications, allowing for field reprogramming without requiring an external high voltage source. The CFM interfaces to the ColdFire core through an optimized read-only memory controller that supports interleaved accesses from the 2-cycle flash memory arrays. A backdoor mapping of the flash memory is used for all program, erase, and verify operations, as well as providing a read datapath for the DMA. Flash memory may also be programmed via the EzPort, which is a serial flash memory programming interface that allows the flash memory to be read, erased and programmed by an external controller in a format compatible with most SPI bus flash memory chips.

1.2.6 Power Management

The device incorporates several low-power modes of operation entered under program control and exited by several external trigger events. An integrated power-on reset (POR) circuit monitors the input supply and forces an MCU reset as the supply voltage rises. The low voltage detector (LVD) monitors the supply voltage and is configurable to force a reset or interrupt condition if it falls below the LVD trip point. The RAM standby switch provides power to RAM when the supply voltage to the chip falls below the standby battery voltage.

1.2.7 USB On-The-Go Controller

The device includes a Universal Serial Bus On-The-Go (USB OTG) dual-mode controller. USB is a popular standard for connecting peripherals and portable consumer electronic devices such as digital cameras and handheld computers to host PCs. The OTG supplement to the USB specification extends USB to peer-to-peer application, enabling devices to connect directly to each other without the need for a PC. The dual-mode controller on the device can act as a USB OTG host and as a USB device. It also supports full-speed and low-speed modes.

1.2.8 UARTs

The device has three full-duplex UARTs that function independently. The three UARTs can be clocked by the system bus clock, eliminating the need for an external clock source. On smaller packages, the third UART is multiplexed with other digital I/O functions.

1.2.9 I²C Bus

The I²C bus is an industry-standard, two-wire, bidirectional serial bus that provides a simple, efficient method of data exchange and minimizes the interconnection between devices. This bus is suitable for applications requiring occasional communications over a short distance between many devices.

1.2.10 QSPI

The queued serial peripheral interface (QSPI) provides a synchronous serial peripheral interface with queued transfer capability. It allows up to 16 transfers to be queued at once, minimizing the need for CPU intervention between transfers.

1.2.11 Fast ADC

The fast ADC consists of an eight-channel input select multiplexer and two independent sample and hold (S/H) circuits feeding separate 12-bit ADCs. The two separate converters store their results in accessible buffers for further processing.

The ADC can be configured to perform a single scan and halt, a scan when triggered, or a programmed scan sequence repeatedly until manually stopped.

The ADC can be configured for sequential or simultaneous conversion. When configured for sequential conversions, up to eight channels can be sampled and stored in any order specified by the channel list register. Both ADCs may be required during a scan, depending on the inputs to be sampled.

During a simultaneous conversion, both S/H circuits are used to capture two different channels at the same time. This configuration requires that a single channel may not be sampled by both S/H circuits simultaneously.

Optional interrupts can be generated at the end of the scan sequence if a channel is out of range (measures below the low threshold limit or above the high threshold limit set in the limit registers) or at several different zero crossing conditions.

1.2.12 DMA Timers (DTIM0–DTIM3)

There are four independent, DMA transfer capable 32-bit timers (DTIM0, DTIM1, DTIM2, and DTIM3) on the device. Each module incorporates a 32-bit timer with a separate register set for configuration and control. The timers can be configured to operate from the system clock or from an external clock source using one of the DTIN_n signals. If the system clock is selected, it can be divided by 16 or 1. The input clock is further divided by a user-programmable 8-bit prescaler that clocks the actual timer counter register (TCR_n). Each of these timers can be configured for input capture or reference (output) compare mode. Timer events may optionally cause interrupt requests or DMA transfers.

1.2.13 General Purpose Timer (GPT)

The general purpose timer (GPT) is a four-channel timer module consisting of a 16-bit programmable counter driven by a seven-stage programmable prescaler. Each of the four channels can be configured for input capture or output compare. Additionally, channel three, can be configured as a pulse accumulator.

A timer overflow function allows software to extend the timing capability of the system beyond the 16-bit range of the counter. The input capture and output compare functions allow simultaneous input waveform measurements and output waveform generation. The input capture function can capture the time of a selected transition edge. The output compare function can generate output waveforms and timer software delays. The 16-bit pulse accumulator can operate as a simple event counter or a gated time accumulator.

1.2.14 Periodic Interrupt Timers (PIT0 and PIT1)

The two periodic interrupt timers (PIT0 and PIT1) are 16-bit timers that provide interrupts at regular intervals with minimal processor intervention. Each timer can count down from the value written in its PIT modulus register or it can be a free-running down-counter.

1.2.15 Real-Time Clock (RTC)

The Real-Time Clock (RTC) module maintains the system (time-of-day) clock and provides stopwatch, alarm, and interrupt functions. It includes full clock features: seconds, minutes, hours, days and supports a host of time-of-day interrupt functions along with an alarm interrupt.

1.2.16 Pulse-Width Modulation (PWM) Timers

The device has an 8-channel, 8-bit PWM timer. Each channel has a programmable period and duty cycle as well as a dedicated counter. Each of the modulators can create independent continuous waveforms with software-selectable duty rates from 0% to 100%. The PWM outputs have programmable polarity, and can be programmed as left aligned outputs or center aligned outputs. For higher period and duty cycle resolution, each pair of adjacent channels ([7:6], [5:4], [3:2], and [1:0]) can be concatenated to form a single 16-bit channel. The module can, therefore, be configured to support 8/0, 6/1, 4/2, 2/3, or 0/4 8-/16-bit channels.

1.2.17 Software Watchdog Timer

The watchdog timer is a 32-bit timer that facilitates recovery from runaway code. The watchdog counter is a free-running down-counter that generates a reset on underflow. To prevent a reset, software must periodically restart the countdown.

1.2.18 Phase-Locked Loop (PLL)

The clock module contains a crystal oscillator, 8 MHz on-chip relaxation oscillator (OCO), phase-locked loop (PLL), reduced frequency divider (RFD), low-power divider status/control registers, and control logic. To improve noise immunity, the PLL, crystal oscillator, and relaxation oscillator have their own power supply inputs: VDDPLL and VSSPLL. All other circuits are powered by the normal supply pins, VDD and VSS.

1.2.19 Interrupt Controller (INTC)

The device has a single interrupt controller that supports up to 63 interrupt sources. There are 56 programmable sources, 49 of which are assigned to unique peripheral interrupt requests. The remaining seven sources are unassigned and may be used for software interrupt requests.

1.2.20 DMA Controller

The direct memory access (DMA) controller provides an efficient way to move blocks of data with minimal processor intervention. It has four channels that allow byte, word, longword, or 16-byte burst line transfers. These transfers are triggered by software explicitly setting a $DCRn[START]$ bit or by the occurrence of certain UART or DMA timer events.

1.2.21 Reset

The reset controller determines the source of reset, asserts the appropriate reset signals to the system, and keeps track of what caused the last reset. There are seven sources of reset:

- External reset input
- Power-on reset (POR)
- Watchdog timer
- Phase locked-loop (PLL) loss of lock
- PLL loss of clock
- Software
- Low-voltage detector (LVD)

Control of the LVD and its associated reset and interrupt are managed by the reset controller. Other registers provide status flags indicating the last source of reset and a control bit for software assertion of the $\overline{RSTO}$ pin.

1.2.22 GPIO

Nearly all pins on the device have general purpose I/O capability and are grouped into 8-bit ports. Some ports do not use all eight bits. Each port has registers that configure, monitor, and control the port pin.

1.2.23 Part Numbers and Packaging

This product is RoHS-compliant. Refer to the product page at freescale.com or contact your sales office for up-to-date RoHS information.

Table 3. Orderable Part Number Summary

Freescal Part Number	Description	Speed (MHz)	Flash/SRAM (Kbytes)	Package	Temp range (°C)
MCF52221CAE66	MCF52221 Microcontroller	66	128/16	64 LQFP	-40 to +85
MCF52221CVM66	MCF52221 Microcontroller	66	128/16	81 MAPBGA	-40 to +85
MCF52221CAF66	MCF52221 Microcontroller	66	128/16	100 LQFP	-40 to +85
MCF52221CVM80	MCF52221 Microcontroller	80	128/16	81 MAPBGA	-40 to +85
MCF52221CAF80	MCF52221 Microcontroller	80	128/16	100 LQFP	-40 to +85
MCF52223CVM66	MCF52223 Microcontroller	66	128/16	81 MAPBGA	-40 to +85
MCF52223CAF66	MCF52223 Microcontroller	66	128/16	100 LQFP	-40 to +85
MCF52223CVM80	MCF52223 Microcontroller	80	128/16	81 MAPBGA	-40 to +85
MCF52223CAF80	MCF52223 Microcontroller	80	128/16	100 LQFP	-40 to +85

Figure 5 shows the pinout configuration for the 100 LQFP.

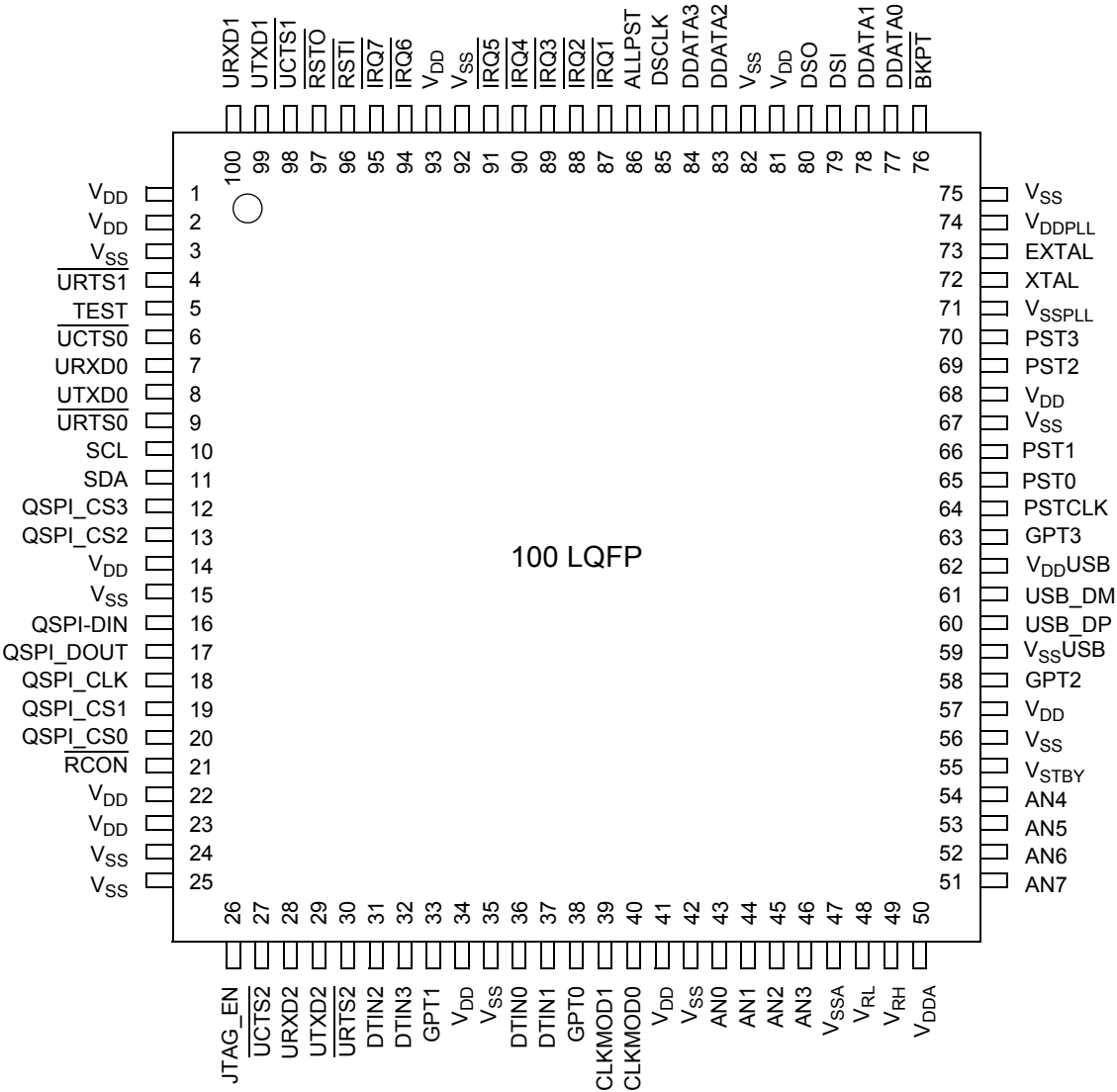


Figure 2. 100 LQFP Pin Assignments

Figure 4 shows the pinout configuration for the 81 MAPBGA.

	1	2	3	4	5	6	7	8	9
A	V _{SS}	UTXD1	$\overline{\text{RSTI}}$	$\overline{\text{IRQ5}}$	$\overline{\text{IRQ3}}$	ALLPST	TDO	TMS	V _{SS}
B	$\overline{\text{URTS1}}$	URXD1	$\overline{\text{RSTO}}$	$\overline{\text{IRQ6}}$	$\overline{\text{IRQ2}}$	$\overline{\text{TRST}}$	TDI	V _{DD} PLL	EXTAL
C	$\overline{\text{UCTS0}}$	TEST	$\overline{\text{UCTS1}}$	$\overline{\text{IRQ7}}$	$\overline{\text{IRQ4}}$	$\overline{\text{IRQ1}}$	TCLK	V _{SS} PLL	XTAL
D	URXD0	UTXD0	$\overline{\text{URTS0}}$	V _{SS}	V _{DD}	V _{SS}	PWM7	GPT3	GPT2
E	SCL	SDA	V _{DD}	V _{DD}	V _{DD}	V _{DD}	V _{DD}	PWM5	GPT1
F	QSPI_CS3	QSPI_CS2	QSPI_DIN	V _{SS}	V _{DD}	V _{SS}	GPT0	V _{STBY}	AN4
G	QSPI_DOUT	QSPI_CLK	$\overline{\text{RCON}}$	DTIN1	CLKMOD0	AN2	AN3	AN5	AN6
H	QSPI_CS0	QSPI_CS1	DTIN3	DTIN0	CLKMOD1	AN1	V _{SSA}	V _{DDA}	AN7
J	V _{SS}	JTAG_EN	DTIN2	PWM3	PWM1	AN0	V _{RL}	V _{RH}	V _{SSA}

Figure 3. 81 MAPBGA Pin Assignments

Family Configurations

	1	2	3	4	5	6	7	8	9
A	V _{SS}	UTXD1	$\overline{\text{RSTI}}$	$\overline{\text{IRQ5}}$	$\overline{\text{IRQ3}}$	ALLPST	TDO	TMS	V _{SS}
B	$\overline{\text{URTS1}}$	URXD1	$\overline{\text{RSTO}}$	$\overline{\text{IRQ6}}$	$\overline{\text{IRQ2}}$	$\overline{\text{TRST}}$	TDI	V _{DD} PLL	EXTAL
C	$\overline{\text{UCTS0}}$	TEST	$\overline{\text{UCTS1}}$	$\overline{\text{IRQ7}}$	$\overline{\text{IRQ4}}$	$\overline{\text{IRQ1}}$	TCLK	V _{SS} PLL	XTAL
D	URXD0	UTXD0	$\overline{\text{URTS0}}$	V _{SS}	V _{DD}	V _{SS}	GPT3	V _{DD} USB	USB_DM
E	SCL	SDA	V _{DD}	V _{DD}	V _{DD}	V _{DD}	V _{DD}	GPT2	USB_DP
F	QSPI_CS3	QSPI_CS2	QSPI_DIN	V _{SS}	V _{DD}	V _{SS}	V _{SS} USB	V _{STBY}	AN4
G	QSPI_DOUT	QSPI_CLK	$\overline{\text{RCON}}$	DTIN1	CLKMOD0	AN2	AN3	AN5	AN6
H	QSPI_CS0	QSPI_CS1	DTIN3	DTIN0	CLKMOD1	AN1	V _{SSA}	V _{DDA}	AN7
J	V _{SS}	JTAG_EN	DTIN2	GPT1	GPT0	AN0	V _{RL}	V _{RH}	V _{SSA}

Figure 4. 81 MAPBGA Pin Assignments

Table 13 shows the pin functions by primary and alternate purpose, and illustrates which packages contain each pin.

Table 4. Pin Functions by Primary and Alternate Purpose

Pin Group	Primary Function	Secondary Function	Tertiary Function	Quaternary Function	Drive Strength/ Control ¹	Slew Rate/ Control ¹	Pull-up / Pull-down ²	Pin on 100 LQFP
ADC	AN7	—	—	GPIO	Low	FAST	—	51
	AN6	—	—	GPIO	Low	FAST	—	52
	AN5	—	—	GPIO	Low	FAST	—	53
	AN4	—	—	GPIO	Low	FAST	—	54
	AN3	—	—	GPIO	Low	FAST	—	46
	AN2	—	—	GPIO	Low	FAST	—	45
	AN1	—	—	GPIO	Low	FAST	—	44
	AN0	—	—	GPIO	Low	FAST	—	43
	SYNCA ³	—	—	—	N/A	N/A	—	—
	SYNCB ³	—	—	—	N/A	N/A	—	—
Clock Generation	VDDA	—	—	—	N/A	N/A	—	50
	VSSA	—	—	—	N/A	N/A	—	47
	VRH	—	—	—	N/A	N/A	—	49
	VRL	—	—	—	N/A	N/A	—	48
Debug Data	EXTAL	—	—	—	N/A	N/A	—	73
	XTAL	—	—	—	N/A	N/A	—	72
	VDDPLL	—	—	—	N/A	N/A	—	74
	VSSPLL	—	—	—	N/A	N/A	—	71
Debug Data	ALLPST	—	—	—	High	FAST	—	86
	DDATA[3:0]	—	—	GPIO	High	FAST	—	84,83,78,77
	PST[3:0]	—	—	GPIO	High	FAST	—	70,69,66,65
I ² C	SCL	USB_DMI	UTXD2	GPIO	PDSR[0]	PSRR[0]	pull-up ⁴	10
	SDA	USB_DPI	URXD2	GPIO	PDSR[0]	PSRR[0]	pull-up ⁴	11

Table 4. Pin Functions by Primary and Alternate Purpose (continued)

Pin Group	Primary Function	Secondary Function	Tertiary Function	Quaternary Function	Drive Strength/ Control ¹	Slew Rate/ Control ¹	Pull-up / Pull-down ²	Pin on 100 LQFP
Interrupts	$\overline{\text{IRQ7}}$	—	—	GPIO	Low	FAST	—	95
	$\overline{\text{IRQ6}}$	—	—	GPIO	Low	FAST	—	94
	$\overline{\text{IRQ5}}$	—	—	GPIO	Low	FAST	—	91
	$\overline{\text{IRQ4}}$	—	—	GPIO	Low	FAST	—	90
	$\overline{\text{IRQ3}}$	—	—	GPIO	Low	FAST	—	89
	$\overline{\text{IRQ2}}$	—	—	GPIO	Low	FAST	—	88
	$\overline{\text{IRQ1}}$	SYNCA	USB_ALT_CLK	GPIO	High	FAST	pull-up ⁴	87
JTAG/BDM	JTAG_EN	—	—	—	N/A	N/A	pull-down	26
	TCLK/ PSTCLK	CLKOUT	—	—	High	FAST	pull-up ⁵	64
	TDI/DSI	—	—	—	N/A	N/A	pull-up ⁵	79
	TDO/DSO	—	—	—	High	FAST	—	80
	TMS /BKPT	—	—	—	N/A	N/A	pull-up ⁵	76
	$\overline{\text{TRST}}$ /DSCLK	—	—	—	N/A	N/A	pull-up ⁵	85
	CLKMOD0	—	—	—	N/A	N/A	pull-down ⁶	40
Mode Selection ⁶	CLKMOD1	—	—	—	N/A	N/A	pull-down ⁶	39
	RCON/ EZPCS	—	—	—	N/A	N/A	pull-up	21

Table 4. Pin Functions by Primary and Alternate Purpose (continued)

Pin Group	Primary Function	Secondary Function	Tertiary Function	Quaternary Function	Drive Strength/ Control ¹	Slew Rate/ Control ¹	Pull-up / Pull-down ²	Pin on 100 LQFP
QSPI	QSPI_DIN/ EZPD	—	URXD1	GPIO	PDSR[2]	PSRR[2]	—	16
	QSPI_DOUT/ EZPQ	—	UTXD1	GPIO	PDSR[1]	PSRR[1]	—	17
	QSPI_CLK/ EZPCK	SCL	URTS [†]	GPIO	PDSR[3]	PSRR[3]	pull-up ⁸	18
	QSPI_CS3	SYNCA	—	GPIO	PDSR[7]	PSRR[7]	pull-up/pull-down ⁷	12
Reset ⁹	QSPI_CS2	—	—	GPIO	PDSR[6]	PSRR[6]	pull-up/pull-down ⁷	13
	QSPI_CS1	—	—	GPIO	PDSR[5]	PSRR[5]	—	19
	QSPI_CS0	SDA	UCTS [†]	GPIO	PDSR[4]	PSRR[4]	pull-up ⁸	20
	RST [†]	—	—	—	N/A	N/A	pull-up ⁹	96
Test	RST [†]	—	—	—	high	FAST	—	97
	TEST	—	—	—	N/A	N/A	pull-down	5
	GPT3	—	PWM7	GPIO	PDSR[23]	PSRR[23]	pull-up ¹⁰	63
	GPT2	—	PWM5	GPIO	PDSR[22]	PSRR[22]	pull-up ¹⁰	58
Timers, 16-bit	GPT1	—	PWM3	GPIO	PDSR[21]	PSRR[21]	pull-up ¹⁰	33
	GPT0	—	PWM1	GPIO	PDSR[20]	PSRR[20]	pull-up ¹⁰	38
	DTIN3	DTOUT3	PWM6	GPIO	PDSR[19]	PSRR[19]	—	32
	DTIN2	DTOUT2	PWM4	GPIO	PDSR[18]	PSRR[18]	—	31
Timers, 32-bit	DTIN1	DTOUT1	PWM2	GPIO	PDSR[17]	PSRR[17]	—	37
	DTIN0	DTOUT0	PWM0	GPIO	PDSR[16]	PSRR[16]	—	36
	UCTS [†]	—	—	GPIO	PDSR[11]	PSRR[11]	—	6
	URTS [†]	—	—	GPIO	PDSR[10]	PSRR[10]	—	9
UART 0	URXD0	—	—	GPIO	PDSR[9]	PSRR[9]	—	7
	UTXD0	—	—	GPIO	PDSR[8]	PSRR[8]	—	8

Table 4. Pin Functions by Primary and Alternate Purpose (continued)

Pin Group	Primary Function	Secondary Function	Tertiary Function	Quaternary Function	Drive Strength/ Control ¹	Slew Rate/ Control ¹	Pull-up / Pull-down ²	Pin on 100 LQFP
UART 1	UCTS1	SYNCA	URXD2	GPIO	PDSR[15]	PSRR[15]	—	98
	URTS1	SYNCB	UTXD2	GPIO	PDSR[14]	PSRR[14]	—	4
	URXD1	—	—	GPIO	PDSR[13]	PSRR[13]	—	100
	UTXD1	—	—	GPIO	PDSR[12]	PSRR[12]	—	99
UART 2	UCTS2	—	—	GPIO	PDSR[27]	PSRR[27]	—	27
	URTS2	—	—	GPIO	PDSR[26]	PSRR[26]	—	30
	URXD2	—	—	GPIO	PDSR[25]	PSRR[25]	—	28
	UTXD2	—	—	GPIO	PDSR[24]	PSRR[24]	—	29
VSTBY	VSTBY	—	—	—	N/A	N/A	—	55
USB	VDDUSB	—	—	—	N/A	N/A	—	62
	VSSUSB	—	—	—	N/A	N/A	—	59
	USB_DM	—	—	—	N/A	N/A	—	61
	USB_DP	—	—	—	N/A	N/A	—	60
VDD	VDD	—	—	—	N/A	N/A	—	1,2,14,22, 23,34,41, 57,68,81,93
VSS	VSS	—	—	—	N/A	N/A	—	3,15,24,25,3 5,42,56, 67,75,82,92

¹ The PDSR and PSSR registers are described in the General Purpose I/O chapter. All programmable signals default to 2 mA drive normal (single-chip) mode.

² All signals have a pull-up in GPIO mode.

³ These signals are multiplexed on other pins.

⁴ For primary and GPIO functions only.

⁵ Only when JTAG mode is enabled.

⁶ CLKMOD0 and CLKMOD1 have internal pull-down resistors; however, the use of external resistors is very strongly recommended.

⁷ When these pins are configured for USB signals, they should use the USB transceiver's internal pull-up/pull-down resistors (see OTG_CTRL register). If these pins are not configured for USB signals, each pin should be pulled down externally using a 10 kΩ resistor.

⁸ For secondary and GPIO functions only.

⁹ RSTI has an internal pull-up resistor; however, the use of an external resistor is very strongly recommended.

¹⁰ For GPIO function. Primary Function has pull-up control within the GPT module.



1.3 Reset Signals

Table 5 describes signals used to reset the chip or as a reset indication.

Table 5. Reset Signals

Signal Name	Abbreviation	Function	I/O
Reset In	$\overline{\text{RSTI}}$	Primary reset input to the device. Asserting $\overline{\text{RSTI}}$ for at least 8 CPU clock cycles immediately resets the CPU and peripherals.	I
Reset Out	$\overline{\text{RSTO}}$	Driven low for 1024 CPU clocks after the reset source has deasserted.	O

1.4 PLL and Clock Signals

Table 6 describes signals used to support the on-chip clock generation circuitry.

Table 6. PLL and Clock Signals

Signal Name	Abbreviation	Function	I/O
External Clock In	EXTAL	Crystal oscillator or external clock input except when the on-chip relaxation oscillator is used.	I
Crystal	XTAL	Crystal oscillator output except when CLKMOD0=0, then sampled as part of the clock mode selection mechanism.	O
Clock Out	CLKOUT	This output signal reflects the internal system clock.	O

1.5 Mode Selection

Table 7 describes signals used in mode selection; Table 8 describes the particular clocking modes.

Table 7. Mode Selection Signals

Signal Name	Abbreviation	Function	I/O
Clock Mode Selection	CLKMOD[1:0]	Selects the clock boot mode.	I
Reset Configuration	RCON	The Serial Flash Programming mode is entered by asserting the RCON pin (with the TEST pin negated) as the chip comes out of reset. During this mode, the EzPort has access to the flash memory which can be programmed from an external device.	
Test	TEST	Reserved for factory testing only and in normal modes of operation should be connected to VSS to prevent unintentional activation of test functions.	I

Table 8. Clocking Modes

CLKMOD[1:0]	XTAL	Configure the clock mode.
00	0	PLL disabled, clock driven by external oscillator
00	1	PLL disabled, clock driven by on-chip oscillator
01	N/A	PLL disabled, clock driven by crystal
10	0	PLL in normal mode, clock driven by external oscillator ¹
10	1	Reserved ²
11	N/A	PLL in normal mode, clock driven by crystal ¹

- ¹ The PLL pre-divider (CCHR+1) reset value is 6 and the PLL input reference range is 2–10 MHz, so in order to boot with the PLL enabled, the external clock or crystal frequency needs to be greater than 12 MHz. MCF5222x devices cannot boot with PLL enabled from an external clock or crystal oscillator with frequency less than 12 MHz. This constraint does not apply to booting with PLL disabled.
- ² Cannot boot from the Internal 8 MHz Relaxation oscillator with the PLL enabled. Refer Note1. Thus this mode has been removed from the table.

1.6 External Interrupt Signals

Table 9 describes the external interrupt signals.

Table 9. External Interrupt Signals

Signal Name	Abbreviation	Function	I/O
External Interrupts	$\overline{\text{IRQ}}[7:1]$	External interrupt sources.	I

1.7 Queued Serial Peripheral Interface (QSPI)

Table 10 describes the QSPI signals.

Table 10. Queued Serial Peripheral Interface (QSPI) Signals

Signal Name	Abbreviation	Function	I/O
QSPI Synchronous Serial Output	QSPI_DOUT	Provides the serial data from the QSPI and can be programmed to be driven on the rising or falling edge of QSPI_CLK.	O
QSPI Synchronous Serial Data Input	QSPI_DIN	Provides the serial data to the QSPI and can be programmed to be sampled on the rising or falling edge of QSPI_CLK.	I
QSPI Serial Clock	QSPI_CLK	Provides the serial clock from the QSPI. The polarity and phase of QSPI_CLK are programmable.	O
Synchronous Peripheral Chip Selects	QSPI_CS[3:0]	QSPI peripheral chip select; can be programmed to be active high or low.	O

1.8 USB On-the-Go

This device is compliant with industry standard USB 2.0 specification.

1.9 I²C I/O Signals

Table 11 describes the I²C serial interface module signals.

Table 11. I²C I/O Signals

Signal Name	Abbreviation	Function	I/O
Serial Clock	SCLn	Open-drain clock signal for the for the I ² C interface. When the bus is in master mode, this clock is driven by the I ² C module; when the bus is in slave mode, this clock becomes the clock input.	I/O
Serial Data	SDAn	Open-drain signal that serves as the data input/output for the I ² C interface.	I/O

1.10 UART Module Signals

Table 12 describes the UART module signals.

Table 12. UART Module Signals

Signal Name	Abbreviation	Function	I/O
Transmit Serial Data Output	UTXD n	Transmitter serial data outputs for the UART modules. The output is held high (mark condition) when the transmitter is disabled, idle, or in the local loopback mode. Data is shifted out, LSB first, on this pin at the falling edge of the serial clock source.	O
Receive Serial Data Input	URXD n	Receiver serial data inputs for the UART modules. Data is received on this pin LSB first. When the UART clock is stopped for power-down mode, any transition on this pin restarts the clock.	I
Clear-to-Send	$\overline{\text{UCTS}}n$	Indication to the UART modules that they can begin data transmission.	I
Request-to-Send	$\overline{\text{URTS}}n$	Automatic request-to-send outputs from the UART modules. This signal can also be configured to be asserted and negated as a function of the RxFIFO level.	O

1.11 DMA Timer Signals

Table 13 describes the signals of the four DMA timer modules.

Table 13. DMA Timer Signals

Signal Name	Abbreviation	Function	I/O
DMA Timer Input	DTIN	Event input to the DMA timer modules.	I
DMA Timer Output	DTOUT	Programmable output from the DMA timer modules.	O

1.12 ADC Signals

Table 14 describes the signals of the Analog-to-Digital Converter.

Table 14. ADC Signals

Signal Name	Abbreviation	Function	I/O
Analog Inputs	AN[7:0]	Inputs to the analog-to-digital converter.	I
Analog Reference	V _{RH}	Reference voltage high and low inputs.	I
	V _{RL}		I
Analog Supply	V _{DDA}	Isolate the ADC circuitry from power supply noise.	—
	V _{SSA}		—
ADC Sync Inputs	SYNCA / SYNCB	These signals can initiate an analog-to-digital conversion process.	I

1.13 General Purpose Timer Signals

Table 15 describes the general purpose timer signals.

Table 15. GPT Signals

Signal Name	Abbreviation	Function	I/O
General Purpose Timer Input/Output	GPT[3:0]	Inputs to or outputs from the general purpose timer module.	I/O

1.14 Pulse Width Modulator Signals

Table 16 describes the PWM signals.

Table 16. PWM Signals

Signal Name	Abbreviation	Function	I/O
PWM Output Channels	PWM[7:0]	Pulse width modulated output for PWM channels.	O

1.15 Debug Support Signals

These signals are used as the interface to the on-chip JTAG controller and the BDM logic.

Table 17. Debug Support Signals

Signal Name	Abbreviation	Function	I/O
JTAG Enable	JTAG_EN	Select between debug module and JTAG signals at reset.	I
Test Reset	$\overline{\text{TRST}}$	This active-low signal is used to initialize the JTAG logic asynchronously.	I
Test Clock	TCLK	Used to synchronize the JTAG logic.	I
Test Mode Select	TMS	Used to sequence the JTAG state machine. TMS is sampled on the rising edge of TCLK.	I
Test Data Input	TDI	Serial input for test instructions and data. TDI is sampled on the rising edge of TCLK.	I
Test Data Output	TDO	Serial output for test instructions and data. TDO is tri-stateable and is actively driven in the shift-IR and shift-DR controller states. TDO changes on the falling edge of TCLK.	O
Development Serial Clock	DSCLK	Development Serial Clock - Internally synchronized input. (The logic level on DSCLK is validated if it has the same value on two consecutive rising bus clock edges.) Clocks the serial communication port to the debug module during packet transfers. Maximum frequency is PSTCLK/5. At the synchronized rising edge of DSCLK, the data input on DSI is sampled and DSO changes state.	I
Breakpoint	$\overline{\text{BKPT}}$	Breakpoint - Input used to request a manual breakpoint. Assertion of $\overline{\text{BKPT}}$ puts the processor into a halted state after the current instruction completes. Halt status is reflected on processor status/debug data signals (PST[3:0] and PSTDDATA[7:0]) as the value 0xF. If CSR[BKD] is set (disabling normal $\overline{\text{BKPT}}$ functionality), asserting $\overline{\text{BKPT}}$ generates a debug interrupt exception in the processor.	I

Table 17. Debug Support Signals (continued)

Signal Name	Abbreviation	Function	I/O
Development Serial Input	DSI	Development Serial Input - Internally synchronized input that provides data input for the serial communication port to the debug module, after the DSCLK has been seen as high (logic 1).	I
Development Serial Output	DSO	Development Serial Output - Provides serial output communication for debug module responses. DSO is registered internally. The output is delayed from the validation of DSCLK high.	O
Debug Data	DDATA[3:0]	Display captured processor data and breakpoint status. The CLKOUT signal can be used by the development system to know when to sample DDATA[3:0].	O
Processor Status Clock	PSTCLK	Processor Status Clock - Delayed version of the processor clock. Its rising edge appears in the center of valid PST and DDATA output. PSTCLK indicates when the development system should sample PST and DDATA values. If real-time trace is not used, setting CSR[PCD] keeps PSTCLK, and PST and DDATA outputs from toggling without disabling triggers. Non-quiescent operation can be reenabled by clearing CSR[PCD], although the external development systems must resynchronize with the PST and DDATA outputs. PSTCLK starts clocking only when the first non-zero PST value (0xC, 0xD, or 0xF) occurs during system reset exception processing.	O
Processor Status Outputs	PST[3:0]	Indicate core status. Debug mode timing is synchronous with the processor clock; status is unrelated to the current bus transfer. The CLKOUT signal can be used by the development system to know when to sample PST[3:0].	O
All Processor Status Outputs	ALLPST	Logical AND of PST[3:0]. The CLKOUT signal can be used by the development system to know when to sample ALLPST.	O

1.16 EzPort Signal Descriptions

Table 18 contains a list of EzPort external signals.

Table 18. EzPort Signal Descriptions

Signal Name	Abbreviation	Function	I/O
EzPort Clock	EZPCK	Shift clock for EzPort transfers.	I
EzPort Chip Select	EZPCS	Chip select for signalling the start and end of serial transfers.	I
EzPort Serial Data In	EZPD	EZPD is sampled on the rising edge of EZPCK.	I
EzPort Serial Data Out	EZPQ	EZPQ transitions on the falling edge of EZPCK.	O

1.17 Power and Ground Pins

The pins described in [Table 19](#) provide system power and ground to the chip. Multiple pins are provided for adequate current capability. All power supply pins must have adequate bypass capacitance for high-frequency noise suppression.

Table 19. Power and Ground Pins

Signal Name	Abbreviation	Function
PLL Analog Supply	VDDPLL, VSSPLL	Dedicated power supply signals to isolate the sensitive PLL analog circuitry from the normal levels of noise present on the digital power supply.
USB Power Supply	V _{DD} USB	This pin supplies power to the USB Module.
USB Ground Supply	V _{SS} USB	This pin is the negative (ground) supply pin for the USB Module.
Positive Supply	VDD	These pins supply positive power to the core logic.
Ground	VSS	This pin is the negative supply (ground) to the chip.

2 Electrical Characteristics

This section contains electrical specification tables and reference timing diagrams for the microcontroller unit, including detailed information on power considerations, DC/AC electrical characteristics, and AC timing specifications.

NOTE

The parameters specified in this data sheet supersede any values found in the module specifications.

2.1 Maximum Ratings

Table 20. Absolute Maximum Ratings^{1, 2}

Rating	Symbol	Value	Unit
Supply voltage	V_{DD}	−0.3 to +4.0	V
Clock synthesizer supply voltage	V_{DDPLL}	−0.3 to +4.0	V
RAM standby supply voltage	V_{STBY}	−0.3 to +4.0	V
USB standby supply voltage	V_{DDUSB}	−0.3 to +4.0	V
Digital input voltage ³	V_{IN}	−0.3 to +4.0	V
EXTAL pin voltage	V_{EXTAL}	0 to 3.3	V
XTAL pin voltage	V_{XTAL}	0 to 3.3	V
Instantaneous maximum current Single pin limit (applies to all pins) ^{4, 5}	I_{DD}	25	mA
Operating temperature range (packaged)	T_A ($T_L - T_H$)	−40 to 85 ⁶	°C
Storage temperature range	T_{stg}	−65 to 150	°C

¹ Functional operating conditions are given in DC Electrical Specifications. Absolute Maximum Ratings are stress ratings only, and functional operation at the maxima is not guaranteed. Stress beyond those listed may affect device reliability or cause permanent damage to the device.

² This device contains circuitry protecting against damage due to high static voltage or electrical fields; however, it is advised that normal precautions be taken to avoid application of any voltages higher than maximum-rated voltages to this high-impedance circuit. Reliability of operation is enhanced if unused inputs are tied to an appropriate logic voltage level (V_{SS} or V_{DD}).

³ Input must be current limited to the I_{DD} value specified. To determine the value of the required current-limiting resistor, calculate resistance values for positive and negative clamp voltages, then use the larger of the two values.

⁴ All functional non-supply pins are internally clamped to V_{SS} and V_{DD} .

⁵ The power supply must maintain regulation within operating V_{DD} range during instantaneous and operating maximum current conditions. If positive injection current ($V_{in} > V_{DD}$) is greater than I_{DD} , the injection current may flow out of V_{DD} and could result in the external power supply going out of regulation. Ensure that the external V_{DD} load shunts current greater than maximum injection current. This is the greatest risk when the MCU is not consuming power (e.g., no clock).

⁶ Depending on the packaging; see the orderable part number summary.

2.2 Current Consumption

Table 21, Table 22, and Figure 5 show the typical current consumption in low-power modes.

Table 21. Current Consumption in Low-Power Mode, Code From Flash Memory^{1,2,3}

Mode	8 MHz (Typ)	16 MHz (Typ)	64 MHz (Typ)	80 MHz (Typ)	Units
Stop mode 3 (Stop 11) ⁴	0.070				mA
Stop mode 2 (Stop 10) ⁴	2.9				
Stop mode 1 (Stop 01) ^{4,5}	3.6	3.9	6	6.7	
Stop mode 0 (Stop 00) ⁵	3.6	3.9	6	6.7	
Wait / Doze	13	23	38	44	
Run	TBD	TBD	TBD	TBD	

¹ All values are measured with a 3.30V power supply. Tests performed at room temperature.

² Refer to the Power Management chapter in the *MCF52223 Reference Manual* for more information on low-power modes.

³ CLKOUT, PST/DDATA signals, and all peripheral clocks except UART0 and CFM off before entering low-power mode. CLKOUT is disabled.

⁴ See the description of the Low-Power Control Register (LPCR) in the *MCF52223 Reference Manual* for more information on stop modes 0–3.

⁵ Results are identical to STOP 00 for typical values because they only differ by CLKOUT power consumption. CLKOUT is already disabled in this instance prior to entering low-power mode.

Table 22. Current Consumption in Low-Power Mode, Code From SRAM^{1,2,3}

Mode	8 MHz (Typ)	16 MHz (Typ)	64 MHz (Typ)	80 MHz (Typ)	Units
Stop mode 3 (Stop 11) ⁴	0.010				mA
Stop mode 2 (Stop 10) ⁴	2.7				
Stop mode 1 (Stop 01) ^{4,5}	3.4	3.7	5.8	6.5	
Stop mode 0 (Stop 00) ⁵	3.4	3.7	5.8	6.5	
Wait / Doze	6	8	22	27	
Run	7	11	33	41	

¹ All values are measured with a 3.30V power supply. Tests performed at room temperature.

² Refer to the Power Management chapter in the *MCF52223 Reference Manual* for more information on low-power modes.

³ CLKOUT, PST/DDATA signals, and all peripheral clocks except UART0 off before entering low-power mode. CLKOUT is disabled. Code executed from SRAM with flash memory shut off by writing 0x0 to the FLASHBAR register.

⁴ See the description of the Low-Power Control Register (LPCR) in the *MCF52223 Reference Manual* for more information on stop modes 0–3.

⁵ Results are identical to STOP 00 for typical values because they only differ by CLKOUT power consumption. CLKOUT is already disabled in this instance prior to entering low-power mode.

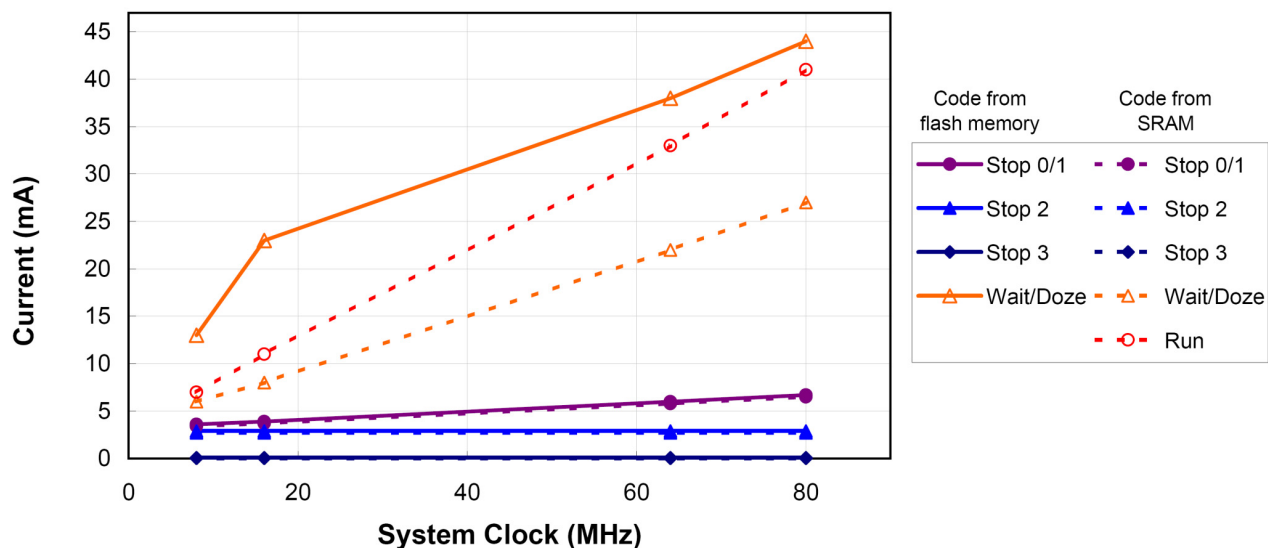


Figure 5. Plot of Current Consumption in Low-Power Modes

Table 23. Typical Active Current Consumption Specifications

Characteristic	Symbol	Typical ¹ Active (SRAM)	Typical ¹ Active (Flash)	Peak ² Active (Flash)	Unit
8 MHz core & I/O	I _{DD}	8	11	18	mA
16 MHz core & I/O		11	19	33	
64 MHz core & I/O		35	44	82	
80 MHz core & I/O		43	52	98	
RAM standby supply current • Normal operation: V _{DD} > V _{STBY} - 0.3 V • Transient condition: V _{STBY} - 0.3 V > V _{DD} > V _{SS} + 0.5 V • Standby operation: V _{DD} < V _{SS} + 0.5 V	I _{STBY}	—	—	0.4 TBD 16	μA
Analog supply current • Normal operation • Standby mode • Powered down	I _{DDA}	2 ^(see note 3) — —	—	13 TBD 0	mA
USB supply current	I _{DDUSB}	—	—	2	mA
PLL supply current	I _{DDPLL}	—	—	6 ^(see note 4)	mA

¹ Tested at room temperature with CPU polling a status register. All clocks were off except the UART and CFM (when running from flash memory).

² Peak current measured with all modules active, CPU polling a status register, and default drive strength with matching load.

³ Tested using Auto Power Down (APD), which powers down the ADC between conversions; ADC running at 4 MHz in Once Parallel mode with a sample rate of 3 kHz.

⁴ Tested with the PLL MFD set to 7 (max value). Setting the MFD to a lower value results in lower current consumption.

2.3 Thermal Characteristics

Table 24 lists thermal resistance values.

Table 24. Thermal Characteristics

	Characteristic		Symbol	Value	Unit
100 LQFP	Junction to ambient, natural convection	Single layer board (1s)	θ_{JA}	53 ^{1,2}	°C/W
	Junction to ambient, natural convection	Four layer board (2s2p)	θ_{JA}	39 ^{1,3}	°C/W
	Junction to ambient, (@200 ft/min)	Single layer board (1s)	θ_{JMA}	42 ^{1,3}	°C/W
	Junction to ambient, (@200 ft/min)	Four layer board (2s2p)	θ_{JMA}	33 ^{1,3}	°C/W
	Junction to board	—	θ_{JB}	25 ⁴	°C/W
	Junction to case	—	θ_{JC}	9 ⁵	°C/W
	Junction to top of package	Natural convection	Ψ_{jt}	2 ⁶	°C/W
	Maximum operating junction temperature	—	T_j	105	°C
81 MAPBGA	Junction to ambient, natural convection	Single layer board (1s)	θ_{JA}	61 ^{1,2}	°C/W
	Junction to ambient, natural convection	Four layer board (2s2p)	θ_{JA}	35 ^{2,3}	°C/W
	Junction to ambient, (@200 ft/min)	Single layer board (1s)	θ_{JMA}	50 ^{2,3}	°C/W
	Junction to ambient, (@200 ft/min)	Four layer board (2s2p)	θ_{JMA}	31 ^{2,3}	°C/W
	Junction to board	—	θ_{JB}	20 ⁴	°C/W
	Junction to case	—	θ_{JC}	12 ⁵	°C/W
	Junction to top of package	Natural convection	Ψ_{jt}	2 ⁶	°C/W
	Maximum operating junction temperature	—	T_j	105	°C
64 LQFP	Junction to ambient, natural convection	Single layer board (1s)	θ_{JA}	62 ^{1,2}	°C/W
	Junction to ambient, natural convection	Four layer board (2s2p)	θ_{JA}	43 ^{1,3}	°C/W
	Junction to ambient (@200 ft/min)	Single layer board (1s)	θ_{JMA}	50 ^{1,3}	°C/W
	Junction to ambient (@200 ft/min)	Four layer board (2s2p)	θ_{JMA}	36 ^{1,3}	°C/W
	Junction to board	—	θ_{JB}	26 ⁴	°C/W
	Junction to case	—	θ_{JC}	9 ⁵	°C/W
	Junction to top of package	Natural convection	Ψ_{jt}	2 ⁶	°C/W
	Maximum operating junction temperature	—	T_j	105	°C

¹ θ_{JA} and Ψ_{jt} parameters are simulated in conformance with EIA/JESD Standard 51-2 for natural convection. Freescale recommends the use of θ_{JA} and power dissipation specifications in the system design to prevent device junction temperatures from exceeding the rated specification. System designers should be aware that device junction temperatures can be significantly influenced by board layout and surrounding devices. Conformance to the device junction temperature specification can be verified by physical measurement in the customer's system using the Ψ_{jt} parameter, the device power dissipation, and the method described in EIA/JESD Standard 51-2.

² Per JEDEC JESD51-2 with the single-layer board (JESD51-3) horizontal.

³ Per JEDEC JESD51-6 with the board JESD51-7) horizontal.

⁴ Thermal resistance between the die and the printed circuit board in conformance with JEDEC JESD51-8. Board temperature is measured on the top surface of the board near the package.

⁵ Thermal resistance between the die and the case top surface as measured by the cold plate method (MIL SPEC-883 Method 1012.1).

Electrical Characteristics

⁶ Thermal characterization parameter indicating the temperature difference between package top and the junction temperature per JEDEC JESD51-2. When Greek letters are not available, the thermal characterization parameter is written in conformance with Psi-JT.

The average chip-junction temperature (T_J) in °C can be obtained from:

$$T_J = T_A + (P_D \times \Theta_{JMA}) \quad (1)$$

Where:

- T_A = ambient temperature, °C
- Θ_{JA} = package thermal resistance, junction-to-ambient, °C/W
- P_D = $P_{INT} + P_{I/O}$
- P_{INT} = chip internal power, $I_{DD} \times V_{DD}$, watts
- $P_{I/O}$ = power dissipation on input and output pins — user determined, watts

For most applications $P_{I/O} < P_{INT}$ and can be ignored. An approximate relationship between P_D and T_J (if $P_{I/O}$ is neglected) is:

$$P_D = K \div (T_J + 273^\circ\text{C}) \quad (2)$$

Solving equations 1 and 2 for K gives:

$$K = P_D \times (T_A + 273^\circ\text{C}) + \Theta_{JMA} \times P_D^2 \quad (3)$$

where K is a constant pertaining to the particular part. K can be determined from equation (3) by measuring P_D (at equilibrium) for a known T_A . Using this value of K, the values of P_D and T_J can be obtained by solving equations (1) and (2) iteratively for any value of T_A .

2.4 Flash Memory Characteristics

The flash memory characteristics are shown in [Table 25](#) and [Table 26](#).

Table 25. SGFM Flash Program and Erase Characteristics

($V_{DD} = 3.0$ to 3.6 V)

Parameter	Symbol	Min	Typ	Max	Unit
System clock (read only)	$f_{\text{sys(R)}}$	0	—	66.67 or 80 ¹	MHz
System clock (program/erase) ²	$f_{\text{sys(P/E)}}$	0.15	—	66.67 or 80 ¹	MHz

¹ Depending on packaging; see the orderable part number summary.

² Refer to the flash memory section for more information

Table 26. SGFM Flash Module Life Characteristics

($V_{DD} = 3.0$ to 3.6 V)

Parameter	Symbol	Value	Unit
Maximum number of guaranteed program/erase cycles ¹ before failure	P/E	10,000 ²	Cycles
Data retention at average operating temperature of 85°C	Retention	10	Years

¹ A program/erase cycle is defined as switching the bits from 1 → 0 → 1.

² Reprogramming of a flash memory array block prior to erase is not required.

2.5 EzPort Electrical Specifications

Table 27. EzPort Electrical Specifications

Name	Characteristic	Min	Max	Unit
EP1	EPCK frequency of operation (all commands except READ)	—	$f_{\text{sys}} / 2$	MHz
EP1a	EPCK frequency of operation (READ command)	—	$f_{\text{sys}} / 8$	MHz
EP2	EPCS_b negation to next EPCS_b assertion	$2 \times T_{\text{cyc}}$	—	ns
EP3	EPCS_B input valid to EPCK high (setup)	5	—	ns
EP4	EPCK high to EPCS_B input invalid (hold)	5	—	ns
EP5	EPD input valid to EPCK high (setup)	2	—	ns
EP6	EPCK high to EPD input invalid (hold)	5	—	ns
EP7	EPCK low to EPQ output valid (out setup)	—	12	ns
EP8	EPCK low to EPQ output invalid (out hold)	0	—	ns
EP9	EPCS_B negation to EPQ tri-state	—	12	ns

2.6 ESD Protection

Table 28. ESD Protection Characteristics^{1, 2}

Characteristics	Symbol	Value	Units
ESD target for Human Body Model	HBM	2000	V
ESD target for Machine Model	MM	200	V
HBM circuit description	R_{series}	1500	Ω
	C	100	pF
MM circuit description	R_{series}	0	Ω
	C	200	pF
Number of pulses per pin (HBM) • Positive pulses • Negative pulses	—	1	—
	—	1	
Number of pulses per pin (MM) • Positive pulses • Negative pulses	—	3	—
	—	3	
Interval of pulses	—	1	sec

¹ All ESD testing is in conformity with CDF-AEC-Q100 Stress Test Qualification for Automotive Grade Integrated Circuits.

² A device is defined as a failure if after exposure to ESD pulses the device no longer meets the device specification requirements. Complete DC parametric and functional testing is performed per applicable device specification at room temperature followed by hot temperature, unless specified otherwise in the device specification.

2.7 DC Electrical Specifications

Table 29. DC Electrical Specifications ¹

Characteristic	Symbol	Min	Max	Unit
Supply voltage	V_{DD}	3.0	3.6	V
Standby voltage	V_{STBY}	1.8	3.6	V
Input high voltage	V_{IH}	$0.7 \times V_{DD}$	4.0	V
Input low voltage	V_{IL}	$V_{SS} - 0.3$	$0.35 \times V_{DD}$	V
Input hysteresis ²	V_{HYS}	$0.06 \times V_{DD}$	—	mV
Low-voltage detect trip voltage (V_{DD} falling)	V_{LVD}	2.15	2.3	V
Low-voltage detect hysteresis (V_{DD} rising)	V_{LVDHYS}	60	120	mV
Input leakage current $V_{in} = V_{DD}$ or V_{SS} , digital pins	I_{in}	-1.0	1.0	μA
Output high voltage (all input/output and all output pins) $I_{OH} = -2.0$ mA	V_{OH}	$V_{DD} - 0.5$	—	V
Output low voltage (all input/output and all output pins) $I_{OL} = 2.0$ mA	V_{OL}	—	0.5	V
Output high voltage (high drive) $I_{OH} = -5$ mA	V_{OH}	$V_{DD} - 0.5$	—	V
Output low voltage (high drive) $I_{OL} = 5$ mA	V_{OL}	—	0.5	V
Output high voltage (low drive) $I_{OH} = -2$ mA	V_{OH}	$V_{DD} - 0.5$	—	V
Output low voltage (low drive) $I_{OL} = 2$ mA	V_{OL}	—	0.5	V
Weak internal pull Up device current, tested at V_{IL} Max. ³	I_{APU}	-10	-130	μA
Input Capacitance ⁴ • All input-only pins • All input/output (three-state) pins	C_{in}	— —	7 7	pF

¹ Refer to Table 30 for additional PLL specifications.

² Only for pins: IRQ1, IRQ2, IRQ3, IRQ4, IRQ5, IRQ6, IRQ7, RSTIN_B, RCON_B, PCS0, SCK, I2C_SDA, I2C_SCL, TCLK, TRST_B

³ Refer to Table 13 for pins having internal pull-up devices.

⁴ This parameter is characterized before qualification rather than 100% tested.

2.8 Clock Source Electrical Specifications

Table 30. Oscillator and PLL Electrical Specifications
 $(V_{DD} \text{ and } V_{DDPLL} = 2.7 \text{ to } 3.6 \text{ V}, V_{SS} = V_{SSPLL} = 0 \text{ V})$

Characteristic	Symbol	Min	Max	Unit
Clock Source Frequency Range of EXTAL Frequency Range • Crystal • External ¹	f_{crystal} f_{ext}	1 0	25.0 ² 66.67 or 80	MHz
PLL reference frequency range	$f_{\text{ref_pll}}$	2	10.0	MHz
System frequency ³ • External clock mode • On-chip PLL frequency	f_{sys}	0 $f_{\text{ref}} / 32$	66.67 or 80 ⁴ 66.67 or 80 ⁴	MHz
Loss of reference frequency ^{5, 7}	f_{LOR}	100	1000	kHz
Self clocked mode frequency ⁶	f_{SCM}	1	5	MHz
Crystal start-up time ^{7, 8}	t_{cst}	—	10	ms
EXTAL input high voltage • External reference	V_{IHEXT}	2.0	3.0 ²	V
EXTAL input low voltage • External reference	V_{ILEXT}	V_{SS}	0.8	V
PLL lock time ^{4,9}	t_{lpll}	—	500	μs
Duty cycle of reference ⁴	t_{dc}	40	60	% f_{ref}
Frequency un-LOCK range	f_{UL}	−1.5	1.5	% f_{ref}
Frequency LOCK range	f_{LCK}	−0.75	0.75	% f_{ref}
CLKOUT period jitter ^{4, 5, 10, 11} , measured at f_{SYS} Max • Peak-to-peak (clock edge to clock edge) • Long term (averaged over 2 ms interval)	C_{jitter}	— —	10 .01	% f_{sys}
On-chip oscillator frequency	f_{oco}	7.84	8.16	MHz

¹ In external clock mode, it is possible to run the chip directly from an external clock source without enabling the PLL.

² This value has been updated.

³ All internal registers retain data at 0 Hz.

⁴ Depending on packaging; see the orderable part number summary.

⁵ Loss of Reference Frequency is the reference frequency detected internally, which transitions the PLL into self clocked mode.

⁶ Self clocked mode frequency is the frequency at which the PLL operates when the reference frequency falls below f_{LOR} with default MFD/RFD settings.

⁷ This parameter is characterized before qualification rather than 100% tested.

⁸ Proper PC board layout procedures must be followed to achieve specifications.

⁹ This specification applies to the period required for the PLL to relock after changing the MFD frequency control bits in the synthesizer control register (SYNCR).

¹⁰ Jitter is the average deviation from the programmed frequency measured over the specified interval at maximum f_{sys} . Measurements are made with the device powered by filtered supplies and clocked by a stable external clock signal. Noise injected into the PLL circuitry via V_{DDPLL} and V_{SSPLL} and variation in crystal oscillator frequency increase the C_{jitter} percentage for a given interval.

¹¹ Based on slow system clock of 40 MHz measured at f_{sys} max.

2.9 General Purpose I/O Timing

GPIO can be configured for certain pins of the QSPI, DDR Control, timer, UART, Interrupt and USB interfaces. When in GPIO mode, the timing specification for these pins is given in Table 31 and Figure 6.

The GPIO timing is met under the following load test conditions:

- 50 pF / 50 Ω for high drive
- 25 pF / 25 Ω for low drive

Table 31. GPIO Timing

NUM	Characteristic	Symbol	Min	Max	Unit
G1	CLKOUT High to GPIO Output Valid	t_{CHPOV}	—	10	ns
G2	CLKOUT High to GPIO Output Invalid	t_{CHPOI}	1.5	—	ns
G3	GPIO Input Valid to CLKOUT High	t_{PVCH}	9	—	ns
G4	CLKOUT High to GPIO Input Invalid	t_{CHPI}	1.5	—	ns

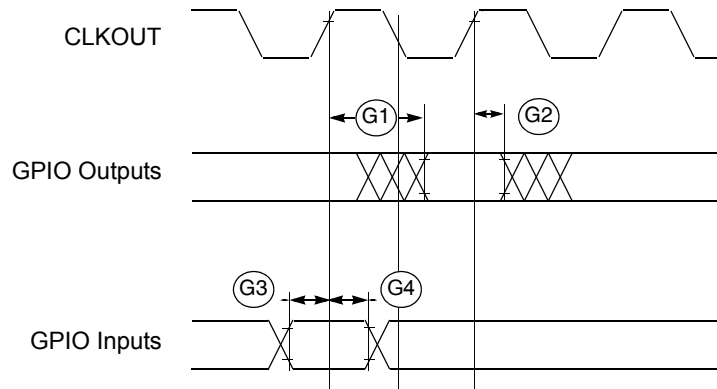


Figure 6. GPIO Timing

2.10 Reset Timing

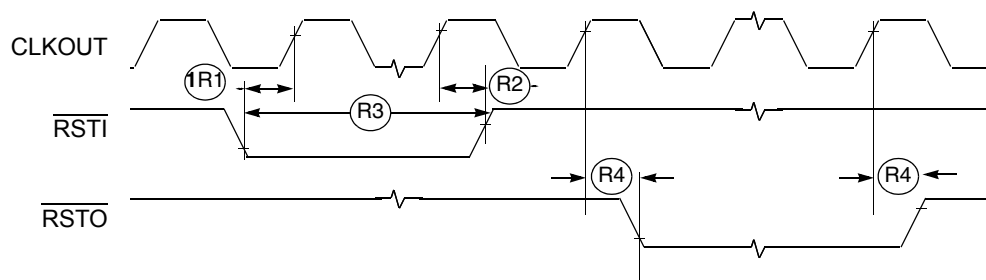
Table 32. Reset and Configuration Override Timing

($V_{DD} = 3.0$ to 3.6 V, $V_{SS} = 0$ V, $T_A = T_L$ to T_H)¹

NUM	Characteristic	Symbol	Min	Max	Unit
R1	$\overline{RSTI}$ input valid to CLKOUT High	t_{RVCH}	9	—	ns
R2	CLKOUT High to $\overline{RSTI}$ Input invalid	t_{CHRI}	1.5	—	ns
R3	$\overline{RSTI}$ input valid time ²	t_{RIVT}	5	—	t_{CYC}
R4	CLKOUT High to $\overline{RSTO}$ Valid	t_{CHROV}	—	10	ns

¹ All AC timing is shown with respect to 50% V_{DD} levels unless otherwise noted.

² During low power STOP, the synchronizers for the $\overline{RSTI}$ input are bypassed and $\overline{RSTI}$ is asserted asynchronously to the system. Thus, $\overline{RSTI}$ must be held a minimum of 100 ns.


Figure 7. $\overline{\text{RSTI}}$ and Configuration Override Timing

2.11 I²C Input/Output Timing Specifications

Table 33 lists specifications for the I²C input timing parameters shown in Figure 8.

Table 33. I²C Input Timing Specifications between I2C_SCL and I2C_SDA

Num	Characteristic	Min	Max	Units
11	Start condition hold time	$2 \times t_{\text{CYC}}$	—	ns
12	Clock low period	$8 \times t_{\text{CYC}}$	—	ns
13	SCL/SDA rise time ($V_{\text{IL}} = 0.5 \text{ V}$ to $V_{\text{IH}} = 2.4 \text{ V}$)	—	1	ms
14	Data hold time	0	—	ns
15	SCL/SDA fall time ($V_{\text{IH}} = 2.4 \text{ V}$ to $V_{\text{IL}} = 0.5 \text{ V}$)	—	1	ms
16	Clock high time	$4 \times t_{\text{CYC}}$	—	ns
17	Data setup time	0	—	ns
18	Start condition setup time (for repeated start condition only)	$2 \times t_{\text{CYC}}$	—	ns
19	Stop condition setup time	$2 \times t_{\text{CYC}}$	—	ns

Table 34 lists specifications for the I²C output timing parameters shown in Figure 8.

Table 34. I²C Output Timing Specifications between I2C_SCL and I2C_SDA

Num	Characteristic	Min	Max	Units
11 ¹	Start condition hold time	$6 \times t_{\text{CYC}}$	—	ns
12 ¹	Clock low period	$10 \times t_{\text{CYC}}$	—	ns
13 ²	I2C_SCL/I2C_SDA rise time ($V_{\text{IL}} = 0.5 \text{ V}$ to $V_{\text{IH}} = 2.4 \text{ V}$)	—	—	μs
14 ¹	Data hold time	$7 \times t_{\text{CYC}}$	—	ns
15 ³	I2C_SCL/I2C_SDA fall time ($V_{\text{IH}} = 2.4 \text{ V}$ to $V_{\text{IL}} = 0.5 \text{ V}$)	—	3	ns
16 ¹	Clock high time	$10 \times t_{\text{CYC}}$	—	ns
17 ¹	Data setup time	$2 \times t_{\text{CYC}}$	—	ns
18 ¹	Start condition setup time (for repeated start condition only)	$20 \times t_{\text{CYC}}$	—	ns
19 ¹	Stop condition setup time	$10 \times t_{\text{CYC}}$	—	ns

Electrical Characteristics

- ¹ Output numbers depend on the value programmed into the IFDR; an IFDR programmed with the maximum frequency (IFDR = 0x20) results in minimum output timings as shown in Table 34. The I²C interface is designed to scale the actual data transition time to move it to the middle of the SCL low period. The actual position is affected by the prescale and division values programmed into the IFDR; however, the numbers given in Table 34 are minimum values.
- ² Because SCL and SDA are open-collector-type outputs, which the processor can only actively drive low, the time SCL or SDA take to reach a high level depends on external signal capacitance and pull-up resistor values.
- ³ Specified at a nominal 50-pF load.

Figure 8 shows timing for the values in Table 33 and Table 34.

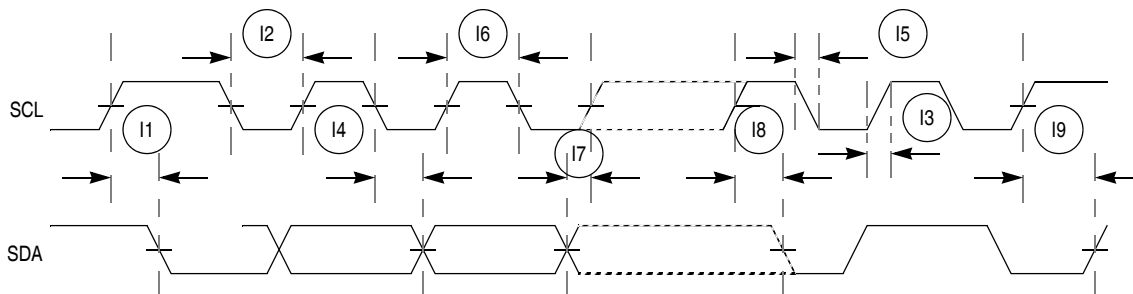


Figure 8. I²C Input/Output Timings

2.12 Analog-to-Digital Converter (ADC) Parameters

Table 35 lists specifications for the analog-to-digital converter.

Table 35. ADC Parameters¹

Name	Characteristic	Min	Typical	Max	Unit
V _{REFL}	Low reference voltage	V _{SS}	—	V _{REFH}	V
V _{REFH}	High reference voltage	V _{REFL}	—	V _{DDA}	V
V _{DDA}	ADC analog supply voltage	3.0	3.3	3.6	V
V _{ADIN}	Input voltages	V _{REFL}	—	V _{REFH}	V
RES	Resolution	12	—	12	Bits
INL	Integral non-linearity (full input signal range) ²	—	±2.5	±3	LSB ³
INL	Integral non-linearity (10% to 90% input signal range) ⁴	—	±2.5	±3	LSB
DNL	Differential non-linearity	—	-1 < DNL < +1	<+1	LSB
Monotonicity		GUARANTEED			
f _{ADIC}	ADC internal clock	0.1	—	5.0	MHz
R _{AD}	Conversion range	V _{REFL}	—	V _{REFH}	V
t _{ADPU}	ADC power-up time ⁵	—	6	13	t _{AIC} cycles ⁶
t _{REC}	Recovery from auto standby	—	0	1	t _{AIC} cycles
t _{ADC}	Conversion time	—	6	—	t _{AIC} cycles
t _{ADS}	Sample time	—	1	—	t _{AIC} cycles
C _{ADI}	Input capacitance	—	See Figure 9	—	pF

Table 35. ADC Parameters¹ (continued)

Name	Characteristic	Min	Typical	Max	Unit
X_{IN}	Input impedance	—	See Figure 9	—	W
I_{ADI}	Input injection current ⁷ , per pin	—	—	3	mA
I_{VREFH}	V_{REFH} current	—	0	—	mA
V_{OFFSET}	Offset voltage internal reference	—	±8	±15	mV
E_{GAIN}	Gain error (transfer path)	.99	1	1.01	—
V_{OFFSET}	Offset voltage external reference	—	±3	9	mV
SNR	Signal-to-noise ratio	—	62 to 66	—	dB
THD	Total harmonic distortion	—	–75	—	dB
SFDR	Spurious free dynamic range	—	67 to 70.3	—	dB
SINAD	Signal-to-noise plus distortion	—	61 to 63.9	—	dB
ENOB	Effective number of bits	9.1	10.6	—	Bits

¹ All measurements are made at $V_{DD} = 3.3V$, $V_{REFH} = 3.3V$, and $V_{REFL} = \text{ground}$

² INL measured from $V_{IN} = V_{BFFL}$ to $V_{IN} = V_{BFFH}$

³ LSB = Least Significant Bit

⁴ INL measured from $V_{IN} = 0.1V_{REFH}$ to $V_{IN} = 0.9V_{REFH}$

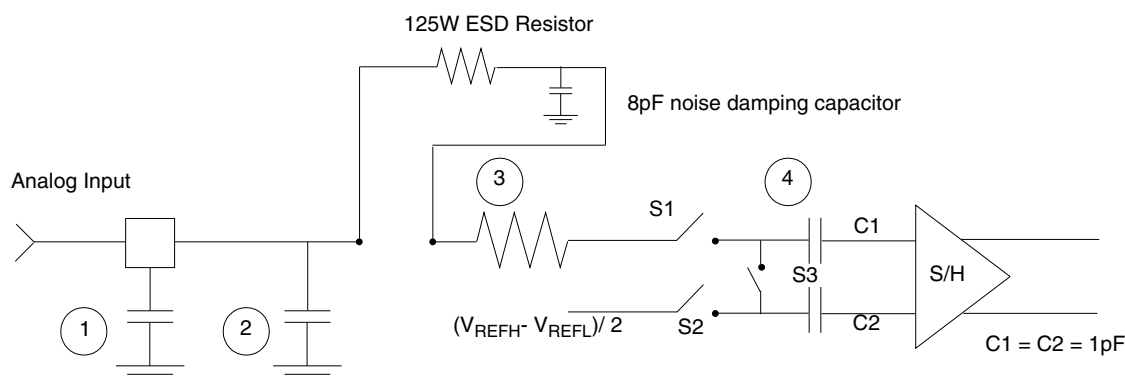
⁵ Includes power-up of ADC and V_{BEE}

⁶ ADC clock cycles

⁷ Current that can be injected or sourced from an unselected ADC signal input without impacting the performance of the ADC

2.13 Equivalent Circuit for ADC Inputs

Figure 9 shows the ADC input circuit during sample and hold. S1 and S2 are always open/closed at the same time that S3 is closed/open. When S1/S2 are closed & S3 is open, one input of the sample and hold circuit moves to $(V_{REFH}-V_{REFL})/2$, while the other charges to the analog input voltage. When the switches are flipped, the charge on C1 and C2 are averaged via S3, with the result that a single-ended analog input is switched to a differential voltage centered about $(V_{REFH}-V_{REFL})/2$. The switches switch on every cycle of the ADC clock (open one-half ADC clock, closed one-half ADC clock). There are additional capacitances associated with the analog input pad, routing, etc., but these do not filter into the S/H output voltage, as S1 provides isolation during the charge-sharing phase. One aspect of this circuit is that there is an on-going input current, which is a function of the analog input voltage, V_{REF} and the ADC clock frequency.



1. Parasitic capacitance due to package, pin-to-pin and pin-to-package base coupling; 1.8pF
2. Parasitic capacitance due to the chip bond pad, ESD protection devices and signal routing; 2.04pF

Electrical Characteristics

3. Equivalent resistance for the channel select mux; 100 Ω s
4. Sampling capacitor at the sample and hold circuit. Capacitor C1 is normally disconnected from the input and is only connected to it at sampling time; 1.4pF
5. Equivalent input impedance, when the input is selected =
$$\frac{1}{(\text{ADC Clock Rate}) \times (1.4 \times 10^{-12})}$$

Figure 9. Equivalent Circuit for A/D Loading

2.14 DMA Timers Timing Specifications

Table 36 lists timer module AC timings.

Table 36. Timer Module AC Timing Specifications

Name	Characteristic ¹	Min	Max	Unit
T1	DTIN0 / DTIN1 / DTIN2 / DTIN3 cycle time	$3 \times t_{CYC}$	—	ns
T2	DTIN0 / DTIN1 / DTIN2 / DTIN3 pulse width	$1 \times t_{CYC}$	—	ns

¹ All timing references to CLKOUT are given to its rising edge.

2.15 QSPI Electrical Specifications

Table 37 lists QSPI timings.

Table 37. QSPI Modules AC Timing Specifications

Name	Characteristic	Min	Max	Unit
QS1	QSPI_CS[3:0] to QSPI_CLK	1	510	t_{CYC}
QS2	QSPI_CLK high to QSPI_DOUT valid	—	10	ns
QS3	QSPI_CLK high to QSPI_DOUT invalid (Output hold)	2	—	ns
QS4	QSPI_DIN to QSPI_CLK (Input setup)	9	—	ns
QS5	QSPI_DIN to QSPI_CLK (Input hold)	9	—	ns

The values in Table 37 correspond to Figure 10.

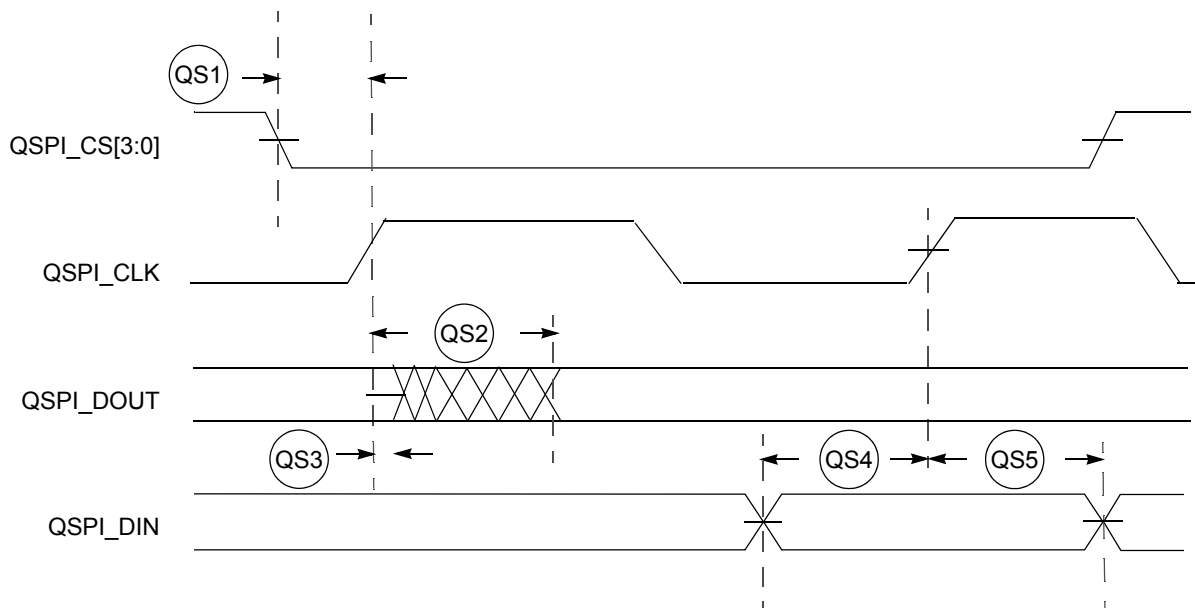


Figure 10. QSPI Timing

2.16 JTAG and Boundary Scan Timing

Table 38. JTAG and Boundary Scan Timing

Num	Characteristics ¹	Symbol	Min	Max	Unit
J1	TCLK frequency of operation	f_{JCYC}	DC	1/4	$f_{sys}/2$
J2	TCLK cycle period	t_{JCYC}	$4 \times t_{CYC}$	—	ns
J3	TCLK clock pulse width	t_{JCW}	26	—	ns
J4	TCLK rise and fall times	t_{JCRF}	0	3	ns
J5	Boundary scan input data setup time to TCLK rise	t_{BSDST}	4	—	ns
J6	Boundary scan input data hold time after TCLK rise	t_{BSDHT}	26	—	ns
J7	TCLK low to boundary scan output data valid	t_{BSDV}	0	33	ns
J8	TCLK low to boundary scan output high Z	t_{BSDZ}	0	33	ns
J9	TMS, TDI input data setup time to TCLK rise	t_{TAPBST}	4	—	ns
J10	TMS, TDI Input data hold time after TCLK rise	t_{TAPBHT}	10	—	ns
J11	TCLK low to TDO data valid	t_{TDODV}	0	26	ns
J12	TCLK low to TDO high Z	t_{TDODZ}	0	8	ns
J13	$\overline{TRST}$ assert time	t_{TRSTAT}	100	—	ns
J14	$\overline{TRST}$ setup time (negation) to TCLK high	t_{TRSTST}	10	—	ns

¹ JTAG_EN is expected to be a static signal. Hence, it is not associated with any timing.

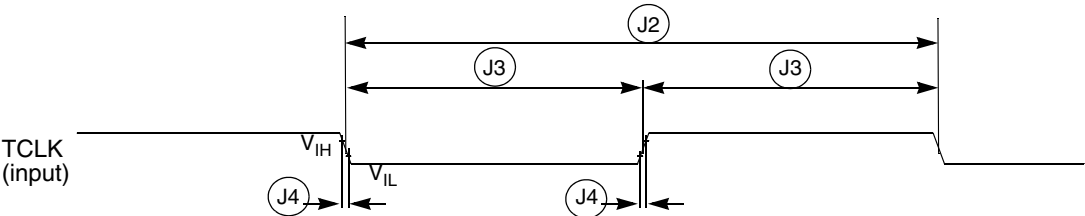


Figure 11. Test Clock Input Timing

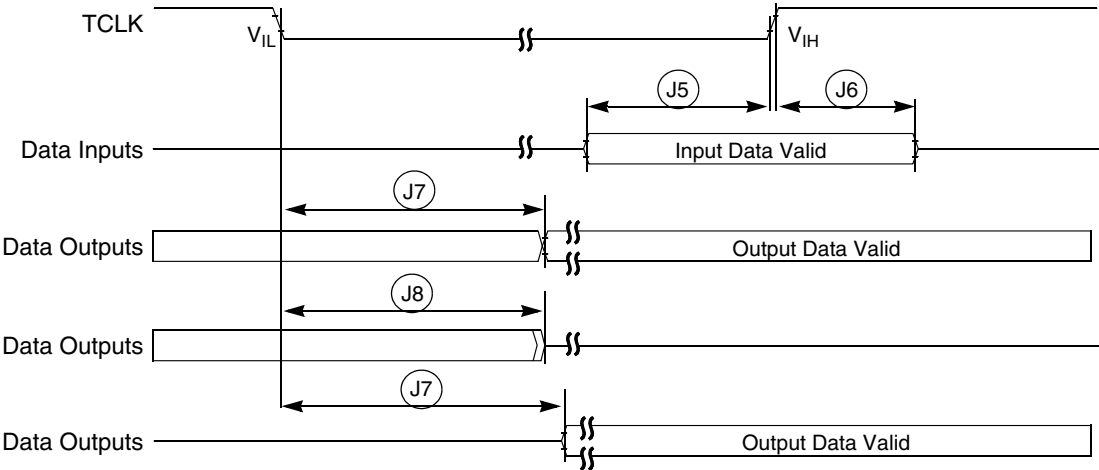


Figure 12. Boundary Scan (JTAG) Timing

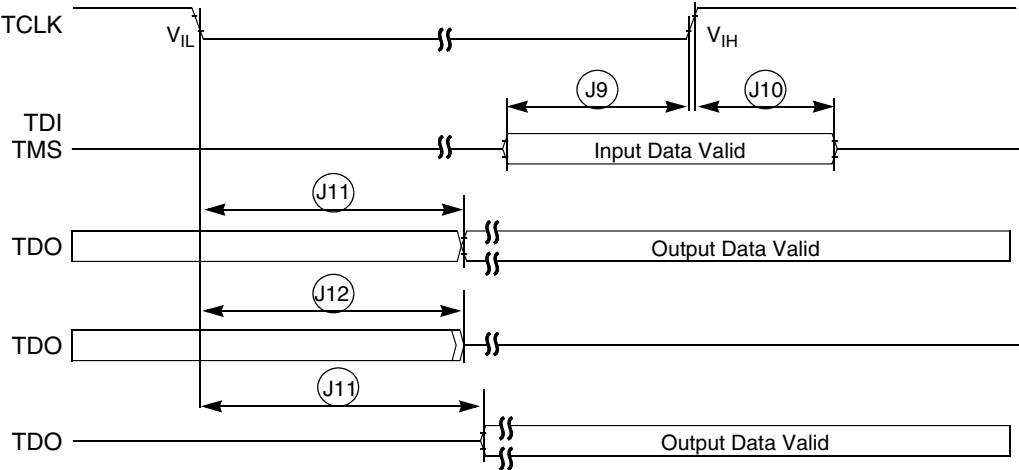


Figure 13. Test Access Port Timing

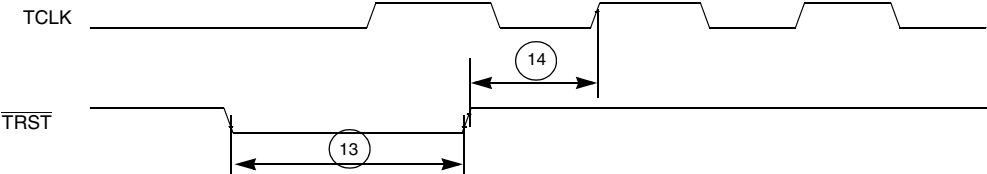


Figure 14. TRST Timing

2.17 Debug AC Timing Specifications

Table 39 lists specifications for the debug AC timing parameters shown in Figure 16.

Table 39. Debug AC Timing Specification

Num	Characteristic	66/80 MHz		Units
		Min	Max	
D1	PST, DDATA to CLKOUT setup	4	—	ns
D2	CLKOUT to PST, DDATA hold	1.5	—	ns
D3	DSI-to-DSCLK setup	$1 \times t_{CYC}$	—	ns
D4 ¹	DSCLK-to-DSO hold	$4 \times t_{CYC}$	—	ns
D5	DSCLK cycle time	$5 \times t_{CYC}$	—	ns
D6	$\overline{BKPT}$ input data setup time to CLKOUT rise	4	—	ns
D7	$\overline{BKPT}$ input data hold time to CLKOUT rise	1.5	—	ns
D8	CLKOUT high to $\overline{BKPT}$ high Z	0.0	10.0	ns

¹ DSCLK and DSI are synchronized internally. D4 is measured from the synchronized DSCLK input relative to the rising edge of CLKOUT.

Figure 15 shows real-time trace timing for the values in Table 39.

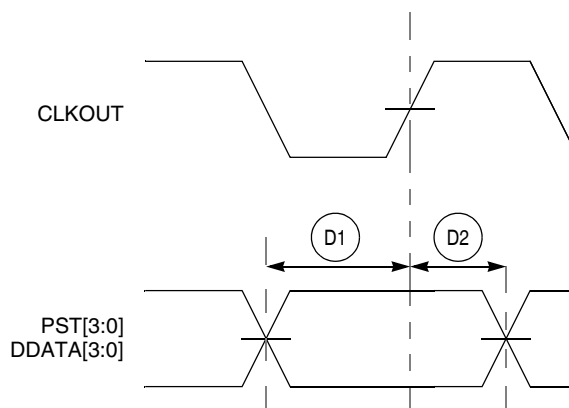


Figure 15. Real-Time Trace AC Timing

Figure 16 shows BDM serial port AC timing for the values in Table 39.

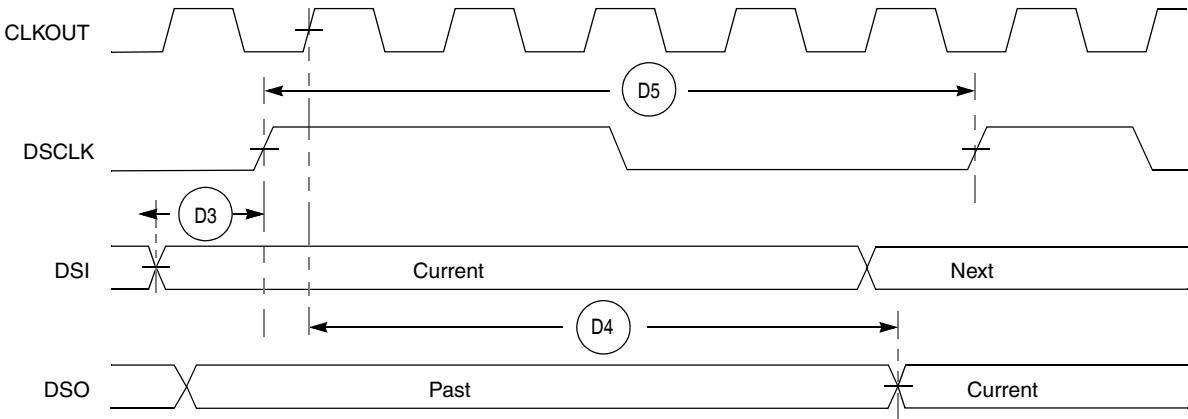
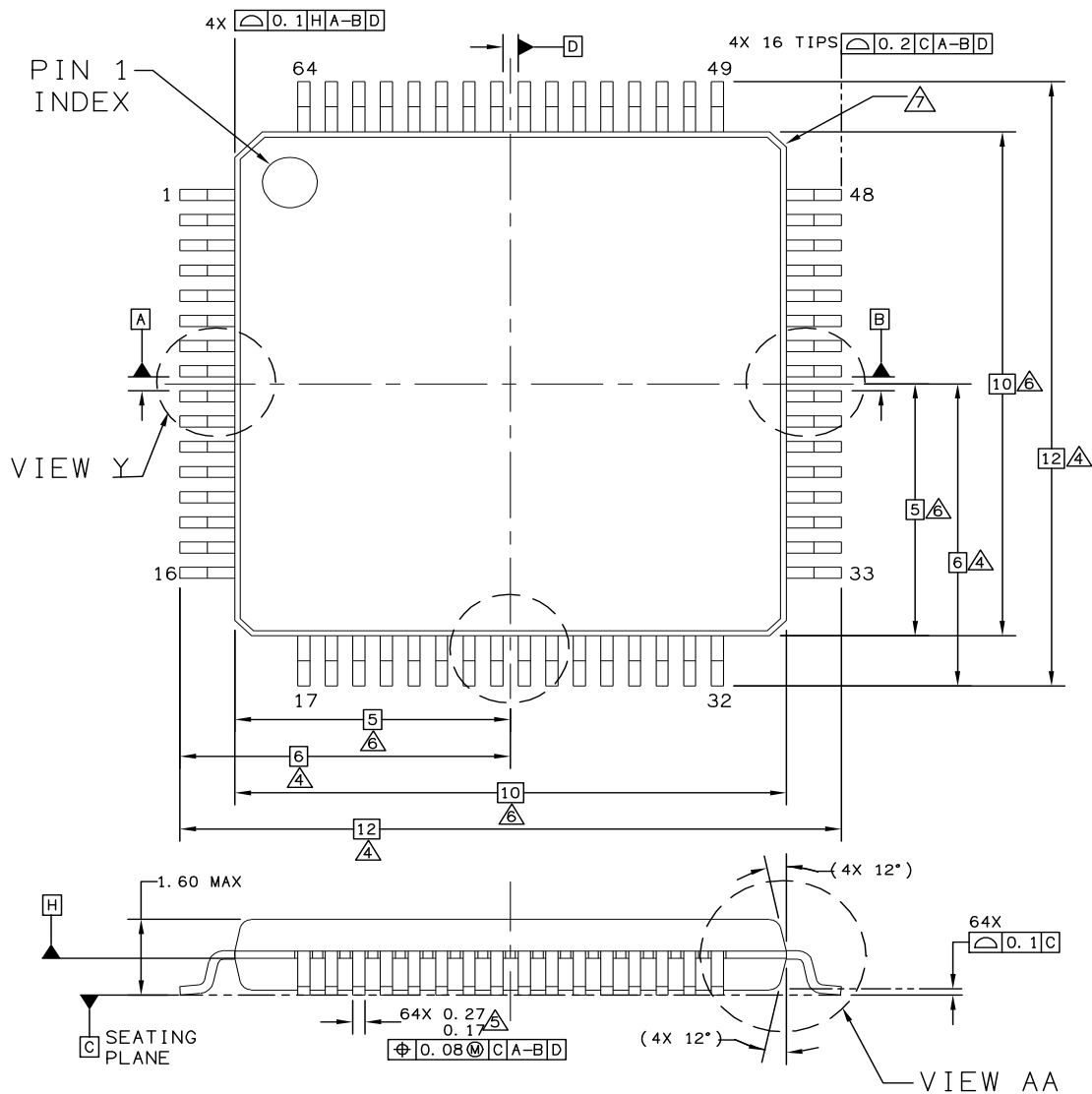


Figure 16. BDM Serial Port AC Timing

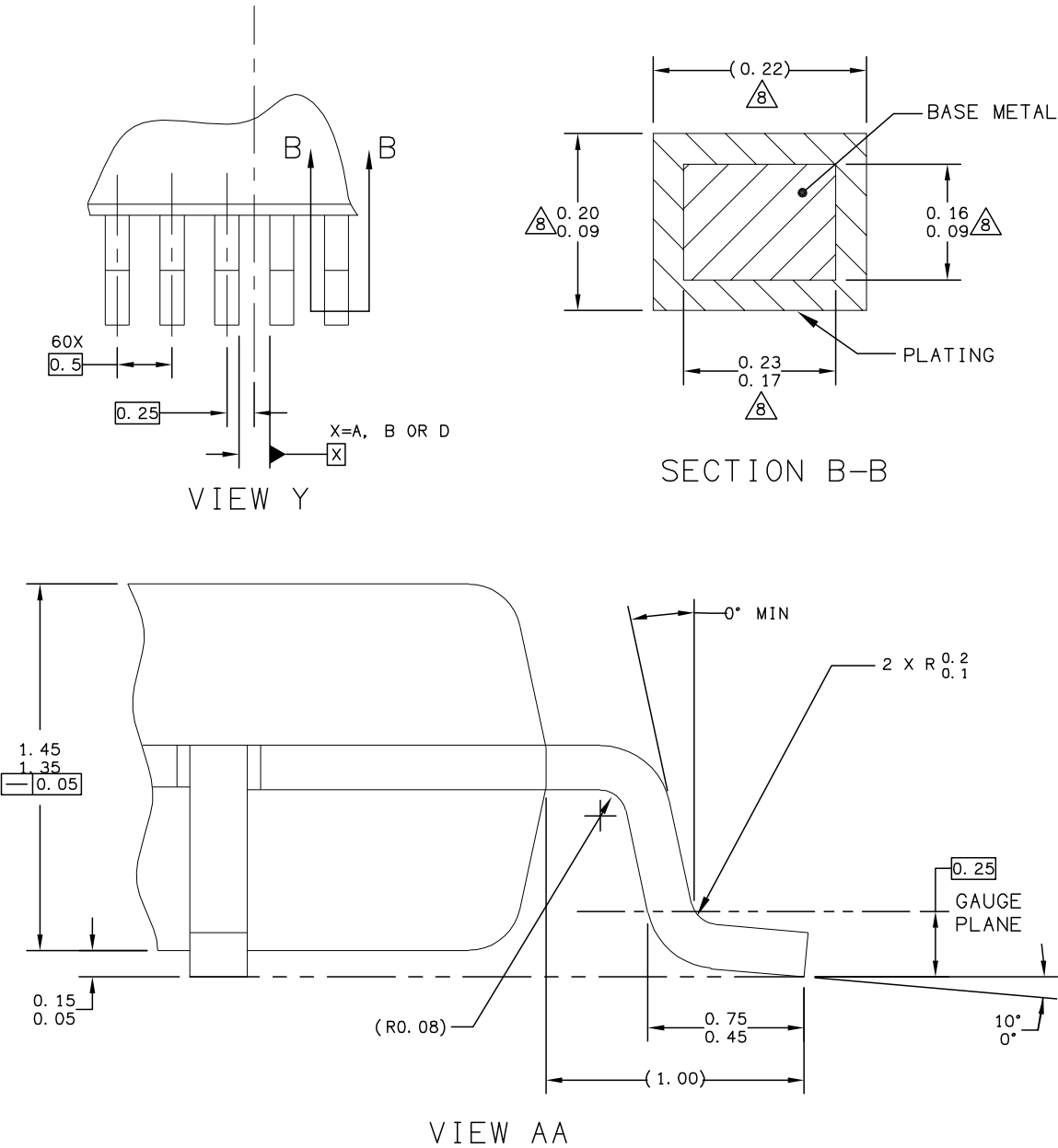
3 Mechanical Outline Drawings

This section describes the physical properties of the device and its derivatives.

3.1 64-pin LQFP Package



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TITLE: 64LD LQFP, 10 X 10 X 1.4 PKG, 0.5 PITCH, CASE OUTLINE		DOCUMENT NO: 98ASS23234W	REV: D
		CASE NUMBER: 840F-02	06 APR 2005
		STANDARD: JEDEC MS-026 BCD	

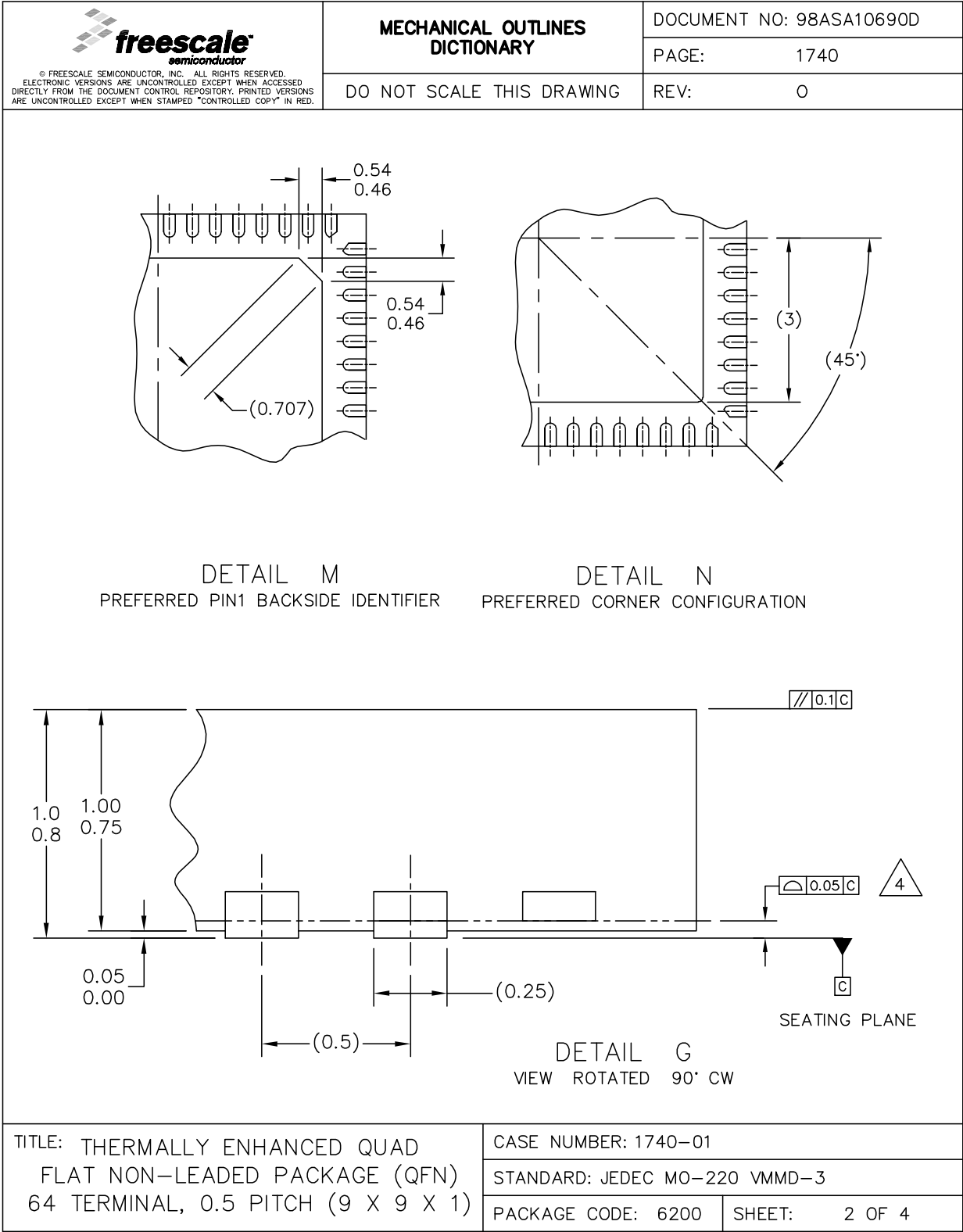


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TITLE: 64LD LQFP, 10 X 10 X 1.4 PKG, 0.5 PITCH, CASE OUTLINE	DOCUMENT NO: 98ASS23234W	REV: D
	CASE NUMBER: 840F-02	06 APR 2005
	STANDARD: JEDEC MS-026 BCD	

NOTES:

1. DIMENSIONS ARE IN MILLIMETERS.
2. DIMENSIONING AND TOLERANCING PER ASME Y14.5M-1994.
3. DATUMS A, B AND D TO BE DETERMINED AT DATUM PLANE H.
- △4. DIMENSIONS TO BE DETERMINED AT SEATING PLANE C.
- △5. THIS DIMENSION DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL NOT CAUSE THE LEAD WIDTH TO EXCEED THE UPPER LIMIT BY MORE THAN 0.08 mm AT MAXIMUM MATERIAL CONDITION. DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OR THE FOOT. MINIMUM SPACE BETWEEN PROTRUSION AND ADJACENT LEAD SHALL NOT BE LESS THAN 0.07 mm.
- △6. THIS DIMENSION DOES NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS 0.25 mm PER SIDE. THIS DIMENSION IS MAXIMUM PLASTIC BODY SIZE DIMENSION INCLUDING MOLD MISMATCH.
- △7. EXACT SHAPE OF EACH CORNER IS OPTIONAL.
- △8. THESE DIMENSIONS APPLY TO THE FLAT SECTION OF THE LEAD BETWEEN 0.1 mm AND 0.25 mm FROM THE LEAD TIP.

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TITLE: 64LD LQFP, 10 X 10 X 1.4 PKG, 0.5 PITCH, CASE OUTLINE	DOCUMENT NO: 98ASS23234W		REV: D
	CASE NUMBER: 840F-02		06 APR 2005
	STANDARD: JEDEC MS-026 BCD		



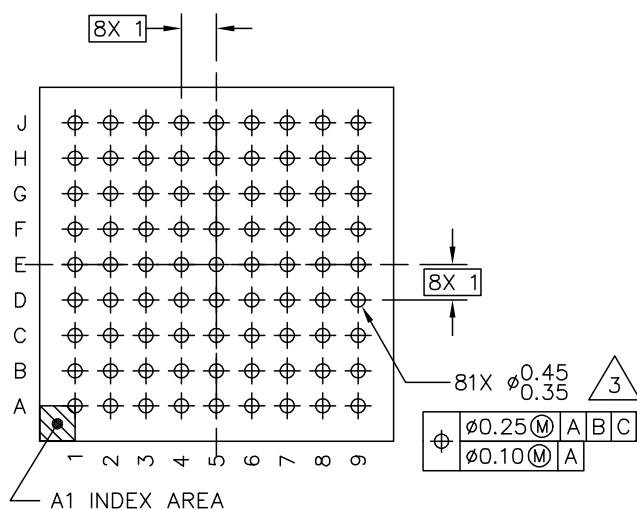
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			PAGE:	1740
	DO NOT SCALE THIS DRAWING		REV:	0
NOTES: 1. ALL DIMENSIONS ARE IN MILLIMETERS. 2. INTERPRET DIMENSIONS AND TOLERANCES PER ASME Y14.5M–1994. 3. THE COMPLETE JEDEC DESIGNATOR FOR THIS PACKAGE IS: HF–PQFN. 4. COPLANARITY APPLIES TO LEADS, CORNER LEADS AND DIE ATTACH PAD. 5. MIN METAL GAP SHOULD BE 0.2MM.				

Mechanical Outline Drawings

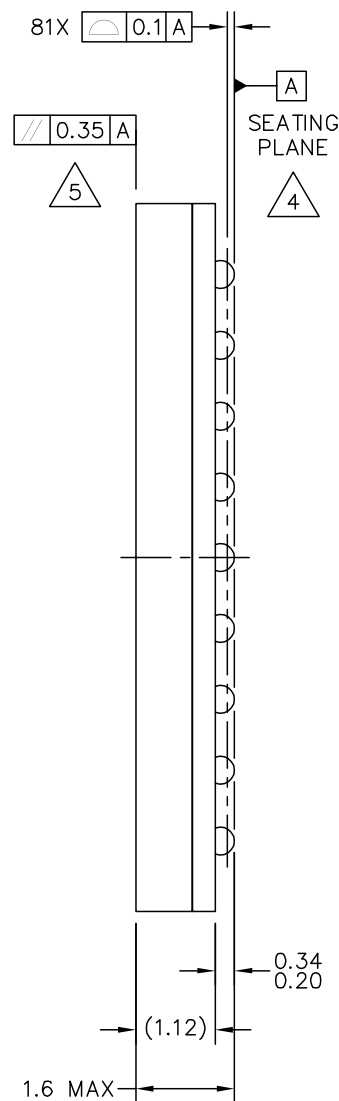
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				PAGE: 1740	
				REV: 0	
LTR	ORIGINATOR	REVISIONS		DRAFTER	DATE
0	ERIC TRIPLETT	RELEASED FOR PRODUCTION		TAYLOR LIU	27JUL2005
TITLE: THERMALLY ENHANCED QUAD FLAT NON-LEADED PACKAGE (QFN) 64 TERMINAL, 0.5 PITCH (9 X 9 X 1)			CASE NUMBER: 1740-01		
			STANDARD: JEDEC MO-220 VMMD-3		
			PACKAGE CODE: 6200	SHEET:	4 OF 4

Figure 1 is a schematic diagram of a square grid. The grid is divided into four quadrants by dashed lines. The top-left quadrant is shaded with diagonal lines and labeled "A1 INDEX AREA" with an arrow. The top edge is labeled "10" and "B". The right edge is labeled "C" and "10". The bottom edge is labeled "4X" and "0.2".

TOP VIEW



BOTTOM VIEW



SIDE VIEW

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TITLE: PBGA, LOW PROFILE, 81 I/O, 10 X 10 PKG, 1 MM PITCH (MAP)		DOCUMENT NO: 98ASA10670D		REV: 0	
		CASE NUMBER: 1662-01		04 FEB 2005	
		STANDARD: NON-JEDEC			

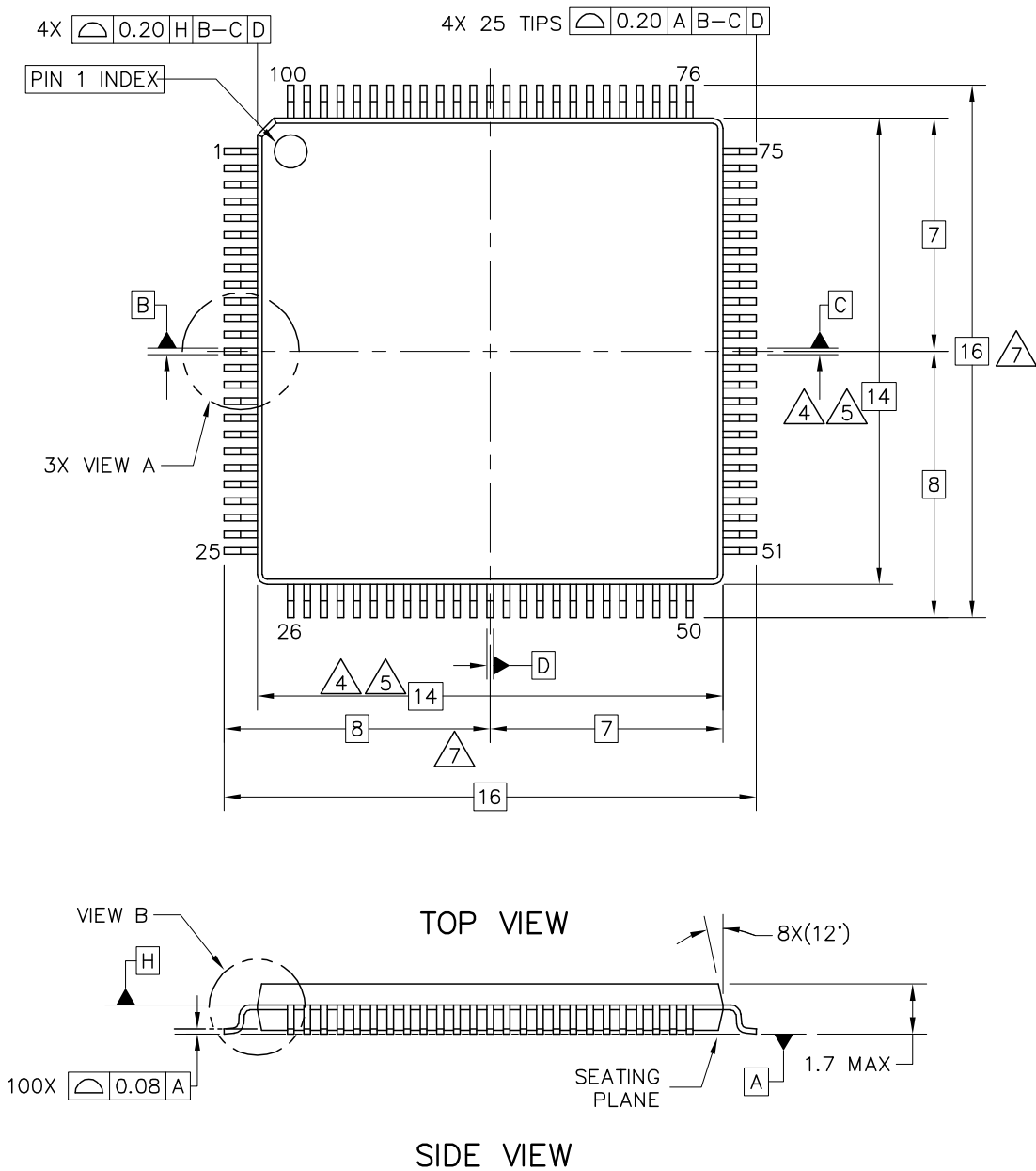
Mechanical Outline Drawings

NOTES:

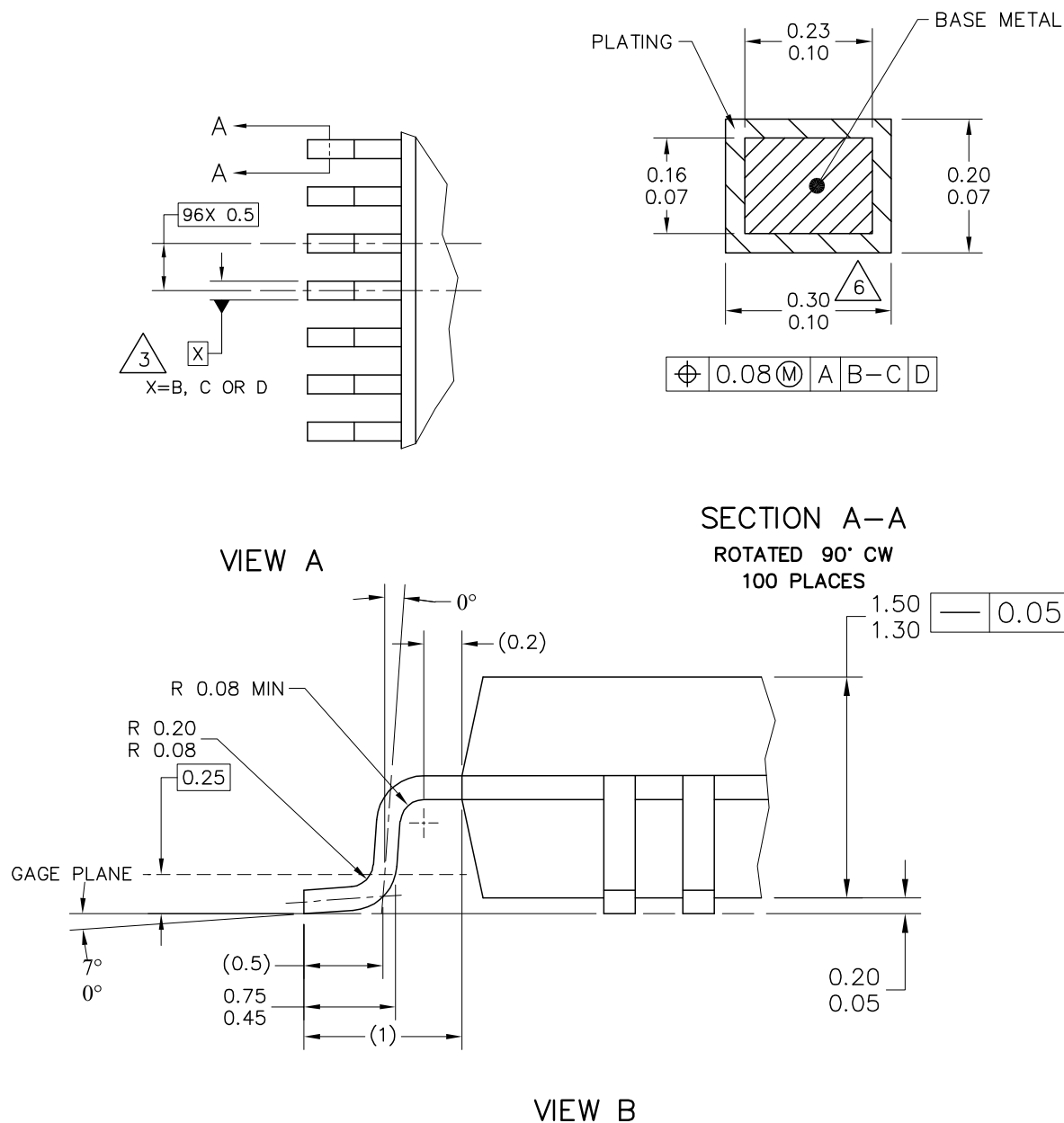
1. ALL DIMENSIONS IN MILLIMETERS.
2. DIMENSIONING AND TOLERANCING PER ASME Y14.5M-1994.
3. MAXIMUM SOLDER BALL DIAMETER MEASURED PARALLEL TO DATUM A.
4. DATUM A, THE SEATING PLANE, IS DETERMINED BY THE SPHERICAL CROWNS OF THE SOLDER BALLS.
5. PARALLELISM MEASUREMENT SHALL EXCLUDE ANY EFFECT OF MARK ON TOP SURFACE OF PACKAGE.

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TITLE: PBGA, LOW PROFILE, 81 I/O, 10 X 10 PKG, 1 MM PITCH (MAP)	DOCUMENT NO: 98ASA10670D		REV: 0
	CASE NUMBER: 1662-01		04 FEB 2005
	STANDARD: NON-JEDEC		

3.3 100-pin LQFP Package



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TITLE: 100 LEAD LQFP 14 X 14, 0.5 PITCH, 1.4 THICK			DOCUMENT NO: 98ASS23308W		REV: G
			CASE NUMBER: 983-03		07 APR 2005
			STANDARD: NON-JEDEC		



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TITLE: 100 LEAD LQFP 14 X 14, 0.5 PITCH, 1.4 THICK			DOCUMENT NO: 98ASS23308W		REV: G
			CASE NUMBER: 983-03		07 APR 2005
			STANDARD: NON-JEDEC		

4 Revision History

Table 40. Revision History

Revision	Description
2	• Formatting, layout, spelling, and grammar corrections. • Removed the “Preliminary” label. • Added missing current consumption data (Section 2.2). • Added revision history. • Corrected signal names in block diagram to match those in the signal description table. • Added an entry for standby voltage (V_{STBY}) to the “DC electrical specifications” table. • Deleted the PSTCLK cycle time row in the “Debug AC timing specifications” table. • Changed the frequency above the “Min” and “Max” column headings in the “Debug AC timing specifications” table (was 166 MHz, is 66/80 MHz). • Added the following signals to the “Pin functions by primary and alternate purpose” table (alternates to IRQ1-6, respectively): USB_ALT_CLK, USB_SESSVLD, USB_SESEND, USB_PULLUP, USB_VBUSVLD, and USB_ID. • Changed the minimum value for SNR, THD, SFDR, and SINAD in the “ADC parameters” table (was TBD, is “—”). • Added values for I_{OH} and I_{OL} to the “DC electrical specifications” table. • Added load test condition information to the “General Purpose I/O Timing” section. • Synchronized the “Pin Functions by Primary and Alternate Purpose” table in this document and the reference manual. • Added a specification for V_{DDUSB} to the “Absolute maximum ratings” table. • Added specifications for V_{LVD} and V_{LVDHYS} to the “DC electrical specifications” table. • Deleted entries for the nonexistent 64 QFN package from the “Thermal Resistances” table.
3	• Updated Table 7 to reflect orderable part numbers.
4	• Updated Clock generation features • Updated Table: Clocking Modes and added appropriate footnote • In Table: CLock Source Electrical Specifications, updated the following values: • fcrystal, fext, freq_pll, EXTAL input high voltage (External reference)

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