THE DATASHEET OF

MC68HC705L5FUE

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HC05L5GRS/D
REV. 2.0

68HC05L5
68HC705L5

General Release Specification

July 9, 1998

Freescale Semiconductor, Inc.

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Section 1. General Description

1.1 Contents

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1.2 Introduction

The MC68HC05L5 is an 80-pin microcontroller unit (MCU) with highly sophisticated on-chip peripheral functions. The memory map includes 8 Kbytes of user ROM and 256 bytes of static RAM. The MCU has five parallel ports: A, B, C, D, and E. The MC68HC05L5 includes a timebase circuit, 8- and 16-bit timers, a computer operating properly (COP) watchdog timer, liquid crystal display (LCD) drivers, and a simple serial peripheral interface (SSPI).

1.3 Features

Features of the MC68HC05L5 MCU include:

- Low-cost HC05 core
- 8,208 bytes of user ROM and 256 bytes of user static RAM
- General-purpose data pins:
  - 14 bidirectional pins
  - 10 input/ouptut-only pins
  - 15 output-only pins, including 8-bit key wakeup interrupts
- Pullup resistors options
- Open-drain outputs options
- Two interrupt request (IRQ) inputs
- 16-bit timer with input capture and output compare (timer 1)
- 8-bit event counter/modulus clock divider (timer 2)
- Simple serial peripheral interface (SSPI)
- LCD drivers — 1-to-4 backplane drivers x 27-to-39 frontplane drivers
- On-chip timebase circuits with COP watchdog timer and timebase interrupts
- Dual oscillators and selectable system clock frequency
- Power-saving stop mode and wait mode
- 80-pin quad flat pack (QFP) package

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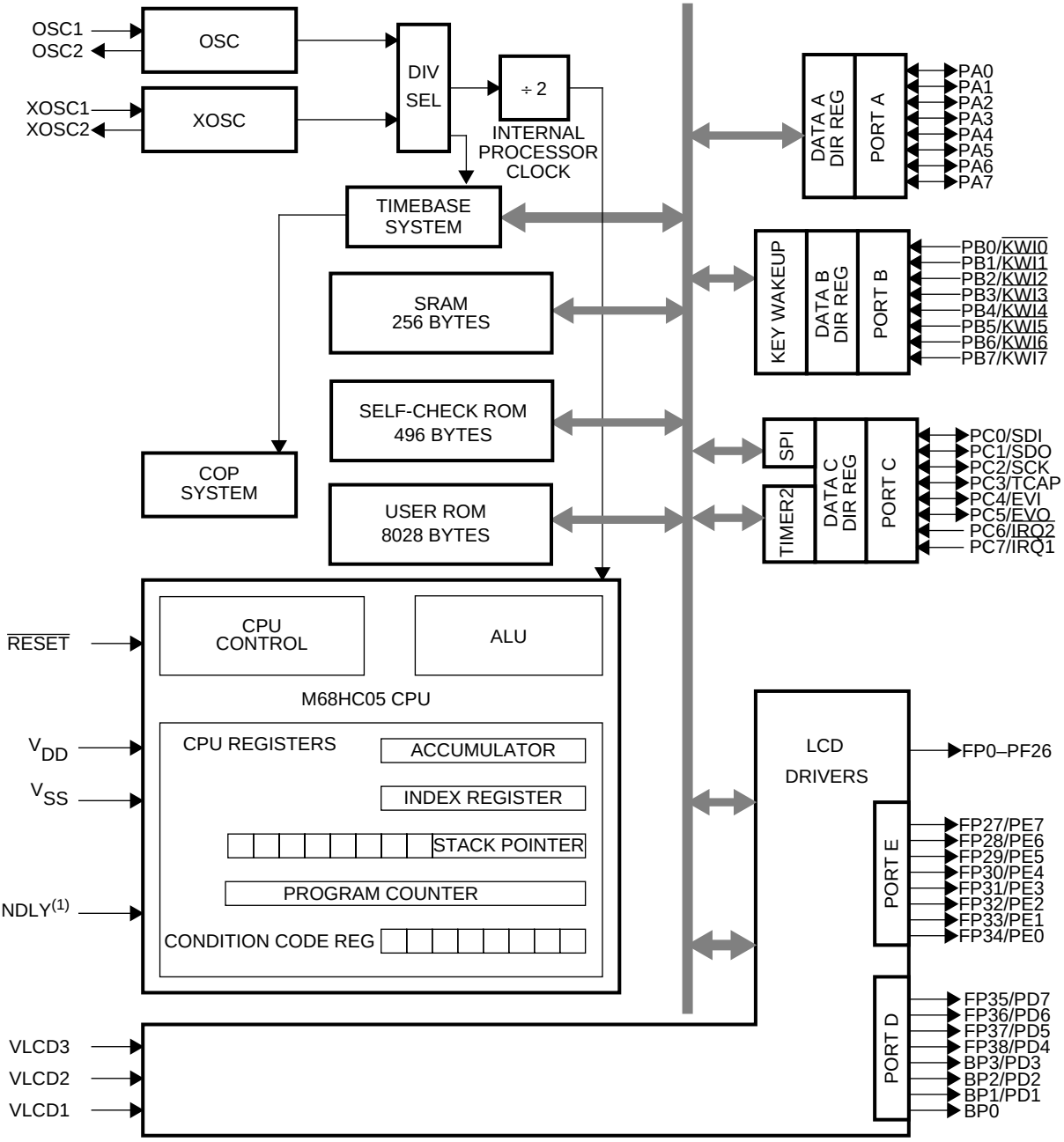
1.4 MCU Structure

Figure 1-1 shows the structure of the MC68HC05L5 MCU.



Note 1. The NDLY pin should be connected to V_{DD}.

Figure 1-1. Block Diagram

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NOTE: *A line over a signal name indicates an active low signal. For example, $\overline{RESET}$ is active low.*

1.5 Mask Options

The three mask options on the MC68HC05L5 are:

1. RSTR: $\overline{\text{RESET}}$ pin pullup resistor
2. OSCR: OSC feedback resistor
3. XOSCR: XOSC feedback/damping resistor

See **2.5.6 Mask Option Status Register**.

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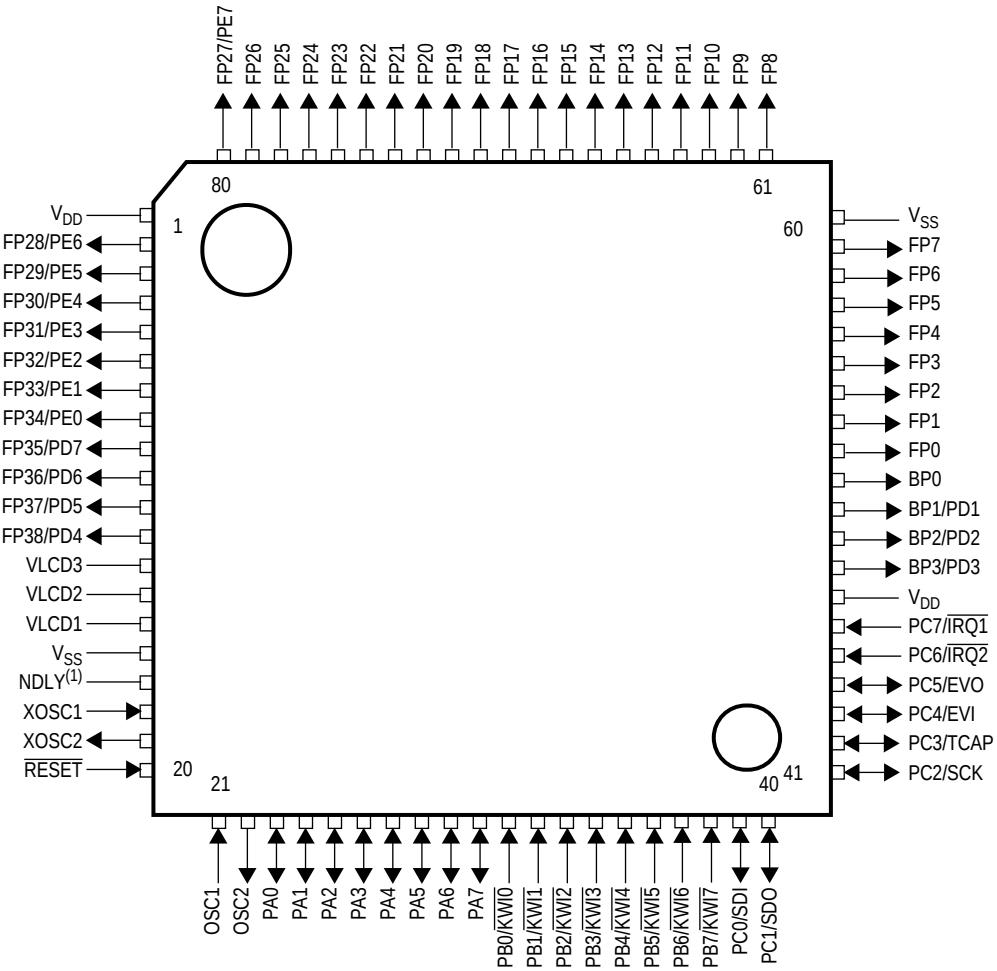
1.6 Functional Pin Description

The MC68HC05L5 is available in an 80-pin QFP. The pin assignment is shown in **Figure 1-2**.



Note 1. The NDLY pin should be connected to V_{DD}.

Figure 1-2. Pin Assignment for Single-Chip Mode

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General Description

Table 1-1. Pin Configuration

Pin Number	SCM, Self-Check	I/O
23	PA0	I/O
24	PA1	I/O
25	PA2	I/O
26	PA3	I/O
27	PA4	I/O
28	PA5	I/O
29	PA6	I/O
30	PA7	I/O
31	PB0/$\overline{KWI0}$	I
32	PB1/$\overline{KWI1}$	I
33	PB2/$\overline{KWI2}$	I
34	PB3/$\overline{KWI3}$	I
35	PB4/$\overline{KWI4}$	I
36	PB5/$\overline{KWI5}$	I
37	PB6/$\overline{KWI6}$	I
38	PB7/$\overline{KWI7}$	I
39	PC0/SDI	I/O
40	PC1/SDO	I/O
41	PC2/SCK	I/O
42	PC3/TCAP	I/O
43	PC4/EVI	I/O
44	PC5/EVO	I/O
45	PC6/$\overline{IRQ2}$	I
46	PC7/$\overline{IRQ1}$	I
17	NDLY(1)	I
47	V_{DD}	I
1	V_{DD}	I
60	V_{SS}	O
16	V_{SS}	O
21	OSC1	I
22	OSC2	O
18	XOSC1	I
19	XOSC2	O
15	VLCD1	I
14	VLCD2	I
13	VLCD3	I
48	BP3/PD3	O
49	BP2/PD2	O
50	BP1/PD1	O
51	BP0	O

Pin Number	SCM, Self-Check	I/O
52	FP0	O
53	FP1	O
54	FP2	O
55	FP3	O
56	FP4	O
57	FP5	O
58	FP6	O
59	FP7	O
61	FP8	O
62	FP9	O
63	FP10	O
64	FP11	O
65	FP12	O
66	FP13	O
67	FP14	O
68	FP15	O
69	FP16	O
70	FP17	O
71	FP18	O
72	FP19	O
73	FP20	O
74	FP21	O
75	FP22	O
76	FP23	O
77	FP24	O
78	FP25	O
79	FP26	O
80	FP27/PE7	O
2	FP28/PE6	O
3	FP29/PE5	O
4	FP30/PE4	O
5	FP31/PE3	O
6	FP32/PE2	O
7	FP33/PE1	O
8	FP34/PE0	O
9	FP35/PD7	O
10	FP36/PD6	O
11	FP37/PD5	O
12	FP38/PD4	O

Note 1.The NDLY pin should be connected to V_{DD}.

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1.6.1 V_{DD} and V_{SS}

Power is supplied to the MCU through V_{DD} and V_{SS}. V_{DD} is the positive supply, and V_{SS} is ground. The MCU operates from a single power supply. Very fast signal transitions occur on the MCU pins. The short rise and fall times place very high short-duration current demands on the power supply. To prevent noise problems, special care should be taken to provide good power supply bypassing at the MCU by using bypass capacitors with good high-frequency characteristics that are positioned as close to the MCU as possible. Bypassing requirements vary, depending on how heavily the MCU pins are loaded.

1.6.2 OSC1 and OSC2

The OSC1 and OSC2 pins are the connections for the 2-pin on-chip oscillator. The OSC1 and OSC2 pins can accept:

- A crystal as shown in **Figure 1-3 (a)**
- An external clock signal as shown in **Figure 1-3 (b)**

The frequency, f_{OSC}, of the oscillator or external clock source is divided by 64 to produce the internal operating frequency, f_{OP}, by default.

1.6.2.1 Crystal or Ceramic Resonator

The circuit in **Figure 1-3 (a)** shows a typical 2-pin oscillator circuit for an AT-cut, parallel resonant crystal. The crystal manufacturer's recommendations should be followed, as the crystal parameters determine the external component values required to provide maximum stability and reliable startup. The load capacitance values used in the oscillator circuit design should include all stray capacitances. The crystal and components should be mounted as close as possible to the pins for startup stabilization and to minimize output distortion. An internal startup feedback resistor of R_{OF} between OSC1 and OSC2 may be selected as a mask option for MC68HC05L5. Typical R_{OF} resistor value is 2 MΩ.

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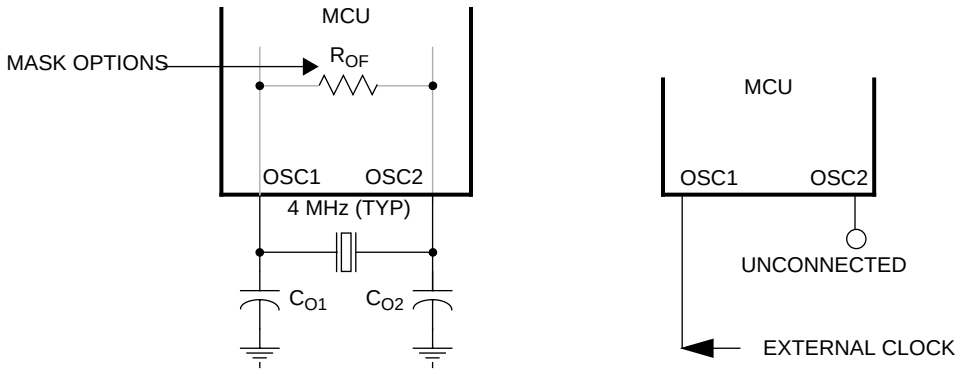

(a) Crystal Connections

(b) External Clock Source Connection

Figure 1-3. Oscillator Connections

1.6.2.2 External Clock

An external clock from another CMOS-compatible device can be connected to the OSC1 input, with the OSC2 input not connected, as shown in **Figure 1-3**. This configuration is possible regardless of how the oscillator is set up.

1.6.3 XOSC1 and XOSC2

The XOSC1 and XOSC2 pins are the connections for the 2-pin on-chip oscillator. The XOSC1 and XOSC2 pins can accept:

- A crystal as shown in **Figure 1-4 (a)**
- An external clock signal as shown in **Figure 1-4 (b)**

The frequency, f_{OSC}, of the oscillator or external clock source is divided by two to produce the internal operating frequency, f_{OP}, if selected by SYS1–SYS0 bits.

When XOSC is not used, the XOSC1 pin must be connected to the $\overline{\text{RESET}}$ pin to assure proper initialization of the clock circuitry. XOSC2 pin should remain unconnected.

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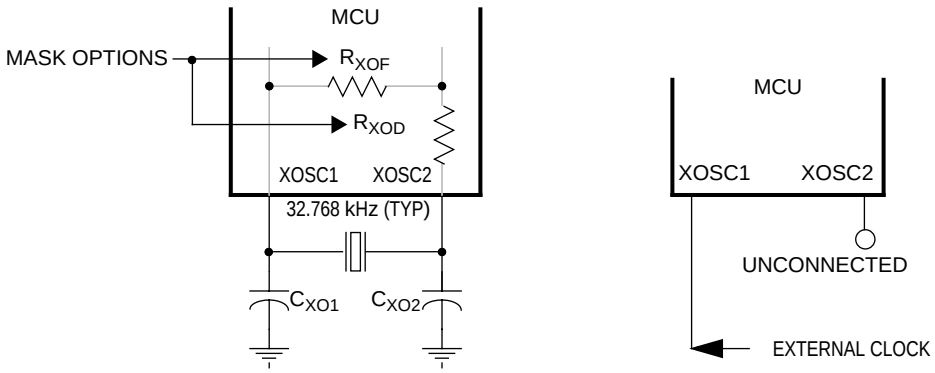
1.6.3.1 Crystal Resonator

The circuit in **Figure 1-4 (a)** shows a typical 2-pin oscillator circuit for an AT-cut, parallel resonant crystal. The crystal manufacturer's recommendations should be followed, as the crystal parameters determine the external component values required to provide maximum stability and reliable startup. The load capacitance values used in the oscillator circuit design should include all stray capacitances. The crystal and components should be mounted as close as possible to the pins for startup stabilization and to minimize output distortion. An internal startup feedback resistor of R_{XOF} between XOSC1 and XOSC2 and a damping resistor of R_{XOD} in series to XOSC2 may be selected as a mask option. Typical R_{XOF} resistor value is 5.5 MΩ, and R_{XOD} resistor value is 320 kΩ.



(a) Crystal Connections

(b) External Clock Source Connection

Figure 1-4. Oscillator Connections

1.6.3.2 External Clock

An external clock from another CMOS-compatible device can be connected to the XOSC1 input, with the XOSC2 input not connected, as shown in **Figure 1-4 (b)**. This configuration is possible regardless of how the oscillator is set up.

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1.6.4 $\overline{\text{RESET}}$

This pin can be used as an input to reset the MCU to a known startup state by pulling it to the low state. When power is removed, the $\overline{\text{RESET}}$ pin contains a steering diode to discharge any voltage on the pin to V_{DD}. The $\overline{\text{RESET}}$ pin contains an internal Schmitt trigger to improve its noise immunity as an input. An internal $\overline{\text{RESET}}$ pin pullup resistor may be selected as a mask option. A typical pullup resistor value is 33 kΩ.

1.6.5 Port A (PA0–PA7)

Port A is an 8-bit I/O port. The state of any pin is software programmable and all port A lines are configured as inputs during power-on or reset. Port A outputs may be configured as open-drain outputs and connected to a pullup resistor by software option.

1.6.6 Port B (PB0–PB7/$\overline{\text{KWI0}}$–$\overline{\text{KWI7}}$)

Port B is an 8-bit input-only port that shares its lines with the key wakeup interrupt (KWI) system. Port B has a pullup option by software option.

1.6.7 Port C (PC0/SDI, PC1/SDO, PC2/SCK, PC3/TCAP, PC4/EVI, PC5/EVO, PC6/$\overline{\text{IRQ2}}$, and PC7/$\overline{\text{IRQ1}}$)

Port C is a 6-bit I/O port and 2-bit input-only port. The state of the PC0–PC5 pins are software programmable and all port C lines are configured as inputs during power-on or reset. All port C lines may connect to a pullup resistor by software option.

- Bits PC0–PC2 are shared with the SSPI subsystem and may be configured as open-drain outputs.
- Bit 3 is shared with the TCAP pin of timer 1 and may be configured as an open-drain output.
- Bit 4 is shared with the EVI bit of timer 2 and may be configured as an open-drain output.

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- Bit 5 is shared with the EVO bit of timer 2 and may be configured as an open-drain output.
- Bit 6 is shared with the $\overline{\text{IRQ2}}$ input. This bit is an input-only pin.
- Bit 7 is shared with the $\overline{\text{IRQ1}}$ input. This bit is an input-only pin.

1.6.8 Port D (PD1–PD3/BP1–BP3 and PD4–PD7/FP34–FP27)

Port D is a 7-bit output-only port that shares its bits with the LCD backplane/frontplane drivers. Port D lines are configured as LCD outputs during power-on or reset. PD1–PD3 and PD4–PD7 outputs may be configured as open-drain outputs by a software option.

1.6.9 Port E (PE0–PE7/FP38–FP35)

Port E is an 8-bit output-only port that shares its bits with LCD frontplane drivers. Port E lines are configured as LCD outputs during power-on or reset. PE0–PE3 and PE4–PE7 outputs may be configured as open-drain outputs by a software option.

1.6.10 VLCD1, VLCD2, and VLCD3

These pins provide offset to the LCD driver bias for adjusting the contrast of the LCD.

1.6.11 NDLY

This pin is reserved for factory test and should be connected to V_{DD} in single-chip mode (user mode).

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1.7 Modes of Operation

The MC68HC05L5 has two operating modes:

- Single-chip mode (SCM)
- Self-check mode

Single-chip mode, also called user mode, allows maximum use of pins for on-chip peripheral functions.

The self-check capability of MC68HC05L5 provides an internal check to determine if the device is functional.

1.7.1 Mode Entry

Mode entry is done at the rising edge of the $\overline{\text{RESET}}$ pin. Once the device enters one of the modes, the mode cannot be changed by software. Only an external reset can change the mode.

At the rising edge of the $\overline{\text{RESET}}$ pin, the device latches the states of $\overline{\text{IRQ1}}$ and $\overline{\text{IRQ2}}$ and places itself in the specified mode. While the $\overline{\text{RESET}}$ pin is low, all pins are configured as single-chip mode. **Table 1-2** shows the states of $\overline{\text{IRQ1}}$ and $\overline{\text{IRQ2}}$ for each mode entry.

High voltage $V_{TST} = 2 \times V_{DD}$ is required to select modes other than single-chip mode.

Table 1-2. Mode Select Summary

Modes	$\overline{\text{RESET}}$	PC6/$\overline{\text{IRQ1}}$	PC7/$\overline{\text{IRQ2}}$
Single-chip (user) mode		V_{SS} or V_{DD}	V_{SS} or V_{DD}
Self-check mode		V_{TST}	V_{DD}

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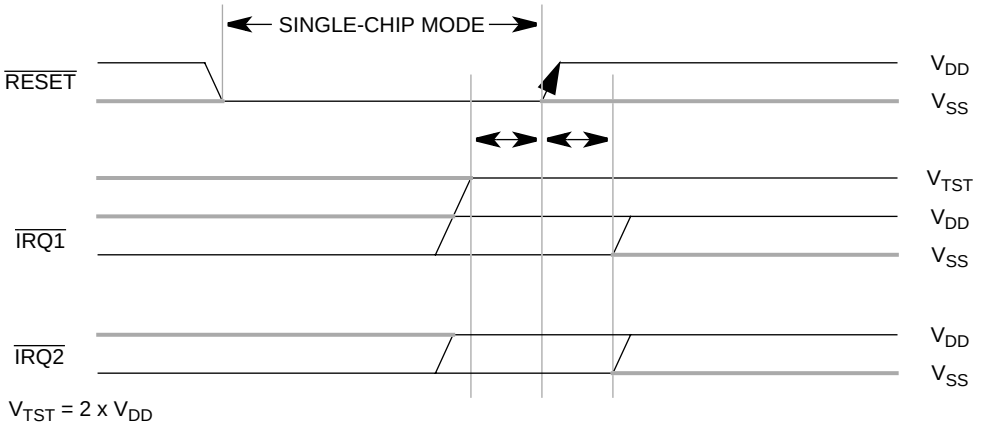

Figure 1-5. Mode Entry Diagram

1.7.2 Single-Chip Mode (SCM)

In this mode, all address and data bus activity occurs within the MCU. Thus, no external pins are required for these functions. The single-chip mode allows the maximum number of I/O pins for on-chip peripheral functions, for example, ports A through E, and LCD drivers.

1.7.3 Self-Check Mode

In this mode, the reset vector is fetched from a 496-byte internal self-check ROM at $3E00–$3FEF. The self-check ROM contains a self-check program to test the functions of internal modules.

Since this mode is not a normal user mode, all of the privileged control bits are accessible. This allows the self-check mode to be used for self-test of the device.

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General Description

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Section 2. Memory Map

2.1 Contents

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2.2 Introduction

The MC68HC05L5 contains an 8,192-byte mask ROM, 480 bytes of self-check ROM, and 256 bytes of RAM. An additional 16 bytes of mask ROM are provided for user vectors at $3FF0–$3FFF.

The MCU's memory map is shown in **Figure 2-1**.

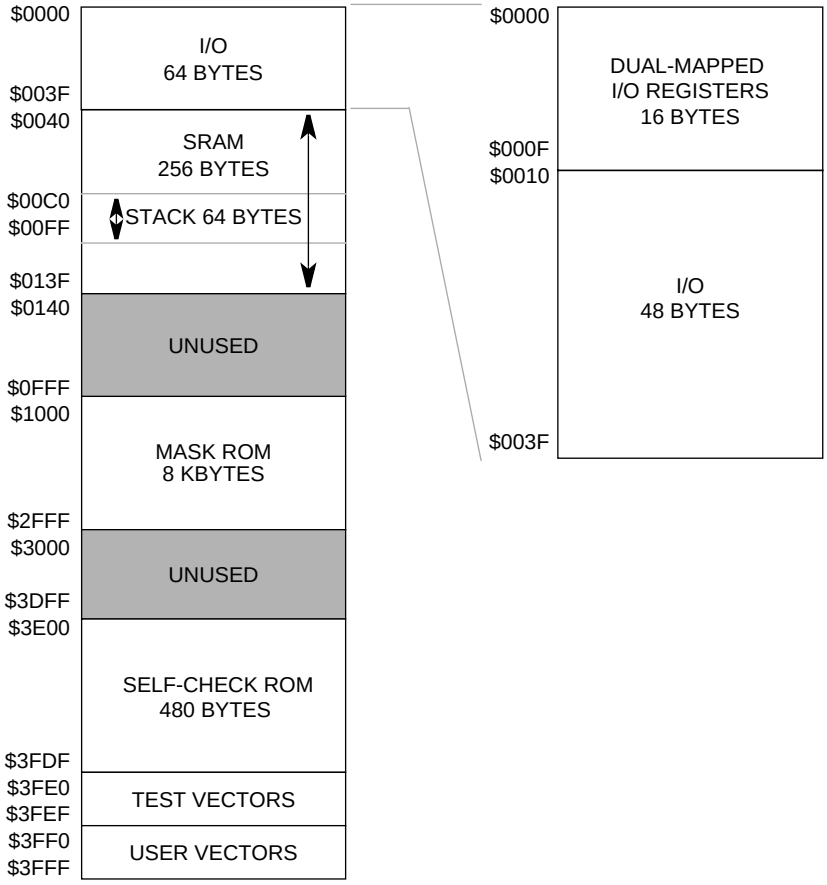

Figure 2-1. Memory Map

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2.3 Input/Output and Control Registers

The input/output (I/O) and control registers reside in locations $0000–$003F. A summary of these registers is shown in **Figure 2-3**. The bit assignments for each register are shown in **Figure 2-4**. Reading from unimplemented bits (denoted by shading) will return unknown states (unless explicitly defined to read 0), and writing to unimplemented bits will have no effect. See also **Figure 2-2**.

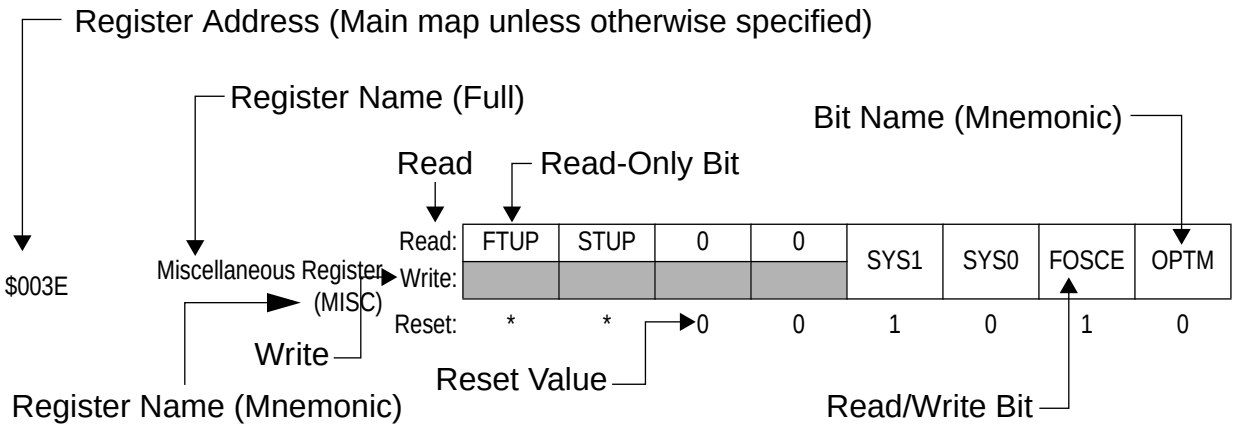

Figure 2-2. Register Description Key

2.3.1 Read/Write Bits

Read/write bits are typically control bits. They are, in general, not modified by a module. Reset indicates the initial value of the latch.

2.3.2 Read-Only Bits

Read-only bits are status flag bits. They are indicators of module status. Reset indicates the value that will be read immediately after system reset or before the module is enabled.

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2.3.3 Write-Only Bits

Write-only bits are control bits. They typically return a state of 0 to prevent an inadvertent write to this bit by a READ-MODIFY-WRITE instruction. Reset indicates the value that will be read immediately after system reset, which is the forced read value (typically 0).

2.3.4 Reserved Bits

Reserved bits are read-only bits that typically read 0. Writes to these bits are ignored, and the user should not write 1 for future compatibility. Reset indicates the value that will be read immediately after system reset which is the forced read value (typically 0).

2.3.5 Reset Value

Values specified on the row marked *Reset:* are initial values of register bits after system reset. Those bits unaffected by reset are marked with the letter U. Those bits that are unaffected by reset but initialized by power-on reset are marked with an asterisk (*).

2.3.6 Option Map

Address locations $0000–$000F are dual mapped. When the OPTM bit in the MISC register is cleared, the main address map is accessed. When the OPTM bit in the MISC register is set, the option address map is accessed.

NOTE: *Although not necessary for this device, for future compatibility the OPTM bit should be cleared when accessing memory locations $0010 and above.*

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2.4 Summary of Internal Registers and I/O Map

Figure 2-3 contains a detailed memory map of the I/O registers.

Addr.	Register Name		Bit 7	6	5	4	3	2	1	Bit 0
$0000	Port A Data Register (PORTA)	Read: Write:	PA7	PA6	PA5	PA4	PA3	PA2	PA1	PA0
		Reset:	Unaffected by reset							
$0001	Port B Data Register (PORTB)	Read: Write:	PB7	PB6	PB5	PB4	PB3	PB2	PB1	PB0
		Reset:	Unaffected by reset							
$0002	Port C Data Register (PORTC)	Read: Write:	PC7	PC6	PC5	PC4	PC3	PC2	PC1	PC0
		Reset:	Unaffected by reset							
$0003	Port D Data Register (PORTD)	Read: Write:	PD7	PD6	PD5	PD4	PD3	PD2	PD1	1
		Reset:	1	1	1	1	1	1	1	1
$0004	Port E Data Register (PORTE)	Read: Write:	PE7	PE6	PE5	PE4	PE3	PE2	PE1	PE0
		Reset:	1	1	1	1	1	1	1	1
$0005	Reserved		R	R	R	R	R	R	R	R
$0006	Reserved		R	R	R	R	R	R	R	R
$0007	Reserved		R	R	R	R	R	R	R	R
$0008	Interrupt Control Register (INTCR)	Read: Write:	IRQ1E	IRQ2E	0	KWIE	IRQ1S	IRQ2S	0	0
		Reset:	0	0	0	0	0	0	0	0
$0009	Interrupt Status Register (INTSR)	Read:	IRQ1F	IRQ2F	0	KWIF	0	0	0	0
		Write:					RIRQ1	RIRQ2		RKWIF
		Reset:	0	0	0	0	0	0	0	0

= Unimplemented R = Reserved

Figure 2-3. Main I/O Map (Sheet 1 of 6)

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Memory Map

Addr.	Register Name		Bit 7	6	5	4	3	2	1	Bit 0
$000A	Serial Peripheral Control Register (SPCR)	Read:	SPIE	SPE	DORD	MSTR	0	0	0	SPR
		Write:								
		Reset:	0	0	0	0	0	0	0	0
$000B	Serial Peripheral Status Register (SPSR)	Read:	SPIF	DCOL	0	0	0	0	0	0
		Write:								
		Reset:	0	0	0	0	0	0	0	0
$000C	Serial Peripheral Data Register (SPDR)	Read:	MSB	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 2	LSB
		Write:								
		Reset:	Unaffected by reset							
$000D	Reserved		R	R	R	R	R	R	R	R
$000E	Reserved		R	R	R	R	R	R	R	R
$000F	Reserved		R	R	R	R	R	R	R	R
$0010	Timer Base Control Register 1 (TBCR1)	Read:	TBCLK	0	LCLK	0	0	0	T2R1	T2R0
		Write:								
		Reset:	0	0	0	0	0	0	0	0
$0011	Timer Base Control Register 2 (TBCR2)	Read:	TBIF	TBIE	TBR1	TBR0	0	0	0	0
		Write:					RTBIF		COPE	COPC
		Reset:	0	0	1	1	0	0	0	0
$0012	Timer Control Register (TCR)	Read:	ICIE	OC1IE	TOIE	0	0	0	IEDG	OLVL
		Write:								
		Reset:	0	0	0	0	0	0	U	0
$0013	Timer Status Register (TSR)	Read:	ICF	OC1F	TOF	0	0	0	0	0
		Write:								
		Reset:	U	U	U	0	0	0	0	0
$0014	Input Capture Register High (ICH)	Read:	BIT 15	BIT 14	BIT 13	BIT 12	BIT 11	BIT 10	BIT 9	BIT 8
		Write:								
		Reset:	Unaffected by reset							

= Unimplemented R = Reserved U = Unaffected

Figure 2-3. Main I/O Map (Sheet 2 of 6)

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Addr.	Register Name		Bit 7	6	5	4	3	2	1	Bit 0
$0015	Input Capture Register Low (ICL)	Read:	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
		Write:								
		Reset:	Unaffected by reset							
$0016	Output Compare Register 1 High (OC1H)	Read:	BIT 15	BIT 14	BIT 13	BIT 12	BIT 11	BIT 10	BIT 9	BIT 8
		Write:								
		Reset:	Unaffected by reset							
$0017	Output Compare Register 1 Low (OC1L)	Read:	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
		Write:								
		Reset:	Unaffected by reset							
$0018	Timer Counter Register High (TCNTH)	Read:	BIT 15	BIT 14	BIT 13	BIT 12	BIT 11	BIT 10	BIT 9	BIT 8
		Write:								
		Reset:	Unaffected by reset							
$0019	Timer Counter Register Low (TCNTL)	Read:	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
		Write:								
		Reset:	Unaffected by reset							
$001A	Alternate Timer Counter Register High (ACNTH)	Read:	BIT 15	BIT 14	BIT 13	BIT 12	BIT 11	BIT 10	BIT 9	BIT 8
		Write:								
		Reset:	Unaffected by reset							
$001B	Alternate Timer Counter Register Low (ACMTL)	Read:	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
		Write:								
		Reset:	Unaffected by reset							
$001C	Timer Control Register 2 (TCR2)	Read:	TI2IE	OC2IE	0	T2CLK	IM2	IL2	OE2	OL2
		Write:								
		Reset:	0	0	0	0	0	0	0	0
$001D	Timer Status Register 2 (TSR2)	Read:	TI2F	OC2F	0	0	0	0	0	0
		Write:					RTI2F	ROC2F		
		Reset:	0	0	0	0	0	0	0	0
$001E	Output Compare Register 2 (OC2)	Read:	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
		Write:								
		Reset:	0	0	0	0	0	0	0	0

= Unimplemented

Figure 2-3. Main I/O Map (Sheet 3 of 6)

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Memory Map

Addr.	Register Name		Bit 7	6	5	4	3	2	1	Bit 0
$001F	Timer Counter Register 2 (TCNT2)	Read: Write:	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
		Reset:	0	0	0	0	0	0	0	1
$0020	LCD Control Register (LCDCR)	Read: Write:	LCDE	DUTY1	DUTY0	0	PEH	PEL	PDH	0
		Reset:	0	0	0	0	0	0	0	0
$0021	LCD Data Register 1 (LCDR1)	Read: Write:	F1B3	F1B2	F1B1	F1B0	F0B3	F0B2	F0B1	F0B0
		Reset:	Unaffected by reset							
$0022	LCD Data Register 2 (LCDR2)	Read: Write:	F3B3	F3B2	F3B1	F3B0	F2B3	F2B2	F2B1	F2B0
		Reset:	Unaffected by reset							
$0023	LCD Data Register 3 (LCDR3)	Read: Write:	F5B3	F5B2	F5B1	F5B0	F4B3	F4B2	F4B1	F4B0
		Reset:	Unaffected by reset							
$0024	LCD Data Register 4 (LCDR4)	Read: Write:	F7B3	F7B2	F7B1	F7B0	F6B3	F6B2	F6B1	F6B0
		Reset:	Unaffected by reset							
$0025	LCD Data Register 5 (LCDR5)	Read: Write:	F9B3	F9B2	F9B1	F9B0	F8B3	F8B2	F8B1	F8B0
		Reset:	Unaffected by reset							
$0026	LCD Data Register 6 (LCDR6)	Read: Write:	F11B3	F11B2	F11B1	F11B0	F10B3	F10B2	F10B1	F10B0
		Reset:	Unaffected by reset							
$0027	LCD Data Register 7 (LCDR7)	Read: Write:	F13B3	F13B2	F13B1	F13B0	F12B3	F12B2	F12B1	F12B0
		Reset:	Unaffected by reset							

Figure 2-3. Main I/O Map (Sheet 4 of 6)

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Addr.	Register Name		Bit 7	6	5	4	3	2	1	Bit 0
$0028	LCD Data Register 8 (LCDR8)	Read: Write:	F15B3	F15B2	F15B1	F15B0	F14B3	F14B2	F14B1	F14B0
		Reset:	Unaffected by reset							
$0029	LCD Data Register 9 (LCDR9)	Read: Write:	F17B3	F17B2	F17B1	F17B0	F16B3	F16B2	F16B1	F16B0
		Reset:	Unaffected by reset							
$002A	LCD Data Register 10 (LCDR10)	Read: Write:	F19B3	F19B2	F19B1	F19B0	F18B3	F18B2	F18B1	F18B0
		Reset:	Unaffected by reset							
$002B	LCD Data Register 11 (LCDR11)	Read: Write:	F21B3	F21B2	F21B1	F21B0	F20B3	F20B2	F20B1	F20B0
		Reset:	Unaffected by reset							
$002C	LCD Data Register 12 (LCDR12)	Read: Write:	F23B3	F23B2	F23B1	F23B0	F22B3	F22B2	F22B1	F22B0
		Reset:	Unaffected by reset							
$002D	LCD Data Register 13 (LCDR13)	Read: Write:	F25B3	F25B2	F25B1	F25B0	F24B3	F24B2	F24B1	F24B0
		Reset:	Unaffected by reset							
$002E	LCD Data Register 14 (LCDR14)	Read: Write:	F27B3	F27B2	F27B1	F27B0	F26B3	F26B2	F26B1	F26B0
		Reset:	Unaffected by reset							
$002F	LCD Data Register 15 (LCDR15)	Read: Write:	F29B3	F29B2	F29B1	F29B0	F28B3	F28B2	F28B1	F28B0
		Reset:	Unaffected by reset							
$0030	LCD Data Register 16 (LCDR16)	Read: Write:	F31B3	F31B2	F31B1	F31B0	F30B3	F30B2	F30B1	F30B0
		Reset:	Unaffected by reset							

Figure 2-3. Main I/O Map (Sheet 5 of 6)

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Memory Map

Addr.	Register Name		Bit 7	6	5	4	3	2	1	Bit 0
$0031	LCD Data Register 17 (LCDR17)	Read:	F33B3	F33B2	F33B1	F33B0	F32B3	F32B2	F32B1	F32B0
		Write:								
		Reset:	Unaffected by reset							
$0032	LCD Data Register 18 (LCDR18)	Read:	F35B3	F35B2	F35B1	F35B0	F34B3	F34B2	F34B1	F34B0
		Write:								
		Reset:	Unaffected by reset							
$0033	LCD Data Register 19 (LCDR19)	Read:	F37B3	F37B2	F37B1	F37B0	F36B3	F36B2	F36B1	F36B0
		Write:								
		Reset:	Unaffected by reset							
$0034	LCD Data Register 20 (LCDR20)	Read:	0	0	0	0	F38B3	F38B2	F38B1	F38B0
		Write:								
		Reset:	Unaffected by reset							
$0035	Reserved		R	R	R	R	R	R	R	R
$0036	Reserved		R	R	R	R	R	R	R	R
$0037	Reserved		R	R	R	R	R	R	R	R
$0038	Reserved		R	R	R	R	R	R	R	R
$0039	Reserved		R	R	R	R	R	R	R	R
$003A	Reserved		R	R	R	R	R	R	R	R
$003B	Reserved		R	R	R	R	R	R	R	R
$003C	Reserved		R	R	R	R	R	R	R	R
$003D	Reserved		R	R	R	R	R	R	R	R
$003E	Miscellaneous Register (MISC)	Read:	FTUP	STUP	0	0	SYS1	SYS0	FOSCE	OPTM
		Write:								
		Reset:	*	*	0	0	1	0	1	0
$003F	Reserved		R	R	R	R	R	R	R	R

* Unaffected by reset but initialized by power-on reset

= Unimplemented R = Reserved

Figure 2-3. Main I/O Map (Sheet 6 of 6)

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2.5 Option Map for I/O Configurations

Most of the I/O configurations are done in the option map (**Figure 2-4**). Some options still remain as mask options for the MC68HC05L5 such as a pullup resistor for the $\overline{\text{RESET}}$ pin and resistors for the OSC1/OSC2 and XOSC1/XOSC2 pins. These mask options may be read by the MOSR ($000F) in the option map.

The option map is located at $0000–$000F of the main memory map and it is available when the OPTM bit in the MISC register ($003E) is set. Main registers at $0000–$000F are not available when OPTM = 1.

I/O port data direction registers are contained in the option map in **Figure 2-4**.

Addr.	Register Name		Bit 7	6	5	4	3	2	1	Bit 0
$0000	Port A Data Direction Register (DDRA)	Read: Write:	DDRA7	DDRA6	DDRA5	DDRA4	DDRA3	DDRA2	DDRA1	DDRA0
		Reset:	0	0	0	0	0	0	0	0
$0001	Reserved		R	R	R	R	R	R	R	R
$0002	Port C Data Direction Register (DDRC)	Read: Write:	0	0	DDRC5	DDRC4	DDRC3	DDRC2	DDRC1	DDRC0
		Reset:	0	0	0	0	0	0	0	0
$0003	Reserved		R	R	R	R	R	R	R	R
$0004	Reserved		R	R	R	R	R	R	R	R
$0005	Reserved		R	R	R	R	R	R	R	R
$0006	Reserved		R	R	R	R	R	R	R	R
$0007	Reserved		R	R	R	R	R	R	R	R
$0008	Resistor Control Register 1 (RCR1)	Read: Write:	0	0	0	0	RBH	RBL	RAH	RAL
		Reset:	0	0	0	0	0	0	0	0

R = Reserved

Figure 2-4. Option Map (Sheet 1 of 2)

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Memory Map

Addr.	Register Name		Bit 7	6	5	4	3	2	1	Bit 0
$0009	Resistor Control Register 2 (RCR2)	Read: Write:	RC7	RC6	RC5	RC4	RC3	RC2	RC1	RC0
		Reset:	0	0	0	0	0	0	0	0
$000A	Open-Drain Output Control Register 1 (WOM1)	Read: Write:	DWOMH	DWOML	EWOMH	EWOML	0	0	AWOMH	AWOML
		Reset:	0	0	0	0	0	0	0	0
$000B	Open-Drain Output Control Register 2 (WOM2)	Read: Write:	0	0	CWOM5	CWOM4	CWOM3	CWOM2	CWOM1	CWOM0
		Reset:	0	0	0	0	0	0	0	0
$000C	Reserved		R	R	R	R	R	R	R	R
$000D	Reserved		R	R	R	R	R	R	R	R
$000E	Key Wakeup Input Enable Register (KWIEN)	Read: Write:	KWIE7	KWIE6	KWIE5	KWIE4	KWIE3	KWIE2	KWIE1	KWIE0
		Reset:	0	0	0	0	0	0	0	0
$000F	Mask Option Status Register	Read:	RSTR	OSCR	XOSCR	0	0	0	0	0
		Write:								
		Reset:	U	U	U	0	0	0	0	0

= Unimplemented R = Reserved U = Unaffected

Figure 2-4. Option Map (Sheet 2 of 2)

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2.5.1 Resistor Control Register 1

Address: Option Map — $0008

	Bit 7	6	5	4	3	2	1	Bit 0
Read: Write:	0	0	0	0	RBH	RBL	RAH	RAL
Reset:	0	0	0	0	0	0	0	0

Figure 2-5. Resistor Control Register 1 (RCR1)

Bits 7–4 — Reserved

These bits are not used and always read as logic 0.

RBH — Port B Pullup Resistor (H)

When this bit is set, pullup resistors are connected to the upper four bits of port B. This bit is cleared on reset.

RBL — Port B Pullup Resistor (L)

When this bit is set, pullup resistors are connected to the lower four bits of port B. This bit is cleared on reset.

RAH — Port A Pullup Resistor (H)

When this bit is set, pullup resistors are connected to the upper four bits of port A. This bit is cleared on reset.

RAL — Port A Pullup Resistor (L)

When this bit is set, pullup resistors are connected to the lower four bits of port A. This bit is cleared on reset.

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2.5.2 Resistor Control Register 2

Address: Option Map — $0009

	Bit 7	6	5	4	3	2	1	Bit 0
Read: Write:	RC7	RC6	RC5	RC4	RC3	RC1	RC1	RC0
Reset:	0	0	0	0	0	0	0	0

Figure 2-6. Resistor Control Register 2 (RCR2)

RC*x* — Port C Pullup Resistor (Bit*x*)

When RC*x* bit is set, the pullup resistor is connected to the corresponding bit of port C. This bit is cleared on reset.

2.5.3 Open-Drain Output Control Register 1

Address: Option Map — $000A

	Bit 7	6	5	4	3	2	1	Bit 0
Read: Write:	DWOMH	DWOML	EWOMH	EWOML	0	0	AWOMH	AWOML
Reset:	0	0	0	0	0	0	0	0

Figure 2-7. Open-Drain Output Control Register 1 (WOM1)

DWOMH — Port D Open-Drain Mode (H)

When this bit is set, the upper four bits of port D are configured as open-drain outputs if these bits are selected as port D output by the PDH bit in the LCDCR. This bit is cleared on reset.

DWOML — Port D Open-Drain Mode (L)

When this bit is set, the lower three bits of port D are configured as open-drain outputs if the corresponding BP*x* pin is not used by the LCD driver. This bit is cleared on reset.

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EWOMH — Port E Open-Drain Mode (H)

When this bit is set, the upper four bits of port E (that are configured as I/O output by the PEH bit in the LCDCR) are configured as open-drain outputs. This bit is cleared on reset.

EWOML — Port E Open-Drain Mode (L)

When this bit is set, the lower four bits of port E (that are configured as I/O output by the PEL bit in the LCDCR) are configured as open-drain outputs. This bit is cleared on reset.

Bits 3 and 2 — Reserved

These bits are not used and always return to logic 0.

AWOMH — Port A Open-Drain Mode (H)

When this bit is set, the upper four bits of port A that are configured as output (corresponding to the DDRA bit set) become open-drain outputs. This bit is cleared on reset.

AWOML — Port E Open-Drain Mode (L)

When this bit is set, the lower four bits of port A that are configured as output (corresponding DDRA bit set) become open-drain outputs. This bit is cleared on reset.

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2.5.4 Open-Drain Output Control Register 2

Address: Option Map — $000B

	Bit 7	6	5	4	3	2	1	Bit 0
Read: Write:	0	0	CWOM5	CWOM4	CWOM3	CWOM2	CWOM1	CWOM0
Reset:	0	0	0	0	0	0	0	0

Figure 2-8. Open-Drain Output Control Register 2 (WOM2)

Bits 7 and 6 — Reserved

These bits are not used and always read as logic 0.

CWOM*x* — Port C Open-Drain Mode (Bit*x*)

When CWOM*x* bit is set, port C bits *x* are configured as open-drain outputs if DDRC*x* is set. This bit is cleared on reset.

2.5.5 Key Wakeup Input Enable Register

Address: Option Map — $000E

	Bit 7	6	5	4	3	2	1	Bit 0
Read: Write:	KWIE7	KWIE6	KWIE5	KWIE4	KWIE3	KWIE2	KWIE1	KWIE0
Reset:	0	0	0	0	0	0	0	0

Figure 2-9. Key Wakeup Input Enable Register (KWIEN)

KWIE*x* — Key Wakeup Input Enable (Bit*x*)

When KWIE*x* bit is set, the KWI*x* (PB*x*) input is enabled for key wakeup interrupt. This bit is cleared on reset.

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2.5.6 Mask Option Status Register

The mask option status register (MOSR) indicates the state of mask options specified prior to production of the MC68HC05L5.

Address: Option Map — $000F

	Bit 7	6	5	4	3	2	1	Bit 0
Read:	RSTR	OSCR	XOSCR	0	0	0	0	0
Write:								
Reset:	U	U	U	0	0	0	0	0

= Unimplemented U = Unaffected

Figure 2-10. Mask Option Status Register (MOSR)

RSTR — $\overline{\text{RESET}}$ Pin Pullup Resistor

When this bit is set, it indicates an internal pullup resistor is attached to the $\overline{\text{RESET}}$ pin by mask option.

OSCR — OSC Feedback Resistor

When this bit is set, it indicates that an internal feedback resistor is attached between OSC1 and OSC2 by mask option.

XOSCR — OSC Feedback Resistor

When this bit is set, it indicates that an internal feedback resistor is attached between XOSC1 and XOSC2. The damping resistor at the XOSC2 pin is attached by mask option.

Bits 4–0 — Reserved

These bits are not used and always read as logic 0.

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2.6 RAM

The 256-byte internal RAM is positioned at $0040–$013F in the memory map. The lower 192 bytes are positioned in the page zero which are accessible by the direct addressing mode. The upper 64 bytes of this area (page zero) are used for the CPU stack area. Care should be taken if the stack area is used for data storage.

The remaining 64 byte of RAM at $0100–$013F are accessed by extended addressing mode.

The RAM is implemented with static cells and retains its contents during the stop and wait modes.

2.7 Self-Check ROM

Self-check ROM is 480 bytes of mask ROM positioned at $3E00–$3FDF. This ROM contains self-check programs and reset/interrupt vectors in the self-check mode.

2.8 Mask ROM

The 8,192-byte user ROM is positioned at $1000–$2FFF, and an additional 16 bytes of ROM are located at $3FF0–$3FFF for user vectors.

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Section 3. Central Processor Unit (CPU)

3.1 Contents

3.2 Introduction

This section describes the central processor unit (CPU).

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3.3 CPU Registers

The MCU contains five registers as shown in **Figure 3-1**. The interrupt stacking order is shown in **Figure 3-2**.

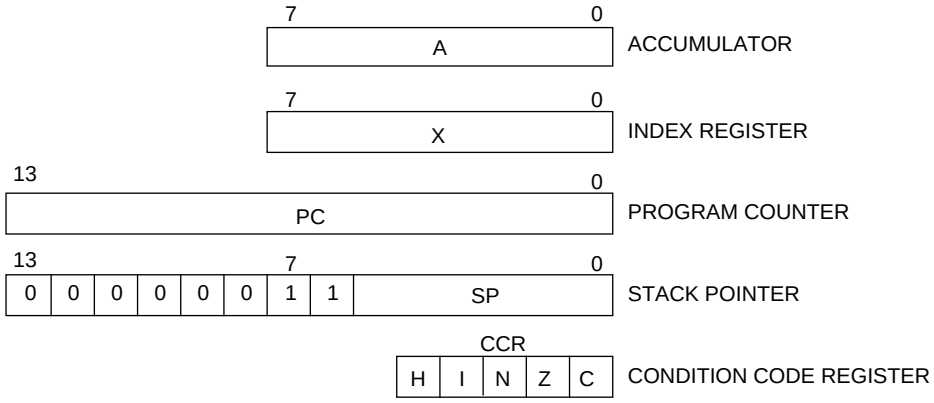
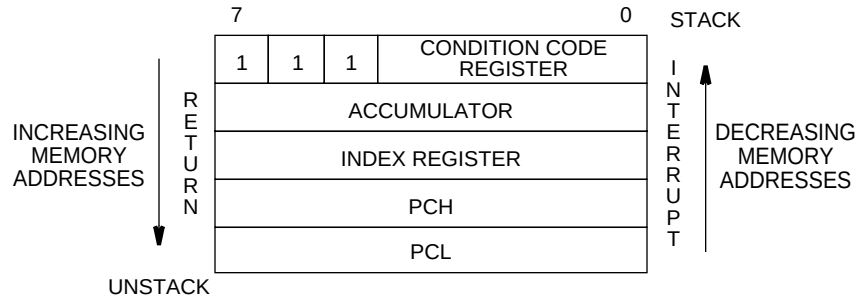


Figure 3-1. Programming Model



NOTE: Since the stack pointer decrements during pushes, the PCL is stacked first, followed by PCH, etc. Pulling from the stack is in the reverse order.

Figure 3-2. Stacking Order

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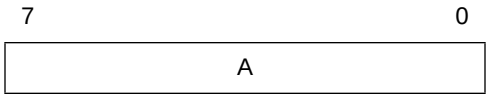
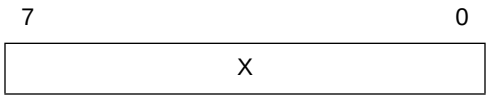
3.4 Accumulator

The accumulator (A) is a general-purpose, 8-bit register used to hold operands and results of arithmetic calculations or data manipulations.



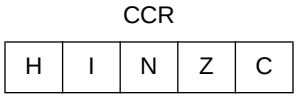
3.5 Index Register

The index register (X) is an 8-bit register used for the indexed addressing value to create an effective address. The index register may also be used as a temporary storage area.



3.6 Condition Code Register

The condition code register (CCR) is a 5-bit register in which the H, N, Z, and C bits are used to indicate the results of the instruction just executed, and the I bit is used to enable or disable interrupts. These bits can be tested individually by a program, and specific actions can be taken as a result of their state. Each bit is explained in the following paragraphs.



Half Carry (H)

This bit is set during ADD and ADC operations to indicate that a carry occurred between bits 3 and 4.

Interrupt (I)

When this bit is set, the timer and external interrupt are masked (disabled). If an interrupt occurs while this bit is set, the interrupt is latched and processed as soon as the I bit is cleared.

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Negative (N)

When set, this bit indicates that the result of the last arithmetic, logical, or data manipulation was negative.

Zero (Z)

When set, this bit indicates that the result of the last arithmetic, logical, or data manipulation was 0.

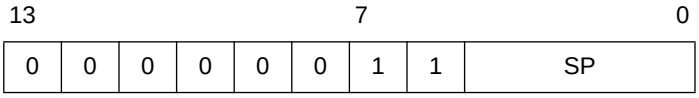
Carry/Borrow (C)

When set, this bit indicates that a carry or borrow out of the arithmetic logic unit (ALU) occurred during the last arithmetic operation. This bit is affected also during bit test and branch instructions and during shifts and rotates.

3.7 Stack Pointer

The stack pointer (SP) contains the address of the next free location on the stack. During an MCU reset or the reset stack pointer (RSP) instruction, the stack pointer is set to location $00FF. The stack pointer is then decremented as data is pushed onto the stack and incremented as data is pulled from the stack.

When accessing memory, the eight most significant bits are permanently set to 00000011. These eight 0 bits are appended to the six least significant register bits to produce an address within the range of $00FF to $00C0. Subroutines and interrupts may use up to 64 (decimal) locations. If 64 locations are exceeded, the stack pointer wraps around and loses the previously stored information. A subroutine call occupies two locations on the stack; an interrupt uses five locations.



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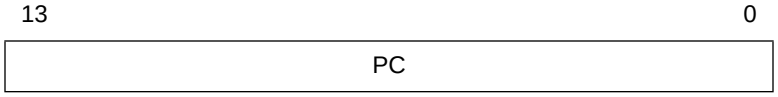
3.8 Program Counter

The program counter (PC) is a 14-bit register that contains the address of the next byte to be fetched.



3.9 Arithmetic Logic Unit

The arithmetic logic unit (ALU) performs the arithmetic and logical operations defined by the instruction set.

The binary arithmetic circuits decode instructions and set up the ALU for the selected operation. Most binary arithmetic is based on the addition algorithm, carrying out subtraction as negative addition. Multiplication is not performed as a discrete operation but as a chain of addition and shift operations within the ALU. The multiply instruction (MUL) requires 11 internal processor cycles to complete this chain of operations.

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Section 4. Resets and Interrupts

4.1 Contents

4.2 Introduction

In user operating modes, the reset/interrupt vectors are located at the top of the address space ($3FF0–$3FFF). In self-check mode, the reset/interrupt vectors are located at $3FE0–$3FEF in the internal self-check ROM. Descriptions in this section assume a user operating mode is in use. **Table 4-1** shows the address assignments for the vectors.

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Table 4-1. Interrupt Vector Assignments

Vector Address	Interrupt Source		Masked by	Local Mask	Priority (1 = Highest)
3FF0–3FF1	Timebase		I bit	TBIE	7
3FF2–3FF3	SSPI		I bit	SPIE	6
3FF4–3FF5	Timer 2	TI2I OC2I	I bit I bit	TI2IE OC2IE	5 5
3FF6–3FF7	Timer 1	ICI OC1I TOI	I bit I bit I bit	ICIE OC1IE TOIE	4 4 4
3FF8–3FF9	KWI		I bit	KWIE	3
3FFA–3FFB	IRQ	$\overline{\text{IRQ1}}$ $\overline{\text{IRQ2}}$	I bit I bit	IRQ1E IRQ2E	2 2
3FFC–3FFD	SWI		None	None	Same level as an instruction
3FFE–3FFF	Reset	COP $\overline{\text{RESET}}$ pin Power-on	None None None	COPE None None	1 1 1

Upon reset, the I bit in the condition code register is set and interrupts are disabled (masked). When an interrupt occurs, the I bit is set automatically by hardware after stacking the condition code register (CCR). All interrupts in the MC68HC05L5 follow a fixed hardware priority circuit to resolve simultaneous requests.

Each interrupt has a software programmable interrupt mask bit which may be used to selectively inhibit automatic hardware response. In addition, the I bit in the CCR acts as a class inhibit mask to inhibit all sources in the I-bit class. $\overline{\text{RESET}}$ and software interrupt (SWI) are not masked by the I bit in the CCR.

SWI is an instruction rather than a prioritized asynchronous interrupt source. In a sense, it is lower in priority than any source because once any interrupt sequence has begun, SWI cannot override it. In another sense, it is higher in priority than any hardware sources, except reset, because once the SWI opcode is fetched, no other sources can be honored until after the first instruction in the SWI service routine has been executed. SWI causes the I mask bit in the CCR to be set.

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4.3 Interrupts

There are six hardware interrupt sources in the MC68HC05L5:

- $\overline{\text{IRQ1}}$ and $\overline{\text{IRQ2}}$
- Key wakeup interrupt ($\overline{\text{KWI}}$)
- Timer 1 (TOI, ICI, and OC1I)
- Timer 2 (TI2I and OC2I)
- Serial transfer complete interrupt (SSPI)
- Timebase interrupt (TBI)

4.3.1 $\overline{\text{IRQ1}}$ and $\overline{\text{IRQ2}}$

Two external interrupt request inputs, $\overline{\text{IRQ1}}$ and $\overline{\text{IRQ2}}$, share the same vector address at $3FFA and $3FFB.

Bits IRQ1S and IRQ2S in interrupt control register (INTCR) control whether $\overline{\text{IRQ1}}$ and $\overline{\text{IRQ2}}$, respectively, respond only to the falling edge or falling edge and low level to trigger an interrupt. The $\overline{\text{IRQ1}}$ and $\overline{\text{IRQ2}}$ are enabled by IRQ1E and IRQ2E bits and IRQ1F and IRQ2F bits are provided as an indicator in the interrupt status register (INTSR). Since the IRQ1(2)F can be set by either the pins or the data latches of PC7(6), be sure to clear the flags by software before setting the IRQ1(2)E bit.

The $\overline{\text{IRQ1}}$ and the $\overline{\text{IRQ2}}$ pins are shared with port C bit 7 and bit 6, respectively, and IRQ*x* pin states can be determined by reading port C pins. The BIL and BIH instructions apply only to the $\overline{\text{IRQ1}}$ input.

4.3.2 Key Wakeup Interrupt ($\overline{\text{KWI}}$)

Eight key wakeup inputs ($\overline{\text{KWI0}}$–$\overline{\text{KWI7}}$) share pins with port B. Each key wakeup input is enabled by the corresponding bit in the KWIEN register which resides in the option map, and $\overline{\text{KWI}}$ is enabled by the KWIE bit in the INTCR. When a falling edge is detected at one of the enabled key wakeup inputs, the KWIF bit in the INTSR is set and $\overline{\text{KWI}}$ is generated if KWIE = 1. Each input has a latch which responds only to the falling edge at the pin, and all input latches are cleared at the same time by clearing the KWIF bit. See **Figure 4-6**.

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4.3.3 IRQ (KWI) Software Consideration

IRQ and KWI interrupts have a timing delay in a case described in **Figure 4-2**. This section shows programming for proper interrupts with IRQ or KWI.

Figure 4-1 shows an example of timer 1 interrupt. In this case, the interrupt by TOF occurs as soon as the TOIE (timer 1 overflow interrupt enable) bit is set.

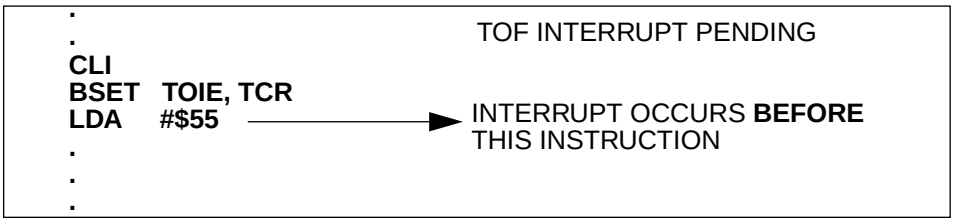

Figure 4-1. Timer 1 Interrupt

Figure 4-2 shows an example of $\overline{\text{IRQ1}}$ interrupt. In this case, the interrupt occurs **after** execution the instruction following the instruction which sets IRQ1E bit. The similar action occurs against $\overline{\text{IRQ2}}$ and $\overline{\text{KWI}}$ interrupts.

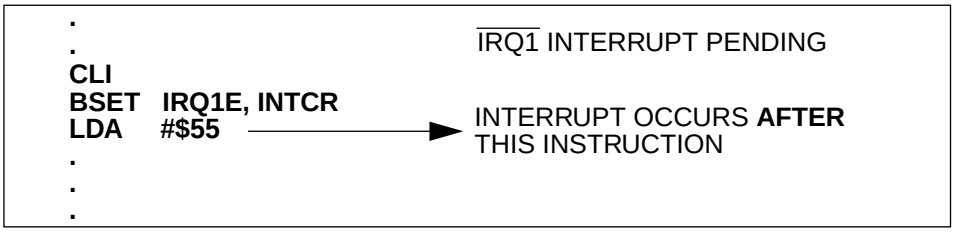

Figure 4-2. IRQ Timing Delay

This problem can be solved by using a software patch like **Figure 4-3**. A similar procedure could be used for $\overline{\text{IRQ2}}$ or $\overline{\text{KWI}}$.

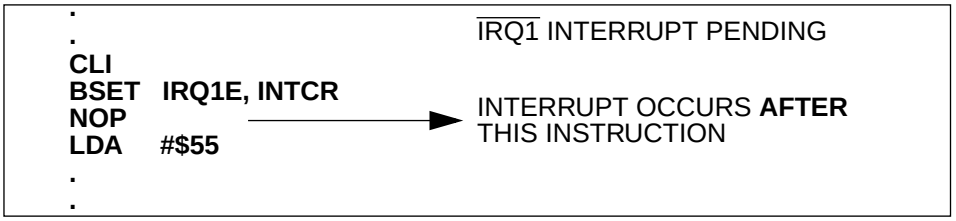

Figure 4-3. Software Patch for $\overline{\text{IRQ1}}$

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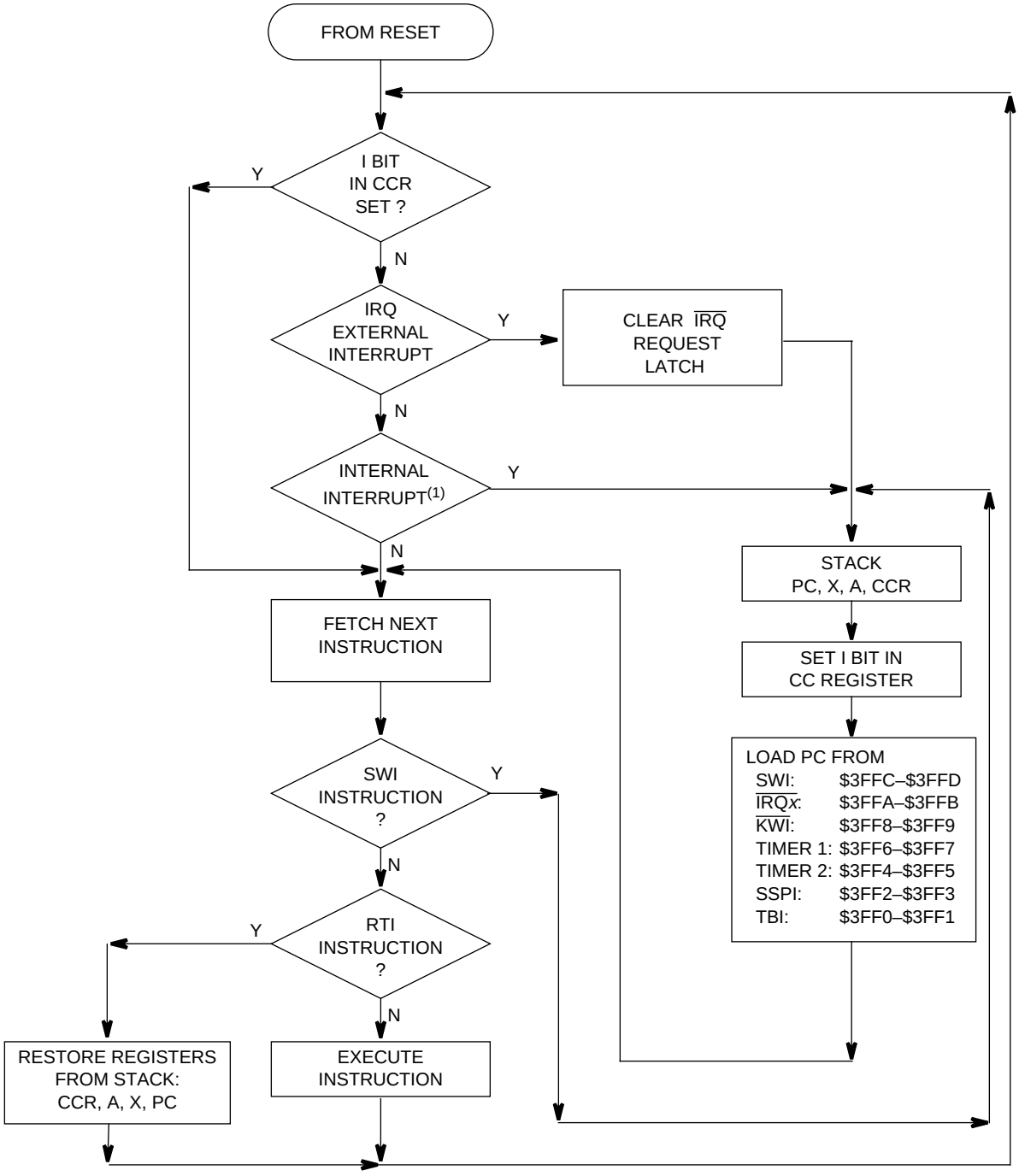

Note 1. KWI, timer 1, timer 2, SSPI, and TBI

Figure 4-4. Interrupt Flowchart

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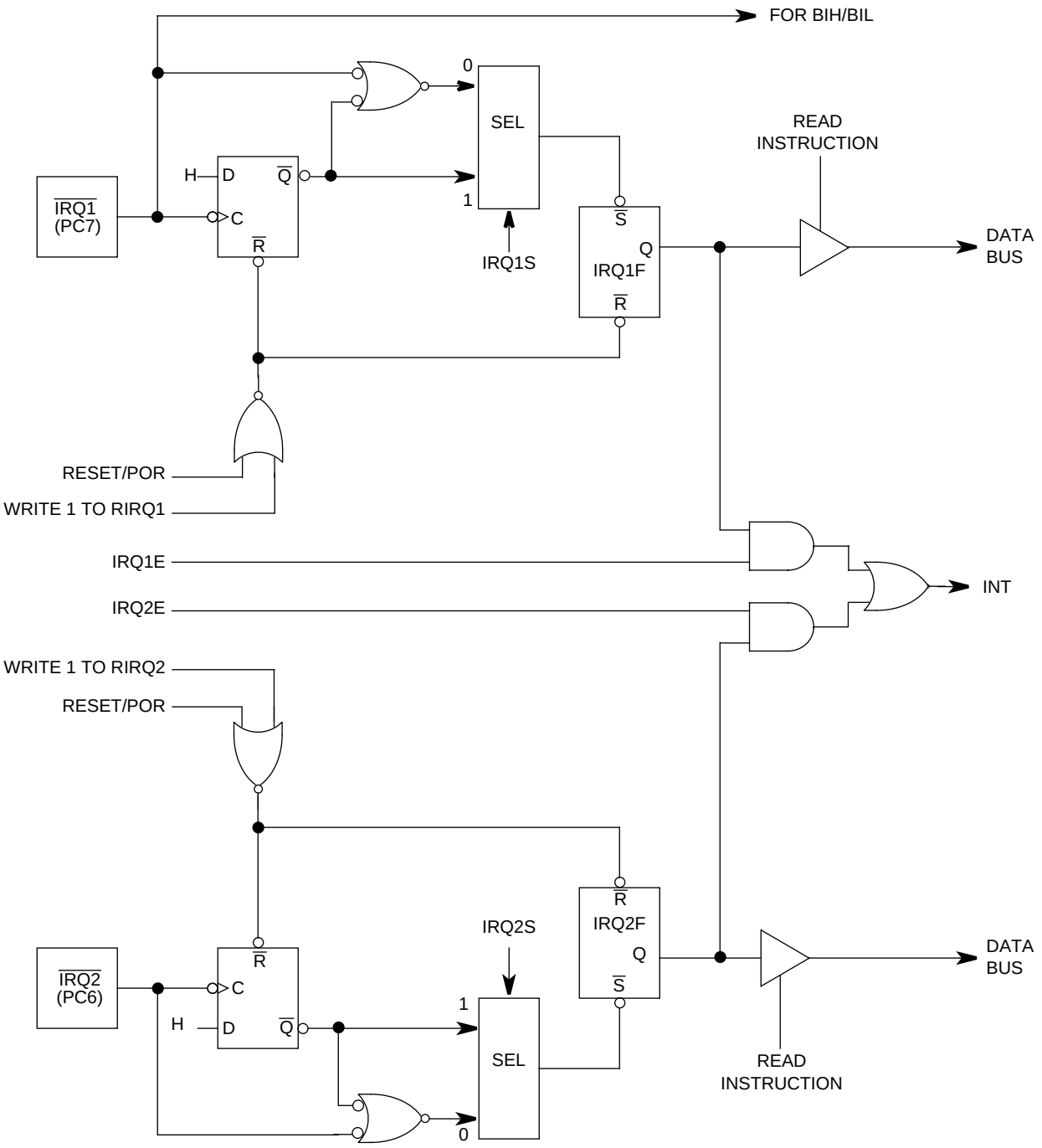

Figure 4-5. $\overline{\text{IRQ1}}$ and $\overline{\text{IRQ2}}$ Block Diagram

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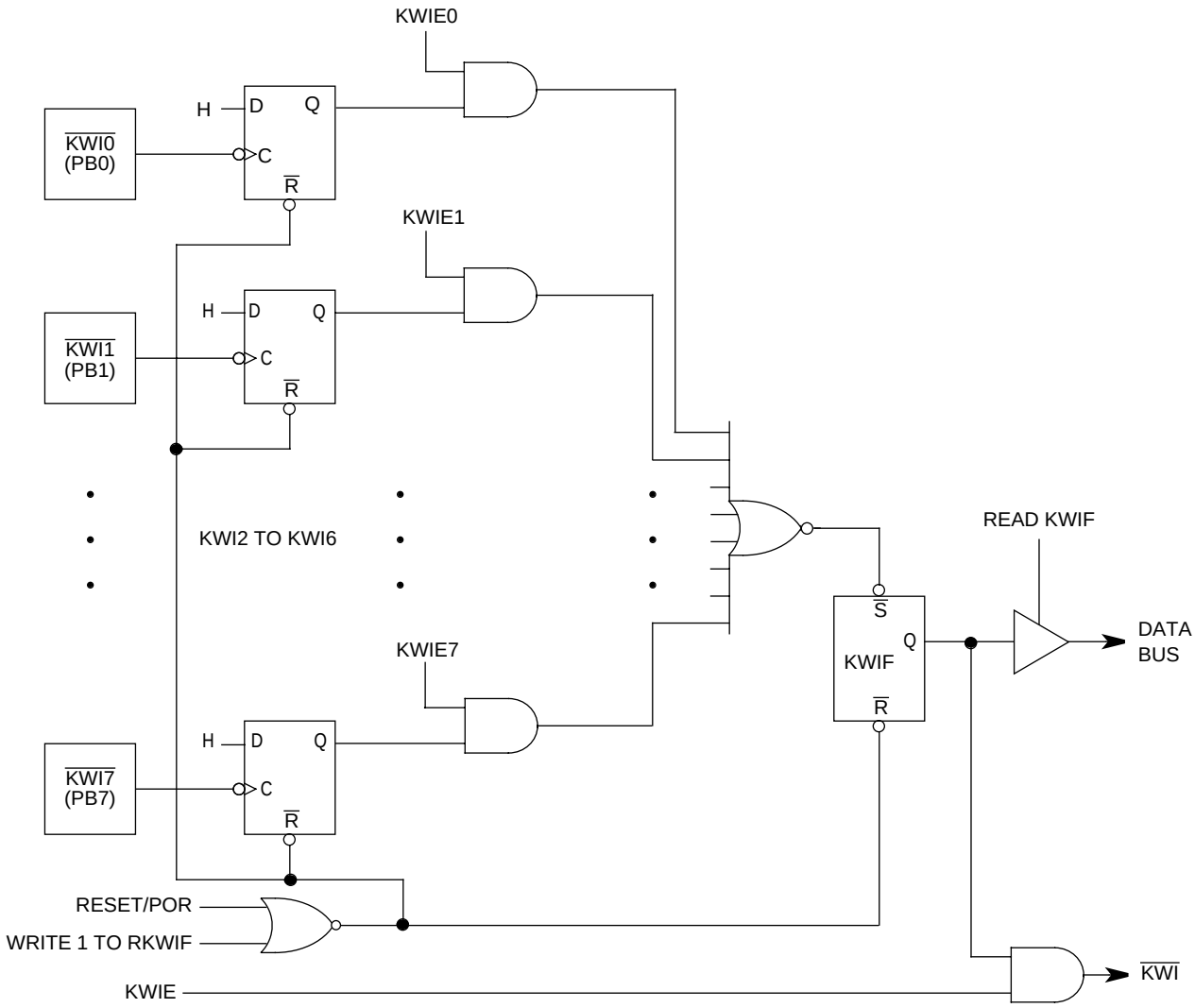

Figure 4-6. Key Wakeup Interrupt ($\overline{\text{KWI}}$)

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4.3.4 Timer 1 Interrupt

Three timer 1 interrupts (TOI, ICI, and OC1I) share the same interrupt vector at $3FF6 and $3FF7. See **9.3 Timer 1.**

4.3.5 Timer 2 Interrupt

Two timer 2 interrupts (TI2I and OC2I) share the same interrupt vector at $3FF4 and $3FF5. See **9.4.1 Timer Control Register 2.**

4.3.6 SSPI Interrupt

The SSPI transfer complete interrupt uses the vector at $3FF2 and $3FF3. See **Section 8. Simple Serial Peripheral Interface (SSPI)**.

4.3.7 Timebase Interrupt

The timebase interrupt uses the vector at $3FF0 and $3FF1. See **7.6 Timebase**.

4.4 Interrupt Control Register

Address: $0008

	Bit 7	6	5	4	3	2	1	Bit 0
Read: Write:	IRQ1E	IRQ2E	0	KWIE	IRQ1S	IRQ2S	0	0
Reset:	0	0	0	0	0	0	0	0

Figure 4-7. Interrupt Control Register (INTCR)

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IRQ1E — IRQ1 Interrupt Enable

The IRQ1E bit enables IRQ1 interrupt when IRQ1F is set. This bit is cleared on reset.

0 = IRQ1 interrupt disabled
1 = IRQ1 interrupt enabled

IRQ2E — IRQ2 Interrupt Enable

The IRQ2E bit enables IRQ2 interrupt when IRQ2F is set. This bit is cleared on reset.

0 = IRQ2 interrupt disabled
1 = IRQ2 interrupt enabled

Bit 5 — Reserved

This bit is not used and is always read as logic 0.

KWIE — Key Wakeup Interrupt (KWI) Enable

The KWIE bit enables key wakeup interrupt when KWIF is set. This bit is cleared on reset.

0 = KWI disabled
1 = KWI enabled

IRQ1S — IRQ1 Select Edge Sensitive Only

0 = IRQ1 configured for low level and negative edge sensitive
1 = IRQ1 configured to respond only to negative edges

IRQ2S — IRQ2 Select Edge Sensitive Only

0 = IRQ2 configured for low level and negative edge sensitive
1 = IRQ2 configured to respond only to negative edges

Bits 1 and 0 — Reserved

These bits are not used and always read as logic 0.

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4.5 Interrupt Status Register

Address: $0009

	Bit 7	6	5	4	3	2	1	Bit 0
Read:	IRQ1F	IRQ2F	0	KWIF	0	0	0	0
Write:					RIRQ1	RIRQ2		RKWIF
Reset:	0	0	0	0	0	0	0	0

= Unimplemented

Figure 4-8. Interrupt Status Register (INTSR)

IRQ1F — IRQ1 Interrupt Flag

When IRQ1S = 0, the falling edge or low level at the $\overline{\text{IRQ1}}$ pin sets IRQ1F. When IRQ1S = 1, only the falling edge sets the IRQ1F bit. If the IRQ1E bit and this bit are set, an interrupt is generated. This read-only bit is cleared by writing a logic 1 to the RIRQ1 bit. Reset clears this bit.

IRQ2F — IRQ2 Interrupt Flag

When IRQ2S = 0, the falling edge or low level at the $\overline{\text{IRQ2}}$ pin sets IRQ2F. When IRQ2S = 1, only the falling edge sets the IRQ2F bit. If the IRQ2E bit and this bit are set, an interrupt is generated. This read-only bit is cleared by writing a logic 1 to the RIRQ2 bit. Reset clears this bit.

Bit 5 — Reserved

This bit is not used and is always read as logic 0.

KWIF — Key Wakeup Interrupt Flag

When the KWIE*x* bit in the KWIEN register is set, the falling edge at the KWI*x* pin sets the KWIF bit. If the KWIE bit and this bit are set, an interrupt is generated. This read-only bit is cleared by writing a logic 1 to the RKWIF bit. Reset clears this bit.

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RIRQ1 — Reset IRQ1 Flag

The RIRQ1 bit is a write-only bit and is always read as logic 0. Writing a logic 1 to this bit clears the IRQ1F bit and writing logic 0 to this bit has no effect.

RIRQ2 — Reset IRQ2 Flag

The RIRQ2 bit is a write-only bit and is always read as logic 0. Writing a logic 1 to this bit clears the IRQ2F bit and writing a logic 0 to this bit has no effect.

Bit 1 — Reserved

This bit is not used and is always read as logic 0.

RKWIF — Reset KWI Flag

The RKWIF bit is a write-only bit and is always read as logic 0. Writing a logic 1 to this bit clears the KWIF bit and writing a logic 0 to this bit has no effect.

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Section 5. Low-Power Modes

5.1 Contents

5.2 Introduction

The MCU has two power-saving modes, stop and wait. Flowcharts of these modes are shown in **Figure 5-2**.

5.3 Stop Mode

The STOP instruction places the MCU in its lowest-power mode. In stop mode, the internal main oscillator OSC is turned off, halting all internal processing, including timer operations (timer 1, timer 2, and computer operating properly (COP) watchdog timer. Suboscillator XOSC does not stop oscillating. Therefore, if XOSC is used as the clock source for the COP watchdog timer, COP is still functional in stop mode. See **Section 7. Oscillators/Clock Distributions.**

During stop mode, the timer prescaler is cleared. The I bit in the condition code register (CCR) is cleared to enable external interrupts. All other registers and memory remain unaltered. All input/output lines remain unchanged. The processor can be brought out of stop mode only by $\overline{\text{RESET}}$ or an interrupt from $\overline{\text{IRQ1}}$, $\overline{\text{IRQ2}}$, $\overline{\text{KWI}}$, SSPI (slave mode only), or TBI. See **Section 7. Oscillators/Clock Distributions.**

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5.4 Wait Mode

The WAIT instruction places the MCU in a low-power mode, but wait mode consumes more power than stop mode. All CPU action is suspended, but on-chip peripherals and oscillators remain active. Any interrupt or reset (including a COP reset) will cause the MCU to exit wait mode.

During wait mode, the I bit in the CCR is cleared to enable interrupts. All other registers, memory, and input/output lines remain in their previous state. The timers may be enabled to allow a periodic exit from wait mode. Wait mode must be exited and the COP must be reset to prevent a COP timeout.

The reduction of power in wait mode depends on how many of the on-chip peripheral's clocks can be shut down. Therefore, the amount of power that will be consumed is dependent on the application, and it would be prohibitive to test all parts for all variations. For these reasons, the values given in **Section 12. Electrical Specifications** reflect typical application conditions after initial characterization of silicon.

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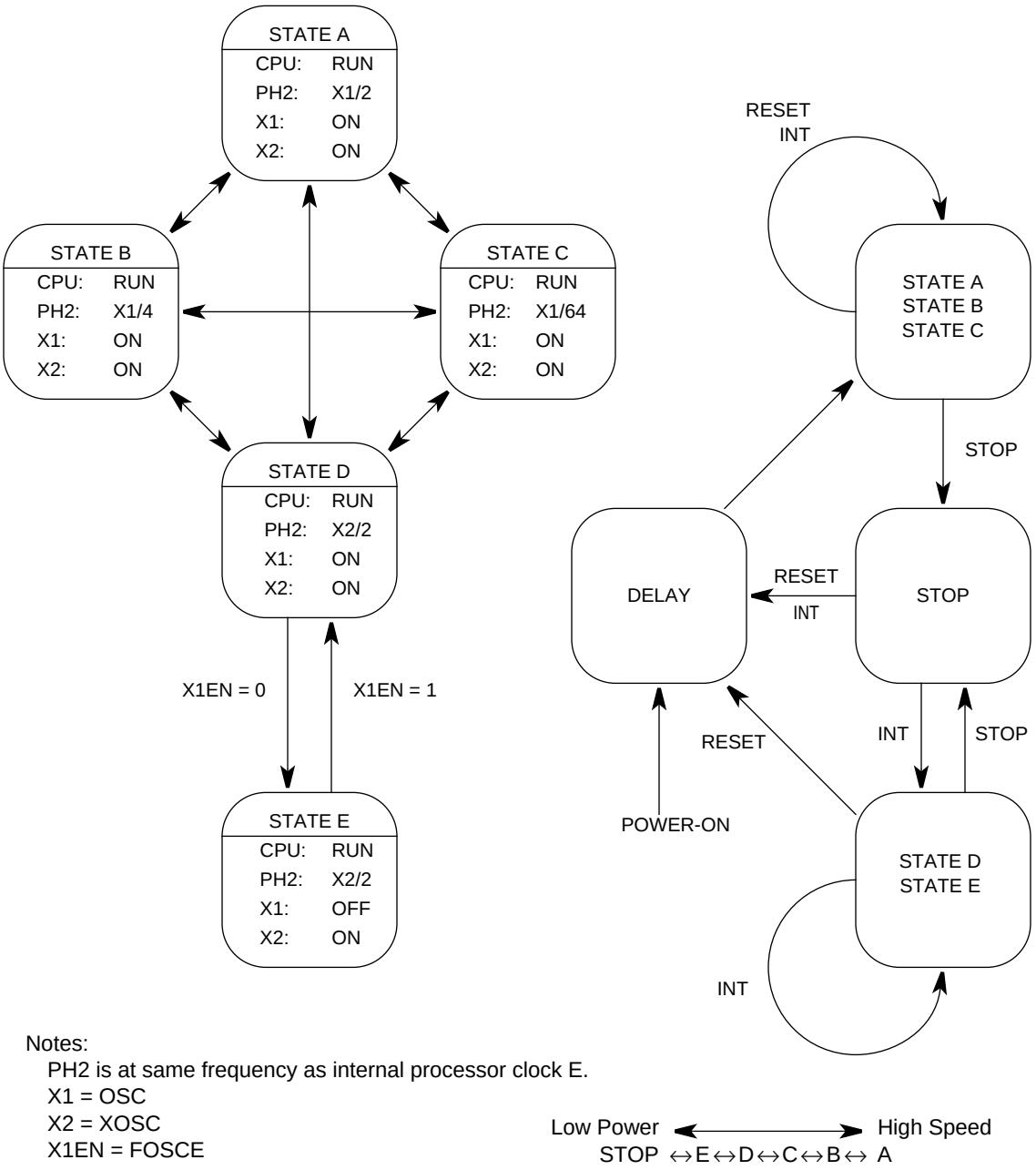

Figure 5-1. Clock State and STOP Recovery/Power-On Reset Delay Diagrams

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Low-Power Modes

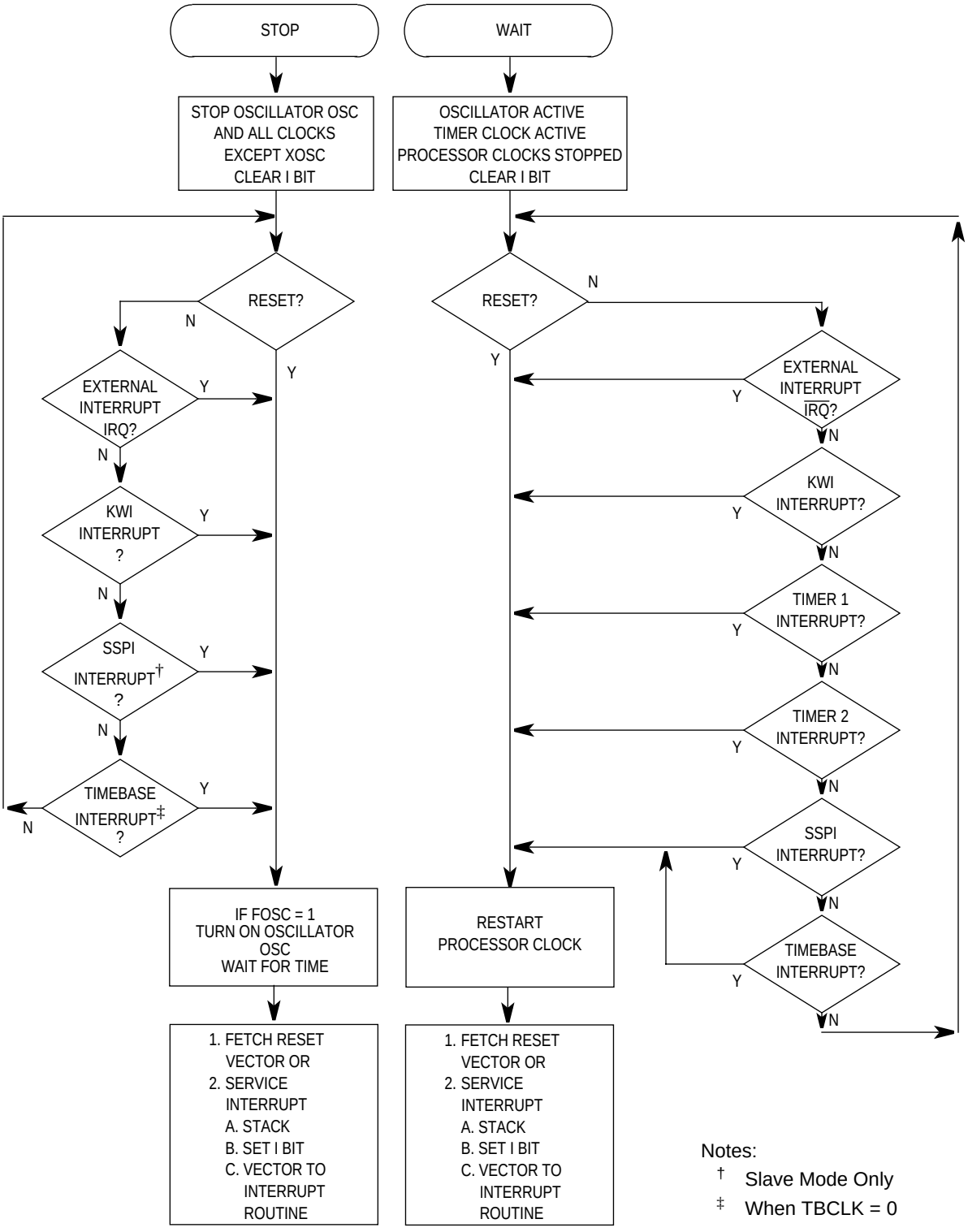

Figure 5-2. Stop/Wait Flowcharts

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Section 6. Parallel Input/Output (I/O)

6.1 Contents

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6.2 Introduction

The MCU has five parallel ports:

- Port A has eight input/output (I/O) pins.
- Port B has eight input-only pins.
- Port C has six I/O pins and tow input-only pins.
- Port D has seven output-only pins.
- Port E has eight output-only pins.

Most of these 39 I/O pins serve multiple purposes, depending on the configuration of the MCU system. The configuration is in turn controlled by hardware mode selection as well as internal control registers.

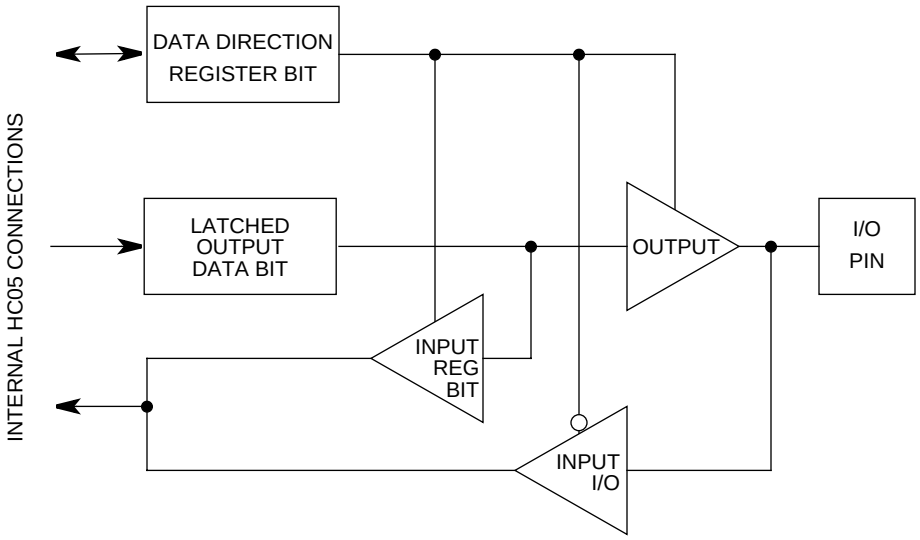

Figure 6-1. Port I/O Circuitry for One Bit

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6.3 Port A

Port A is an 8-bit, bidirectional, general-purpose port. The data direction of a port A pin is determined by its corresponding DDRA bit.

When a port A pin is programmed as an output by the corresponding DDRA bit, data in the PORTA data register becomes output data to the pin. This data is returned when the PORTA register is read.

Open drain or CMOS outputs are selected by AWOMH and AWOML bits in the WOM1 register. If the AWOMH bit is set, the P-channel drivers of bits 7–4 output buffers are disabled (open drain). If the AWOML bit is set, the P-channel drivers of bits 3–0 output buffers are disabled (open drain).

When a bit is programmed as input by the corresponding DDRA bit, the pin level is read by the CPU.

Port A has optional pullup resistors. When the RAH bit or RAL bit in the RCR1 is set, pullup resistors are attached to the upper four bits or lower four bits of port A pins, respectively. When a pin outputs a low level, the pullup resistor is disconnected regardless of the RAH or RAL bit state.

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6.3.1 Port A Data Register

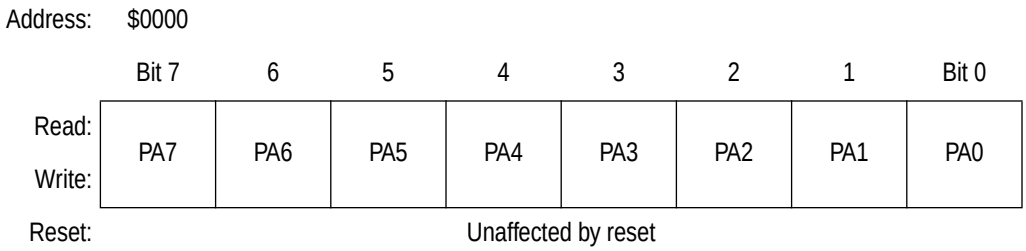

Figure 6-2. Port A Data Register (PORTA)

Read

Anytime; returns pin level if DDR set to input; returns output data latch if DDR set to output

Write

Anytime; data stored in an internal latch; drives pin only if DDR set for output

Reset

Becomes high-impedance inputs

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6.3.2 Port A Data Direction Register

Address: Option Map — $0000

	Bit 7	6	5	4	3	2	1	Bit 0
Read: Write:	DDRA7	DDRA6	DDRA5	DDRA4	DDRA3	DDRA2	DDRA1	DDRA0
Reset:	0	0	0	0	0	0	0	0

Figure 6-3. Port A Data Direction Register (DDRA)

Read

Anytime when OPTM = 1

Write

Anytime when OPTM = 1

Reset

Cleared to $00; all general-purpose I/O configured for input

DDRA*x* — Port A Data Direction Register Bit *x*

0 = Configure I/O pin PA*x* to input

1 = Configure I/O pin PA*x* to output

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6.4 Port B

Port B pins serve two basic functions: $\overline{\text{KWI}}$ input pins and general-purpose input pins.

Each $\overline{\text{KWI}}$ input is enabled or disabled by the corresponding KWIE*x* bit in the KWIEN register, and the usage of the $\overline{\text{KWI}}$ input does not affect the general-purpose input function.

Port B pin states may be read any time regardless of the configurations. Since there is no output drive logic associated with port B, there is no DDRB register and the write to the PORTB register has no meaning.

Port B has optional pullup resistors. When the RBH or RBL bit in the RCR1 is set, pullup resistors are attached to the upper four bits or lower four bits of port A pins, respectively.

Address: $0001

	Bit 7	6	5	4	3	2	1	Bit 0
Read: Write:	PB7	PB6	PB5	PB4	PB3	PB2	PB1	PB0
Reset:	Unaffected by reset							

Figure 6-4. Port B Data Register (PORTB)

Read

Anytime; returns pin level

Write

Has no meaning or effect

Reset

Unaffected; always an input port

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6.5 Port C

Port C pins share functions with several on-chip peripherals. A pin function is controlled by the enable bit of each associated peripheral.

Bit 7 and bit 6 of port C are input-only pins and IRQ input pins. Since IRQ1F or IRQ2F can be set by either the pins or the data latches, when using IRQs, be sure to clear the flags by software before enabling the IRQ1E or IRQ2E bits.

The PC5 pin is a general-purpose I/O pin and the direction of the pin is determined by the DDRC5 bit in the data direction register C (DDRC). When the event output (EVO) is enabled, the PC5 is configured as an event output pin and the DDRC5 bit has meaning only for the read of PC5 bit in the PORTC register; if the DDRC5 is set, the PC5 data latch is read by the CPU. Otherwise, PC5 pin level (EVO state) is read. When EVO is disabled, the DDRC5 bit decides the idling state of EVO (if DDRC5 = 1).

The PC4 and PC3 pins share functions with the timer input pins (EVI and TCAP). These bits are not affected by the usage of timer input functions and the directions of pins are always controlled by the DDRC4 and DDRC3 bits. Also, the DDRC4 and DDRC3 bits determine whether the pin states or data latch states should be read by the CPU.

NOTE: *Since the TCAP pin is shared with the PC3 I/O pin, changing the state of the PC3 DDR or data register can cause an unwanted TCAP interrupt. This can be handled by clearing the ICIE bit before changing the configuration of PC3 and clearing any pending interrupts before enabling ICIE.*

Since the EVI pin is shared with the PC4 I/O pin, DDRC4 should always be cleared whenever EVI is used. EVI should not be used when DDRC4 is high.

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The PC2–PC0 pins are shared with the simple serial peripheral interface (SSPI). When the SSPI is not used (SPE = 0), DDRC2–DDRC0 bits control the direction of the pins, and when the SSPI is enabled, the pins are configured as serial clock output or input (SCK), serial data output (SDO), and serial data input (SDI). The direction of the SCK depends on the MSTR bit in the SPCR. When PORTC is read, the value read will be determined by the data direction register. When the port is configured for input (DDRC2, DDRC1, or DDRC0 equal to logic 0), the pin state is read. When the port is configured for output (DDRC2, DDRC1, or DDRC0 equal to logic 0), the output data latch is read.

Port C has optional pullup resistors. When the RC*x* bit in the RCR2 is set, pullup resistors are attached to the PC*x* pin. When a pin outputs a low level, the pullup resistor is disconnected regardless of an RCR2 register bit being set

Bits 5–0 have open drain or CMOS output options, which are controlled by the corresponding WOM2 register bits. These open drain or CMOS output options may be selected for either the general-purpose output ports or the peripheral outputs (EVO, SCK, and SDO).

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6.5.1 Port C Data Register

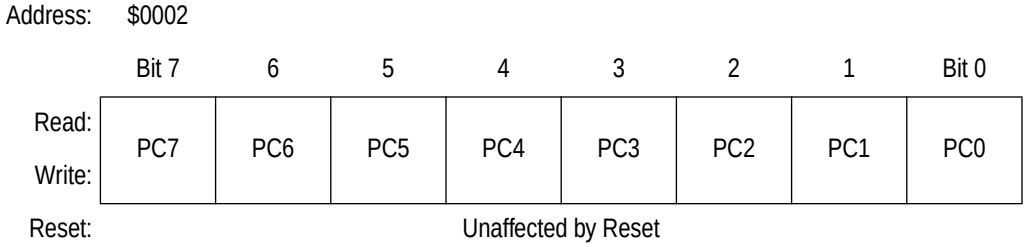

Figure 6-5. Port C Data Register (PORTC)

Read

Anytime; returns pin level if DDR set to input; returns output data latch if DDR set to output, PC7 and PC6 are input-only pins

Write

Anytime; data stored in an internal latch; drives pin only if DDR set for output; writes do not change pin state; when pin configured for SDO, SCK, and EVO peripheral output, bits 7 and 6 are read-only bits and write has no effect

Reset

Becomes high-impedance input

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6.5.2 Port C Data Direction Register

Address: Option Map — $0002

	Bit 7	6	5	4	3	2	1	Bit 0
Read: Write:	0	0	DDRC5	DDRC4	DDRC3	DDRC2	DDRC1	DDRC0
Reset:	0	0	0	0	0	0	0	0

Figure 6-6. Port C Data Direction Register (DDRC)

Read

Anytime when OPTM = 1

Write

Anytime when OPTM = 1; bits7 and 6 are read-only and write has no effect

Reset

Cleared to $00; all general-purpose I/O configured for input

Bits 7 and 6 — Not used

Always read logic 0

DDRC5–DDRC0 — Port C Data Direction Register Bit *x*

The timer and SSPI force the I/O state to be an output for each port C line associated with an enabled output function such as SDO and EVO. For these cases, the data direction bits will not change.

0 = Configure I/O pin PC*x* to input

1 = Configure I/O pin PC*x* to output

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6.6 Port D

Port D pins serve one of two basic functions, depending on the MCU mode selected:

- LCD frontplane and backplane driver outputs
- General-purpose output pins

Since port D is an output-only port, there is no DDRD register.

On reset, all port D outputs are disconnected from the pins and the port D data latches are set to a logic 1.

By writing a 1 the PDH bit in the LCD control register (LCDCR), LCD frontplanes drivers (FP35–FP38) are disabled and the upper four bits of port D output are connected to the pins.

The pin connections of the lower three bits of port D depend on the LCD duty selection by the DUTY1 and DUTY0 bits in the LCDCR. When the LCD duty is not 1/4, the unused backplane driver(s) is (are) replaced by the port D output pin(s) automatically.

If DWOMH bit or DWOML bit in the WOM1 register is set, the P-channel drivers of output buffers at the upper four bits or lower three bits, respectively, are disabled (open-drain mode). These open-drain controls do not apply to the pins which are configured as frontplane or backplane driver outputs.

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Address: $0003

	Bit 7	6	5	4	3	2	1	Bit 0
Read: Write:	PD7	PD6	PD5	PD4	PD3	PD2	PD1	1
Reset:	1	1	1	1	1	1	1	1

Figure 6-7. Port D Data Register (PORTD)

Read

Anytime; returns output data latch; bit 0 is always read logic 1

Write

Anytime; writes do not change pin state when configured for LCD driver output

Reset

All bits set to logic 1 and output ports disconnected from the pins; LCD is enabled on reset

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6.7 Port E

Port E pins serve one of two basic functions, depending on the MCU mode selected:

- LCD frontplane driver outputs
- General-purpose output pins

Since port E is an output-only port, there is no DDRE register.

On reset, all port E outputs are disconnected from the pins and the port E data latches are set to a logic 1.

The upper or lower four bits of port E output are connected to the pins instead of the LCD frontplane drivers by writing 1 to the PEH or PEL bit, respectively, in the LCD control register(LCDCR).

If EWOMH bit or EWOML bit in the WOM1 register is set, the P-channel driver of output buffers at the upper or lower four bits, respectively, are disabled (open-drain mode). These open-drain controls do not apply to the pins which are configured as frontplane driver outputs.

Address: $0004

	Bit 7	6	5	4	3	2	1	Bit 0
Read: Write:	PE7	PE6	PE5	PE4	PE3	PE2	PE1	PE0
Reset:	1	1	1	1	1	1	1	1

Figure 6-8. Port E Data Register (PORTE)

Read

Anytime; returns output data latch

Write

Anytime; writes do not change pin state when configured for LCD driver output

Reset

All bits set to logic 1 and output ports disconnected from the pins; LCD is enabled on reset

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Section 7. Oscillators/Clock Distributions

7.1 Contents

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7.2 Introduction

The two oscillator blocks are OSC and XOSC. Several combinations of the clock distributions are allowed for the modules in the MC68HC05L5. Refer to **Figure 7-1**.

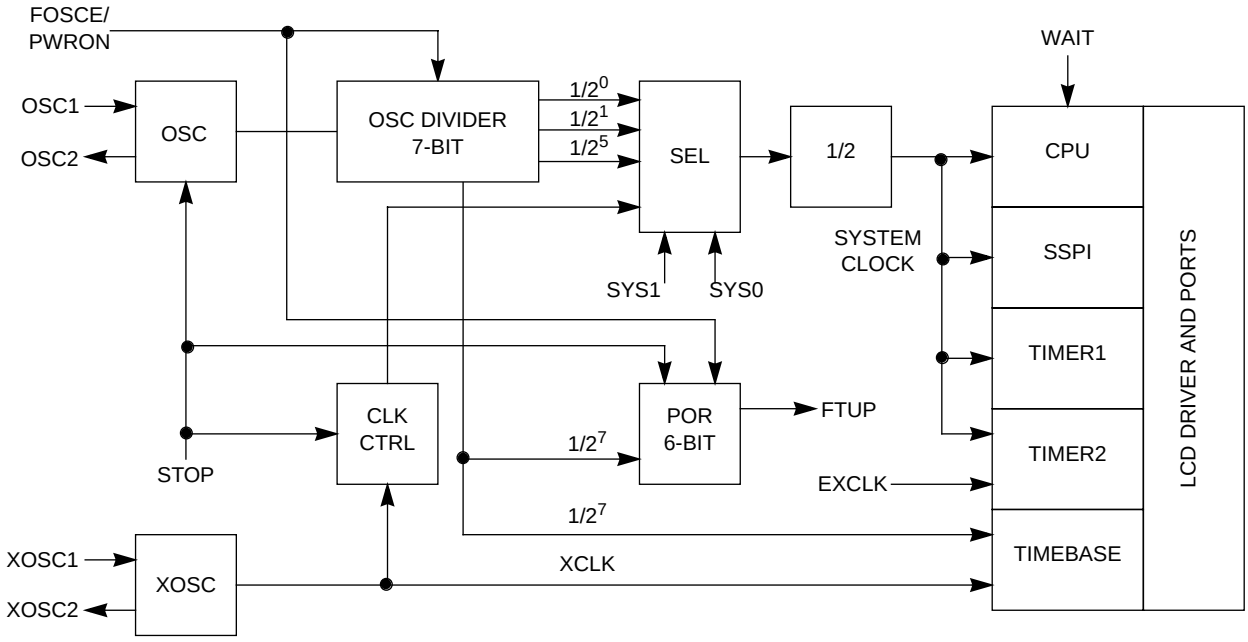

Figure 7-1. Clock Signal Distribution

7.3 OSC Clock Divider and POR Counter

The OSC clock is divided by a 7-bit counter which is used for the system clock, timebase, and power-on reset (POR) counter. Clocks divided by 2, 4, and 64 are available for the system clock selections and a clock divided by 128 is provided for the timebase and POR counter.

The POR counter is a 6-bit clock counter that is driven by the OSC divided by 128. The overflow of this counter is used for setting FTUP bit, releasing the POR, and resuming operation from stop mode.

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The 7-bit divider and POR counter are initialized to $0078 by two conditions:

- Power-on detection
- When FOSCE bit is cleared

7.4 System Clock Control

The system clock is provided for all internal modules except timebase. Both OSC and XOSC are available as the system clock source. The divide ratio is selected by the SYS1 and SYS0 bits in the MISC register. (See **Table 7-1**.)

By default, OSC divided by 64 is selected on reset.

NOTE: *Do not switch the system clock to XOSC (SYS1 and SYS0 = 11) when XOSC clock is not available. The XOSC clock is available when STUP flag is set.*

Do not switch the system clock to OSC (SYS1 and SYS0 = 00, 01, or 10) when OSC clock is not available. The OSC clock is available when FTUP flag is set.

Table 7-1. System Bus Clock Frequency Selection

SYS1	SYS0	Divide Ratio	CPU Bus Frequency (Hz)		
			OSC = 4.0 M	OSC = 4.1943 M	XOSC = 32.768 k
0	0	OSC ÷ 2	2.0 M	2.0972 M	—
0	1	OSC ÷ 4	1.0 M	1.0486 M	—
1	0	OSC ÷ 64	62.5 k	65.536 k	—
1	1	XOSC ÷ 2	—	—	16.384 k

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7.5 OSC and XOSC

The secondary oscillator (XOSC) runs continuously after power up. The main oscillator (OSC) can be stopped to conserve power via the STOP instruction or the FOSCE bit in the MISC register. The effects of restarting the OSC will vary depending on the current state of the MCU, including SYS0, SYS1, and FOSCE.

7.5.1 OSC on Line

If the system clock is OSC, FOSCE should remain logic 1. Executing the STOP instruction in this condition will halt OSC, put the MCU into a low-power mode and clear the 6-bit POR counter. The 7-bit divider is not initialized. Exiting STOP with external IRQ or reset re-starts the oscillator. When the POR counter overflows, internal reset is released and execution can begin. The stabilization time will vary between 8064 and 8192 counts.

NOTE: *Exiting STOP with external reset will always return the MCU to the state as defined by the default register definitions, for example, SYS0:SYS1 = 1:0, FOSCE = 1.*

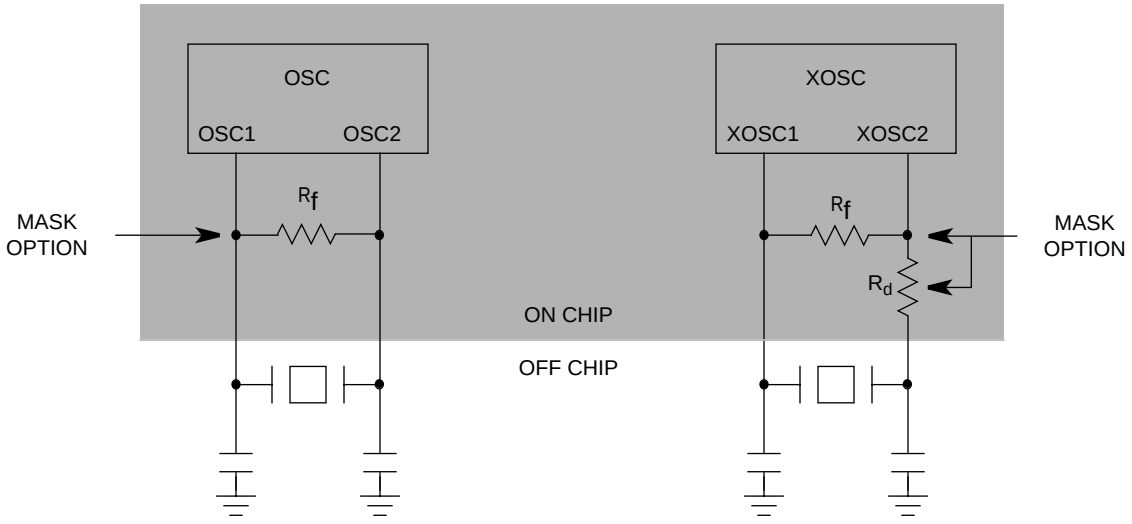

Figure 7-2. OSC1, OSC2, XOSC1, and XOSC2 Mask Options

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7.5.2 XOSC on Line

If XOSC is the system clock (SYS:SYS1 = 1:1), OSC can be stopped either by the STOP instruction or by clearing the FOSCE bit.

The suboscillator (XOSC) never stops except during power down. This clock also may be used as the clock source of the system clock and timebase. STUP bit indicates that the XOSC clock is available.

OSC and XOSC pins have options for feedback and damping resistor implementations. These options are set through mask option and may be read through the MOSR register.

NOTE: *When XOSC is not used, the XOSC1 input pin should be connected to the $\overline{RESET}$ pin.*

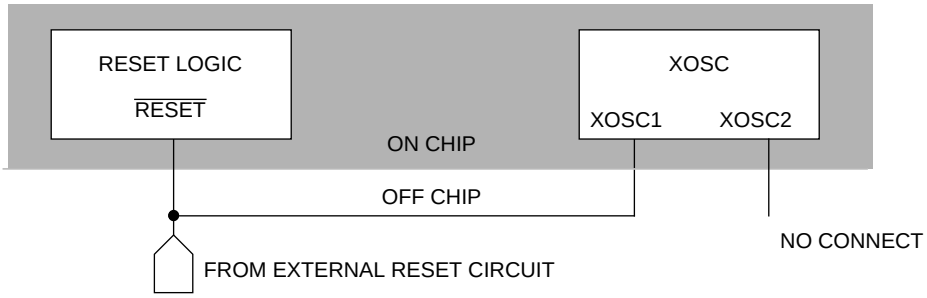

Figure 7-3. Unused XOSC1 Pin

7.5.2.1 XOSC with FOSCE = 1

If the system clock is XOSC and FOSCE = 1, executing the STOP instruction will halt OSC, put the MCU into a low-power mode and clear the 6-bit POR counter. The 7-bit divider is not initialized. Exiting STOP with external IRQ re-starts the oscillator; however, execution begins immediately using XOSC. When the POR counter overflows, FTUP is set, signaling that OSC is stable and OSC can be used as the system clock. The stabilization time will vary between 8064 and 8192 counts.

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7.5.2.2 XOSC with FOSCE = 0

If XOSC is the system clock, clearing FOSCE will stop OSC and preset the 7-bit divider and 6-bit POR counter to $0078. Execution will continue with XOSC and when FOSCE is set again, OSC will re-start. When the POR counter overflows, FTUP is set, signaling that OSC is stable and OSC can be used as the system clock. The stabilization time will be 8072 counts.

7.5.2.3 XOSC with FOSCE = 0 and STOP

If XOSC is the system clock and FOSCE is cleared, further power reduction can be achieved by executing the STOP instruction. In this case, OSC is stopped, the 7-bit divider and 6-bit POR counter are preset to $0078 (since FOSCE = 0) and execution is halted. Exiting STOP with external IRQ does not re-start the OSC; however, execution begins immediately using XOSC. OSC may be re-started by setting FOSCE. When the POR counter overflows, FTUP will be set, signaling that OSC is stable and can be used as the system clock. The stabilization time will be 8072 counts.

7.5.2.4 Stop Mode and Wait Mode

During stop mode, the main oscillator (OSC) is shut down and the clock path from the second oscillator (XOSC) is disconnected. All modules except timebase are halted. Entering stop mode clears the FTUP flag in the MISC register and initializes the POR counter. Stop mode is exited by $\overline{\text{RESET}}$, $\overline{\text{IRQ1}}$, $\overline{\text{IRQ2}}$, $\overline{\text{KWI}}$, SSPI (slave mode), or timebase interrupt.

If OSC is selected as the system clock source during stop mode, CPU resumes after the overflow of the POR counter and this overflow also sets the FTUP status flag.

If XOSC is selected as the system clock source during stop mode, no stop recovery time is required for exiting stop mode because XOSC never stops. Re-start of the main oscillator depends on the FOSCE bit.

During wait mode, only the CPU clocks are halted and the peripheral modules are not affected. Wait mode is exited by $\overline{\text{RESET}}$ and any interrupts.

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Table 7-2. Recovery Time Requirements

Before Reset or Interrupt			Power-On Reset	External Reset	Exit Stop Mode by Interrupt
CPU Clock Source	Stop	FOSCE			
—	—	—	Wait	—	—
OSC (OSC on)	Out	1	—	No wait	—
OSC (OSC off)	Out In In(1)	0(2) 1 0(1)	— — —	Wait Wait Wait	— Wait Wait
XOSC (OSC on)	Out	1	—	No wait	—
XOSC (OSC off)	Out In In	0 1 0	— — —	Wait Wait Wait	— No wait No wait

Notes:

1. This case never occurs.
2. This case has no meaning for the applications.

7.6 Timebase

Timebase is a 14-bit up-counter which is clocked by XOSC input or OSC input divided by 128. TBCLK bit in the TBCR1 register selects the clock source.

This 14-bit divider is initialized to $0078 only upon power-on reset (POR). After counting 8072 clocks, the STUP bit in the MISC register is set.

The divided clocks from the timebase are used for LCDCLK, STUP, TBI, and COP. (See **Figure 7-4**).

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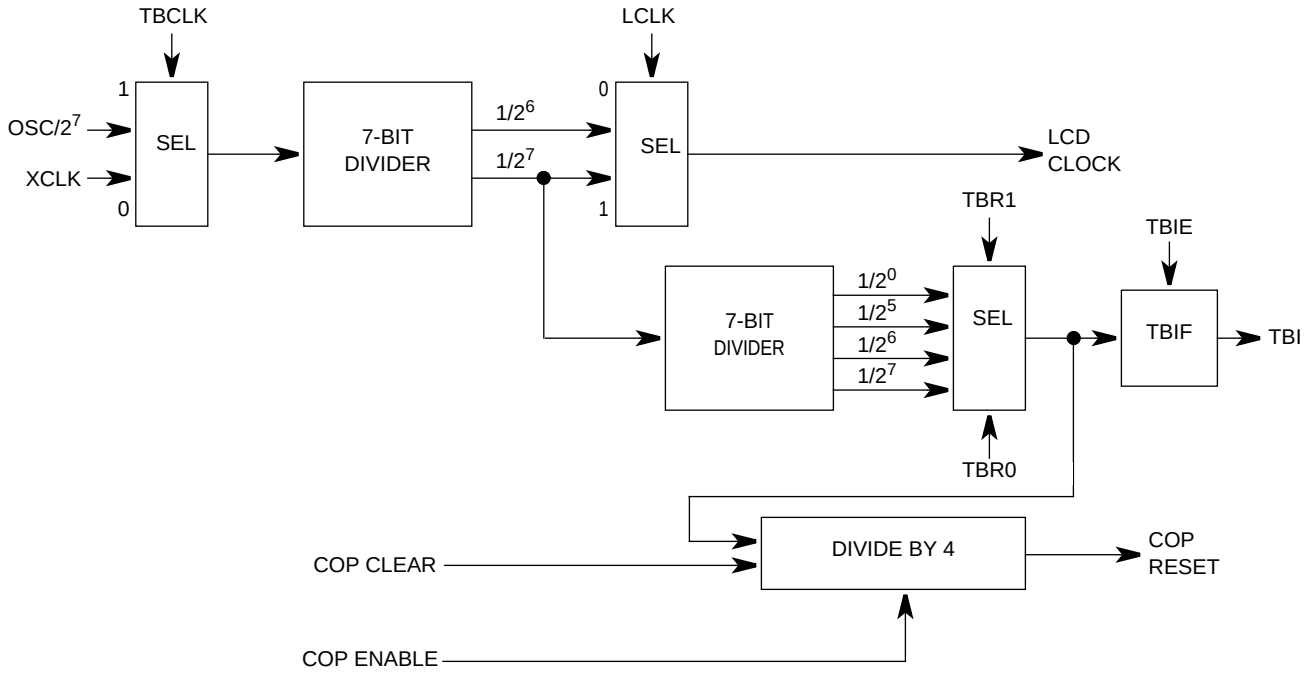

Figure 7-4. Timebase Clock Divider

7.6.1 LCDCLK

The clocks divided by 64 and 128 are used as LCD clocks at the LCD driver module, and clocks are selected by the LCLK bit in the TBCR1.

7.6.2 STUP

Timebase divider is initialized to $0078 by the power-on detection and when the count reaches 8072, the STUP flag in the MISC register is set. Once the STUP flag is set, it is never cleared until power down.

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7.6.3 TBI

Timebase interrupts may be generated every 0.5, 0.25, 0.125, or 0.0039 seconds with a 32.768-kHz crystal at XOSC pins.

The timebase interrupt flag (TBIF) is set every period and interrupt is requested if the enable bit (TBIE) is set. The clock divided by 128, 4096, 8192, or 16,384 is used to set TBIF, and this clock is selected by the TBR1 and TBR0 bits in the TBCR2 register. (See **Table 7-3**.)

Table 7-3. Timebase Interrupt Frequency

TBCR2		Divide Ratio	Frequency (Hz)		
TBR1	TBR0		OSC = 4.0 M	OSC = 4.1943 M	XOSC = 32.768 k
0	0	TBCLK ÷ 128	244	256	256
0	1	TBCLK ÷ 4096	7.63	8.00	8.00
1	0	TBCLK ÷ 8192	3.81	4.00	4.00
1	1	TBCLK ÷ 16,384	1.91	2.00	2.00

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7.6.4 COP

The computer operating properly (COP) watchdog timer is controlled by the COPE and COPC bits in the TBCR2 register.

The COP uses the same clock as TBI that is selected by the TBR1 and TBR0 bits. The TBI is divided by four and overflow of this divider generates COP timeout reset if the COP enable (COPE) bit is set. The COP timeout reset has the same vector address as POR and external $\overline{\text{RESET}}$. To prevent the COP timeout, the COP divider is cleared by writing a logic 1 to the COP clear (COPC) bit.

When the timebase divider is driven by the OSC clock, clock for the divider is suspended during stop mode or when FOSCE is a logic 0. This may cause COP period stretching or no COP timeout reset when processing errors occur. To avoid these problems, it is recommended that the XOSC clock be used for the COP functions.

When the timebase (COP) divider is driven by the XOSC clock, the divider does not stop counting and the COPC bit must be triggered to prevent the COP timeout.

Table 7-4. COP Timeout Period

TBCR2		COP Period (ms)					
TBR1	TBR0	OSC = 4.0 MHz		OSC = 4.1943 MHz		XOSC = 32.768 kHz	
		Min	Max	Min	Max	Min	Max
0	0	12.3	16.4	11.7	15.6	11.7	15.6
0	1	393	524	375	500	375	500
1	0	786	1048	750	1000	750	1000
1	1	1573	2097	1500	2000	1500	2000

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7.6.5 Timebase Control Register 1

Address: $0010

	Bit 7	6	5	4	3	2	1	Bit 0
Read: Write:	TBCLK	0	LCLK	0	0	0	T2R1	T2R0
Reset:	0	0	0	0	0	0	0	0

Figure 7-5. Timebase Control Register 1 (TBCR1)

Read

Anytime

Write

Anytime; only one write is allowed on bit 7 after reset

TBCLK — Timebase Clock

The TBCLK bit selects the timebase clock source. This bit is cleared on reset. After reset, a write to this bit is allowed only once.

0 = XOSC clock selected
1 = OSC clock divided by 128 selected

Bit 6 — Reserved

This bit is not used and always reads as logic 0.

LCLK — LCD Clock

The LCLK bit selects the clock for the LCD driver. This bit is cleared on reset.

0 = Divide by 64 selected
1 = Divide by 128 selected

Bits 4–2 — Reserved

These bits are not used and always read as logic 0.

T2R1 and T2R0 — Timer 2 Prescale Rate Select Bits

T2R1 and T2R0 select timer 2 clock rate. See **9.4 Timer 2** for more detail.

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7.6.6 Timebase Control Register 2

Address: $0011

	Bit 7	6	5	4	3	2	1	Bit 0
Read:	TBIF	TBIE	TBR1	TBR0	0	0	0	0
Write:					RTBIF		COPE	COPC
Reset:	0	0	1	1	0	0	0	0

= Unimplemented

Figure 7-6. Timebase Control Register 2 (TBCR2)

Read

Anytime; bits 3 and 0 are write-only bits and always read as logic 0

Write

Anytime; bit 7 is a read-only bit and write has no effect; bit 1 is 1-time write bit

TBIF — Timebase Interrupt Flag

The TBIF bit is set every timeout interval of the timebase counter. This read-only bit is cleared by writing a logic 1 to the RTBIF bit. Reset clears the TBIF bit. The timebase interrupt period between reset and the first TBIF depends on the time elapsed during reset, since the timebase divider is not initialized on reset.

TBIE — Timebase Interrupt Enable

The TBIE bit enables the timebase interrupt capability. If TBIF = 1 and TBIE = 1, the timebase interrupt is generated.

0 = Timebase interrupt disabled
1 = Timebase interrupt requested when TBIF = 1

TBR1 and TBR0 — Timebase Interrupt Rate Select

The TBR1 and TBR0 bits select one of four rates for the timebase interrupt period (see **Table 7-3**). The TBI rate is also related to the COP timeout reset period. These bits are set to logic 1 on reset.

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Table 7-5. Timebase Interrupt Frequency

TBCR2		Divide Ratio	Frequency (Hz)		
TBR1	TBR0		OSC = 4.0 M	OSC = 4.1943 M	XOSC = 32.768 k
0	0	TBCLK ÷ 128	244	256	256
0	1	TBCLK ÷ 4096	7.63	8.00	8.00
1	0	TBCLK ÷ 8192	3.81	4.00	4.00
1	1	TBCLK ÷ 16,384	1.91	2.00	2.00

RTBIF — Reset Timebase Interrupt Flag

The RTBIF bit is a write-only bit and is always read as logic 0. Writing logic 1 to this bit clears the TBIF bit and writing logic 0 to this bit has no effect.

Bit 2 — Reserved

This bit is not used and is always read as logic 0.

COPE — COP Enable

When the COPE bit is logic 1, the COP reset function is enabled. This bit is cleared on reset (including COP timeout reset) and write to this bit is allowed only once after reset.

COPC — COP Clear

Writing logic 1 to the COPC bit clears the 2-bit divider to prevent COP timeout. (The COP timeout period depends on the TBI rate.) This bit is write-only and returns to logic 0 when read.

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7.6.7 Miscellaneous Register

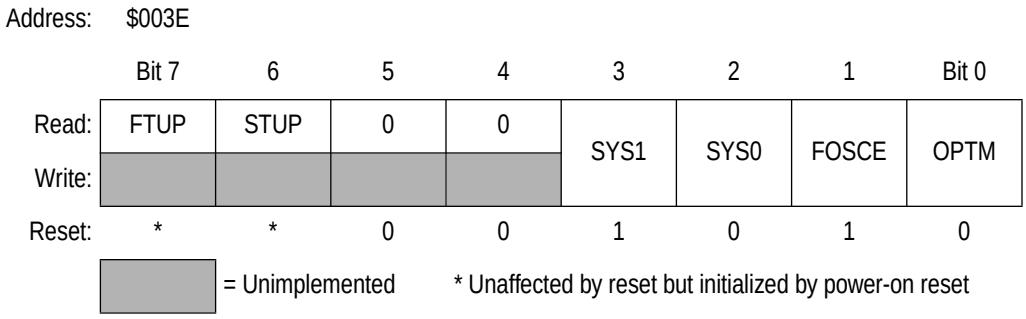

Figure 7-7. Miscellaneous Register (MISC)

FTUP — OSC Time Up Flag

Power-on detection and clearing the FOSCE bit clears this read-only bit. This bit is set by the overflow of the POR counter. Reset does not affect this bit.

0 = During POR or OSC shut down
1 = OSC clock available for the system clock

STUP — XOSC Time Up Flag

Power-on detection clears this read-only bit. This bit is set after the timebase has counted 8072 clocks. Reset does not affect this bit.

0 = XOSC not stabilized or no signal on XOSC1 and XOSC2 pins
1 = XOSC clock available for the system clock

Bits 5 and 4 — Reserved

These bits are not used and always read as logic 0.

SYS1 and SYS0 — System Clock Select

These two bits select the system clock source. On reset, the SYS1 and SYS0 bits are initialized to 1 and 0, respectively.

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NOTE: *Do not switch the system clock to XOSC (SYS1 and SYS0 = 11) when the XOSC clock is not available. The XOSC clock is available when the STUP flag is set.*

Do not switch the system clock to OSC (SYS1 and SYS 0 = 00, 01, or 10) when the OSC clock is not available. The OSC clock is available when the FTUP flag is set.

Table 7-6. System Bus Clock Frequency Selection

SYS1	SYS0	Divide Ratio	CPU Bus Frequency (Hz)		
			OSC = 4.0 M	OSC = 4.1943 M	XOSC = 32.768 k
0	0	OSC ÷ 2	2.0 M	2.0972 M	—
0	1	OSC ÷ 4	1.0 M	1.0486 M	—
1	0	OSC ÷ 64	62.5 k	65.536 k	—
1	1	XOSC ÷ 2	—	—	16.384 k

FOSCE — Fast (Main) Oscillator Enable

The FOSCE bit controls the main oscillator activity. This bit should not be cleared by the CPU when the main oscillator is selected as the system clock source.

When this bit is cleared:

1. OSC is shut down.
2. 7-bit dividers at the OSC input and POR counter are initialized to $0078.
3. FTUP flag is cleared.

When this bit is set:

1. Main oscillator starts again.
2. FTUP flag is set by the POR counter overflow (8072 clocks).

OPTM — Option Map Select

The OPTM bit selects one of two register maps at $0000–$000F. This bit is cleared on reset.

0 = Main register map selected
1 = Option map selected

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Section 8. Simple Serial Peripheral Interface (SSPI)

8.1 Contents

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8.2 Introduction

The simple serial peripheral interface (SSPI) of the MC68HC05L5 is a master/slave synchronous serial communication module.

SSPI uses a 3-wire protocol: data input, data output, and serial clock. In this format, the clock is not being included in the data stream and must be provided as a separate signal.

When the SSPI is enabled (SPE = 1), bits 0–2 of port C become SDI (serial data in), SDO (serial data out), and SCK (serial clock) pins. The corresponding DDRC bit does not change the direction of the pin.

The MSTR bit decides the SSPI operation mode. The SCK pin is configured as output in master mode and configured as input in slave mode.

The DORD bit in the serial peripheral control register (SPCR) selects the data transmission order. When DORD is set, the least significant bit (LSB) of serial data is shifted out/in first. When the DORD is clear, serial data is shifted from/to the most significant bit (MSB).

Master serial clock speed is selected by the SPR bit in the SPCR. An interrupt may be generated by the completion of a transfer.

8.3 Features

Features of the SSPI are:

- Full-duplex, 3-wire synchronous transfers
- Master or slave operation
- Programmable data transmission order, LSB or MSB first
- 1.05-MHz (maximum) transmission bit frequency at 2.1-MHz CPU bus frequency at 5 Vdc
- Two programmable transmission bit rates
- End-of-transmission interrupt flag
- Wakeup from stop mode (slave mode only)

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8.4 Functional Descriptions

In master mode, the clock start logic is triggered by the CPU (detection of a CPU write to the 8-bit shift register (SPDR)). The SCK is based on the internal processor clock. This clock is also used in the 3-bit counter and 8-bit shift register. See **Figure 8-2**.

When data is written to the 8-bit shift register of the master device, it is then shifted out to the SDO pin for application to the slave device. At the same time, data applied from the slave device via the SDI pin is shifted into the 8-bit shift register.

After 8-bit data is shifted in/out, SCK stops and SPIF is set. If SPIE is enabled, an interrupt request is generated. The slave device in stop mode wakes up by this interrupt. Further transfers (writes to SPDR) are inhibited while SPIF is a logic 1.

The master-slave basic interconnection is illustrated in **Figure 8-1**.

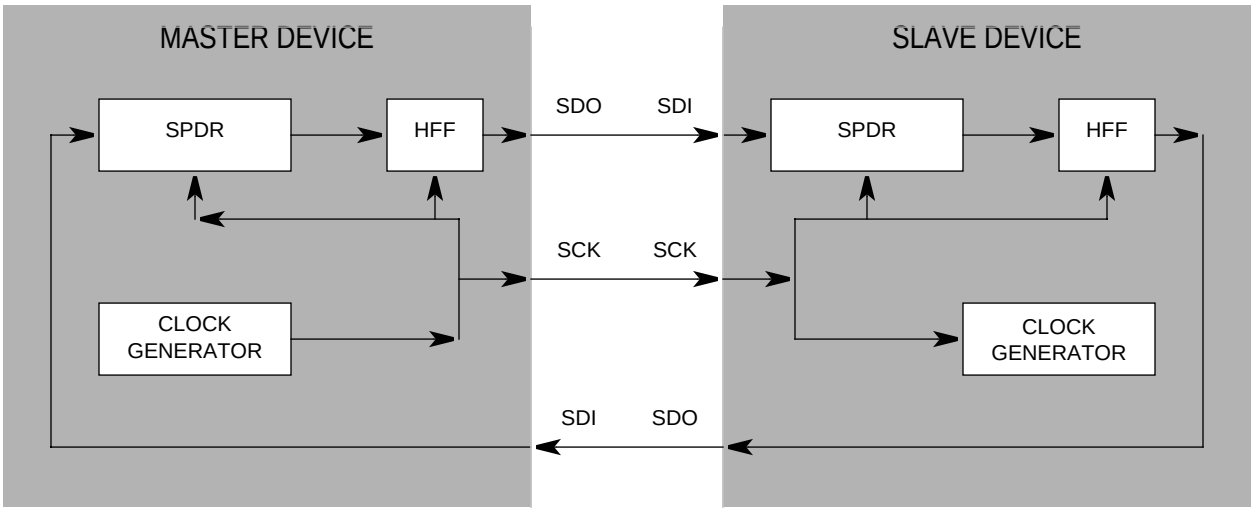

Figure 8-1. SSPI Master-Slave Interconnection

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8.5 Internal Block Descriptions

The following paragraphs describe the main blocks in the SSPI module. (See **Figure 8-2**).

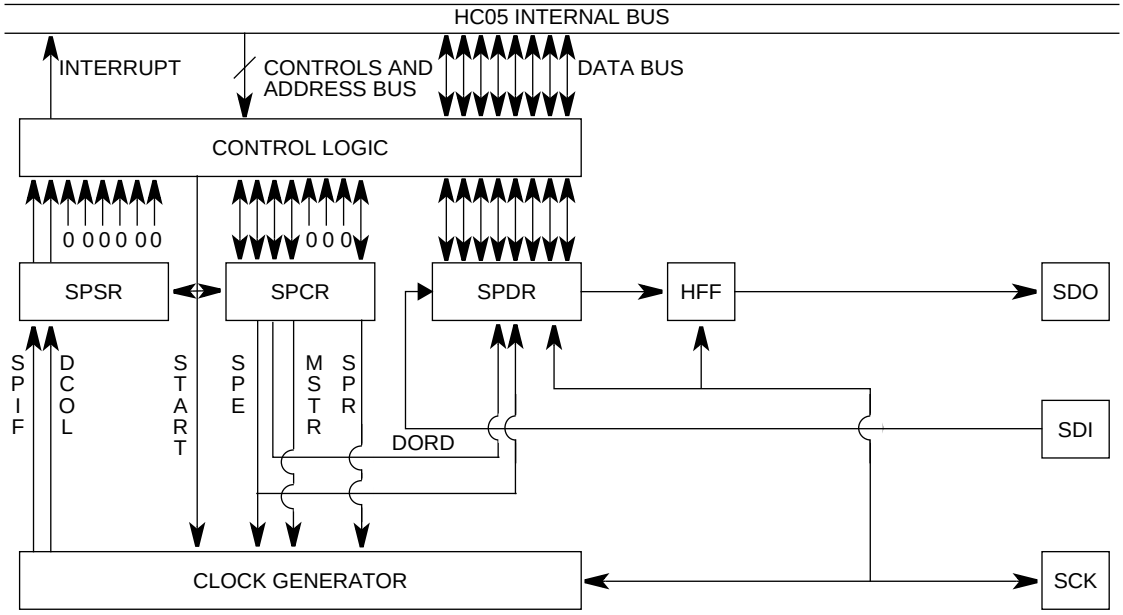

Figure 8-2. SSPI Block Diagram

8.5.1 Control

This block is an interface to the HC05 internal bus and generates a start signal when a write to the SPDR is detected in master mode. It also generates an interrupt request to the CPU.

8.5.2 SPDR

This serial peripheral data register (SPDR) is an 8-bit shift register. The DORD bit in the SPCR determines the bus connection between the internal data bus and SPDR. This register can be read and written by the CPU.

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8.5.3 SPCR

Bits in the serial peripheral control register (SPCR) control SSPI functions.

8.5.4 SPSR

The serial peripheral status register (SPSR) mainly sets flags such as SPIF and DCOL.

8.5.5 CLKGEN

In master mode, this block generates SCK when the CPU writes to the data register (SPDR) and the clock rate is selected by the SPR bit in the control register.

In slave mode, the external clock from the SCK pin is used instead of the master mode clock, and SPR has no affect.

This clock generator includes a 3-bit clock counter. Overflow of this counter sets SPIF.

8.6 Signal Descriptions

Three basic signals — SDI, SDO, and SCK — are described in the following subsections. The relationship among SCK, SDI, and SDO is shown in **Figure 8-3**.

8.6.1 SSPI Data I/O (SDI and SDO)

The two serial data lines — SDI for input and SDO for output — are connected to PC0 and PC1, respectively, when SSPI is enabled (SPE = 1).

At the falling edge of SCK, a serial data bit is transmitted out of the SDO pin. At the rising edge of SCK, a serial data bit on the SDI pin is sampled internally.

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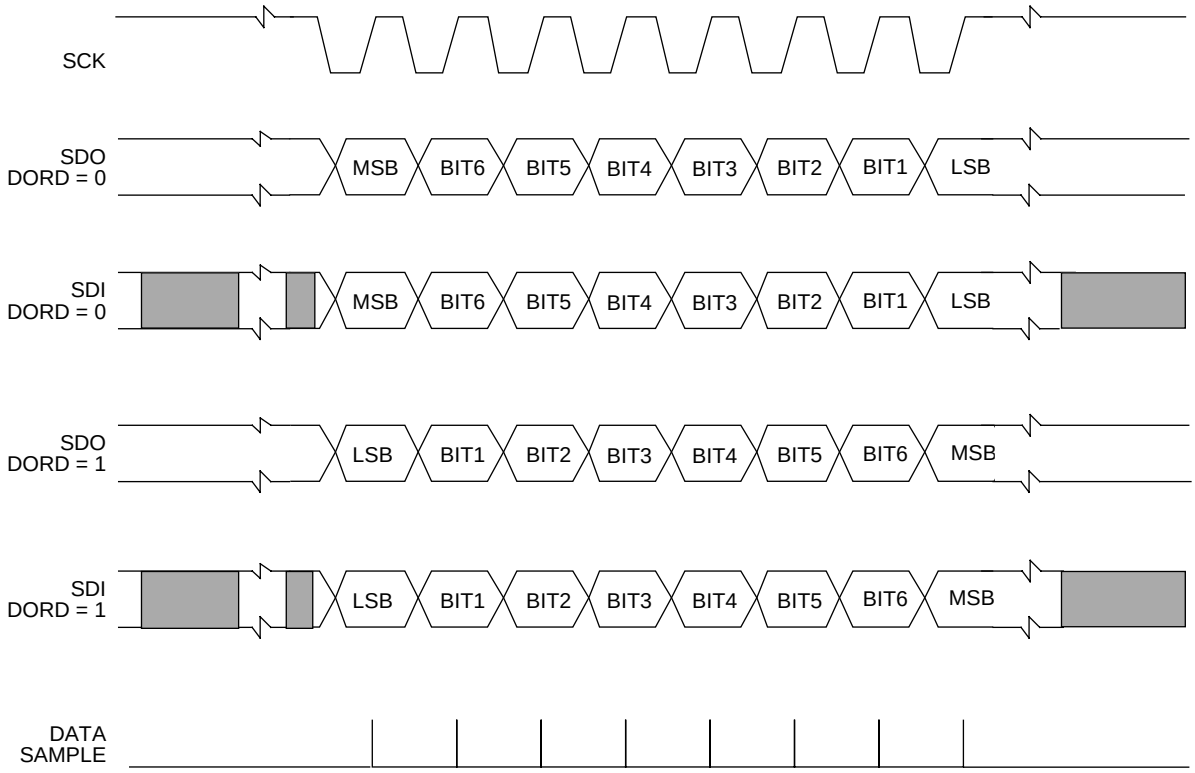

Figure 8-3. SSPI Clock-Data Timing Diagram

When data is transmitted to other devices via the SDO line, the receiving data is shifted into the shift register through the SDI pin. This implies full-duplex transmission with both data-out and data-in synchronized with the same clock signal. Thus, the byte transmitted is replaced by the byte received and eliminates the need for separate transmit-empty and receiver-full status bits. A single status bit, SPIF, is used to signify the completion of data transfer.

8.6.2 Serial Clock (SCK)

SCK is used for synchronization of both input and output data streams through its SDI and SDO pins.

The master and slave devices are capable of exchanging a data byte during a sequence of eight clock pulses. Since the SCK is generated by

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the master, slave data transfer is accomplished by synchronization to SCK.

The master generates the SCK through a circuit driven by the internal processor clock and uses the SCK to latch incoming slave device data on the SDI pin and shift out data to the slave via the SDO pin. The SPR bit in the SPCR of the master selects the transmission clock rate.

The slave device receives the SCK from the master device, and uses the SCK to latch incoming master device data on the SDI pin and shifts out data to the master via the SDO pin. The SPR bit in the SPCR of the slave has no meaning.

NOTE: *PC2/SCK should be at V_{DD} level before SSPI is enabled. This can be done with an internal or external pullup resistor or by setting DDRC2 = 1 and PC2 = 1 prior to enabling the SSPI. Otherwise, the circuit will not initialize correctly.*

8.7 Registers

Three registers are in the SSPI provide control, status, and data storage functions. They are:

- Serial peripheral control register, SPCR location $000A
- Serial peripheral status register, SPSR location $000B
- Serial peripheral data register, SPDR location $000C

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8.7.1 Serial Peripheral Control Register

Address: $000A

	Bit 7	6	5	4	3	2	1	Bit 0
Read: Write:	SPIE	SPE	DORD	MSTR	0	0	0	SPR
Reset:	0	0	0	0	0	0	0	0

Figure 8-4. Serial Peripheral Control Register (SPCR)

SPIE — SSPI Interrupt Enable

If the serial peripheral interrupt enable (SPIE) bit is set, an interrupt is generated when SPIF in the SPSR is set and I bit (interrupt mask bit) in the condition code register (CCR) is clear.

During stop mode, an SSPI request is accepted only in slave mode. Interrupt in master mode will be pending until stop mode is exited. STOP instruction does not change SPIF and SPIE.

0 = Disable SSPI interrupt
1 = Enable SSPI interrupt

SPE — SSPI Enable

When the SSPI enable (SPE) bit is set, the SSPI system is enabled and connected to the port C pins.

Clearing the SPE bit initializes all control logic in the SSPI modules and disconnects the SSPI from port C pins.

This bit is cleared on reset.

0 = Disable SSPI
1 = Enable SSPI

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DORD — Data Transmission ORDer

When this bit is set, the data in the 8-bit shift register (SPDR) is shifted in/out from the LSB. When this bit is cleared, the data in the SPDR is shifted in/out from the MSB.

This bit is cleared on reset.

0 = MSB first
1 = LSB first

MSTR — MaSTeR Mode Select

The MSTR bit determines whether the device is in master mode or slave mode.

In master mode (MSTR = 1), the SCK pin is configured as an output and the serial clock is generated by the internal clock generator when the CPU writes to the SPDR.

In slave mode (MSTR = 0), the SCK pin is configured as an input and the serial clock is applied externally. This bit is cleared on reset.

0 = Slave mode
1 = Master mode

Bits 3–1 — Reserved

These bits are not used and are fixed to 0.

SPR — SSPI Clock Rate Select

This serial peripheral clock rate bit selects one of two bit rates of SCK. This bit is cleared on reset.

0 = Internal processor clock divided by 2
1 = Internal processor clock divided by 16

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8.7.2 Serial Peripheral Status Register

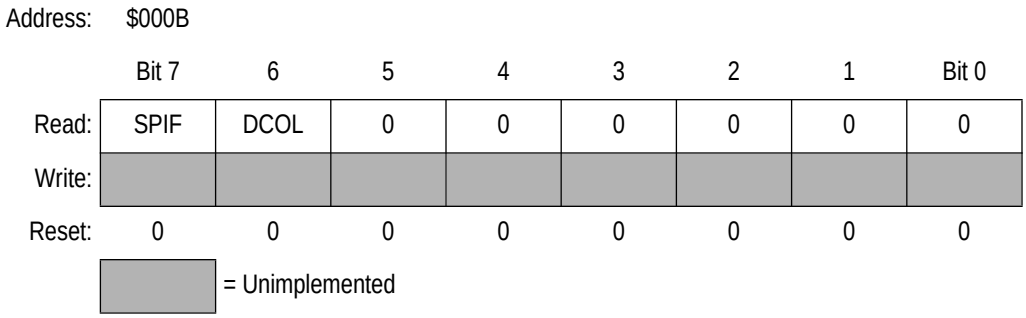

Figure 8-5. Serial Peripheral Status Register (SPSR)

SPIF — Serial Transfer Complete Flag

The serial peripheral data transfer complete flag bit notifies the user that a data transfer between the MC68HC05L5 and an external device has been completed. With the completion of the data transfer, the rising edge of the eighth pulse sets SPIF, and if SPIE is set, SSPI is generated. However, during STOP, the interrupt request is serviced only in slave mode. STOP execution never affects the SPIF flag or SPIE.

When SPIF is set, the ninth clock from the clock generator or from the SCK pin is inhibited.

Clearing the SPIF bit is done by a software sequence of accessing the SPSR while the SPIF bit is set followed by accessing SPDR (8-bit shift register). This also clears the DCOL bit. While SPIF is set, all writes to the SPDR are inhibited until SPSR is read by the CPU.

The SPIF bit is a read-only bit and is cleared on reset.

0 = Data transfer not complete
1 = Data transfer complete

DCOL — Data COLlision

The data collision bit notifies the user that an attempt was made to write or read the serial peripheral data register while a data transfer was taking place with an external device. The transfer continues uninterrupted; therefore, a write will be unsuccessful, and a data read will be incorrect.

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A data collision only sets the DCOL bit and does not generate an SSPI interrupt. The DCOL bit indicates only the occurrence of data collision.

Clearing the DCOL bit is done by a software sequence of accessing the SPSR while SPIF is set followed by accessing the SPDR. Both the SPIF and DCOL bits will be cleared by this sequence.

The DCOL bit is cleared on reset.

0 = No data collision
1 = Data collision occurred

Bits 5–0 — Reserved

These bits are not used and are fixed to 0.

8.7.3 Serial Peripheral Data Register

Address: $000C

	Bit 7	6	5	4	3	2	1	Bit 0
Read: Write:	MSB	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 2	LSB
Reset:	Unaffected by Reset							

Figure 8-6. Serial Peripheral Data Register (SPDR)

Read

A read during transmission causes DCOL to be set.

Write

A write during transmission causes DCOL to be set.

The SPDR is used to transmit and receive data on the serial bus.

In master mode, a write to this register initiates transmission/reception of a data byte.

The SPIF status bit is set at the completion of data byte transmission. A write to the SPDR is inhibited while this register is shifting (a write

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attempt sets DCOL) or when the SPIF bit is set without reading SPSR. Data collision never affects the receiving and transmitting data in SPDR.

A write or read of the SPDR after accessing the SPSR with SPIF set will clear the SPIF and DCOL bits.

The ability to access the SPDR is inhibited when a transmission is taking place. It is important to read the discussion defining the DCOL and SPIF bits to understand the limits on using the SPDR.

When SSPI is not used (SPE = 0), the SPDR can be used as a general-purpose data storage register.

8.8 Port Function

The SSPI shares I/O pins with PC0–PC2. When SPE is set, PC0 becomes SDI input, PC1 becomes SDO output and PC2 becomes SCK. The direction of SCK depends on the MSTR bit. Setting DDRC bits 0–2 does not change the data direction of the pin to output, but instead changes the source of data when PC0–PC2 is read. If DDRC*x* = 1, port C bit *x* data latch is read and if DDRC*x* = 0, PORTC*x* pin level is read by the CPU.

When SPE is clear, SSPI is disconnected from the I/O pins and PC0–PC2 are used as general-purpose I/O pins. See **6.5 Port C.**

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Section 9. Timer System

9.1 Contents

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9.2 Introduction

The MC68HC05L5 has two timer modules: timer 1 with a 16-bit counter and timer 2 with an 8-bit counter. Timer 1 has one input pin (TCAP) and no output pin. Timer 2 has one input pin (EVI) and one output pin (EVO). **Figure 9-1** illustrates the timer system of the MC68HC05L5.

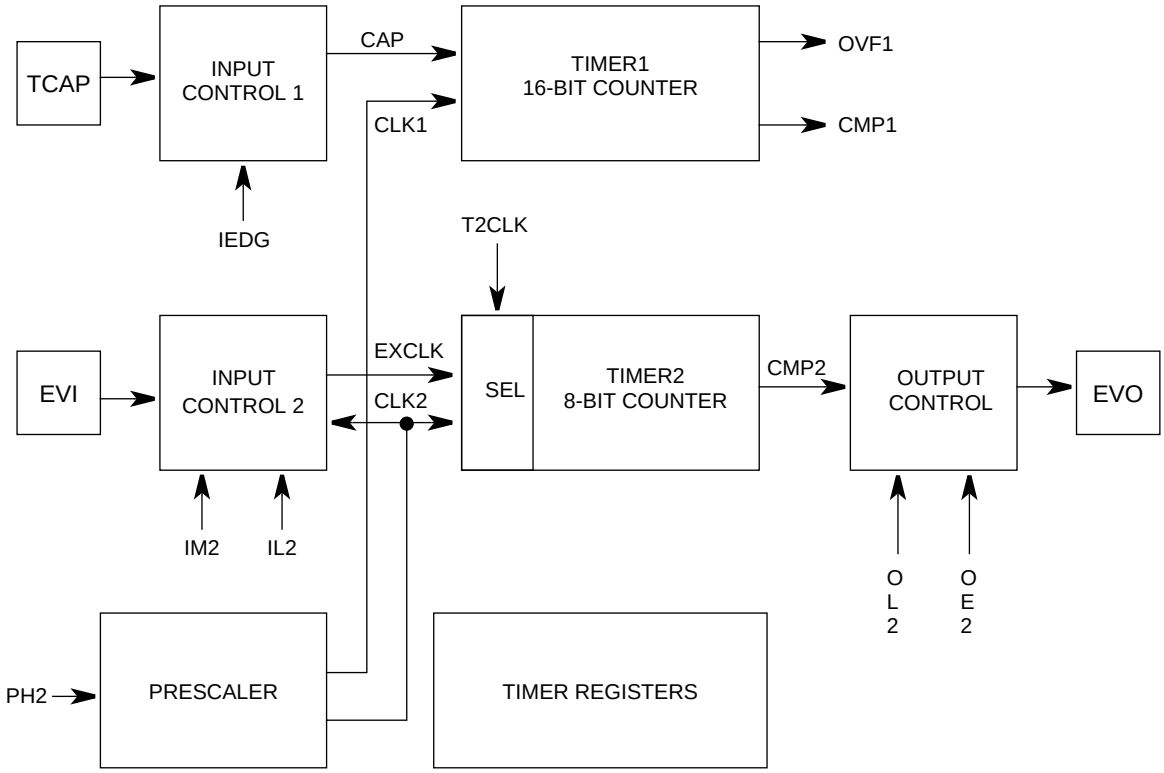

Figure 9-1. Timer System Block Diagram

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9.3 Timer 1

Timer 1 consists of a 16-bit software-programmable counter driven by a fixed divide-by-four prescaler. This timer can be used for many purposes, including input waveform measurements while simultaneously generating an output compare interrupt. Pulse widths can vary from several microseconds to many seconds. See **Figure 9-2**.

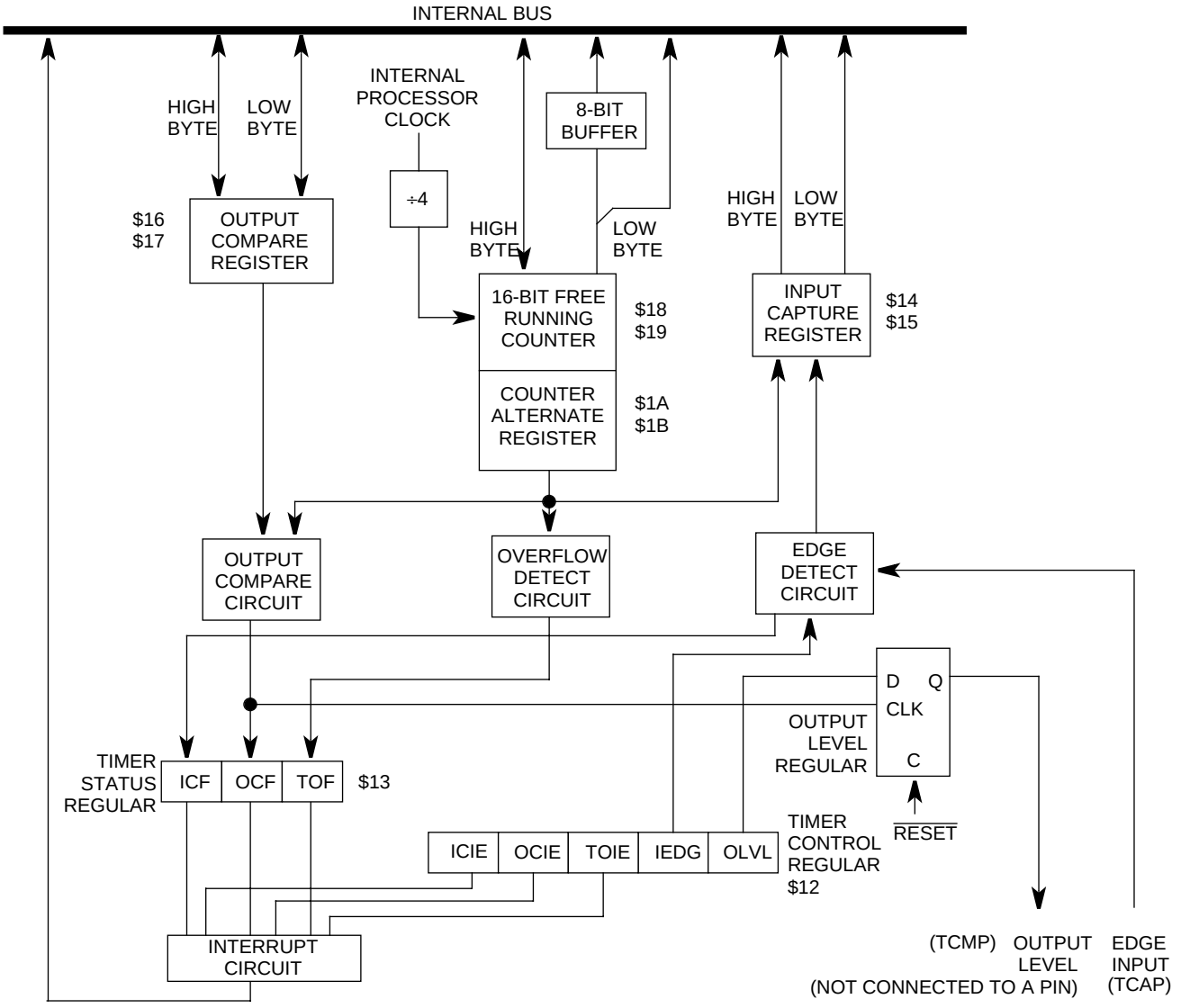

Figure 9-2. Timer 1 Block Diagram

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Because the timer has a 16-bit architecture, each specific functional segment (capability) is represented by two registers. These registers contain the high byte and low byte of that functional segment. Generally, accessing the low byte of a specific timer function allows full control of that function; however, an access of the high byte inhibits that specific timer function until the low byte is accessed also.

NOTE: *The I bit in the condition code register (CCR) should be set while manipulating both the high byte and low byte register of a specific timer function to ensure that an interrupt does not occur.*

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9.3.1 Counter

The key element in the programmable timer is a 16-bit, free-running counter or counter register preceded by a prescaler that divides the internal processor clock by four. The prescaler gives the timer a resolution of 2.0 microseconds if the internal bus clock is 2.0 MHz. The counter is incremented during the low portion of the internal bus clock. Software can read the counter at any time without affecting its value.

The double-byte, free-running counter can be read from either of two locations: $18–$19 (counter register) or $1A–$1B (counter alternate register). A read from only the least significant byte (LSB) of the free-running counter ($19, $1B) receives the count value at the time of the read. If a read of the free-running counter or counter alternate register first addresses the most significant byte (MSB) ($18, $1A), the LSB ($19, $1B) is transferred to a buffer. This buffer value remains fixed after the first MSB read, even if the user reads the MSB several times. This buffer is accessed when reading the free-running counter or counter alternate register LSB ($19 or $1B) and, thus, completes a read sequence of the total counter value. In reading either the free-running counter or counter alternate register, if the MSB is read, the LSB must also be read to complete the sequence.

The counter alternate register differs from the counter register in one respect: A read of the counter register MSB can clear the timer overflow flag (TOF). Therefore, the counter alternate register can be read at any time without the possibility of missing timer overflow interrupts due to clearing of the TOF.

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The free-running counter is configured to $FFFC during reset and is always a read-only register. During a power-on reset, the counter is also preset to $FFFC and begins running after the oscillator startup delay. Because the free-running counter is 16 bits preceded by a fixed divided-by-4 prescaler, the value in the free-running counter repeats every 262,144 internal bus clock cycles. When the counter rolls over from $FFFF to $0000, the TOF bit is set. An interrupt also can be enabled when counter roll over occurs by setting its interrupt enable bit (TOIE).

9.3.2 Output Compare Register

The 16-bit output compare register is made up of two 8-bit registers at locations $16 (MSB) and $17 (LSB). The output compare register is used for several purposes, such as indicating when a period of time has elapsed. All bits are readable and writable and are not altered by the timer hardware or reset. If the compare function is not needed, the two bytes of the output compare register can be used as storage locations.

The output compare register contents are compared with the contents of the free-running counter continually, and if a match is found, the corresponding output compare flag (OCF) bit is set. The output compare register values should be changed after each successful comparison to establish a new elapsed timeout. An interrupt also can accompany a successful output compare, provided the corresponding interrupt enable bit (OCIE) is set.

After a processor write cycle to the output compare register containing the MSB ($16), the output compare function is inhibited until the LSB ($17) also is written. The user must write both bytes (locations) if the MSB is written first. A write made only to the LSB ($17) will not inhibit the compare function. The free-running counter is updated every four internal bus clock cycles. The minimum time required to update the output compare register is a function of the program rather than the internal hardware.

The processor can write to either byte of the output compare register without affecting the other byte.

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9.3.3 Input Capture Register

Two 8-bit registers, which make up the 16-bit input capture register, are read-only and are used to latch the value of the free-running counter after the corresponding input capture edge detector senses a defined transition. The level transition which triggers the counter transfer is defined by the corresponding input edge bit (IEDG). Reset does not affect the contents of the input capture register.

The result obtained by an input capture will be one more than the value of the free-running counter on the rising edge of the internal bus clock preceding the external transition. This delay is required for internal synchronization. Resolution is one count of the free-running counter, which is four internal bus clock cycles.

The free-running counter contents are transferred to the input capture register on each proper signal transition regardless of whether the input capture flag (ICF) is set or clear. The input capture register always contains the free-running counter value that corresponds to the most recent input capture.

After a read of the input capture register ($14) MSB, the counter transfer is inhibited until the LSB ($15) is also read. This characteristic causes the timer used in the input capture software routine and its interaction with the main program to determine the minimum pulse period.

A read of the input capture register LSB ($15) does not inhibit the free-running counter transfer since they occur on opposite edges of the internal bus clock.

NOTE: *Since the TCAP pin is shared with the PC3 I/O pin, changing the state of the PC3 DDR or data register can cause an unwanted TCAP interrupt. This can be handled by clearing the ICIE bit before changing the configuration of PC3 and clearing any pending interrupts before enabling ICIE.*

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9.3.4 Timer Control Register

The TCR is a read/write register containing five control bits. Three bits enable interrupts associated with the timer status register flags ICF, OCF, and TOF.

Address: $0012

	Bit 7	6	5	4	3	2	1	Bit 0
Read: Write:	ICIE	OC1IE	TOIE	0	0	0	IEDG	OLVL
Reset:	0	0	0	0	0	0	U	0

U = Unaffected

Figure 9-3. Timer Control Register (TCR)

ICIE — Input Capture Interrupt Enable
- 0 = Interrupt disabled
- 1 = Interrupt enabled

OC1IE — Output Compare 1 Interrupt Enable
- 0 = Interrupt disabled
- 1 = Interrupt enabled

TOIE — Timer Overflow Interrupt Enable
- 0 = Interrupt disabled
- 1 = Interrupt enabled

IEDG — Input Edge

The value of the input edge determines which level transition on the TCAP pin will trigger free-running counter transfer to the input capture register.

Reset does not affect the IEDG bit.
- 0 = Negative edge
- 1 = Positive edge

Bits 2–4 — Not Used

Always read logic 0

OLVL — Not Used

Always read logic 0

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9.3.5 Timer Status Register

The TSR is a read-only register containing three status flag bits.

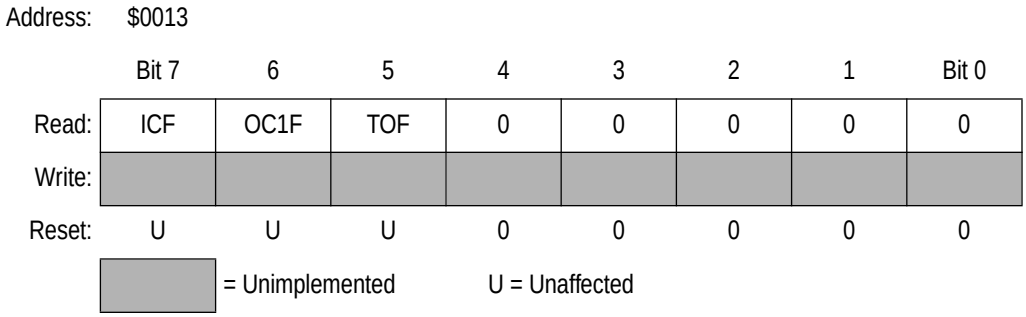

Figure 9-4. Timer Status Register (TSR)

ICF — Input Capture Flag

0 = Flag cleared when TSR and input capture low register ($15) are accessed

1 = Flag set when selected polarity edge is sensed by input capture edge detector

OC1F — Output Compare 1 Flag

0 = Flag cleared when TSR and output compare low register ($17) are accessed

1 = Flag set when output compare register contents match the free-running counter contents

TOF — Timer Overflow Flag

0 = Flag cleared when TSR and counter low register ($19) are accessed

1 = Flag set when free-running counter transition from $FFFF to $0000 occurs

Bits 0–4 — Not Used

Always read logic 0

Accessing the timer status register satisfies the first condition required to clear status bits. The remaining step is to access the register corresponding to the status bit.

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A problem can occur when using the timer overflow function and reading the free-running counter at random times to measure an elapsed time. Without incorporating the proper precautions into software, the timer overflow flag could unintentionally be cleared if:

1. The timer status register is read or written when TOF is set.
2. The LSB of the free-running counter is read but not for the purpose of servicing the flag.

The counter alternate register at address $1A and $1B contains the same value as the free-running counter (at address $18 and $19); therefore, this alternate register can be read at any time without affecting the timer overflow flag in the timer status register.

9.3.6 Timer During Wait Mode

The CPU clock halts during wait mode, but timer 1 remains active. If interrupts are enabled, a timer interrupt will cause the processor to exit wait mode.

9.3.7 Timer During Stop Mode

In stop mode, timer 1 stops counting and holds the last count value if STOP is exited by an interrupt. If $\overline{\text{RESET}}$ is used, the counter is forced to $FFFC. During STOP, if at least one valid input capture edge occurs at the TCAP pin, the input capture detect circuit is armed. This does not set any timer flags or wake up the MCU. When the MCU does wake up, there is an active input capture flag and data from the first valid edge that occurred during stop mode. If $\overline{\text{RESET}}$ is used to exit stop mode, then no input capture flag or data remains, even if a valid input capture edge occurred.

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9.4 Timer 2

Timer 2 is an 8-bit event counter which has one compare register, one event input pin (EVI), and one event output pin (EVO). The event counter is clocked by the external clock (EXCLK) or prescaled system clock (CLK2), selected by the T2CLK bit in the TCR2 register. The EXCLK may be EVI direct or EVI gated by CLK2, which is selected by the IM2 bit at the EVI block (see **9.4.6 Timer Input 2 (EVI)**).

Timer 2 may be used as a modulus clock divider with EVO pin, free-running counter (when compare register is $00), or periodic interrupt timer.

The timer counter 2 (TCNT2) is an 8-bit up counter with preset input. The counter is preset to $01 by a CMP2 signal from the comparator or by a CPU write to it that is done while the system clock (PH2) is low.

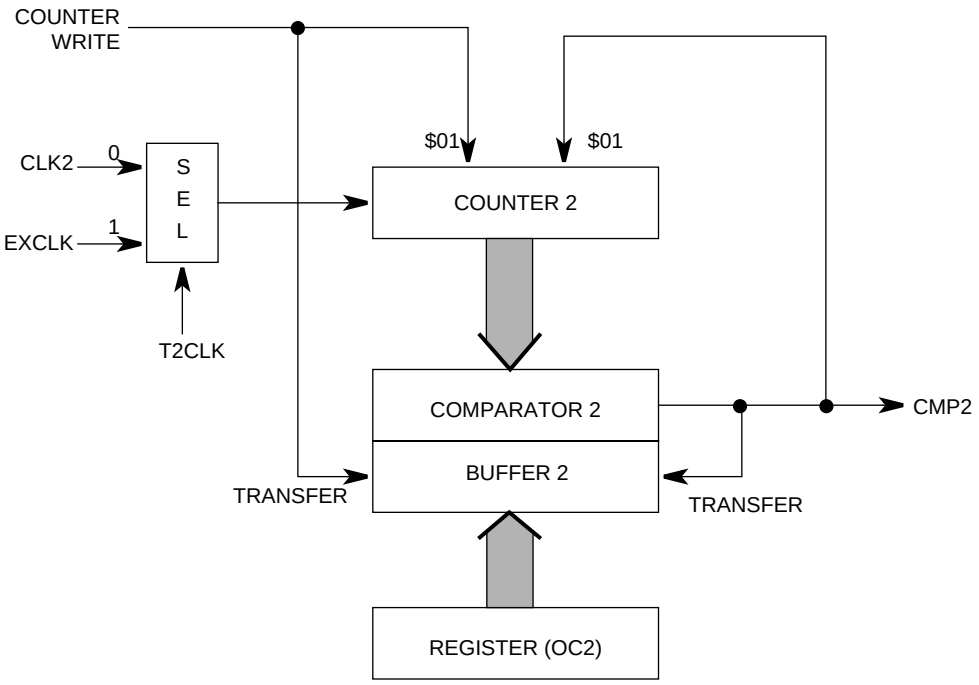

Figure 9-5. Timer 2 Block Diagram

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The CLK2 from the prescaler or the EXTCLK from the EVI block is selected as timer clock by the T2CLK bit in the TCR2 register. The CLK2 and the EXCLK are synchronized to the falling edge of system clock in the prescaler and the EVI blocks. The minimum pulse width of CLK2 is the same as the system clock, and the minimum pulse width of EXCLK (event mode) is one PH2 cycle. When the EXCLK (event mode) is selected, 50% duty is not guaranteed.

The counter is incremented by the falling edge of the timer clock and the period between two falling edges is defined as one timer cycle in the following description.

The compare register (OC2) is provided for comparison with the timer counter 2 (TCNT2). The OC2 data is transferred to the buffer register when the counter is preset by a CPU write or by a compare output (CMP2). This buffer register is compared with the timer counter 2 (TCNT2).

The comparison between the counter and the OC2 buffer register is done when the system clock is high in each bus cycle. If the counter matches with the OC2 buffer register, the comparator latches this result during the current timer cycle. When the next timer cycle begins, the comparator outputs CMP2 signal (if the compare match is detected during previous timer cycle). This CMP2 is used in the counter preset data transfer to the buffer register, setting OC2F in the TSR2 and the EVO block. The counter preset overrides the counter increment.

The OC2F bit may generate interrupt requests if the OC2IE bit in the TCR2 is set.

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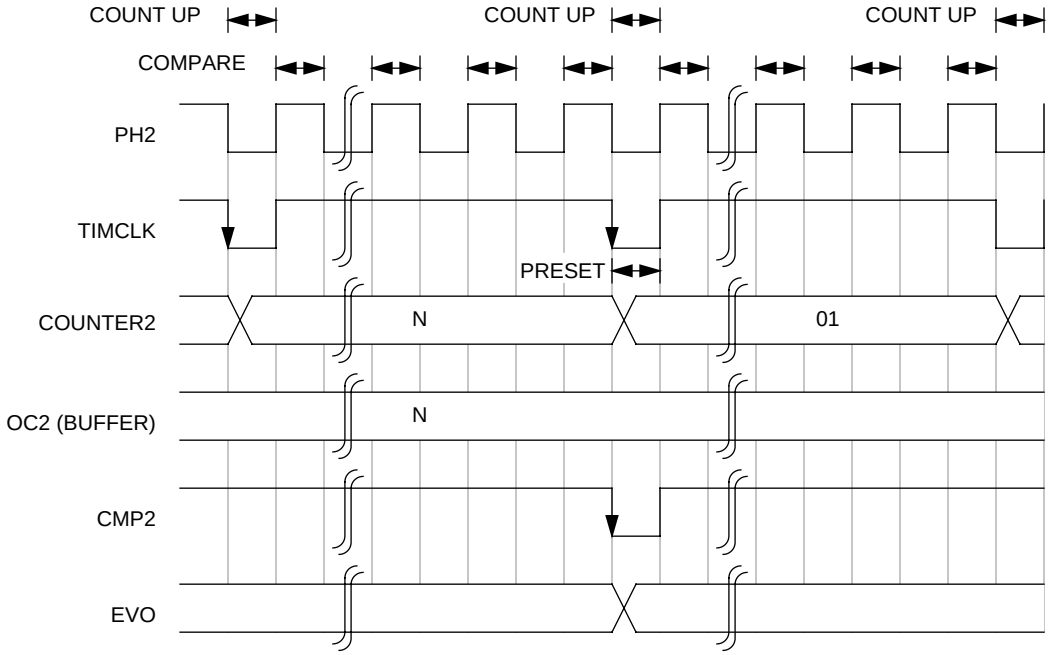
OC2 = 2, 3, 4 . . . FF, 0



OC2 = 1

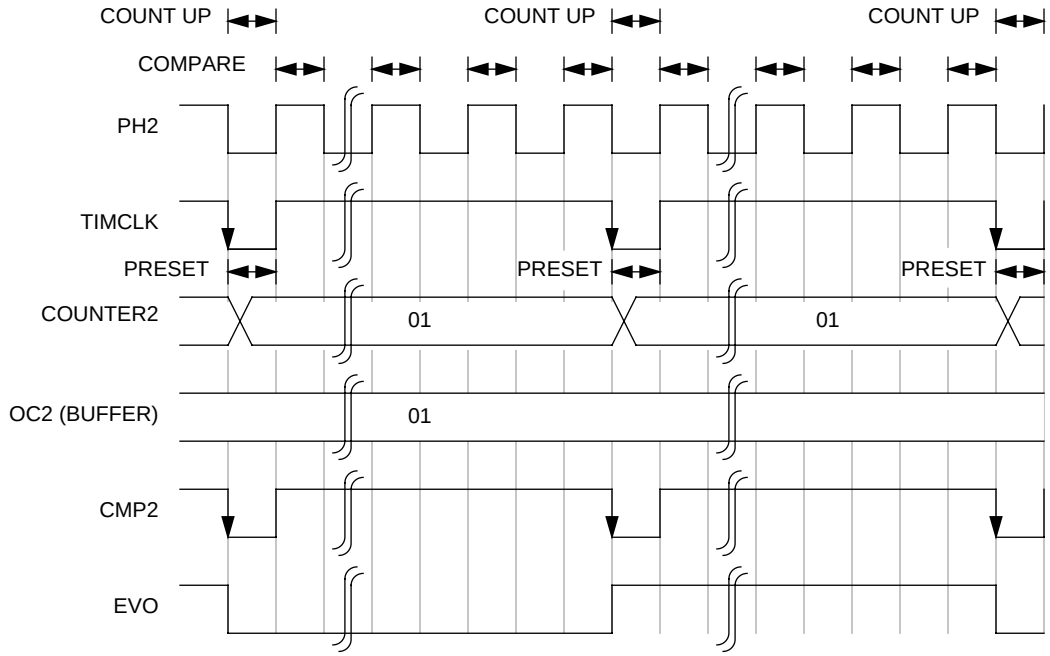


Figure 9-6. Timer 2 Timing Diagram for f(PH2) > f(TIMCLK)

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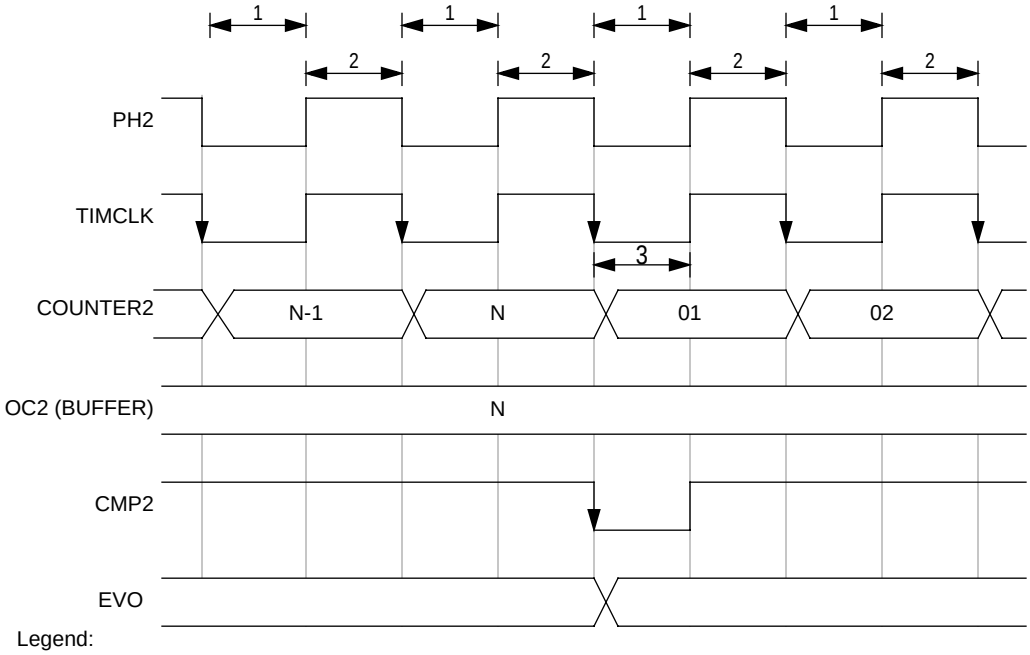
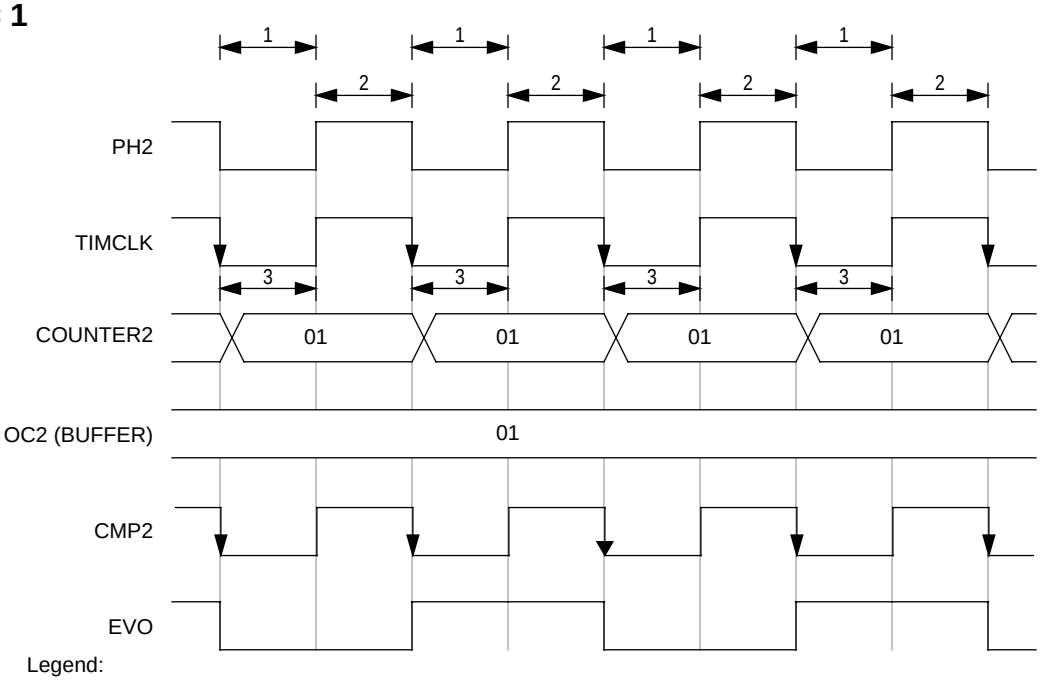
OC2 = 2, 3, 4 . . . FF, 0



Legend:
1. COUNT UP
2. COMPARE
3. PRESET that overrides COUNT UP

OC2 = 1



Legend:
1. COUNT UP
2. COMPARE
3. PRESET that overrides COUNT UP

Figure 9-7. Timer 2 Timing Diagram for f(PH2) = f(TIMCLK)

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9.4.1 Timer Control Register 2

Address: $001C

	Bit 7	6	5	4	3	2	1	Bit 0
Read: Write:	TI2IE	OC2IE	0	T2CLK	IM2	IL2	OE2	OL2
Reset:	0	0	0	0	0	0	0	0

Figure 9-8. Timer Control Register 2 (TCR2)

TI2IE — Timer Input 2 Interrupt Enable

The TI2IE bit enables timer input 2 (EVI) interrupt when TI2F is set. This bit is cleared on reset.

0 = Timer input 2 interrupt disabled
1 = Timer input 2 interrupt enabled

OC2IE — Compare 2 Interrupt Enable

The OC2IE bit enables compare 2 (CMP2) interrupt when compare match is detected (OC2F is set). This bit is cleared on reset.

0 = Timer input 2 interrupt disabled
1 = Timer input 2 interrupt enabled

Bit 5 — Reserved

This bit is not used and is always read as logic 0.

T2CLK — Timer 2 Clock Select

The T2CLK bit selects the clock source for the timer counter 2. This bit is cleared on reset.

0 = CLK2 from prescaler selected
1 = EXCLK from EVI input block selected

IM2 — Timer Input 2 Mode Select

The IM2 bit selects whether EVI input is gated or not gated by CLK2. This bit is cleared on reset.

0 = EVI not gated by CLK2 (event mode)
1 = EVI gated by CLK2 (gate mode)

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IL2 — Timer Input 2 Active Edge (Level) Select

The IL2 bit selects the active edge of EVI to increment the counter for event mode (IM2 = 0) or gate enable level of EVI for gate mode (IM2 = 1). This bit is cleared on reset.

0 = Falling edge selected (event mode)
Low level enables counting (gate mode)

1 = Rising edge selected (event mode)
High level enables counting (gate mode)

Table 9-1. EVI Modes Selection

IM2	IL2	Action on Clock
0	0	Falling edge of EVI increments counter
0	1	Rising edge of EVI increments counter
1	0	Low level on EVI enables counting
1	1	High level on EVI enables counting

OE2 — Timer Output 2 (EVO) Output Enable

The OE2 bit enables EVO output on the PC5 pin. When this bit is changed, control of the pin is delayed (synchronized) until the next active edge of EVO is selected by the OL2 bit. This bit is cleared on reset.

0 = EVO output disabled
1 = EVO output enabled

OL2 — Timer Output 2 Edge Select for Synchronization

The OL2 bit selects which edge of EVO clock should be synchronized by the OE2 bit control. The OL2 bit also decides the initial value of the CMP2 divider, when counter 2 is written to by the CPU. This bit is cleared on reset.

0 = The falling edge of EVO switches EVO output and PC5 if the OE2 bit has been changed.

1 = The rising edge of EVO switches EVO output and PC5 if the OE2 bit has been changed.

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9.4.2 Timer Status Register 2

Address: $001D

	Bit 7	6	5	4	3	2	1	Bit 0
Read:	TI2F	OC2F	0	0	0	0	0	0
Write:					RTI2F	ROC2F		
Reset:	0	0	0	0	0	0	0	0

= Unimplemented

Figure 9-9. Timer Status Register 2 (TSR2)

TI2F — Timer Input 2 (EVI) Interrupt Flag

In event mode, the event edge sets TI2F. In gated time accumulation mode, the trailing edge of the gate signal at the EVI input pin sets TI2F. When the TI2IE bit and this bit are set, an interrupt is generated. This bit is a read-only bit and writes have no effect. The TI2F is cleared by writing a logic 1 to the RTI2F bit and on reset.

OC2F — Compare 2 Interrupt Flag

The OC2F bit is set when compare match is detected between counter 2 and OC2 register. When OC2IE bit and this bit are set, an interrupt is generated. This bit is a read-only bit and writes have no effect. The OC2F is cleared by writing a logic 1 to ROC2F bit and on reset.

Bits 5 and 4 — Reserved

These bits are not used and always read as logic 0.

RTI2F — Reset Timer Input 2 Flag

The RTI2F bit is a write-only bit and always reads as logic 0. Writing logic 1 to this bit clears the TI2F bit and writing a logic 0 to this bit has no effect.

ROC2F — Reset Output Compare 2 Flag

The ROC2F bit is a write-only bit and always reads as logic 0. Writing logic 1 to this bit clears the OC2F bit and writing a logic 0 to this bit has no effect.

Bits 1 and 0 — Reserved

These bits are not used and always read as logic 0.

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9.4.3 Output Compare Register 2

Address: $001E

	Bit 7	6	5	4	3	2	1	Bit 0
Read: Write:	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Reset:	0	0	0	0	0	0	0	0

Figure 9-10. Output Compare Register 2 (OC2)

The OC2 register data is transferred to the buffer register when the CPU writes to TCNT2, when the CMP2 presets the TCNT2, or when system resets.

When the OC2 buffer register matches the TCNT2 register, the OC2F bit in the TSR2 register is set and TCNT2 is preset to $01.

9.4.4 Timer Counter Register 2

Address: $001F

	Bit 7	6	5	4	3	2	1	Bit 0
Read: Write:	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Reset:	0	0	0	0	0	0	0	1

Figure 9-11. Timer Counter Register 2 (TCNT2)

TCNT2 is incremented by the falling edge of the timer clock, which is synchronized and has the same timing as the falling edge of PH2.

The TCNT2 register is compared with the OC2 buffer register and initialized to $01 if it matches. It is also initialized to $01 on reset and any CPU write to this register.

The CPU read of this counter should be done while PH2 is high. Data may be latched by the local or main data bus while PH2 is low.

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9.4.5 Timebase Control Register 1

Address: $0010

	Bit 7	6	5	4	3	2	1	Bit 0
Read: Write:	TBCLK	0	LCLK	0	0	0	T2R1	T2R0
Reset:	0	0	0	0	0	0	0	0

Figure 9-12. Timebase Control Register 1 (TBCR1)

T2R1/T2R0 — Prescale Rate Select Bits for Timer 2

The T2R1 and T2R0 bits select prescale rate of CLK2 for timer 2 and timer input 2. These bits are cleared on reset.

Table 9-2. Time Base Prescale Rate Selection

T2R1	T2R0	System Clock Divided by
0	0	1
0	1	4
1	0	32
1	1	256

9.4.6 Timer Input 2 (EVI)

The event input (EVI) is used as an external clock input for timer 2.

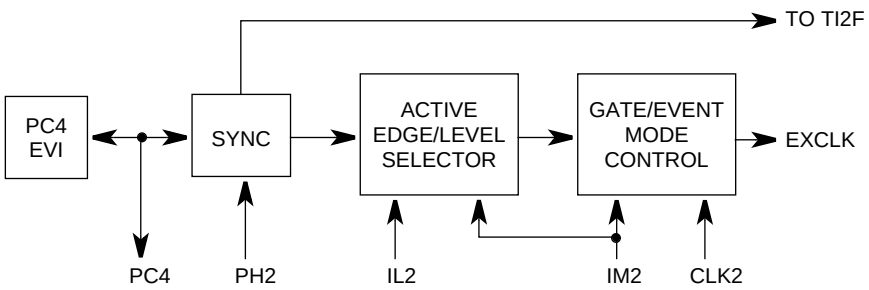

Figure 9-13. EVI Block Diagram

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Since the external clock may be asynchronous to the internal clock, this input has a synchronizer which samples external clock by the internal system clock. (The input transition synchronizes to the falling edge of PH2. Therefore, to be measured, the minimum pulse width for EVI must be larger than one system clock.)

The IM2 and IL2 bits in the TCR2 determine how this synchronized external clock is used. The IM2 bit decides between event mode and gate mode, and the IL2 bit decides which level or edge is activated.

In event mode (IM2 = 0), the external clock drives the timer 2 counter directly and the active edge at the EVI pin is selected by the IL2 bit. When an active edge is detected, the TI2F bit in the TCR2 is set.

Table 9-3. EVI Modes Selection

IM2	IL2	Action on Clock
0	0	Falling edge of EVI increments counter
0	1	Rising edge of EVI increments counter
1	0	Low level on EVI enables counting
1	1	High level on EVI enables counting

NOTE: *Since the EVI pin is shared with the PC4 I/O pin, DDRC4 should always be cleared whenever EVI is used. EVI should not be used when DDRC4 is high.*

In gate mode (IM2 = 1), the EVI input is gated by CLK2 from the prescaler and gate output drives the timer 2 counter. The IL2 bit decides active level of the external input. When the transition from active level to inactive level is detected, the TI2F bit is set.

Changing the IM2 bit may cause an illegal count up of TCNT2, thus presetting TCNT2 after initializing IM2 is required.

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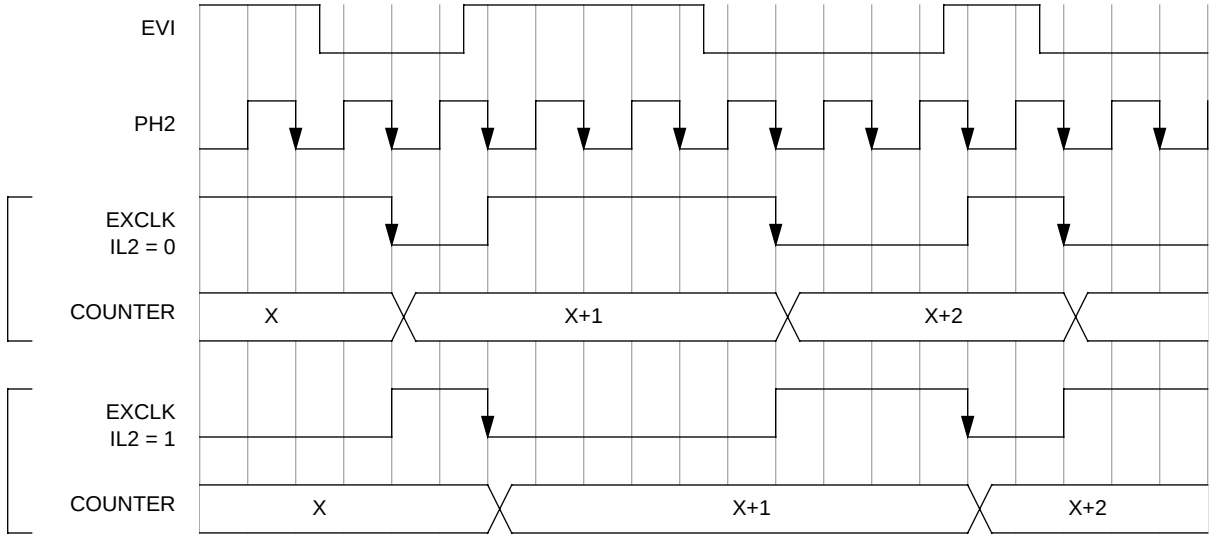
IM2 = 0 Event Mode



IM2 = 1 Gate Mode

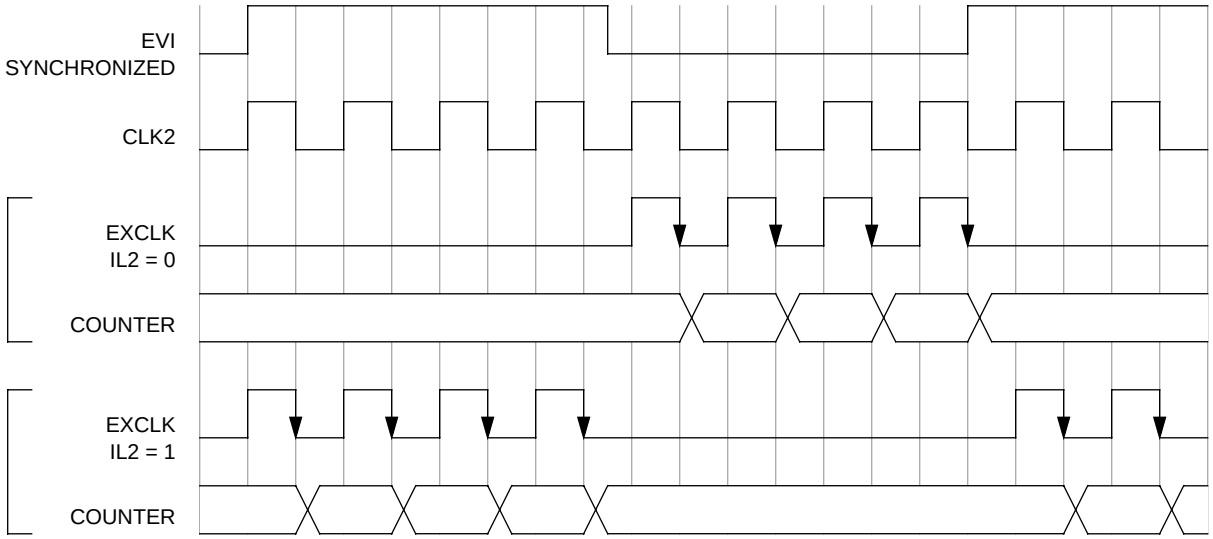


Figure 9-14. EVI Timing Diagram

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9.4.7 Event Output (EVO)

The EVO pin is the clock output pin of timer 2. The compare output from the timer 2 (CMP2) is divided in this block for 50% duty output signal. This 1/2 divider is initialized to the level of the OL2 bit when the timer counter 2 is written to by the CPU (initialized). When the OE2 bit in the timer control register 2 (TCR2) is set, the EVO output is activated, and, when OE2 is cleared, EVO is deactivated. These controls must be done synchronously to the EVO output signal to avoid an incomplete pulse on the pin. The OL2 bit in the TCR2 decides which edge of EVO should be synchronized.

When the DDRC5 bit is set or the synchronized output enable is high (clock on), the output buffer at the EVO/PC5 pin is enabled. If the DDRC5 bit is set to 1, the pin state during the idling condition (clock off) depends on the PC5 output data latch. If the DDRC5 bit is cleared, the pin becomes high impedance during clock off.

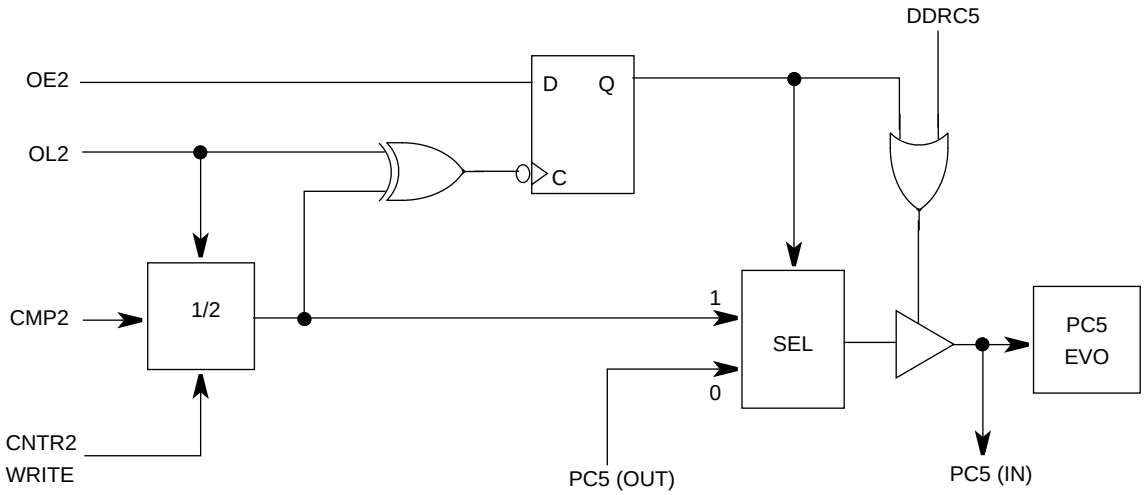

Figure 9-15. EVO Block Diagram

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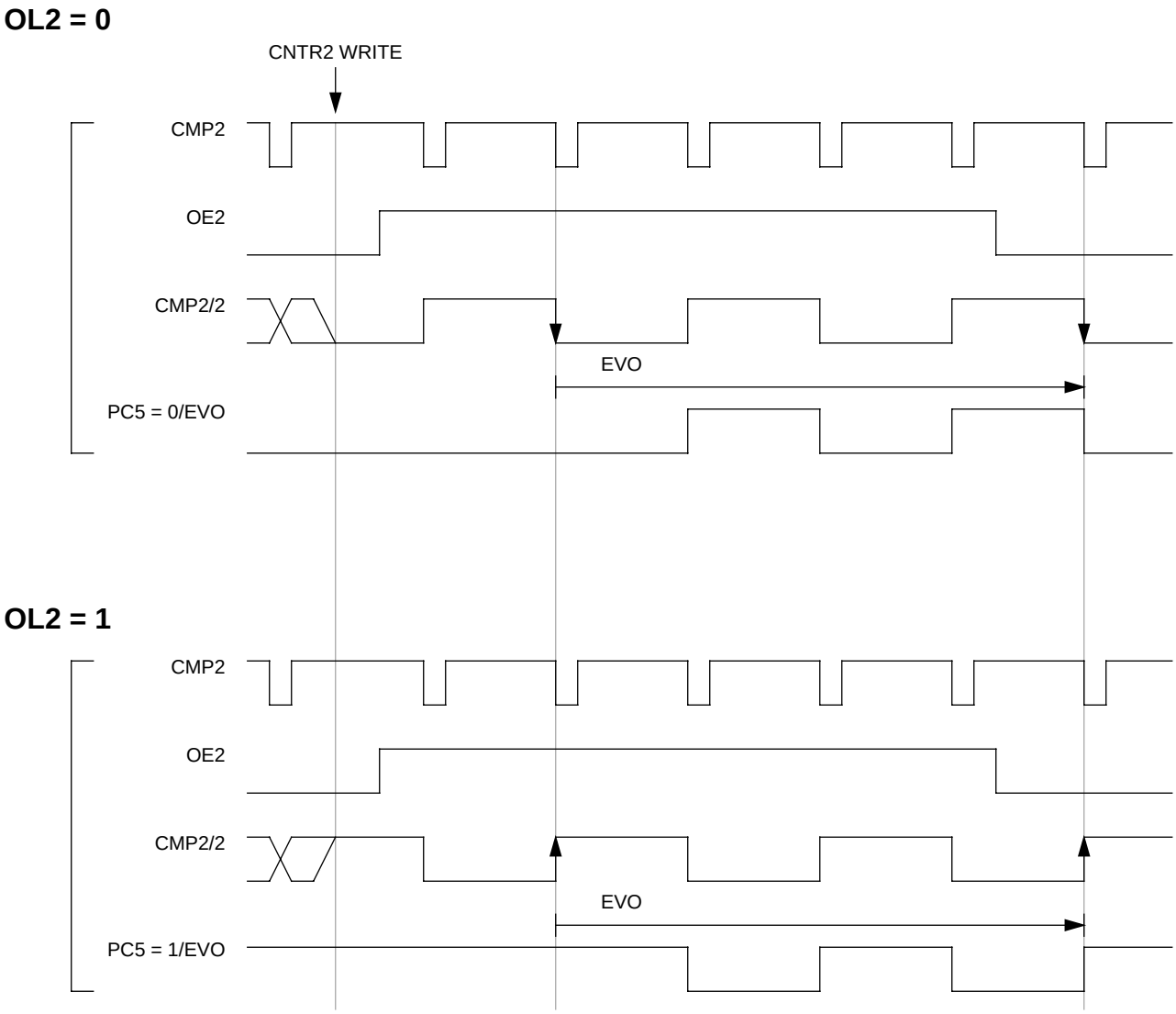

Figure 9-16. EVO Timing Diagram

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9.5 Prescaler

The 8-bit prescaler in the timer system divides system clock (PH2) and provides divided clock to each timer and event input.

CLK1 for timer 1 is a fixed frequency clock (PH2/PH4).

CLK2 for timer 2 is selected by T2R1 and T2R0 bits in the TBCR1, and this clock is also used as the event input for gate mode. The CLK2 transitions must be synchronous to the falling edge of PH2.

Table 9-4. Timebase Prescale Rate Selection

T2R1	T2R0	System Clock Divided by
0	0	1
0	1	4
1	0	32
1	1	256

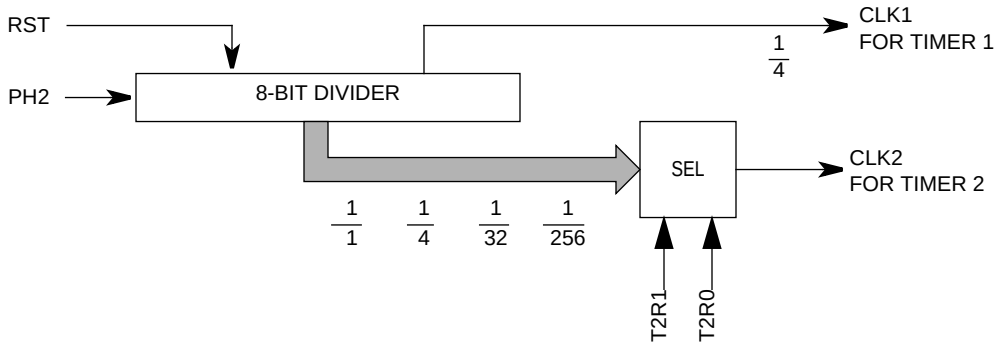

Figure 9-17. Prescaler Block Diagram

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Timer System

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Section 10. LCD Driver

10.1 Contents

10.2 Introduction

The LCD driver may be configured with four backplanes (BP) and 39 frontplanes (FP) maximum. The V_{DD} voltage is the highest level of the output waveform and the lower three levels are applied from VLCD1, VLCD2, and VLCD3 inputs.

On reset, LCD enable bit (LCDE) in the LCD control register (LCDCR) is cleared (LCD drivers at a disabled state) and all BP pins and FP pins output V_{DD} levels.

The LCD clock is generated by the timebase module, and the LCLK bit in the TBCR1 selects the clock frequency.

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10.3 LCD Waveform Examples

Figure 10-1, **Figure 10-2**, **Figure 10-3**, and **Figure 10-4** illustrate the LCD timing examples.

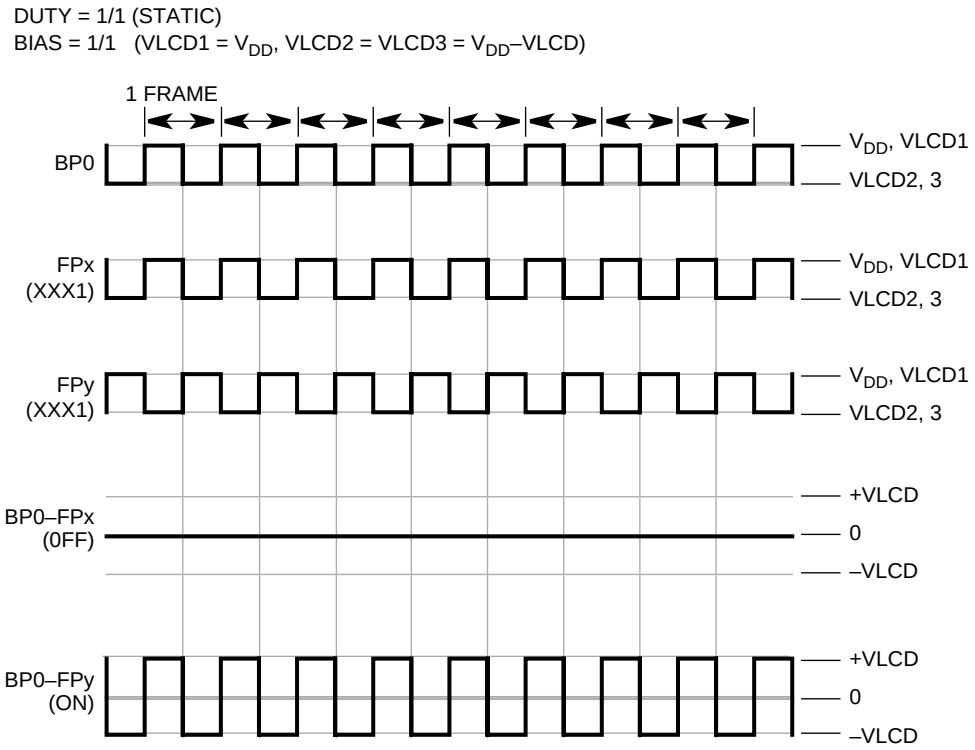

Figure 10-1. LCD 1/1 Duty and 1/1 Bias Timing Diagram

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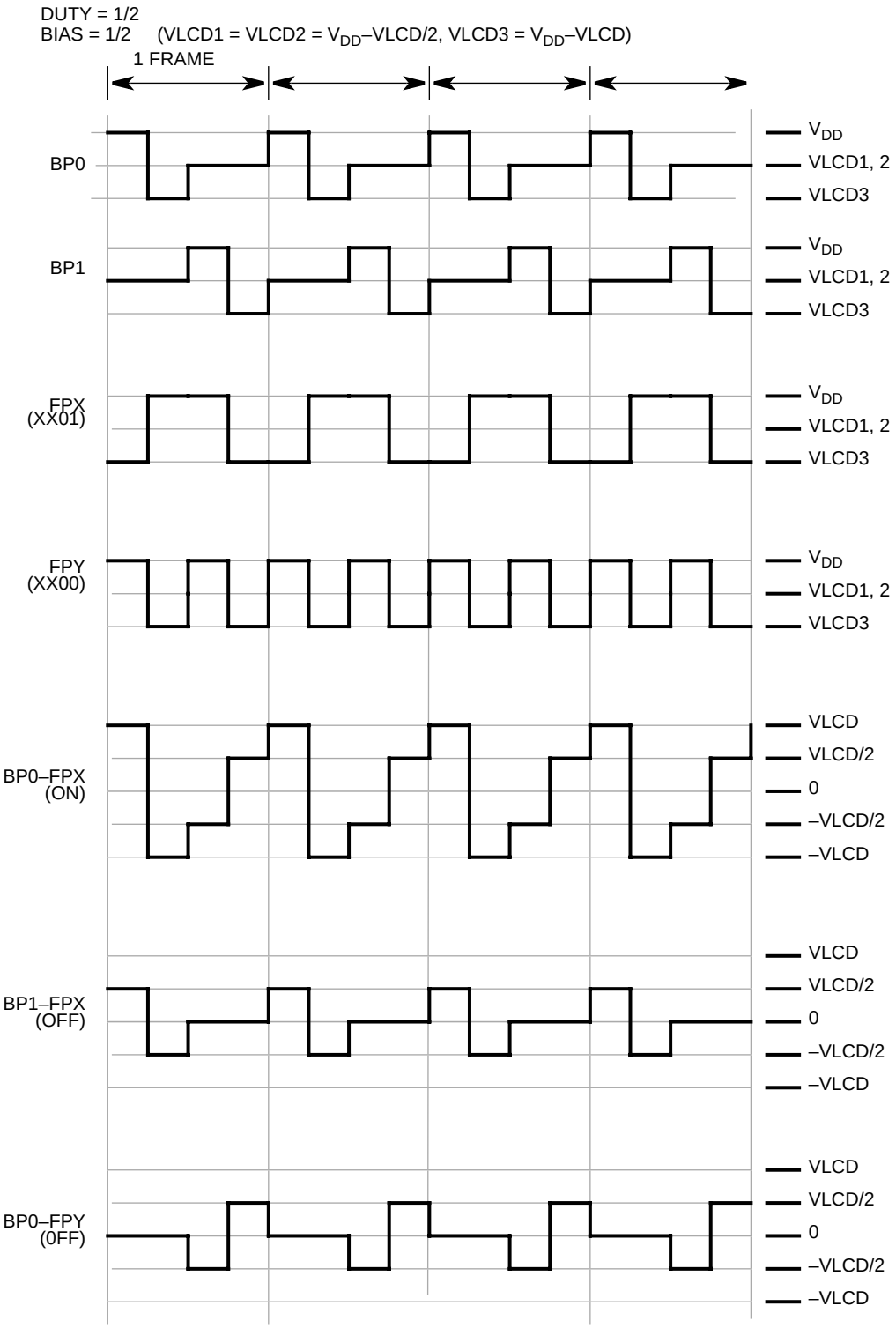

Figure 10-2. LCD 1/2 Duty and 1/2 Bias Timing Diagram

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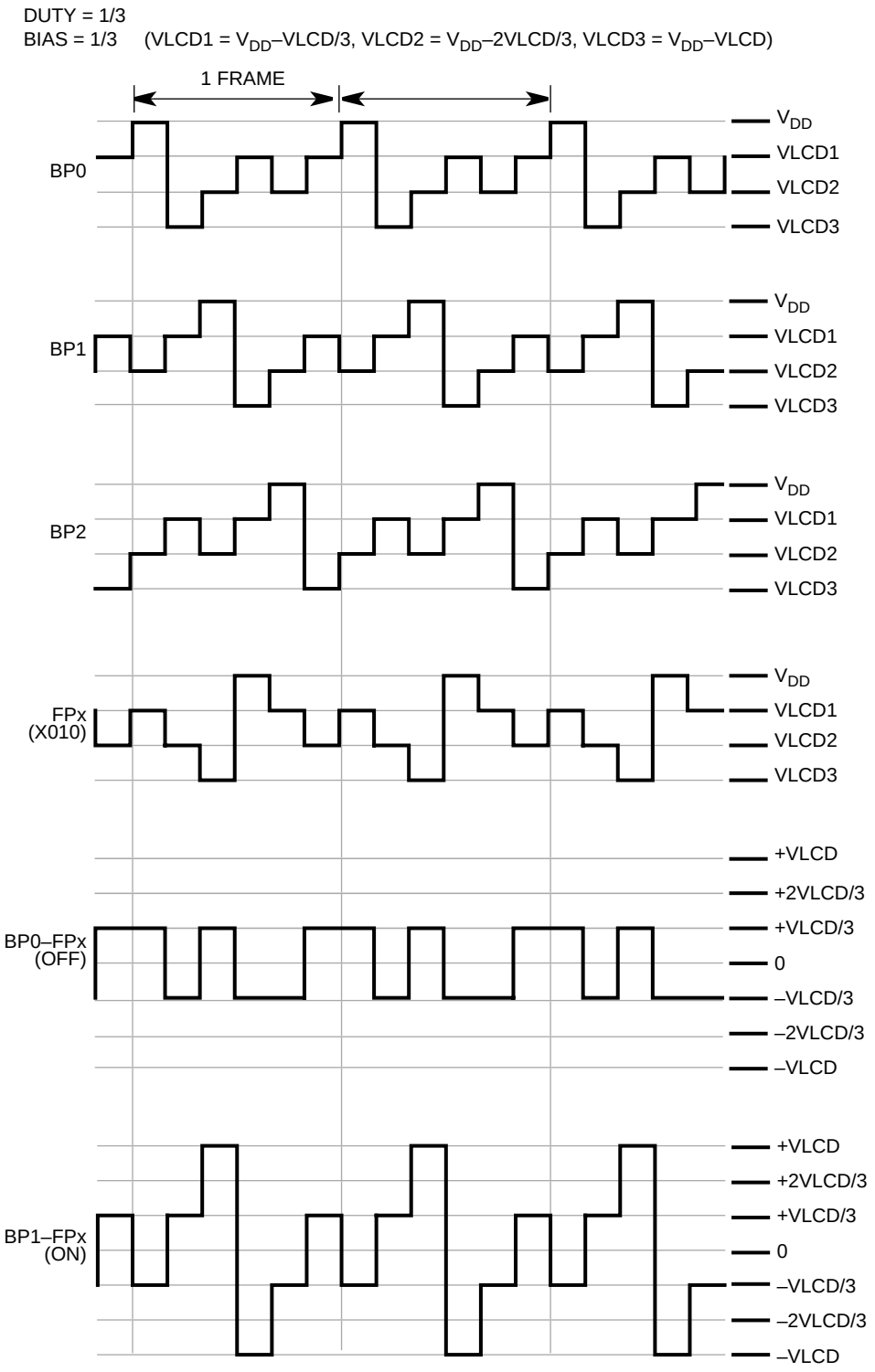

Figure 10-3. LCD 1/3 Duty and 1/3 Bias Timing Diagram

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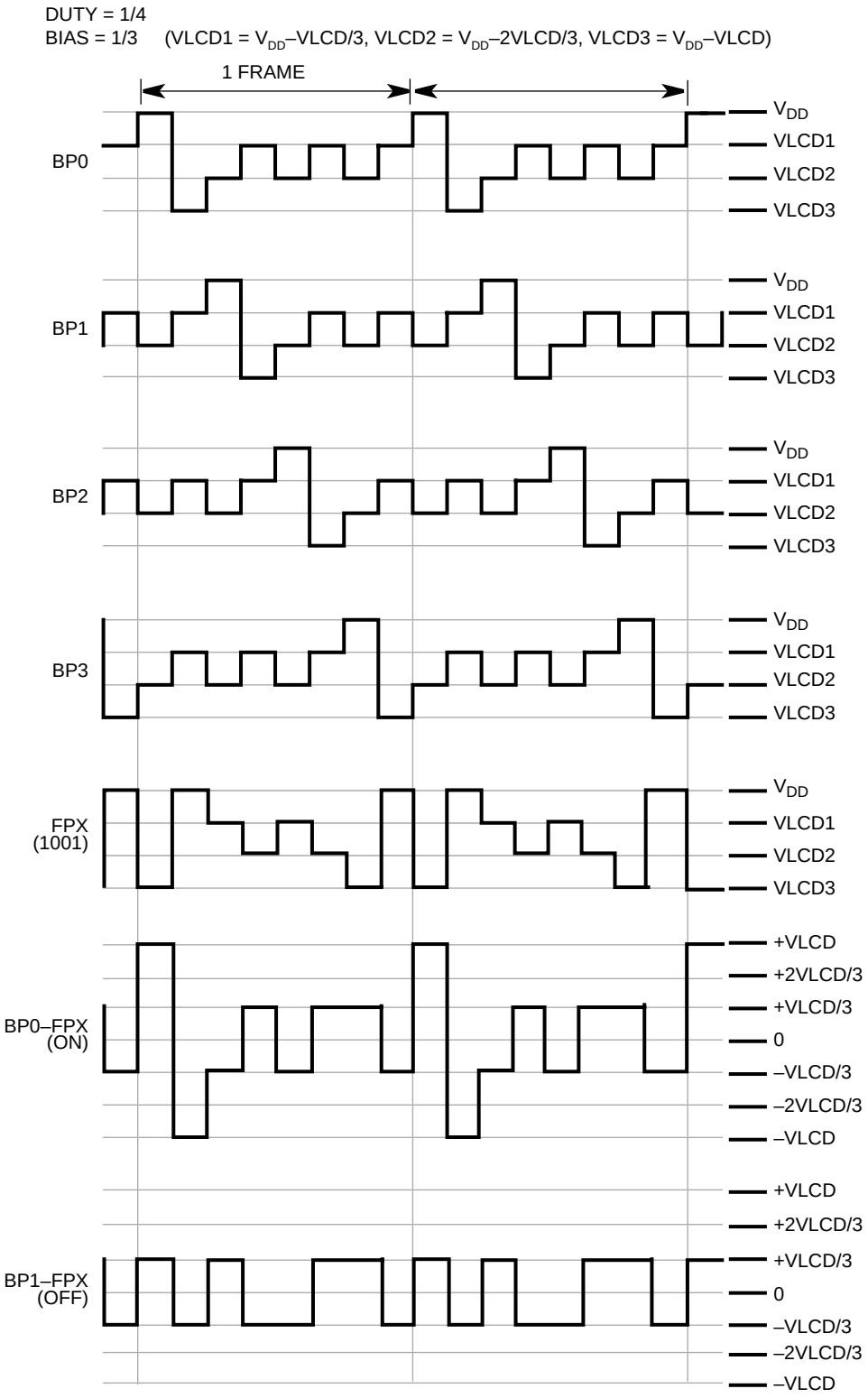

Figure 10-4. LCD 1/4 Duty and 1/3 Bias Timing Diagram

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10.4 Backplane Driver and Port Selection

The number of backplane (port D) pins depends on the LCD duty. It is automatically selected by DUTY1 and DUTY0 bits in the LCD control register (LCDCR). On reset, these bits are cleared and 1/4 duty is selected. (See **Table 10-1**.)

Table 10-1. Backplane and Port Selection

Duty	LCD Control		Pin Selection			
	DUTY1	DUTY0	BP3/PD3	BP2/PD2	BP1/PD1	BP0
1 / 1	0	1	PD3	PD2	PD1	BP0
1 / 2	1	0	PD3	PD2	BP1	BP0
1 / 3	1	1	PD3	BP2	BP1	BP0
1 / 4	0	0	BP3	BP2	BP1	BP0

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10.5 Frontplane Driver and Port Selection

The number of frontplane (FP) pins depends on the number of port D and port E bits. If port bits are selected as a parallel output port, the number of the FP pins is decreased to 27 as a minimum. The selections between frontplane and port (nibble wide) are done by the PEH, PEL, and PDH bits in the LCDCR (see **Table 10-2**). On reset, port D and port E bits are disconnected and FP27–FP38 pins output V_{DD} levels.

Table 10-2. Frontplane and Port Selection

FP / Port Control			Port Selection		
PEH	**PEL**	**PDH**	**FP27:FP30/ PE7:PE4**	**FP31:FP34/ PE3:PE0**	**FP35:FP38/ PD7:PD4**
		0			FP35:FP38
		1			PD7:PD4
	0			FP31:FP34	
	1			PE3:PE0	
0			FP27:FP30		
1			PE7:PE4		

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10.6 LCD Control Register

Address: $0020

	Bit 7	6	5	4	3	2	1	Bit 0
Read: Write:	LCDE	DUTY1	DUTY0	0	PEH	PEL	PDH	0
Reset:	0	0	0	0	0	0	0	0

Figure 10-5. LCD Control Register (LCDCR)

LCDE — LCD Output Enable

The LCDE bit enables all BP and FP outputs. (This bit does not affect PEH, PEL, or PDH bits.) This bit is cleared on reset.

0 = All dedicated FP pins output highest (V_{DD}) level; BP and FP pins are shared with an output port data.

1 = All BP and FP pins output LCD waveforms.

DUTY1 and DUTY0 — LCD Duty Select

The DUTY1 and DUTY0 bits select the duty of the LCD driver. The number of BP pins is related to this duty selection. The unused BP pin is used as a port D pin. Default duty is 1/4 duty. These bits are cleared on reset. See **Table 10-1**.

Bit 4 — Reserved

This bit is not used and always reads as logic 0.

PEH — Select Port E (H)

The PEH bit enables the upper four bits of port E instead of LCD drivers. This bit is cleared on reset. See **10.5 Frontplane Driver and Port Selection**.

0 = FP27–FP30 selected

1 = PE7–PE4 selected

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PEL — Select Port E (L)

The PEL bit enables the lower four bits of port E instead of LCD drivers. This bit is cleared on reset. See **10.5 Frontplane Driver and Port Selection**.

0 = FP31–FP34 selected
1 = PE3–PE0 selected

PDH — Select Port D (H)

The PDH bit enables the upper four bits of port D instead of LCD drivers. This bit is cleared on reset. See **10.5 Frontplane Driver and Port Selection**.

0 = FP35–FP38 selected
1 = PD7–PD4 selected

Bit 0 — Reserved

This bit is not used and is always read as logic 0.

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10.7 LCD Data Register

Address: $0021–$0034

	FP (2x–1)				FP (2x–2)			
	Bit 7	6	5	4	3	2	1	Bit 0
Read: Write:	BP3	BP2	BP1	BP0	BP3	BP2	BP1	BP0
Reset:	Unaffected by Reset							

Figure 10-6. LDC Data Registers

LCDRx — LCD Data Registers

Data in the LCDR*x* (LCDR1–LCDR20) controls the waveform of the two frontplane drivers. Bits 0–3 and bits 4–7 of this register decide the waveforms at the BP0–BP3 timings. If the LCD duty is not 1/4, the register bit for the unused backplane has no meaning. The upper four bits of LCDR20 are not implemented and unknown data may be read. (See **Table 10-3**.)

0 = Output deselect waveform at the corresponding backplane timing

1 = Output select waveform at the corresponding backplane timing

Table 10-3. Frontplane Data Register Bit Usage

Duty	Frontplane Data Register Bit Usage							
	Bit 7	**Bit 6**	**Bit 5**	**Bit 4**	**Bit 3**	**Bit 2**	**Bit 1**	**Bit 0**
1 / 1	—	—	—	BP0	—	—	—	BP0
1 / 2	—	—	BP1	BP0	—	—	BP1	BP0
1 / 3	—	BP2	BP1	BP0	—	BP2	BP1	BP0
1 / 4	BP3	BP2	BP1	BP0	BP3	BP2	BP1	BP0

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Section 11. Instruction Set

11.1 Contents

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11.2 Introduction

The MCU instruction set has 62 instructions and uses eight addressing modes. The instructions include all those of the M146805 CMOS Family plus one more: the unsigned multiply (MUL) instruction. The MUL instruction allows unsigned multiplication of the contents of the accumulator (A) and the index register (X). The high-order product is stored in the index register, and the low-order product is stored in the accumulator.

11.3 Addressing Modes

The CPU uses eight addressing modes for flexibility in accessing data. The addressing modes provide eight different ways for the CPU to find the data required to execute an instruction. The eight addressing modes are:

- Inherent
- Immediate
- Direct
- Extended
- Indexed, no offset
- Indexed, 8-bit offset
- Indexed, 16-bit offset
- Relative

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11.3.1 Inherent

Inherent instructions are those that have no operand, such as return from interrupt (RTI) and stop (STOP). Some of the inherent instructions act on data in the CPU registers, such as set carry flag (SEC) and increment accumulator (INCA). Inherent instructions require no operand address and are one byte long.

11.3.2 Immediate

Immediate instructions are those that contain a value to be used in an operation with the value in the accumulator or index register. Immediate instructions require no operand address and are two bytes long. The opcode is the first byte, and the immediate data value is the second byte.

11.3.3 Direct

Direct instructions can access any of the first 256 memory locations with two bytes. The first byte is the opcode, and the second is the low byte of the operand address. In direct addressing, the CPU automatically uses $00 as the high byte of the operand address.

11.3.4 Extended

Extended instructions use three bytes and can access any address in memory. The first byte is the opcode; the second and third bytes are the high and low bytes of the operand address.

When using the Motorola assembler, the programmer does not need to specify whether an instruction is direct or extended. The assembler automatically selects the shortest form of the instruction.

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11.3.5 Indexed, No Offset

Indexed instructions with no offset are 1-byte instructions that can access data with variable addresses within the first 256 memory locations. The index register contains the low byte of the effective address of the operand. The CPU automatically uses $00 as the high byte, so these instructions can address locations $0000–$00FF.

Indexed, no offset instructions are often used to move a pointer through a table or to hold the address of a frequently used RAM or I/O location.

11.3.6 Indexed, 8-Bit Offset

Indexed, 8-bit offset instructions are 2-byte instructions that can access data with variable addresses within the first 511 memory locations. The CPU adds the unsigned byte in the index register to the unsigned byte following the opcode. The sum is the effective address of the operand. These instructions can access locations $0000–$01FE.

Indexed 8-bit offset instructions are useful for selecting the kth element in an n-element table. The table can begin anywhere within the first 256 memory locations and could extend as far as location 510 ($01FE). The k value is typically in the index register, and the address of the beginning of the table is in the byte following the opcode.

11.3.7 Indexed,16-Bit Offset

Indexed, 16-bit offset instructions are 3-byte instructions that can access data with variable addresses at any location in memory. The CPU adds the unsigned byte in the index register to the two unsigned bytes following the opcode. The sum is the effective address of the operand. The first byte after the opcode is the high byte of the 16-bit offset; the second byte is the low byte of the offset.

Indexed, 16-bit offset instructions are useful for selecting the kth element in an n-element table anywhere in memory.

As with direct and extended addressing, the Motorola assembler determines the shortest form of indexed addressing.

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11.3.8 Relative

Relative addressing is only for branch instructions. If the branch condition is true, the CPU finds the effective branch destination by adding the signed byte following the opcode to the contents of the program counter. If the branch condition is not true, the CPU goes to the next instruction. The offset is a signed, two's complement byte that gives a branching range of –128 to +127 bytes from the address of the next location after the branch instruction.

When using the Motorola assembler, the programmer does not need to calculate the offset, because the assembler determines the proper offset and verifies that it is within the span of the branch.

11.4 Instruction Types

The MCU instructions fall into the following five categories:

- Register/Memory Instructions
- Read-Modify-Write Instructions
- Jump/Branch Instructions
- Bit Manipulation Instructions
- Control Instructions

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11.4.1 Register/Memory Instructions

These instructions operate on CPU registers and memory locations. Most of them use two operands. One operand is in either the accumulator or the index register. The CPU finds the other operand in memory.

Table 11-1. Register/Memory Instructions

Instruction	Mnemonic
Add Memory Byte and Carry Bit to Accumulator	ADC
Add Memory Byte to Accumulator	ADD
AND Memory Byte with Accumulator	AND
Bit Test Accumulator	BIT
Compare Accumulator	CMP
Compare Index Register with Memory Byte	CPX
EXCLUSIVE OR Accumulator with Memory Byte	EOR
Load Accumulator with Memory Byte	LDA
Load Index Register with Memory Byte	LDX
Multiply	MUL
OR Accumulator with Memory Byte	ORA
Subtract Memory Byte and Carry Bit from Accumulator	SBC
Store Accumulator in Memory	STA
Store Index Register in Memory	STX
Subtract Memory Byte from Accumulator	SUB

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11.4.2 Read-Modify-Write Instructions

These instructions read a memory location or a register, modify its contents, and write the modified value back to the memory location or to the register.

NOTE: *Do not use read-modify-write operations on write-only registers.*

Table 11-2. Read-Modify-Write Instructions

Instruction	Mnemonic
Arithmetic Shift Left (Same as LSL)	ASL
Arithmetic Shift Right	ASR
Bit Clear	BCLR(1)
Bit Set	BSET(1)
Clear Register	CLR
Complement (One's Complement)	COM
Decrement	DEC
Increment	INC
Logical Shift Left (Same as ASL)	LSL
Logical Shift Right	LSR
Negate (Two's Complement)	NEG
Rotate Left through Carry Bit	ROL
Rotate Right through Carry Bit	ROR
Test for Negative or Zero	TST(2)

1. Unlike other read-modify-write instructions, BCLR and BSET use only direct addressing.
2. TST is an exception to the read-modify-write sequence because it does not write a replacement value.

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11.4.3 Jump/Branch Instructions

Jump instructions allow the CPU to interrupt the normal sequence of the program counter. The unconditional jump instruction (JMP) and the jump-to-subroutine instruction (JSR) have no register operand. Branch instructions allow the CPU to interrupt the normal sequence of the program counter when a test condition is met. If the test condition is not met, the branch is not performed.

The BRCLR and BRSET instructions cause a branch based on the state of any readable bit in the first 256 memory locations. These 3-byte instructions use a combination of direct addressing and relative addressing. The direct address of the byte to be tested is in the byte following the opcode. The third byte is the signed offset byte. The CPU finds the effective branch destination by adding the third byte to the program counter if the specified bit tests true. The bit to be tested and its condition (set or clear) is part of the opcode. The span of branching is from –128 to +127 from the address of the next location after the branch instruction. The CPU also transfers the tested bit to the carry/borrow bit of the condition code register.

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Table 11-3. Jump and Branch Instructions

Instruction	Mnemonic
Branch if Carry Bit Clear	BCC
Branch if Carry Bit Set	BCS
Branch if Equal	BEQ
Branch if Half-Carry Bit Clear	BHCC
Branch if Half-Carry Bit Set	BHCS
Branch if Higher	BHI
Branch if Higher or Same	BHS
Branch if $\overline{\text{IRQ}}$ Pin High	BIH
Branch if $\overline{\text{IRQ}}$ Pin Low	BIL
Branch if Lower	BLO
Branch if Lower or Same	BLS
Branch if Interrupt Mask Clear	BMC
Branch if Minus	BMI
Branch if Interrupt Mask Set	BMS
Branch if Not Equal	BNE
Branch if Plus	BPL
Branch Always	BRA
Branch if Bit Clear	BRCLR
Branch Never	BRN
Branch if Bit Set	BRSET
Branch to Subroutine	BSR
Unconditional Jump	JMP
Jump to Subroutine	JSR

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11.4.4 Bit Manipulation Instructions

The CPU can set or clear any writable bit in the first 256 bytes of memory, which includes I/O registers and on-chip RAM locations. The CPU can also test and branch based on the state of any bit in any of the first 256 memory locations.

Table 11-4. Bit Manipulation Instructions

Instruction	Mnemonic
Bit Clear	BCLR
Branch if Bit Clear	BRCLR
Branch if Bit Set	BRSET
Bit Set	BSET

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11.4.5 Control Instructions

These instructions act on CPU registers and control CPU operation during program execution.

Table 11-5. Control Instructions

Instruction	Mnemonic
Clear Carry Bit	CLC
Clear Interrupt Mask	CLI
No Operation	NOP
Reset Stack Pointer	RSP
Return from Interrupt	RTI
Return from Subroutine	RTS
Set Carry Bit	SEC
Set Interrupt Mask	SEI
Stop Oscillator and Enable $\overline{\text{IRQ}}$ Pin	STOP
Software Interrupt	SWI
Transfer Accumulator to Index Register	TAX
Transfer Index Register to Accumulator	TXA
Stop CPU Clock and Enable Interrupts	WAIT

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11.5 Instruction Set Summary

Table 11-6. Instruction Set Summary

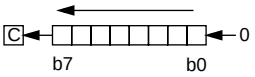
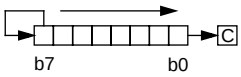
Source Form	Operation	Description	Effect on CCR					Address Mode	Opcode	Operand	Cycles
			H	I	N	Z	C				
ADC #*opr* ADC *opr* ADC *opr* ADC *opr*,X ADC *opr*,X ADC ,X	Add with Carry	A ← (A) + (M) + (C)	↕	—	↕	↕	↕	IMM DIR EXT IX2 IX1 IX	A9 B9 C9 D9 E9 F9	ii dd hh ll ee ff ff	2 3 4 5 4 3
ADD #*opr* ADD *opr* ADD *opr* ADD *opr*,X ADD *opr*,X ADD ,X	Add without Carry	A ← (A) + (M)	↕	—	↕	↕	↕	IMM DIR EXT IX2 IX1 IX	AB BB CB DB EB FB	ii dd hh ll ee ff ff	2 3 4 5 4 3
AND #*opr* AND *opr* AN*D opr* AND *opr*,X AND *opr*,X AND ,X	Logical AND	A ← (A) ∧ (M)	—	—	↕	↕	—	IMM DIR EXT IX2 IX1 IX	A4 B4 C4 D4 E4 F4	ii dd hh ll ee ff ff	2 3 4 5 4 3
ASL *opr* ASLA ASLX ASL *opr*,X ASL ,X	Arithmetic Shift Left (Same as LSL)		—	—	↕	↕	↕	DIR INH INH IX1 IX	38 48 58 68 78	dd ff 	5 3 3 6 5
ASR *opr* ASRA ASRX ASR *opr*,X ASR ,X	Arithmetic Shift Right		—	—	↕	↕	↕	DIR INH INH IX1 IX	37 47 57 67 77	dd ff 	5 3 3 6 5
BCC *rel*	Branch if Carry Bit Clear	PC ← (PC) + 2 + *rel* ? C = 0	—	—	—	—	—	REL	24	rr	3
BCLR *n opr*	Clear Bit n	Mn ← 0	—	—	—	—	—	DIR (b0) DIR (b1) DIR (b2) DIR (b3) DIR (b4) DIR (b5) DIR (b6) DIR (b7)	11 13 15 17 19 1B 1D 1F	dd dd dd dd dd dd dd dd	5 5 5 5 5 5 5 5
BCS *rel*	Branch if Carry Bit Set (Same as BLO)	PC ← (PC) + 2 + *rel* ? C = 1	—	—	—	—	—	REL	25	rr	3
BEQ *rel*	Branch if Equal	PC ← (PC) + 2 + *rel* ? Z = 1	—	—	—	—	—	REL	27	rr	3
BHCC *rel*	Branch if Half-Carry Bit Clear	PC ← (PC) + 2 + *rel* ? H = 0	—	—	—	—	—	REL	28	rr	3
BHCS *rel*	Branch if Half-Carry Bit Set	PC ← (PC) + 2 + *rel* ? H = 1	—	—	—	—	—	REL	29	rr	3

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Table 11-6. Instruction Set Summary (Continued)

Source Form	Operation	Description	Effect on CCR					Address Mode	Opcode	Operand	Cycles
			H	I	N	Z	C				
BHI *rel*	Branch if Higher	PC ← (PC) + 2 + *rel* ? C ∨ Z = 0	—	—	—	—	—	REL	22	rr	3
BHS *rel*	Branch if Higher or Same	PC ← (PC) + 2 + *rel* ? C = 0	—	—	—	—	—	REL	24	rr	3
BIH *rel*	Branch if IRQ Pin High	PC ← (PC) + 2 + *rel* ? IRQ = 1	—	—	—	—	—	REL	2F	rr	3
BIL *rel*	Branch if IRQ Pin Low	PC ← (PC) + 2 + *rel* ? IRQ = 0	—	—	—	—	—	REL	2E	rr	3
BIT #*opr* BIT *opr* BIT *opr* BIT *opr*,X BIT *opr*,X BIT ,X	Bit Test Accumulator with Memory Byte	(A) ∧ (M)	—	—	↕	↕	—	IMM DIR EXT IX2 IX1 IX	A5 B5 C5 D5 E5 F5	ii dd hh ll ee ff ff	2 3 4 5 4 3
BLO *rel*	Branch if Lower (Same as BCS)	PC ← (PC) + 2 + *rel* ? C = 1	—	—	—	—	—	REL	25	rr	3
BLS *rel*	Branch if Lower or Same	PC ← (PC) + 2 + *rel* ? C ∨ Z = 1	—	—	—	—	—	REL	23	rr	3
BMC *rel*	Branch if Interrupt Mask Clear	PC ← (PC) + 2 + *rel* ? I = 0	—	—	—	—	—	REL	2C	rr	3
BMI *rel*	Branch if Minus	PC ← (PC) + 2 + *rel* ? N = 1	—	—	—	—	—	REL	2B	rr	3
BMS *rel*	Branch if Interrupt Mask Set	PC ← (PC) + 2 + *rel* ? I = 1	—	—	—	—	—	REL	2D	rr	3
BNE *rel*	Branch if Not Equal	PC ← (PC) + 2 + *rel* ? Z = 0	—	—	—	—	—	REL	26	rr	3
BPL *rel*	Branch if Plus	PC ← (PC) + 2 + *rel* ? N = 0	—	—	—	—	—	REL	2A	rr	3
BRA *rel*	Branch Always	PC ← (PC) + 2 + *rel* ? 1 = 1	—	—	—	—	—	REL	20	rr	3
BRCLR *n opr rel*	Branch if Bit n Clear	PC ← (PC) + 2 + *rel* ? Mn = 0	—	—	—	—	↕	DIR (b0) DIR (b1) DIR (b2) DIR (b3) DIR (b4) DIR (b5) DIR (b6) DIR (b7)	01 03 05 07 09 0B 0D 0F	dd rr dd rr dd rr dd rr dd rr dd rr dd rr dd rr	5 5 5 5 5 5 5 5
BRN *rel*	Branch Never	PC ← (PC) + 2 + *rel* ? 1 = 0	—	—	—	—	—	REL	21	rr	3
BRSET *n opr rel*	Branch if Bit n Set	PC ← (PC) + 2 + *rel* ? Mn = 1	—	—	—	—	↕	DIR (b0) DIR (b1) DIR (b2) DIR (b3) DIR (b4) DIR (b5) DIR (b6) DIR (b7)	00 02 04 06 08 0A 0C 0E	dd rr dd rr dd rr dd rr dd rr dd rr dd rr dd rr	5 5 5 5 5 5 5 5
BSET *n opr*	Set Bit n	Mn ← 1	—	—	—	—	—	DIR (b0) DIR (b1) DIR (b2) DIR (b3) DIR (b4) DIR (b5) DIR (b6) DIR (b7)	10 12 14 16 18 1A 1C 1E	dd dd dd dd dd dd dd dd	5 5 5 5 5 5 5 5

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Table 11-6. Instruction Set Summary (Continued)

Source Form	Operation	Description	Effect on CCR					Address Mode	Opcode	Operand	Cycles
			H	I	N	Z	C				
BSR *rel*	Branch to Subroutine	PC ← (PC) + 2; push (PCL) SP ← (SP) – 1; push (PCH) SP ← (SP) – 1 PC ← (PC) + *rel*	—	—	—	—	—	REL	AD	rr	6
CLC	Clear Carry Bit	C ← 0	—	—	—	—	0	INH	98		2
CLI	Clear Interrupt Mask	I ← 0	—	0	—	—	—	INH	9A		2
CLR *opr* CLRA CLRX CLR *opr*,X CLR ,X	Clear Byte	M ← $00 A ← $00 X ← $00 M ← $00 M ← $00	—	—	0	1	—	DIR INH INH IX1 IX	3F 4F 5F 6F 7F	dd ff 	5 3 3 6 5
CMP #*opr* CMP *opr* CMP *opr* CMP *opr*,X CMP *opr*,X CMP ,X	Compare Accumulator with Memory Byte	(A) – (M)	—	—	↕	↕	↕	IMM DIR EXT IX2 IX1 IX	A1 B1 C1 D1 E1 F1	ii dd hh ll ee ff ff 	2 3 4 5 4 3
COM *opr* COMA COMX COM *opr*,X COM ,X	Complement Byte (One's Complement)	M ← ($\overline{M}$) = $FF – (M) A ← ($\overline{A}$) = $FF – (A) X ← ($\overline{X}$) = $FF – (X) M ← ($\overline{M}$) = $FF – (M) M ← ($\overline{M}$) = $FF – (M)	—	—	↕	↕	1	DIR INH INH IX1 IX	33 43 53 63 73	dd ff 	5 3 3 6 5
CPX #*opr* CPX *opr* CPX *opr* CPX *opr*,X CPX *opr*,X CPX ,X	Compare Index Register with Memory Byte	(X) – (M)	—	—	↕	↕	↕	IMM DIR EXT IX2 IX1 IX	A3 B3 C3 D3 E3 F3	ii dd hh ll ee ff ff 	2 3 4 5 4 3
DEC *opr* DECA DECX DEC *opr*,X DEC ,X	Decrement Byte	M ← (M) – 1 A ← (A) – 1 X ← (X) – 1 M ← (M) – 1 M ← (M) – 1	—	—	↕	↕	—	DIR INH INH IX1 IX	3A 4A 5A 6A 7A	dd ff 	5 3 3 6 5
EOR #*opr* EOR *opr* EOR *opr* EOR *opr*,X EOR *opr*,X EOR ,X	EXCLUSIVE OR Accumulator with Memory Byte	A ← (A) ⊕ (M)	—	—	↕	↕	—	IMM DIR EXT IX2 IX1 IX	A8 B8 C8 D8 E8 F8	ii dd hh ll ee ff ff 	2 3 4 5 4 3
INC *opr* INCA INCX INC *opr*,X INC ,X	Increment Byte	M ← (M) + 1 A ← (A) + 1 X ← (X) + 1 M ← (M) + 1 M ← (M) + 1	—	—	↕	↕	—	DIR INH INH IX1 IX	3C 4C 5C 6C 7C	dd ff 	5 3 3 6 5

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Table 11-6. Instruction Set Summary (Continued)

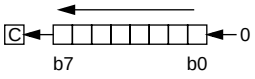
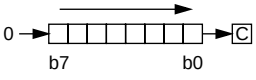
Source Form	Operation	Description	Effect on CCR					Address Mode	Opcode	Operand	Cycles
			H	I	N	Z	C				
JMP *opr* JMP *opr* JMP *opr*,X JMP *opr*,X JMP ,X	Unconditional Jump	PC ← Jump Address	—	—	—	—	—	DIR EXT IX2 IX1 IX	BC CC DC EC FC	dd hh ll ee ff ff	2 3 4 3 2
JSR *opr* JSR *opr* JSR *opr*,X JSR *opr*,X JSR ,X	Jump to Subroutine	PC ← (PC) + n (n = 1, 2, or 3) Push (PCL); SP ← (SP) – 1 Push (PCH); SP ← (SP) – 1 PC ← Effective Address	—	—	—	—	—	DIR EXT IX2 IX1 IX	BD CD DD ED FD	dd hh ll ee ff ff	5 6 7 6 5
LDA #*opr* LDA *opr* LDA *opr* LDA *opr*,X LDA *opr*,X LDA ,X	Load Accumulator with Memory Byte	A ← (M)	—	—	↕	↕	—	IMM DIR EXT IX2 IX1 IX	A6 B6 C6 D6 E6 F6	ii dd hh ll ee ff ff	2 3 4 5 4 3
LDX #*opr* LDX *opr* LDX *opr* LDX *opr*,X LDX *opr*,X LDX ,X	Load Index Register with Memory Byte	X ← (M)	—	—	↕	↕	—	IMM DIR EXT IX2 IX1 IX	AE BE CE DE EE FE	ii dd hh ll ee ff ff	2 3 4 5 4 3
LSL *opr* LSLA LSLX LSL *opr*,X LSL ,X	Logical Shift Left (Same as ASL)		—	—	↕	↕	↕	DIR INH INH IX1 IX	38 48 58 68 78	dd ff 	5 3 3 6 5
LSR *opr* LSRA LSRX LSR *opr*,X LSR ,X	Logical Shift Right		—	—	0	↕	↕	DIR INH INH IX1 IX	34 44 54 64 74	dd ff 	5 3 3 6 5
MUL	Unsigned Multiply	X : A ← (X) × (A)	0	—	—	—	0	INH	42		11
NEG *opr* NEGA NEGX NEG *opr*,X NEG ,X	Negate Byte (Two's Complement)	M ← –(M) = $00 – (M) A ← –(A) = $00 – (A) X ← –(X) = $00 – (X) M ← –(M) = $00 – (M) M ← –(M) = $00 – (M)	—	—	↕	↕	↕	DIR INH INH IX1 IX	30 40 50 60 70	dd ff 	5 3 3 6 5
NOP	No Operation		—	—	—	—	—	INH	9D		2
ORA #*opr* ORA *opr* ORA *opr* ORA *opr*,X ORA *opr*,X ORA ,X	Logical OR Accumulator with Memory	A ← (A) ∨ (M)	—	—	↕	↕	—	IMM DIR EXT IX2 IX1 IX	AA BA CA DA EA FA	ii dd hh ll ee ff ff	2 3 4 5 4 3

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Table 11-6. Instruction Set Summary (Continued)

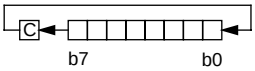
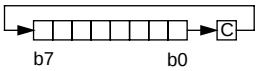
Source Form	Operation	Description	Effect on CCR					Address Mode	Opcode	Operand	Cycles
			H	I	N	Z	C				
ROL *opr* ROLA ROLX ROL *opr*,X ROL ,X	Rotate Byte Left through Carry Bit		—	—	↕	↕	↕	DIR INH INH IX1 IX	39 49 59 69 79	dd ff 	5 3 3 6 5
ROR *opr* RORA RORX ROR *opr*,X ROR ,X	Rotate Byte Right through Carry Bit		—	—	↕	↕	↕	DIR INH INH IX1 IX	36 46 56 66 76	dd ff 	5 3 3 6 5
RSP	Reset Stack Pointer	SP ← $00FF	—	—	—	—	—	INH	9C		2
RTI	Return from Interrupt	SP ← (SP) + 1; Pull (CCR) SP ← (SP) + 1; Pull (A) SP ← (SP) + 1; Pull (X) SP ← (SP) + 1; Pull (PCH) SP ← (SP) + 1; Pull (PCL)	↕	↕	↕	↕	↕	INH	80		9
RTS	Return from Subroutine	SP ← (SP) + 1; Pull (PCH) SP ← (SP) + 1; Pull (PCL)	—	—	—	—	—	INH	81		6
SBC #*opr* SBC *opr* SBC *opr* SBC *opr*,X SBC *opr*,X SBC ,X	Subtract Memory Byte and Carry Bit from Accumulator	A ← (A) – (M) – (C)	—	—	↕	↕	↕	IMM DIR EXT IX2 IX1 IX	A2 B2 C2 D2 E2 F2	ii dd hh ll ee ff ff	2 3 4 5 4 3
SEC	Set Carry Bit	C ← 1	—	—	—	—	1	INH	99		2
SEI	Set Interrupt Mask	I ← 1	—	1	—	—	—	INH	9B		2
STA *opr* STA *opr* STA *opr*,X STA *opr*,X STA ,X	Store Accumulator in Memory	M ← (A)	—	—	↕	↕	—	DIR EXT IX2 IX1 IX	B7 C7 D7 E7 F7	dd hh ll ee ff ff	4 5 6 5 4
STOP	Stop Oscillator and Enable IRQ Pin		—	0	—	—	—	INH	8E		2
STX *opr* STX *opr* STX *opr*,X STX *opr*,X STX ,X	Store Index Register In Memory	M ← (X)	—	—	↕	↕	—	DIR EXT IX2 IX1 IX	BF CF DF EF FF	dd hh ll ee ff ff	4 5 6 5 4
SUB #*opr* SUB *opr* SUB *opr* SUB *opr*,X SUB *opr*,X SUB ,X	Subtract Memory Byte from Accumulator	A ← (A) – (M)	—	—	↕	↕	↕	IMM DIR EXT IX2 IX1 IX	A0 B0 C0 D0 E0 F0	ii dd hh ll ee ff ff	2 3 4 5 4 3

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Table 11-6. Instruction Set Summary (Continued)

Source Form	Operation	Description	Effect on CCR					Address Mode	Opcode	Operand	Cycles
			H	I	N	Z	C				
SWI	Software Interrupt	PC ← (PC) + 1; Push (PCL) SP ← (SP) – 1; Push (PCH) SP ← (SP) – 1; Push (X) SP ← (SP) – 1; Push (A) SP ← (SP) – 1; Push (CCR) SP ← (SP) – 1; I ← 1 PCH ← Interrupt Vector High Byte PCL ← Interrupt Vector Low Byte	—	1	—	—	—	INH	83		10
TAX	Transfer Accumulator to Index Register	X ← (A)	—	—	—	—	—	INH	97		2
TST *opr* TSTA TSTX TST *opr*,X TST ,X	Test Memory Byte for Negative or Zero	(M) – $00	—	—	↕	↕	—	DIR INH INH IX1 IX	3D 4D 5D 6D 7D	dd ff 	4 3 3 5 4
TXA	Transfer Index Register to Accumulator	A ← (X)	—	—	—	—	—	INH	9F		2
WAIT	Stop CPU Clock and Enable Interrupts		—	0	—	—	—	INH	8F		2

A	Accumulator	*opr*	Operand (one or two bytes)
C	Carry/borrow flag	PC	Program counter
CCR	Condition code register	PCH	Program counter high byte
dd	Direct address of operand	PCL	Program counter low byte
dd rr	Direct address of operand and relative offset of branch instruction	REL	Relative addressing mode
DIR	Direct addressing mode	*rel*	Relative program counter offset byte
ee ff	High and low bytes of offset in indexed, 16-bit offset addressing	rr	Relative program counter offset byte
EXT	Extended addressing mode	SP	Stack pointer
ff	Offset byte in indexed, 8-bit offset addressing	X	Index register
H	Half-carry flag	Z	Zero flag
hh ll	High and low bytes of operand address in extended addressing	#	Immediate value
I	Interrupt mask	∧	Logical AND
ii	Immediate operand byte	∨	Logical OR
IMM	Immediate addressing mode	⊕	Logical EXCLUSIVE OR
INH	Inherent addressing mode	( )	Contents of
IX	Indexed, no offset addressing mode	–( )	Negation (two's complement)
IX1	Indexed, 8-bit offset addressing mode	←	Loaded with
IX2	Indexed, 16-bit offset addressing mode	?	If
M	Memory location	:	Concatenated with
N	Negative flag	↕	Set or cleared
n	Any bit	—	Not affected

11.6 Opcode Map

See **Table 11-7.**

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Table 11-7. Opcode Map

	Bit Manipulation		Branch	Read-Modify-Write					Control		Register/Memory						
	DIR	DIR	REL	DIR	INH	INH	IX1	IX	INH	INH	IMM	DIR	EXT	IX2	IX1	IX	
MSB / LSB	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F	MSB / LSB
0	5 BRSET0 3 DIR	5 BSET0 2 DIR	3 BRA 2 REL	5 NEG 2 DIR	3 NEGA 1 INH	3 NEGX 1 INH	6 NEG 2 IX1	5 NEG 1 IX	9 RTI 1 INH		2 SUB 2 IMM	3 SUB 2 DIR	4 SUB 3 EXT	5 SUB 3 IX2	4 SUB 2 IX1	3 SUB 1 IX	0
1	5 BRCLR0 3 DIR	5 BCLR0 2 DIR	3 BRN 2 REL						6 RTS 1 INH		2 CMP 2 IMM	3 CMP 2 DIR	4 CMP 3 EXT	5 CMP 3 IX2	4 CMP 2 IX1	3 CMP 1 IX	1
2	5 BRSET1 3 DIR	5 BSET1 2 DIR	3 BHI 2 REL		11 MUL 1 INH						2 SBC 2 IMM	3 SBC 2 DIR	4 SBC 3 EXT	5 SBC 3 IX2	4 SBC 2 IX1	3 SBC 1 IX	2
3	5 BRCLR1 3 DIR	5 BCLR1 2 DIR	3 BLS 2 REL	5 COM 2 DIR	3 COMA 1 INH	3 COMX 1 INH	6 COM 2 IX1	5 COM 1 IX	10 SWI 1 INH		2 CPX 2 IMM	3 CPX 2 DIR	4 CPX 3 EXT	5 CPX 3 IX2	4 CPX 2 IX1	3 CPX 1 IX	3
4	5 BRSET2 3 DIR	5 BSET2 2 DIR	3 BCC 2 REL	5 LSR 2 DIR	3 LSRA 1 INH	3 LSRX 1 INH	6 LSR 2 IX1	5 LSR 1 IX			2 AND 2 IMM	3 AND 2 DIR	4 AND 3 EXT	5 AND 3 IX2	4 AND 2 IX1	3 AND 1 IX	4
5	5 BRCLR2 3 DIR	5 BCLR2 2 DIR	3 BCS/BLO 2 REL								2 BIT 2 IMM	3 BIT 2 DIR	4 BIT 3 EXT	5 BIT 3 IX2	4 BIT 2 IX1	3 BIT 1 IX	5
6	5 BRSET3 3 DIR	5 BSET3 2 DIR	3 BNE 2 REL	5 ROR 2 DIR	3 RORA 1 INH	3 RORX 1 INH	6 ROR 2 IX1	5 ROR 1 IX			2 LDA 2 IMM	3 LDA 2 DIR	4 LDA 3 EXT	5 LDA 3 IX2	4 LDA 2 IX1	3 LDA 1 IX	6
7	5 BRCLR3 3 DIR	5 BCLR3 2 DIR	3 BEQ 2 REL	5 ASR 2 DIR	3 ASRA 1 INH	3 ASRX 1 INH	6 ASR 2 IX1	5 ASR 1 IX		2 TAX 1 INH		4 STA 2 DIR	5 STA 3 EXT	6 STA 3 IX2	5 STA 2 IX1	4 STA 1 IX	7
8	5 BRSET4 3 DIR	5 BSET4 2 DIR	3 BHCC 2 REL	5 ASL/LSL 2 DIR	3 ASLA/LSLA 1 INH	3 ASLX/LSLX 1 INH	6 ASL/LSL 2 IX1	5 ASL/LSL 1 IX		2 CLC 1 INH	2 EOR 2 IMM	3 EOR 2 DIR	4 EOR 3 EXT	5 EOR 3 IX2	4 EOR 2 IX1	3 EOR 1 IX	8
9	5 BRCLR4 3 DIR	5 BCLR4 2 DIR	3 BHCS 2 REL	5 ROL 2 DIR	3 ROLA 1 INH	3 ROLX 1 INH	6 ROL 2 IX1	5 ROL 1 IX		2 SEC 1 INH	2 ADC 2 IMM	3 ADC 2 DIR	4 ADC 3 EXT	5 ADC 3 IX2	4 ADC 2 IX1	3 ADC 1 IX	9
A	5 BRSET5 3 DIR	5 BSET5 2 DIR	3 BPL 2 REL	5 DEC 2 DIR	3 DECA 1 INH	3 DECX 1 INH	6 DEC 2 IX1	5 DEC 1 IX		2 CLI 1 INH	2 ORA 2 IMM	3 ORA 2 DIR	4 ORA 3 EXT	5 ORA 3 IX2	4 ORA 2 IX1	3 ORA 1 IX	A
B	5 BRCLR5 3 DIR	5 BCLR5 2 DIR	3 BMI 2 REL							2 SEI 1 INH	2 ADD 2 IMM	3 ADD 2 DIR	4 ADD 3 EXT	5 ADD 3 IX2	4 ADD 2 IX1	3 ADD 1 IX	B
C	5 BRSET6 3 DIR	5 BSET6 2 DIR	3 BMC 2 REL	5 INC 2 DIR	3 INCA 1 INH	3 INCX 1 INH	6 INC 2 IX1	5 INC 1 IX		2 RSP 1 INH		2 JMP 2 DIR	3 JMP 3 EXT	4 JMP 3 IX2	3 JMP 2 IX1	2 JMP 1 IX	C
D	5 BRCLR6 3 DIR	5 BCLR6 2 DIR	3 BMS 2 REL	4 TST 2 DIR	3 TSTA 1 INH	3 TSTX 1 INH	5 TST 2 IX1	4 TST 1 IX		2 NOP 1 INH	6 BSR 2 REL	5 JSR 2 DIR	6 JSR 3 EXT	7 JSR 3 IX2	6 JSR 2 IX1	5 JSR 1 IX	D
E	5 BRSET7 3 DIR	5 BSET7 2 DIR	3 BIL 2 REL						2 STOP 1 INH		2 LDX 2 IMM	3 LDX 2 DIR	4 LDX 3 EXT	5 LDX 3 IX2	4 LDX 2 IX1	3 LDX 1 IX	E
F	5 BRCLR7 3 DIR	5 BCLR7 2 DIR	3 BIH 2 REL	5 CLR 2 DIR	3 CLRA 1 INH	3 CLRX 1 INH	6 CLR 2 IX1	5 CLR 1 IX	2 WAIT 1 INH	2 TXA 1 INH		4 STX 2 DIR	5 STX 3 EXT	6 STX 3 IX2	5 STX 2 IX1	4 STX 1 IX	F

INH = Inherent
IMM = Immediate
DIR = Direct
EXT = Extended

REL = Relative
IX = Indexed, No Offset
IX1 = Indexed, 8-Bit Offset
IX2 = Indexed, 16-Bit Offset

LSB of Opcode in Hexadecimal

MSB / LSB	0
0	5 BRSET0 3 DIR

MSB of Opcode in Hexadecimal
Number of Cycles
Opcode Mnemonic
Number of Bytes/Addressing Mode

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Go to: www.freescale.com

Section 12. Electrical Specifications

12.1 Contents

12.2 Introduction

This section contains parametric and timing information.

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12.3 Maximum Ratings

Maximum ratings are the extreme limits to which the MCU can be exposed without permanently damaging it.

The MCU contains circuitry to protect the inputs against damage from high static voltages; however, do not apply voltages higher than those shown in this table. Keep V_{In} and V_{Out} within the range $V_{SS} \le (V_{In}$ or $V_{Out}) \le V_{DD}$. Connect unused inputs to the appropriate voltage level, either V_{SS} or V_{DD}.

Rating	Symbol	Value	Unit
Supply voltage	V_{DD} V_{LCD1} V_{LCD2} V_{LCD3}	–0.3 to +7.0 V_{SS} –0.3 to V_{DD} +0.3 V_{SS} –0.3 to V_{DD} +0.3 V_{SS} –0.3 to V_{DD} +0.3	V
Input voltage	V_{In}	V_{SS} –0.3 to V_{DD} + 0.3	V
Self-check mode ($\overline{IRQ1}$ pin only)	V_{In}	V_{SS} –0.3 to 2 x V_{DD} + 0.3	V
Output voltage	V_{Out}	V_{SS} –0.3 to V_{DD} + 0.3	V
Current drain per pin excluding V_{DD} and V_{SS}	I	12.5	mA
Operating junction temperature	T_J	+150	°C
Storage temperature range	T_{stg}	–55 to +150	°C

NOTE: *This device is not guaranteed to operate properly at the maximum ratings. Refer to* ***12.7 5.0-Volt DC Electrical Characteristics*** *and* ***12.8 3.3-Volt DC Electrical Characteristics*** *for guaranteed operating conditions.*

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12.4 Operating Temperature Range

Characteristic	Symbol	Value	Unit
Operating temperature range MC68HC05L5 (standard) MC68HC05L5C (extended)	T_A	T_L to T_H 0 to +70 –40 to +85	°C

12.5 Thermal Characteristics

Characteristic	Symbol	Value	Unit
Thermal resistance 80-pin plastic quad flat pack	θ_{JA}	120	°C/W

12.6 Recommended Operating Conditions

Rating[1]	Symbol	Min	Typ	Max	Unit
(f_{OP} = 2.1 MHz)	V_{DD}	4.5	5.0	5.5	V
(f_{OP} = 1.0 MHz)	V_{DD}	2.2	—	5.5	V
Supply voltage	V_{LCD1}	V_{DD} – 1/3 V_{LCD}			V
	V_{LCD2}	V_{DD} – 2/3 V_{LCD}			V
	V_{LCD3}	V_{DD} – 3/3 V_{LCD}			V
Fast clock oscillation frequency	f_{OSC}	—	3.52	4.2	MHz
External capacitance (f_{OSC} = 3.52 MHz)	C1 C2	— —	33 33	— —	pF
Slow clock oscillation frequency	f_{XOSC}	—	32.768	—	MHz
External capacitance (f_{XOSC} = 32.768 kHz)	CX1 CX2	— —	18 22	— —	pF

1. +2.2 ≤ V_{DD} ≤ +5.5 Vdc, V_{SS} = 0 Vdc, $T_L \le T_A \le T_H$, unless otherwise noted

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12.7 5.0-Volt DC Electrical Characteristics

Characteristic[1]	Symbol	Min	Typ	Max	Unit
Output voltage I_{Load} = 10.0 µA I_{Load} = –10.0 µA	 V_{OL} V_{OH}	 — V_{DD} –0.1	 — —	 0.1 —	 V
Output high voltage (V_{DD} = 5.0 V) (I_{Load} = –0.4 mA) PA0–PA7, PC0–PC5, PD1–PD7, PE0–PE7	V_{OH}	V_{DD} –0.8	—	—	V
Output low voltage (V_{DD} = 5.0 V) (I_{Load} = 0.8 mA) PA0–PA7, PC0–PC5, PD1–PD7, PE0–PE7	V_{OL}	—	—	0.4	V
Input high voltage PA0–PA7, PB0–PB7, PC0–PC7, $\overline{\text{RESET}}$, OSC1, XOSC1	V_{IH}	0.8 x V_{DD}	—	V_{DD}	V
Input low voltage PA0–PA7, PB0–PB7, PC0–PC7, $\overline{\text{RESET}}$, OSC1, XOSC1	V_{IL}	V_{SS}	—	0.2 x V_{DD}	V
Supply current[2], [3], [4], [5] Run (f_{op} = 2.1 MHz) Wait (f_{op} = 2.1 MHz) Stop No clock XOSC = 32.768 kHz, V_{DD} = 5.0 V, T_A = +25 °C	 I_{DD}	 — —	 6.0 3.0 3.0 17.0	 12.0 6.0 10.0 —	 mA mA µA µA
Input current[6] (with pullups disabled) PA0–PA7, PB0–PB7, PC0–PC7, $\overline{\text{RESET}}$, OSC1, XOSC1	I_{in}	—	—	± 1.0	µA
Input current[6] (with pullups enabled, V_{DD} = 5.0 V) PA0–PA7 PB0–PB7 PC0–PC7	 I_{in}	 40 40 150	 150 150 500	 340 340 1000	 µA µA µA
LCD pin output impedance FP0–FP26 BP0–BP3	 Zo, FP Zo, BP	 — —	 10 5	 20 18	 kΩ kΩ

1. +4.5 ≤ V_{DD} ≤ +5.5 Vdc, V_{SS} = 0 Vdc, $T_L \le T_A \le T_H$, unless otherwise noted. All values shown reflect average measurements. Typical values at midpoint of voltage range, 25 °C only.
2. Run (Operating) I_{DD}, wait I_{DD}; measured using external square wave clock source (f_{OSC} = 4.2 MHz); all inputs 0.2 V from rail (V_{SS} or V_{DD}); no dc loads; less than 50 pF on all outputs; C_L = 20 pF on OSC2
3. Wait, stop I_{DD}; all ports configured as inputs; V_{IL} = 0.2 V; V_{IH} = V_{DD} –0.2 V
4. Stop I_{DD} measured with OSC1 = V_{SS}.
5. Wait I_{DD} is affected linearly by the OSC2 capacitance.
6. Input current is measured with output transistor turned off and V_{In} = 0 V.

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12.8 3.3-Volt DC Electrical Characteristics

Characteristic[1]	Symbol	Min	Typ	Max	Unit
Output voltage I_{Load} = 10.0 µA I_{Load} = –10.0 µA	 V_{OL} V_{OH}	 — V_{DD} –0.1	 — —	 0.1 —	 V
Output high voltage (V_{DD} = 3.5 V) (I_{Load} = –0.4 mA) PA0–PA7, PC0–PC5, PD1–PD7, PE0–PE7	V_{OH}	V_{DD} –0.8	—	—	V
Output low voltage (V_{DD} = 3.5 V) (I_{Load} = 0.8 mA) PA0–PA7, PC0–PC5, PD1–PD7, PE0–PE7	V_{OL}	—	—	0.4	V
Input high voltage PA0–PA7, PB0–PB7, PC0–PC7, $\overline{\text{RESET}}$,OSC1, XOSC1	V_{IH}	0.8 x V_{DD}	—	V_{DD}	V
Input low voltage PA0–PA7, PB0–PB7, PC0–PC7, $\overline{\text{RESET}}$, OSC1, XOSC1	V_{IL}	V_{SS}	—	02 x V_{DD}	V
Supply current[2], [3], [4], [5] Run (f_{op} = 1.0 MHz) Wait (f_{op} = 1.0 MHz) Stop No clock XOSC = 32.768 kHz, V_{DD} = 3.0 V, T_A= +25 °C	 I_{DD}	 — —	 1.8 0.8 2.0 8.0	 8.0 5.0 10.0 —	 mA mA µA µA
Input current[6] (with pullups disabled) PA0–PA7, PB0–PB7, PC0–PC7, $\overline{\text{RESET}}$, OSC1, XOSC1	I_{In}	—	—	± 1.0	µA
Input current[6] (with pullups enabled, V_{DD} = 3.3 V) PA0–PA7 PB0–PB7 PC0–PC7	 I_{In}	 20 20 60	 80 80 300	 230 230 760	 µA µA µA
LCD pin output impedance FP0–FP26 BP0–BP3	 Zo, FP Zo, BP	 — —	 10 5	 20 18	 kΩ kΩ

1. +3.0 ≤ V_{DD} < +4.5 Vdc, V_{SS} = 0 Vdc, $T_L \le T_A \le T_H$, unless otherwise noted. All values shown reflect average measurements. Typical values at midpoint of voltage range, 25 °C only.
2. Run (Operating) I_{DD}, wait I_{DD}; measured using external square wave clock source (f_{OSC} = 2.0 MHz); all inputs 0.2 V from rail (V_{SS} or V_{DD}); no dc loads; less than 50 pF on all outputs; C_L = 20 pF on OSC2
3. Wait, stop I_{DD}; all ports configured as inputs; V_{IL} = 0.2 V; V_{IH} = V_{DD} –0.2 V
4. Stop I_{DD} measured with OSC1 = V_{SS}.
5. Wait I_{DD} is affected linearly by the OSC2 capacitance.
6. Input current is measured with output transistor turned off and V_{In} = 0 V.

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12.9 2.7-Volt DC Electrical Characteristics

Characteristic[1]	Symbol	Min	Typ	Max	Unit
Output voltage I_{Load} = 10.0 µA I_{Load} = –10.0 µA	 V_{OL} V_{OH}	 — V_{DD} –0.1	 — —	 0.1 —	 V
Output high voltage (V_{DD} = 2.2 V) (I_{Load} = –0.4 mA) PA0–PA7, PC0–PC5, PD1–PD7, PE0–PE7	V_{OH}	V_{DD} –0.6	—	—	V
Output low voltage (V_{DD} = 2.2 V) (I_{Load} = 0.4 mA) PA0–PA7, PC0–PC5, PD1–PD7, PE0–PE7	V_{OL}	—	—	0.3	V
Input high voltage PA0–PA7, PB0–PB7, PC0–PC7, $\overline{\text{RESET}}$, OSC1, XOSC1	V_{IH}	0.8 x V_{DD}	—	V_{DD}	V
Input low voltage PA0–PA7, PB0–PB7, PC0–PC7, $\overline{\text{RESET}}$, OSC1, XOSC1	V_{IL}	V_{SS}	—	0.2 x V_{DD}	V
Supply current[2], [3], [4], [5] Run (f_{op} = 1.0 MHz) Wait (f_{op} = 1.0 MHz) Stop No clock XOSC = 32.768 kHz, V_{DD} = 2.2 V, T_A= +25 °C	 I_{DD}	 — — — —	 0.7 0.4 1.5 5.0	 8.0 5.0 10.0 —	 mA mA µA µA
Input current[6] (with pullups disabled) PA0–PA7, PB0–PB7, PC0–PC7, $\overline{\text{RESET}}$, OSC1, XOSC1	I_{In}	—	—	± 1.0	µA
Input current[6] (with pullups enabled, V_{DD} = 2.7 V) PA0–PA7 PB0–PB7 PC0–PC7	 I_{In}	 5 5 30	 40 40 150	 110 110 420	 µA µA µA
LCD pin output impedance FP0–FP26 BP0–BP3	 Zo, FP Zo, BP	 — —	 10 5	 20 18	 kΩ kΩ

1. +2.2 ≤ V_{DD} < +3.0 Vdc, V_{SS} = 0 Vdc, $T_L \le T_A \le T_H$, unless otherwise noted. All values shown reflect average measurements. Typical values at midpoint of voltage range, 25 °C only.
2. Run (Operating) I_{DD}, wait I_{DD}; measured using external square wave clock source (f_{OSC} = 2.0 MHz); all inputs 0.2 V from rail (V_{SS} or V_{DD}); no dc loads; less than 50 pF on all outputs; C_L = 20 pF on OSC2
3. Wait, stop I_{DD}; all ports configured as inputs; V_{IL} = 0.2 V; V_{IH} = V_{DD} –0.2 V
4. Stop I_{DD} measured with OSC1 = V_{SS}.
5. Wait I_{DD} is affected linearly by the OSC2 capacitance.
6. Input current is measured with output transistor turned off and V_{In} = 0 V.

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12.10 Control Timing

Characteristic[1]	Symbol	Min	Max	Unit
Frequency of oscillation (OSC) Crystal External clock	f_{osc}	 — dc	 4.2 4.2	MHz
Internal operating frequency[2], crystal or external clock (f_{OSC}/2) V_{DD} = 4.5 V to 5.5 V V_{DD} = 2.2 V to 5.5 V	f_{op}	 — —	 2.1 1.0	MHz
Cycle time (fast OSC selected) V_{DD} = 4.5 V to 5.5 V V_{DD} = 2.2 V to 5.5 V	t_{cyc}	 480 1.0	 — —	 ns µs
$\overline{\text{RESET}}$ pulse width when bus clock active	t_{RL}	1.5	—	t_{cyc}
Timer Resolution Input capture (TCAP) pulse width	 t_{RESL} t_{TH}, t_{TL}	 4.0 284	 — —	 t_{cyc} ns
Interrupt pulse width low (edge-triggered)	t_{ILIH}	284	—	ns
Interrupt pulse period[3]	t_{ILIL}	note 3	—	t_{cyc}
OSC1 pulse width (external clock input)	t_{OH}, t_{OL}	110	—	ns

1. +2.2 ≤ V_{DD} ≤ +5.5 Vdc, V_{SS} = 0 Vdc, $T_L \le T_A \le T_H$, unless otherwise noted.
2. The system clock divider configuration (SYS1–SYS0 bits) should be selected such that the internal operating frequency (f_{OP}) does not exceed value specified in f_{OP} for a given f_{OSC}.
3. The minimum period, t_{ILIL}, should not be less than the number of cycle times it takes to execute the interrupt service routine plus 21 t_{cyc}.

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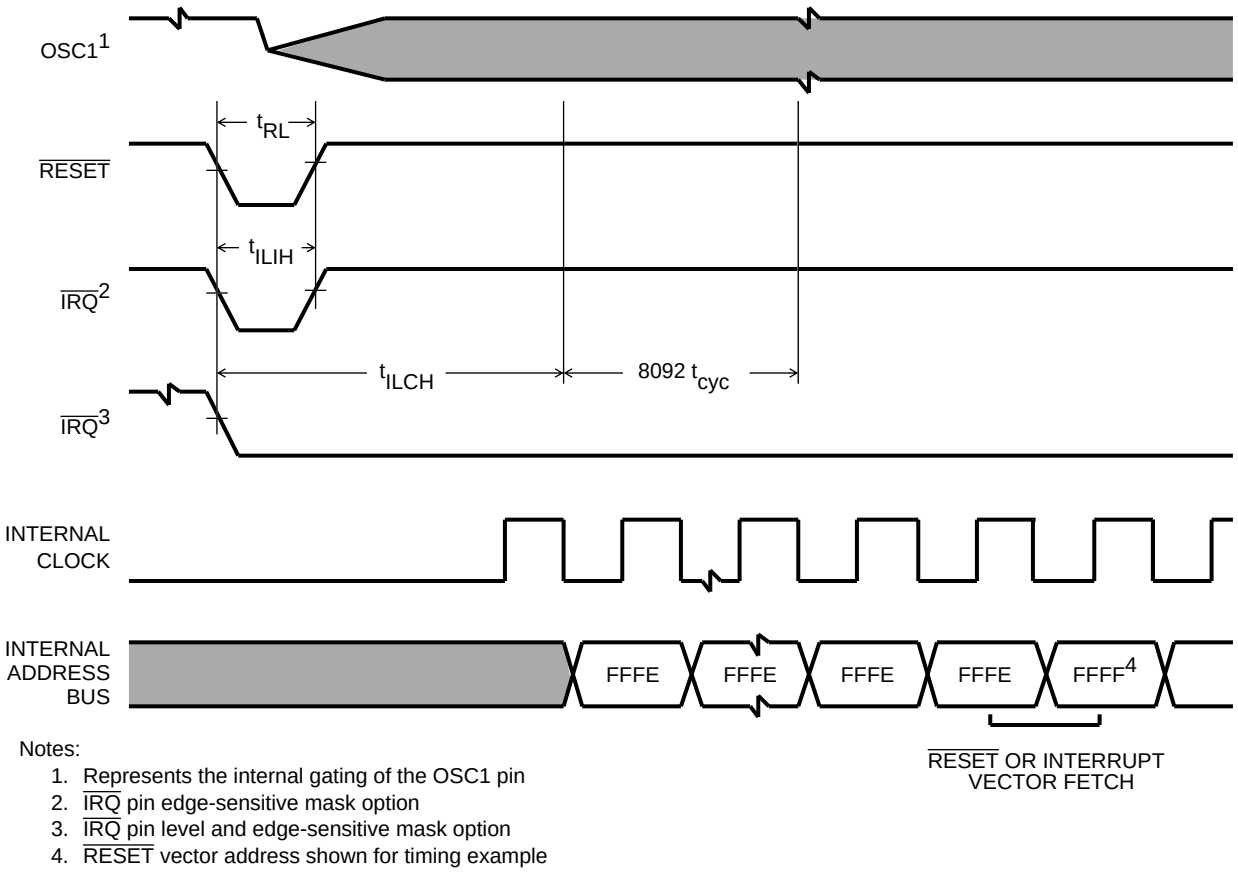
Electrical Specifications



Notes:
1. Represents the internal gating of the OSC1 pin
2. $\overline{IRQ}$ pin edge-sensitive mask option
3. $\overline{IRQ}$ pin level and edge-sensitive mask option
4. $\overline{RESET}$ vector address shown for timing example

Figure 12-1. Stop Recovery Timing Diagram

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Go to: www.freescale.com

Section 13. Mechanical Specifications

13.1 Contents

13.2 Introduction

This section describes the dimensions of the quad flat pack (QFP).

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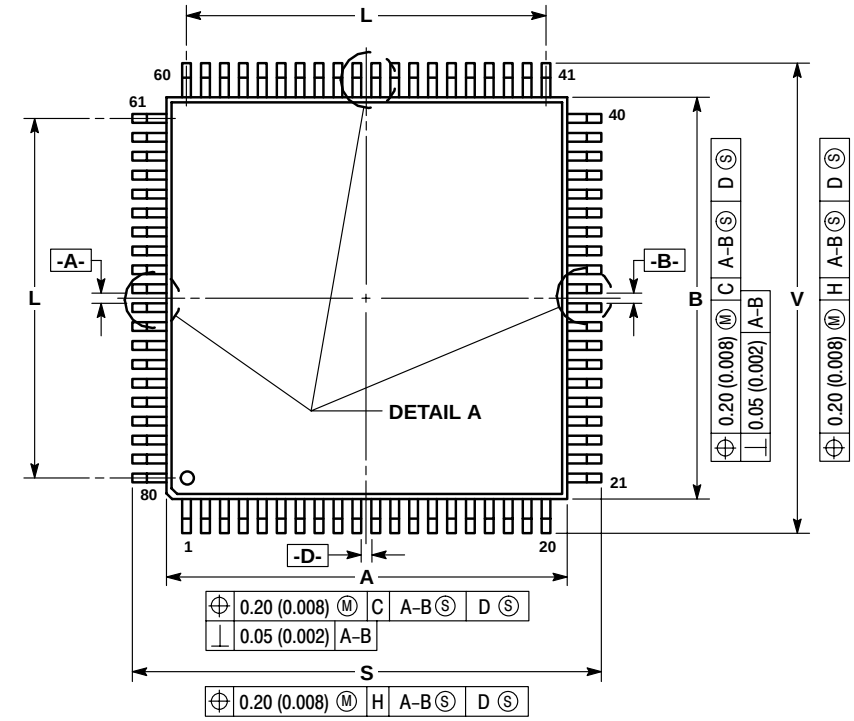
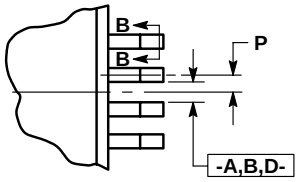
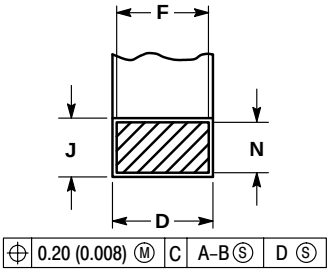
13.3 Quad Flat Pack (QFP) — Case 841B-01

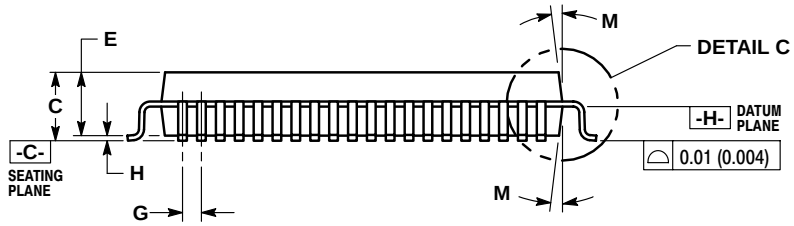


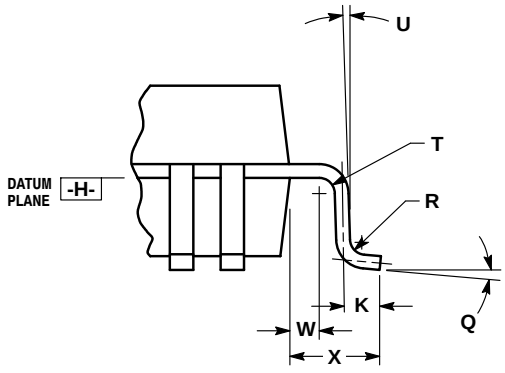


DETAIL A



SECTION B-B





DETAIL C

NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DATUM PLANE -H- IS LOCATED AT BOTTOM OF LEAD AND IS COINCIDENT WITH THE LEAD WHERE THE LEAD EXITS THE PLASTIC BODY AT THE BOTTOM OF THE PARTING LINE.
4. DATUMS -A-, -B- AND -D- TO BE DETERMINED AT DATUM PLANE -H-.
5. DIMENSIONS S AND V TO BE DETERMINED AT SEATING PLANE -C-.
6. DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS 0.25 (0.010) PER SIDE. DIMENSIONS A AND B DO INCLUDE MOLD MISMATCH AND ARE DETERMINED AT DATUM PLANE -H-.
7. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 (0.003) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION. DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OR THE FOOT.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	13.90	14.10	0.547	0.555
B	13.90	14.10	0.547	0.555
C	2.15	2.45	0.084	0.096
D	0.22	0.38	0.009	0.015
E	2.00	2.40	0.079	0.094
F	0.22	0.33	0.009	0.013
G	0.65 BSC		0.026 BSC	
H	—	0.25	—	0.010
J	0.13	0.23	0.005	0.009
K	0.65	0.95	0.026	0.037
L	12.35 BSC		0.486 BSC	
M	5°	10°	5°	10°
N	0.13	0.17	0.005	0.007
P	0.325 BSC		0.013 BSC	
Q	0°	7°	0°	7°
R	0.13	0.30	0.005	0.012
S	16.95	17.45	0.667	0.687
T	0.13	—	0.005	—
U	0°	—	0°	—
V	16.95	17.45	0.667	0.687
W	0.35	0.45	0.014	0.018
X	1.6 REF		0.06 REF	

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Go to: www.freescale.com

Section 14. Ordering Information

14.1 Contents

14.2 Introduction

This section contains instructions for ordering custom-masked ROM MCUs.

14.3 MCU Ordering Forms

To initiate an order for a ROM-based MCU, first obtain the current ordering form for the MCU from a Motorola representative. Submit the following items when ordering MCUs:

- A current MCU ordering form that is **completely filled out** (Contact your Motorola sales office for assistance.)
- A copy of the customer specification if the customer specification deviates from the Motorola specification for the MCU
- Customer's application program on one of the media listed in **14.4 Application Program Media**

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The current MCU ordering form is also available through the Motorola Freeware Bulletin Board Service (BBS). The telephone number is (512) 891-FREE. After making the connection, type bbs in lowercase letters. Then press the return key to start the BBS software.

14.4 Application Program Media

Please deliver the application program to Motorola in one of the following media:

- Macintosh®[1] 3 1/2-inch diskette (double-sided 800 K or double-sided high-density 1.4 M)
- MS-DOS®[2] or PC-DOS™[3] 3 1/2-inch diskette (double-sided 720 K or double-sided high-density 1.44 M)
- MS-DOS® or PC-DOS™ 5 1/4-inch diskette (double-sided double-density 360 K or double-sided high-density 1.2 M)

Use positive logic for data and addresses.

When submitting the application program on a diskette, clearly label the diskette with the following information:

- Customer name
- Customer part number
- Project or product name
- File name of object code
- Date
- Name of operating system that formatted diskette
- Formatted capacity of diskette

On diskettes, the application program must be in Motorola's S-record format (S1 and S9 records), a character-based object file format generated by M6805 cross assemblers and linkers.

1. Macintosh is a registered trademark of Apple Computer, Inc.
2. MS-DOS is a registered trademark of Microsoft Corporation.
3. PC-DOS is a trademark of International Business Machines Corporation.

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Go to: www.freescale.com

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NOTE: *Begin the application program at the first user ROM location. Program addresses must correspond exactly to the available on-chip user ROM addresses as shown in the memory map. Write $00 in all non-user ROM locations or leave all non-user ROM locations blank. Refer to the current MCU ordering form for additional requirements. Motorola may request pattern re-submission if non-user areas contain any non-zero code.*

If the memory map has two user ROM areas with the same addresses, then write the two areas in separate files on the diskette. Label the diskette with both filenames.

In addition to the object code, a file containing the source code can be included. Motorola keeps this code confidential and uses it only to expedite ROM pattern generation in case of any difficulty with the object code. Label the diskette with the filename of the source code.

14.5 ROM Program Verification

The primary use for the on-chip ROM is to hold the customer's application program. The customer develops and debugs the application program and then submits the MCU order along with the application program.

Motorola inputs the customer's application program code into a computer program that generates a listing verify file. The listing verify file represents the memory map of the MCU. The listing verify file contains the user ROM code and may also contain non-user ROM code, such as self-check code. Motorola sends the customer a computer printout of the listing verify file along with a listing verify form.

To aid the customer in checking the listing verify file, Motorola will program the listing verify file into customer-supplied blank preformatted Macintosh or DOS disks. All original pattern media are filed for contractual purposes and are not returned.

Check the listing verify file thoroughly, then complete and sign the listing verify form and return the listing verify form to Motorola. The signed listing verify form constitutes the contractual agreement for the creation of the custom mask.

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Go to: www.freescale.com

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14.6 ROM Verification Units (RVUs)

After receiving the signed listing verify form, Motorola manufactures a custom photographic mask. The mask contains the customer's application program and is used to process silicon wafers. The application program cannot be changed after the manufacture of the mask begins. Motorola then produces 10 MCUs, called RVUs, and sends the RVUs to the customer. RVUs are usually packaged in unmarked ceramic and tested to 5 Vdc at room temperature. RVUs are not tested to environmental extremes because their sole purpose is to demonstrate that the customer's user ROM pattern was properly implemented. The 10 RVUs are free of charge with the minimum order quantity. These units are not to be used for qualification or production. RVUs are not guaranteed by Motorola Quality Assurance.

14.7 MC Order Numbers

Table 14-1 shows the MC order numbers for the available package types.

Table 14-1. MC Order Numbers

Package Type	Operating Temperature Range	MC Order Number
80-pin plastic quad flat pack (QFP)	0 °C to +70 °C	MC68HC05L5FU
	–40 °C to +85 °C	MC68HC05L5CFU

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For More Information On This Product,
Go to: www.freescale.com

Appendix A. MC68HC705L5

A.1 Contents

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A.2 Introduction

The MC68HC705L5 is similar to the MC68HC05L5 with the exception of the EPROM feature. The program ROM on the MC68HC05L5 has been replaced by 8-K electrically programmable read-only memory to allow modification of the program code for emulation. All information pertaining to the MC68HC05L5 in this document applies to the EPROM part with the additions and exceptions explained in this appendix.

The additional features available on the MC68HC705L5 are:

- 8,192 bytes of EPROM
- On-chip bootstrap firmware for programming use
- Self-check mode replaced by bootstrap capability

A.3 Differences between MC68HC05L5 and MC68HC705L5

Table A-1. Differences Between MC68HC05L5 and MC68HC705L5

Item	MC68HC05L5	MC68HC705L5
ROM memory type	Mask ROM	EPROM
Internal test mode	Self-check mode	Bootstrap mode
LCD 1/2 duty 1/2 bias waveform	See **Figure 10-2**	See **Figure A-6**
COP watch dog timer	Software selectable	No COP function
EPROM programming	Not applicable	Through V_{PP} pin and PCR
Mask option	Customer specified	No mask option
OSC, XOSC, and $\overline{\text{RESET}}$ pin resistor option	Available by mask option	Not available

A.4 MCU Structure

Figure A-1 shows the structure of the MC68HC705L5 MCU.

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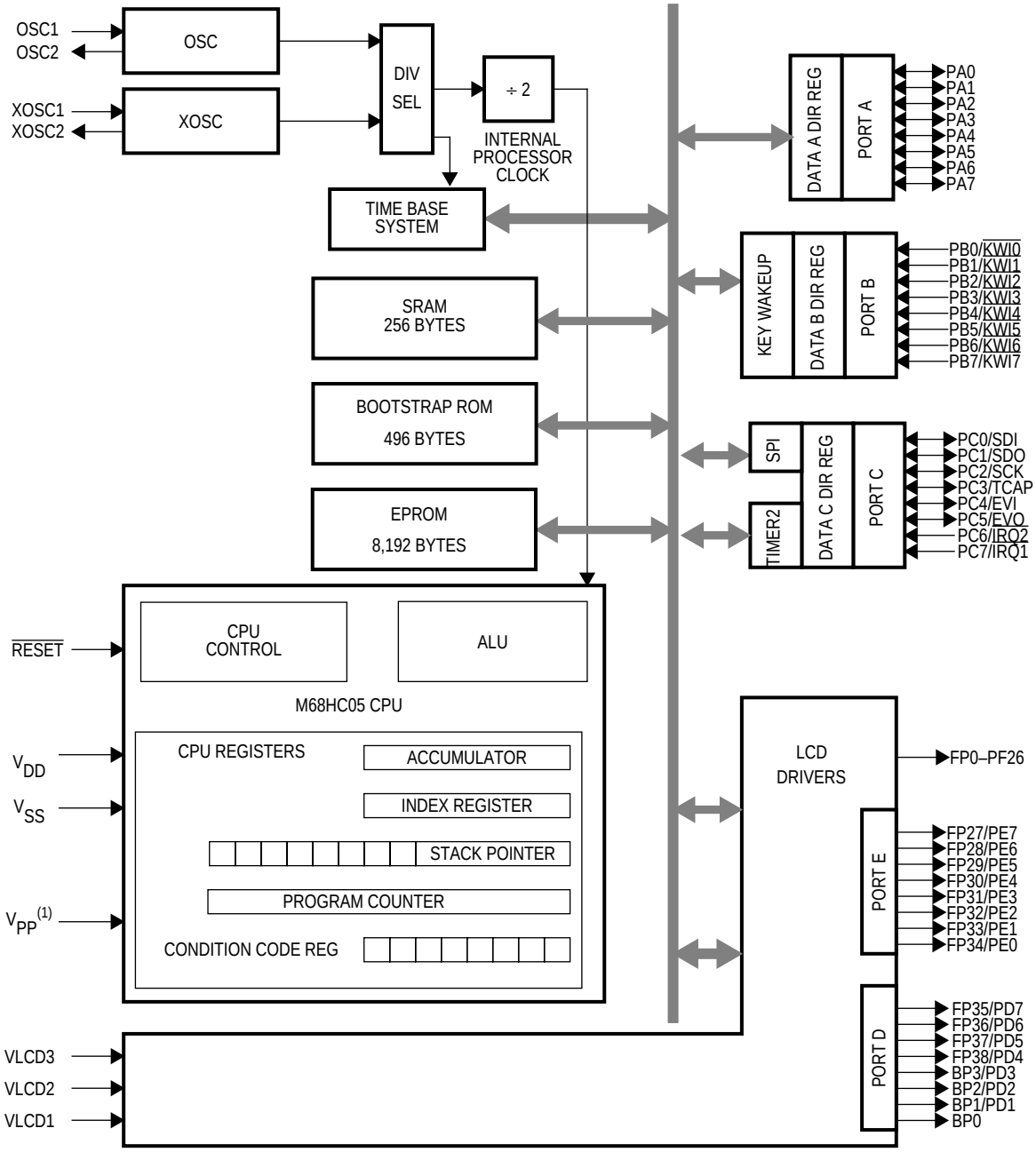

Note 1. The V_{PP} pin should be connected to V_{DD} in single-chip mode.

Figure A-1. Block Diagram

NOTE: *A line over a signal name indicates an active low signal. For example, $\overline{RESET}$ is active low.*

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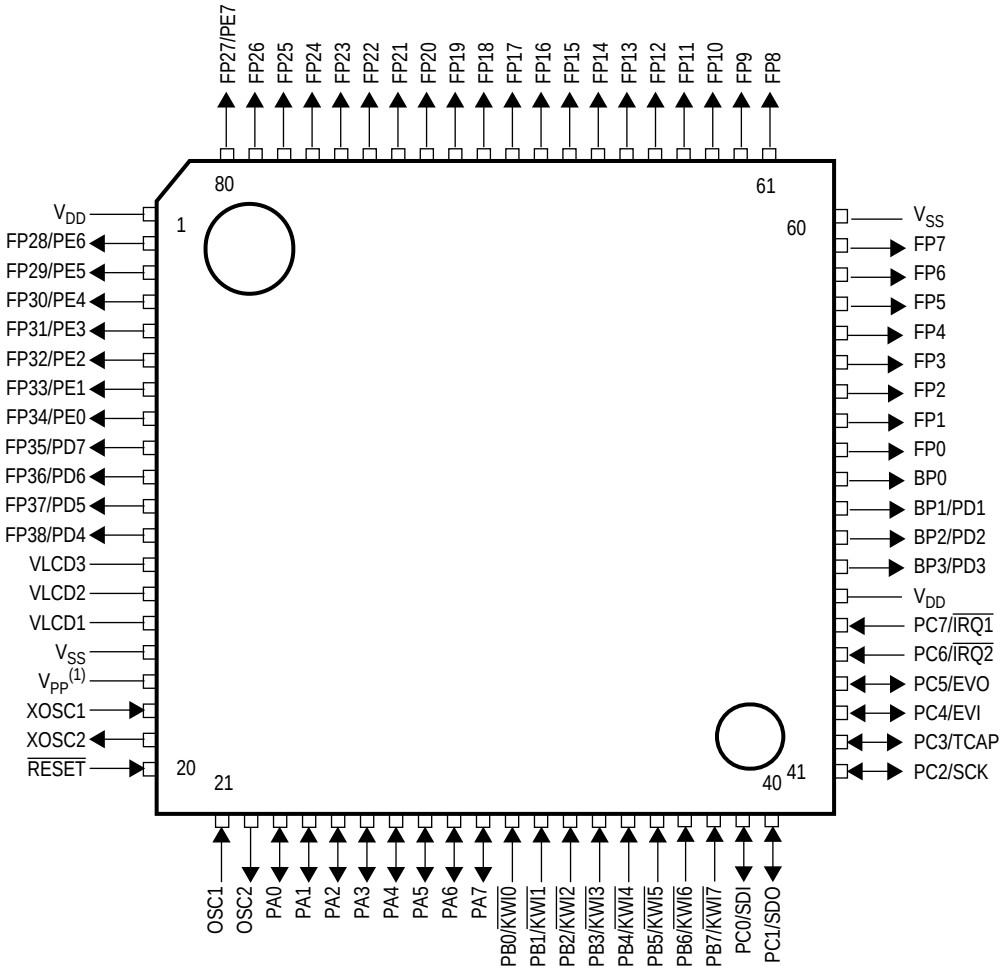
A.5 Mask Options

There are no mask options available for the MC68HC705L5. For this reason, the MOR register at address $000F of option map shown in **Section 2. Memory Map** has no meaning.

A.6 Functional Pin Description

The MC68HC705L5 is available in the 80-pin quad flat pack (QFP). The pin assignment is shown in **Figure A-2.**



Note 1. The V_{PP} pin should be connect to V_{DD} in single-chip mode.

Figure A-2. Pin Assignments for Single-Chip Mode

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Table A-2. Pin Configuration

Pin Number	SCM, Bootstrap	I/O
23	PA0	I/O
24	PA1	I/O
25	PA2	I/O
26	PA3	I/O
27	PA4	I/O
28	PA5	I/O
29	PA6	I/O
30	PA7	I/O
31	PB0/$\overline{\text{KWI0}}$	I
32	PB1/$\overline{\text{KWI1}}$	I
33	PB2/$\overline{\text{KWI2}}$	I
34	PB3/$\overline{\text{KWI3}}$	I
35	PB4/$\overline{\text{KWI4}}$	I
36	PB5/$\overline{\text{KWI5}}$	I
37	PB6/$\overline{\text{KWI6}}$	I
38	PB7/$\overline{\text{KWI7}}$	I
39	PC0/SDI	I/O
40	PC1/SDO	I/O
41	PC2/SCK	I/O
42	PC3/TCAP	I/O
43	PC4/EVI	I/O
44	PC5/EVO	I/O
45	PC6/$\overline{\text{IRQ2}}$	I
46	PC7/$\overline{\text{IRQ1}}$	I
17	V_{PP}[(1)]	I
47	V_{DD}	I
1	V_{DD}	I
60	V_{SS}	O
16	V_{SS}	O
21	OSC1	I
22	OSC2	O
18	XOSC1	I
19	XOSC2	O
15	VLCD1	I
14	VLCD2	I
13	VLCD3	I
48	BP3/PD3	O
49	BP2/PD2	O
50	BP1/PD1	O
51	BP0	O

Pin Number	SCM, Bootstrap	I/O
52	FP0	O
53	FP1	O
54	FP2	O
55	FP3	O
56	FP4	O
57	FP5	O
58	FP6	O
59	FP7	O
61	FP8	O
62	FP9	O
63	FP10	O
64	FP11	O
65	FP12	O
66	FP13	O
67	FP14	O
68	FP15	O
69	FP16	O
70	FP17	O
71	FP18	O
72	FP19	O
73	FP20	O
74	FP21	O
75	FP22	O
76	FP23	O
77	FP24	O
78	FP25	O
79	FP26	O
80	FP27/PE7	O
2	FP28/PE6	O
3	FP29/PE5	O
4	FP30/PE4	O
5	FP31/PE3	O
6	FP32/PE2	O
7	FP33/PE1	O
8	FP34/PE0	O
9	FP35/PD7	O
10	FP36/PD6	O
11	FP37/PD5	O
12	FP38/PD4	O

Note 1. The V_{PP} pin should be connected to V_{DD} in single-chip mode.

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A.7 Programming Voltage (V_{PP})

In single-chip (user) mode, the V_{PP} pin should be tied to V_{DD} level.

A.8 Modes of Operation

The MC68HC705L5 has two operating modes: single-chip mode (SCM) and bootstrap mode.

Single-chip mode, also called user mode, allows maximum use of pins for on-chip peripheral functions.

The bootstrap mode is provided for EPROM programming, dumping EPROM contents, and loading programs into the internal RAM and executing them. This is a very versatile mode because there are essentially no limitations on the special-purpose program that is boot-loaded into the internal RAM.

A.8.1 Mode Entry

Mode entry is done at the rising edge of the $\overline{\text{RESET}}$ pin. Once the device enters one of the modes, the mode cannot be changed by software. Only an external reset can change the mode.

At the rising edge of the $\overline{\text{RESET}}$ pin, the device latches the states of $\overline{\text{IRQ1}}$ and $\overline{\text{IRQ2}}$ and places itself in the specified mode. While the $\overline{\text{RESET}}$ pin is low, all pins are configured as single-chip mode. **Table A-3** shows the states of $\overline{\text{IRQ1}}$ and $\overline{\text{IRQ2}}$ for each mode entry.

High voltage $V_{TST} = 2 \times V_{DD}$ is required to select modes other than single-chip mode.

Table A-3. Mode Select Summary

Modes	$\overline{\text{RESET}}$	PC6/$\overline{\text{IRQ1}}$	PC7/$\overline{\text{IRQ2}}$
Single-chip (user) mode	↑	V_{SS} or V_{DD}	V_{SS} or V_{DD}
Boot-strap mode		V_{TST}	V_{DD}

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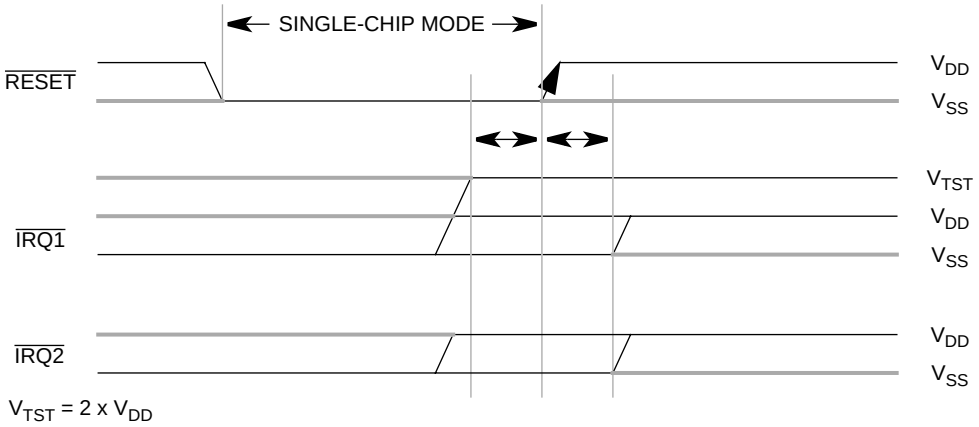

Figure A-3. Mode Entry Diagram

A.8.2 Single-Chip Mode (SCM)

In this mode, all address and data bus activity occurs within the MCU. Thus, no external pins are required for these functions. The single-chip mode allows the maximum number of I/O pins for on-chip peripheral functions, for example, ports A through E, and LCD drivers.

A.8.3 Bootstrap Mode

In this mode, the reset vector is fetched from a 496-byte internal bootstrap ROM at $3E00–$3FEF. The bootstrap ROM contains a small program which loads a program into the internal RAM and then passes control to that program at location $00C0 or executes the EPROM programming sequence and dumps EPROM contents.

Since these modes are not normal user modes, all of the privileged control bits are accessible. This allows the bootstrap mode to be used for self test of the device.

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A.9 Memory Map

The MC68HC705L5 contains a 8,192-byte EPROM, 496 bytes of bootstrap ROM, and 256 bytes of RAM. An additional 16 bytes of EPROM are provided for user vectors at $3FF0–$3FFF.

The MCU's memory map is shown in **Figure A-4**.

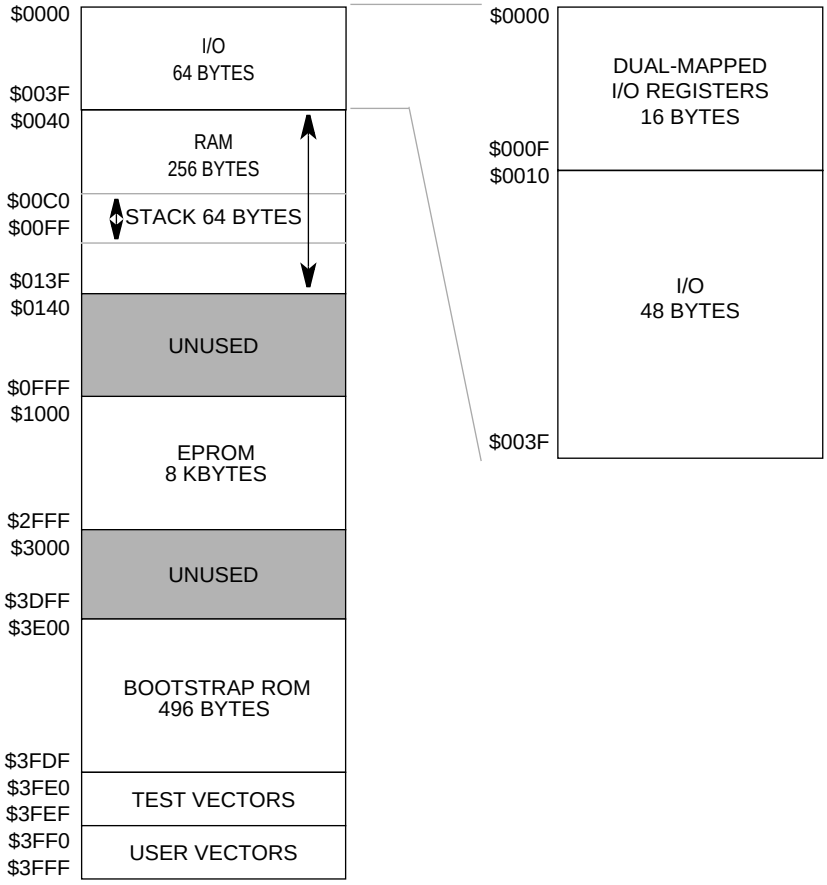

Figure A-4. Memory Map

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A.10 Boot ROM

Boot ROM is 496 bytes of mask ROM positioned at $3E00–$3FEF. This ROM contains bootstrap loader programs and reset/interrupt vectors in the bootstrap mode. The bootstrap loader programs include:

- EPROM programming and verification
- Dumping EPROM contents
- Loading programs into the internal RAM
- Executing programs in the internal RAM

A.11 EPROM

The 8-Kbyte EPROM is positioned at $1000–$2FFF, and the additional 16 bytes of EPROM are located at $3FF0–$3FFF for user vectors. The erased state of EPROM is read as $FF and EPROM power is supplied from the V_{PP} pin and the V_{DD} pin.

The program control register (PCR) is provided for EPROM programming and testing. The functions of EPROM depend on the device mode.

In user mode, ELAT and PGM bits in the PCR are available for user programming, and the remaining test bits become read-only bits. The V_{PP} pin should be tied to 5 volts or programming voltage.

A.11.1 Programming Sequence

To program the MC68HC705L5, execute this sequence:

- Set the ELAT bit
- Write the data to the address to be programmed
- Set the PGM bit
- Delay for an appropriate amount of time
- Clear the PGM bit and the ELAT bit

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Clearing the PGM bit and the ELAT bit may be done on a single CPU write.

NOTE: *It is important to remember that an external programming voltage must be applied to the V_{PP} pin while programming, but it should be equal to V_{DD} during normal operations.*

A.11.2 Program Control Register

A program control register is provided for EPROM programming.

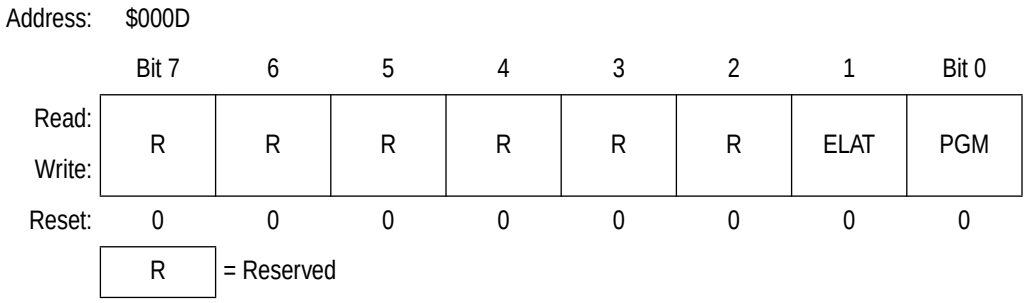

Figure A-5. Program Control Register (PCR)

Bits 7–3 — Reserved

These bits are reserved and read as logic 0 in user mode.

Bit 2 — Reserved

This bit is not used and always reads as logic 0.

ELAT — EPROM LATch control

0 = EPROM address and data bus configured for normal reads

1 = EPROM address and data bus configured for programming (Writes to EPROM cause address and data to be latched.) EPROM is in programming mode and cannot be read if ELAT is logic 1. This bit should not be set when no programming voltage is applied to the V_{PP} pin.

PGM — EPROM ProGraM command

0 = Programming power switched off from EPROM array

1 = Programming power switched on to EPROM array

If ELAT ≠ 1, then PGM = 0.

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A.12 COP Watchdog Timer

The MC68HC705L5 does not have a COP watchdog timer. For this reason, the COPE and COPC bits in timebase control register 2 (address: $0011) has no meaning. These bits are not used and always read as logic 0.

Also or the same reason, COP watchdog timer reset does not occur on the MC68HC705L5.

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A.13 LCD 1/2 Duty and 1/2 Bias Timing Diagram

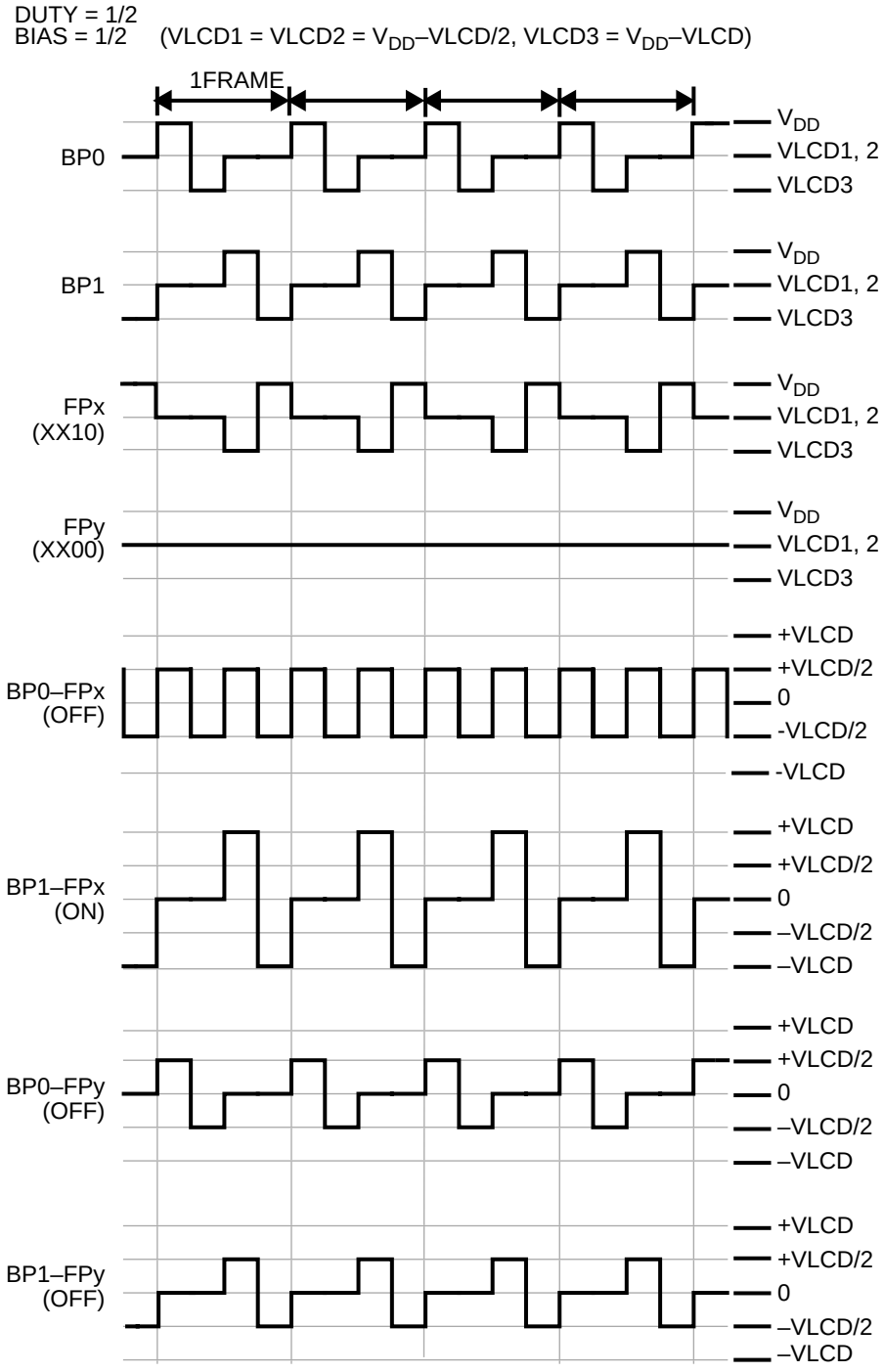

Figure A-6. CD 1/2 Duty and 1/2 Bias Timing Diagram

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A.14 Electrical Specifications

This section contains parametric and timing information for the MC68HC705L5.

A.14.1 Maximum Ratings

Maximum ratings are the extreme limits to which the MCU can be exposed without permanently damaging it.

The MCU contains circuitry to protect the inputs against damage from high static voltages; however, do not apply voltages higher than those shown in this table. Keep V_{In} and V_{OUT} within the range $V_{SS} \le (V_{In}$ or $V_{OUT}) \le V_{DD}$. Connect unused inputs to the appropriate voltage level, either V_{SS} or V_{DD}.

Rating	Symbol	Value	Unit
Supply voltage	V_{DD} V_{LCD1} V_{LCD2} V_{LCD3}	–0.3 to +7.0 V_{SS} –0.3 to V_{DD} +0.3 V_{SS} –0.3 to V_{DD} +0.3 V_{SS} –0.3 to V_{DD} +0.3	V
Input voltage	V_{In}	V_{SS} –0.3 to V_{DD} + 0.3	V
Boot-strap mode $\overline{IRQ1}$ pin only	V_{In}	V_{SS} –0.3 to 2 x V_{DD} + 0.3	V
Output voltage	V_{Out}	V_{SS} –0.3 to V_{DD} + 0.3	V
Current drain per pin excluding V_{DD} and V_{SS}	I	12.5	mA
Operating junction temperature	T_J	+150	°C
Storage temperature range	T_{stg}	–55 to +150	°C

NOTE: *This device is not guaranteed to operate properly at the maximum ratings. Refer to* ***A.15.2 5.0-Volt DC Electrical Characteristics*** *and* ***A.15.3 3.3-Volt DC Electrical Characteristics*** *for guaranteed operating conditions.*

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A.14.2 Operating Temperature Range

Characteristic	Symbol	Value	Unit
Operating temperature range MC68HC705L5 (standard)	T_A	T_L to T_H 0 to +70	°C

A.14.3 Thermal Characteristics

Characteristic	Symbol	Value	Unit
Thermal resistance 80-pin plastic quad flat pack	θ_{JA}	120	°C/W

A.15 Recommended Operating Conditions

Rating[1]	Symbol	Min	Typ	Max	Unit
(f_{OP} = 2.1 MHz)	V_{DD}	4.5	5.0	5.5	V
(f_{OP} = 1.0 MHz)	V_{DD}	3.0	—	5.5	V
Supply voltage	V_{LCD1}	V_{DD} – 1/3 V_{LCD}			V
	V_{LCD2}	V_{DD} – 2/3 V_{LCD}			V
	V_{LCD3}	V_{DD} – 3/3 V_{LCD}			V
Fast clock oscillation frequency	f_{OSC}	—	3.52	4.2	MHz
External capacitance (f_{OSC} = 3.52 MHz)	C1 C2	— —	33 33	— —	pF
Slow clock oscillation frequency	f_{XOSC}	—	32.768	—	MHz
External capacitance (f_{XOSC} = 32.768 kHz)	CX1 CX2	— —	18 22	— —	pF

1. +3.0 ≤ V_{DD} ≤ +5.5 Vdc, V_{SS} = 0 Vdc, $T_L \le T_A \le T_H$, unless otherwise noted

A.15.1 EPROM Programming Voltage

Characteristics[1]	Symbol	Min	Typ	Max	Unit
EPROM programming voltage	V_{PP}	12.0	12.5	13.0	V

1. V_{DD} = 5.0 Vdc, V_{SS} = 0 Vdc, T_A = 25 °C

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A.15.2 5.0-Volt DC Electrical Characteristics

Characteristic[1]	Symbol	Min	Typ	Max	Unit
Output voltage I_{Load} = 10.0 µA I_{Load} = –10.0 µA	 V_{OL} V_{OH}	 — V_{DD} –0.1	 — —	 0.1 —	 V
Output high voltage (V_{DD} = 5.0 V) (I_{Load} = –0.4 mA) PA0–PA7, PC0–PC5, PD1–PD7, PE0–PE7	V_{OH}	V_{DD} –0.8	—	—	V
Output low voltage (V_{DD} = 5.0 V) (I_{Load} = 0.8 mA) PA0–PA7, PC0–PC5, PD1–PD7, PE0–PE7	V_{OL}	—	—	0.4	V
Input high voltage PA0–PA7, PB0–PB7, PC0–PC7, $\overline{\text{RESET}}$, OSC1, XOSC1	V_{IH}	0.8 x V_{DD}	—	V_{DD}	V
Input low voltage PA0–PA7, PB0–PB7, PC0–PC7, $\overline{\text{RESET}}$, OSC1, XOSC1	V_{IL}	V_{SS}	—	0.2 x V_{DD}	V
Supply current[2], [3], [4], [5] Run (f_{OP} = 2.1 MHz) Wait (f_{OP} = 2.1 MHz) Stop No clock XOSC = 32.768 kHz, V_{DD} = 5.0 V, T_A = +25 °C	 I_{DD}	 —	 6.0 3.0 3.0 17.0	 12.0 6.0 10.0 —	 mA mA µA µA
Input current[6] (with pullups disabled) PA0–PA7, PB0–PB7, PC0–PC7, $\overline{\text{RESET}}$, OSC1, XOSC1	I_{In}	—	—	± 1.0	µA
Input current[6] (with pullups enabled, V_{DD} = 5.0 V) PA0–PA7 PB0–PB7 PC0–PC7	 I_{In}	 40 40 160	 150 150 500	 340 340 1000	 µA µA µA
LCD pin output impedance FP0–FP26 BP0–BP3	 Zo, FP Zo, BP	 — —	 10 5	 20 18	 kΩ kΩ

1. +4.5 ≤ V_{DD} ≤ +5.5 Vdc, V_{SS} = 0 Vdc, $T_L \le T_A \le T_H$, unless otherwise noted. All values shown reflect average measurements. Typical values at midpoint of voltage range, 25 °C only.
2. Run (Operating) I_{DD}, wait I_{DD}; measured using external square wave clock source (f_{OSC} = 4.2 MHz); all inputs 0.2 V from rail (V_{SS} or V_{DD}); no dc loads; less than 50 pF on all outputs; C_L = 20 pF on OSC2
3. Wait, stop I_{DD}; all ports configured as inputs; V_{IL} = 0.2 V; V_{IH} = V_{DD} –0.2 V
4. Stop I_{DD} measured with OSC1 = V_{SS}.
5. Wait I_{DD} is affected linearly by the OSC2 capacitance.
6. Input current measured with output transistor turned off and V_{In} = 0 V.

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A.15.3 3.3-Volt DC Electrical Characteristics

Characteristic[1]	Symbol	Min	Typ	Max	Unit
Output voltage I_{Load} = 10.0 µA I_{Load} = –10.0 µA	 V_{OL} V_{OH}	 — V_{DD} –0.1	 — —	 0.1 —	 V
Output high voltage (V_{DD} = 3.5 V) (I_{Load} = –0.4 mA) PA0–PA7, PC0–PC5, PD1–PD7, PE0–PE7	V_{OH}	V_{DD} –0.8	—	—	V
Output low voltage (V_{DD} = 3.5 V) (I_{Load} = 0.8 mA) PA0–PA7, PC0–PC5, PD1–PD7, PE0–PE7	V_{OL}	—	—	0.4	V
Input high voltage PA0–PA7, PB0–PB7, PC0–PC7, $\overline{\text{RESET}}$, OSC1, XOSC1	V_{IH}	0.8 x V_{DD}	—	V_{DD}	V
Input low voltage PA0–PA7, PB0–PB7, PC0–PC7, $\overline{\text{RESET}}$, OSC1, XOSC1	V_{IL}	V_{SS}	—	0.2 x V_{DD}	V
Supply current[2], [3], [4], [5] Run (f_{OP} = 1.0 MHz) Wait (f_{OP} = 1.0 MHz) Stop No clock XOSC = 32.768 kHz, V_{DD} = 3.0 V, T_A= +25 °C	 I_{DD}	 — —	 1.8 0.8 2.0 8.0	 8.0 5.0 10.0 —	 mA mA µA µA
Input current[6] (with pullups disabled) PA0–PA7, PB0–PB7, PC0–PC7, $\overline{\text{RESET}}$, OSC1, XOSC1	I_{In}	—	—	± 1.0	µA
Input current[6] (with pullups enabled, V_{DD} = 3.3 V) PA0–PA7 PB0–PB7 PC0–PC7	 I_{In}	 20 20 60	 80 80 300	 230 230 760	 µA µA µA
LCD pin output impedance FP0–FP26 BP0–BP3	 Zo, FP Zo, BP	 — —	 10 5	 20 18	 kΩ kΩ

1. +3.0 ≤ V_{DD} < +4.5 Vdc, V_{SS} = 0 Vdc, $T_L \le T_A \le T_H$, unless otherwise noted. All values shown reflect average measurements. Typical values at midpoint of voltage range, 25 °C only.
2. Run (Operating) I_{DD}, wait I_{DD}; measured using external square wave clock source (f_{OSC} = 2.0 MHz); all inputs 0.2 V from rail (V_{SS} or V_{DD}); no dc loads; less than 50 pF on all outputs; C_L = 20 pF on OSC2
3. Wait, stop I_{DD}; all ports configured as inputs; V_{IL} = 0.2 V; V_{IH} = V_{DD} –0.2 V
4. Stop I_{DD} measured with OSC1 = V_{SS}.
5. Wait I_{DD} is affected linearly by the OSC2 capacitance.
6. Input current measured with output transistor turned off and V_{In} = 0 V.

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A.15.4 3.3-Volt and 5.0-Volt Control Timing

Characteristic[1]	Symbol	Min	Max	Unit
Frequency of oscillation (OSC) Crystal External Clock	f_{OSC}	— dc	4.2 4.2	MHz
Internal operating frequency[2], crystal or external clock (f_{OSC}/2) V_{DD} = 4.5 V to 5.5 V V_{DD} = 3.0 V to 5.5 V	f_{OP}	— —	2.1 1.0	MHz
Cycle time (fast OSC selected) V_{DD} = 4.5 V to 5.5 V V_{DD} = 3.0 V to 5.5 V	t_{cyc}	480 1.0	— —	ns µs
$\overline{\text{RESET}}$ pulse width (when bus clock active)	t_{RL}	1.5	—	t_{cyc}
Timer Resolution Input capture (TCAP) pulse width	 t_{RESL} t_{TH}, t_{TL}	 4.0 284	 — —	 t_{cyc} ns
Interrupt pulse width low (edge-triggered)	t_{ILIH}	284	—	ns
Interrupt pulse period[3]	t_{ILIL}	see note	—	t_{cyc}
OSC1 pulse width (external clock input)	t_{OH}, t_{OL}	110	—	ns

1. $+3.0 \le V_{DD} \le +5.5$ Vdc, V_{SS} = 0 Vdc, $T_L \le T_A \le T_H$, unless otherwise noted.
2. The system clock divider configuration (SYS1–SYS0 bits) should be selected such that the internal operating frequency (f_{OP}) does not exceed value specified in f_{OP} for a given f_{OSC}.
3. The minimum period, t_{ILIL}, should not be less than the number of cycle times it takes to execute the interrupt service routine plus 21 t_{cyc}.

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A.16 MC Order Number

Table A-4 shows the MC order number for the available package type.

Table A-4. MC Order Number

Package Type	Operating Temperature Range	MC Order Number
80-pin plastic quad flat pack (QFP)	0 °C to +70 °C	MC68HC705L5FU

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