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PRODUCT INFORMATION

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MC68340
MC68340V

Product Brief

Integrated Processor With **DMA**

The MC68340 is a high-performance 32-bit integrated processor with direct memory access (DMA), combining an enhanced M68000-compatible processor, 32-bit DMA, and other peripheral subsystems on a single integrated circuit. The MC68340 CPU32 delivers 32-bit CISC processor performance from a lower cost 16-bit memory system. The combination of peripherals offered in the MC68340 can be found in a diverse range of microprocessor-based systems, including embedded control and general computing. Systems requiring very high-speed block transfers of data can especially benefit from the MC68340's DMA.

The MC68340's high level of functional integration results in significant reductions in component count, power consumption, board space, and cost while yielding much higher system reliability and shorter design time. The 3.3-V MC68340V is particularly attractive to applications requiring a very tight power budget. Complete code compatibility with the MC68000 affords the designer access to a broad base of established real-time kernels, operating systems, languages, applications, and development tools—many oriented towards embedded control. Figure 1 shows a block diagram of the MC68340.

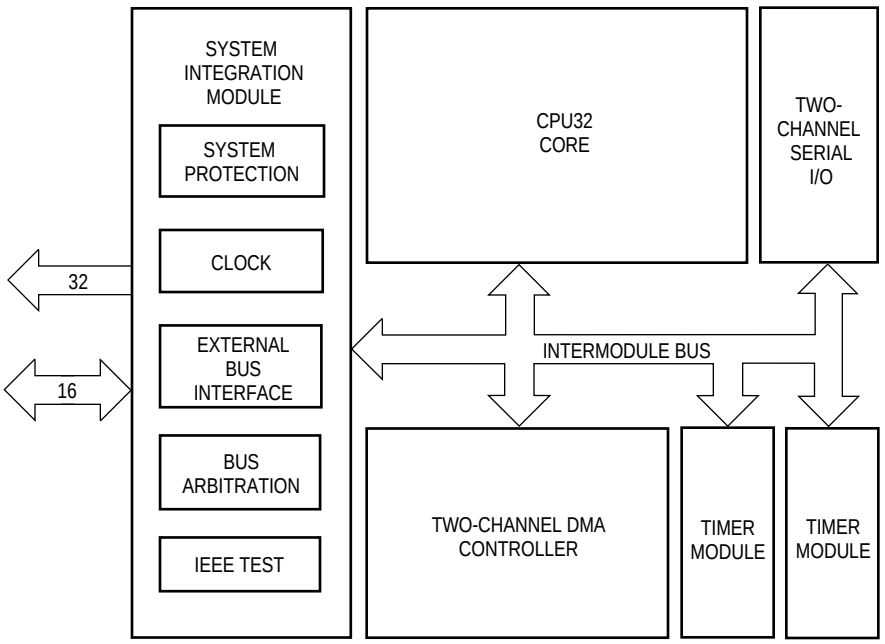

Figure 1. MC68340 Simplified Block Diagram

The primary features of the MC68340 are as follows:

- High Functional Integration on a Single Piece of Silicon
- CPU32—MC68020-Derived 32-Bit Central Processor Unit
  - — Upward Object-Code Compatible with MC68000 and MC68010
  - — Additional 32-Bit MC68020 Instructions and Addressing Modes
  - — Unique Embedded Control Instructions
  - — Fast Two-Clock Register Instructions—10,045 Dhrystones/Second
- Two-Channel Low-Latency DMA Controller for High-Speed Memory Transfers
  - — Single- or Dual-Address Transfers
  - — 32-Bit Addresses and Counters
  - — 8-, 16-, and 32-Bit Data Transfers
  - — 50 Mbyte/Sec Sustained Transfers (12.5 Mbyte/Sec Memory-to-Memory)
- Two-Channel Universal Synchronous/Asynchronous Receiver/Transmitter (USART)
  - — Baud Rate Generators
  - — Modem Control
  - — MC68681/MC2681 Compatible
  - — 9.8 Mbits/Sec Maximum Transfer Rate
- Two Independent Counter/Timers
  - — 16-Bit Counter
  - — Up to 8-Bit Prescaler
  - — Multimode Operation
  - — 80-ns Resolution
- System Integration Module Incorporates Many Functions Typically Relegated to External PALs, TTL, and ASIC, such as:
  - — System Configuration
  - — System Protection
  - — Chip Select and Wait State Generation
  - — Clock Generation
  - — Dynamic Bus Sizing
  - — Up to 16 Discrete I/O Lines
  - — External Bus Interface
  - — Periodic Interrupt Timer
  - — Interrupt Response
  - — Bus Arbitration
  - — IEEE 1149.1 Boundary Scan (JTAG)
  - — Power-On Reset
- 32 Address Lines, 16 Data Lines
- Power Consumption Control
  - — Static HCMOS Technology Reduces Power in Normal Operation
  - — Low Voltage Operation at 3.3 V ±0.3 V (MC68340V only)
  - — Programmable Clock Generator Throttles Frequency
  - — Unused Peripherals Can Be Turned Off
  - — LPSTOP Provides an Idle State for Lowest Standby Current
- 0–16.78 MHz or 0–25.16 MHz Operation
- 144-Pin Ceramic Quad Flat Pack (CQFP) or 145-Pin Plastic Pin Grid Array (PGA)

As a low voltage part, the MC68340V can operate with a 3.3-V power supply. MC68340 is used throughout this document to refer to both the low voltage and standard 5-V parts since both are functionally equivalent.

M68300 FAMILY

The MC68340 is one of a series of components in Motorola's M68300 Family. Other members of the family include the MC68302, MC68330, MC68331, MC68332, and MC68F333.

ORGANIZATION

The M68300 family of integrated processors and controllers is built on an M68000 core processor, an on-chip bus, and a selection of intelligent peripherals appropriate for a set of applications. The CPU32 is a powerful central processor with nearly the performance of the MC68020. A system integration module incorporates the external bus interface and many of the smaller circuits that typically surround a microprocessor for address decoding, wait-state insertion, interrupt prioritization, clock generation, arbitration, watchdog timing, and power-on reset timing.

Each member of the M68300 family is distinguished by its selection of peripherals. Peripherals are chosen to address specific applications but are often useful in a wide variety of applications. The peripherals may be highly sophisticated timing or protocol engines that have their own processors, or they may be more traditional peripheral functions, such as UARTs and timers. Since each major function is designed in a standalone module, each module might be found in many different M68300 family parts. Driver software written for a module on one M68300 part can be used to run the same module that appears on another part.

ADVANTAGES

By incorporating so many major features into a single M68300 family chip, a system designer can realize significant savings in design time, power consumption, cost, board space, pin count, and programming. The equivalent functionality can easily require 20 separate components. Each component might have 16–64 pins, totaling over 350 connections. Most of these connections require interconnects or are duplications. Each connection is a candidate for a bad solder joint or misrouted trace. Each component is another part to qualify, purchase, inventory, and maintain. Each component requires a share of the printed circuit board. Each component draws power—often to drive large buffers to get the signal to another chip. The cumulative power consumption of all the components must be available from the power supply. The signals between the CPU and a peripheral might not be compatible nor run from the same clock, requiring time delays or other special design considerations.

In a M68300 family component, the major functions and glue logic are all properly connected internally, timed with the same clock, fully tested, and uniformly documented. Power consumption stays well under a watt, and a special standby mode drops current well under a milliamp during idle periods. Only essential signals are brought out to pins. The primary package is the surface-mount quad flat pack for the smallest possible footprint; pin grid arrays are also available.

MC68340 SIGNALS

Figure 2 shows the components and signals.

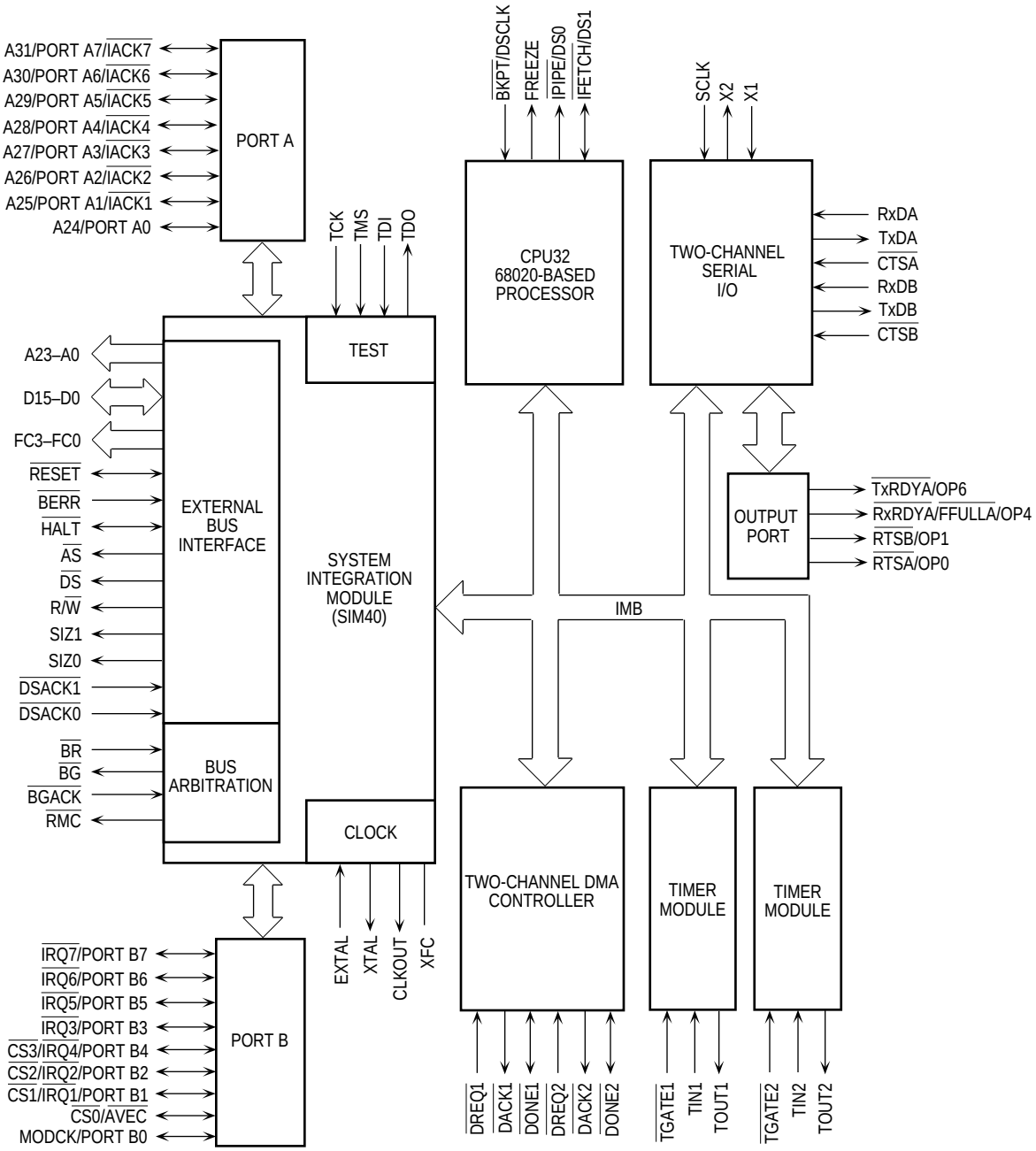

Figure 2. MC68340 Detailed Block Diagram

CENTRAL PROCESSOR UNIT

The CPU32 is a powerful central processor that supervises system functions, makes decisions, manipulates data, and directs I/O. A special debugging mode simplifies processor emulation during system debug.

CPU32

The CPU32 is an M68000 family processor specially designed for use as a 32-bit core processor and for operation over the intermodule bus (IMB). Designers used the MC68020 as a model and included advances of the later M68000 family processors, resulting in an instruction execution performance of 4 MIPS (VAX-equivalent) at 25.16 MHz.

The powerful and flexible M68000 architecture is the basis of the CPU32. MC68000 (including the MC68HC000 and the MC68EC000) and MC68010 user programs will run unmodified on the CPU32. The programmer can use any of the eight 32-bit data registers for fast manipulation of data and any of the eight 32-bit address registers for indexing data in memory. The CPU32 can operate on data types of single bits, binary-coded decimal (BCD) digits, and 8, 16, and 32 bits. Peripherals and data in memory can reside anywhere in the 4-Gbyte linear address space. A supervisor operating mode protects system-level resources from the more restricted user mode, allowing a true virtual environment to be developed.

Flexible instructions for data movement, arithmetic functions, logical operations, shifts and rotates, bit set and clear, conditional and unconditional program branches, and overall system control are supported, including a fast 32 $\times$ 32 multiply and 32-bit conditional branches. Instructions, such as table lookup and interpolate and low power stop, support specific requirements of embedded control applications. Many addressing modes complement these instructions, including predecrement and postincrement, which allow simple stack and queue maintenance and scaled indexed for efficient table accesses. Data types and addressing modes are supported orthogonally by all data operations and with all appropriate addressing modes. Position-independent code is easily written.

The CPU32 is specially optimized to run with the MC68340's 16-bit data bus. Most instructions execute in one-half the number of clocks compared to the original MC68000, yielding an overall 1.6 times the performance of the same-speed MC68000 and measuring 10,045 Dhrystones/sec @ 25.16 MHz (6,742 Dhrystones/sec @ 16.78 MHz).

Like all M68000 family processors, the CPU32 recognizes interrupts of seven different priority levels and allows the peripheral to vector the processor to the desired service routine. Internal trap exceptions ensure proper instruction execution with good addresses and data, allow operating system intervention in special situations, and permit instruction tracing. Hardware signals can either terminate or rerun bad memory accesses before instructions process data incorrectly.

The CPU32 offers the programmer full 32-bit data processing performance with complete M68000 compatibility, yet with more compact code than is available with RISC processors. The CPU32 is identical in all CPU32-based M68300 family products.

BACKGROUND DEBUG MODE

A special operating mode is available in the CPU32 in which normal instruction execution is suspended while special on-chip microcode performs the functions of a debugger. Commands are received over a dedicated, high-speed, full-duplex serial interface. Commands allow the manual reading or writing of CPU32 registers, reading or writing of external memory locations, and diversion to user-specified patch code. This background debug mode permits a much simpler emulation environment while leaving the processor chip in the target system, running its own debugging operations.

ON-CHIP PERIPHERALS

To improve total system throughput and reduce part count, board size, and cost of system implementation, the M68300 family integrates on-chip, intelligent peripheral modules and typical glue logic. These functions on the MC68340 include the SIM40, a DMA controller, a serial module, and two timers.

The processor communicates with these modules over the on-chip intermodule bus (IMB). This backbone of the chip is similar to traditional external buses with address, data, clock, interrupt, arbitration, and handshake signals. Because bus masters (like the CPU32 and DMA), peripherals, and the SIM40 are all on the chip, the IMB ensures that communication between these modules is fully synchronized and that arbitration and interrupts can be handled in parallel with data transfers, greatly improving system performance. Internal accesses across the IMB may be monitored from outside of the chip, if desired.

Each module operates independently. No direct connections between peripheral modules are made inside the chip; however, external connections could, for instance, link a serial output to a DMA control line. Modules and their registers are accessed in the memory map of the CPU32 (and DMA) for easy access by general M68000 instructions and are relocatable. Each module may be assigned its own interrupt level, response vector, and arbitration priority. Since each module is a self-contained design and adheres to the IMB interface specifications, the modules may appear on other M68300 family products, retaining the investment in the software drivers for the module.

SYSTEM INTEGRATION MODULE

The MC68340 SIM40 provides the external bus interface for both the CPU32 and the DMA. It also eliminates much of the glue logic that typically supports the microprocessor and its interface with the peripheral and memory system. The SIM40 provides programmable circuits to perform address decoding and chip selects, wait-state insertion, interrupt handling, clock generation, bus arbitration, watchdog timing, discrete I/O, and power-on reset timing. A boundary scan test capability is also provided.

External Bus Interface

The external bus interface (EBI) handles the transfer of information between the internal CPU32 or DMA controller and memory, peripherals, or other processing elements in the external address space. Based on the MC68030 bus, the external bus provides up to 32 address lines and 16 data lines. Address extensions identify each bus cycle as CPU32 or DMA initiated, supervisor or user privilege level, and instruction or data access. The data bus allows dynamic sizing for 8- or 16-bit bus accesses (plus 32 bits for DMA). Synchronous transfers for the CPU32 or the DMA can be made in as little as two clock cycles. Asynchronous transfers allow the memory system to signal the CPU32 or DMA when the transfer is complete and to note the number of bits in the transfer. An external master can arbitrate for the bus using a three-line handshaking interface.

System Configuration And Protection

The M68000 family of processors is designed with the concept of providing maximum system safeguards. System configuration and various monitors and timers are provided in the MC68340. Power-on reset circuitry is a part of the SIM40. A bus monitor ensures that the system does not lock up when there is no response to a memory access. The bus fault monitor can reset the processor when a catastrophic bus failure occurs. Spurious interrupts are detected and handled appropriately. A software watchdog can pull the processor out of an infinite loop. An interrupt can be sent to the CPU32 with programmable regularity for DRAM refresh, time-of-day clock, task switching, etc.

Clock Synthesizer

The clock synthesizer generates the clock signals used by all internal operations as well as a clock output used by external devices. The clock synthesizer can operate with an inexpensive 32768-Hz watch crystal or an external oscillator for reference, using an internal phase-locked loop and voltage-controlled oscillator. At any time, software can select clock frequencies from 131 kHz to 16.78 MHz or 25.16 MHz, favoring either low power consumption or high performance. Alternately, an external clock can drive the clock signal directly at the operating frequency. With its fully static HCMOS design, it is possible to completely stop the system clock without losing the contents of the internal registers.

Chip Select And Wait State Generation

Four programmable chip selects provide signals to enable external memory and peripheral circuits, providing all handshaking and timing signals with up to 175-ns access times with a 25-MHz system clock (265 ns @ 16.78 MHz). Each chip select signal has an associated base address and an address mask that determine the addressing characteristics of that chip select. Address space and write protection can be selected for each. The block size can be selected from 256 bytes up to 4 Gbytes in increments of 2^n. Accesses can be preselected for either 8- or 16-bit transfers. Fast synchronous termination or up to three wait states can be programmed, whether or not the chip select signals are used. External handshakes can also signal the end of a bus transfer. A system can boot from reset out of 8-bit-wide memory, if desired.

Interrupt Handling

Seven input signals are provided to trigger an external interrupt, one for each of the seven priority levels supported. Seven separate outputs can indicate the priority level of the interrupt being serviced. An input can direct the processor to a default service routine, if desired. Interrupts at each priority level can be preprogrammed to go to the default service routine. For maximum flexibility, interrupts can be vectored to the correct service routine by the interrupting device.

Discrete I/O Pins

When not used for other functions, 16 pins can be programmed as discrete input or output lines. Additionally, in other peripheral modules, pins for otherwise unused functions can often be used for general input/output.

IEEE 1149.1 Test

To aid in system diagnostics, the MC68340 includes dedicated user-accessible test logic that is fully compliant with the IEEE 1149.1 standard for boundary scan testability, often referred to as JTAG (Joint Test Action Group).

DIRECT MEMORY ACCESS MODULE

The most distinguishing MC68340 characteristic is the high-speed 32-bit DMA controller, used to quickly move large blocks of data between internal peripherals, external peripherals, or memory, without processor intervention. The DMA module consists of two, independent, programmable channels. Each channel has separate request, acknowledge, and done signals. Each channel can operate in a single-address (flyby) or a dual-address mode.

In single-address mode, only one (the source or the destination) address is provided, and a peripheral device such as a serial communications controller receives or supplies the data. An external request must start a single-address transfer. In this mode, each channel supports 32 bits of address and 8, 16, or 32 bits of data.

In dual-address mode, two bus transfers occur, one from a source device and the other to a destination device. Dual-address transfers can be started by either an internal or external request. In this mode, each channel supports 32 bits of address and 8 or 16 bits of data (32 bits require external logic). The source and destination port size can be selected independently; when they are different, the data will be packed or unpacked. An 8-bit disk interface can be read twice before the concatenated 16-bit result is passed into memory.

Byte, word, and long-word counts up to 32 bits can be transferred. All addresses and transfer counters are 32 bits. Addresses increment or remain constant, as programmed. The DMA channels support two external request modes, burst transfer and cycle steal. Internal requests can be programmed to occupy 25, 50, 75, or 100 percent of the data bus bandwidth. Interrupts can be programmed to postpone DMA completion.

The DMA module can sustain a transfer rate of 12.5 Mbytes/sec in dual-address mode and nearly 50 Mbytes/sec in single-address mode @ 25.16 MHz (8.4 and 33.3 Mbytes/sec @ 16.78 MHz, respectively). The DMA controller arbitrates with the CPU32 for the bus in parallel with existing bus cycles and is fully synchronized with the CPU32, eliminating all delays normally associated with bus arbitration by allowing DMA bus cycles to butt seamlessly with CPU bus cycles.

SERIAL MODULE

Most digital systems use serial I/O to communicate with host computers, operator terminals, or remote devices. The MC68340 contains a two-channel, full-duplex USART. An on-chip baud rate generator provides standard baud rates up to 76.8k baud independently to each channel's receiver and transmitter. The module is functionally equivalent to the MC68681/MC2681 DUART.

Each communication channel is completely independent. Data formats can be 5, 6, 7, or 8 bits with even, odd, or no parity and stop bits up to 2 in 1/16 increments. Four-byte receive buffers and two-byte transmit buffers minimize CPU service calls. A wide variety of error detection and maskable interrupt capability is provided on each channel. Full-duplex, autoecho loopback, local loopback, and remote loopback modes can be selected. Multidrop applications are supported.

A 3.6864-MHz crystal drives the baud rate generators. Each transmit and receive channel can be programmed for a different baud rate, or an external 1× and 16× clock input can be selected. Full modem support is provided with separate request-to-send (RTS) and clear-to-send (CTS) signals for each channel. One channel also provides service request signals. The two serial ports can sustain rates of 9.8 Mbps with a 25-MHz system clock in 1× mode, 612 kbps in 16× mode (6.5 Mbps and 410 kbps @ 16.78 MHz).

TIMER MODULES

Timers and counters are used in a system to monitor elapsed time, generate waveforms, measure signals, keep time-of-day clocks, initiate DRAM refresh cycles, count events, and provide “time slices” to ensure that no task dominates the activity of the processor. A counter that counts clock pulses makes a timer, which is most useful when it causes certain actions to occur in response to reaching desired counts.

The MC68340 has two, identical, versatile, on-chip counter/timers as well as a simple timer in the SIM40. These general-purpose counter/timers can be used for precisely timed events without the errors to which software-based counters and timers are susceptible—e.g., errors caused by dynamic memory refreshing, DMA cycle steals, and interrupt servicing. The programmable timer operating modes are input capture, output compare, square-wave generation, variable duty-cycle square-wave generation, variable-width single-shot pulse generation, event counting, period measurement, and pulse-width measurement.

Each timer consists of a 16-bit countdown counter with an 8-bit countdown prescaler for a composite 24-bit resolution. The two timers can be externally cascaded for a maximum count width of 48 bits. The

counter/timer can be clocked by the internal system clock generated by the SIM40 (÷2) or by an external clock input. Either the processor or external stimuli can trigger the starting and stopping of the counter. When a counter reaches a predetermined value, either an external output signal can be driven, or an interrupt can be made to the CPU32. The finest resolution of the timer is 80 ns with a 25-MHz system clock (125 ns @ 16.78 MHz).

POWER CONSUMPTION MANAGEMENT

The MC68340 is very power efficient due to its advanced 0.8-µ HCMOS process technology and its static logic design. The resulting power consumption is typically 500 mW in full operation @ 16.78 MHz (750 mW @ 25 MHz)—far less than the comparable discrete component implementation the MC68340 can replace. For applications employing reduced voltage operation, selection of the MC68340V, which requires only a 3.3-V power supply, reduces current consumption by 40–60% in all modes of operation (as well as reducing noise emissions).

The MC68340 has many additional methods of dynamically controlling power consumption during operation. The frequency of operation can be lowered under software control to reduce current consumption when performance is less critical. Idle internal peripheral modules can be turned off to save power (5–10% each). Running a special low power stop (LPSTOP) instruction shuts down the active circuits in the CPU and peripheral modules, halting instruction execution. Power consumption in this standby mode is reduced to about 300 µW. Processing and power consumption can be resumed by resetting the part or by generating an interrupt which can be done with the SIM40's periodic interrupt timer.

PHYSICAL

The MC68340 is available as 0–16.78 MHz and 0–25.16 MHz, 0°C to +70°C and -40°C to +85°C, and 5.0 V ±5% and 3.3 V ±0.3 supply voltages (reduced frequencies at 3.3 V). Thirty-two power and ground leads minimize ground bounce and ensure proper isolation of different sections of the chip, including the clock oscillator. A 144 pins are used for signals and power. The MC68340 is available in a gull-wing ceramic quad flat pack (CQFP) with 0.65 mm lead spacing or a 15 × 15 plastic pin grid array (PPGA) with 0.1-in pin spacing.

COMPACT DISC-INTERACTIVE

The MC68340 was designed to meet the needs of many markets, including compact disc-interactive (CD-I). CD-I is an emerging standard for a publishing medium that will bring multimedia to a broad general audience—the consumer. CD-I players combine television and stereo systems as output devices, with interactive control using a TV remote-control-like device to provide a multimedia experience selected from software “titles” contained in compressed form on standard compact discs.

The highly integrated MC68340 is ideal as the central processor for CD-I players. It provides the M68000 microprocessor code compatibility and DMA functions required by the *CD-I Green Book* specification as well as many other useful on-chip functions for a very cost-effective solution. The extra demands of full-motion video CD-I systems make the best use of the MC68340 high performance. The MC68340 is CD-I compliant and has been CD-I qualified. With its low voltage operation, the MC68340V is the only practical choice for portable CD-I.

MORE INFORMATION

The following table identifies the packages, supply voltages, temperature range, and operating frequencies available for the MC68340.

MC68340 Package/Frequency Availability

	Frequency/Volts			
Package	**8 MHz/3.3 V**	**16 MHz/3.3 V**	**16 MHz/5 V**	**25 MHz/5 V**
Plastic Pin Grid Array (RP)	✔	✔	✔	✔
Ceramic Quad Flat Pack (FE)	✔	✔	✔	✔
Temperature	0–70 °C/-40–85 °C	0–70 °C	0–70 °C/-40–85 °C	0–70 °C

The documents listed in the following table contain detailed information on the MC68340. These documents may be obtained from the Literature Distribution Centers at the addresses listed at the bottom of this page.

Documentation

Document Number	Document Name
BR1114/D	*M68300 Integrated Processor Family*
MC68340UM/AD	*MC68340 User's Manual*
M68000PM/AD	*M68000 Family Programmer's Reference Manual*
AN1063/D	*DRAM Controller for the MC68340*
AN453	*Software Implementation of SPI on the MC68340*
BR573/D	*M68340 Evaluation System Product Brief*
BR729/D	*The 68K Source*
BR1407/D	*3.3 Volt Logic and Interface Circuits*

Literature Distribution Centers:

USA: Motorola Literature Distribution; P.O. Box 20912; Phoenix, Arizona 85036.
EUROPE: Motorola Ltd.; European Literature Centre; 88 Tanners Drive, Blakelands, Milton Keynes, MK14 5BP, England.
JAPAN: Nipon Motorola Ltd.; 4-32-1, Nishi-Gotanda, Shinagawa-ku, Tokyo 141 Japan.
ASIA-Pacific: Motorola Semiconductors H.K. Ltd.; Silicon Harbour Center, No. 2 Dai King Street, Tai Po Industrail Estate, Tai Po, N.T., Hong Kong.

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