



**THE DATASHEET OF
MAX7310ATE+**





2-Wire-Interfaced 8-Bit I/O Port Expander with Reset

MAX7310

General Description

The MAX7310 provides 8-bit parallel input/output port expansion for SMBus™-compatible and I²C-compatible applications. The MAX7310 consists of an input port register, an output port register, a polarity inversion register, a configuration register, a bus timeout register, and an SMBus/I²C-compatible serial interface. The system master can invert the MAX7310 input data by writing to the active-high polarity inversion register. The system master can enable or disable bus timeout by writing to the bus timeout register.

Any of the eight I/O ports may be configured as input or output. An active-low reset input sets the eight I/Os as inputs. Three address select pins configure one of 56 slave ID addresses.

The MAX7310 is available in 16-pin thin QFN, TSSOP, and QSOP packages and is specified over the -40°C to +125°C automotive temperature range.

Applications

Servers
RAID Systems
Industrial Control
Medical Equipment
Instrumentation, Test Measurement

SMBus is a trademark of Intel Corp.

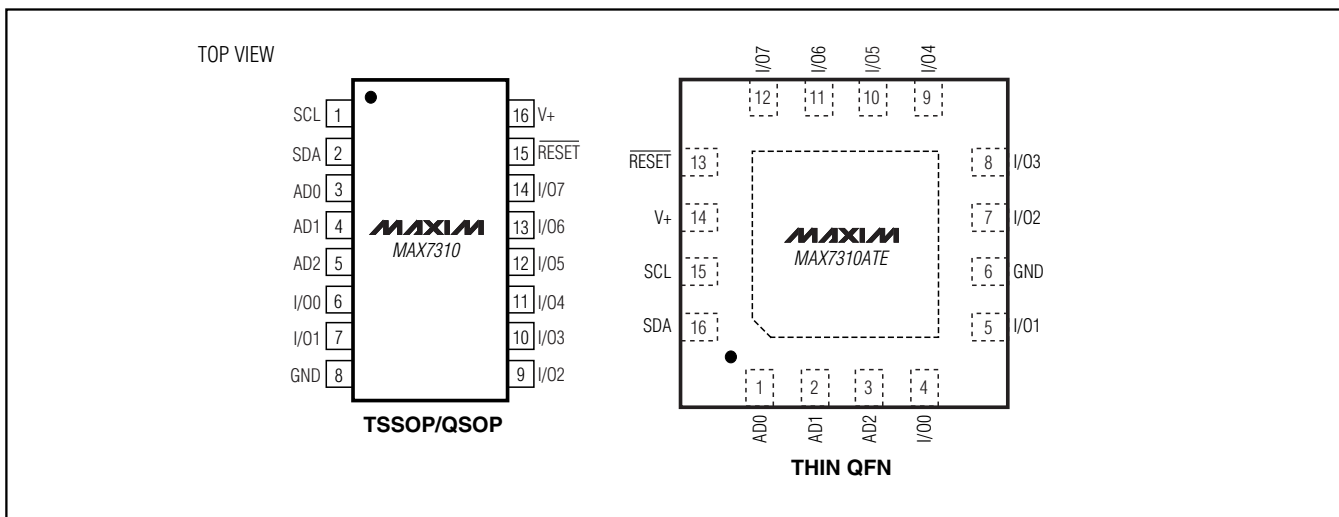
Features

- ◆ 400kHz 2-Wire Interface
- ◆ 2.3V to 5.5V Operation
- ◆ Low Standby Current (1.7µA typ)
- ◆ Bus Timeout for Lock-Up-Free Operation
- ◆ 56 Slave ID Addresses
- ◆ Polarity Inversion
- ◆ Eight I/O Pins that Default to Inputs on Power-Up
- ◆ 5V Tolerant Open-Drain Output on I/O0
- ◆ 4mm x 4mm, 0.8mm Thin QFN Package
- ◆ -40°C to +125°C Operation

Ordering Information

| PART | TEMP RANGE | PIN-PACKAGE | PKG CODE |
|------------|-----------------|-------------|----------|
| MAX7310AUE | -40°C to +125°C | 16 TSSOP | — |
| MAX7310AEE | -40°C to +125°C | 16 QSOP | — |
| MAX7310ATE | -40°C to +125°C | 16 Thin QFN | T1644-4 |

Pin Configurations



2-Wire-Interfaced 8-Bit I/O Port Expander with Reset

ABSOLUTE MAXIMUM RATINGS

| | |
|--------------------------------------|--|
| V+ to GND | -0.3V to +6V |
| I/O1–I/O7 as an Input | (V _{SS} - 0.3V) to (V _{DD} + 0.3V) |
| I/O0 as an Input | (V _{SS} - 0.3V) to +6V |
| SCL, SDA, AD0, AD1, AD2, RESET | (V _{SS} - 0.3V) to +6V |
| DC Current on I/O0 | +400μA |
| DC Current on I/O1 to I/O7 | ±50mA |
| Maximum GND and V+ Current | 180mA |

| | |
|---|-----------------|
| Continuous Power Dissipation (T _A = +70°C) | |
| 16-Pin TSSOP (derate 5.7mW/°C above +70°C) | 457mW |
| 16-Pin QSOP (derate 8.3mW/°C above +70°C) | 667mW |
| 16-Pin Thin QFN (derate 16.9mW/°C above +70°C) ... | 1349mW |
| Operating Temperature Range | -40°C to +125°C |
| Junction Temperature | +150°C |
| Storage Temperature Range | -65°C to +150°C |
| Lead Temperature (soldering, 10s) | +300°C |

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC ELECTRICAL CHARACTERISTICS

(V+ = 2.3V to 5.5V, GND = 0, RESET = V+, T_A = -40°C to +125°C, unless otherwise noted. Typical values are at V+ = 3.3V, T_A = +25°C.)
(Note 1)

| PARAMETER | SYMBOL | CONDITIONS | MIN | TYP | MAX | UNITS |
|-----------------------------------|------------------|--|-----------|-----|-----|-------|
| Supply Voltage | V+ | | 2.3 | | 5.5 | V |
| Supply Current | I+ | All outputs floating, all inputs at V+ or GND, f _{SCL} = 400kHz | V+ = 2.3V | 19 | 30 | μA |
| | | | V+ = 3.3V | 29 | 40 | |
| | | | V+ = 5.5V | 65 | 80 | |
| Standby Current | | All outputs floating, all inputs at V+ or GND, f _{SCL} = 0 | V+ = 2.3V | 1.5 | 3.4 | μA |
| | | | V+ = 3.3V | 1.7 | 3.9 | |
| | | | V+ = 5.5V | 2.1 | 5 | |
| Power-On Reset Voltage | | | | 1.6 | 2.1 | V |
| SCL, SDA | | | | | | |
| Input Voltage Low | V _{IL} | | | | 0.8 | V |
| Input Voltage High | V _{IH} | | 2 | | | V |
| Low-Level Output Voltage | V _{OIL} | I _{SINK} = 6mA | | | 0.4 | V |
| Leakage Current | I _L | | -1 | | +1 | μA |
| Input Capacitance | C _I | | | 10 | | pF |
| I/Os | | | | | | |
| Input Voltage Low | V _{IL} | | | | 0.8 | V |
| Input Voltage High | V _{IH} | | 2 | | | V |
| Input Leakage Current | I _L | All inputs at V+ or GND | -1 | | +1 | μA |
| Low-Level Output Current | I _{OL} | V+ = 2.3V, V _{OL} = 0.5V | 8 | 14 | | mA |
| | | V+ = 3.3V, V _{OL} = 0.5V | 12.5 | 22 | | |
| | | V+ = 5.5V, V _{OL} = 0.5V | 19 | 30 | | |
| High Output Current for I/O1–I/O7 | I _{OH} | V+ = 3.3V, V _{OH} = 2.4V | 6.5 | 11 | | mA |
| | | V+ = 5.5V, V _{OH} = 4.5V | 12.5 | 18 | | |
| AD0, AD1, AD2, AND RESET | | | | | | |
| Input Voltage Low | | | | | 0.8 | V |
| Input Voltage High | | | 2 | | | V |

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DC ELECTRICAL CHARACTERISTICS (continued)

(V+ = 2.3V to 5.5V, GND = 0, $\overline{\text{RESET}} = V+$, T_A = -40°C to +125°C, unless otherwise noted. Typical values are at V+ = 3.3V, T_A = +25°C.) (Note 1)

| PARAMETER | SYMBOL | CONDITIONS | MIN | TYP | MAX | UNITS |
|-------------------|--------|------------|-----|-----|-----|-------|
| Leakage Current | | | -1 | | +1 | μA |
| Input Capacitance | | | | 10 | | pF |

AC ELECTRICAL CHARACTERISTICS

(V+ = 2.3V to 5.5V, GND = 0, $\overline{\text{RESET}} = V+$, T_A = -40°C to +125°C, unless otherwise noted.) (Note 1)

| PARAMETER | SYMBOL | CONDITIONS | MIN | TYP | MAX | UNITS |
|--|----------------------|-------------------|-----|-----|-----|-------|
| SCL Clock Frequency | f _{SCL} | (Note 2) | | | 400 | kHz |
| BUS Timeout | t _{TIMEOUT} | | 30 | | 60 | ms |
| Bus Free Time Between STOP and START Condition | t _{BUF} | Figure 2 | 1.3 | | | μs |
| Hold Time (Repeated) START Condition | t _{HD, STA} | Figure 2 | 0.6 | | | μs |
| Repeated START Condition Setup Time | t _{SU, STA} | Figure 2 | 0.6 | | | μs |
| STOP Condition Setup Time | t _{SU, STO} | Figure 2 | 0.6 | | | μs |
| Data Hold Time | t _{HD, DAT} | Figure 2 (Note 3) | | | 0.9 | μs |
| Data Setup Time | t _{SU, DAT} | Figure 2 | 0.1 | | | μs |
| SCL Low Period | t _{LOW} | Figure 2 | 1.3 | | | μs |
| SCL High Period | t _{HIGH} | Figure 2 | 0.7 | | | μs |
| SCL/SDA Fall Time (Transmitting) | t _F | Figure 2 (Note 4) | | | 250 | ns |
| Pulse Width of Spike Suppressed | t _{SP} | (Note 5) | | 50 | | ns |
| PORT TIMING | | | | | | |
| Output Data Valid | t _{PV} | Figure 9 | | | 1 | μs |
| Input Data Setup Time | t _{PS} | Figure 10 | 29 | | | μs |
| Input Data Hold Time | t _{PH} | Figure 10 | 0 | | | μs |
| RESET | | | | | | |
| Reset Pulse Width | | | 100 | | | ns |

Note 1: All parameters are 100% production tested at T_A = +25°C. Specifications over temperature are guaranteed by design.

Note 2: Minimum SCL clock frequency is limited by the MAX7310 bus timeout feature, which resets the serial bus interface if either SDA or SCL is held low for a 30ms minimum.

Note 3: A master device must internally provide a hold time of at least 300ns for the SDA signal (referred to the V_{IL} of the SCL signal) in order to bridge the undefined region of SCL's falling edge.

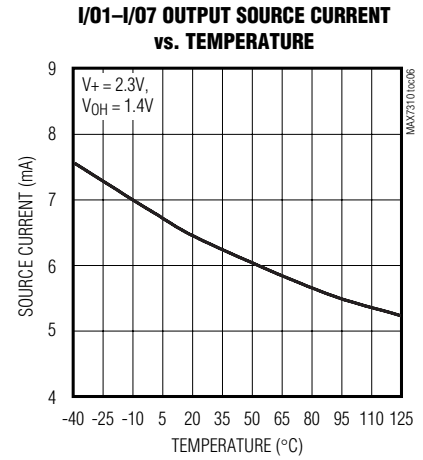
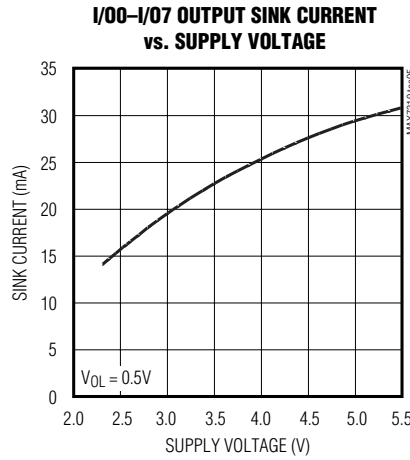
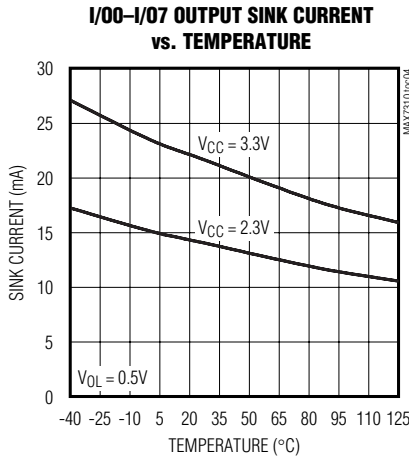
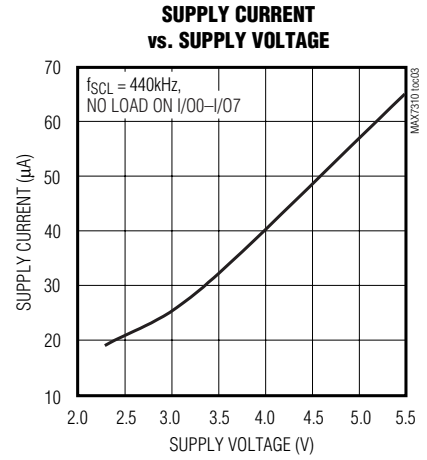
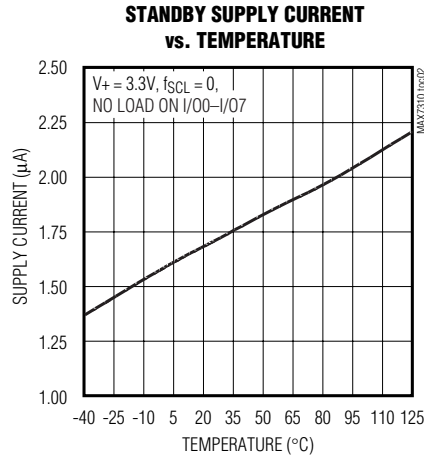
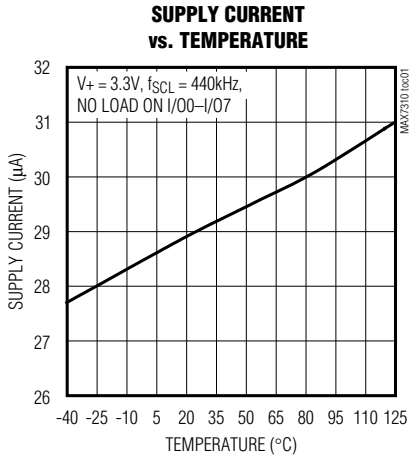
Note 4: t_F measured between 90% to 10% of V+.

Note 5: Input filters on the SDA and SCL inputs suppress noise spikes less than 50ns.

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Typical Operating Characteristics

($T_A = +25^\circ\text{C}$, unless otherwise noted.)



2-Wire-Interfaced 8-Bit I/O Port Expander with Reset

Pin Description

MAX7310

| PIN | | | |
|----------------|-------------|---------------------------|---|
| TSSOP/ QSOP | THIN QFN | NAME | FUNCTION |
| 1 | 15 | SCL | Serial Clock Line |
| 2 | 16 | SDA | Serial Data Line |
| 3 | 1 | AD0 | Address Input 0 |
| 4 | 2 | AD1 | Address Input 1 |
| 5 | 3 | AD2 | Address Input 2 |
| 6 | 4 | I/O0 | Input/Output Port 0 (Open Drain) |
| 7 | 5 | I/O1 | Input/Output Port 1 |
| 8 | 6 | GND | Supply Ground |
| 9–14 | 7–12 | I/O2–I/O7 | Input/Output Port 2—Input/Output Port 7 |
| 15 | 13 | $\overline{\text{RESET}}$ | External Reset (Active Low). Pull $\overline{\text{RESET}}$ low to configure I/O pins as inputs. Set $\overline{\text{RESET}}$ high for normal operation. |
| 16 | 14 | V+ | Supply Voltage. Bypass with a 0.047 μ F capacitor to GND. |
| — | PAD | Exposed pad | Exposed Pad on Package Underside. Connect to GND. |

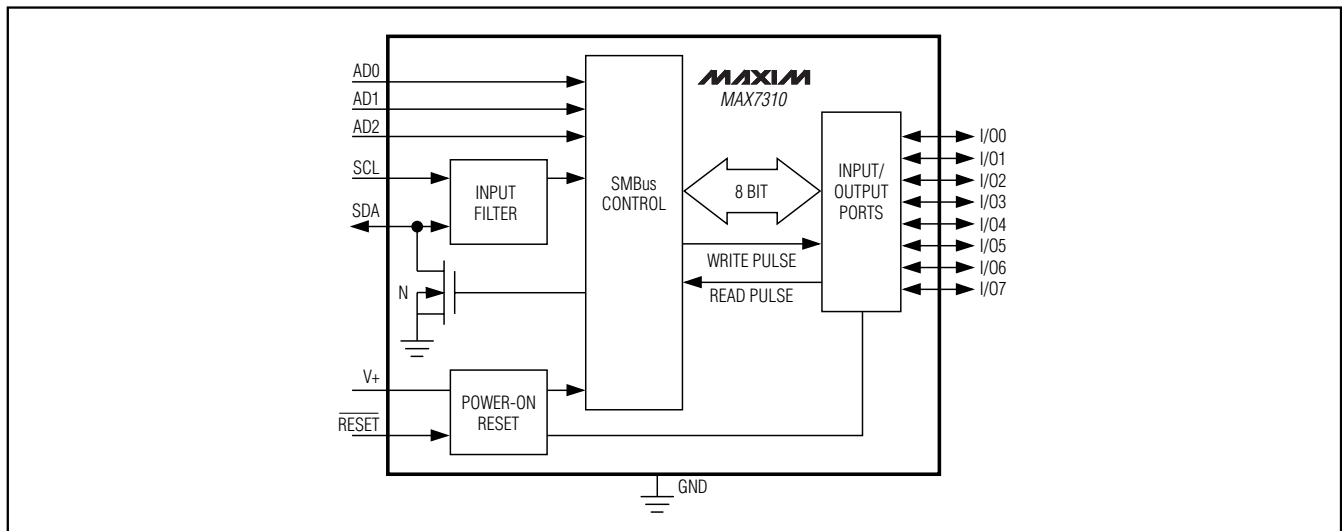


Figure 1. MAX7310 Block Diagram

Detailed Description

The MAX7310 general-purpose input/output (GPIO) peripheral provides up to eight I/O ports, controlled through an I²C-compatible serial interface. The MAX7310 consists of an input port register, an output

port register, a polarity inversion register, a configuration register, and a bus timeout register. An active-low reset input sets the eight I/O lines as inputs. Three slave ID address select pins (AD0, AD1, and AD2) choose one of 56 slave ID addresses (Figure 1).

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Table 1 is the register address table. Tables 2–6 list register 0 through register 4 information.

Serial Interface

Serial Addressing

The MAX7310 operates as a slave that sends and receives data through a 2-wire interface. The interface uses a serial data line (SDA) and a serial clock line (SCL) to achieve bidirectional communication between master(s) and slave(s). A master, typically a microcontroller, initiates all data transfers to and from the MAX7310, and generates the SCL clock that synchronizes the data transfer (Figure 2).

Each transmission consists of a start condition sent by a master, followed by the MAX7310 7-bit slave address plus an R/W bit, a register address byte, one or more data bytes, and finally a stop condition (Figure 3).

Start and Stop Conditions

Both SCL and SDA remain high when the interface is not busy. A master signals the beginning of a transmission with a start (S) condition by transitioning SDA from high to low while SCL is high. When the master has finished communicating with the slave, it issues a stop (P) condition by transitioning SDA from low to high while SCL is high.

SCL is high. The bus is then free for another transmission (Figure 3).

Bit Transfer

One data bit is transferred during each clock pulse. The data on SDA must remain stable while SCL is high (Figure 4).

Acknowledge

The acknowledge bit is a clocked 9th bit, which the recipient uses as a handshake receipt of each byte of data (Figure 5). Thus, each byte transferred effectively requires 9 bits. The master generates the 9th clock pulse, and the recipient pulls down SDA during the acknowledge clock pulse, such that the SDA line is stable low during the high period of the clock pulse. When the master is transmitting to the MAX7310, the MAX7310 generates the acknowledge bit since the MAX7310 is the recipient. When the MAX7310 is transmitting to the master, the master generates the acknowledge bit.

Slave Address

The MAX7310 has a 7-bit-long slave address (Figure 6). The 8th bit following the 7-bit slave address is the R/W bit. Set this bit low for a write command and high for a read command.

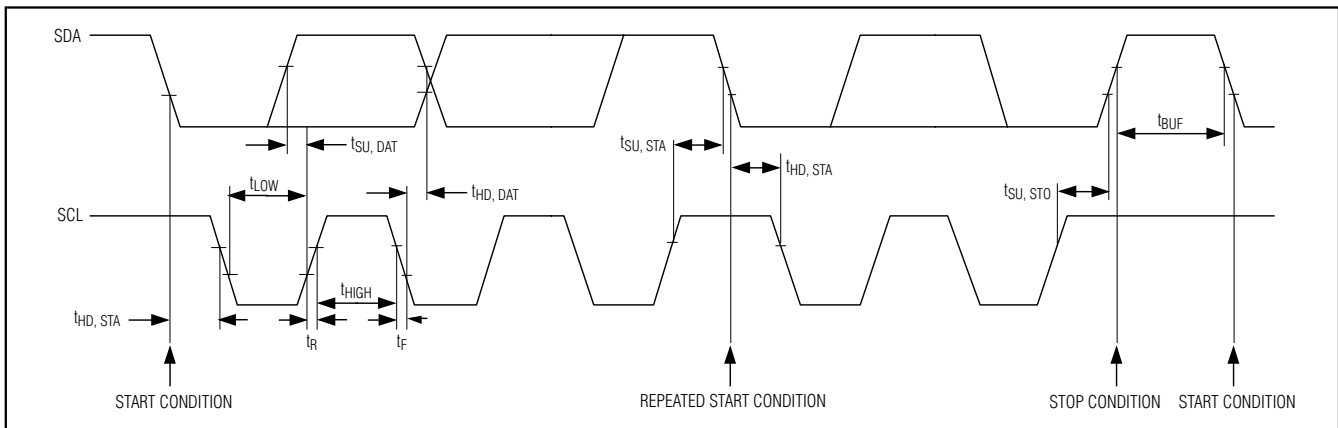


Figure 2. 2-Wire Serial Interface Timing Diagrams

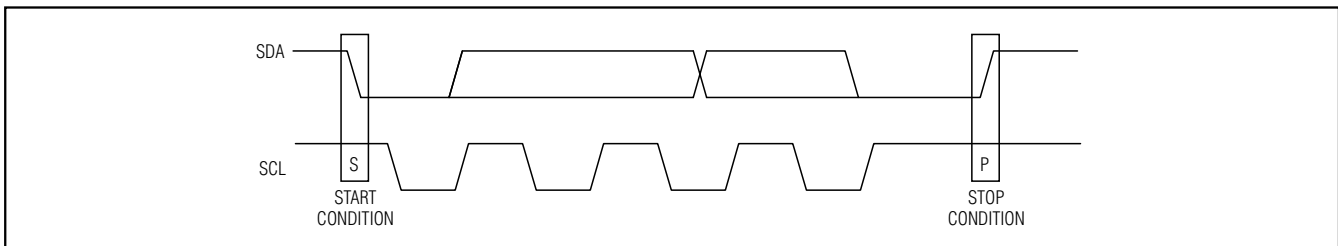


Figure 3. Start and Stop Conditions

2-Wire-Interfaced 8-Bit I/O Port Expander with Reset

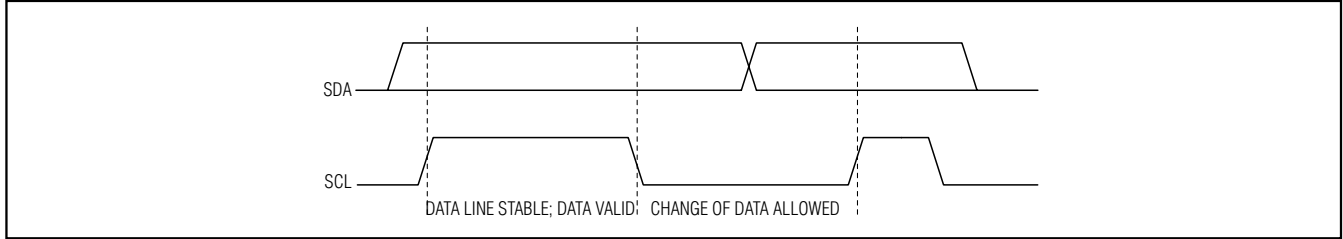


Figure 4. Bit Transfer

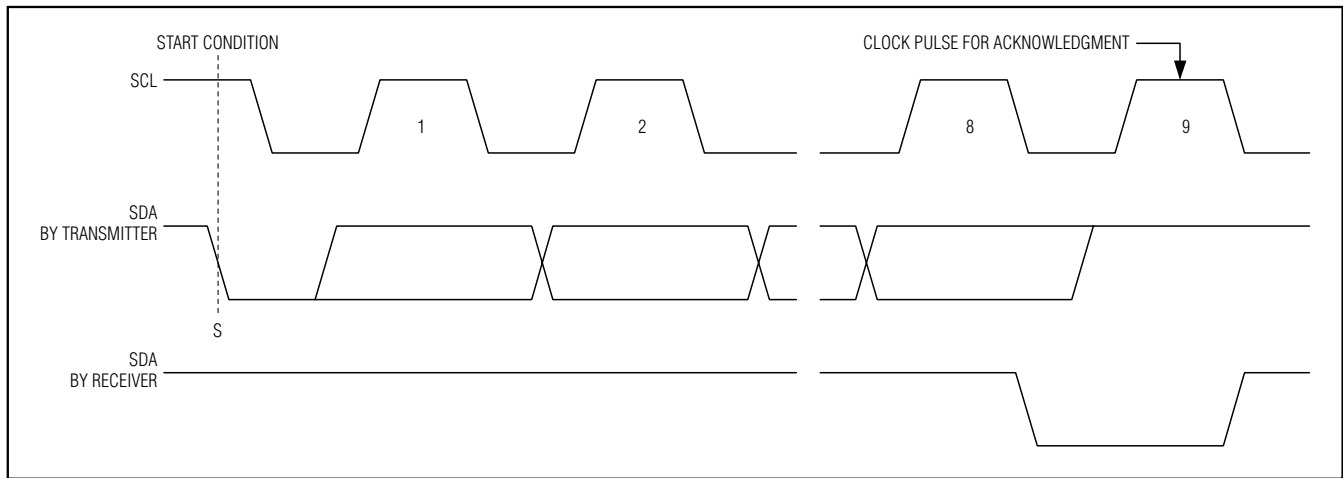


Figure 5. Acknowledge

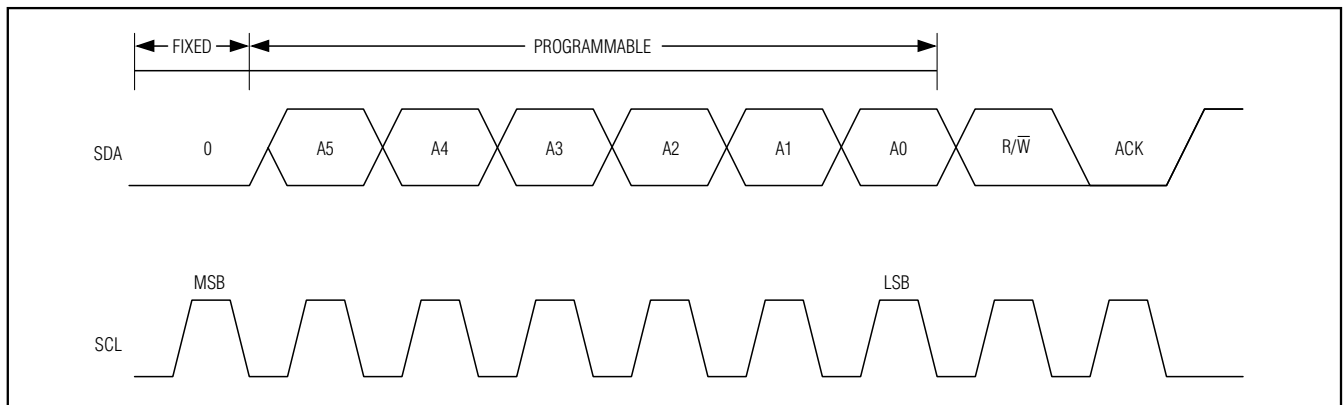


Figure 6. Slave Address

The first bits (MSBs) of the MAX7310 slave address are always zero. Slave address bits AD₂, AD₁, and AD₀ choose 1 of 56 slave ID addresses (Table 7).

Registers

The register address byte is the first byte to follow the address byte during a read/write transmission. The reg-

ister address byte acts as a pointer to determine which register is written or read.

The input port register is a read-only port. It reflects the incoming logic levels of the I/O ports, regardless of whether the pin is defined as an input or an output by the configuration register. Writes to the input port register are ignored.

2-Wire-Interfaced 8-Bit I/O Port Expander with Reset

Table 1. Register Address

| REGISTER ADDRESS (hex) | FUNCTION | PROTOCOL |
|------------------------|-----------------------------|--|
| 0x00 | Input port register | Read byte. |
| 0x01 | Output port register | Read/write byte. |
| 0x02 | Polarity inversion register | Read/write byte. |
| 0x03 | Configuration register | Read/write byte. |
| 0x04 | Timeout register | Read/write byte. |
| 0xFF | Reserved register | Factory reserved. Do not write to this register. |

Table 2. Register 0—Input Port Register

| BIT | I7 | I6 | I5 | I4 | I3 | I2 | I1 | I0 |
|-----|----|----|----|----|----|----|----|----|
| | | | | | | | | |

The output port register sets the outgoing logic levels of the I/O ports, defined as outputs by the configuration register. Reads from the output port register reflect the value that is in the flip-flop controlling the output selection, not the actual I/O value, which may differ if the output is overloaded.

Table 3. Register 1—Output Port Register

| BIT | O7 | O6 | O5 | O4 | O3 | O2 | O1 | O0 |
|---------|----|----|----|----|----|----|----|----|
| Default | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

Table 4. Register 2—Polarity Inversion Register

| BIT | I/O7 | I/O6 | I/O5 | I/O4 | I/O3 | I/O2 | I/O1 | I/O0 |
|---------|------|------|------|------|------|------|------|------|
| Default | 1 | 1 | 1 | 1 | 0 | 0 | 0 | 0 |

Table 5. Register 3—Configuration Register

| BIT | I/O7 | I/O6 | I/O5 | I/O4 | I/O3 | I/O2 | I/O1 | I/O0 |
|---------|------|------|------|------|------|------|------|------|
| Default | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |

Table 6. Register 4—Timeout Register

| BIT | T7 | T6 | T5 | T4 | T3 | T2 | T1 | T0 |
|---------|----|----|----|----|----|----|----|----|
| Default | x | x | x | x | x | x | x | 1 |

The polarity inversion register enables polarity inversion of ports defined as inputs by the configuration register. Set the bit in the polarity inversion register (write with a 1) to invert the corresponding port pin's polarity. Clear the bit in the polarity inversion register (write with a zero) to retain the corresponding port pin's original polarity.

The configuration register configures the directions of the ports. Set the bit in the configuration register to enable the corresponding port pin as an input with a high-impedance output driver. Clear the bit in the configuration register to enable the corresponding port pin as an output.

Set bit T0 to enable the bus timeout function and low to disable the bus timeout function. Enabling the timeout feature resets the serial bus interface when SCL stops either high or low during a read or write access to the MAX7310. If either SCL or SDA is low for more than 30ms min and 60ms max after the start of a valid serial transfer, the interface resets itself. Resetting the serial bus interface sets up SDA as an input. The MAX7310 then waits for another start condition.

Standby

The MAX7310 goes into standby when all pins are set to V+ or GND. Standby supply current is typically 1.7µA.

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Table 7. MAX7310 Address Map

| AD2 | AD1 | AD0 | A6 | A5 | A4 | A3 | A2 | A1 | A0 |
|-----|-----|-----|----|----|----|----|----|----|----|
| GND | SCL | GND | 0 | 0 | 0 | 1 | 0 | 0 | 0 |
| GND | SCL | V+ | 0 | 0 | 0 | 1 | 0 | 0 | 1 |
| GND | SDA | GND | 0 | 0 | 0 | 1 | 0 | 1 | 0 |
| GND | SDA | V+ | 0 | 0 | 0 | 1 | 0 | 1 | 1 |
| V+ | SCL | GND | 0 | 0 | 0 | 1 | 1 | 0 | 0 |
| V+ | SCL | V+ | 0 | 0 | 0 | 1 | 1 | 0 | 1 |
| V+ | SDA | GND | 0 | 0 | 0 | 1 | 1 | 1 | 0 |
| V+ | SDA | V+ | 0 | 0 | 0 | 1 | 1 | 1 | 1 |
| GND | GND | SCL | 0 | 0 | 1 | 0 | 0 | 0 | 0 |
| GND | GND | SDA | 0 | 0 | 1 | 0 | 0 | 0 | 1 |
| GND | V+ | SCL | 0 | 0 | 1 | 0 | 0 | 1 | 0 |
| GND | V+ | SDA | 0 | 0 | 1 | 0 | 0 | 1 | 1 |
| V+ | GND | SCL | 0 | 0 | 1 | 0 | 1 | 0 | 0 |
| V+ | GND | SDA | 0 | 0 | 1 | 0 | 1 | 0 | 1 |
| V+ | V+ | SCL | 0 | 0 | 1 | 0 | 1 | 1 | 0 |
| V+ | V+ | SDA | 0 | 0 | 1 | 0 | 1 | 1 | 1 |
| GND | GND | GND | 0 | 0 | 1 | 1 | 0 | 0 | 0 |
| GND | GND | V+ | 0 | 0 | 1 | 1 | 0 | 0 | 1 |
| GND | V+ | GND | 0 | 0 | 1 | 1 | 0 | 1 | 0 |
| GND | V+ | V+ | 0 | 0 | 1 | 1 | 0 | 1 | 1 |
| V+ | GND | GND | 0 | 0 | 1 | 1 | 1 | 0 | 0 |
| V+ | GND | V+ | 0 | 0 | 1 | 1 | 1 | 0 | 1 |
| V+ | V+ | GND | 0 | 0 | 1 | 1 | 1 | 1 | 0 |
| V+ | V+ | V+ | 0 | 0 | 1 | 1 | 1 | 1 | 1 |
| SCL | SCL | SCL | 0 | 1 | 0 | 0 | 0 | 0 | 0 |
| SCL | SCL | SDA | 0 | 1 | 0 | 0 | 0 | 0 | 1 |
| SCL | SDA | SCL | 0 | 1 | 0 | 0 | 0 | 1 | 0 |
| SCL | SDA | SDA | 0 | 1 | 0 | 0 | 0 | 1 | 1 |
| SDA | SCL | SCL | 0 | 1 | 0 | 0 | 1 | 0 | 0 |
| SDA | SCL | SDA | 0 | 1 | 0 | 0 | 1 | 0 | 1 |
| SDA | SDA | SCL | 0 | 1 | 0 | 0 | 1 | 1 | 0 |
| SDA | SDA | SDA | 0 | 1 | 0 | 0 | 1 | 1 | 1 |
| SCL | SCL | GND | 0 | 1 | 0 | 1 | 0 | 0 | 0 |
| SCL | SCL | V+ | 0 | 1 | 0 | 1 | 0 | 0 | 1 |
| SCL | SDA | GND | 0 | 1 | 0 | 1 | 0 | 1 | 0 |
| SCL | SDA | V+ | 0 | 1 | 0 | 1 | 0 | 1 | 1 |
| SDA | SCL | GND | 0 | 1 | 0 | 1 | 1 | 0 | 0 |
| SDA | SCL | V+ | 0 | 1 | 0 | 1 | 1 | 0 | 1 |
| SDA | SDA | GND | 0 | 1 | 0 | 1 | 1 | 1 | 0 |
| SDA | SDA | V+ | 0 | 1 | 0 | 1 | 1 | 1 | 1 |

2-Wire-Interfaced 8-Bit I/O Port Expander with Reset

Table 7. MAX7310 Address Map (continued)

| AD2 | AD1 | AD0 | A6 | A5 | A4 | A3 | A2 | A1 | A0 |
|-----|-----|-----|----|----|----|----|----|----|----|
| SCL | GND | SCL | 0 | 1 | 1 | 0 | 0 | 0 | 0 |
| SCL | GND | SDA | 0 | 1 | 1 | 0 | 0 | 0 | 1 |
| SCL | V+ | SCL | 0 | 1 | 1 | 0 | 0 | 1 | 0 |
| SCL | V+ | SDA | 0 | 1 | 1 | 0 | 0 | 1 | 1 |
| SDA | GND | SCL | 0 | 1 | 1 | 0 | 1 | 0 | 0 |
| SDA | GND | SDA | 0 | 1 | 1 | 0 | 1 | 0 | 1 |
| SDA | V+ | SCL | 0 | 1 | 1 | 0 | 1 | 1 | 0 |
| SDA | V+ | SDA | 0 | 1 | 1 | 0 | 1 | 1 | 1 |
| SCL | GND | GND | 0 | 1 | 1 | 1 | 0 | 0 | 0 |
| SCL | GND | V+ | 0 | 1 | 1 | 1 | 0 | 0 | 1 |
| SCL | V+ | GND | 0 | 1 | 1 | 1 | 0 | 1 | 0 |
| SCL | V+ | V+ | 0 | 1 | 1 | 1 | 0 | 1 | 1 |
| SDA | GND | GND | 0 | 1 | 1 | 1 | 1 | 0 | 0 |
| SDA | GND | V+ | 0 | 1 | 1 | 1 | 1 | 0 | 1 |
| SDA | V+ | GND | 0 | 1 | 1 | 1 | 1 | 1 | 0 |
| SDA | V+ | V+ | 0 | 1 | 1 | 1 | 1 | 1 | 1 |

Applications Information

Power-Supply Consideration

The MAX7310 operates from a supply voltage of 2.3V to 5.5V. Bypass the power supply to GND with a 0.047 μ F capacitor as close to the device as possible. For the QFN version, connect the underside exposed pad to GND.

Chip Information

TRANSISTOR COUNT: 10,256

PROCESS: BiCMOS

2-Wire-Interfaced 8-Bit I/O Port Expander with Reset

MAX7310

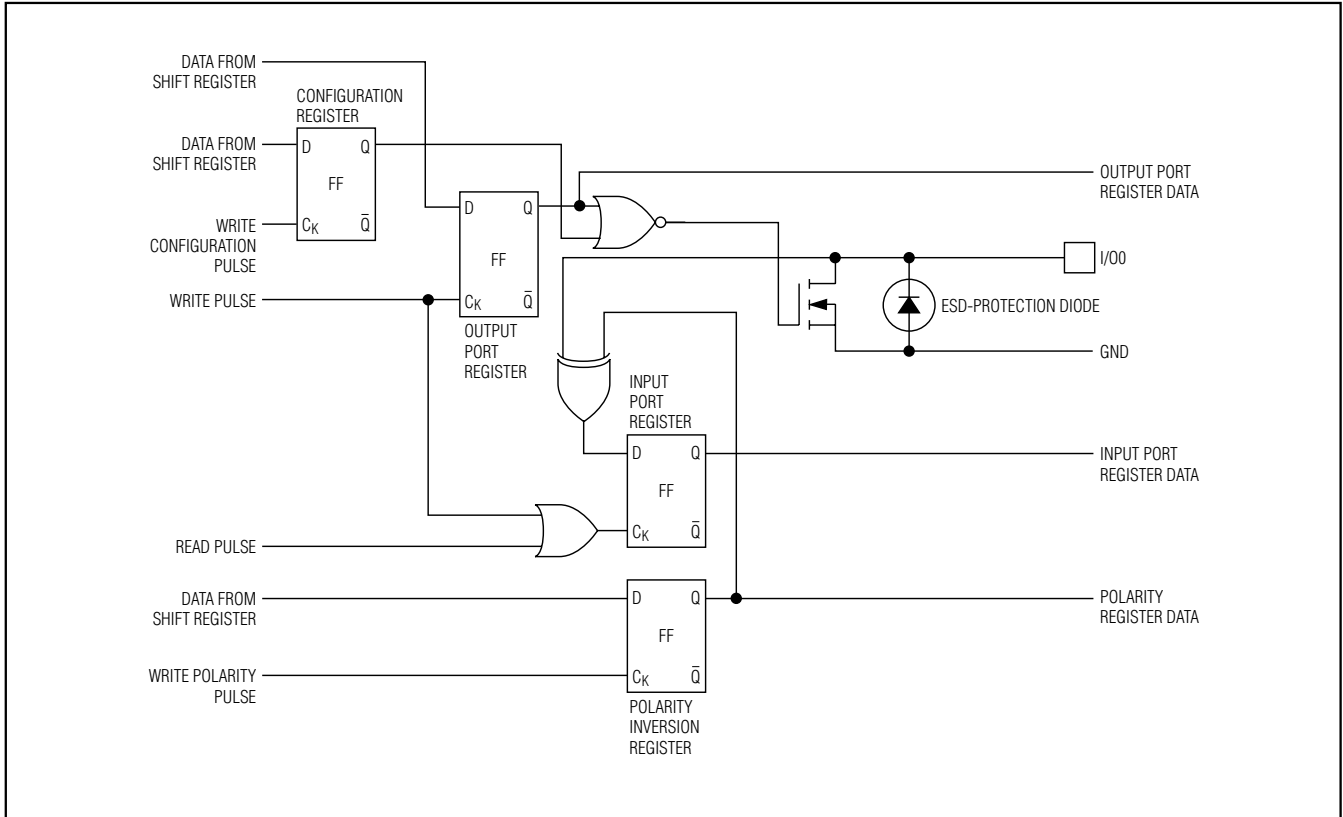


Figure 7. Simplified Schematic of I/O

2-Wire-Interfaced 8-Bit I/O Port Expander with Reset

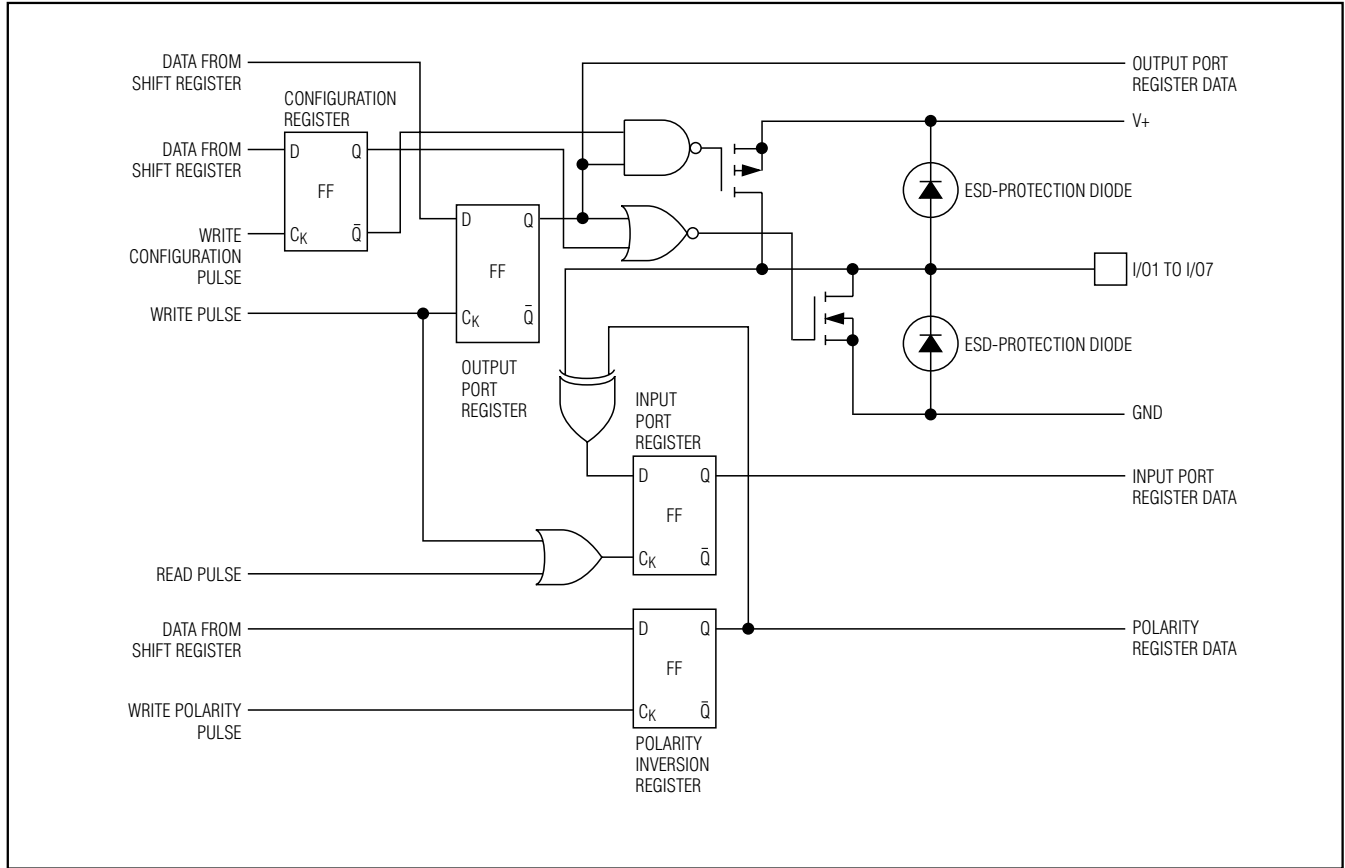


Figure 8. Simplified Schematic of I/O1-I/O7

2-Wire-Interfaced 8-Bit I/O Port Expander with Reset

MAX7310

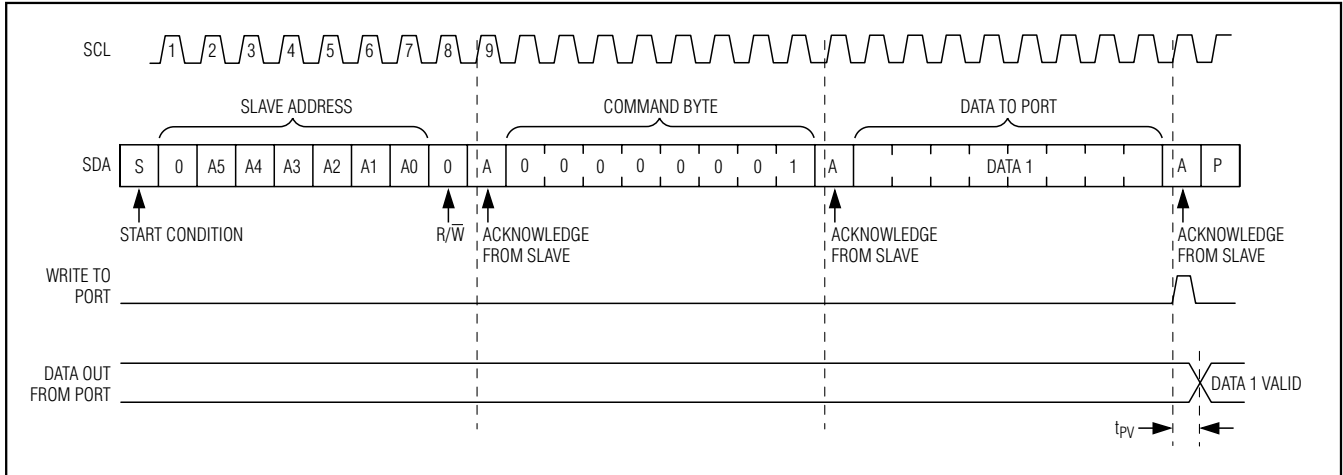


Figure 9. Write to Output Port Register Through Write-Byte Protocol

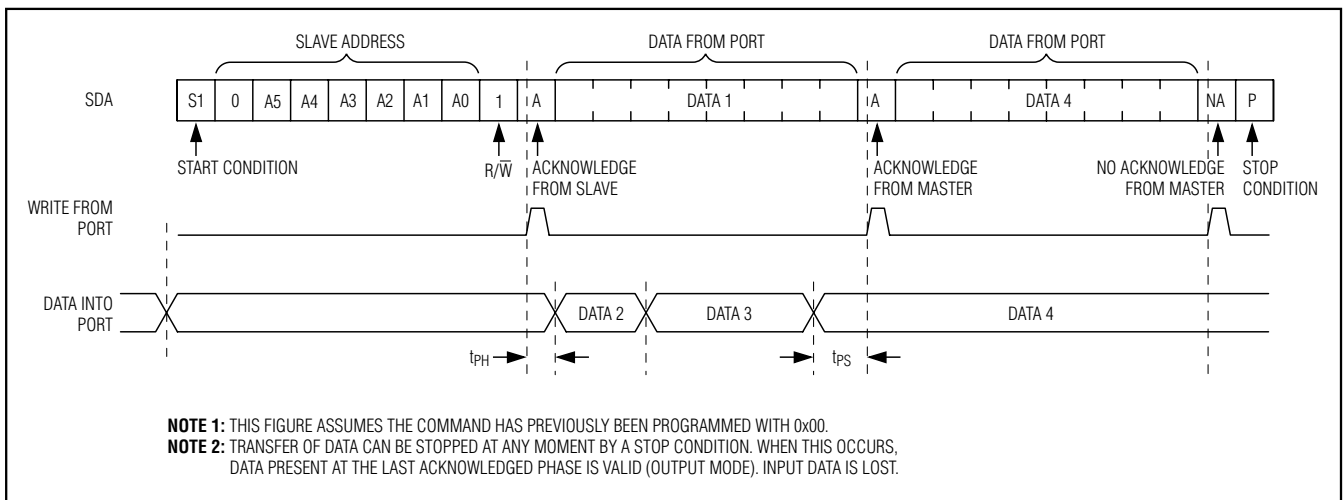
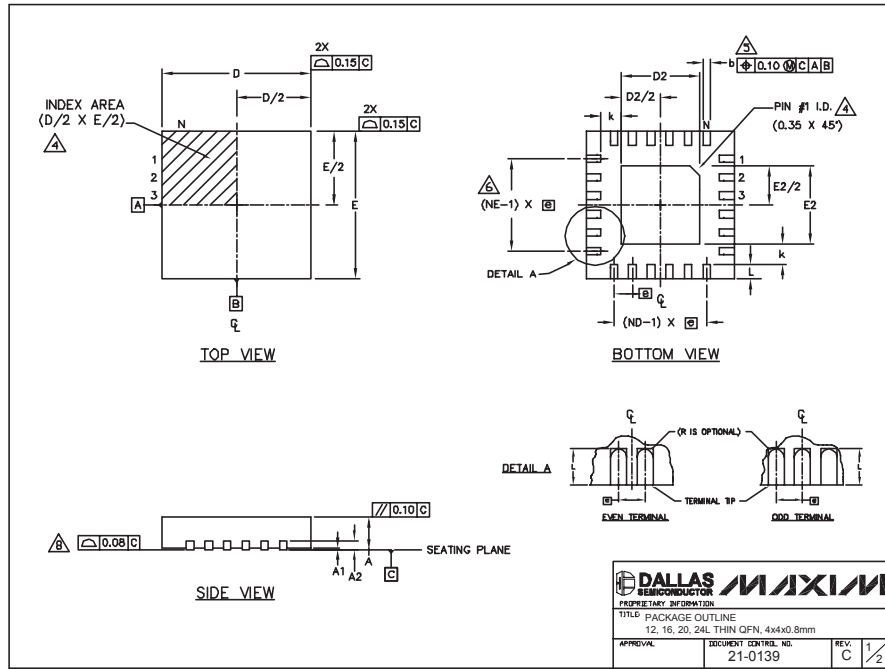


Figure 10. Read Input Port Register Through Receive-Byte Protocol

2-Wire-Interfaced 8-Bit I/O Port Expander with Reset

Package Information

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information, go to www.maxim-ic.com/packages.)



| COMMON DIMENSIONS | | | | | | | | | | | | |
|-------------------|-----------|------|------|-----------|------|------|-----------|------|------|-----------|------|------|
| PKG REF. | 12L 4x4 | | | 16L 4x4 | | | 20L 4x4 | | | 24L 4x4 | | |
| | MIN. | NOM. | MAX. | MIN. | NOM. | MAX. | MIN. | NOM. | MAX. | MIN. | NOM. | MAX. |
| A | 0.70 | 0.75 | 0.80 | 0.70 | 0.75 | 0.80 | 0.70 | 0.75 | 0.80 | 0.70 | 0.75 | 0.80 |
| AL | 0.0 | 0.02 | 0.05 | 0.0 | 0.02 | 0.05 | 0.0 | 0.02 | 0.05 | 0.0 | 0.02 | 0.05 |
| A2 | 0.20 REF. | | | 0.20 REF. | | | 0.20 REF. | | | 0.20 REF. | | |
| b | 0.25 | 0.30 | 0.35 | 0.25 | 0.30 | 0.35 | 0.20 | 0.25 | 0.30 | 0.18 | 0.23 | 0.30 |
| D | 3.90 | 4.00 | 4.10 | 3.90 | 4.00 | 4.10 | 3.90 | 4.00 | 4.10 | 3.90 | 4.00 | 4.10 |
| E | 3.90 | 4.00 | 4.10 | 3.90 | 4.00 | 4.10 | 3.90 | 4.00 | 4.10 | 3.90 | 4.00 | 4.10 |
| e | 0.80 BSC. | | | 0.65 BSC. | | | 0.50 BSC. | | | 0.50 BSC. | | |
| k | 0.25 | - | - | 0.25 | - | - | 0.25 | - | - | 0.25 | - | - |
| L | 0.45 | 0.55 | 0.65 | 0.45 | 0.55 | 0.65 | 0.45 | 0.55 | 0.65 | 0.30 | 0.40 | 0.50 |
| N | 12 | | | 16 | | | 20 | | | 24 | | |
| ND | 3 | | | 4 | | | 5 | | | 6 | | |
| NE | 3 | | | 4 | | | 5 | | | 6 | | |
| Jdec Vpr. | WGGB | | | WGGC | | | WGGD-1 | | | WGGD-2 | | |

| PKG CODES | D2 | | | E2 | | | DOWN BENDS ALLOWED |
|-----------|------|------|------|------|------|------|--------------------|
| | MIN. | NOM. | MAX. | MIN. | NOM. | MAX. | |
| T1244-2 | 1.95 | 2.10 | 2.25 | 1.95 | 2.10 | 2.25 | NO |
| T1244-3 | 1.95 | 2.10 | 2.25 | 1.95 | 2.10 | 2.25 | YES |
| T1244-4 | 1.95 | 2.10 | 2.25 | 1.95 | 2.10 | 2.25 | NO |
| T1644-2 | 1.95 | 2.10 | 2.25 | 1.95 | 2.10 | 2.25 | NO |
| T1644-3 | 1.95 | 2.10 | 2.25 | 1.95 | 2.10 | 2.25 | YES |
| T1644-4 | 1.95 | 2.10 | 2.25 | 1.95 | 2.10 | 2.25 | NO |
| T2044-1 | 1.95 | 2.10 | 2.25 | 1.95 | 2.10 | 2.25 | NO |
| T2044-2 | 1.95 | 2.10 | 2.25 | 1.95 | 2.10 | 2.25 | YES |
| T2044-3 | 1.95 | 2.10 | 2.25 | 1.95 | 2.10 | 2.25 | NO |
| T2444-1 | 2.45 | 2.60 | 2.63 | 2.45 | 2.60 | 2.63 | NO |
| T2444-2 | 1.95 | 2.10 | 2.25 | 1.95 | 2.10 | 2.25 | YES |
| T2444-3 | 2.45 | 2.60 | 2.63 | 2.45 | 2.60 | 2.63 | YES |
| T2444-4 | 2.45 | 2.60 | 2.63 | 2.45 | 2.60 | 2.63 | NO |

NOTES:

- DIMENSIONING & TOLERANCING CONFORM TO ASME Y14.5M-1994.
- ALL DIMENSIONS ARE IN MILLIMETERS, ANGLES ARE IN DEGREES.
- N IS THE TOTAL NUMBER OF TERMINALS.
- THE TERMINAL #1 IDENTIFIER AND TERMINAL NUMBERING CONVENTION SHALL CONFORM TO JEDEC 95-1 SPP-012. DETAILS OF TERMINAL #1 IDENTIFIER ARE OPTIONAL, BUT MUST BE LOCATED WITHIN THE ZONE INDICATED. THE TERMINAL #1 IDENTIFIER MAY BE EITHER A MOLD OR MARKED FEATURE.
- DIMENSION b APPLIES TO METALLIZED TERMINAL AND IS MEASURED BETWEEN 0.25 mm AND 0.30 mm FROM TERMINAL TIP.
- ND AND NE REFER TO THE NUMBER OF TERMINALS ON EACH D AND E SIDE RESPECTIVELY.
- DEPOPULATION IS POSSIBLE IN A SYMMETRICAL FASHION.
- COPLANARITY APPLIES TO THE EXPOSED HEAT SINK SLUG AS WELL AS THE TERMINALS.
- DRAWING CONFORMS TO JEDEC MO220, EXCEPT FOR T2444-1, T2444-3 AND T2444-4.

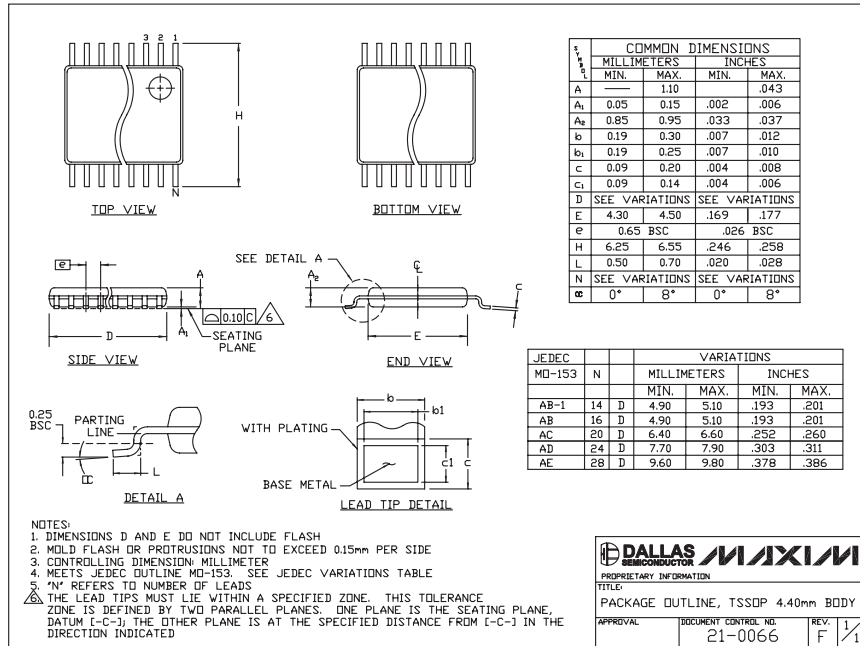
| | |
|--------------------------------------|---------------------------------|
| DALLAS MAXIM SEMICONDUCTOR | |
| PROPRIETARY INFORMATION | |
| TITLE: PACKAGE OUTLINE | |
| 12, 16, 20, 24L THIN QFN, 4x4x0.8mm | |
| APPROVAL: | DOCUMENT CONTROL NO. 21-0139 |
| REV. C | 1/2 |

2-Wire-Interfaced 8-Bit I/O Port Expander with Reset

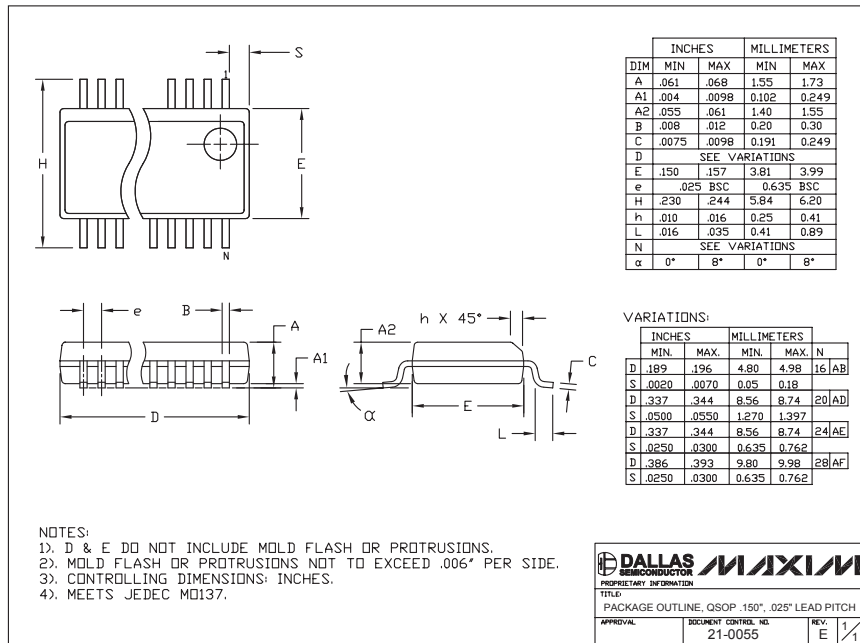
Package Information (continued)

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information, go to www.maxim-ic.com/packages.)

MAX7310



TSSOP4.40mmLEPS



QSOP150

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