



**THE DATASHEET OF  
MAX4885ETJ+**



# Complete VGA 1:2 or 2:1 Multiplexer

## General Description

The MAX4885 integrates high-bandwidth analog switches and level-translating buffers to implement a complete 1:2 or 2:1 multiplexer for VGA signals. The device provides switching for RGB, display data channel (DDC), and horizontal and vertical synchronization (HSYNC, VSYNC) signals. A low-noise charge pump with internal capacitors provides a boosted gate-drive voltage to improve performance of the RGB switches.

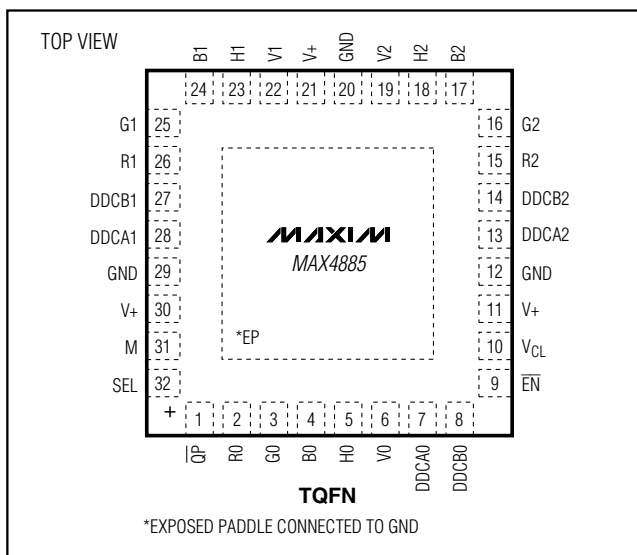
In the 1:2 multiplexer mode, HSYNC/VSYNC inputs feature level-shifting buffers to support low-voltage CMOS or standard TTL-compatible graphics controllers. In the 2:1 multiplexer mode, the output buffers for the HSYNC/VSYNC inputs are disabled, allowing bidirectional signaling. In both modes, DDC signals are voltage-clamped to an external voltage to provide level translation and protection. The MAX4885 features a 5 $\mu$ A shutdown mode and is ESD protected to  $\pm$ 8kV Human Body Model (HBM) on externally routed pins.

The MAX4885 is specified over the extended (-40°C to +85°C) temperature range, and is available in the 32-pin, 5mm x 5mm TQFN package.

## Applications

Notebook Computers  
Digital Projectors  
Computer Monitors  
Servers  
KVM Switches

## Pin Configuration



## Features

- ◆ +5V Single-Supply Operation
- ◆ Programmable Voltage Clamp for Open-Drain DDC Signals
- ◆ Low 5 $\Omega$  (typ) On-Resistance (R, G, B Signals)
- ◆ Low 13pF (typ) On-Capacitance (R, G, B Signals)
- ◆ Break-Before-Make Switching Protects Against Circuit Shorts
- ◆  $\pm$ 8kV HBM ESD Protection on Externally Routed Pins
- ◆ Low 300 $\mu$ A Supply Current (Lower than 1 $\mu$ A with Charge Pump Disabled)
- ◆ Space-Saving, Lead-Free, 32-Pin (5mm x 5mm) TQFN Package

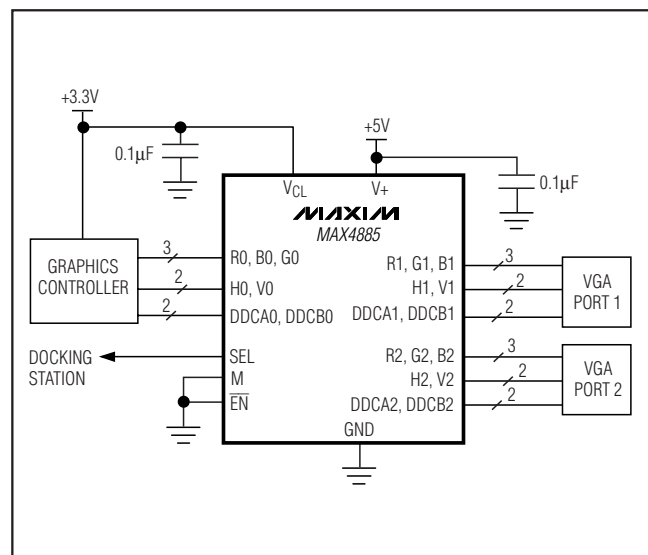
## Ordering Information

| PART        | TEMP RANGE     | PIN-PACKAGE | PKG CODE |
|-------------|----------------|-------------|----------|
| MAX4885ETJ+ | -40°C to +85°C | 32 TQFN-EP* | T3255-4  |

\*EP = Exposed pad.

+Denotes lead-free package.

## Typical Operating Circuit



# Complete VGA 1:2 or 2:1 Multiplexer

## ABSOLUTE MAXIMUM RATINGS

(All voltages referenced to GND.)

|  |                                |
|--|--------------------------------|
| V <sub>+</sub> , V <sub>CL</sub> .....   | -0.3V to +6V                   |
| R <sub>-</sub> , G <sub>-</sub> , B <sub>-</sub> , DDCA <sub>-</sub> , DDCB <sub>-</sub> , SEL, M,<br>$\overline{EN}$ , $\overline{QP}$ (Note 1) ..... | -0.3V to V <sub>+</sub> + 0.3V |
| H <sub>-</sub> , V <sub>-</sub> .....  | -0.3V to +6V                   |
| Continuous Current Through RGB Switches .....  | ±70mA                          |
| Continuous Current Through HV, DDC Switches .....  | ±50mA                          |
| Peak Current Through RGB Switches<br>(pulsed at 1ms, 10% duty cycle) .....   | ±140mA                         |
| Peak Current Through HV, DDC Switches (pulsed at 1ms,<br>10% duty cycle) .....   | ±100mA                         |

Continuous Power Dissipation (T<sub>A</sub> = +70°C)

|  |                 |
|--|-----------------|
| 32-Pin TQFN (derate 21.3mW/°C above +70°C) ..... | 1702mW          |
| Operating Temperature Range .....                | -40°C to +85°C  |
| Storage Temperature Range .....                  | -65°C to +150°C |
| Junction Temperature .....                       | +150°C          |
| Lead Temperature (soldering, 10s) .....          | +300°C          |

**Note 1:** Signals exceeding V<sub>+</sub> or GND are clamped by internal diodes. Limit forward-diode current to maximum current rating.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

## ELECTRICAL CHARACTERISTICS

(V<sub>+</sub> = +5.0V ±10%, V<sub>CL</sub> = +3.3V ±10%, T<sub>A</sub> = T<sub>MIN</sub> to T<sub>MAX</sub>,  $\overline{QP}$  = GND, unless otherwise noted. Typical values are at V<sub>+</sub> = +5.0V, V<sub>CL</sub> = +3.3V and T<sub>A</sub> = +25°C.)

| PARAMETER                                | SYMBOL                | CONDITIONS   | MIN | TYP  | MAX            | UNITS |
|--|-----------------------|--|-----|------|----------------|-------|
| Supply Voltage Range                     | V <sub>+</sub>        |  | 4.5 |      | 5.5            | V     |
| Clamp Voltage Range                      | V <sub>CL</sub>       |  | 2.7 |      | V <sub>+</sub> | V     |
| V <sub>+</sub> Quiescent Supply Current  | I <sub>+</sub>        | V <sub>+</sub> = +5.5V   |     | 0.3  | 0.5            | mA    |
|  |                       | $\overline{QP}$ = GND<br>$\overline{QP}$ = V <sub>+</sub>  |     |      | 1              |       |
| V <sub>CL</sub> Quiescent Supply Current | I <sub>CL</sub>       | V <sub>CL</sub> = V <sub>+</sub> = +5.5V   |     |      | 1              | μA    |
| V <sub>+</sub> Shutdown Current          | I <sub>+</sub> SHDN   | V <sub>+</sub> = +5.5V, all digital inputs to V <sub>+</sub> or GND                              |     |      | 5              | μA    |
| V <sub>CL</sub> Shutdown Current         | I <sub>CL</sub> SHDN  | V <sub>CL</sub> = V <sub>+</sub> = +5.5V, all digital inputs to V <sub>+</sub> or GND            |     |      | 1              | μA    |
| <b>RGB ANALOG SWITCHES</b>               |                       |  |     |      |                |       |
| On-Resistance                            | R <sub>ON</sub>       | 0V < V <sub>IN</sub> < +2.5V, I <sub>IN</sub> = -40mA  |     | 5    | 7.5            | Ω     |
|  |                       | $\overline{QP}$ = GND<br>$\overline{QP}$ = V <sub>+</sub>  |     | 6    | 10             |       |
| On-Resistance Matching                   | ΔR <sub>ON</sub>      | 0V < V <sub>IN</sub> < +2.5V, I <sub>IN</sub> = -40mA  |     | 0.5  | 1.5            | Ω     |
| On-Resistance Flatness                   | R <sub>FLAT(ON)</sub> | 0V < V <sub>IN</sub> < +2.5V, I <sub>IN</sub> = -40mA  |     | 0.02 | 0.75           | Ω     |
| Off-Leakage Current                      | I <sub>L(OFF)</sub>   | R <sub>-</sub> , G <sub>-</sub> , B <sub>-</sub> = 0V or +5.5V, $\overline{EN}$ = GND            | -1  |      | +1             | μA    |
| On-Leakage Current                       | I <sub>L(ON)</sub>    | R <sub>-</sub> , G <sub>-</sub> , B <sub>-</sub> = 0V or +5.5V, $\overline{EN}$ = V <sub>+</sub> | -1  |      | +1             | μA    |
| Charge Injection                         | Q                     | R <sub>-</sub> , G <sub>-</sub> , B <sub>-</sub> = 0V, C <sub>L</sub> = 1000pF                   |     | 10   |                | pC    |
|  |                       | $\overline{QP}$ = GND<br>$\overline{QP}$ = V <sub>+</sub>  |     | 8    |                |       |
| <b>HV MULTIPLEXER</b>                    |                       |  |     |      |                |       |
| Input-Voltage Low                        | V <sub>ILHV</sub>     | M = GND  |     |      | 0.8            | V     |
| Input-Voltage High                       | V <sub>IHHV</sub>     | M = GND  | 2.0 |      |                | V     |
| High-Output Drive Current                | I <sub>OHHV</sub>     | V <sub>OUT</sub> = V <sub>+</sub> - 0.5V, M = GND  | -16 |      |                | mA    |
| Low-Output Drive Current                 | I <sub>OLHV</sub>     | V <sub>OUT</sub> = +0.5V, M = GND  |     |      | +16            | mA    |
| On-Resistance                            | R <sub>ONHV</sub>     | H <sub>-</sub> = V <sub>-</sub> = +2.5V, I <sub>IN</sub> = -40mA, M = V <sub>+</sub>             |     |      | 15             | Ω     |
| Charge Injection                         | Q                     | H <sub>-</sub> , V <sub>-</sub> = 0V, M = V <sub>+</sub> , C <sub>L</sub> = 1000pF               |     | 21   |                | pC    |

# Complete VGA 1:2 or 2:1 Multiplexer

MAX4885

## ELECTRICAL CHARACTERISTICS (continued)

(V<sub>+</sub> = +5.0V ±10%, V<sub>CL</sub> = +3.3V ±10%, T<sub>A</sub> = T<sub>MIN</sub> to T<sub>MAX</sub>,  $\overline{QP}$  = GND, unless otherwise noted. Typical values are at V<sub>+</sub> = +5.0V, V<sub>CL</sub> = +3.3V and T<sub>A</sub> = +25°C.)

| PARAMETER                            | SYMBOL               | CONDITIONS   | MIN | TYP | MAX | UNITS |
|--------------------------------------|----------------------|--|-----|-----|-----|-------|
| <b>DDC MULTIPLEXER</b>               |                      |  |     |     |     |       |
| On-Resistance                        | R <sub>ON(DDC)</sub> | V <sub>IN</sub> < +0.4V, V <sub>CL</sub> = +3.0V, I <sub>IN</sub> = -20mA  |     |     | 20  | Ω     |
| DDC Leakage                          | I <sub>L(DDC)</sub>  | V <sub>CL</sub> - 0.4V < V <sub>OUT</sub> < V <sub>CL</sub> , V <sub>IN</sub> = V <sub>+</sub>   | -1  |     | +1  | μA    |
| Charge Injection                     | Q                    | DDCA <sub>-</sub> , DDCB <sub>-</sub> = 0V, C <sub>L</sub> = 1000pF  |     | 10  |     | pC    |
| <b>SWITCH LOGIC (SEL, M, EN, QP)</b> |                      |  |     |     |     |       |
| Input-Low Voltage                    | V <sub>IL</sub>      | V <sub>+</sub> = +5.5V   |     |     | 0.8 | V     |
| Input-High Voltage                   | V <sub>IH</sub>      | V <sub>+</sub> = +4.5V   | 2.0 |     |     | V     |
| Input Leakage Current                | I <sub>LEAK</sub>    | V <sub>IN</sub> = V <sub>+</sub>   | -1  |     | +1  | μA    |
| <b>ESD PROTECTION</b>                |                      |  |     |     |     |       |
| ESD Protection                       |                      | Human Body Model, all pins   |     | ±2  |     | kV    |
|                                      |                      | Human Body Model, R <sub>-</sub> , G <sub>-</sub> , B <sub>-</sub> , H <sub>-</sub> , V <sub>-</sub> , DDCA <sub>-</sub> , DDCB <sub>-</sub> |     | ±8  |     | kV    |

## AC ELECTRICAL CHARACTERISTICS

(V<sub>+</sub> = +5.0V ±10%, V<sub>CL</sub> = +3.3V ±10%, T<sub>A</sub> = T<sub>MIN</sub> to T<sub>MAX</sub>,  $\overline{QP}$  = GND. Typical values are at V<sub>+</sub> = +5.0V, V<sub>CL</sub> = +3.3V and T<sub>A</sub> = +25°C, unless otherwise noted.) (Note 2)

| PARAMETER         | SYMBOL           | CONDITIONS   | MIN                              | TYP  | MAX | UNITS |
|-------------------|------------------|--|----------------------------------|------|-----|-------|
| Bandwidth         | f <sub>MAX</sub> | R <sub>S</sub> = R <sub>L</sub> = 50Ω  | $\overline{QP}$ = GND            | 350  |     | MHz   |
|                   |                  |  | $\overline{QP}$ = V <sub>+</sub> | 350  |     |       |
| Insertion Loss    | I <sub>LOS</sub> | 1MHz < f < 50MHz,<br>R <sub>S</sub> = R <sub>L</sub> = 50Ω   | $\overline{QP}$ = GND            | 0.85 | 1.2 | dB    |
|                   |                  |  | $\overline{QP}$ = V <sub>+</sub> | 1    | 1.6 |       |
| Crosstalk         | V <sub>CT</sub>  | 1MHz < f < 50MHz, V <sub>IN</sub> = 0.7V <sub>P-P</sub> ,<br>R <sub>S</sub> = R <sub>L</sub> = 50Ω |                                  | -40  |     | dB    |
| Off-Capacitance   | C <sub>OFF</sub> | f = 1MHz,<br>$\overline{QP}$ = GND or V <sub>+</sub>   |                                  | 5    |     | pF    |
| On-Capacitance    | C <sub>ON</sub>  | f = 1 MHz  | $\overline{QP}$ = GND            | 13   |     | pF    |
|                   |                  |  | $\overline{QP}$ = V <sub>+</sub> | 17   |     |       |
| Charge-Pump Noise | V <sub>NQP</sub> | V <sub>IN</sub> = +1.0V, R <sub>S</sub> = R <sub>L</sub> = 50Ω                                     |                                  | 50   | 200 | μV    |

# Complete VGA 1:2 or 2:1 Multiplexer

## TIMING CHARACTERISTICS

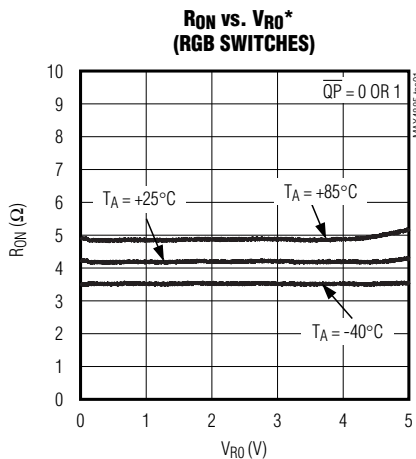
( $V_+ = +5.0V \pm 10\%$ ,  $V_{CL} = +3.3V \pm 10\%$ ,  $T_A = T_{MIN}$  to  $T_{MAX}$ ,  $\overline{QP} = GND$ . Typical values are at  $V_+ = +5.0V$ ,  $V_{CL} = +3.3V$  and  $T_A = +25^\circ C$ , unless otherwise noted.) (Note 2)

| PARAMETER                  | SYMBOL     | CONDITIONS   | MIN       | TYP  | MAX | UNITS   |
|----------------------------|------------|--|-----------|------|-----|---------|
| Charge-Pump Startup Time   | $t_{QPON}$ |  |           | 150  |     | $\mu s$ |
| <b>RGB ANALOG SWITCHES</b> |            |  |           |      |     |         |
| Turn-On Time               | $t_{ON}$   | $V_{IN} = +1.0V$ , $R_L = 100\Omega$ , Figure 1                                      |           |      | 7   | $\mu s$ |
| Turn-Off Time              | $t_{OFF}$  | $V_{IN} = +1.0V$ , $R_L = 100\Omega$ , Figure 1                                      |           | 0.1  |     | $\mu s$ |
| Propagation Delay          | $t_{PD}$   | $C_L = 10pF$ , Figure 2, $R_L = R_S = 50\Omega$                                      |           | 0.1  |     | ns      |
| Output Skew Between Ports  | $t_{SKEW}$ | $C_L = 10pF$ , Skew between any two ports: R, G, B. Figure 2, $R_S = R_L = 50\Omega$ |           | 30   |     | ps      |
| <b>HV MULTIPLEXER</b>      |            |  |           |      |     |         |
| Turn-On Time               | $t_{ON}$   | $M = 0$ , Figure 1   |           |      | 5   | $\mu s$ |
| Turn-Off Time              | $t_{OFF}$  | $M = 0$ , Figure 1   |           | 0.1  |     | $\mu s$ |
| Propagation Delay          | $t_{PD}$   | $C_L = 10pF$   | $M = GND$ | 6    | 16  | ns      |
|                            |            |  | $M = V_+$ | 0.1  |     |         |
| <b>DDC MULTIPLEXER</b>     |            |  |           |      |     |         |
| Turn-On Time               | $t_{ON}$   | $V_{IN} = +1.0V$ , $R_L = 100\Omega$ , Figure 1                                      |           |      | 5   | $\mu s$ |
| Turn-Off Time              | $t_{OFF}$  | $V_{IN} = +1.0V$ , $R_L = 100\Omega$ , Figure 1                                      |           | 0.1  |     | $\mu s$ |
| Propagation Delay          | $t_{PD}$   | $C_L = 10pF$ , Figure 2  |           | 0.25 |     | ns      |

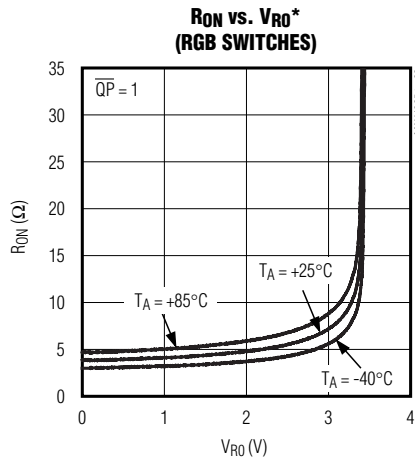
**Note 2:** Timing parameters are guaranteed by design and correlation over the full operating temperature range.

## Typical Operating Characteristics

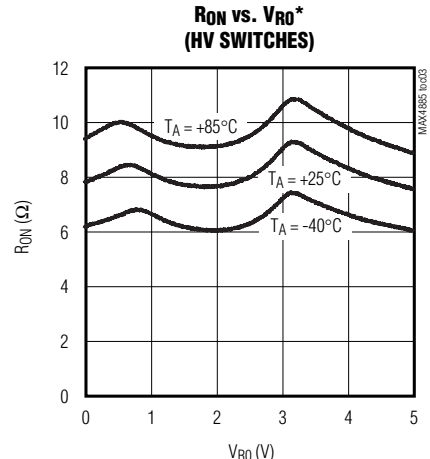
( $V_+ = +5.0V$ ,  $V_{CL} = +3.3V$  and  $T_A = +25^\circ C$ , unless otherwise noted.)



\*RO, GO, BO ARE INTERCHANGEABLE.



\*RO, GO, BO ARE INTERCHANGEABLE.



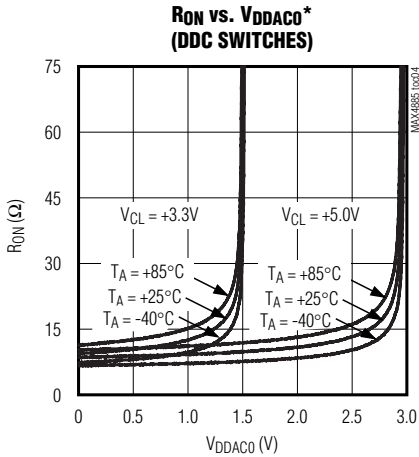
\*RO, GO, BO ARE INTERCHANGEABLE.

# Complete VGA 1:2 or 2:1 Multiplexer

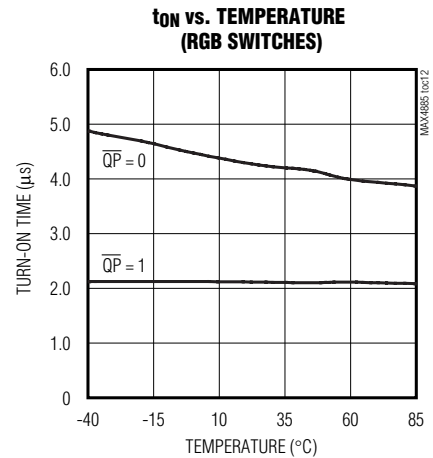
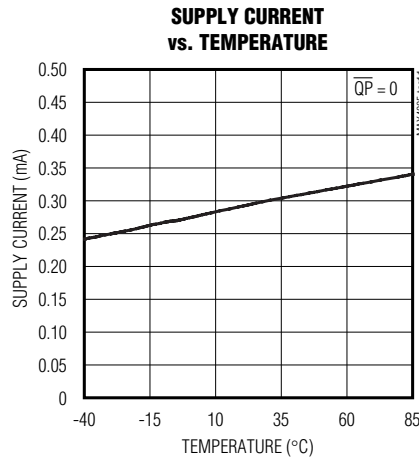
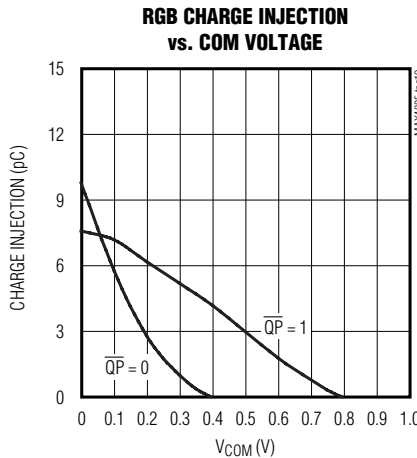
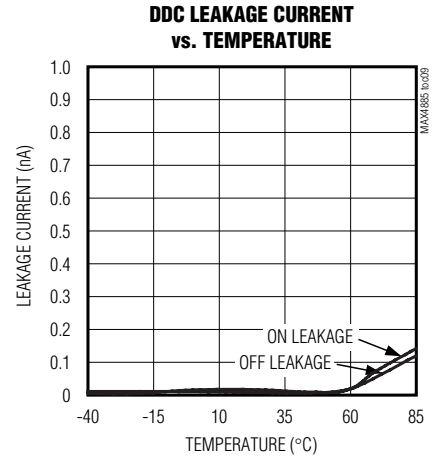
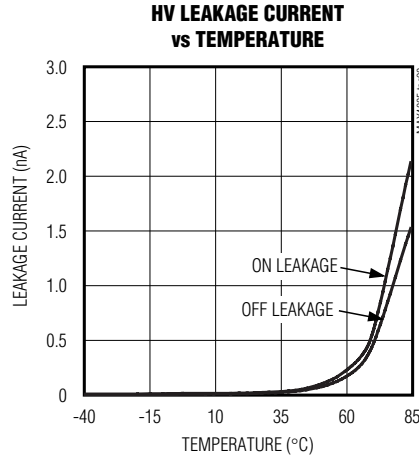
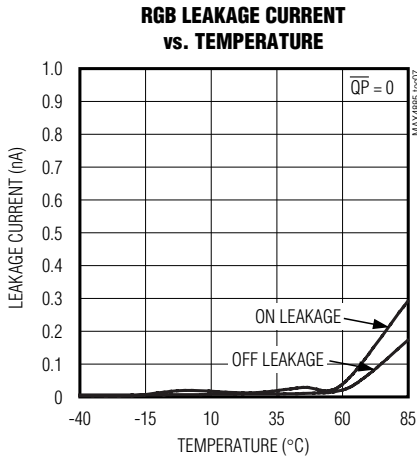
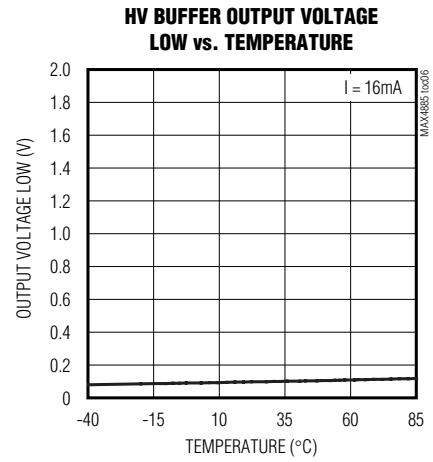
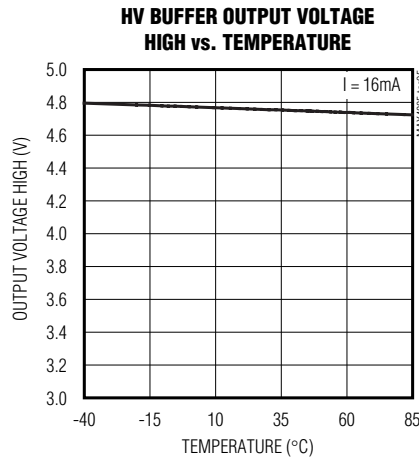
MAX4885

## Typical Operating Characteristics (continued)

( $V_+ = +5.0V$ ,  $V_{CL} = +3.3V$  and  $T_A = +25^\circ C$ , unless otherwise noted.)



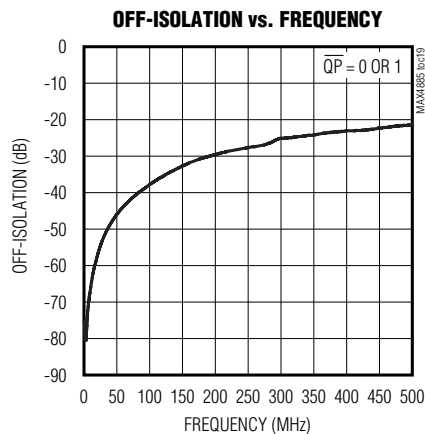
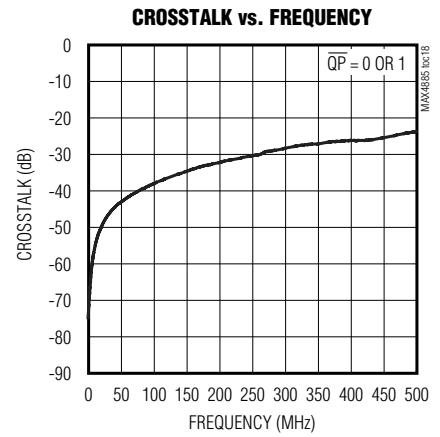
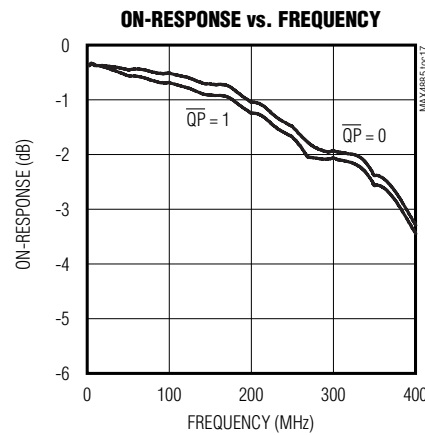
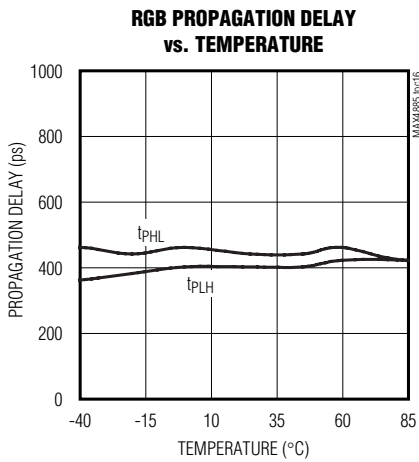
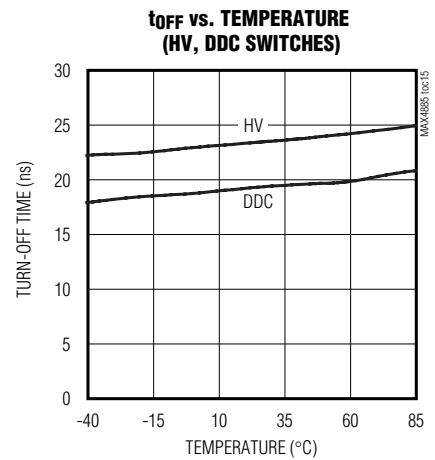
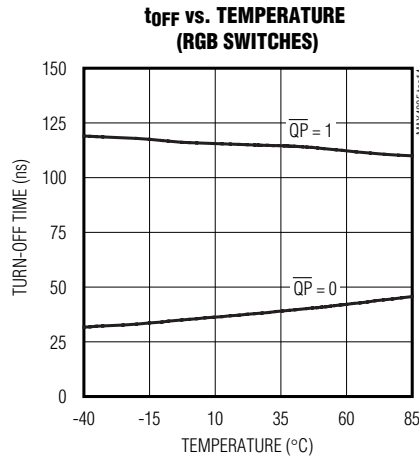
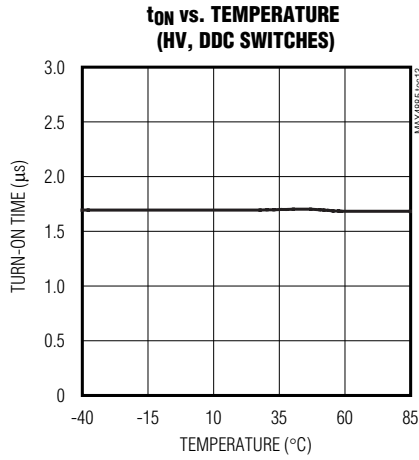
\*DDACO AND DDCB0 ARE INTERCHANGEABLE.



# Complete VGA 1:2 or 2:1 Multiplexer

## Typical Operating Characteristics (continued)

(V+ = +5.0V, V<sub>CL</sub> = +3.3V and T<sub>A</sub> = +25°C, unless otherwise noted.)



# Complete VGA 1:2 or 2:1 Multiplexer

## Timing Circuits/Timing Diagrams

**MAX4885**

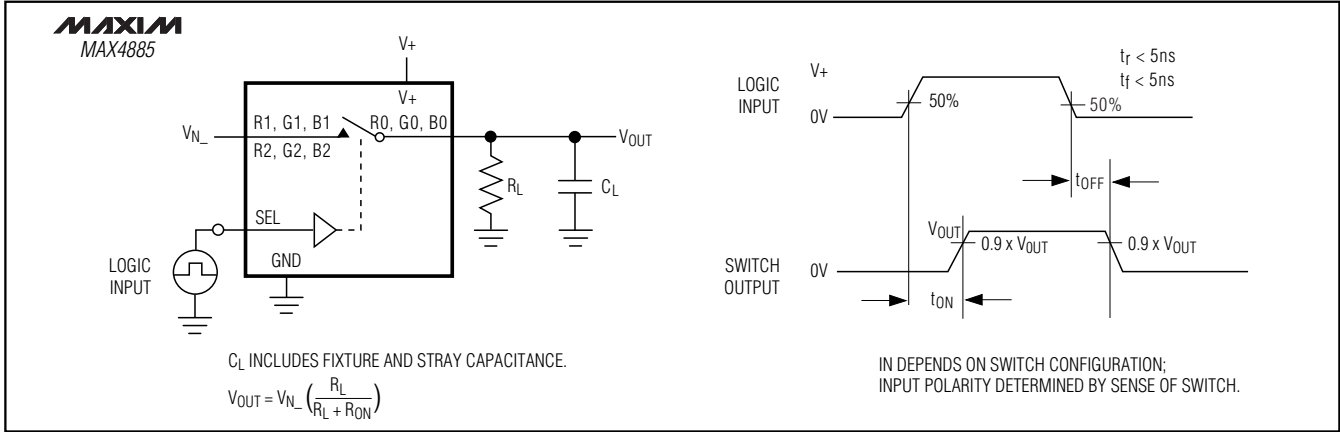


Figure 1. Switching Time

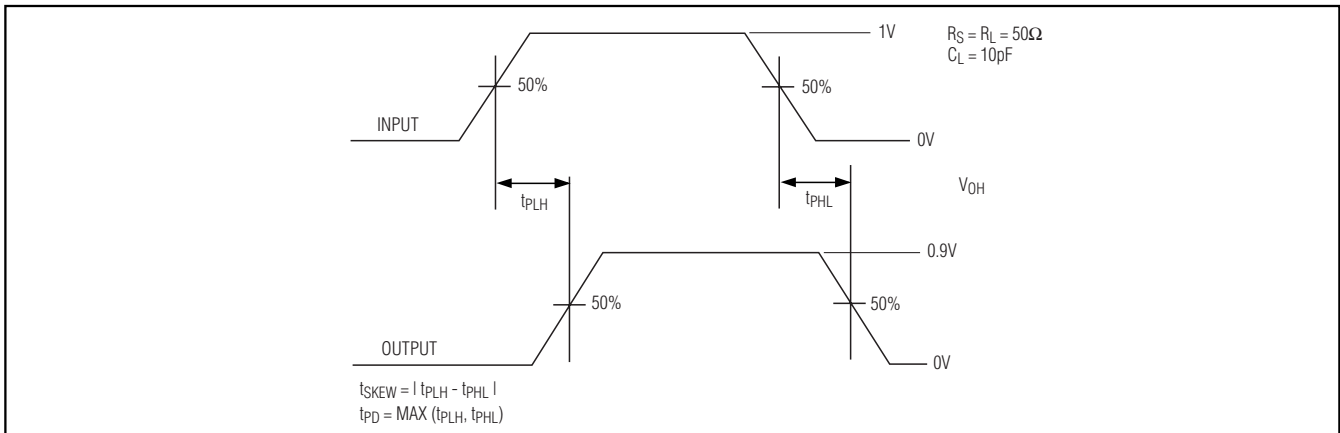


Figure 2. Propagation Delay and Skew Waveforms

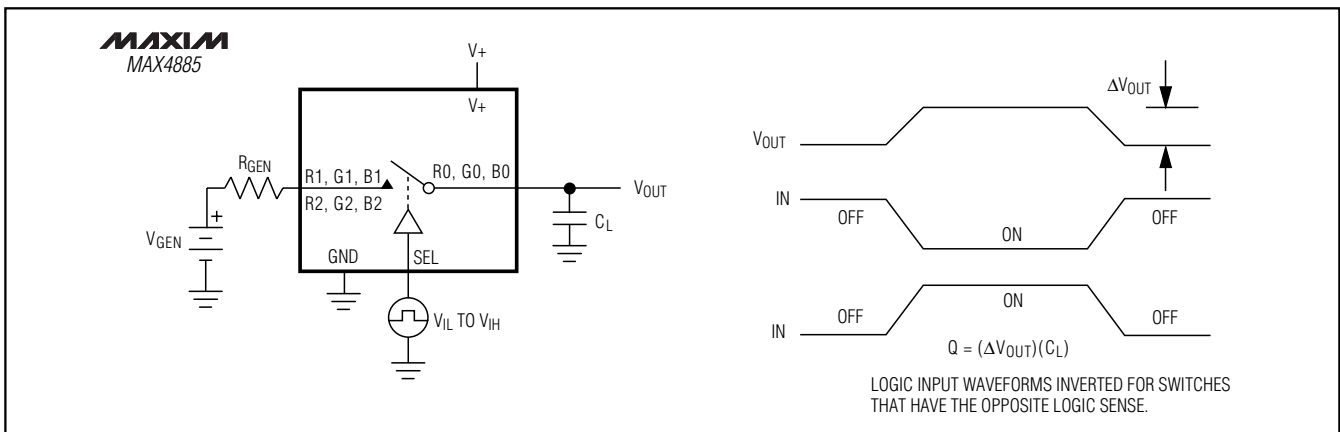


Figure 3. Charge Injection

# Complete VGA 1:2 or 2:1 Multiplexer

## Timing Circuits/Timing Diagrams (continued)

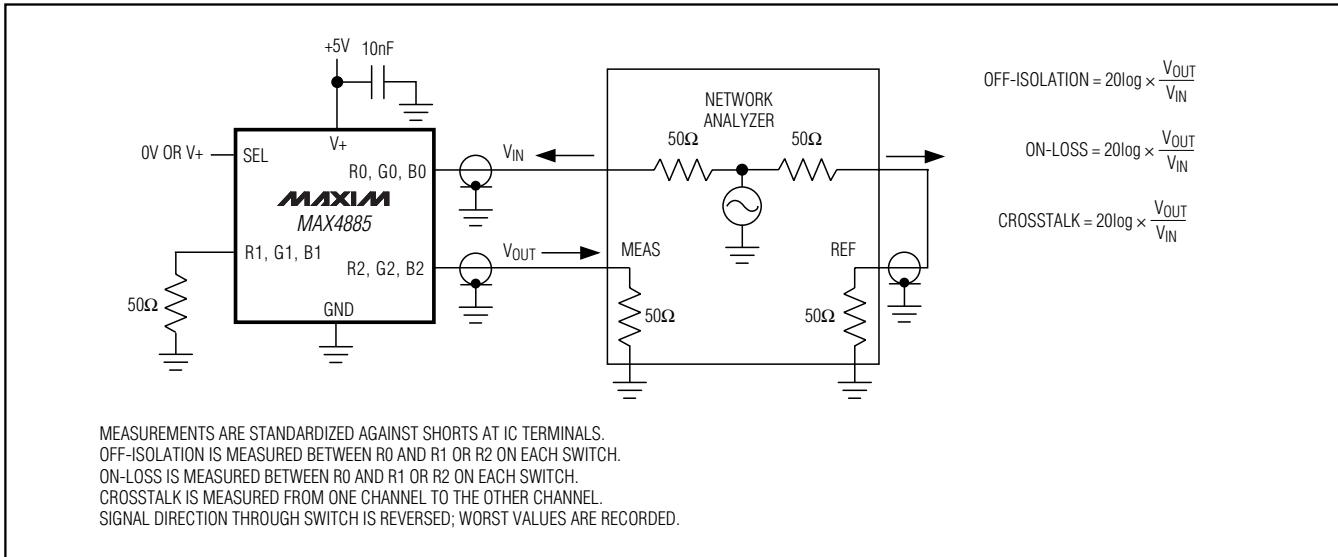


Figure 4. On-Loss, Off-Isolation, and Crosstalk

## Pin Description

| PIN        | NAME                   | FUNCTION   |
|------------|------------------------|--|
| 1          | $\overline{\text{QP}}$ | Charge-Pump Enable, Active Low. Drive $\overline{\text{QP}}$ low for normal operation. Drive $\overline{\text{QP}}$ high to disable the internal charge pump.  |
| 2          | R0                     | RGB Analog I/O   |
| 3          | G0                     | RGB Analog I/O   |
| 4          | B0                     | RGB Analog I/O   |
| 5          | H0                     | Horizontal Sync I/O  |
| 6          | V0                     | Vertical Sync I/O  |
| 7          | DDCA0                  | DDC I/O  |
| 8          | DDCB0                  | DDC I/O  |
| 9          | $\overline{\text{EN}}$ | Enable Input, Active Low. Drive $\overline{\text{EN}}$ low for normal operation. Drive $\overline{\text{EN}}$ high to disable the device. All I/Os are high-impedance and charge pump is off when the device is disabled.  |
| 10         | $V_{\text{CL}}$        | DDC Clamp Voltage. Open-drain DDCA_ and DDCB_ outputs are clamped to one diode-drop below $V_{\text{CL}}$ . $+2.7\text{V} < V_{\text{CL}} < V_+$ . Connect $V_{\text{CL}}$ to +3.3V for voltage clamping, or connect to $V_+$ to disable clamping. Bypass $V_{\text{CL}}$ to GND with a 0.1 $\mu\text{F}$ or larger ceramic capacitor. |
| 11, 21, 30 | $V_+$                  | Supply Voltage. $V_+ = +5.0\text{V} \pm 10\%$ . Bypass each to GND with a 0.1 $\mu\text{F}$ or larger ceramic capacitor.   |
| 12, 20, 29 | GND                    | Ground   |
| 13         | DDCA2                  | DDC I/O  |
| 14         | DDCB2                  | DDC I/O  |
| 15         | R2                     | RGB Analog I/O   |
| 16         | G2                     | RGB Analog I/O   |
| 17         | B2                     | RGB Analog I/O   |

# Complete VGA 1:2 or 2:1 Multiplexer

MAX4885

## Pin Description (continued)

| PIN | NAME  | FUNCTION  |
|-----|-------|---|
| 18  | H2    | Horizontal Sync I/O   |
| 19  | V2    | Vertical Sync I/O   |
| 22  | V1    | Vertical Sync I/O   |
| 23  | H1    | Horizontal Sync I/O   |
| 24  | B1    | RGB Analog I/O  |
| 25  | G1    | RGB Analog I/O  |
| 26  | R1    | RGB Analog I/O  |
| 27  | DDCB1 | DDC I/O   |
| 28  | DDCA1 | DDC I/O   |
| 31  | M     | Mode Select. Drive M low for 1:2 multiplexer mode. Drive M high for 2:1 multiplexer mode. See Tables 1, 2, and 3. |
| 32  | SEL   | Select. Logic input for switching RGB, HV, and DDC switches. See Tables 1, 2, and 3.                              |
| EP  | EP    | Exposed Pad. Connect exposed pad to ground.   |

## Detailed Description

The MAX4885 integrates high-bandwidth analog switches and level-translating buffers to implement a complete 1:2 or 2:1 multiplexer for VGA signals. The device provides switching for RGB, HSYNC, VSYNC, and DDC signals. A low-noise charge pump with internal capacitors provides a boosted gate-drive voltage to improve performance of the RGB switches.

The device provides two modes of operation: 1:2 and 2:1. In 1:2 mode (M = 0), the HSYNC and VSYNC inputs feature level-shifting buffers to support TTL output logic levels from low-voltage graphics controllers. These buffered switches may be driven from as little as +2.0V up to +5.5V. In 2:1 mode (M=1), the output buffers for the HSYNC and VSYNC signals are disabled. In both modes, RGB signals are routed with the same high-performance analog switches, and DDC signals are voltage clamped to a diode drop less than V<sub>CL</sub>. Voltage clamping provides protection and compatibility with DDC signals and low-voltage ASICs. In keyboard/video/mouse (KVM) applications, V<sub>CL</sub> is normally set to +5V because low-voltage clamping is not required, as specified by the VESA standard.

Drive  $\overline{\text{EN}}$  logic high to shut down the MAX4885. In shutdown mode, supply current is reduced to 5 $\mu$ A and all switches are high impedance, providing high-signal rejection. The RGB, HSYNC, VSYNC, and DDC switches are ESD protected to  $\pm$ 8kV by the Human Body Model.

Table 1. RGB Truth Table

| $\overline{\text{EN}}$ | SEL | FUNCTION  |
|------------------------|-----|---|
| 0                      | 0   | R0 to R1<br>G0 to G1<br>B0 to B1                                      |
| 0                      | 1   | R0 to R2<br>G0 to G2<br>B0 to B2                                      |
| 1                      | X   | R <sub>-</sub> , B <sub>-</sub> , and G <sub>-</sub> , High Impedance |

X = Don't Care

## RGB Switches

The MAX4885 provides three SPDT high-bandwidth switches to route standard VGA R, G, and B signals (see Table 1). A boosted gate-drive voltage is generated by an internal charge pump to improve performance of the RGB switches. The R, G, and B analog switches are identical, and any of the three switches can be used to route red, green, or blue video signals. The RGB switches function with reduced performance with the charge pump disabled.

## Charge Pump

A low-noise charge pump with internal capacitors provides a doubled voltage for driving the RGB analog switches. Noise voltage from the charge pump is less than 50 $\mu$ V<sub>p-p</sub>. The noise level is more than 80dB below the signal level, making the charge pump suitable for

# Complete VGA 1:2 or 2:1 Multiplexer

standard VGA signals. The charge pump can be disabled to eliminate charge-pump noise; however, RGB switch performance is slightly degraded. Connect  $\overline{QP}$  to ground for normal operation.

## Horizontal/Vertical Sync Multiplexer

### 1:2 Multiplexer Mode

The MAX4885 provides two modes of operation for the HSYNC and VSYNC signals. In 1:2 mode ( $M = 0$ ), the HSYNC/VSYNC inputs are buffered to provide level shifting and drive capability to meet the VESA specification.

### 2:1 Multiplexer Mode

In 2:1 mode ( $M = 1$ ), the HSYNC/VSYNC output buffers are disabled, and switches pass signals directly. The HSYNC and VSYNC switches/buffers are identical, and either input can be used to route HSYNC and VSYNC signals.

## Display Data Channel Multiplexer

The MAX4885 provides two voltage-clamped switches to route DDC signals (see Table 3). Each switch clamps signals to a diode drop less than the voltage applied on  $V_{CL}$ . Supply +3.3V on  $V_{CL}$  to provide voltage clamping for VESA I<sup>2</sup>C-compatible signals. If voltage clamping is not required, connect  $V_{CL}$  to  $V_+$ . The DDCA and DDCB switches are identical, and each switch can be used to route either DDC signal.

## ESD Protection

As with all Maxim devices, ESD-protection structures are incorporated on all pins to protect against electrostatic discharges encountered during handling and assembly. Additionally, the MAX4885 is protected to  $\pm 8\text{kV}$  on RGB, HSYNC, VSYNC, and DDC switches by the Human Body Model (HBM). For optimum ESD performance, bypass each  $V_+$  pin to ground with a  $0.1\mu\text{F}$  or larger ceramic capacitor.

### Human Body Model (HBM)

Several ESD testing standards exist for measuring the robustness of ESD structures. The ESD protection of the MAX4885 is characterized with the Human Body Model. Figure 5 shows the model used to simulate an ESD event resulting from contact with the human body. The model consists of a  $100\text{pF}$  storage capacitor that is charged to a high voltage, then discharged through a  $1.5\text{k}\Omega$  resistor. Figure 6 shows the current waveform when the storage capacitor is discharged into a low impedance.

### ESD Test Conditions

ESD performance depends on a variety of conditions. Please contact Maxim for a reliability report documenting test setup, methodology, and results.

Table 2. HV Truth Table

| $\overline{EN}$ | M | SEL | FUNCTION   |
|-----------------|---|-----|--|
| 0               | 0 | 0   | 1:2 Mode<br>Buffers Enabled<br>H0 to H1<br>V0 to V1  |
| 0               | 0 | 1   | 1:2 Mode<br>Buffers Enabled<br>H0 to H2<br>V0 to V2  |
| 0               | 1 | 0   | 2:1 Mode<br>Buffers Disabled<br>H0 to H1<br>V0 to V1 |
| 0               | 1 | 1   | 2:1 Mode<br>Buffers Disabled<br>H0 to H2<br>V0 to V2 |
| 1               | X | X   | $H_-, V_-$<br>High Impedance                         |

X = Don't Care

Table 3. DDC Truth Table

| $\overline{EN}$ | SEL | FUNCTION                         |
|-----------------|-----|----------------------------------|
| 0               | 0   | DDCA0 to DDCA1<br>DDCB0 to DDCB1 |
| 0               | 1   | DDCA0 to DDCA2<br>DDCB0 to DDCB2 |
| 1               | X   | DDCA_, DDCB_<br>High Impedance   |

X = Don't Care

## Applications Information

### 1:2 Multiplexer for Low-Voltage Graphics Controllers

The MAX4885 provides the level shifting necessary to drive two standard VGA ports from a graphics controller as low as +2.2V. In 1:2 mode, internal buffers drive the HSYNC and VSYNC signals to VGA standard TTL levels. The DDC multiplexer provides level shifting by clamping signals to a diode drop less than  $V_{CL}$  (see the *Typical Operating Circuit*). Connect  $V_{CL}$  to +3.3V for normal operation, or to  $V_+$  to disable voltage clamping for DDC signals.

# Complete VGA 1:2 or 2:1 Multiplexer

**MAX4885**

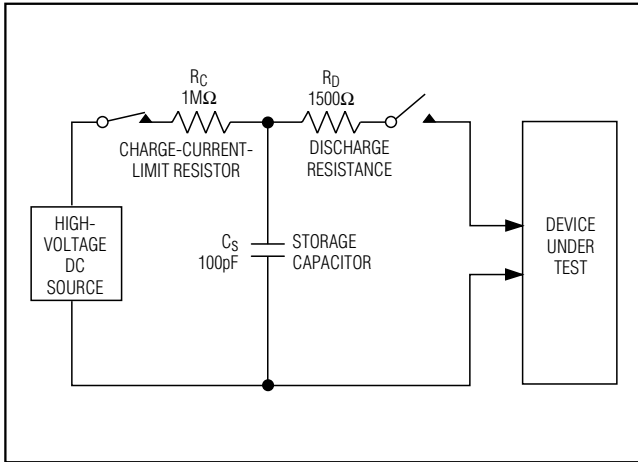


Figure 5. Human Body ESD Test Model

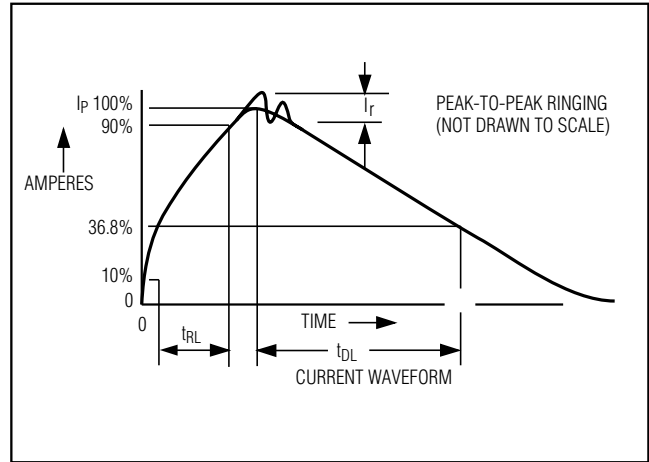


Figure 6. HBM Discharge Current Waveform

## 2:1 Multiplexer

In 2:1 mode, HSYNC and VSYNC buffers are disabled, allowing bidirectional signaling. The DDC multiplexer provides level shifting by clamping signals to a diode drop less than  $V_{CL}$  (see the *Typical Operating Circuit*). Connect  $V_{CL}$  to  $V+$  to disable voltage clamping for DDC signals.

## Power-Supply Decoupling

Bypass each  $V+$  pin and  $V_{CL}$  to ground with a 0.1 $\mu$ F or larger ceramic capacitor as close to the device as possible.

## PC Board Layout

High-speed switches such as the MAX4885 require proper PC board layout for optimum performance. Ensure that impedance-controlled PC board traces for high-speed signals are matched in length and as short as possible. Connect the exposed pad to a solid ground plane.

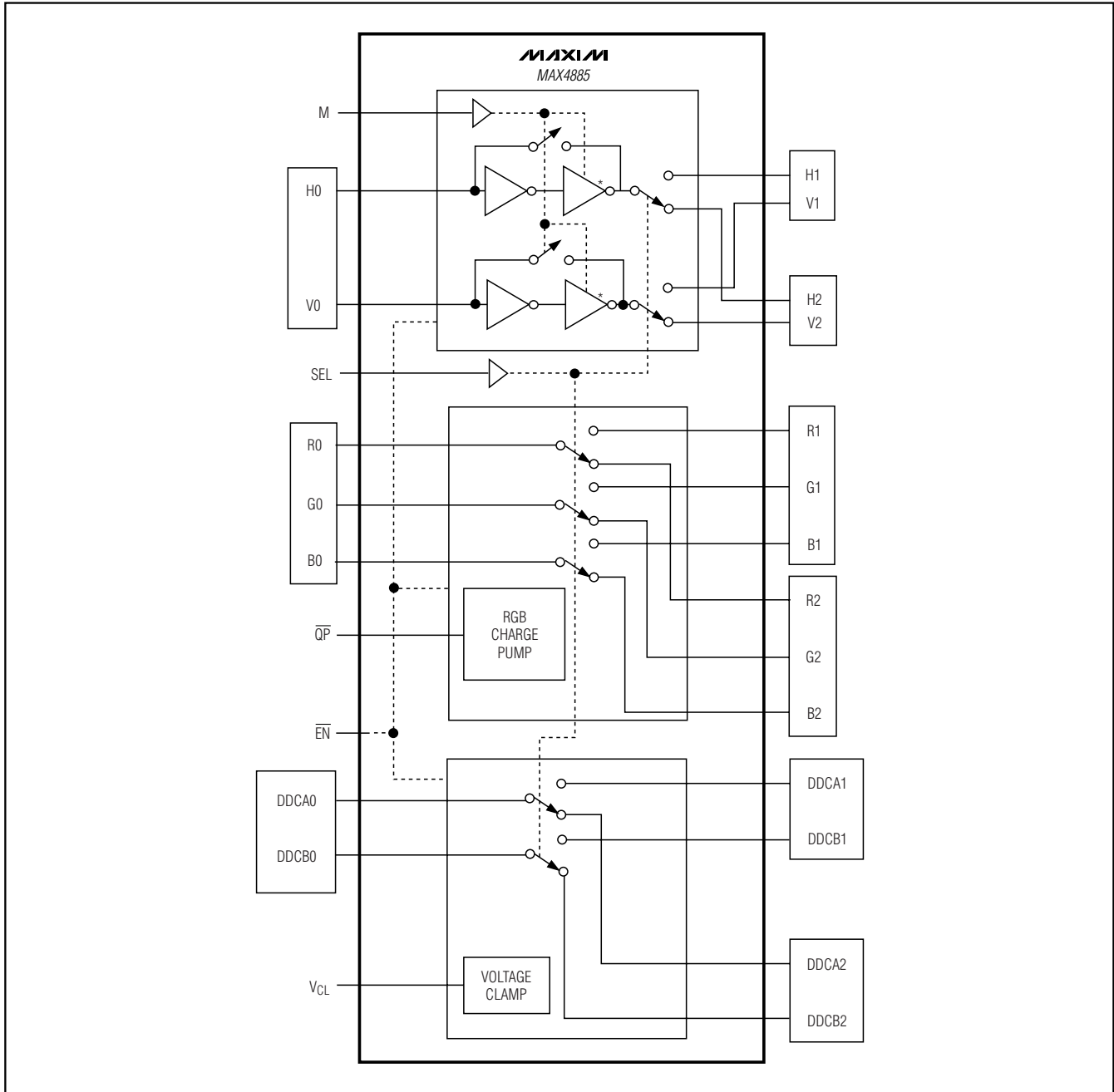
## Chip Information

PROCESS: BiCMOS

CONNECT EXPOSED PAD TO GND

# Complete VGA 1:2 or 2:1 Multiplexer

Functional Diagram

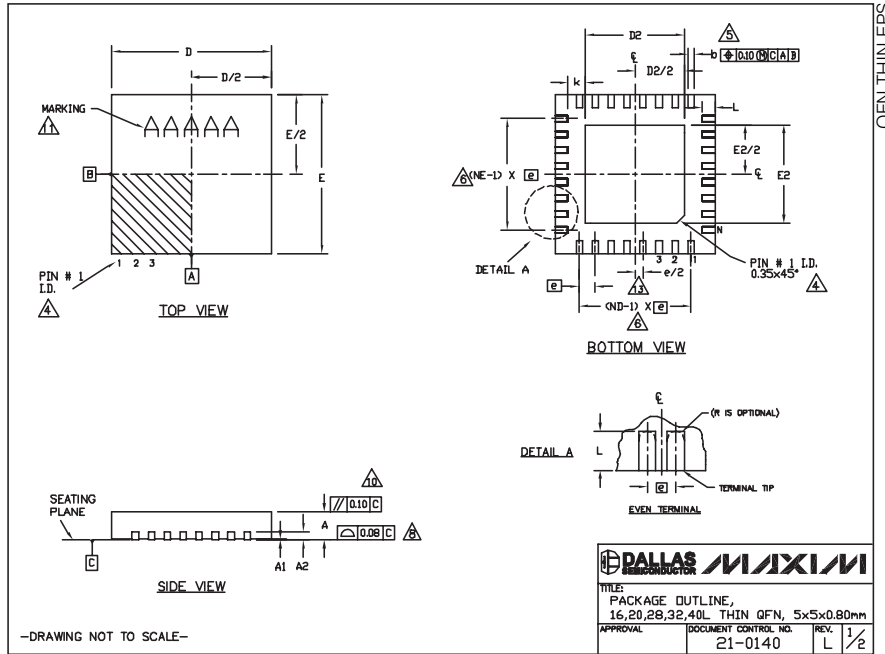


# Complete VGA 1:2 or 2:1 Multiplexer

## Package Information

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information, go to [www.maxim-ic.com/packages](http://www.maxim-ic.com/packages).)

MAX4885



| COMMON DIMENSIONS |           |      |      |           |      |      |           |      |      |           |      |      |
|-------------------|-----------|------|------|-----------|------|------|-----------|------|------|-----------|------|------|
| PKG               | 16L 5x5   |      |      | 20L 5x5   |      |      | 28L 5x5   |      |      | 40L 5x5   |      |      |
| SYMBOL            | MIN.      | NOM. | MAX. | MIN.      | NOM. | MAX. | MIN.      | NOM. | MAX. | MIN.      | NOM. | MAX. |
| A                 | 0.70      | 0.75 | 0.80 | 0.70      | 0.75 | 0.80 | 0.70      | 0.75 | 0.80 | 0.70      | 0.75 | 0.80 |
| A1                | 0         | 0.02 | 0.05 | 0         | 0.02 | 0.05 | 0         | 0.02 | 0.05 | 0         | 0.02 | 0.05 |
| A2                | 0.20 REF. |      |      | 0.20 REF. |      |      | 0.20 REF. |      |      | 0.20 REF. |      |      |
| b                 | 0.25      | 0.30 | 0.35 | 0.25      | 0.30 | 0.35 | 0.20      | 0.25 | 0.30 | 0.15      | 0.20 | 0.25 |
| D                 | 4.90      | 5.00 | 5.10 | 4.90      | 5.00 | 5.10 | 4.90      | 5.00 | 5.10 | 4.90      | 5.00 | 5.10 |
| E                 | 4.90      | 5.00 | 5.10 | 4.90      | 5.00 | 5.10 | 4.90      | 5.00 | 5.10 | 4.90      | 5.00 | 5.10 |
| e                 | 0.80 BSC. |      |      | 0.65 BSC. |      |      | 0.50 BSC. |      |      | 0.40 BSC. |      |      |
| k                 | 0.25      | -    | -    | 0.25      | -    | -    | 0.25      | -    | -    | 0.25      | -    | -    |
| L                 | 0.30      | 0.40 | 0.50 | 0.45      | 0.55 | 0.65 | 0.40      | 0.50 | 0.60 | 0.40      | 0.50 | 0.60 |
| N                 | 16        |      |      | 20        |      |      | 28        |      |      | 32        |      |      |
| ND                | 4         |      |      | 5         |      |      | 7         |      |      | 8         |      |      |
| NE                | 4         |      |      | 5         |      |      | 7         |      |      | 8         |      |      |
| JEDEC             | VHFB      |      |      | WHHC      |      |      | WHHD-1    |      |      | WHHD-2    |      |      |

| EXPOSED PAD VARIATIONS |      |      |      |      |      |      |  |  |
|------------------------|------|------|------|------|------|------|--|--|
| PKG CODES              | D2   |      |      | E2   |      |      |  |  |
|                        | MIN. | NOM. | MAX. | MIN. | NOM. | MAX. |  |  |
| T1655-2                | 3.00 | 3.10 | 3.20 | 3.00 | 3.10 | 3.20 |  |  |
| T1655-3                | 3.00 | 3.10 | 3.20 | 3.00 | 3.10 | 3.20 |  |  |
| T1655N-1               | 3.00 | 3.10 | 3.20 | 3.00 | 3.10 | 3.20 |  |  |
| T2055-3                | 3.00 | 3.10 | 3.20 | 3.00 | 3.10 | 3.20 |  |  |
| T2055-4                | 3.00 | 3.10 | 3.20 | 3.00 | 3.10 | 3.20 |  |  |
| T2055-5                | 3.15 | 3.25 | 3.35 | 3.15 | 3.25 | 3.35 |  |  |
| T2055N-5               | 3.15 | 3.25 | 3.35 | 3.15 | 3.25 | 3.35 |  |  |
| T2855-3                | 3.15 | 3.25 | 3.35 | 3.15 | 3.25 | 3.35 |  |  |
| T2855-4                | 2.60 | 2.70 | 2.80 | 2.60 | 2.70 | 2.80 |  |  |
| T2855-5                | 2.60 | 2.70 | 2.80 | 2.60 | 2.70 | 2.80 |  |  |
| T2855-6                | 3.15 | 3.25 | 3.35 | 3.15 | 3.25 | 3.35 |  |  |
| T2855-7                | 2.60 | 2.70 | 2.80 | 2.60 | 2.70 | 2.80 |  |  |
| T2855-8                | 3.15 | 3.25 | 3.35 | 3.15 | 3.25 | 3.35 |  |  |
| T2855N-1               | 3.15 | 3.25 | 3.35 | 3.15 | 3.25 | 3.35 |  |  |
| T3255-3                | 3.00 | 3.10 | 3.20 | 3.00 | 3.10 | 3.20 |  |  |
| T3255-4                | 3.00 | 3.10 | 3.20 | 3.00 | 3.10 | 3.20 |  |  |
| T3255N-4               | 3.00 | 3.10 | 3.20 | 3.00 | 3.10 | 3.20 |  |  |
| T3255-5                | 3.00 | 3.10 | 3.20 | 3.00 | 3.10 | 3.20 |  |  |
| T3255N-1               | 3.00 | 3.10 | 3.20 | 3.00 | 3.10 | 3.20 |  |  |
| T4055-1                | 3.40 | 3.50 | 3.60 | 3.40 | 3.50 | 3.60 |  |  |
| T4055-2                | 3.40 | 3.50 | 3.60 | 3.40 | 3.50 | 3.60 |  |  |
| T4055N-1               | 3.40 | 3.50 | 3.60 | 3.40 | 3.50 | 3.60 |  |  |

NOTES:

- DIMENSIONING & TOLERANCING CONFORM TO ASME Y14.5M-1994.
- ALL DIMENSIONS ARE IN MILLIMETERS. ANGLES ARE IN DEGREES.
- N IS THE TOTAL NUMBER OF TERMINALS.
- THE TERMINAL #1 IDENTIFIER AND TERMINAL NUMBERING CONVENTION SHALL CONFORM TO JEDEC 95-1 SPP-012. DETAILS OF TERMINAL #1 IDENTIFIER ARE OPTIONAL, BUT MUST BE LOCATED WITHIN THE ZONE INDICATED. THE TERMINAL #1 IDENTIFIER MAY BE EITHER A MOLD OR MARKED FEATURE.
- DIMENSION b APPLIES TO METALLIZED TERMINAL AND IS MEASURED BETWEEN 0.25 mm AND 0.30 mm FROM TERMINAL TIP.
- ND AND NE REFER TO THE NUMBER OF TERMINALS ON EACH D AND E SIDE RESPECTIVELY.
- DEPOPULATION IS POSSIBLE IN A SYMMETRICAL FASHION.
- COPLANARITY APPLIES TO THE EXPOSED HEAT SINK SLUG AS WELL AS THE TERMINALS.
- DRAWING CONFORMS TO JEDEC MO220, EXCEPT EXPOSED PAD DIMENSION FOR T2855-3, T2855-6, T4055-1 AND T4055-2.
- WARPAGE SHALL NOT EXCEED 0.10 mm.
- MARKING IS FOR PACKAGE ORIENTATION REFERENCE ONLY.
- NUMBER OF LEADS SHOWN ARE FOR REFERENCE ONLY.
- LEAD CENTERLINES TO BE AT TRUE POSITION AS DEFINED BY BASIC DIMENSION 'e', ±0.05.
- ALL DIMENSIONS APPLY TO BOTH LEADED AND PUFREE PARTS.

DRAWING NOT TO SCALE-

|  |                                 |              |       |
|--|---------------------------------|--------------|-------|
| <b>DALLAS</b><br>REPRODUCER  |                                 | <b>MAXIM</b> |       |
| TITLE:<br>PACKAGE OUTLINE,<br>16,20,28,32,40L THIN QFN, 5x5x0.80mm |                                 |              |       |
| APPROVAL   | DOCUMENT CONTROL NO.<br>21-0140 | REV.         | L 1/2 |

Maxim cannot assume responsibility for use of any circuitry other than circuitry entirely embodied in a Maxim product. No circuit patent licenses are implied. Maxim reserves the right to change the circuitry and specifications without notice at any time.

Maxim Integrated Products, 120 San Gabriel Drive, Sunnyvale, CA 94086 408-737-7600 13

## Looking for pricing, stock, or lifecycle information?

Click below to explore more details on WIN SOURCE:

 [View MAX4885ETJ+ on WIN SOURCE](#)

 [Maxim Integrated Information](#)

## Optimize Your Supply Chain with WIN SOURCE Solutions

-  Global Sourcing Solution
-  Obsolete Management
-  Cost Control Management
-  Shortage Management
-  Alternative Solution
-  Excess Inventory Management