THE DATASHEET OF

M48T129V-85PM1

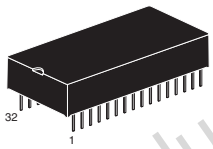
M48T129Y
M48T129V

5.0 or 3.3 V, 1 Mbit (128 Kbit x 8) TIMEKEEPER® SRAM

Not recommended for new design

Features

- Integrated, ultra low power SRAM, real-time clock, power-fail control circuit, battery, and crystal
- BCD coded century, year, month, day, date, hours, minutes, and seconds
- Battery low warning flag
- Automatic power-fail chip deselect and WRITE protection
- Two WRITE protect voltages:
  (V_{PFD} = power-fail deselect voltage)
  - M48T129Y: V_{CC} = 4.5 to 5.5 V;
    4.2 V ≤ V_{PFD} ≤ 4.5 V
  - M48T129V: V_{CC} = 3.0 to 3.6 V;
    2.7 V ≤ V_{PFD} ≤ 3.0 V
- Conventional SRAM operation; unlimited WRITE cycles
- Software controlled clock calibration for high accuracy applications
- 10 years of data retention and clock operation in the absence of power
- Self-contained battery and crystal in DIP package
- Microprocessor power-on reset
  (valid even during battery backup mode)
- Programmable alarm output active in battery backup mode
- RoHS compliant
  - Lead-free second level interconnect



PMDIP32 module

This is information on a product still in production but not recommended for new designs. www.st.com

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1 Description

The M48T129Y/V TIMEKEEPER® RAM is a 128 Kb x 8 non-volatile static RAM and real-time clock with programmable alarms and a watchdog timer. The special DIP package provides a fully integrated battery-backed memory and real-time clock solution. The M48T129Y/V directly replaces industry standard 128 Kb x 8 SRAM. It also provides the non-volatility of Flash without any requirement for special WRITE timing or limitations on the number of WRITEs that can be performed.

The 32-pin, 600 mil DIP hybrid houses a controller chip, SRAM, quartz crystal, and a long-life lithium button cell in a single package.

Figure 1. Logic diagram

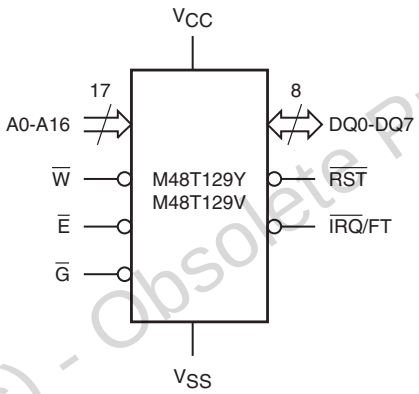


Table 1. Signal names

A0-A16	Address inputs
DQ0-DQ7	Data Inputs / outputs
$\overline{E}$	Chip enable input
$\overline{G}$	Output enable input
$\overline{W}$	WRITE enable input
$\overline{RST}$	Reset output (open drain)
$\overline{IRQ}$/FT	Interrupt / frequency test output (open drain)
V_{CC}	Supply voltage
V_{SS}	Ground

Figure 2. 32-pin module connections

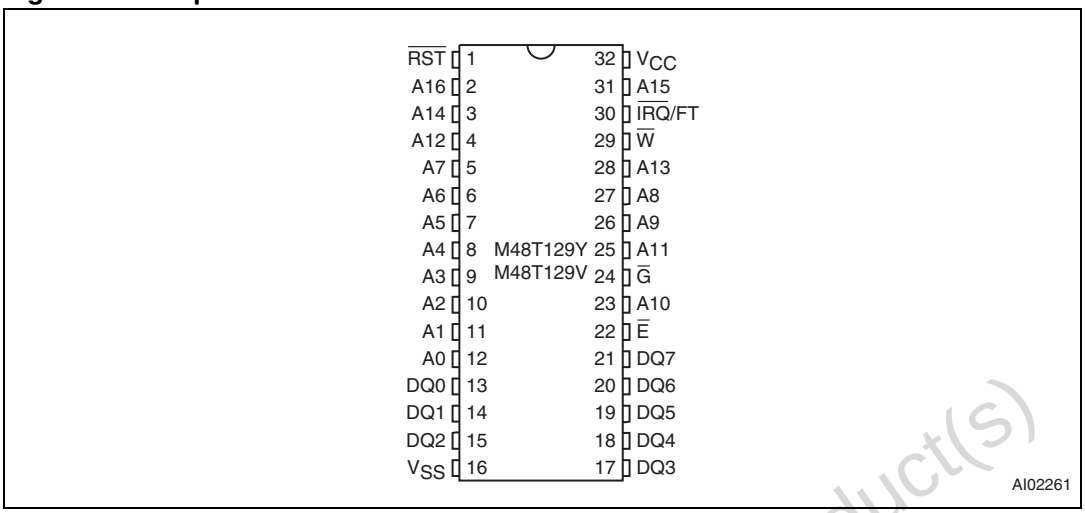
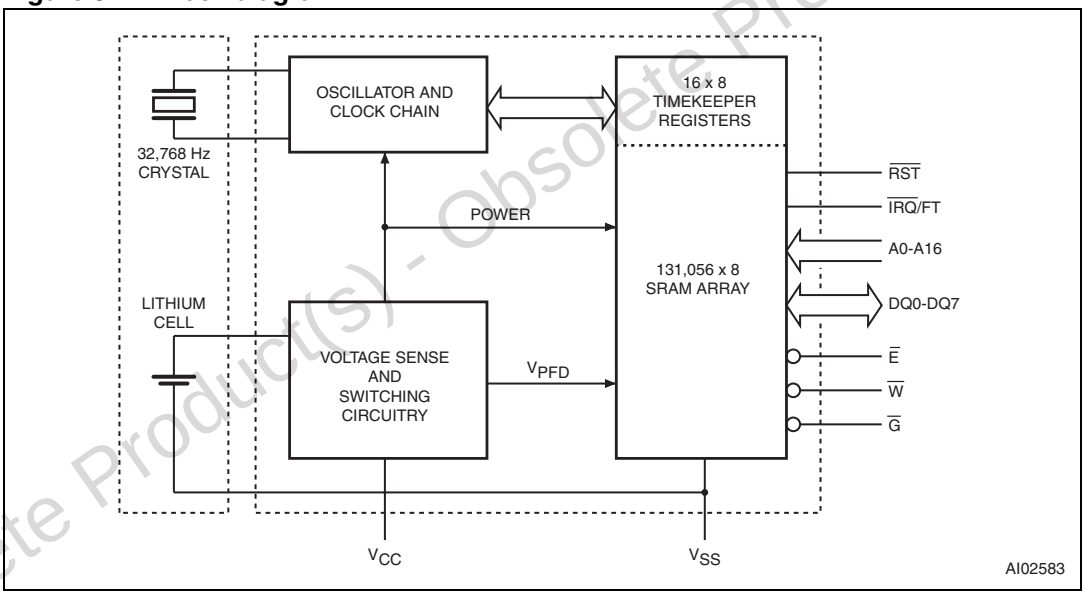


Figure 3. Block diagram



2 Operating modes

Figure 3 on page 6 illustrates the static memory array and the quartz controlled clock oscillator. The clock locations contain the century, year, month, date, day, hour, minute, and second in 24-hour BCD format. Corrections for 28, 29 (leap year - valid until 2100), 30, and 31 day months are made automatically. The nine clock bytes (1FFFFh-1FFF9h and 1FFF1h) are not the actual clock counters, they are memory locations consisting of BiPORT™ READ/WRITE memory cells within the static RAM array.

The M48T129Y/V includes a clock control circuit which updates the clock bytes with current information once per second. The information can be accessed by the user in the same manner as any other location in the static memory array. Byte 1FFF8h is the clock control register. This byte controls user access to the clock information and also stores the clock calibration setting.

Byte 1FFF7h contains the watchdog timer setting. The watchdog timer can generate either a reset or an interrupt, depending on the state of the watchdog steering bit (WDS). Bytes 1FFF6h-1FFF2h include bits that, when programmed, provide for clock alarm functionality. Alarms are activated when the register content matches the month, date, hours, minutes, and seconds of the clock registers. Byte 1FFF1h contains century information. Byte 1FFF0h contains additional flag information pertaining to the watchdog timer, the alarm condition and the battery status. The M48T129Y/V also has its own power-fail detect circuit. This control circuitry constantly monitors the supply voltage for an out of tolerance condition. When V_{CC} is out of tolerance, the circuit write protects the TIMEKEEPER® register data and external SRAM, providing data security in the midst of unpredictable system operation. As V_{CC} falls below battery backup switchover voltage (V_{SO}), the control circuitry automatically switches to the battery, maintaining data and clock operation until valid power is restored.

Table 2. Operating modes

Mode	V_{CC}	E	G	W	DQ0-DQ7	Power
Deselect	4.5 to 5.5V or 3.0 to 3.6V	V_{IH}	X	X	High Z	Standby
WRITE		V_{IL}	X	V_{IL}	D_{IN}	Active
READ		V_{IL}	V_{IL}	V_{IH}	D_{OUT}	Active
READ		V_{IL}	V_{IH}	V_{IH}	High Z	Active
Deselect	V_{SO} to V_{PFD} (min)(1)	X	X	X	High Z	CMOS standby
Deselect	$\leq V_{SO}$(1)	X	X	X	High Z	Battery backup mode

1. See *Table 12 on page 23* for details.

Note: X = V_{IH} or V_{IL}; V_{SO} = battery backup switchover voltage.

2.1 READ mode

The M48T129Y/V is in the READ mode whenever $\overline{W}$ (WRITE enable) is high and $\overline{E}$ (chip enable) is low. The unique address specified by the 17 address inputs defines which one of the 131,072 bytes of data is to be accessed. Valid data will be available at the data I/O pins within t_{AVQV} (address access time) after the last address input signal is stable, providing the $\overline{E}$ and $\overline{G}$ access times are also satisfied. If the $\overline{E}$ and $\overline{G}$ access times are not met, valid data will be available after the latter of the chip enable access times (t_{ELQV}) or output enable access time (t_{GLQV}).

The state of the eight three-state data I/O signals is controlled by $\overline{E}$ and $\overline{G}$. If the outputs are activated before t_{AVQV}, the data lines will be driven to an indeterminate state until t_{AVQV}. If the address inputs are changed while $\overline{E}$ and $\overline{G}$ remain active, output data will remain valid for t_{AXQX} (output data hold time) but will go indeterminate until the next address access.

Figure 4. Chip enable or output enable controlled, READ mode AC waveforms

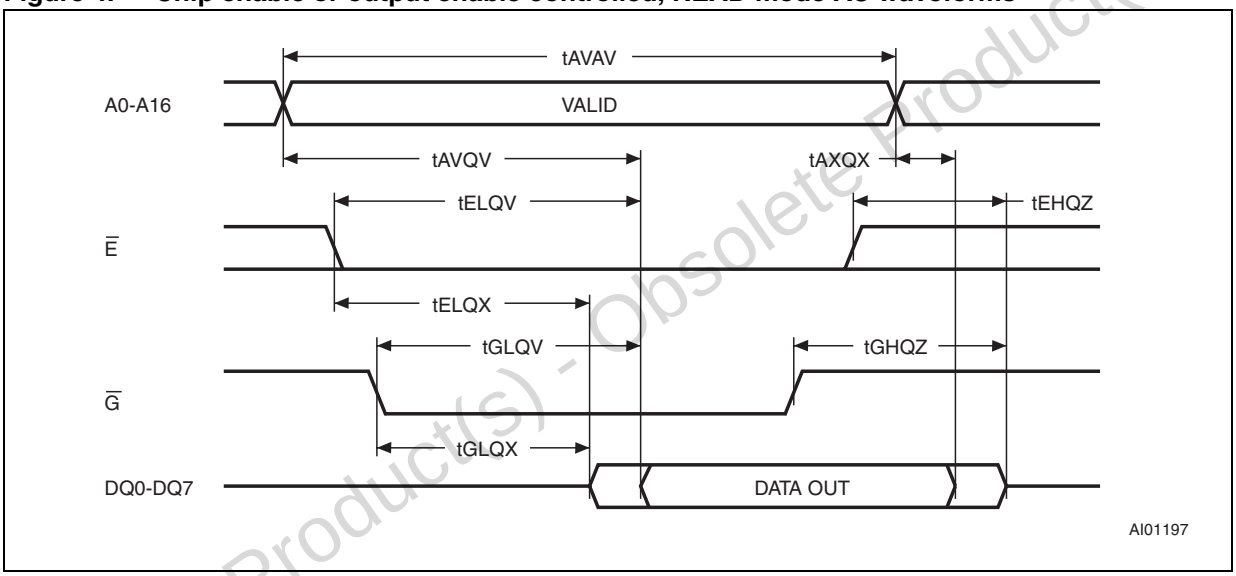


Figure 5. Address controlled, READ mode AC waveforms

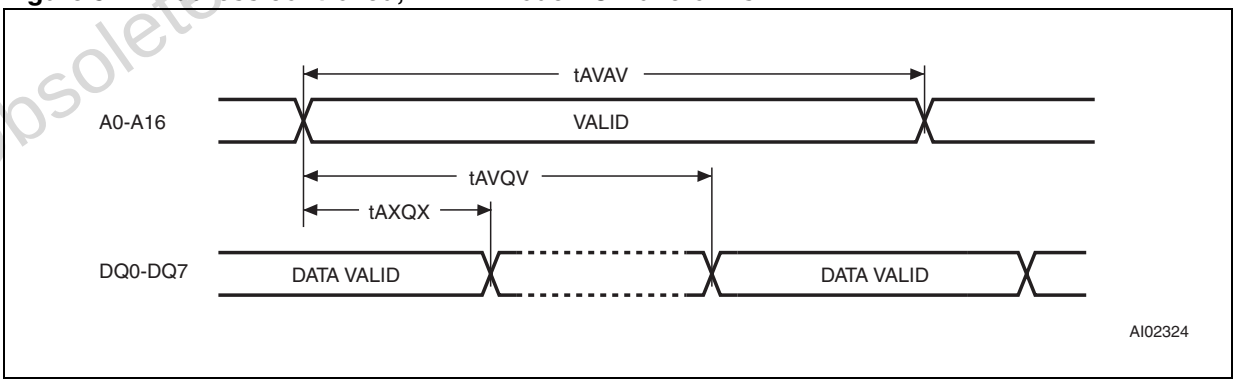


Table 3. READ mode AC characteristics

Symbol	Parameter[1]	M48T129Y		M48T129V		Unit
		–70		–85		
		Min	Max	Min	Max	
t_{AVAV}	READ cycle time	70		85		ns
t_{AVQV}	Address valid to output valid		70		85	ns
t_{ELQV}	Chip enable low to output valid		70		85	ns
t_{GLQV}	Output enable low to output valid		40		55	ns
t_{ELQX}[2]	Chip enable low to output transition	5		5		ns
t_{GLQX}[2]	Output enable low to output transition	5		5		ns
t_{EHQZ}[2]	Chip enable high to output Hi-Z		25		30	ns
t_{GHQZ}[2]	Output enable high to output Hi-Z		25		30	ns
t_{AXQX}	Address transition to output transition	5		5		ns

1. Valid for ambient operating temperature: T_A = 0 to 70 °C; V_{CC} = 4.5 to 5.5 V or 3.0 to 3.6 V (except where noted).
2. C_L = 5 pF.

2.2 WRITE mode

The M48T129Y/V is in the WRITE mode whenever $\overline{W}$ (WRITE enable) and $\overline{E}$ (chip enable) are low state after the address inputs are stable.

The start of a WRITE is referenced from the latter occurring falling edge of $\overline{W}$ or $\overline{E}$. A WRITE is terminated by the earlier rising edge of $\overline{W}$ or $\overline{E}$. The addresses must be held valid throughout the cycle. $\overline{E}$ or $\overline{W}$ must return high for a minimum of t_{EHAX} from chip enable or t_{WHAX} from WRITE Enable prior to the initiation of another READ or WRITE cycle. Data-in must be valid t_{DVWH} prior to the end of WRITE and remain valid for t_{WHDX} afterward. $\overline{G}$ should be kept high during WRITE cycles to avoid bus contention; although, if the output bus has been activated by a low on $\overline{E}$ and $\overline{G}$ a low on $\overline{W}$ will disable the outputs t_{WLQZ} after $\overline{W}$ falls.

Figure 6. WRITE enable controlled, WRITE AC waveforms

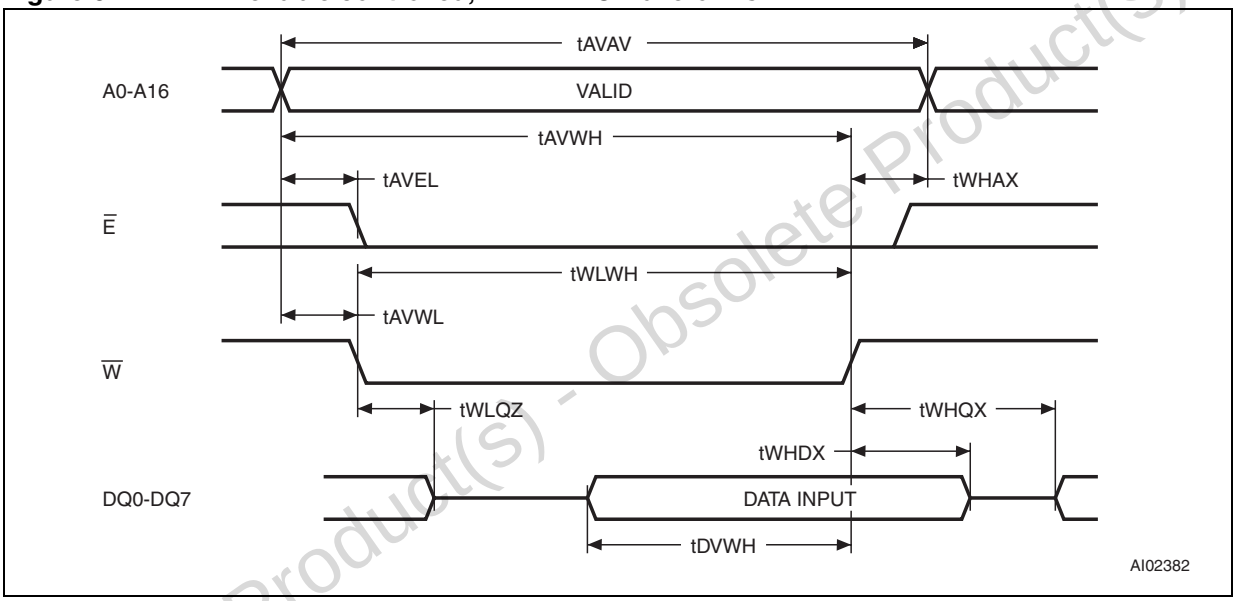


Figure 7. Chip enable controlled, WRITE AC waveforms

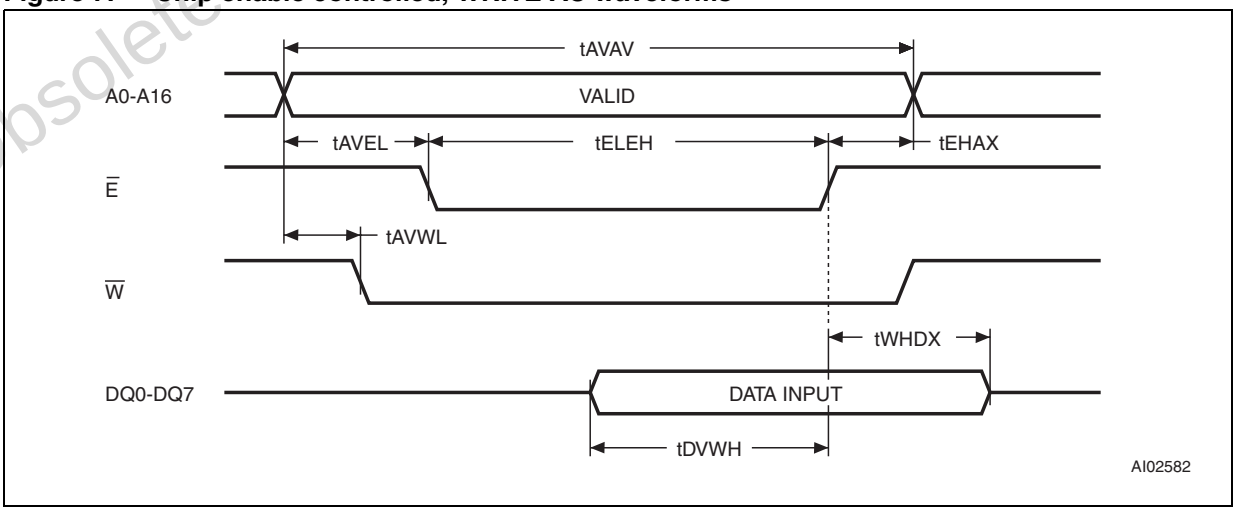


Table 4. WRITE mode AC characteristics

Symbol	Parameter[1]	M48T129Y		M48T129V		Unit
		–70		–85		
		Min	Max	Min	Max	
t_{AVAV}	WRITE cycle time	70		85		ns
t_{AVWL}	Address valid to WRITE enable low	0		0		ns
t_{AVEL}	Address valid to chip enable low	0		0		ns
t_{WLWH}	WRITE enable pulse width	50		60		ns
t_{ELEH}	Chip enable low to chip enable high	55		65		ns
t_{WHAX}	WRITE enable high to address transition	5		5		ns
t_{EHAX}	Chip enable high to address transition	10		15		ns
t_{DVWH}	Input valid to WRITE enable high	30		35		ns
t_{DVEH}	Input valid to chip enable high	30		35		ns
t_{WHDX}	WRITE enable high to input transition	5		5		ns
t_{EHDX}	Chip enable high to input transition	10		15		ns
t_{WLQZ}[2][3]	WRITE enable low to output Hi-Z		25		30	ns
t_{AVWH}	Address valid to WRITE enable high	60		70		ns
t_{AVEH}	Address valid to chip enable high	60		70		ns
t_{WHQX}[2][3]	WRITE enable high to output transition	5		5		ns

1. Valid for ambient operating temperature: T_A = 0 to 70 °C; V_{CC} = 4.5 to 5.5 V or 3.0 to 3.6 V (except where noted).
2. C_L = 5 pF.
3. If $\overline{E}$ goes low simultaneously with $\overline{W}$ going low, the outputs remain in the high impedance state.

2.3 Data retention mode

With valid V_{CC} applied, the M48T129Y/V operates as a conventional BYTEWIDE™ static RAM. Should the supply voltage decay, the RAM will automatically deselect, write protecting itself when V_{CC} falls between V_{PFD} (max), V_{PFD} (min) window. All outputs become high impedance and all inputs are treated as “Don't care.”

Note: A power failure during a WRITE cycle may corrupt data at the current addressed location, but does not jeopardize the rest of the RAM's content. At voltages below V_{PFD} (min), the memory will be in a write protected state, provided the V_{CC} fall time is not less than t_F. The M48T129Y/V may respond to transient noise spikes on V_{CC} that cross into the deselect window during the time the device is sampling V_{CC}. Therefore, decoupling of the power supply lines is recommended.

When V_{CC} drops below V_{SO}, the control circuit switches power to the internal battery, preserving data and powering the clock. The internal energy source will maintain data in the M48T129Y/V for an accumulated period of at least 10 years at room temperature. As system power rises above V_{SO}, the battery is disconnected, and the power supply is switched to external V_{CC}. Deselect continues for t_{REC} after V_{CC} reaches V_{PFD} (max). For a further more detailed review of lifetime calculations, please see application note AN1012.

3 Clock operations

3.1 TIMEKEEPER® registers

The M48T129Y/V offers 16 internal registers which contain TIMEKEEPER®, alarm, watchdog, interrupt, flag, and control data. These registers are memory locations which contain external (user accessible) and internal copies of the data (usually referred to as BiPORT™ TIMEKEEPER cells). The external copies are independent of internal functions except that they are updated periodically by the simultaneous transfer of the incremented internal copy. TIMEKEEPER® and alarm registers store data in BCD.

3.2 Reading the clock

Updates to the TIMEKEEPER® registers should be halted before clock data is read to prevent reading data in transition. The BiPORT™ TIMEKEEPER cells in the RAM array are only data registers and not the actual clock counters, so updating the registers can be halted without disturbing the clock itself.

Updating is halted when a '1' is written to the READ bit, D6 in the control register (1FFF8h). As long as a '1' remains in that position, updating is halted. After a halt is issued, the registers reflect the count; that is, the day, date, and time that were current at the moment the halt command was issued. All of the TIMEKEEPER® registers are updated simultaneously. A halt will not interrupt an update in progress. Updating occurs 1 second after the READ bit is reset to a '0.'

3.3 Setting the clock

Bit D7 of the control register (1FFF8h) is the WRITE bit. Setting the WRITE bit to a '1,' like the READ bit, halts updates to the TIMEKEEPER® registers. The user can then load them with the correct day, date, and time data in 24-hour BCD format (see *Table 5 on page 13*).

Resetting the WRITE bit to a '0' then transfers the values of all time registers (1FFFFh-1FFF9h, 1FFF1h) to the actual TIMEKEEPER® counters and allows normal operation to resume. After the WRITE bit is reset, the next clock update will occur approximately one second later.

Note: Upon power-up following a power failure, both the WRITE bit and the READ bit will be reset to '0.'

3.4 Stopping and starting the oscillator

The oscillator may be stopped at any time. If the device is going to spend a significant amount of time on the shelf, the oscillator can be turned off to minimize current drain on the battery. The STOP bit is located at bit D7 within 1FFF9h. Setting it to a '1' stops the oscillator. When reset to a '0', the M48T129Y/V oscillator starts within one second.

Note: It is not necessary to set the WRITE bit when setting or resetting the FREQUENCY TEST bit (FT) or the STOP bit (ST).

Table 5. TIMEKEEPER® register map

Address	Data								Function/range BCD format	
	D7	D6	D5	D4	D3	D2	D1	D0		
1FFFFh	10 Years				Year				Year	00-99
1FFFEh	0	0	0	10 M	Month				Month	01-12
1FFFDh	0	0	10 date		Date				Date	01-31
1FFFCh	0	FT	0	0	0	Day of week			Day	01-07
1FFFBh	0	0	10 hours		Hours (24-hour format)				Hours	00-23
1FFFAh	0	10 minutes			Minutes				Minutes	00-59
1FFF9h	ST	10 seconds			Seconds				Seconds	00-59
1FFF8h	W	R	S	Calibration					Control	
1FFF7h	WDS	BMB4	BMB3	BMB2	BMB1	BMB0	RB1	RB0	Watchdog	
1FFF6h	AFE	0	ABE	Al 10M	Alarm month				A month	01-12
1FFF5h	RPT4	RPT5	Al 10 date		Alarm date				Al date	01-31
1FFF4h	RPT3	0	Al 10 hours		Alarm hours				A hours	00-23
1FFF3h	RPT2	Al 10 minutes			Alarm minutes				A min	00-59
1FFF2h	RPT1	Al 10 seconds			Alarm seconds				A sec	00-59
1FFF1h	1000 year				100 year				Century	00-99
1FFF0h	WDF	AF	0	BL	Y	Y	Y	Y	Flag	

Keys:

S = SIGN bit
FT = FREQUENCY TEST bit
R = READ bit
W = WRITE bit
ST = STOP bit
0 = Must be set to '0'
Y = '1' or '0‘
BL = Battery low (read only)
AF = Alarm flag (read only)
WDS = Watchdog steering bit
BMB0-BMB4 = Watchdog multiplier bits
RB0-RB1 = Watchdog resolution bits
AFE = Alarm flag enable
ABE = Alarm in battery backup mode enable
RPT1-RPT5 = Alarm repeat mode bits
WDF = Watchdog flag (read only)

3.5 Calibrating the clock

The M48T129Y/V is driven by a quartz controlled oscillator with a nominal frequency of 32,768 Hz. The devices are factory calibrated at 25 °C and tested for accuracy. Clock accuracy will not exceed 35 ppm (parts per million) oscillator frequency error at 25 °C, which equates to about ±1.53 minutes per month (see *Figure 8 on page 15*). When the calibration circuit is properly employed, accuracy improves to better than +1/–2 ppm at 25 °C. The oscillation rate of crystals changes with temperature. The M48T129Y/V design employs periodic counter correction. The calibration circuit adds or subtracts counts from the oscillator divider circuit at the divide by 256 stage, as shown in *Figure 9 on page 15*.

The number of times pulses are blanked (subtracted, negative calibration) or split (added, positive calibration) depends upon the value loaded into the five calibration bits found in the control register. Adding counts speeds the clock up, subtracting counts slows the clock down. The calibration bits occupy the five lower order bits (D4-D0) in the control register 1FFF8h. These bits can be set to represent any value between 0 and 31 in binary form. Bit D5 is a sign bit; '1' indicates positive calibration, '0' indicates negative calibration. Calibration occurs within a 64 minute cycle. The first 62 minutes in the cycle may, once per minute, have one second either shortened by 128 or lengthened by 256 oscillator cycles.

If a binary '1' is loaded into the register, only the first 2 minutes in the 64 minute cycle will be modified; if a binary 6 is loaded, the first 12 will be affected, and so on. Therefore, each calibration step has the effect of adding 512 or subtracting 256 oscillator cycles for every 125, 829, 120 actual oscillator cycles, that is +4.068 or –2.034 ppm of adjustment per calibration step in the calibration register. Assuming that the oscillator is running at exactly 32,768Hz, each of the 31 increments in the calibration byte would represent +10.7 or –5.35 seconds per month which corresponds to a total range of +5.5 or –2.75 minutes per month. *Figure 9 on page 15* illustrates a TIMEKEEPER® calibration waveform.

Two methods are available for ascertaining how much calibration a given M48T129Y/V may require. The first involves setting the clock, letting it run for a month and comparing it to a known accurate reference and recording deviation over a fixed period of time.

Calibration values, including the number of seconds lost or gained in a given period, can be found in the application note “AN934, Timekeeper calibration.”

This allows the designer to give the end user the ability to calibrate the clock as the environment requires, even if the final product is packaged in a non-user serviceable enclosure. The designer could provide a simple utility that accesses the calibration byte.

The second approach is better suited to a manufacturing environment, and involves the use of the $\overline{\text{IRQ}}$/FT pin. The pin will toggle at 512 Hz, when the stop bit (ST, D7 of 1FFF9h) is '0,' the frequency test bit (FT, D6 of 1FFFCh) is '1,' the alarm flag enable bit (AFE, D7 of 1FFF6h) is '0,' and the watchdog steering bit (WDS, D7 of 1FFF7h) is '1' or the watchdog register (1FFF7h = 0) is reset.

Note: A 4 second settling time must be allowed before reading the 512 Hz output.

Any deviation from 512 Hz indicates the degree and direction of oscillator frequency shift at the test temperature. For example, a reading of 512.010124 Hz would indicate a +20 ppm oscillator frequency error, requiring a –10 (WR001010) to be loaded into the calibration byte for correction. Note that setting or changing the calibration byte does not affect the frequency test output frequency.

The $\overline{\text{IRQ}}$/FT pin is an open drain output which requires a pull-up resistor for proper operation. A 500-10 kΩ resistor is recommended in order to control the rise time. The FT bit is cleared on power-up.

Figure 8. Crystal accuracy across temperature

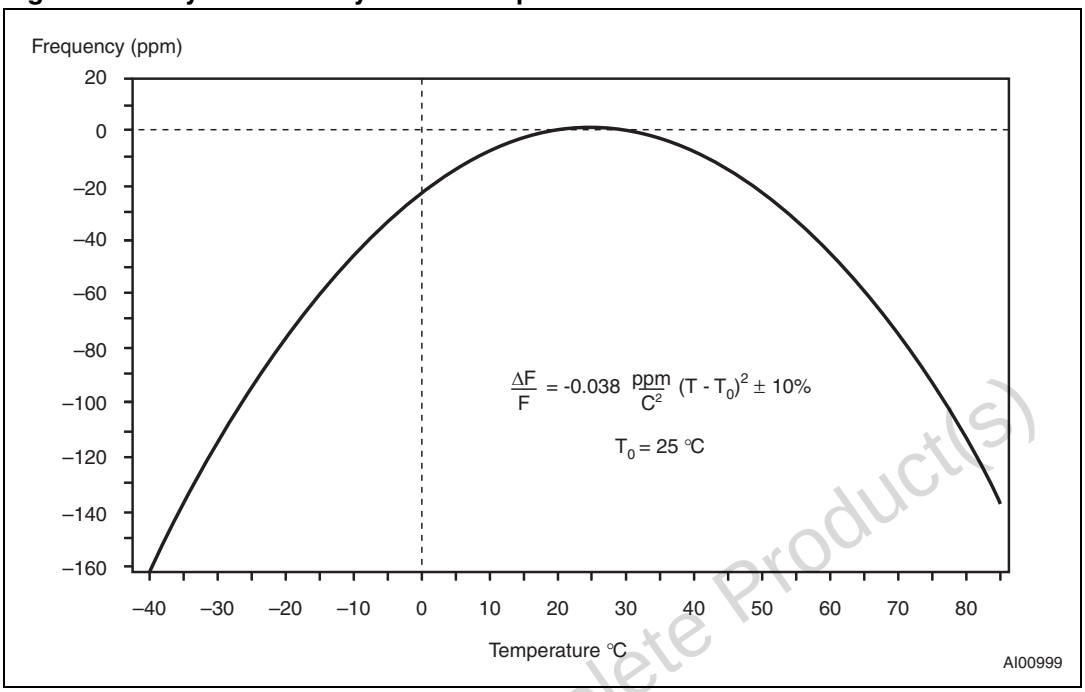
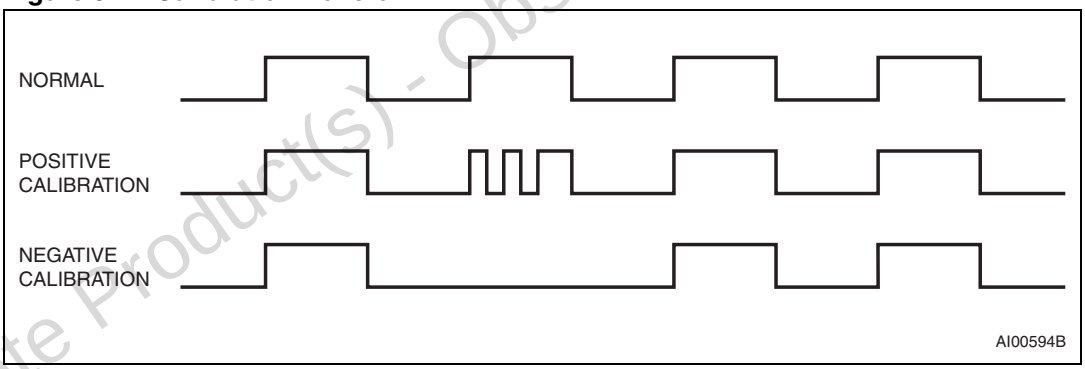


Figure 9. Calibration waveform



3.6 Setting the alarm clock

Registers 1FFF6h-1FFF2h contain the alarm settings. The alarm can be configured to go off at a prescribed time on a specific month, date, hour, minute, or second or repeat every month, day, hour, minute, or second. It can also be programmed to go off while the M48T129Y/V is in the battery back-up to serve as a system wake-up call.

Bits RPT5-RPT1 put the alarm in the repeat mode of operation. *Table 6 on page 16* shows the possible configurations. Codes not listed in the table default to the once per second mode to quickly alert the user of an incorrect alarm setting.

Note: User must transition address (or toggle chip enable) to see flag bit change.

When the clock information matches the alarm clock settings based on the match criteria defined by RPT5-RPT1, the AF (alarm flag) is set. If AFE (alarm flag enable) is also set, the alarm condition activates the $\overline{IRQ}$/FT pin. To disable alarm, write '0' to the alarm date register and RPT1-5. The $\overline{IRQ}$/FT output is cleared by a READ to the flags register as shown in *Figure 10* A subsequent READ of the flags register is necessary to see that the value of the alarm flag has been reset to '0.'

The $\overline{IRQ}$/FT pin can also be activated in the battery back-up mode. The $\overline{IRQ}$/FT will go low if an alarm occurs and both ABE (alarm in battery backup mode enable) and AFE are set. The ABE and AFE bits are reset during power-up, therefore an alarm generated during power-up will only set AF. The user can read the flag register at system boot-up to determine if an alarm was generated while the M48T129Y/V was in the deselect mode during power-up. *Figure 11 on page 17* illustrates the backup mode alarm timing.

Figure 10. Alarm interrupt reset waveform

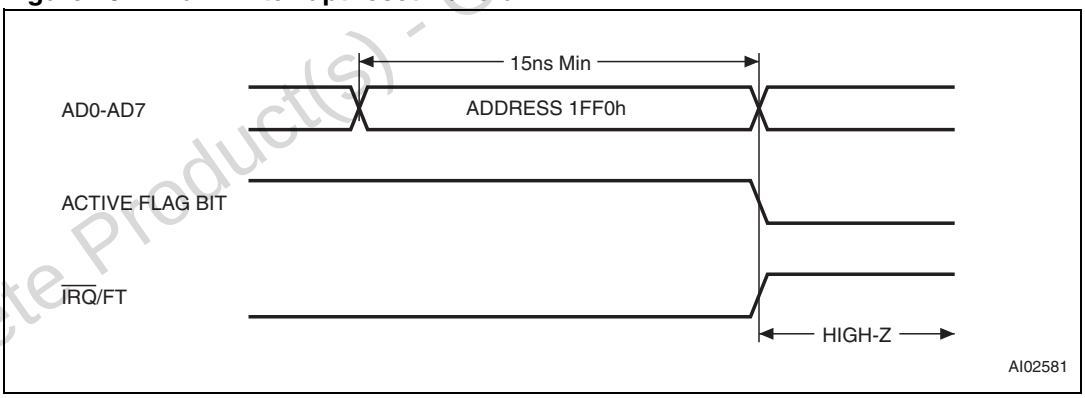
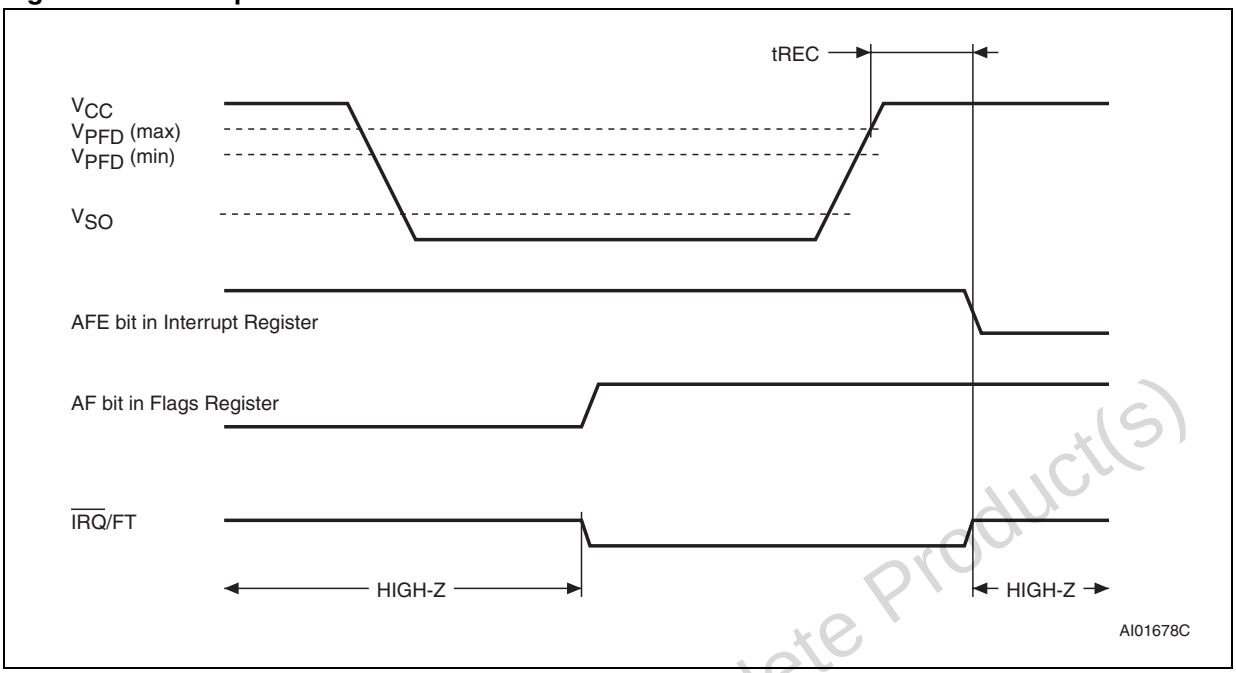


Table 6. Alarm repeat mode

RPT5	RPT4	RPT3	RPT2	RPT1	Alarm activated
1	1	1	1	1	Once per second
1	1	1	1	0	Once per minute
1	1	1	0	0	Once per hour
1	1	0	0	0	Once per day
1	0	0	0	0	Once per month
0	0	0	0	0	Once per year

Figure 11. Backup mode alarm waveforms



3.7 Watchdog timer

The watchdog timer can be used to detect an out-of-control microprocessor. The user programs the watchdog timer by setting the desired amount of time-out into the watchdog register, address 1FFF7h. Bits BMB4-BMB0 store a binary multiplier and the two lower order bits RB1-RB0 select the resolution, where 00 = 1/16 second, 01 = 1/4 second, 10 = 1 second, and 11 = 4 seconds. The amount of time-out is then determined to be the multiplication of the five-bit multiplier value with the resolution. (For example: writing 00001110 in the watchdog register = 3*1 or 3 seconds).

Note: Accuracy of timer is a function of the selected resolution.

If the processor does not reset the timer within the specified period, the M48T129Y/V sets the WDF (watchdog flag) and generates a watchdog interrupt or a microprocessor reset. WDF is reset by reading the flags register (address 1FFF0h). The most significant bit of the watchdog register is the watchdog steering bit (WDS). When set to a '0,' the watchdog will activate the $\overline{IRQ}$/FT pin when timed-out. When WDS is set to a '1,' the watchdog will output a negative pulse on the $\overline{RST}$ pin for 40 to 200 ms. The watchdog register and the FT bit will reset to a '0' at the end of a watchdog time-out when the WDS bit is set to a '1.'

The watchdog timer can be reset by two methods:

1. a transition (high-to-low or low-to-high) can be applied to the watchdog input pin (WDI); or
2. the microprocessor can perform a WRITE of the watchdog register.

The time-out period then starts over. The WDI pin should be tied to V_{SS} if not used. The watchdog will be reset on each transition (edge) seen by the WDI pin. In the order to perform a software reset of the watchdog timer, the original time-out period can be written into the watchdog register, effectively restarting the count-down cycle.

Should the watchdog timer time-out, and the WDS bit is programmed to output an interrupt, a value of “00h” needs to be written to the watchdog register in order to clear the $\overline{IRQ}$/FT pin. This will also disable the watchdog function until it is again programmed correctly. A READ of the flags register will reset the watchdog flag (bit D7; register 1FFF0h).

The watchdog function is automatically disabled upon power-down and the watchdog register is cleared. If the watchdog function is set to output to the $\overline{IRQ}$/FT pin and the frequency test function is activated, the watchdog or alarm function prevails and the frequency test function is denied.

3.8 Power-on reset

The M48T129Y/V continuously monitors V_{CC}. When V_{CC} falls to the power fail detect trip point, the $\overline{RST}$ pulls low (open drain) and remains low on power-up for t_{REC} after V_{CC} passes V_{PFD} (max). The $\overline{RST}$ pin is an open drain output and an appropriate pull-up resistor to V_{CC} should be chosen to control the rise time.

3.9 Battery low warning

The M48T129Y/V automatically performs battery voltage monitoring upon power-up and at factory-programmed time intervals of approximately 24 hours. The battery low (BL) bit, bit D4 of flags register 1FFF0h, will be asserted if the battery voltage is found to be less than approximately 2.5 V.

If a battery low is generated during a power-up sequence, this indicates that the battery is below approximately 2.5 volts and may not be able to maintain data integrity in the SRAM. Data should be considered suspect and verified as correct.

If a battery low indication is generated during the 24-hour interval check, this indicates that the battery is near end of life. However, data is not compromised due to the fact that a nominal V_{CC} is supplied.

The M48T129Y/V only monitors the battery when a nominal V_{CC} is applied to the device. Thus applications which require extensive durations in the battery back-up mode should be powered-up periodically (at least once every few months) in order for this technique to be beneficial. Additionally, if a battery low is indicated, data integrity should be verified upon power-up via a checksum or other technique.

3.10 Initial power-on defaults

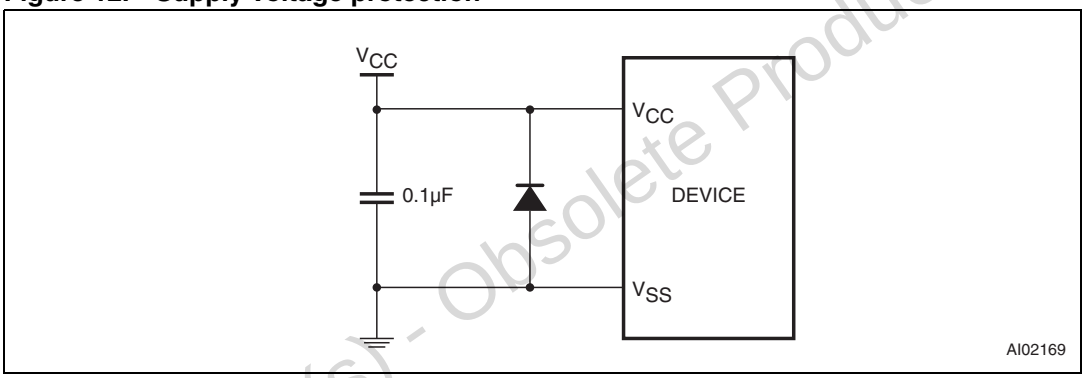
Upon application of power to the device, the following register bits are set to a '0' state: WDS, BMB0-BMB4, RB0,RB1, AFE, ABE, W, R and FT.

3.11 V_{CC} noise and negative going transients

I_{CC} transients, including those produced by output switching, can produce voltage fluctuations, resulting in spikes on the V_{CC} bus. These transients can be reduced if capacitors are used to store energy which stabilizes the V_{CC} bus. The energy stored in the bypass capacitors will be released as low going spikes are generated or energy will be absorbed when overshoots occur. A ceramic bypass capacitor value of 0.1 µF (see *Figure 12*) is recommended in order to provide the needed filtering.

In addition to transients that are caused by normal SRAM operation, power cycling can generate negative voltage spikes on V_{CC} that drive it to values below V_{SS} by as much as one volt. These negative spikes can cause data corruption in the SRAM while in battery backup mode. To protect from these voltage spikes, ST recommends connecting a schottky diode from V_{CC} to V_{SS} (cathode connected to V_{CC}, anode to V_{SS}). (Schottky diode 1N5817 is recommended for through hole and MBRS120T3 is recommended for surface-mount).

Figure 12. Supply voltage protection



4 Maximum ratings

Stressing the device above the rating listed in the absolute maximum ratings table may cause permanent damage to the device. These are stress ratings only and operation of the device at these or any other conditions above those indicated in the operating sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Table 7. Absolute maximum ratings

Symbol	Parameter		Value	Unit
T_A	Ambient operating temperature		0 to 70	°C
T_{STG}	Storage temperature (V_{CC} off, oscillator off)		–40 to 85	°C
T_{SLD} (1)(2)	Lead solder temperature for 10 seconds		260	°C
V_{IO}	Input or output voltages		–0.3 to V_{CC} +0.3	V
V_{CC}	Supply voltage	M48T129Y	–0.3 to 7.0	V
		M48T129V	–0.3 to 4.6	V
I_O	Output current		20	mA
P_D	Power dissipation		1	W

1. Soldering temperature of the IC leads is to not exceed 260 °C for 10 seconds. Furthermore, the devices shall not be exposed to IR reflow nor preheat cycles (as performed as part of wave soldering). ST recommends the devices be hand-soldered or placed in sockets to avoid heat damage to the batteries.
2. For DIP packaged devices, ultrasonic vibrations should not be used for post-solder cleaning to avoid damaging the crystal.

Caution: *Negative undershoots below –0.3 V are not allowed on any pin while in the battery backup mode.*

5 DC and AC parameters

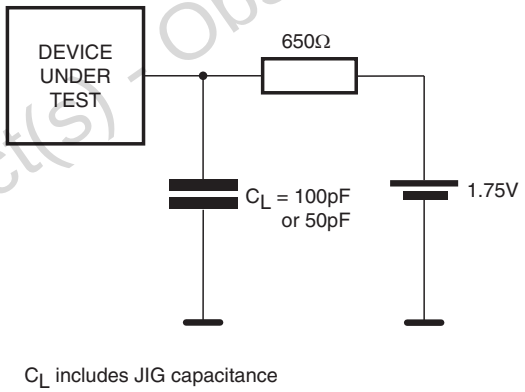
This section summarizes the operating and measurement conditions, as well as the DC and AC characteristics of the device. The parameters in the following DC and AC characteristic tables are derived from tests performed under the measurement conditions listed in the relevant tables. Designers should check that the operating conditions in their projects match the measurement conditions when using the quoted parameters.

Table 8. Operating and AC measurement conditions

Parameter	M48T129Y	M48T129V	Unit
Supply voltage (V_{CC})	4.5 to 5.5	3.0 to 3.6	V
Ambient operating temperature (T_A)	0 to 70	0 to 70	°C
Load capacitance (C_L)	100	50	pF
Input rise and fall times	≤ 5	≤ 5	ns
Input pulse voltages	0 to 3	0 to 3	V
Input and output timing ref. voltages	1.5	1.5	V

Note: Output Hi-Z is defined as the point where data is no longer driven.

Figure 13. AC testing load circuit



C_L includes JIG capacitance

AI01803C

Note: Excluding open drain output pins; 50 pF for M48T129V.

Table 9. Capacitance

Symbol	Parameter[1][2]	Min	Max	Unit
C_{IN}	Input capacitance	-	20	pF
C_{IO}[3]	Input / output capacitance	-	20	pF

1. Effective capacitance measured with power supply at 5 V (M48T129Y) or 3.3 V (M48T129V); sampled only, not 100% tested.
2. At 25 °C, f = 1 MHz.
3. Outputs deselected.

Table 10. DC characteristics

Sym.	Parameter	Test condition(1)	M48T129Y		M48T129V		Unit
			–70		–85		
			Min	Max	Min	Max	
I_{LI}(2)	Input leakage current	$0 V \le V_{IN} \le V_{CC}$		±2		±2	µA
I_{LO}(2)	Output leakage current	$0 V \le V_{OUT} \le V_{CC}$		±2		±2	µA
I_{CC}	Supply current	Outputs open		95		50	mA
I_{CC1}	Supply current (standby) TTL	$\overline{E} = V_{IH}$		8		4	mA
I_{CC2}	Supply current (standby) CMOS	$\overline{E} = V_{CC} - 0.2 V$		4		3	mA
V_{IL}	Input low voltage		–0.3	0.8	–0.3	0.4	V
V_{IH}	Input high voltage		2.2	V_{CC} + 0.3	2.2	V_{CC} + 0.3	V
V_{OL}	Output low voltage	I_{OL} = 2.1 mA		0.4		0.4	V
V_{OH}	Output high voltage	I_{OH} = –1 mA	2.4		2.2		V

1. Valid for ambient operating temperature: T_A = 0 to 70 °C; V_{CC} = 4.5 to 5.5 V or 3.0 to 3.6 V (except where noted).
2. Outputs deselected.

Figure 14. Power down/up mode AC waveforms

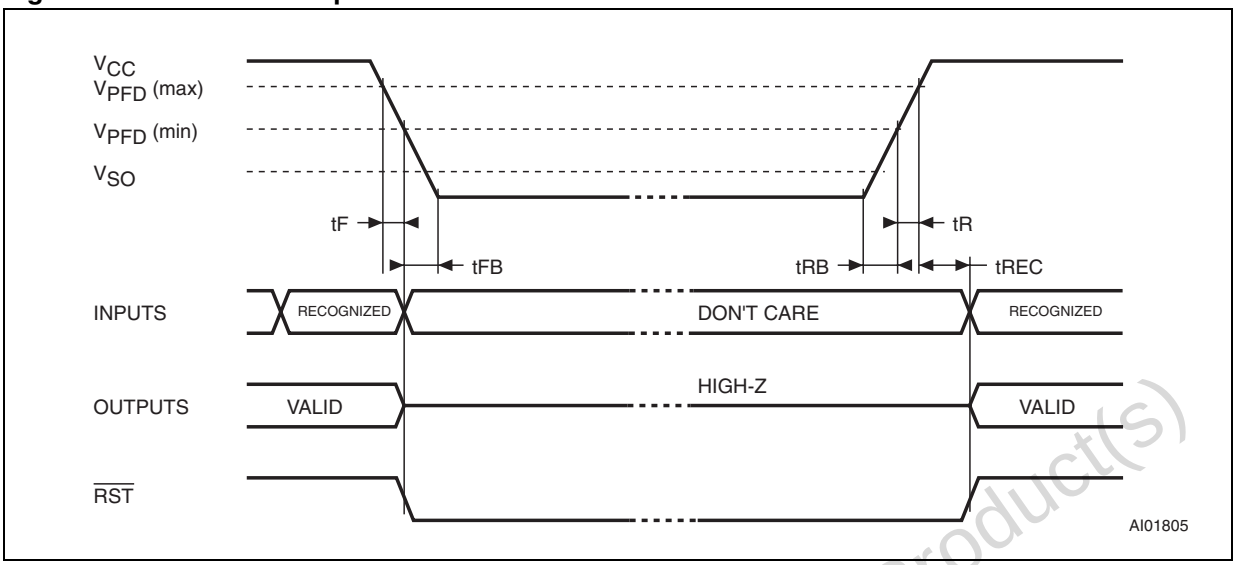


Table 11. Power down/up AC characteristics

Symbol	Parameter[1]		Min	Max	Unit
t_F[2]	V_{PFD} (max) to V_{PFD} (min) V_{CC} fall time		300		µs
t_{FB}[3]	V_{PFD} (min) to V_{SS} V_{CC} fall time	M48T129Y	10		µs
		M48T129V	150		µs
t_R	V_{PFD} (min) to V_{PFD} (max) V_{CC} rise time		0		µs
t_{RB}	V_{SS} to V_{PFD} (min) V_{CC} rise time		1		µs
t_{REC}	V_{PFD} (max) to $\overline{RST}$ high		40	200	ms

1. Valid for ambient operating temperature: T_A = 0 to 70 °C; V_{CC} = 4.5 to 5.5 V or 3.0 to 3.6 V (except where noted).
2. V_{PFD} (max) to V_{PFD} (min) fall time of less than t_F may result in deselection/write protection not occurring until 200 µs after V_{CC} passes V_{PFD} (min).
3. V_{PFD} (min) to V_{SS} fall time of less than t_{FB} may cause corruption of RAM data.

Table 12. Power down/up trip points DC characteristics

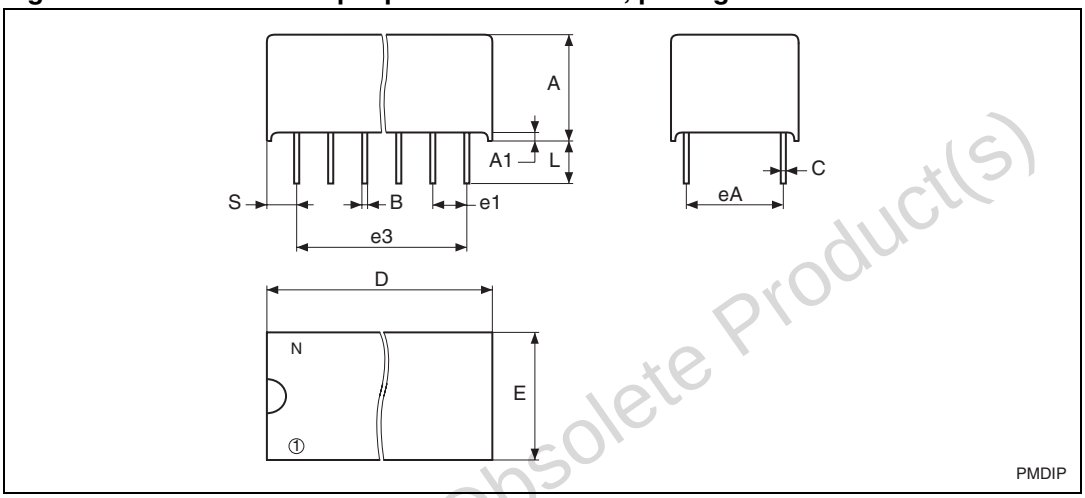
Symbol	Parameter[1][2]		Min	Typ	Max	Unit
V_{PFD}	Power-fail deselect voltage	M48T129Y	4.2	4.35	4.5	V
		M48T129V	2.7	2.9	3.0	V
V_{SO}	Battery backup switchover voltage	M48T129Y		3.0		V
		M48T129V		V_{PFD} –100mV		
t_{DR}[3]	Expected data retention time		10			YEARS

1. All voltages referenced to V_{SS}.
2. Valid for ambient operating temperature: T_A = 0 to 70 °C; V_{CC} = 4.5 to 5.5 V or 3.0 to 3.6 V (except where noted).
3. At 25 °C; V_{CC} = 0 V.

6 Package mechanical data

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: *www.st.com*. ECOPACK® is an ST trademark.

Figure 15. PMDIP32 – 32-pin plastic DIP module, package outline



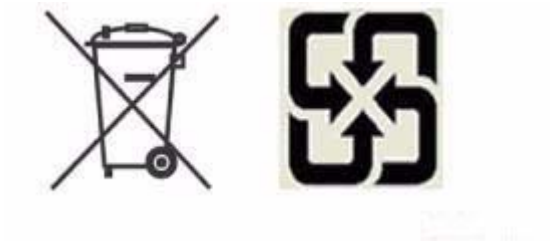
Note: Drawing is not to scale.

Table 13. PMDIP32 – 32-pin plastic DIP module, package mechanical data

Symbol	mm			inches		
	Typ	Min	Max	Typ	Min	Max
A		9.27	9.52		0.365	0.375
A1		0.38	–		0.015	–
B		0.43	0.59		0.017	0.023
C		0.20	0.33		0.008	0.013
D		42.42	43.18		1.670	1.700
E		18.03	18.80		0.710	0.740
e1		2.29	2.79		0.090	0.110
e3	38.1			1.5		
eA		14.99	16.00		0.590	0.630
L		3.05	3.81		0.120	0.150
S		1.91	2.79		0.075	0.110
N	32			32		

7 Environmental information

Figure 16. Recycling symbols



This product contains a non-rechargeable lithium (lithium carbon monofluoride chemistry) button cell battery fully encapsulated in the final product.

Recycle or dispose of batteries in accordance with the battery manufacturer's instructions and local/national disposal and recycling regulations.

8 Part numbering

Table 14. Ordering information scheme

Example: M48T 129Y –70 PM 1

Device type

M48T

Supply voltage and write protect voltage

129Y(1) = V_{CC} = 4.5 to 5.5 V; V_{PFD} = 4.2 to 4.5 V

129V(1) = V_{CC} = 3.0 to 3.6 V; V_{PFD} = 2.7 to 3.0 V

Speed

–70 = 70 ns (for M48T129Y)

–85 = 85 ns (for M48T129V)

Package

PM = PMDIP32

Temperature range

1 = 0 to 70 °C

Shipping method

Blank = ECOPACK® package, tubes

1. Device is not recommended for new design. Contact local ST sales office for availability.

For other options, or for more information on any aspect of this device, please contact the ST sales office nearest you.

9 Revision history

Table 15. Document revision history

Date	Revision	Changes
Apr-2000	1	Chipset data sheet - First Issue
22-Jun-2001	2	Reformatted; added temperature information (*Table 9*, *10*, *3*, *4*, *11*, <Blue>12)
01-Aug-2001	2.1	Added value to AC Testing Load Circuit (*Figure 13*)
06-Aug-2001	2.2	Fix text and table for “Setting the Alarm Clock” (*Table 6*)
13-Aug-2001	2.3	Fix error in “Setting the Alarm Clock” text
07-Nov-2001	2.4	Remove chipset option from ordering information (*Table 14*)
26-Mar-2002	2.5	Replace “chipset” term with “solution,” as well as related changes throughout the document
20-May-2002	2.6	Modify reflow time and temperature footnotes (*Table 7*)
18-Nov-2002	2.7	Modified SMT text (*Figure 2*, *4*)
24-Oct-2003	2.8	Remove references to M68Zxxx (obsolete) parts (*Figure 4)*; corrected footnote (*Table 11*)
22-Feb-2005	3	Reformatted; IR reflow, SO package updates (*Table 7*)
09-Jun-2010	4	Removed SOH44 package, SNAPHAT housing and all references throughout datasheet; updated *Features*, *Section 4*, *Section 6*, *Table 13*, *14*; added *Section 7: Environmental information*; reformatted document.
24-Jun-2011	5	Devices are not recommended for new design (updated cover page, *Table 14*); updated footnote of *Table 7*; updated *Section 7: Environmental information*.

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