

To our customers,

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## Old Company Name in Catalogs and Other Documents

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April 1<sup>st</sup>, 2010  
Renesas Electronics Corporation

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## 1. Overview

The M16C/26A Group (M16C/26A, M16C/26B, M16C/26T) is a single-chip control MCU, fabricated using high-performance silicon gate CMOS technology, embedding the M16C/60 Series CPU core. The M16C/26A Group (M16C/26A, M16C/26B, M16C/26T) is housed in 42-pin and 48-pin plastic molded packages. With a 1M byte address space, this MCU combines advanced instruction manipulation capabilities to process complex instructions by less bytes and execute instructions at higher speed. The M16C/26A Group (M16C/26A, M16C/26B, M16C/26T) has a multiplier and DMAC adequate for office automation, communication devices and industrial equipment, and other high-speed processing applications.

### 1.1 Applications

Audio, cameras, office/communications/portable/ equipment, air-conditioning equipment, home appliances, etc.

## 1.2 Performance Outline

**Table 1.1** and **1.2** outline performance overview of the M16C/26A Group (M16C/26A, M16C/26B, M16C/26T).

**Table 1.1. M16C/26A Group(M16C/26A, M16C/26B, M16C/26T) Performance (48-Pin Package)**

Item		Specification
CPU	Basic instructions	91 instructions
	Minimum instruction execution time	41.7 ns (f(BCLK) = 24MHz <sup>(4)</sup> , Vcc = 4.2 to 5.5 V) (M16C/26B)
		50 ns (f(BCLK) = 20MHz, Vcc = 3.0 to 5.5 V) (M16C/26A, M16C/26B, M16C/26T(T-ver.))
		100 ns (f(BCLK) = 10MHz, Vcc = 2.7 to 5.5 V) (M16C/26A, M16C/26B)
		50 ns (f(BCLK) = 20MHz, Vcc = 4.2 to 5.5 V -40 to 105°C) (M16C/26T(V-ver.))
		62.5 ns (f(BCLK) = 16MHz, Vcc = 4.2 to 5.5 V -40 to 125°C) (M16C/26T(V-ver.))
Operating mode	Single-chip mode	
Address space	1 Mbyte	
Memory capacity	See <b>1.4 Product Information</b>	
Peripheral Function	I/O ports	39 I/O pins
	Multifunction timers	TimerA:16 bits x 5 channels, TimerB:16 bits x 3 channels Three-phase motor control timer
	Serial I/O	2 channels (UART, clock synchronous serial I/O) 1 channel (UART, clock synchronous, I <sup>2</sup> C bus <sup>(1)</sup> , or IEBus <sup>(2)</sup> )
	A/D converter	10 bit A/D Converter : 1 circuit, 12 channels
	DMAC	2 channels
	CRC calculation circuit	1 circuit (CRC-CCITT and CRC-16) with MSB/LSB selectable
	Watchdog timer	15 bits x 1 channel (with prescaler)
	Interrupts	20 internal and 8 external sources, 4 software sources, Interrupt priority level: 7
	Clock generation circuit	4 circuits Main clock oscillation circuit(*), Sub-clock oscillation circuit(*) On-chip oscillator, PLL frequency synthesizer (* )Equipped with a built-in feedback resistor.
	Oscillation stop detection	Main clock oscillation stop, re-oscillation detection function
	Voltage detection circuit	On-chip (M16C/26A, M16C/26B), not on-chip (M16C/26T)
Electrical Characteristics	Power supply voltage	Vcc = 4.2 to 5.5 V (f(BCLK) = 24 MHz) <sup>(4)</sup> (M16C/26B)
		Vcc = 3.0 to 5.5 V (f(BCLK) = 20 MHz) (M16C/26A, M16C/26B)
		Vcc = 2.7 to 5.5 V (f(BCLK) = 10 MHz)
		Vcc = 3.0 to 5.5 V (M16C/26T(T-ver.))
	Vcc = 4.2 to 5.5 V (M16C/26T(V-ver.))	
Power consumption	16 mA (Vcc = 5 V, f(BCLK) = 20 MHz) 25 μA (f(XCIN) = 32 KHz on RAM) 3 μA (Vcc = 3 V, f(XCIN) = 32 KHz, in wait mode) 0.7 μA (Vcc = 3 V, in stop mode)	
Flash Memory Version	Programming /erasure voltage	2.7 to 5.5 V (M16C/26A, M16C/26B) 3.0 to 5.5 V (M16C/26T(T-ver.)) 4.2 to 5.5 V (M16C/26T(V-ver.))
	Programming /erasure endurance	100 times (all area) or 1,000 times (block 0 to 3) / 10,000 times (block A, block B) <sup>(3)</sup>
Operating Ambient Temperature		-20 to 85°C / -40 to 85°C <sup>(3)</sup> (M16C/26A, M16C/26B)
		-40 to 85°C (M16C/26T(T-ver.))
		-40 to 105°C / -40 to 125°C (M16C/26T(V-ver.))
Package	48-pin plastic molded QFP	

**NOTES:**

- I<sup>2</sup>C bus is a trademark of Koninklijke Philips Electronics N. V.
- IEBus is a trademark of NEC Electronics Corporation.
- See **Table 1.7 Product Code** for the program and erase endurance, and operating ambient temperature.
- The PLL frequency synthesizer is used to run the M16C/26B at f(BCLK) = 24 MHz.

**Table 1.2. Performance outline of M16C/26A group (M16C/26A, M16C/26B) (42-pin device)**

	Item	Performance
CPU	Basic instructions	91 instructions
	Minimum instruction execution time	41.7 ns (f(BCLK) = 24 MHz <sup>(4)</sup> , VCC = 4.2 to 5.5 V) (M16C/26B)
		50 ns (f(BCLK) = 20 MHz, VCC = 3.0 to 5.5 V) (M16C/26A, M16C/26B)
		100 ns (f(BCLK) = 10 MHz, VCC = 2.7 to 5.5 V) (M16C/26A, M16C/26B)
	Operation mode	Single-chip mode
Address space	1M byte	
Memory capacity	See <b>1.4 Product Information</b>	
Peripheral function	Port	33 I/O pins
	Multifunction timer	Timer A: 16 bits x 5 channels, Timer B: 16 bits x 3 channels Three-phase motor control timer
	Serial I/O	1 channel (UART, clock synchronous serial I/O)
		1 channel (UART, clock synchronous, I <sup>2</sup> C bus <sup>(1)</sup> , or IEBus <sup>(2)</sup> )
	A/D converter	10 bit A/D converter: 1 circuit, 10 channels
	DMAC	2 channels
	CRC calculation circuit	1 circuits (CRC-CCITT and CRC-16) with MSB/LSB selectable
	Watchdog timer	15 bits x 1 channel (with prescaler)
	Interrupt	18 internal and 8 external sources, 4 software sources, Interrupt priority level: 7
	Clock generation circuit	4 circuits Main clock(*), Sub-clock(*) On-chip oscillator, PLL frequency synthesizer (* )Equipped with a built-in feedback resistor.
Oscillation stop detection		Main clock oscillation stop, re-oscillation detection function
Voltage detection circuit	On-chip	
Electrical Characteristics	Supply voltage	VCC = 4.2 to 5.5 V (f(BCLK) = 24 MHz) <sup>(4)</sup> (M16C/26B)
		VCC = 3.0 to 5.5 V (f(BCLK) = 20 MHz) (M16C/26A, M16C/26B)
VCC = 2.7 to 5.5 V (f(BCLK) = 10 MHz)		
Power Consumption	16 mA (VCC = 5 V, f(BCLK) = 20 MHz)	
	25 μA (f(XCIN) = 32 KHz on RAM)	
	3 μA (VCC = 3 V, f(XCIN) = 32 KHz, in wait mode)	
	0.7 μA (VCC = 3 V, in stop mode)	
Flash memory	Programming/erasure voltage	2.7 to 5.5 V
	Programming/erasure endurance	100 times (all area) or 1,000 times (block 0 to 3) / 10,000 times (block A, block B) <sup>(3)</sup>
Operating Ambient Temperature		-20 to 85°C / -40 to 85°C <sup>(3)</sup>
Package		42-pin plastic molded SSOP

## NOTES:

1. I<sup>2</sup>C bus is a trademark of Koninklijke Philips Electronics N. V.
2. IEBus is a trademark of NEC Electronics Corporation.
3. See **Table 1.7 Product Code** for the program and erase endurance, and operating ambient temperature.
4. The PLL frequency synthesizer is used to run the M16C/26B at f(BCLK) = 24 MHz.

### 1.3 Block Diagram

Figure 1.1 and 1.2 show block diagrams of the M16C/26A Group (M16C/26A, M16C/26B, M16C/26T) 48-pin package and 42-pin package.

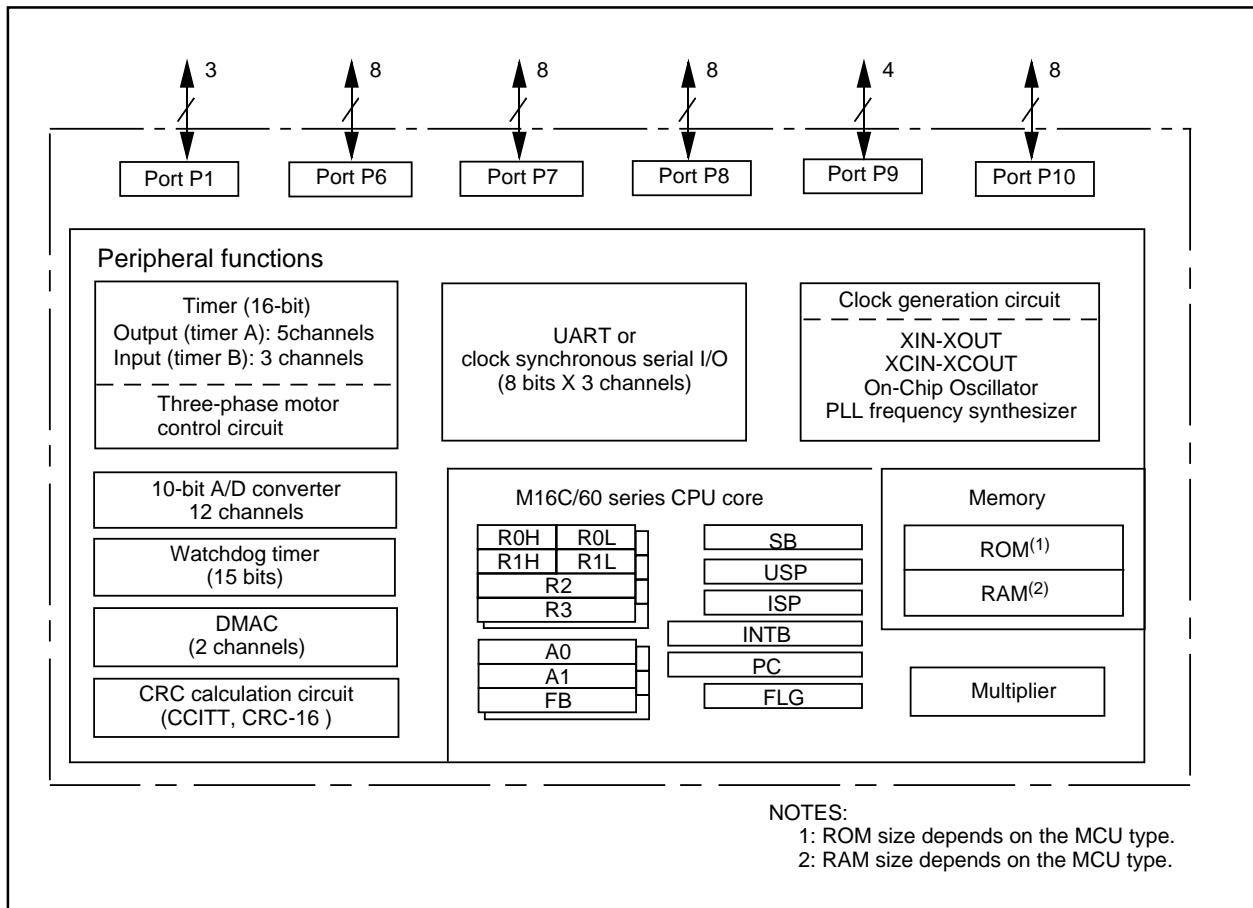


Figure 1.1 Block Diagram(48-pin Package)

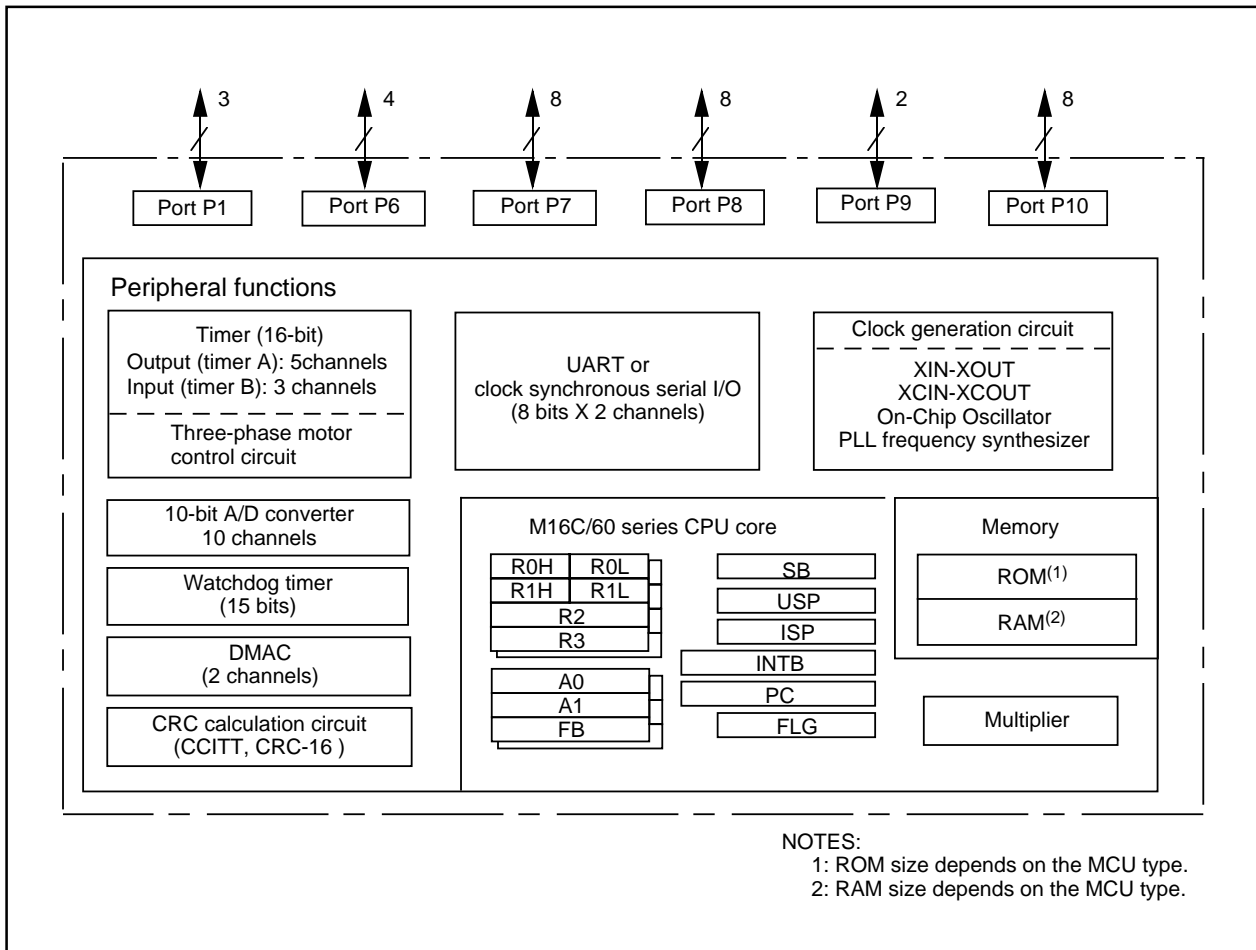


Figure 1.2 Block Diagram( 42-pin Package)

## 1.4 Product List

Tables 1.3 to 1.6 lists product information, Figure 1.3 shows a product numbering system, Table 1.7 lists the product code, and Figure 1.4 shows the marking.

**Table 1.3 M16C/26A**

Current as of Jul., 2006

Type Number	ROM Capacity	RAM Capacity	Package Type	Remarks	Product Code
M30260F3AGP (N)	24K + 4K	1K	PLQP0048KB-A (48P6Q-A)	Flash memory	U3, U5, U7, U9
M30260F6AGP (N)	48K + 4K	2K			
M30260F8AGP (N)	64K + 4K	2K			
M30263F3AFP (N)	24K + 4K	1K	PRSP0042GA-B (42P2R)		U5, U9
M30263F6AFP (N)	48K + 4K	2K			
M30263F8AFP (N)	64K + 4K	2K			
M30260M3A-XXXGP (N)	24K	1K	PLQP0048KB-A (48P6Q-A)	Mask ROM	U3, U5
M30260M6A-XXXGP (N)	48K	2K			
M30260M8A-XXXGP (N)	64K	2K			
M30263M3A-XXXFP (N)	24K	1K	PRSP0042GA-B (42P2R)		U5
M30263M6A-XXXFP (N)	48K	2K			
M30263M8A-XXXFP (N)	64K	2K			

(N): New

**Table 1.4 M16C/26B**

Current as of Jul., 2006

Type Number	ROM Capacity	RAM Capacity	Package Type	Remarks	Product Code
M30260F8BGP (D)	64K + 4K	2K	PLQP0048KB-A (48P6Q-A)	Flash memory	U7
M30263F8BFP (D)	64K + 4K	2K	PRSP0042GA-B (42P2R)		U9

(D): Under development

**Table 1.5 M16C/26T T-ver.**

Current as of Jul., 2006

Type Number	ROM Capacity	RAM Capacity	Package Type	Remarks	Product Code
M30260F3TGP	24K + 4K	1K	PLQP0048KB-A (48P6Q-A)	Flash memory	U3, U7
M30260F6TGP	48K + 4K	2K			
M30260F8TGP	64K + 4K	2K			

NOTE:

1. Please contact Renesas Technology Corp. for details on Mask ROM version.

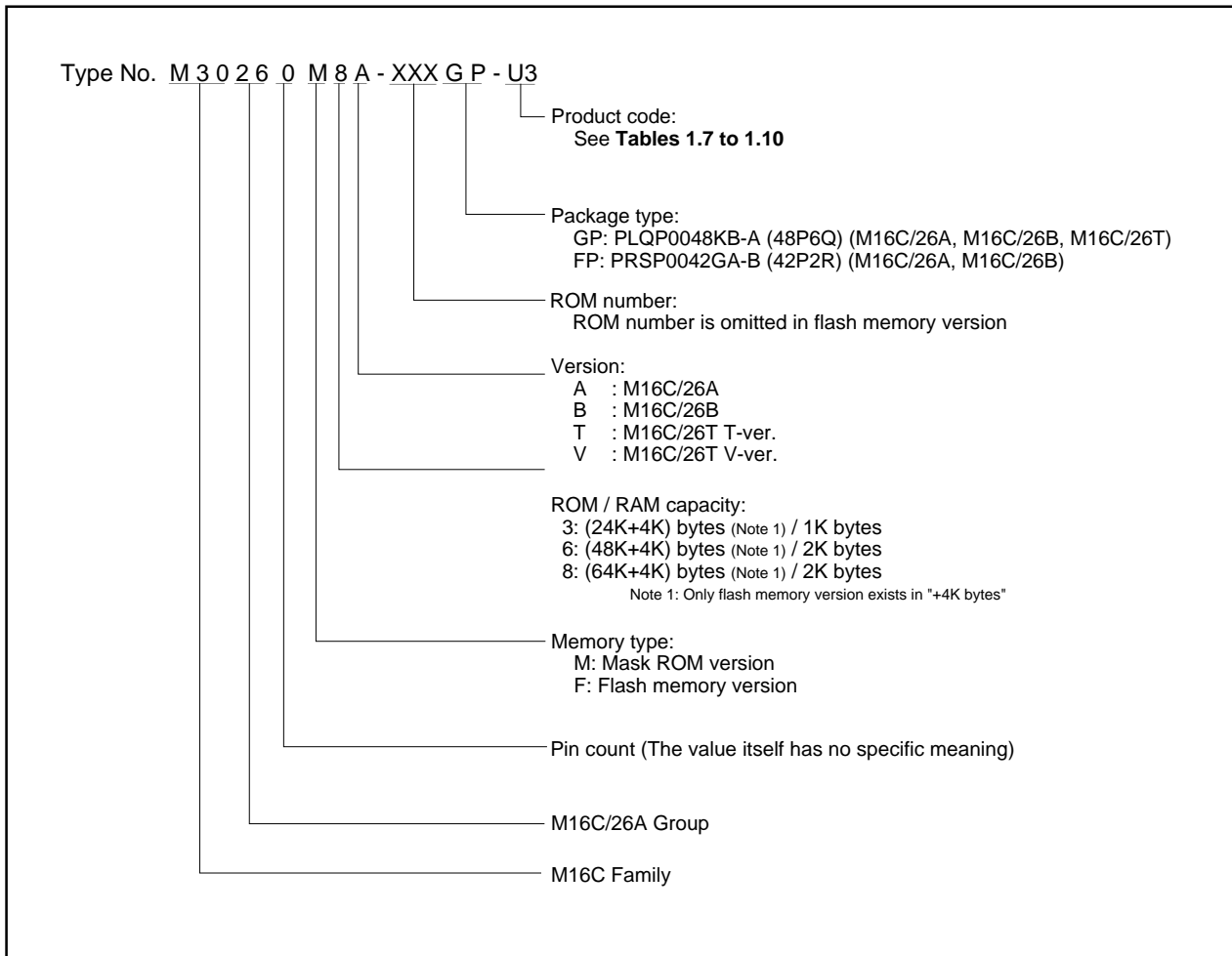
**Table 1.6 M16C/26T V-ver.**

Current as of Jul., 2006

Type Number	ROM Capacity	RAM Capacity	Package	Remarks	Product Code
M30260F3VGP	24K + 4K	1K	PLQP0048KB-A (48P6Q-A)	Flash memory	U3, U7
M30260F6VGP	48K + 4K	2K			
M30260F8VGP	64K + 4K	2K			

NOTE:

1. Please contact Renesas Technology Corp. for details on Mask ROM version.



**Figure 1.3 Product Numbering System**

**Table 1.7 Product Code (Flash Memory Version) - M16C/26A, M16C/26B**

Product Code	Package	Internal ROM (User Program Space)		Internal ROM (Data Space)		Operating Ambient Temperature
		Program and Erase Endurance	Temperature Range	Program and Erase Endurance	Temperature Range	
U3	Lead free	100	0 to 60°C	100	0 to 60°C	-40 to 85°C
U5						-20 to 85°C
U7		1,000		10,000	-40 to 85°C	-40 to 85°C
U9					-20 to 85°C	-20 to 85°C

**Table 1.8 Product Code (Mask ROM Version - M16C/26A)**

Product Code	Package	Operating Ambient Temperature
U3	Lead free	-40°C to 85°C
U5		-20°C to 85°C

## NOTE:

- The lead contained products, D3, D5, D7, and D9 are put together with U3, U5, U7, and U9 respectively. Lead-free products can be mounted by both conventional Sn-Pb paste and Lead-free paste (Sn-Ag-Cu plating).

**Table 1.9 Product Code (Flash Memory Version) - M16C/26T T-ver.**

Product Code	Package	Internal ROM (User Program Space)		Internal ROM (Data Space)		Operating Ambient Temperature
		Programming and erasure endurance	Temperature range	Programming and erasure endurance	Temperature range	
U3	Lead free	100	0°C to 60°C	100	-40°C to 85°C	-40°C to 85°C
U7		1,000		10,000		

**Table 1.10 Product Code (Flash Memory Version) - M16C/26T V-ver.**

Product Code	Package	Internal ROM (User Program Space)		Internal ROM (Data Space)		Operating Ambient Temperature
		Programming and erasure endurance	Temperature range	Programming and erasure endurance	Temperature range	
U3	Lead free	100	0°C to 60°C	100	-40°C to 125°C	-40°C to 125°C
U7		1,000		10,000		

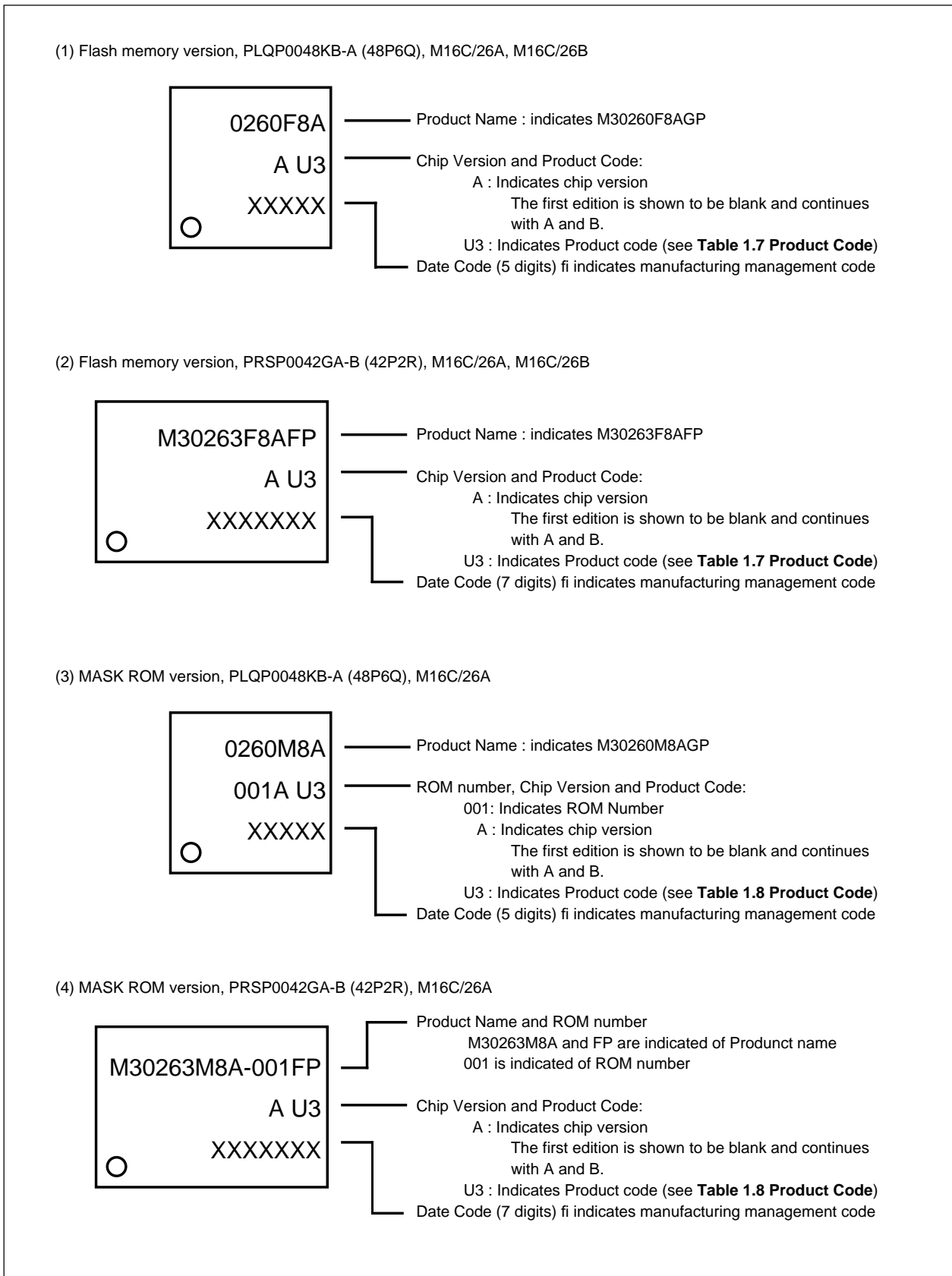
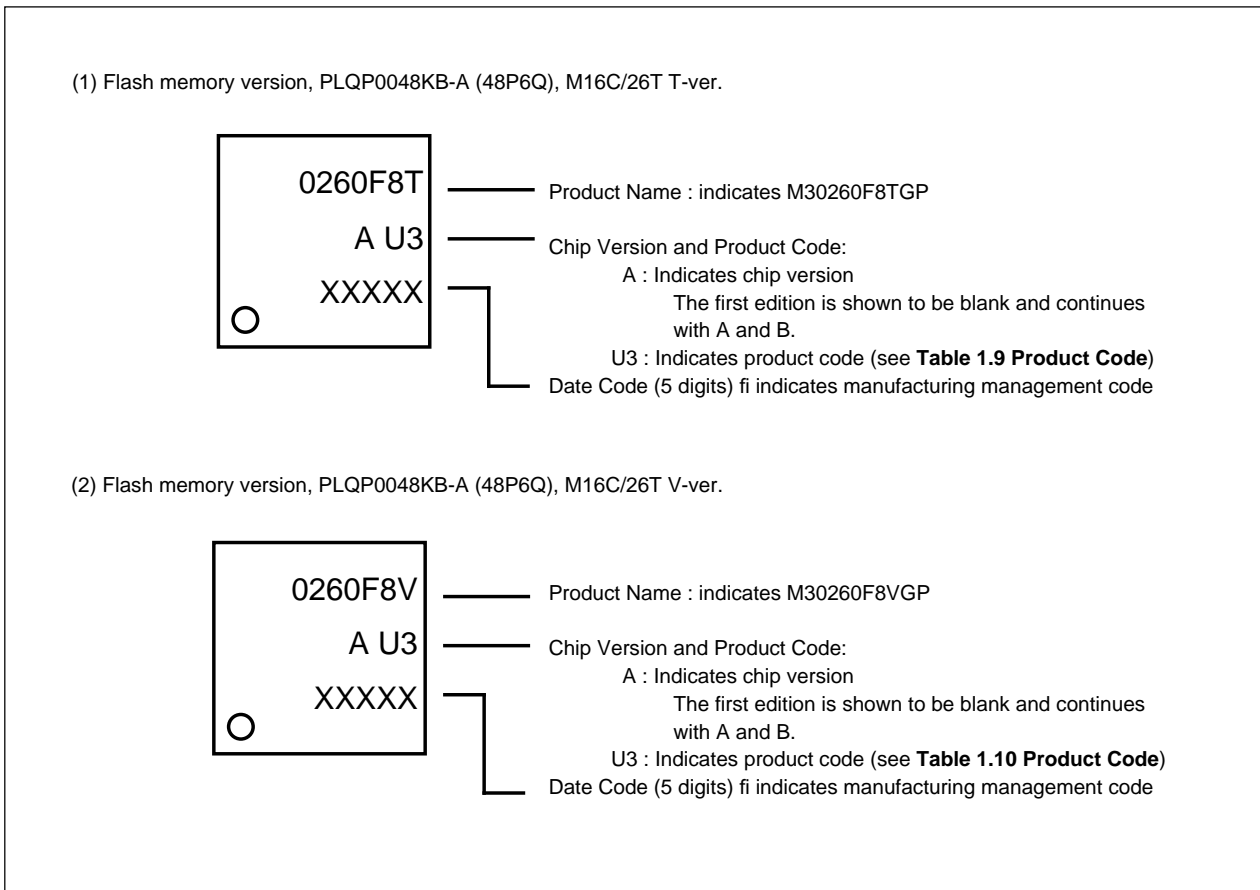


Figure 1.4 Marking Diagram (M16C/26A , M16C/26B)



**Figure 1.5 Marking Diagram (M16C/26T)**

### 1.5 Pin Assignments

Figures 1.6 and 1.7 show the Pin Assignments (top view).

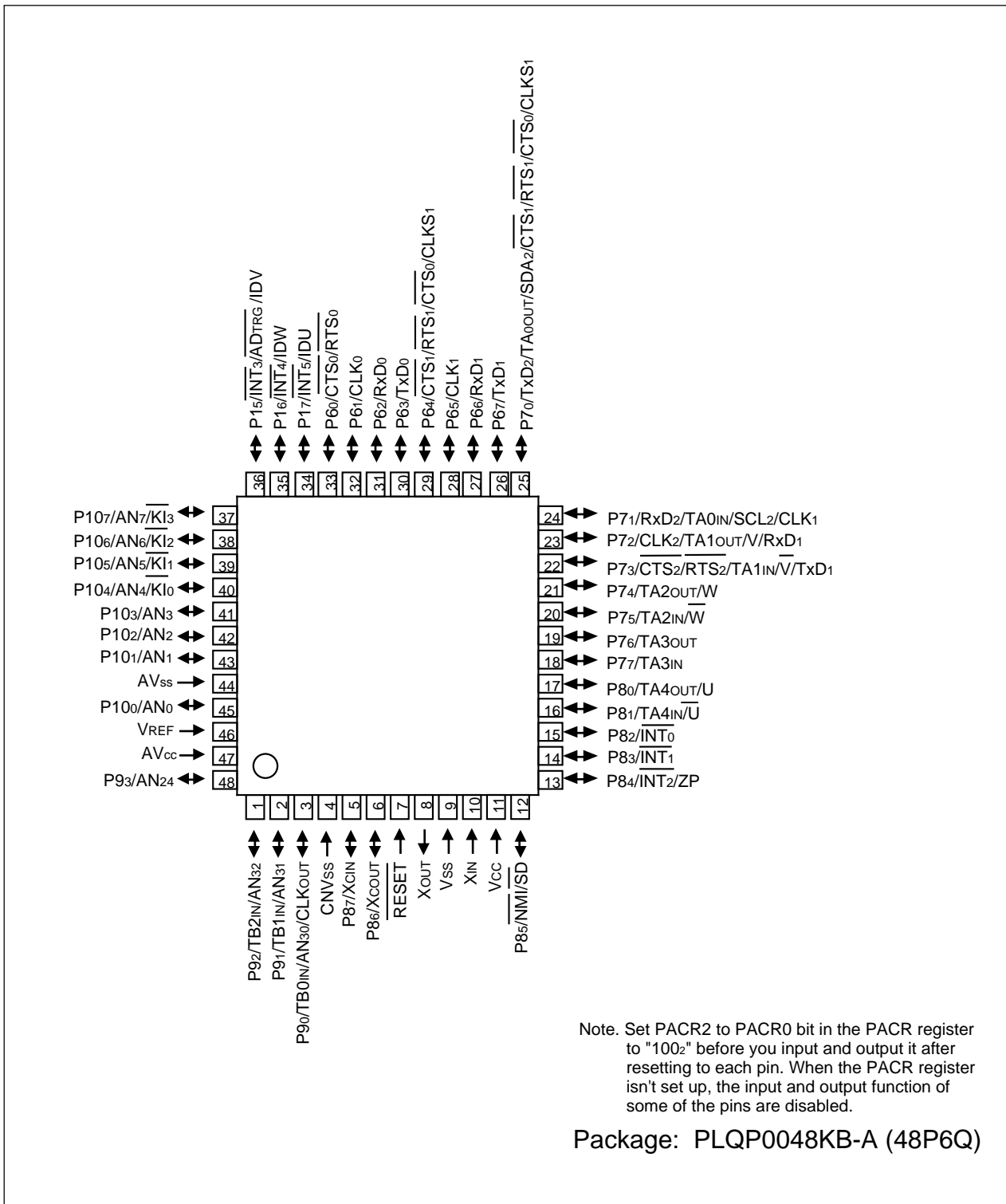


Figure 1.6 Pin Assignment for 48-Pin Package (Top View)

Table 1.11 Pin Characteristics for 48-Pin Package

Pin No.	Control Pin	Port	Interrupt Pin	Timer Pin	UART Pin	Analog Pin
1		P92		TB2IN		AN32
2		P91		TB1IN		AN31
3		P90		TB0IN	CLKOUT	AN30
4	CNVss					
5	XCIN	P87				
6	XcOUT	P86				
7	RESET					
8	XOUT					
9	Vss					
10	XIN					
11	Vcc					
12		P85	$\overline{\text{NMI}}$	$\overline{\text{SD}}$		
13		P84	$\overline{\text{INT}}_2$	ZP		
14		P83	$\overline{\text{INT}}_1$			
15		P82	$\overline{\text{INT}}_0$			
16		P81		TA4IN / $\overline{\text{U}}$		
17		P80		TA4OUT / U		
18		P77		TA3IN		
19		P76		TA3OUT		
20		P75		TA2IN / $\overline{\text{W}}$		
21		P74		TA2OUT / W		
22		P73		TA1IN / $\overline{\text{V}}$	$\overline{\text{CTS}}_2 / \overline{\text{RTS}}_2 / \text{TxD}_1$	
23		P72		TA1OUT / V	CLK2 / $\text{RxD}_1$	
24		P71		TA0IN	$\text{RxD}_2 / \text{SCL}_2 / \text{CLK}_1$	
25		P70		TA0OUT	$\text{TxD}_2 / \text{SDA}_2 / \overline{\text{RTS}}_1 / \overline{\text{CTS}}_1 / \overline{\text{CTS}}_0 / \text{CLKS}_1$	
26		P67			$\text{TxD}_1$	
27		P66			$\text{RxD}_1$	
28		P65			CLK1	
29		P64			$\overline{\text{RTS}}_1 / \overline{\text{CTS}}_1 / \overline{\text{CTS}}_0 / \text{CLKS}_1$	
30		P63			$\text{TxD}_0$	
31		P62			$\text{RxD}_0$	
32		P61			CLK0	
33		P60			$\overline{\text{RTS}}_0 / \overline{\text{CTS}}_0$	
34		P17	$\overline{\text{INT}}_5$	IDU		
35		P16	$\overline{\text{INT}}_4$	IDW		
36		P15	$\overline{\text{INT}}_3$	IDV		ADTRG
37		P107	$\overline{\text{KI}}_3$			AN7
38		P106	$\overline{\text{KI}}_2$			AN6
39		P105	$\overline{\text{KI}}_1$			AN5
40		P104	$\overline{\text{KI}}_0$			AN4
41		P103				AN3
42		P102				AN2
43		P101				AN1
44	AVss					
45		P100				AN0
46	VREF					
47	AVcc					
48		P93				AN24

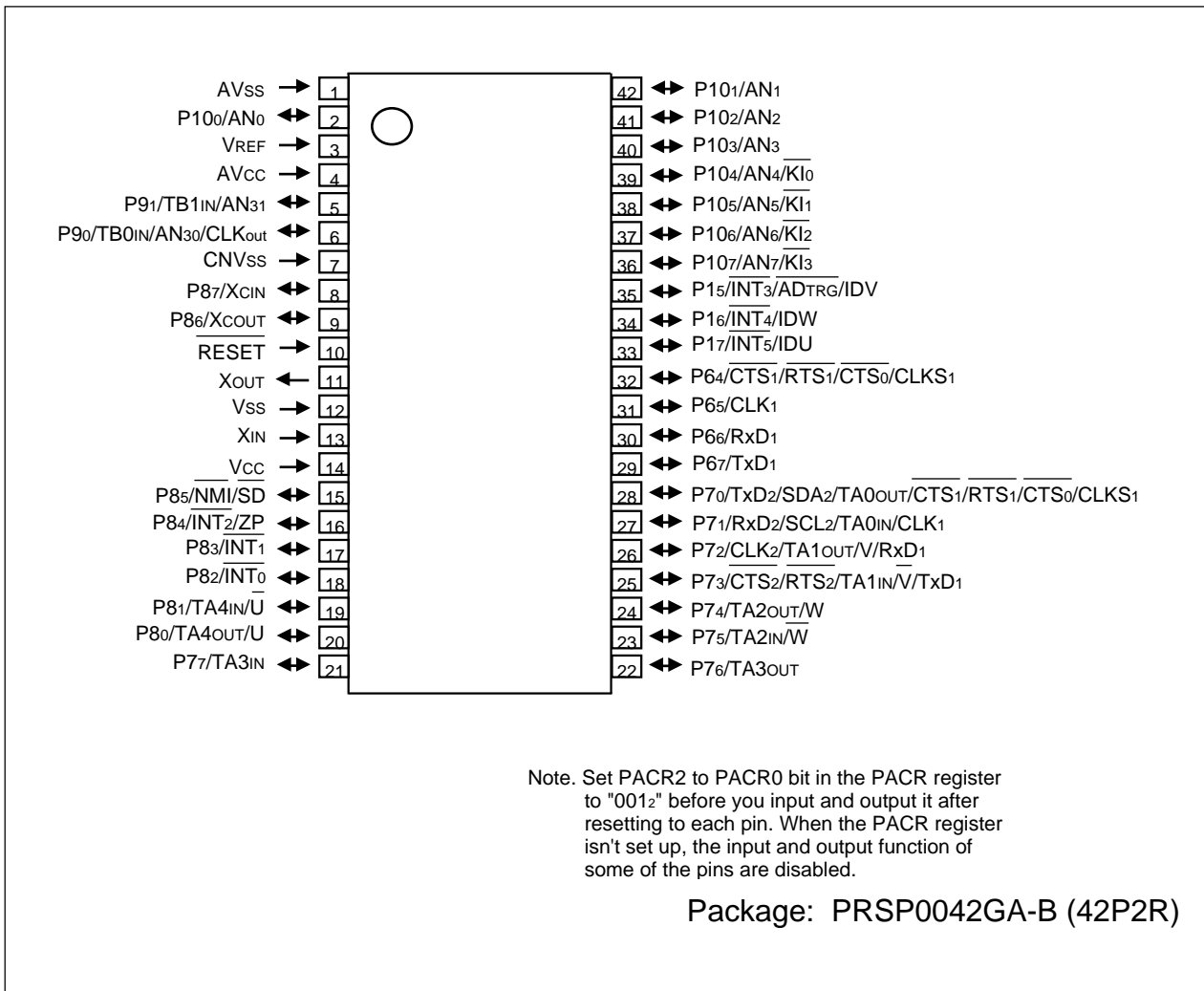


Figure 1.7 Pin Assignment for 42-Pin Package (Top View)

Table 1.12 Pin Characteristics for 42-Pin Package

Pin No.	Control Pin	Port	Interrupt Pin	Timer Pin	UART Pin	Analog Pin
1	AVss					
2		P100				AN0
3	VREF					
4	AVCC					
5		P91		TB1IN		AN31
6		P90		TB0IN	CLKOUT	AN30
7	CNVss					
8	XCIN	P87				
9	XCOUT	P86				
10	RESET					
11	XOUT					
12	Vss					
13	XIN					
14	VCC					
15		P85	NMI	SD		
16		P84	INT2	ZP		
17		P83	INT1			
18		P82	INT0			
19		P81		TA4IN / U		
20		P80		TA4OUT / U		
21		P77		TA3IN		
22		P76		TA3OUT		
23		P75		TA2IN / W		
24		P74		TA2OUT / W		
25		P73		TA1IN / V	CTS2 / RTS2 / TxD1	
26		P72		TA1OUT / V	CLK2 / RxD1	
27		P71		TA0IN	RxD2 / SCL2 / CLK1	
28		P70		TA0OUT	TxD2 / SDA2 / RTS1 / CTS1 / CTS0 / CLKS1	
29		P67			TxD1	
30		P66			RxD1	
31		P65			CLK1	
32		P64			RTS1 / CTS1 / CTS0 / CLKS1	
33		P17	INT5	IDU		
34		P16	INT4	IDW		
35		P15	INT3	IDV		ADTRG
36		P107	KI3			AN7
37		P106	KI2			AN6
38		P105	KI1			AN5
39		P104	KI0			AN4
40		P103				AN3
41		P102				AN2
42		P101				AN1

## 1.6 Pin Description

**Table 1.13 Pin Description (48-Pin and 42-Pin Packages)**

Classification	Pin Name	I/O Type	Description
Power Supply	Vcc, Vss	I	Apply 0V to the Vss pin. Apply following voltage to the Vcc pin. 2.7 to 5.5 V (M16C/26A, M16C/26B), 3.0 to 5.5 V (M16C/26T T-ver.), 4.2 to 5.5 V (M16C/26T V-ver.)
Analog Power Supply	AVcc AVss	I	Supplies power to the A/D converter. Connect the AVcc pin to Vcc and the AVss pin to Vss
Reset Input	RESET	I	The MCU is in a reset state when "L" is applied to the RESET pin
CNVSS	CNVss	I	Connect the CNVss pin to Vss
Main Clock Input	XIN	I	I/O pins for the main clock oscillation circuit. Connect a ceramic resonator or crystal oscillator between XIN and XOUT. To apply external clock, apply it to XIN and leave XOUT open. If XIN is not used (for external oscillator or external clock), connect XIN pin to Vcc and leave XOUT open
Main Clock Output	XOUT	O	
Sub Clock Input	Xcin	I	I/O pins for the sub clock oscillation circuit. Connect a crystal oscillator between Xcin and Xcout
Sub Clock Output	Xcout	O	
Clock Output	CLKOUT	O	Outputs the clock having the same frequency as f1, f8, f32, or fc
INT Interrupt Input	INT0 to INT5	I	Input pins for the INT interrupt. INT2 can be used for Timer A Z-phase function
NMI Interrupt Input	NMI	I	NMI interrupt input pin. NMI cannot be used as I/O port while the three-phase motor control is enabled. Apply a stable "H" to $\overline{\text{NMI}}$ after setting it's direction register to "0" when the three-phase motor control is enabled
Key Input Interrupt	KI0 to KI3	I	Input pins for the key input interrupt
Timer A	TA0OUT to TA4OUT	I/O	I/O pins for the timer A0 to A4
	TA0IN to TA4IN	I	Input pins for the timer A0 to A4
	ZP	I	Input pin for Z-phase
Timer B	TB0IN to TB1IN	I	Timer B0 to B1 input pins
Three-Phase Motor Control Timer Output	U, $\overline{\text{U}}$ , V, $\overline{\text{V}}$ , W, $\overline{\text{W}}$	O	Output pins for the three-phase motor control timer
	IDU, IDW, IDV, $\overline{\text{SD}}$	I/O	I/O pins for the three-phase motor control timer
Serial I/O	CTS1 to CTS2	I	Input pins to control data transmission
	RTS1 to RTS2	O	Output pins to control data reception
	CLK1 to CLK2	I/O	Inputs and outputs the transfer clock
	RxD1 to RxD2	I	Inputs serial data
	TxD1 to TxD2	O	Outputs serial data
	CLKS1	O	Output pin for transfer clock
Reference Voltage Input	VREF	I	Applies reference voltage to the A/D converter
A/D Converter	AN0 to AN7 AN30 to AN31	I	Analog input pins for the A/D converter
	ADTRG	I	Input pin for an external A/D trigger
I/O Ports	P15 to P17	I/O	I/O ports for CMOS. Each port can be programmed for input or output under the control of the direction register. An input port can be set, by program, for a pull-up resistor available or for no pull-up resistor available in 3-bit units
	P64 to P67 P70 to P77 P80 to P87 P100 to P107 P90 to P91	I/O	I/O ports for CMOS. Each port can be programmed for input or output under the control of the direction register. An input port can be set, by program, for a pull-up resistor available or for no pull-up resistor available in 4-bit units

I : Input    O : Output    I/O : Input and output

**Table 1.13 Pin Description ( 48-pin packages only) (Continued)**

Classification	Pin Name	I/O Type	Description
Serial I/O	CTS0	I	Inputs pin to control data transmission
	RTS0	O	Output pin to control data reception
	CLK0	I/O	Inputs and outputs the transfer clock
	RxD0	I	Inputs serial data
	TxD0	O	Outputs serial data
Timer B	TB2IN	I	Timer B2 input pin
A/D Converter	AN24	I	Analog input pins for the A/D converter
	AN32		
I/O Ports	P60 to P63 P92 to P93	I/O	I/O ports for CMOS. Each port can be programmed for input or output under the control of the direction register. An input port can be set, by program, for a pull-up resistor available or for no pull-up resistor available in 4-bit units

I : Input    O : Output    I/O : Input and output

## 2. Central Processing Unit (CPU)

Figure 2.1 shows the CPU registers. The register bank is comprised of seven registers (R0, R1, R2, R3, A0, A1 and FB) out of 13 registers. There are two sets of register bank.

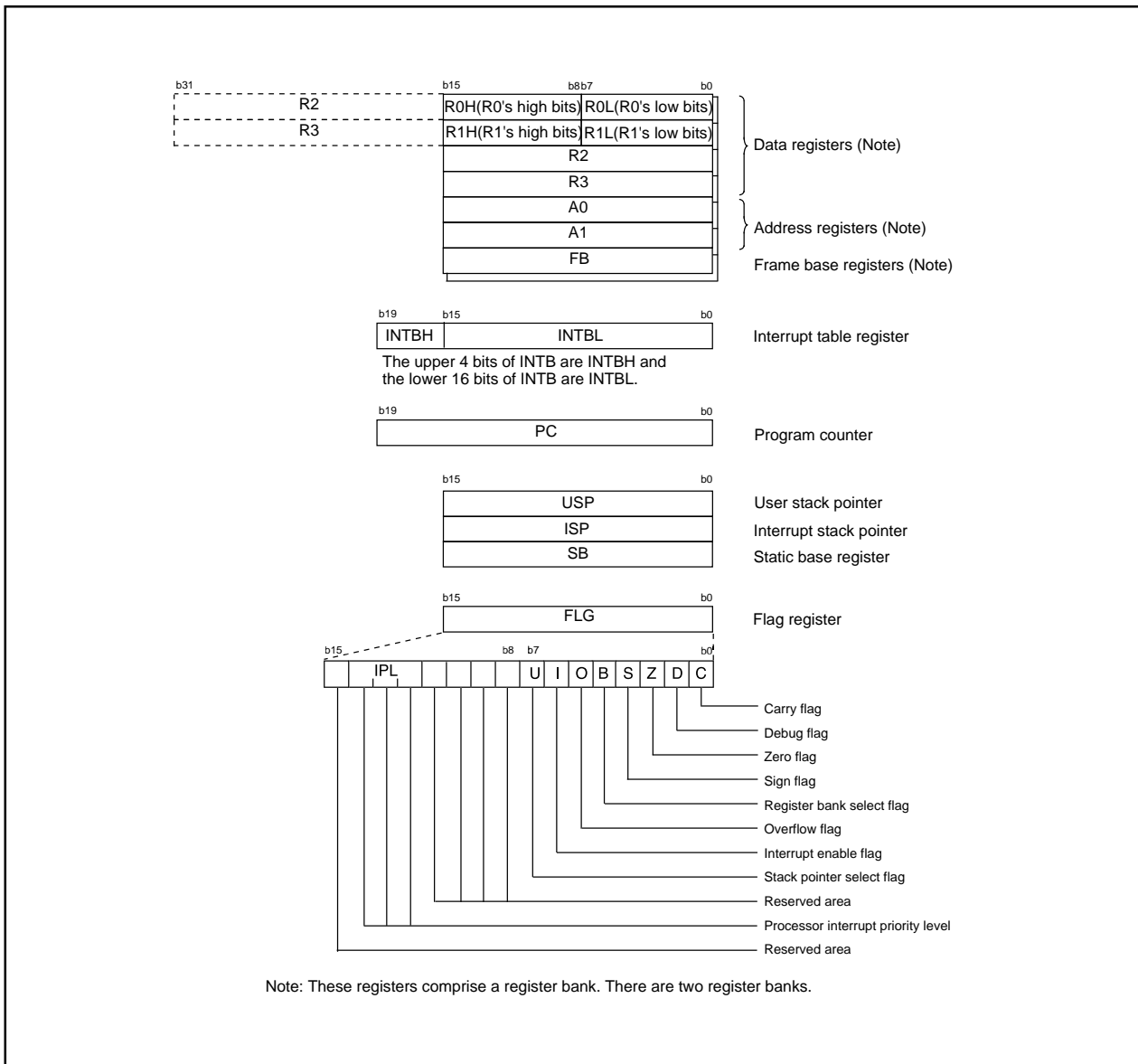


Figure 2.1. CPU Register

### 2.1 Data Registers (R0, R1, R2 and R3)

The R0 register consists of 16 bits, and is used mainly for transfers and arithmetic/logic operations. R1 to R3 are the same as R0.

The R0 register can be separated between high (R0H) and low (R0L) for use as two 8-bit data registers. R1H and R1L are the same as R0H and R0L. Conversely, R2 and R0 can be combined for use as a 32-bit data register (R2R0). R3R1 is the same as R2R0.

### 2.2 Address Registers (A0 and A1)

The register A0 consists of 16 bits, and is used for address register indirect addressing and address register relative addressing. They also are used for transfers and arithmetic/logic operations. A1 is the same as A0.

In some instructions, registers A1 and A0 can be combined for use as a 32-bit address register (A1A0).

## 2.3 Frame Base Register (FB)

FB is configured with 16 bits, and is used for FB relative addressing.

## 2.4 Interrupt Table Register (INTB)

INTB is configured with 20 bits, indicating the start address of an interrupt vector table.

## 2.5 Program Counter (PC)

PC is configured with 20 bits, indicating the address of an instruction to be executed.

## 2.6 User Stack Pointer (USP) and Interrupt Stack Pointer (ISP)

Stack pointer (SP) comes in two types: USP and ISP, each configured with 16 bits.

Your desired type of stack pointer (USP or ISP) can be selected by the U flag of FLG.

## 2.7 Static Base Register (SB)

SB is configured with 16 bits, and is used for SB relative addressing.

## 2.8 Flag Register (FLG)

FLG consists of 11 bits, indicating the CPU status.

### 2.8.1 Carry Flag (C Flag)

This flag retains a carry, borrow, or shift-out bit that has occurred in the arithmetic/logic unit.

### 2.8.2 Debug Flag (D Flag)

The D flag is used exclusively for debugging purpose. During normal use, it must be set to 0.

### 2.8.3 Zero Flag (Z Flag)

This flag is set to 1 when an arithmetic operation resulted in 0; otherwise, it is 0.

### 2.8.4 Sign Flag (S Flag)

This flag is set to 1 when an arithmetic operation resulted in a negative value; otherwise, it is 0.

### 2.8.5 Register Bank Select Flag (B Flag)

Register bank 0 is selected when this flag is 0; register bank 1 is selected when this flag is 1.

### 2.8.6 Overflow Flag (O Flag)

This flag is set to 1 when the operation resulted in an overflow; otherwise, it is 0.

### 2.8.7 Interrupt Enable Flag (I Flag)

This flag enables a maskable interrupt.

Maskable interrupts are disabled when the I flag is 0, and are enabled when the I flag is 1.

The I flag is cleared to 0 when the interrupt request is accepted.

### 2.8.8 Stack Pointer Select Flag (U Flag)

ISP is selected when the U flag is 0; USP is selected when the U flag is 1.

The U flag is cleared to 0 when a hardware interrupt request is accepted or an INT instruction for software interrupt Nos. 0 to 31 is executed.

### 2.8.9 Processor Interrupt Priority Level (IPL)

IPL is configured with three bits, for specification of up to eight processor interrupt priority levels from level 0 to level 7.

If a requested interrupt has priority greater than IPL, the interrupt is enabled.

### 2.8.10 Reserved Area

When write to this bit, write 0. When read, its content is undefined.

### 3. Memory

**Figure 3.1** is a memory map of the M16C/26A Group (M16C/26A, M16C/26B, M16C/26T). The M16C/26A Group provides 1-Mbyte address space addresses 00000<sub>16</sub> to FFFFF<sub>16</sub>.

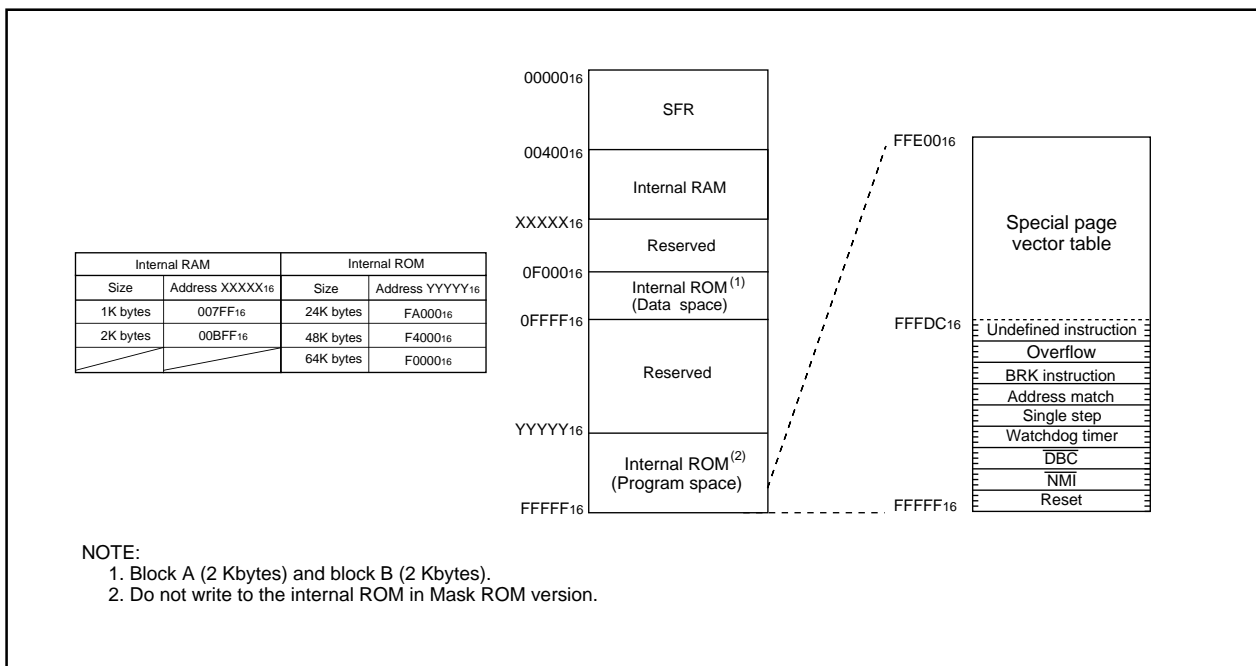
The internal ROM is allocated lower address, beginning with address FFFFF<sub>16</sub>. For example, a 64-Kbyte internal ROM area is allocated in addresses F0000<sub>16</sub> to FFFFF<sub>16</sub>. The flash memory version has two sets of 2-Kbyte internal ROM area, block A and block B, for data space. These blocks are allocated addresses F000<sub>16</sub> to FFFF<sub>16</sub>.

The fixed interrupt vectors are allocated addresses FFFDC<sub>16</sub> to FFFFF<sub>16</sub> and they store the start address of each interrupt routine.

The internal RAM is allocated higher addresses, beginning with address 00400<sub>16</sub>. For example, a 1-Kbyte internal RAM area is allocated in addresses 00400<sub>16</sub> to 007FF<sub>16</sub>. The internal RAM is used for temporarily storing data. The area is also used as stacks when subroutines are called or interrupt requests are acknowledged.

The SFR is allocated addresses 00000<sub>16</sub> to 003FF<sub>16</sub>. The peripheral function control registers are allocated here. All blank spaces within SFR location are reserved and cannot be accessed by users.

The special page vectors are allocated addresses FFE00<sub>16</sub> to FFFDB<sub>16</sub>. They are used for the JMPS instruction and JSRS instruction. Refer to the Renesas publication **M16C/60 and M16C/20 Series Software Manual** for details.



**Figure 3.1 Memory Map**

## 4. Special Function Register (SFR)

Table 4.1 SFR Information(1)(1)

Address	Register	Symbol	After reset
0000 <sub>16</sub>			
0001 <sub>16</sub>			
0002 <sub>16</sub>			
0003 <sub>16</sub>			
0004 <sub>16</sub>	Processor mode register 0	PM0	00 <sub>16</sub>
0005 <sub>16</sub>	Processor mode register 1	PM1	00001000 <sub>2</sub>
0006 <sub>16</sub>	System clock control register 0	CM0	01001000 <sub>2</sub> (M16C/26A) 01101000 <sub>2</sub> (M16C/26T)
0007 <sub>16</sub>	System clock control register 1	CM1	00100000 <sub>2</sub>
0008 <sub>16</sub>			
0009 <sub>16</sub>	Address match interrupt enable register	AIER	XXXXXX00 <sub>2</sub>
000A <sub>16</sub>	Protect register	PRCR	XX000000 <sub>2</sub>
000B <sub>16</sub>			
000C <sub>16</sub>	Oscillation stop detection register <sup>(2)</sup>	CM2	0X000000 <sub>2</sub>
000D <sub>16</sub>			
000E <sub>16</sub>	Watchdog timer start register	WDTS	XX <sub>16</sub>
000F <sub>16</sub>	Watchdog timer control register	WDC	00XXXXXX <sub>2</sub> <sup>(3)</sup>
0010 <sub>16</sub>	Address match interrupt register 0	RMAD0	00 <sub>16</sub>
0011 <sub>16</sub>			00 <sub>16</sub>
0012 <sub>16</sub>			X0 <sub>16</sub>
0013 <sub>16</sub>			
0014 <sub>16</sub>	Address match interrupt register 1	RMAD1	00 <sub>16</sub>
0015 <sub>16</sub>			00 <sub>16</sub>
0016 <sub>16</sub>			X0 <sub>16</sub>
0017 <sub>16</sub>			
0018 <sub>16</sub>			
0019 <sub>16</sub>	Voltage detection register 1 <sup>(4, 5)</sup>	VCR1	00001000 <sub>2</sub>
001A <sub>16</sub>	Voltage detection register 2 <sup>(4, 5)</sup>	VCR2	00 <sub>16</sub>
001B <sub>16</sub>			
001C <sub>16</sub>	PLL control register 0	PLC0	0001X010 <sub>2</sub>
001D <sub>16</sub>			
001E <sub>16</sub>	Processor mode register 2	PM2	XXX00000 <sub>2</sub>
001F <sub>16</sub>	Low voltage detection interrupt register <sup>(5)</sup>	D4INT	00 <sub>16</sub>
0020 <sub>16</sub>	DMA0 source pointer	SAR0	XX <sub>16</sub>
0021 <sub>16</sub>			XX <sub>16</sub>
0022 <sub>16</sub>			XX <sub>16</sub>
0023 <sub>16</sub>			
0024 <sub>16</sub>	DMA0 destination pointer	DAR0	XX <sub>16</sub>
0025 <sub>16</sub>			XX <sub>16</sub>
0026 <sub>16</sub>			XX <sub>16</sub>
0027 <sub>16</sub>			
0028 <sub>16</sub>	DMA0 transfer counter	TCR0	XX <sub>16</sub>
0029 <sub>16</sub>			XX <sub>16</sub>
002A <sub>16</sub>			
002B <sub>16</sub>			
002C <sub>16</sub>	DMA0 control register	DM0CON	00000X00 <sub>2</sub>
002D <sub>16</sub>			
002E <sub>16</sub>			
002F <sub>16</sub>			
0030 <sub>16</sub>	DMA1 source pointer	SAR1	XX <sub>16</sub>
0031 <sub>16</sub>			XX <sub>16</sub>
0032 <sub>16</sub>			XX <sub>16</sub>
0033 <sub>16</sub>			XX <sub>16</sub>
0034 <sub>16</sub>	DMA1 destination pointer	DAR1	XX <sub>16</sub>
0035 <sub>16</sub>			XX <sub>16</sub>
0036 <sub>16</sub>			XX <sub>16</sub>
0037 <sub>16</sub>			
0038 <sub>16</sub>	DMA1 transfer counter	TCR1	XX <sub>16</sub>
0039 <sub>16</sub>			XX <sub>16</sub>
003A <sub>16</sub>			
003B <sub>16</sub>			
003C <sub>16</sub>	DMA1 control register	DM1CON	00000X00 <sub>2</sub>
003D <sub>16</sub>			
003E <sub>16</sub>			
003F <sub>16</sub>			

NOTES:

1. The blank spaces are reserved. No access is allowed.
2. Bits CM27, CM21, and CM20 do not change at oscillation stop detection reset.
3. The WDC5 bit is 0 (cold start) immediately after power-on. It can only be set to 1 by program. The WDC5 bit cannot be used in M16C/26T.
4. The VCR1 and VCR2 registers do not change at software reset, watchdog timer reset, and oscillation stop detection reset.
5. Registers VCR1, VCR2, and D4INT cannot be used in M16C/26T.

X : Undefined

Table 4.2 SFR Information(2)<sup>(1)</sup>

Address	Register	Symbol	After reset
0040 <sub>16</sub>			
0041 <sub>16</sub>			
0042 <sub>16</sub>			
0043 <sub>16</sub>			
0044 <sub>16</sub>	INT3 interrupt control register	INT3IC	XX00X000 <sub>2</sub>
0045 <sub>16</sub>			
0046 <sub>16</sub>			
0047 <sub>16</sub>			
0048 <sub>16</sub>	INT5 interrupt control register	INT5IC	XX00X000 <sub>2</sub>
0049 <sub>16</sub>	INT4 interrupt control register	INT4IC	XX00X000 <sub>2</sub>
004A <sub>16</sub>	UART2 Bus collision detection interrupt control register	BCNIC	XXXXX000 <sub>2</sub>
004B <sub>16</sub>	DMA0 interrupt control register	DM0IC	XXXXX000 <sub>2</sub>
004C <sub>16</sub>	DMA1 interrupt control register	DM1IC	XXXXX000 <sub>2</sub>
004D <sub>16</sub>	Key input interrupt control register	KUPIC	XXXXX000 <sub>2</sub>
004E <sub>16</sub>	A/D conversion interrupt control register	ADIC	XXXXX000 <sub>2</sub>
004F <sub>16</sub>	UART2 transmit interrupt control register	S2TIC	XXXXX000 <sub>2</sub>
0050 <sub>16</sub>	UART2 receive interrupt control register	S2RIC	XXXXX000 <sub>2</sub>
0051 <sub>16</sub>	UART0 transmit interrupt control register	S0TIC	XXXXX000 <sub>2</sub>
0052 <sub>16</sub>	UART0 receive interrupt control register	S0RIC	XXXXX000 <sub>2</sub>
0053 <sub>16</sub>	UART1 transmit interrupt control register	S1TIC	XXXXX000 <sub>2</sub>
0054 <sub>16</sub>	UART1 receive interrupt control register	S1RIC	XXXXX000 <sub>2</sub>
0055 <sub>16</sub>	TimerA0 interrupt control register	TA0IC	XXXXX000 <sub>2</sub>
0056 <sub>16</sub>	TimerA1 interrupt control register	TA1IC	XXXXX000 <sub>2</sub>
0057 <sub>16</sub>	TimerA2 interrupt control register	TA2IC	XXXXX000 <sub>2</sub>
0058 <sub>16</sub>	TimerA3 interrupt control register	TA3IC	XXXXX000 <sub>2</sub>
0059 <sub>16</sub>	TimerA4 interrupt control register	TA4IC	XXXXX000 <sub>2</sub>
005A <sub>16</sub>	TimerB0 interrupt control register	TB0IC	XXXXX000 <sub>2</sub>
005B <sub>16</sub>	TimerB1 interrupt control register	TB1IC	XXXXX000 <sub>2</sub>
005C <sub>16</sub>	TimerB2 interrupt control register	TB2IC	XXXXX000 <sub>2</sub>
005D <sub>16</sub>	INT0 interrupt control register	INT0IC	XX00X000 <sub>2</sub>
005E <sub>16</sub>	INT1 interrupt control register	INT1IC	XX00X000 <sub>2</sub>
005F <sub>16</sub>	INT2 interrupt control register	INT2IC	XX00X000 <sub>2</sub>
0060 <sub>16</sub>			
0061 <sub>16</sub>			
0062 <sub>16</sub>			
0063 <sub>16</sub>			
0064 <sub>16</sub>			
0065 <sub>16</sub>			
0066 <sub>16</sub>			
0067 <sub>16</sub>			
0068 <sub>16</sub>			
0069 <sub>16</sub>			
006A <sub>16</sub>			
006B <sub>16</sub>			
006C <sub>16</sub>			
006D <sub>16</sub>			
006E <sub>16</sub>			
006F <sub>16</sub>			
0070 <sub>16</sub>			
0071 <sub>16</sub>			
0072 <sub>16</sub>			
0073 <sub>16</sub>			
0074 <sub>16</sub>			
0075 <sub>16</sub>			
0076 <sub>16</sub>			
0077 <sub>16</sub>			
0078 <sub>16</sub>			
0079 <sub>16</sub>			
007A <sub>16</sub>			
007B <sub>16</sub>			
007C <sub>16</sub>			
007D <sub>16</sub>			
007E <sub>16</sub>			
007F <sub>16</sub>			

## NOTE:

1. Blank spaces are reserved. No access is allowed.

X: Undefined

Table 4.3 SFR Information(3)<sup>(1)</sup>

Address	Register	Symbol	After reset
0080 <sub>16</sub>			
0081 <sub>16</sub>			
0082 <sub>16</sub>			
0083 <sub>16</sub>			
0084 <sub>16</sub>			
0085 <sub>16</sub>			
0086 <sub>16</sub>			
01B0 <sub>16</sub>			
01B1 <sub>16</sub>			
01B2 <sub>16</sub>			
01B3 <sub>16</sub>	Flash memory control register 4 (Note 2)	FMR4	01000000 <sub>2</sub>
01B4 <sub>16</sub>			
01B5 <sub>16</sub>	Flash memory control register 1 (Note 2)	FMR1	000XXX0X <sub>2</sub>
01B6 <sub>16</sub>			
01B7 <sub>16</sub>	Flash memory control register 0 (Note 2)	FMR0	01 <sub>16</sub>
01B8 <sub>16</sub>			
01B9 <sub>16</sub>			
01BA <sub>16</sub>			
01BB <sub>16</sub>			
01BC <sub>16</sub>			
01BD <sub>16</sub>			
01BE <sub>16</sub>			
01BF <sub>16</sub>			
0250 <sub>16</sub>			
0251 <sub>16</sub>			
0252 <sub>16</sub>			
0253 <sub>16</sub>			
0254 <sub>16</sub>			
0255 <sub>16</sub>			
0256 <sub>16</sub>			
0257 <sub>16</sub>			
0258 <sub>16</sub>			
0259 <sub>16</sub>			
025A <sub>16</sub>	Three phase protect control register	TPRC	00 <sub>16</sub>
025B <sub>16</sub>			
025C <sub>16</sub>	On-chip oscillator control register	ROCR	00000101 <sub>2</sub>
025D <sub>16</sub>	Pin assignment control register	PACR	00 <sub>16</sub>
025E <sub>16</sub>	Peripheral clock select register	PCLKR	00000011 <sub>2</sub>
025F <sub>16</sub>			
0330 <sub>16</sub>			
0331 <sub>16</sub>			
0332 <sub>16</sub>			
0333 <sub>16</sub>			
0334 <sub>16</sub>			
0335 <sub>16</sub>			
0336 <sub>16</sub>			
0337 <sub>16</sub>			
0338 <sub>16</sub>			
0339 <sub>16</sub>			
033A <sub>16</sub>			
033B <sub>16</sub>			
033C <sub>16</sub>			
033D <sub>16</sub>			
033E <sub>16</sub>	NMI digital debounce register	NDDR	FF <sub>16</sub>
033F <sub>16</sub>	Port17 digital debounce register	P17DDR	FF <sub>16</sub>

## NOTES:

- Blank spaces are reserved. No access is allowed.
- This register is included in the flash memory version.

X: Undefined

Table 4.4 SFR Information(4)<sup>(1)</sup>

Address	Register	Symbol	After reset
0340 <sub>16</sub>			
0341 <sub>16</sub>			
0342 <sub>16</sub> 0343 <sub>16</sub>	Timer A1-1 register	TA11	XX <sub>16</sub> XX <sub>16</sub>
0344 <sub>16</sub> 0345 <sub>16</sub>	Timer A2-1 register	TA21	XX <sub>16</sub> XX <sub>16</sub>
0346 <sub>16</sub> 0347 <sub>16</sub>	Timer A4-1 register	TA41	XX <sub>16</sub> XX <sub>16</sub>
0348 <sub>16</sub>	Three phase PWM control register 0	INVC0	00 <sub>16</sub>
0349 <sub>16</sub>	Three phase PWM control register 1	INVC1	00 <sub>16</sub>
034A <sub>16</sub>	Three phase output buffer register 0	IDB0	3F <sub>16</sub>
034B <sub>16</sub>	Three phase output buffer register 1	IDB1	3F <sub>16</sub>
034C <sub>16</sub>	Dead time timer	DTT	XX <sub>16</sub>
034D <sub>16</sub>	Timer B2 Interrupt occurrence frequency set counter	ICTB2	XX <sub>16</sub>
034E <sub>16</sub>	Position-data-retain function control register	PDRF	XXXX0000 <sub>2</sub>
034F <sub>16</sub>			
0350 <sub>16</sub>			
0351 <sub>16</sub>			
0352 <sub>16</sub>			
0353 <sub>16</sub>			
0354 <sub>16</sub>			
0355 <sub>16</sub>			
0356 <sub>16</sub>			
0357 <sub>16</sub>			
0358 <sub>16</sub>	Port function control register	PFCR	00111111 <sub>2</sub>
0359 <sub>16</sub>			
035A <sub>16</sub>			
035B <sub>16</sub>			
035C <sub>16</sub>			
035D <sub>16</sub>			
035E <sub>16</sub>	Interrupt request cause select register 2	IFSR2A	XXXXXXXX <sub>2</sub>
035F <sub>16</sub>	Interrupt request cause select register	IFSR	00 <sub>16</sub>
0360 <sub>16</sub>			
0361 <sub>16</sub>			
0362 <sub>16</sub>			
0363 <sub>16</sub>			
0364 <sub>16</sub>			
0365 <sub>16</sub>			
0366 <sub>16</sub>			
0367 <sub>16</sub>			
0368 <sub>16</sub>			
0369 <sub>16</sub>			
036A <sub>16</sub>			
036B <sub>16</sub>			
036C <sub>16</sub>			
036D <sub>16</sub>			
036E <sub>16</sub>			
036F <sub>16</sub>			
0370 <sub>16</sub>			
0371 <sub>16</sub>			
0372 <sub>16</sub>			
0373 <sub>16</sub>			
0374 <sub>16</sub>	UART2 special mode register 4	U2SMR4	00 <sub>16</sub>
0375 <sub>16</sub>	UART2 special mode register 3	U2SMR3	00X0X0X <sub>2</sub>
0376 <sub>16</sub>	UART2 special mode register 2	U2SMR2	X0000000 <sub>2</sub>
0377 <sub>16</sub>	UART2 special mode register	U2SMR	X0000000 <sub>2</sub>
0378 <sub>16</sub>	UART2 transmit/receive mode register	U2MR	00 <sub>16</sub>
0379 <sub>16</sub>	UART2 bit rate register	U2BRG	XX <sub>16</sub>
037A <sub>16</sub>	UART2 transmit buffer register	U2TB	XXXXXXXX <sub>2</sub>
037B <sub>16</sub>			XXXXXXXX <sub>2</sub>
037C <sub>16</sub>	UART2 transmit/receive control register 0	U2C0	00001000 <sub>2</sub>
037D <sub>16</sub>	UART2 transmit/receive control register 1	U2C1	00000010 <sub>2</sub>
037E <sub>16</sub>	UART2 receive buffer register	U2RB	XXXXXXXX <sub>2</sub>
037F <sub>16</sub>			XXXXXXXX <sub>2</sub>

## NOTE:

1. Blank spaces are reserved. No access is allowed.

X : Undefined

**Table 4.5 SFR Information(5)<sup>(1)</sup>**

Address	Register	Symbol	After reset
0380 <sub>16</sub>	Count start flag	TABSR	00 <sub>16</sub>
0381 <sub>16</sub>	Clock prescaler reset flag	CPSRF	0XXXXXXX <sub>2</sub>
0382 <sub>16</sub>	One-shot start flag	ONSF	00 <sub>16</sub>
0383 <sub>16</sub>	Trigger select register	TRGSR	00 <sub>16</sub>
0384 <sub>16</sub>	Up-downm flag	UDF	00 <sub>16</sub>
0385 <sub>16</sub>			
0386 <sub>16</sub> 0387 <sub>16</sub>	Timer A0 register	TA0	XX <sub>16</sub> XX <sub>16</sub>
0388 <sub>16</sub> 0389 <sub>16</sub>	Timer A1 register	TA1	XX <sub>16</sub> XX <sub>16</sub>
038A <sub>16</sub> 038B <sub>16</sub>	Timer A2 register	TA2	XX <sub>16</sub> XX <sub>16</sub>
038C <sub>16</sub> 038D <sub>16</sub>	Timer A3 register	TA3	XX <sub>16</sub> XX <sub>16</sub>
038E <sub>16</sub> 038F <sub>16</sub>	Timer A4 register	TA4	XX <sub>16</sub> XX <sub>16</sub>
0390 <sub>16</sub> 0391 <sub>16</sub>	Timer B0 register	TB0	XX <sub>16</sub> XX <sub>16</sub>
0392 <sub>16</sub> 0393 <sub>16</sub>	Timer B1 register	TB1	XX <sub>16</sub> XX <sub>16</sub>
0394 <sub>16</sub> 0395 <sub>16</sub>	Timer B2 register	TB2	XX <sub>16</sub> XX <sub>16</sub>
0396 <sub>16</sub>	Timer A0 mode register	TA0MR	00 <sub>16</sub>
0397 <sub>16</sub>	Timer A1 mode register	TA1MR	00 <sub>16</sub>
0398 <sub>16</sub>	Timer A2 mode register	TA2MR	00 <sub>16</sub>
0399 <sub>16</sub>	Timer A3 mode register	TA3MR	00 <sub>16</sub>
039A <sub>16</sub>	Timer A4 mode register	TA4MR	00 <sub>16</sub>
039B <sub>16</sub>	Timer B0 mode register	TB0MR	00XX0000 <sub>2</sub>
039C <sub>16</sub>	Timer B1 mode register	TB1MR	00XX0000 <sub>2</sub>
039D <sub>16</sub>	Timer B2 mode register	TB2MR	00XX0000 <sub>2</sub>
039E <sub>16</sub> 039F <sub>16</sub>	Timer B2 special mode register	TB2SC	X0000000 <sub>2</sub>
03A0 <sub>16</sub>	UART0 transmit/receive mode register	U0MR	00 <sub>16</sub>
03A1 <sub>16</sub>	UART0 bit rate register	U0BRG	XX <sub>16</sub>
03A2 <sub>16</sub> 03A3 <sub>16</sub>	UART0 transmit buffer register	U0TB	XXXXXXXX <sub>2</sub> XXXXXXXX <sub>2</sub>
03A4 <sub>16</sub>	UART0 transmit/receive control register 0	U0C0	00001000 <sub>2</sub>
03A5 <sub>16</sub>	UART0 transmit/receive control register 1	U0C1	00000010 <sub>2</sub>
03A6 <sub>16</sub> 03A7 <sub>16</sub>	UART0 receive buffer register	U0RB	XXXXXXXX <sub>2</sub> XXXXXXXX <sub>2</sub>
03A8 <sub>16</sub>	UART1 transmit/receive mode register	U1MR	00 <sub>16</sub>
03A9 <sub>16</sub>	UART1 bit rate register	U1BRG	XX <sub>16</sub>
03AA <sub>16</sub> 03AB <sub>16</sub>	UART1 transmit buffer register	U1TB	XXXXXXXX <sub>2</sub> XXXXXXXX <sub>2</sub>
03AC <sub>16</sub>	UART1 transmit/receive control register 0	U1C0	00001000 <sub>2</sub>
03AD <sub>16</sub>	UART1 transmit/receive control register 1	U1C1	00000010 <sub>2</sub>
03AE <sub>16</sub> 03AF <sub>16</sub>	UART1 receive buffer register	U1RB	XXXXXXXX <sub>2</sub> XXXXXXXX <sub>2</sub>
03B0 <sub>16</sub> 03B1 <sub>16</sub> 03B2 <sub>16</sub> 03B3 <sub>16</sub>	UART transmit/receive control register 2	UCON	X0000000 <sub>2</sub>
03B4 <sub>16</sub> 03B5 <sub>16</sub>	CRC snoop address register	CRCSAR	XX <sub>16</sub> 00XXXXXXXX <sub>2</sub>
03B6 <sub>16</sub> 03B7 <sub>16</sub>	CRC mode register	CRCMR	0XXXXXXXX0 <sub>2</sub>
03B8 <sub>16</sub> 03B9 <sub>16</sub>	DMA0 request cause select register	DM0SL	00 <sub>16</sub>
03BA <sub>16</sub> 03BB <sub>16</sub>	DMA1 request cause select register	DM1SL	00 <sub>16</sub>
03BC <sub>16</sub> 03BD <sub>16</sub>	CRC data register	CRCD	XX <sub>16</sub> XX <sub>16</sub>
03BE <sub>16</sub> 03BF <sub>16</sub>	CRC input register	CRCIN	XX <sub>16</sub>

**NOTE:**

1. Blank spaces are reserved. No access is allowed.

X : Undefined

Table 4.6 SFR Information(6)<sup>(1)</sup>

Address	Register	Symbol	After Reset
03C0 <sub>16</sub> 03C1 <sub>16</sub>	A/D register 0	AD0	XXXXXXXX <sub>2</sub> XXXXXXXX <sub>2</sub>
03C2 <sub>16</sub> 03C3 <sub>16</sub>	A/D register 1	AD1	XXXXXXXX <sub>2</sub> XXXXXXXX <sub>2</sub>
03C4 <sub>16</sub> 03C5 <sub>16</sub>	A/D register 2	AD2	XXXXXXXX <sub>2</sub> XXXXXXXX <sub>2</sub>
03C6 <sub>16</sub> 03C7 <sub>16</sub>	A/D register 3	AD3	XXXXXXXX <sub>2</sub> XXXXXXXX <sub>2</sub>
03C8 <sub>16</sub> 03C9 <sub>16</sub>	A/D register 4	AD4	XXXXXXXX <sub>2</sub> XXXXXXXX <sub>2</sub>
03CA <sub>16</sub> 03CB <sub>16</sub>	A/D register 5	AD5	XXXXXXXX <sub>2</sub> XXXXXXXX <sub>2</sub>
03CC <sub>16</sub> 03CD <sub>16</sub>	A/D register 6	AD6	XXXXXXXX <sub>2</sub> XXXXXXXX <sub>2</sub>
03CE <sub>16</sub> 03CF <sub>16</sub>	A/D register 7	AD7	XXXXXXXX <sub>2</sub> XXXXXXXX <sub>2</sub>
03D0 <sub>16</sub>			
03D1 <sub>16</sub>			
03D2 <sub>16</sub>	A/D trigger control register	ADTRGCON	00 <sub>16</sub>
03D3 <sub>16</sub>	A/D status register 0	ADSTAT0	0000X00 <sub>2</sub>
03D4 <sub>16</sub> 03D5 <sub>16</sub>	A/D control register 2	ADCON2	00 <sub>16</sub>
03D6 <sub>16</sub>	A/D control register 0	ADCON0	0000XXX <sub>2</sub>
03D7 <sub>16</sub> 03D8 <sub>16</sub>	A/D control register 1	ADCON1	00 <sub>16</sub>
03D9 <sub>16</sub>			
03DA <sub>16</sub>			
03DB <sub>16</sub>			
03DC <sub>16</sub>			
03DD <sub>16</sub>			
03DE <sub>16</sub>			
03DF <sub>16</sub>			
03E0 <sub>16</sub>			
03E1 <sub>16</sub> 03E2 <sub>16</sub>	Port P1 register	P1	XX <sub>16</sub>
03E3 <sub>16</sub> 03E4 <sub>16</sub>	Port P1 direction register	PD1	00 <sub>16</sub>
03E5 <sub>16</sub>			
03E6 <sub>16</sub>			
03E7 <sub>16</sub>			
03E8 <sub>16</sub>			
03E9 <sub>16</sub>			
03EA <sub>16</sub>			
03EB <sub>16</sub>			
03EC <sub>16</sub>	Port P6 register	P6	XX <sub>16</sub>
03ED <sub>16</sub>	Port P7 register	P7	XX <sub>16</sub>
03EE <sub>16</sub>	Port P6 direction register	PD6	00 <sub>16</sub>
03EF <sub>16</sub>	Port P7 direction register	PD7	00 <sub>16</sub>
03F0 <sub>16</sub>	Port P8 register	P8	XX <sub>16</sub>
03F1 <sub>16</sub>	Port P9 register	P9	XXXXXXXX <sub>2</sub>
03F2 <sub>16</sub>	Port P8 direction register	PD8	00 <sub>16</sub>
03F3 <sub>16</sub>	Port P9 direction register	PD9	XXXX0000 <sub>2</sub>
03F4 <sub>16</sub> 03F5 <sub>16</sub>	Port P10 register	P10	XX <sub>16</sub>
03F6 <sub>16</sub>	Port P10 direction register	PD10	00 <sub>16</sub>
03F7 <sub>16</sub>			
03F8 <sub>16</sub>			
03F9 <sub>16</sub>			
03FA <sub>16</sub>			
03FB <sub>16</sub>			
03FC <sub>16</sub>	Pull-up control register 0	PUR0	00 <sub>16</sub>
03FD <sub>16</sub>	Pull-up control register 1	PUR1	00 <sub>16</sub>
03FE <sub>16</sub>	Pull-up control register 2	PUR2	00 <sub>16</sub>
03FF <sub>16</sub>	Port control register	PCR	00 <sub>16</sub>

## NOTE:

1. Blank spaces are reserved. No access is allowed.

X: Undefined

# Package

JEITA Package Code	RENEASAS Code	Previous Code	MASS[Typ.]
P-LQFP48-7x7-0.50	PLQP0048KB-A	48P6Q-A	0.2g

NOTE)

1. DIMENSIONS \*1\* AND \*2\* DO NOT INCLUDE MOLD FLASH.
2. DIMENSION \*3\* DOES NOT INCLUDE TRIM OFFSET.

Reference Symbol	Dimension in Millimeters		
	Min	Nom	Max
D	6.9	7.0	7.1
E	6.9	7.0	7.1
A <sub>2</sub>	—	1.4	—
H <sub>D</sub>	8.8	9.0	9.2
H <sub>E</sub>	8.8	9.0	9.2
A	—	—	1.7
A <sub>1</sub>	0	0.1	0.2
b <sub>D</sub>	0.17	0.22	0.27
b <sub>1</sub>	—	0.20	—
c	0.09	0.145	0.20
c <sub>1</sub>	—	0.125	—
β	0°	—	8°
ⓐ	—	0.5	—
x	—	—	0.08
y	—	—	0.10
Z <sub>D</sub>	—	0.75	—
Z <sub>E</sub>	—	0.75	—
L	0.35	0.5	0.65
L <sub>1</sub>	—	1.0	—

JEITA Package Code	RENEASAS Code	Previous Code	MASS[Typ.]
P-SSOP42-8.4x17.5-0.80	PRSP0042GA-B	42P2R-E	0.6g

NOTE)

1. DIMENSIONS \*1\* AND \*2\* DO NOT INCLUDE MOLD FLASH.
2. DIMENSION \*3\* DOES NOT INCLUDE TRIM OFFSET.

Reference Symbol	Dimension in Millimeters		
	Min	Nom	Max
D	17.3	17.5	17.7
E	8.2	8.4	8.6
A <sub>2</sub>	—	2.0	—
A	—	—	2.4
A <sub>1</sub>	0.05	—	—
b <sub>D</sub>	0.25	0.3	0.4
c	0.13	0.15	0.2
β	0°	—	10°
H <sub>E</sub>	11.63	11.93	12.23
e	0.65	0.8	0.95
y	—	—	0.15
L	0.3	0.5	0.7

<b>REVISION HISTORY</b>	M16C/26A Group (M16C/26A, M16C/26B, M16C/26T) Shortsheet
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Rev.	Date	Description	
		Page	Summary
0.51	07/25/06	-	First edition

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