THE DATASHEET OF

LTM4627MPY#PBF

www.win-source.net 0086-755-83957316

15A DC/DC µModule Regulator

FEATURES

- **Complete 15A Switch Mode Power Supply**
- **Wide Input Voltage Range: 4.5V to 20V**
- **0.6V to 5V Output Range**
- **±1.5% Total DC Output Error**
- **Differential Remote Sense Amplifier for Precision Regulation**
- **Current Mode Control/ Fast Transient Response**
- **Frequency Synchronization**
- **Parallel Current Sharing (Up to 60A)**
- Selectable Pulse-Skipping or Burst Mode® Operation
- Soft-Start/Voltage Tracking
- Up to 93% Efficiency ($12V_{IN}$, $3.3V_{OUT}$)
- Overcurrent Foldback Protection
- Output Overvoltage Protection
- Small Surface Mount Footprint, Low Profile 15mm × 15mm × 4.32mm LGA and 15mm × 15mm × 4.92mm BGA Packages

APPLICATIONS

- Telecom Servers and Networking Equipment
- ATCA and Storage Cards
- Industrial Equipment
- Medical Systems

DESCRIPTION

The LTM®4627 is a complete 15A output high efficiency switch mode DC/DC power supply. Included in the package are the switching controller, power FETs, inductor and compensation components. Operating over an input voltage range from 4.5V to 20V, the LTM4627 supports an output voltage range of 0.6V to 5V, set by a single external resistor. Only a few input and output capacitors are needed.

Current mode operation allows precision current sharing of up to four LTM4627 regulators to obtain 60A output. High switching frequency and a current mode architecture enable a very fast transient response to line and load changes without sacrificing stability. The device supports frequency synchronization, multiphase/current sharing operation, Burst Mode operation and output voltage tracking for supply rail sequencing.

The LTM4627 is offered in thermally enhanced 15mm × 15mm × 4.32mm LGA and 15mm × 15mm × 4.92mm BGA packages. The LTM4627 is available with SnPb (BGA) or RoHS compliant terminal finish.

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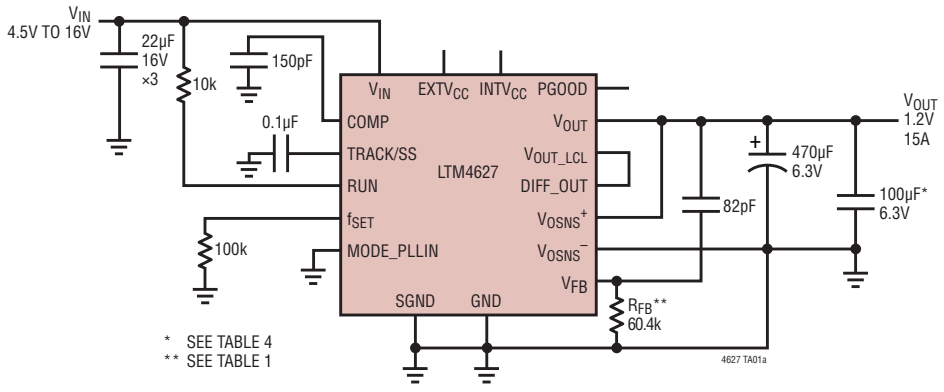
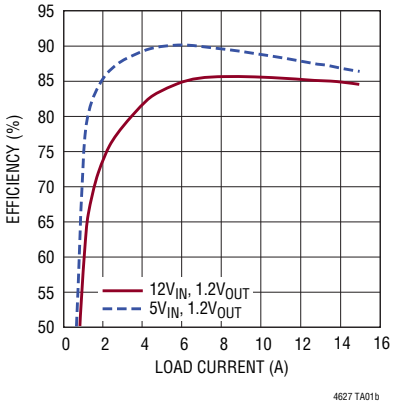
TYPICAL APPLICATION

1.2V, 15A DC/DC µModule® Regulator



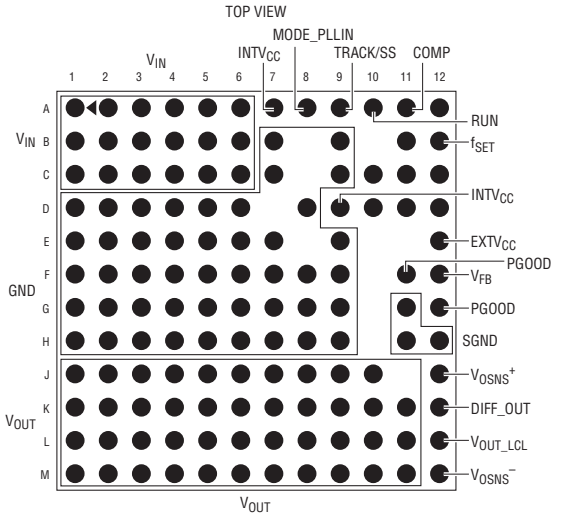
Efficiency vs Load Current



ABSOLUTE MAXIMUM RATINGS (Note 1)

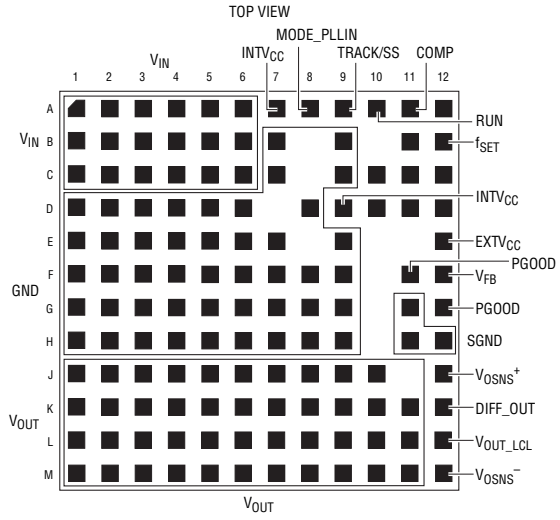
V_{IN} ..... –0.3V to 22V
$INTV_{CC}$, V_{OUT} ($V_{OUT} \leq 3.3V$ with DIFF AMP), V_{OUT_LCL}, PGOOD, $EXTV_{CC}$ ..... –0.3V to 6V
MODE_PLLIN, f_{SET}, TRACK/SS, V_{OSNS}^-, V_{OSNS}^+, DIFF_OUT ..... –0.3V to $INTV_{CC}$
COMP, V_{FB} ..... –0.3V to 2.7V
RUN (Note 5) ..... –0.3V to 5V
$INTV_{CC}$ Peak Output Current (Note 6) 100mA
Internal Operating Temperature Range (Note 2) .....
E and I-Grades ..... –40°C to 125°C
MP-Grade ..... –55°C to 125°C
Storage Temperature Range ..... –55°C to 125°C
Reflow (Peak Body) Temperature ..... 250°C

PIN CONFIGURATION



BGA PACKAGE
133-LEAD (15mm × 15mm × 4.92mm)

$T_{J(MAX)}$ = 125°C, θ_{JA} = 17.9°C/W, $\theta_{JCbottom}$ = 5.9°C/W, θ_{JCtop} = 15°C/W, θ_{JB} = 6.1°C/W,
θ VALUES DETERMINED PER JESD 51-12 USING A JESD 51-9 DEFINED PCB
WEIGHT = 2.8g



LGA PACKAGE
133-LEAD (15mm × 15mm × 4.32mm)

$T_{J(MAX)}$ = 125°C, θ_{JA} = 16.6°C/W, $\theta_{JCbottom}$ = 4.6°C/W, θ_{JCtop} = 15°C/W, θ_{JB} = 5.1°C/W,
θ VALUES DETERMINED PER JESD 51-12 USING A JESD 51-9 DEFINED PCB
WEIGHT = 2.6g

ORDER INFORMATION

PART NUMBER	PAD OR BALL FINISH	PART MARKING* DEVICE	PART MARKING* FINISH CODE	PACKAGE TYPE	MSL RATING	TEMPERATURE RANGE (Note 2)
LTM4627EV#PBF	Au (RoHS)	LTM4627V	e4	LGA	3	–40°C to 125°C
LTM4627IV#PBF	Au (RoHS)	LTM4627V	e4	LGA	3	–40°C to 125°C
LTM4627EY#PBF	SAC305 (RoHS)	LTM4627Y	e1	BGA	3	–40°C to 125°C
LTM4627IY#PBF	SAC305 (RoHS)	LTM4627Y	e1	BGA	3	–40°C to 125°C
LTM4627IY	SnPb (63/37)	LTM4627Y	e0	BGA	3	–40°C to 125°C
LTM4627MPY#PBF	SAC305 (RoHS)	LTM4627Y	e1	BGA	3	–55°C to 125°C
LTM4627MPY	SnPb (63/37)	LTM4627Y	e0	BGA	3	–55°C to 125°C

Consult Marketing for parts specified with wider operating temperature ranges. *Device temperature grade is indicated by a label on the shipping container. Pad or ball finish code is per IPC/JEDEC J-STD-609.

- Terminal Finish Part Marking: www.linear.com/leadfree
- Recommended LGA and BGA PCB Assembly and Manufacturing Procedures: www.linear.com/umodule/pcbassembly
- LGA and BGA Package and Tray Drawings: www.linear.com/packaging

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the specified internal operating temperature range, otherwise specifications are at T_A = 25°C (Note 2), V_{IN} = 12V, per the typical application in Figure 18.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
V_{IN}	Input DC Voltage		●	4.5		20	V
$V_{OUT(DC)}$	Output Voltage, Total Variation with Line and Load	C_{IN} = 22µF × 3 C_{OUT} = 100µF Ceramic, 470µF POSCAP R_{FB} = 40.2k, MODE_PLLIN = GND V_{IN} = 5V to 20V, I_{OUT} = 0A to 15A (Note 4)	●	1.477	1.50	1.523	V
Input Specifications							
V_{RUN}	RUN Pin On Threshold	V_{RUN} Rising		1.1	1.25	1.4	V
V_{RUNHYS}	RUN Pin On Hysteresis				130		mV
$I_{Q(VIN)}$	Input Supply Bias Current	V_{IN} = 12V, V_{OUT} = 1.5V, Burst Mode Operation, I_{OUT} = 0.1A V_{IN} = 12V, V_{OUT} = 1.5V, Pulse-Skipping Mode, I_{OUT} = 0.1A V_{IN} = 12V, V_{OUT} = 1.5V, Switching Continuous, I_{OUT} = 0.1A Shutdown, RUN = 0, V_{IN} = 12V			17 25 54 40		mA mA mA µA
$I_{S(VIN)}$	Input Supply Current	V_{IN} = 5V, V_{OUT} = 1.5V, I_{OUT} = 15A V_{IN} = 12V, V_{OUT} = 1.5V, I_{OUT} = 15A			5.05 2.13		A A
Output Specifications							
$I_{OUT(DC)}$	Output Continuous Current Range	V_{IN} = 12V, V_{OUT} = 1.5V (Note 4)		0		15	A
$\frac{\Delta V_{OUT}\ (Line)}{V_{OUT}}$	Line Regulation Accuracy	V_{OUT} = 1.5V, V_{IN} from 4.5V to 20V I_{OUT} = 0A	●		0.02	0.06	%/V
$\frac{\Delta V_{OUT}\ (Load)}{V_{OUT}}$	Load Regulation Accuracy	V_{OUT} = 1.5V, I_{OUT} = 0A to 15A, V_{IN} = 12V (Note 4)	●		0.2	0.45	%
$V_{OUT(AC)}$	Output Ripple Voltage	I_{OUT} = 0A, C_{OUT} = 100µF Ceramic, 470µF POSCAP V_{IN} = 12V, V_{OUT} = 1.5V			15		mV_{P-P}
$\Delta V_{OUT(START)}$	Turn-On Overshoot	C_{OUT} = 100µF Ceramic, 470µF POSCAP, V_{OUT} = 1.5V, I_{OUT} = 0A, V_{IN} = 12V			20		mV
t_{START}	Turn-On Time	C_{OUT} = 100µF Ceramic, 470µF POSCAP, No Load, TRACK/SS = 0.001µF, V_{IN} = 12V			0.6		ms
ΔV_{OUTLS}	Peak Deviation for Dynamic Load	Load: 0% to 50% to 0% of Full Load C_{OUT} = 100µF Ceramic, 470µF POSCAP, V_{IN} = 12V, V_{OUT} = 1.5V			60		mV
t_{SETTLE}	Settling Time for Dynamic Load Step	Load: 0% to 50% to 0% of Full Load V_{IN} = 5V, C_{OUT} = 100µF Ceramic, 470µF POSCAP			20		µs
I_{OUTPK}	Output Current Limit	V_{IN} = 12V, V_{OUT} = 1.5V V_{IN} = 5V, V_{OUT} = 1.5V			25 25		A A
Control Section							
V_{FB}	Voltage at V_{FB} Pin	I_{OUT} = 0A, V_{OUT} = 1.5V	●	0.594	0.60	0.606	V
I_{FB}	Current at V_{FB} Pin	(Note 7)			–12	–25	nA
V_{OVL}	Feedback Overvoltage Lockout		●	0.65	0.67	0.69	V
$I_{TRACK/SS}$	Track Pin Soft-Start Pull-Up Current	TRACK/SS = 0V		1.0	1.2	1.4	µA
$t_{ON(MIN)}$	Minimum On-Time	(Note 3)			90		ns
R_{FBHI}	Resistor Between V_{OUT_LCL} and V_{FB} Pins			60.05	60.40	60.75	kΩ
V_{OSNS^+}, V_{OSNS^-} CM RANGE	Common Mode Input Range	V_{IN} = 12V, Run > 1.4V		0		4	V
$V_{DIFF\_OUT(MAX)}$	Maximum DIFF_OUT Voltage	I_{DIFF_OUT} = 300µA		$INTV_{CC}$ – 1.4			V

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the specified internal operating temperature range, otherwise specifications are at T_A = 25°C (Note 2), V_{IN} = 12V, per the typical application in Figure 18.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
V_{OS}	Input Offset Voltage	V_{OSNS^+} = V_{DIFF_OUT} = 1.5V, I_{DIFF_OUT} = 100µA				2	mV
A_V	Differential Gain	(Note 7)			1		V/V
SR	Slew Rate	(Note 6)			2		V/µs
GBP	Gain Bandwidth Product	(Note 6)			3		MHz
CMRR	Common Mode Rejection	(Note 7)			60		dB
I_{DIFF_OUT}	DIFF_OUT Current	Sourcing		2			mA
PSRR	Power Supply Rejection Ratio	5V < V_{IN} < 20V (Note 7)			100		dB
R_{IN}	Input Resistance	V_{OSNS}+ to GND			80		kΩ
V_{PGOOD}	PGOOD Trip Level	V_{FB} With Respect to Set Output V_{FB} Ramping Negative V_{FB} Ramping Positive			 –10 10		 % %
V_{PGL}	PGOOD Voltage Low	I_{PGOOD} = 2mA			0.1	0.3	V
$INTV_{CC}$ Linear Regulator							
V_{INTVCC}	Internal V_{CC} Voltage	6V < V_{IN} < 20V		4.8	5	5.2	V
V_{INTVCC} Load Reg	$INTV_{CC}$ Load Regulation	I_{CC} = 0 to 50mA			0.5		%
V_{EXTVCC}	External V_{CC} Switchover	$EXTV_{CC}$ Ramping Positive	●	4.5	4.7		V
VLDO Ext	$EXTV_{CC}$ Voltage Drop	I_{CC} = 25mA, V_{EXTVCC} = 5V			50	100	mV
Oscillator and Phase-Locked Loop							
f_{SYNC}	Frequency Sync Capture Range	MODE_PLLIN Clock Duty Cycle = 50%		250		800	kHz
f_{NOM}	Nominal Frequency	V_{fSET} = 1.2V		450	500	550	kHz
f_{LOW}	Lowest Frequency	V_{fSET} = 1V		350	400	450	kHz
f_{HIGH}	Highest Frequency	V_{fSET} ≥ 2.4V		700	770	850	kHz
I_{FREQ}	Frequency Set Current			9	10	11	µA
R_{MODE_PLLIN}	MODE_PLLIN Input Resistance				250		kΩ
$V_{IH\_MODE\_PLLIN}$	Clock Input Level High			2.0			V
$V_{IL\_MODE\_PLLIN}$	Clock Input Level Low					0.8	V

Note 1: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

Note 2: The LTM4627 is tested under pulsed load conditions such that $T_J \approx T_A$. The LTM4627E is guaranteed to meet performance specifications over the 0°C to 125°C internal operating temperature range. Specifications over the –40°C to 125°C internal operating temperature range are assured by design, characterization and correlation with statistical process controls. The LTM4627I is guaranteed to meet specifications over the –40°C to 125°C internal operating temperature range. The LTM4627MP is guaranteed and tested over the –55°C to 125°C internal operating temperature range. Note that the maximum ambient temperature consistent with these specifications is determined by specific operating conditions in conjunction with board layout, the rated package thermal resistance and other environmental factors.

Note 3: The minimum on-time condition is specified for a peak-to-peak inductor ripple current of ~40% of I_{MAX} Load. (See the Applications Information section)

Note 4: See output current derating curves for different V_{IN}, V_{OUT} and T_A.

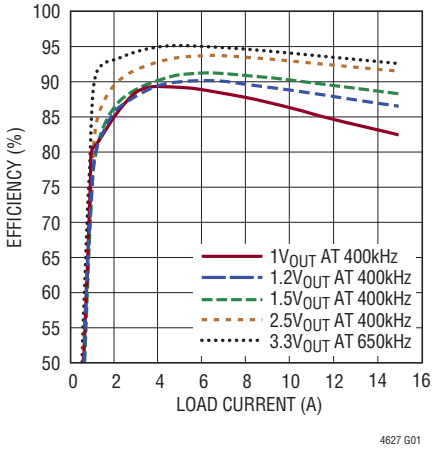
Note 5: Limit current into the RUN pin to less than 2mA.

Note 6: Guaranteed by design.

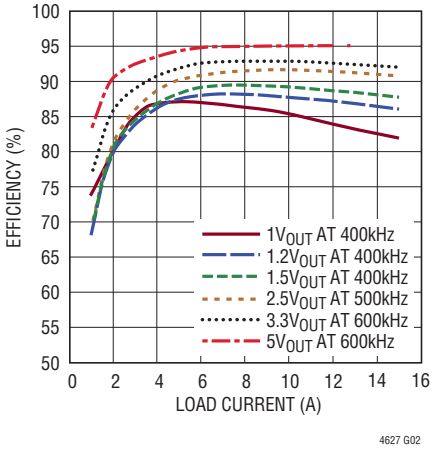
Note 7: 100% tested at wafer level.

TYPICAL PERFORMANCE CHARACTERISTICS

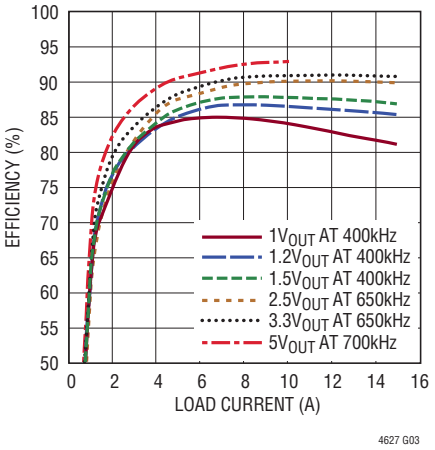
Efficiency vs Load Current with $5V_{IN}$



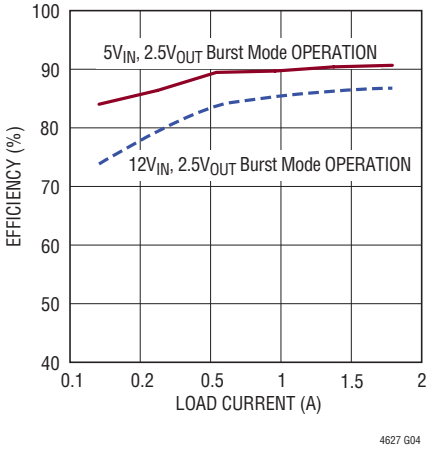
Efficiency vs Load Current with $8V_{IN}$



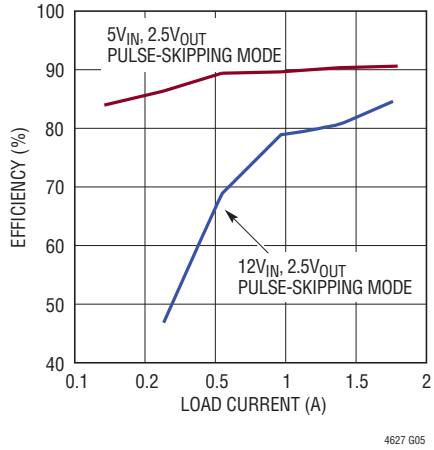
Efficiency vs Load Current with $12V_{IN}$



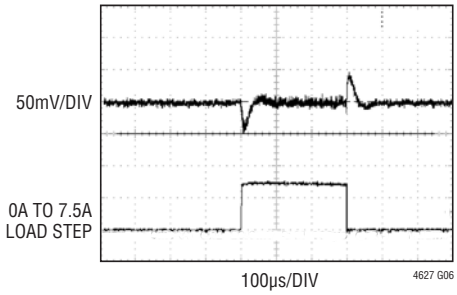
Burst Mode Efficiency



Pulse-Skipping Mode Efficiency

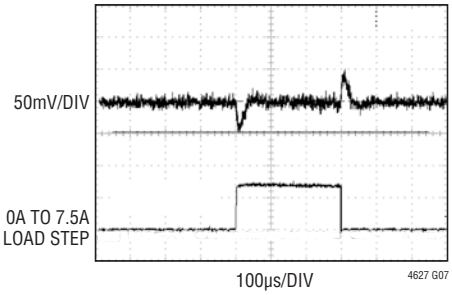


1.0V Transient Response



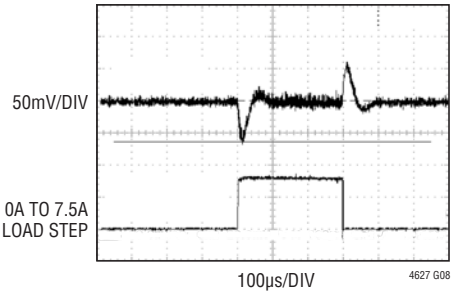
V_{IN} = 12V, V_{OUT} = 1.0V,
C_{FF} = 82pF, C_{COMP} = 33pF
OUTPUT CAPACITOR = 5 × 100µF CERAMIC X5R

1.2V Transient Response



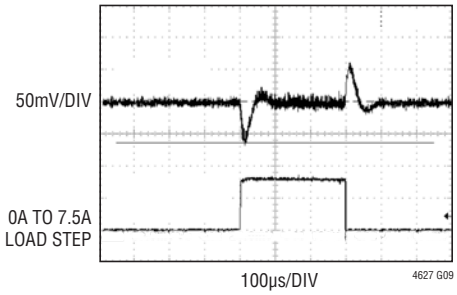
V_{IN} = 12V, V_{OUT} = 1.2V,
C_{FF} = 82pF, C_{COMP} = 33pF
OUTPUT CAPACITOR = 5 × 100µF CERAMIC X5R

1.5V Transient Response



V_{IN} = 12V, V_{OUT} = 1.5V,
C_{FF} = 82pF, C_{COMP} = 33pF
OUTPUT CAPACITOR = 5 × 100µF CERAMIC X5R

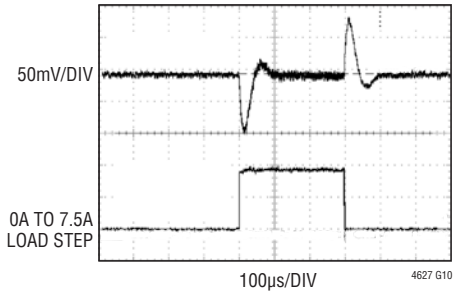
1.8V Transient Response



V_{IN} = 12V, V_{OUT} = 1.8V,
C_{FF} = 82pF, C_{COMP} = 33pF
OUTPUT CAPACITOR = 4 × 100µF CERAMIC X5R

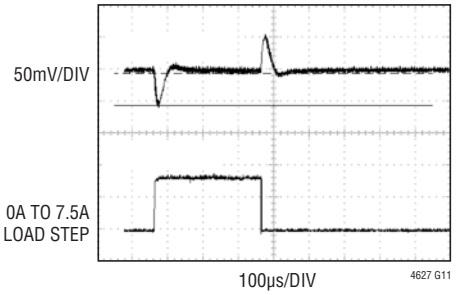
TYPICAL PERFORMANCE CHARACTERISTICS

2.5V Transient Response



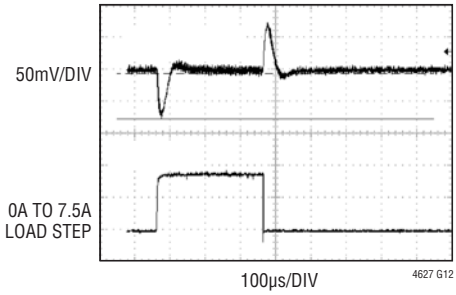
V_{IN} = 12V, V_{OUT} = 2.5V,
C_{FF} = 82pF, C_{COMP} = 33pF
OUTPUT CAPACITOR = 4 × 100µF CERAMIC X5R

3.3V Transient Response



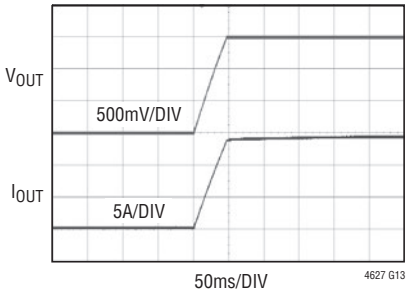
V_{IN} = 12V, V_{OUT} = 3.3V,
C_{FF} = 82pF, C_{COMP} = 33pF
OUTPUT CAPACITOR = 2 × 100µF CERAMIC X5R

5.0V Transient Response



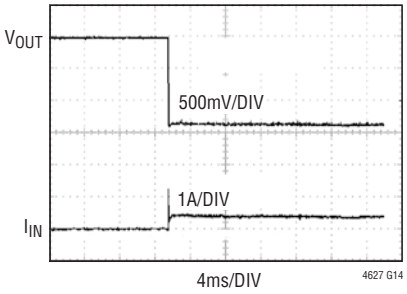
V_{IN} = 12V, V_{OUT} = 5V,
C_{FF} = 82pF, C_{COMP} = 33pF
OUTPUT CAPACITOR = 2 × 100µF CERAMIC X5R

Start-Up with Soft-Start



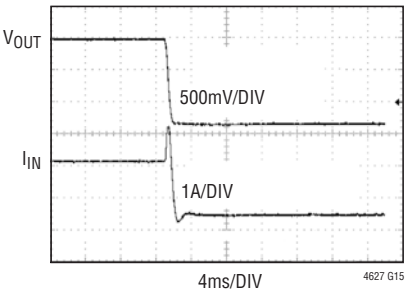
V_{IN} = 12V, V_{OUT} = 1.5V, I_{OUT} = 15A
INPUT CAP 150µF SANYO ELECTROLYTIC CAP
AND 22µF × 2 X5R CERAMIC CAP
OUTPUT CAP 1 × 100µF X5R CERAMIC
AND 470µF SANYO POSCAP
0.1µF CAP FROM TRACK/SS TO GND

Short-Circuit Protection No Load



V_{IN} = 12V, V_{OUT} = 1.5V, I_{OUT} = 0A

Short-Circuit Protection 15A Load



V_{IN} = 12V, V_{OUT} = 1.5V, I_{OUT} = 15A

PIN FUNCTIONS

V_{IN} (A1-A6, B1-B6, C1-C6): Power Input Pins. Apply input voltage between these pins and GND pins. Recommend placing input decoupling capacitance directly between V_{IN} pins and GND pins.

V_{OUT} (J1-J10, K1-K11, L1-L11, M1-M11): Power Output Pins. Apply output load between these pins and GND pins. Recommend placing output decoupling capacitance directly between these pins and GND pins. Review Table 4.

GND (B7, B9, C7, C9, D1-D6, D8, E1-E7, E9, F1-F9, G1-G9, H1-H9): Power Ground Pins for Both Input and Output Returns.

PGOOD (F11, G12): Output Voltage Power Good Indicator. Open-drain logic output that is pulled to ground when the output voltage exceeds a ±10% regulation window. Both pins are tied together internally.

SGND (G11, H11, H12): Signal Ground Pin. Return ground path for all analog and low power circuitry. Tie a single connection to the output capacitor GND in the application. See layout guidelines in Figure 17.

MODE_PLLIN (A8): Forced Continuous Mode, Burst Mode Operation, or Pulse-Skipping Mode Selection Pin and External Synchronization Input to Phase Detector Pin. Connect this pin to $INTV_{CC}$ to enable pulse-skipping mode of operation. Connect to ground to enable forced continuous mode of operation. Floating this pin will enable Burst Mode operation. A clock on this pin will enable synchronization with forced continuous operation. See the Applications Information section.

f_{SET} (B12): A resistor can be applied from this pin to ground to set the operating frequency, or a DC voltage can be applied to set the frequency. See the Applications Information section.

TRACK/SS (A9): Output Voltage Tracking Pin and Soft-Start Inputs. The pin has a 1.2µA pull-up current source. A capacitor from this pin to ground will set a soft-start ramp rate. In tracking, the regulator output can be tracked to a different voltage. The different voltage is applied to a voltage divider then the slave output's track pin. This voltage divider is equal to the slave output's feedback divider for coincidental tracking. See the Applications Information section.

V_{FB} (F12): The Negative Input of the Error Amplifier. Internally, this pin is connected to V_{OUT_LCL} with a 60.4k precision resistor. Different output voltages can be programmed with an additional resistor between V_{FB} and ground pins. In PolyPhase® operation, tying the V_{FB} pins together allows for parallel operation. See the Applications Information section for details.

COMP (A11): Current Control Threshold and Error Amplifier Compensation Point. The current comparator threshold increases with this control voltage. Tie all COMP pins together for parallel operation. The device is internally compensated.

RUN: (A10) Run Control Pin. A voltage above 1.4V will turn on the module. A 5.1V Zener diode to ground is internal to the module for limiting the voltage on the RUN pin to 5V, and allowing a pull-up resistor to V_{IN} for enabling the device. Limit current into the RUN pin to ≤ 2mA.

$INTV_{CC}$: (A7, D9) Internal 5V LDO for Driving the Control Circuitry and the Power MOSFET Drivers. Both pins are internally connected. The 5V LDO has a 100mA current limit.

$EXTV_{CC}$ (E12): External power input to an internal control switch allows an external source greater than 4.7V, but less than 6V to supply IC power and bypass the internal $INTV_{CC}$ LDO. $EXTV_{CC}$ must be less than V_{IN} at all times during power-on and power-off sequences. See the Applications Information section.

PIN FUNCTIONS

V_{OUT_LCL}: (L12) This pin connects to V_{OUT} through a 1M resistor, and to V_{FB} with a 60.4k resistor. The remote sense amplifier output DIFF_OUT is connected to V_{OUT_LCL}, and drives the 60.4k top feedback resistor in remote sensing applications. When the remote sense amplifier is used, DIFF_OUT effectively eliminates the 1MΩ from V_{OUT} to V_{OUT_LCL}. When the remote sense amplifier is not used, then connect V_{OUT_LCL} to V_{OUT} directly.

V_{OSNS}^{+}: (J12) (+) Input to the Remote Sense Amplifier. This pin connects to the output remote sense point. The remote sense amplifier is used for $V_{OUT} \leq 3.3V$. Connect to ground when not used.

V_{OSNS}^{-}: (M12) (–) Input to the Remote Sense Amplifier. This pin connects to the ground remote sense point. The remote sense amplifier is used for $V_{OUT} \leq 3.3V$. Connect to ground when not used.

DIFF_OUT: (K12) Output of the Remote Sense Amplifier. This pin connects to the V_{OUT_LCL} pin for remote sense applications. Otherwise float when not used.

MTP1, MTP2, MTP3, MTP4, MTP5, MTP6, MTP7, MTP8 (A12, B11, C10, C11, C12, D10, D11, D12): Extra mounting pads used for increased solder integrity strength. Leave floating.

BLOCK DIAGRAM

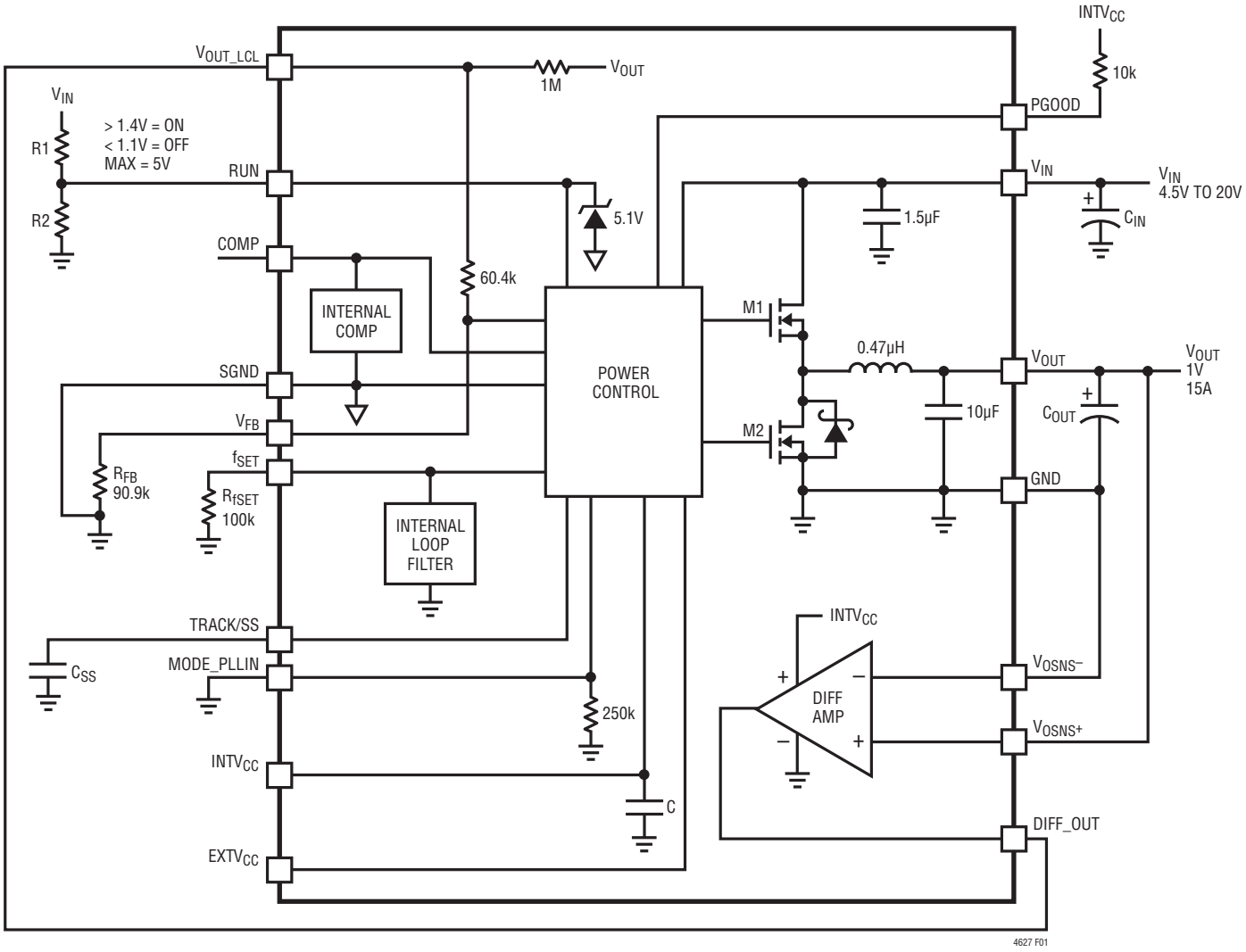


Figure 1. Simplified LTM4627 Block Diagram

DECOUPLING REQUIREMENTS

T_A = 25°C. Use Figure 1 configuration.

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
C_{IN}	External Input Capacitor Requirement (V_{IN} = 4.5V to 20V, V_{OUT} = 1.5V)	I_{OUT} = 15A	66			µF
C_{OUT}	External Output Capacitor Requirement (V_{IN} = 4.5V to 20V, V_{OUT} = 1.5V)	I_{OUT} = 15A		200		µF

OPERATION

Power Module Description

The LTM4627 is a high performance single output standalone nonisolated switching mode DC/DC power supply. It can provide a 15A output with few external input and output capacitors. This module provides precisely regulated output voltages programmable via external resistors from $0.6V_{DC}$ to $5V_{DC}$ over a 4.5V to 20V input range. The typical application schematic is shown in Figure 18.

The LTM4627 has an integrated constant-frequency current mode regulator, power MOSFETs, 0.47µH inductor, and other supporting discrete components. The switching frequency range is from 400kHz to 770kHz, and the typical operating frequency is 500kHz. For switching noise-sensitive applications, it can be externally synchronized from 250kHz to 800kHz, subject to minimum on-time limitations. A single resistor is used to program the frequency. See the Applications Information section.

With current mode control and internal feedback loop compensation, the LTM4627 module has sufficient stability margins and good transient performance with a wide range of output capacitors, even with all ceramic output capacitors.

Current mode control provides cycle-by-cycle fast current limit in an overcurrent condition. An internal overvoltage monitor protects the output voltage in the event of an overvoltage >10%. The top MOSFET is turned off and the bottom MOSFET is turned on until the output is cleared.

Pulling the RUN pin below 1.1V forces the regulator into a shutdown state. The TRACK/SS pin is used for programming the output voltage ramp and voltage tracking during start-up. See the Application Information section.

The LTM4627 is internally compensated to be stable over all operating conditions. Table 4 provides a guideline for input and output capacitances for several operating conditions. LTpowerCAD™ is available for transient and stability analysis. The V_{FB} pin is used to program the output voltage with a single external resistor to ground.

A remote sense amplifier is provided for accurately sensing output voltages ≤3.3V at the load point.

Multiphase operation can be easily employed with the synchronization inputs using an external clock source. See application examples.

High efficiency at light loads can be accomplished with selectable Burst Mode operation using the MODE_PLLIN pin. These light load features will accommodate battery operation. Efficiency graphs are provided for light load operation in the Typical Performance Characteristics section.

APPLICATIONS INFORMATION

The typical LTM4627 application circuit is shown in Figure 18. External component selection is primarily determined by the maximum load current and output voltage. Refer to Table 4 for specific external capacitor requirements for particular applications.

V_{IN} to V_{OUT} Step-Down Ratios

There are restrictions in the V_{IN} to V_{OUT} step-down ratio that can be achieved for a given input voltage. The V_{IN} to V_{OUT} minimum dropout is a function of load current and at very low input voltage and high duty cycle applications output power may be limited as the internal top power MOSFET is not rated for 15A operation at higher ambient temperatures. At very low duty cycles the minimum 90ns on-time must be maintained. See the Frequency Adjustment section and temperature derating curves.

Output Voltage Programming

The PWM controller has an internal 0.6V ±1% reference voltage. As shown in the Block Diagram, a 60.4k internal feedback resistor connects the V_{OUT_LCL} and V_{FB} pins together. When the remote sense amplifier is used, then DIFF_OUT is connected to the V_{OUT_LCL} pin. If the remote sense amplifier is not used, then V_{OUT_LCL} connects to V_{OUT}. The output voltage will default to 0.6V with no feedback resistor. Adding a resistor R_{FB} from V_{FB} to ground programs the output voltage:

$$V_{OUT} = 0.6V \bullet \frac{60.4k + R_{FB}}{R_{FB}}$$

Table 1. V_{FB} Resistor Table vs Various Output Voltages

V_{OUT} (V)	0.6	1.0	1.2	1.5	1.8	2.5	3.3	5.0
R_{FB} (k)	Open	90.9	60.4	40.2	30.1	19.1	13.3	8.25

For a given V_{OUT}, R_{FB} can be determined by:

$$R_{FB} = \frac{60.4k}{\frac{V_{OUT}}{0.6V} - 1}$$

For parallel operation of N LTM4627s, the following equation can be used to solve for R_{FB}:

$$R_{FB} = \frac{60.4k / N}{\frac{V_{OUT}}{0.6V} - 1}$$

Tie the V_{FB} pins together for each parallel output. The COMP pins must be tied together also.

Input Capacitors

The LTM4627 module should be connected to a low AC-impedance DC source. Additional input capacitors are needed for the RMS input ripple current rating. The $I_{CIN(RMS)}$ equation which follows can be used to calculate the input capacitor requirement. Typically 22µF X7R ceramics are a good choice with RMS ripple current ratings of ~ 2A each. A 47µF to 100µF surface mount aluminum electrolytic bulk capacitor can be used for more input bulk capacitance. This bulk input capacitor is only needed if the input source impedance is compromised by long inductive leads, traces or not enough source capacitance. If low impedance power planes are used, then this bulk capacitor is not needed.

For a buck converter, the switching duty cycle can be estimated as:

$$D = \frac{V_{OUT}}{V_{IN}}$$

Without considering the inductor ripple current, for each output, the RMS current of the input capacitor can be estimated as:

$$I_{CIN(RMS)} = \frac{I_{OUT(MAX)}}{\eta\%} \bullet \sqrt{D \bullet (1 - D)}$$

In the previous equation, η% is the estimated efficiency of the power module. The bulk capacitor can be a switcher-rated electrolytic aluminum capacitor or a Polymer capacitor.

APPLICATIONS INFORMATION

Output Capacitors

The LTM4627 is designed for low output voltage ripple noise. The bulk output capacitors defined as C_{OUT} are chosen with low enough effective series resistance (ESR) to meet the output voltage ripple and transient requirements. C_{OUT} can be a low ESR tantalum capacitor, low ESR Polymer capacitor or ceramic capacitors. The typical output capacitance range is from 200µF to 800µF. Additional output filtering may be required by the system designer if further reduction of output ripple or dynamic transient spikes is required. Table 4 shows a matrix of different output voltages and output capacitors to minimize the voltage droop and overshoot during a 7.5A/µs transient. The table optimizes total equivalent ESR and total bulk capacitance to optimize the transient performance. Stability criteria are considered in the Table 4 matrix, and LTpowerCAD is available for stability analysis. Multiphase operation will reduce effective output ripple as a function of the number of phases. Application Note 77 discusses this noise reduction versus output ripple current cancellation, but the output capacitance should be considered carefully as a function of stability and transient response. LTpowerCAD can be used to calculate the output ripple reduction as the number of implemented phases increases by N times.

Burst Mode Operation

The LTM4627 is capable of Burst Mode operation in which the power MOSFETs operate intermittently based on load demand, thus saving quiescent current. For applications where maximizing the efficiency at very light loads is a high priority, Burst Mode operation should be applied. To enable Burst Mode operation, simply float the MODE_PLLIN pin. During Burst Mode operation, the peak current of the inductor is set to approximately 30% of the maximum peak current value in normal operation even though the voltage at the COMP pin indicates a lower value. The voltage at the COMP pin drops when the inductor's average current is greater than the load requirement. As the COMP voltage drops below 0.5V, the burst comparator trips, causing the internal sleep line to go high and turn off both power MOSFETs.

In sleep mode, the internal circuitry is partially turned off, reducing the quiescent current. The load current is now being supplied from the output capacitors. When the output voltage drops, causing COMP to rise, the internal sleep line goes low, and the LTM4627 resumes normal operation. The next oscillator cycle will turn on the top power MOSFET and the switching cycle repeats.

Pulse-Skipping Mode Operation

In applications where low output ripple and high efficiency at intermediate currents are desired, pulse-skipping mode should be used. Pulse-skipping operation allows the LTM4627 to skip cycles at low output loads, thus increasing efficiency by reducing switching loss. Tying the MODE_PLLIN pin to $INTV_{CC}$ enables pulse-skipping operation. With pulse-skipping mode at light load, the internal current comparator may remain tripped for several cycles, thus skipping operation cycles. This mode has lower ripple than Burst Mode operation and maintains a higher frequency operation than Burst Mode operation.

Forced Continuous Operation

In applications where fixed frequency operation is more critical than low current efficiency, and where the lowest output ripple is desired, forced continuous operation should be used. Forced continuous operation can be enabled by tying the MODE_PLLIN pin to ground. In this mode, inductor current is allowed to reverse during low output loads, the COMP voltage is in control of the current comparator threshold throughout, and the top MOSFET always turns on with each oscillator pulse. During start-up, forced continuous mode is disabled and inductor current is prevented from reversing until the LTM4627's output voltage is in regulation.

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Multiphase Operation

For outputs that demand more than 15A of load current, multiple LTM4627 devices can be paralleled to provide more output current without increasing input and output ripple voltage. The MODE_PLLIN pin allows the LTM4627 to be synchronized to an external clock and the internal phase-locked loop allows the LTM4627 to lock onto input clock phase as well. The f_{SET} resistor is selected for normal frequency, then the incoming clock can synchronize the device over the specified range. See Figure 20 for a synchronizing example circuit.

A multiphase power supply significantly reduces the amount of ripple current in both the input and output capacitors. The RMS input ripple current is reduced by, and the effective ripple frequency is multiplied by, the number of phases used (assuming that the input voltage is greater than the number of phases used times the output voltage). The output ripple amplitude is also reduced by the number of phases used. See Application Note 77.

The LTM4627 device is an inherently current mode controlled device, so parallel modules will have good current sharing. This will balance the thermals in the design. Tie the COMP and V_{FB} pins of each LTM4627 together to share the current evenly. Figure 20 shows a schematic of the parallel design.

Input RMS Ripple Current Cancellation

Application Note 77 provides a detailed explanation of multiphase operation. The input RMS ripple current cancellation mathematical derivations are presented, and a graph is displayed representing the RMS ripple current reduction as a function of the number of interleaved phases (see Figure 2).

PLL, Frequency Adjustment and Synchronization

The LTM4627 switching frequency is set by a resistor (R_{fSET}) from the f_{SET} pin to signal ground. A 10µA current (I_{FREQ}) flowing out of the f_{SET} pin through R_{fSET} develops a voltage on f_{SET}. R_{fSET} can be calculated as:

$$R_{fSET} = \left[\frac{FREQ}{500kHz/V} + 0.2V\right]\frac{1}{10\mu A}$$

The relationship of f_{SET} voltage to switching frequency is shown in Figure 3. For low output voltages from 0.8V to 1.5V, 400kHz operation is an optimal frequency for the best power conversion efficiency while maintaining the inductor ripple current to about 30% to 40% of maximum load current. For output voltages from 1.8V to 3.0V, 500kHz to 600kHz is optimal. For output voltages from 3.0V to 5.0V, 750kHz operation is optimal, but due to the higher ripple current at 5V operation the output current is limited to 10A.

The LTM4627 can be synchronized from 250kHz to 800kHz with an input clock that has a high level above 2V and a low level below 0.8V. However, a 400kHz low end operating frequency is recommended to limit inductor ripple current. See the Typical Applications section for synchronization examples. The LTM4627 minimum on-time is limited to approximately 90ns. Guardband the on-time to 130ns. The on-time can be calculated as:

$$t_{ON(MIN)} = \frac{1}{FREQ} \bullet \left(\frac{V_{OUT}}{V_{IN}}\right)$$

Output Voltage Tracking

Output voltage tracking can be programmed externally using the TRACK/SS pin. The output can be tracked up and down with another regulator. The master regulator's output is divided down with an external resistor divider that is the same as the slave regulator's feedback divider to implement coincident tracking. The LTM4627 uses an accurate 60.4k resistor internally for the top feedback resistor. Figure 4 shows an example of coincident tracking.

$$V_{OUT(SLAVE)} = \left(1 + \frac{60.4k}{R_{TA}}\right) \bullet V_{TRACK}$$

V_{TRACK} is the track ramp applied to the slave's track pin. V_{TRACK} has a control range of 0V to 0.6V, or the internal reference voltage. When the master's output is divided down with the same resistor values used to set the slave's output, then the slave will coincident track with the master until it reaches its final value. The master will continue to

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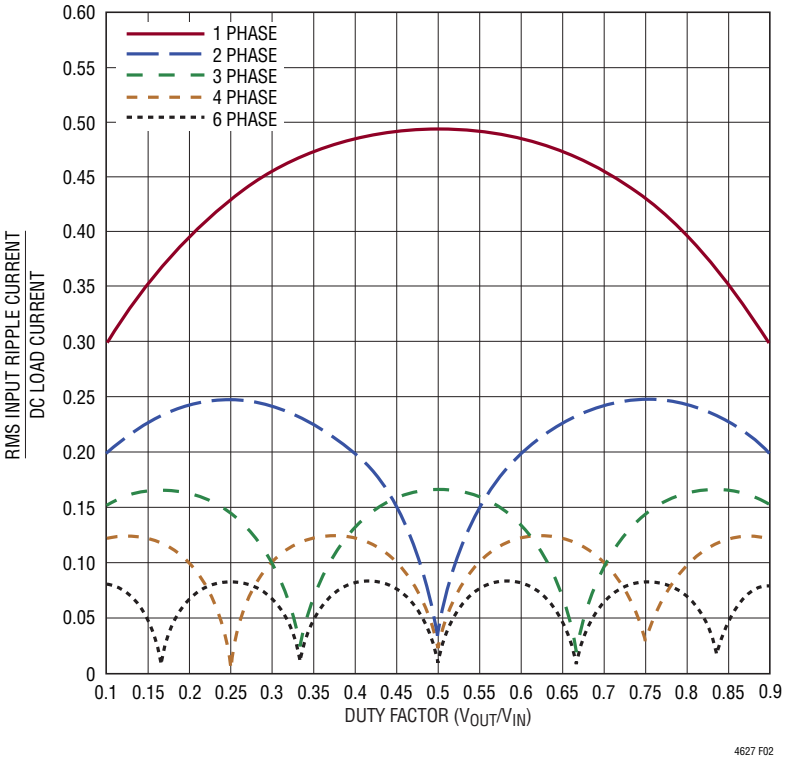

Figure 2. Normalized Input RMS Ripple Current vs Duty Factor for One to Six µModule Regulators (Phases)

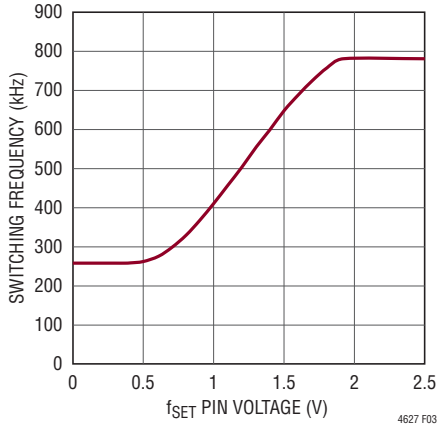

Figure 3. Relationship Between Switching Frequency and Voltage at the f_{SET} Pin

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its final value from the slave's regulation point. Voltage tracking is disabled when V_{TRACK} is more than 0.6V. R_{TA} in Figure 4 will be equal to the R_{FB} for coincident tracking.

The TRACK/SS pin of the master can be controlled by an external ramp or the soft-start function of that regulator can be used to develop that master ramp. The LTM4627 can be used as a master by setting the ramp rate on its track pin using a soft-start capacitor. A 1.2µA current source is used to charge the soft-start capacitor. The following equation can be used:

$$t_{SOFT\text{-}START} = 0.6V \bullet \left(\frac{C_{SS}}{1.2\mu A} \right)$$

Ratiometric tracking can be achieved by a few simple calculations and the slew rate value applied to the master's TRACK/SS pin. As mentioned above, the TRACK/SS pin has a control range from 0V to 0.6V. The master's TRACK/SS pin slew rate is directly equal to the master's output slew rate in volts/time. The equation:

$$\frac{MR}{SR} \bullet 60.4k = R_{TB}$$

where MR is the master's output slew rate and SR is the slave's output slew rate in volts/time. When coincident tracking is desired, then MR and SR are equal, thus R_{TB} is equal to 60.4k. R_{TA} is derived from equation:

$$R_{TA} = \frac{0.6V}{\frac{V_{FB}}{60.4k} + \frac{V_{FB}}{R_{FB}} - \frac{V_{TRACK}}{R_{TB}}}$$

where V_{FB} is the feedback voltage reference of the regulator, and V_{TRACK} is 0.6V. Since R_{TB} is equal to the 60.4k

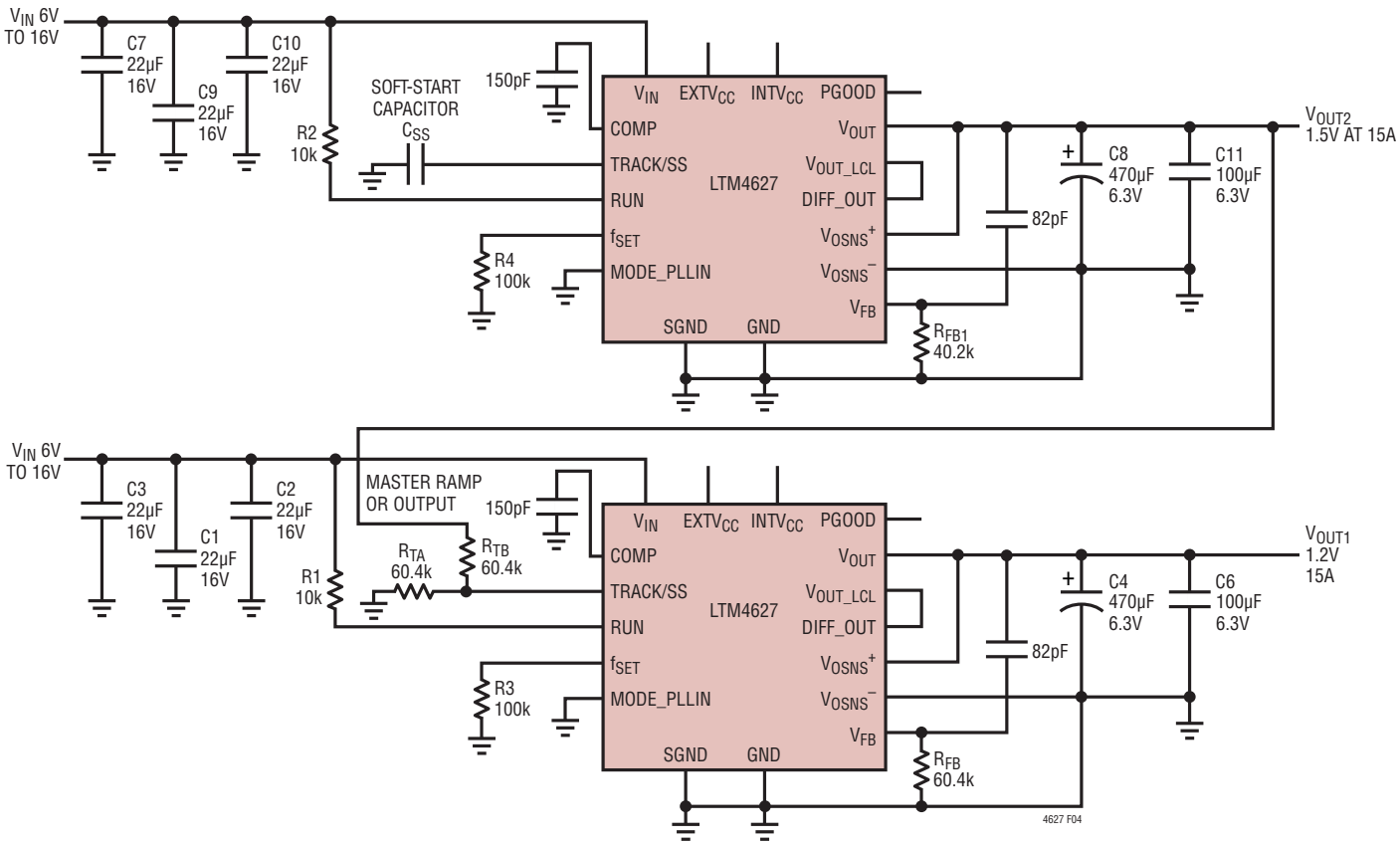

Figure 4. Dual Outputs (1.5V and 1.2V) with Coincident Tracking

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top feedback resistor of the slave regulator in equal slew rate or coincident tracking, then R_{TA} is equal to R_{FB} with $V_{FB} = V_{TRACK}$. Therefore R_{TB} = 60.4k, and R_{TA} = 60.4k in Figure 4.

In ratiometric tracking, a different slew rate maybe desired for the slave regulator. R_{TB} can be solved for when SR is slower than MR. Make sure that the slave supply slew rate is chosen to be fast enough so that the slave output voltage will reach its final value before the master output.

For example, MR = 1.5V/ms, and SR = 1.2V/ms. Then R_{TB} = 75k. Solve for R_{TA} to equal 51.1k.

For applications that do not require tracking or sequencing, simply tie the TRACK/SS pin to $INTV_{CC}$ to let RUN control the turn on/off. When the RUN pin is below its threshold or the V_{IN} undervoltage lockout, then TRACK/SS is pulled low.

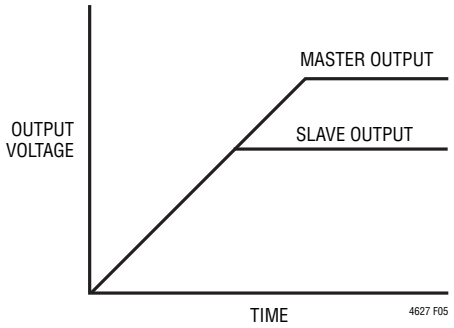

Figure 5. Output Voltage Coincident Tracking

Overcurrent and Overvoltage Protection

The LTM4627 has overcurrent protection (OCP) in a short circuit. The internal current comparator threshold folds back during a short to reduce the output current. An overvoltage condition (OVP) above 10% of the regulated output voltage will force the top MOSFET off and the bottom MOSFET on until the condition is cleared. An input electronic circuit breaker or fuse can be sized to be tripped or cleared when the bottom MOSFET is turned on to protect against the overvoltage. Foldback current limiting is disabled during soft-start or tracking start-up.

Run Enable

The RUN pin is used to enable the power module or sequence the power module. The threshold is 1.25V, and the pin has an internal 5.1V Zener to protect the pin. The RUN pin can be used as an undervoltage lockout (UVLO) function by connecting a resistor divider from the input supply to the RUN pin:

V_{UVLO} = ((R1+R2)/R2) • 1.25V.

See the Block Diagram for the example of use.

$INTV_{CC}$ Regulator

The LTM4627 has an internal low dropout regulator from V_{IN} called $INTV_{CC}$. This regulator output has a 4.7µF ceramic capacitor internal. This regulator powers the internal controller and MOSFET drivers. The gate driver current is ~20mA for 750kHz operation. The regulator loss can be calculated as:

$$(V_{IN} - 5V) \bullet 20mA = P_{LOSS}$$

$EXTV_{CC}$ external voltage source ≥ 4.7V can be applied to this pin to eliminate the internal $INTV_{CC}$ LDO power loss and increase regulator efficiency. A 5V supply can be applied to run the internal circuitry and power MOSFET driver. If unused, leave pin floating. $EXTV_{CC}$ must be less than V_{IN} at all times during power-on and power-off sequences.

Stability Compensation

The LTM4627 has already been internally compensated for all output voltages. Table 4 is provided for most application requirements. LTpowerCAD is available for other control loop optimization.

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Thermal Considerations and Output Current Derating

The thermal resistances reported in the Pin Configuration section of the data sheet are consistent with those parameters defined by JESD 51-12 and are intended for use with finite element analysis (FEA) software modeling tools that leverage the outcome of thermal modeling, simulation, and correlation to hardware evaluation performed on a µModule package mounted to a hardware test board defined by JESD 51-9 ("Test Boards for Area Array Surface Mount Package Thermal Measurements"). The motivation for providing these thermal coefficients is found in JESD 51-12 ("Guidelines for Reporting and Using Electronic Package Thermal Information").

Many designers, in lieu of or to compliment any FEA activities, may opt to use laboratory equipment and a test vehicle such as the demo board to anticipate the µModule regulator's thermal performance in their application at various electrical and environmental operating conditions. Without FEA software, the thermal resistances reported in the Pin Configuration section are in-and-of themselves not relevant to providing guidance of thermal performance; instead, the derating curves provided later in this data sheet can be used in a manner that yields insight and guidance pertaining to one's application-usage, and can be adapted to correlate thermal performance to one's own application.

The Pin Configuration section gives four thermal coefficients explicitly defined in JESD 51-12; these coefficients are quoted or paraphrased below:

1 θ_{JA}, the thermal resistance from junction to ambient, is the natural convection junction-to-ambient air thermal resistance measured in a one cubic foot sealed enclosure. This environment is sometimes referred to as "still air" although natural convection causes the air to move. This value is determined with the part mounted to a JESD 51-9 defined test board, which does not reflect an actual application or viable operating condition.

2 $\theta_{JCbottom}$, the thermal resistance from junction to the bottom of the product case, is determined with all of the component power dissipation flowing through the bottom of the package. In the typical µModule regulator, the bulk of the heat flows out the bottom of the package, but there is always heat flow out into the ambient environment. As a result, this thermal resistance value may be useful for comparing packages but the test conditions don't generally match the user's application.

3 θ_{JCtop}, the thermal resistance from junction to top of the product case, is determined with nearly all of the component power dissipation flowing through the top of the package. As the electrical connections of the typical µModule regulator are on the bottom of the package, it is rare for an application to operate such that most of the heat flows from the junction to the top of the part. As in the case of $\theta_{JCbottom}$, this value may be useful for comparing packages but the test conditions don't generally match the user's application.

4 θ_{JB}, the thermal resistance from junction to the printed circuit board, is the junction-to-board thermal resistance where almost all of the heat flows through the bottom of the µModule package and into the board, and is really the sum of the $\theta_{JCbottom}$ and the thermal resistance of the bottom of the part through the solder joints and through a portion of the board. The board temperature is measured at a specified distance from the package, using a two sided, two layer board. This board is described in JESD 51-9.

A graphical representation of the aforementioned thermal resistances is given in Figure 6; blue resistances are contained within the µModule regulator, whereas green resistances are external to the µModule package.

As a practical matter, it should be clear to the reader that no individual or sub-group of the four thermal resistance parameters defined by JESD 51-12 or provided in the Pin Configuration section replicates or conveys normal operating conditions of a µModule regulator. For example, in normal board-mounted applications, never does 100% of the device's total power loss (heat) thermally conduct exclusively through the top or exclusively through bottom of the µModule package—as the standard defines for θ_{JCtop} and $\theta_{JCbottom}$, respectively. In practice, power loss is thermally dissipated in both directions away from the package—granted, in the absence of a heat sink and airflow, a majority of the heat flow is into the board.

APPLICATIONS INFORMATION

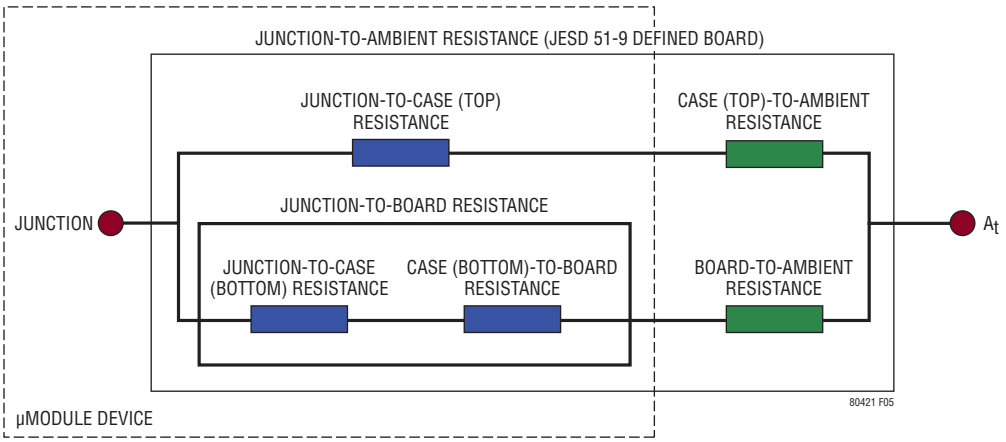

Figure 6. Graphical Representation of JESD 51-12 Thermal Coefficients

Within the LTM4627, be aware there are multiple power devices and components dissipating power, with a consequence that the thermal resistances relative to different junctions of components or die are not exactly linear with respect to total package power loss. To reconcile this complication without sacrificing modeling simplicity—but also, not ignoring practical realities—an approach has been taken using FEA software modeling along with laboratory testing in a controlled-environment chamber to reasonably define and correlate the thermal resistance values supplied in this data sheet: (1) Initially, FEA software is used to accurately build the mechanical geometry of the LTM4627 and the specified PCB with all of the correct material coefficients along with accurate power loss source definitions; (2) this model simulates a software-defined JEDEC environment consistent with JESD 51-12 to predict power loss heat flow and temperature readings at different interfaces that enable the calculation of the JEDEC-defined thermal resistance values; (3) the model and FEA software is used to evaluate the LTM4627 with heat sink and airflow; (4) having solved for and analyzed these thermal resistance values and simulated various operating conditions in the software model, a thorough laboratory evaluation replicates the simulated conditions with thermocouples within a controlled-environment chamber while operating the device at the same power loss as that which was simulated. An outcome of this process and due diligence yields the set of derating curves shown in this data sheet.

The 1.2V and 3.3V power loss curves in Figures 7 and 8 can be used in coordination with the load current derating curves in Figures 9 to 16 for calculating an approximate θ_{JA} thermal resistance for the LTM4627 with various heat sinking and airflow conditions. The power loss curves are taken at room temperature, and are increased with multiplicative factors according to the ambient temperature. These approximate factors are: 1 for 40°C; 1.05 for 50°C; 1.1 for 60°C; 1.15 for 70°C; 1.2 for 80°C; 1.25 for 90°C; 1.3 for 100°C; 1.35 for 110°C and 1.4 for 120°C. The derating curves are plotted with the output current starting at 15A and the ambient temperature at 40°C. The output voltages are 1.2V, and 3.3V. These are chosen to include the lower and higher output voltage ranges for correlating the thermal resistance. Thermal models are derived from several temperature measurements in a controlled temperature chamber along with thermal modeling analysis. The junction temperatures are monitored while ambient temperature is increased with and without airflow. The power loss increase with ambient temperature change is factored into the derating curves. The junctions are maintained at 120°C maximum while lowering output current or power with increasing ambient temperature. The decreased output current will decrease the internal module loss as ambient temperature is increased. The monitored junction temperature of 120°C minus the ambient operating temperature specifies how much module temperature rise can be allowed. As an example in

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Figure 11 the load current is derated to ~12A at ~80°C with no air or heat sink and the power loss for the 12V to 1.2V at 12A output is about 2.8W. The 2.8W loss is calculated with the ~2.35W room temperature loss from the 12V to 1.2V power loss curve at 12A, and the 1.2 multiplying factor at 80°C ambient. If the 80°C ambient temperature is subtracted from the 120°C junction temperature, then the difference of 40°C divided by 2.8W equals a 14°C/W θ_{JA} thermal resistance. Table 2 specifies a 13°C/W value which is very close. Table 2 and Table 3 provide equivalent thermal resistances for 1.2V and 3.3V outputs with and without airflow and heat sinking. The derived thermal resistances in Tables 2 and 3 for the various conditions can be multiplied by the calculated power loss as a function of ambient temperature to derive temperature rise above ambient, thus maximum junction temperature. Room temperature power loss can be derived from the efficiency curves in the Typical Performance Characteristics section and adjusted with the above ambient temperature multiplicative factors. The printed circuit board is a 1.6mm thick four layer board with two ounce copper for the two outer layers and one ounce copper for the two inner layers. The PCB dimensions are 95mm × 76mm. The BGA heat sinks are listed in Table 4.

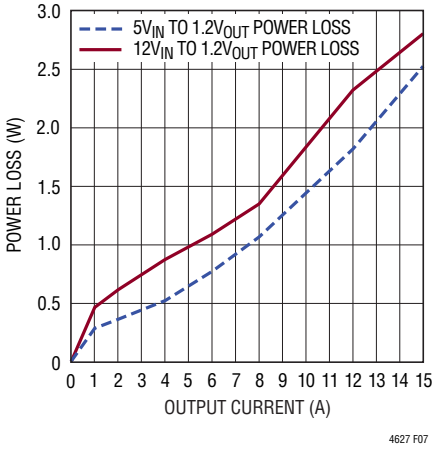


Figure 7. 1.2V_{OUT} Power Loss at 25°C

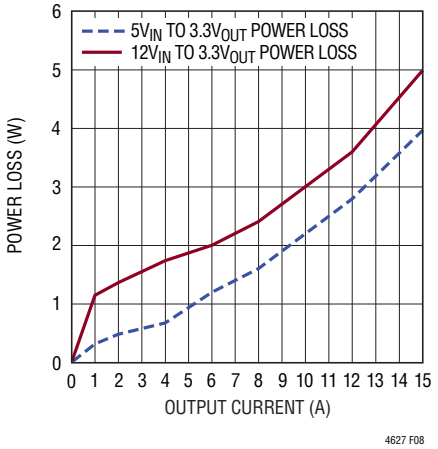


Figure 8. 3.3V_{OUT} Power Loss at 25°C

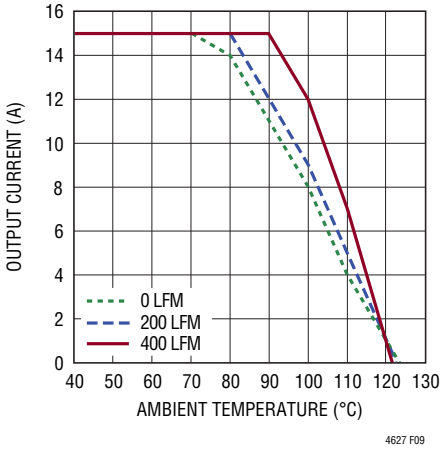


Figure 9. 5V_{IN} to 1.2V_{OUT} No Heat Sink

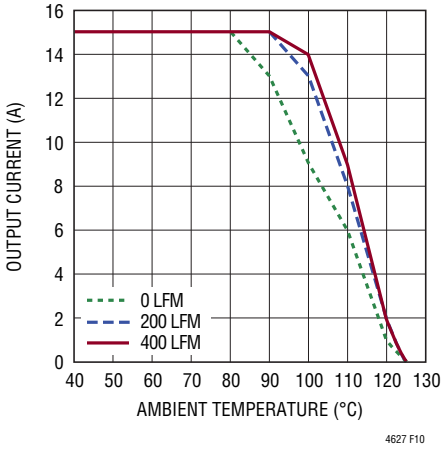


Figure 10. 5V_{IN} to 1.2V_{OUT} with Heat Sink

APPLICATIONS INFORMATION

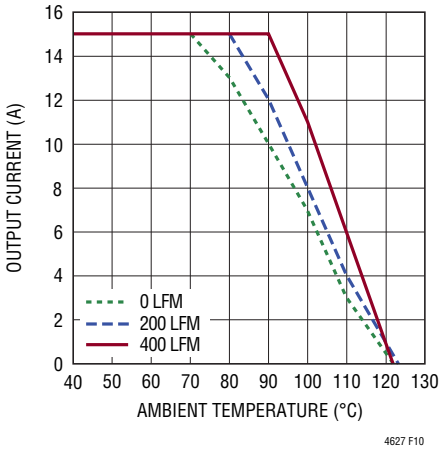


Figure 11. $12V_{IN}$ to $1.2V_{OUT}$ No Heat Sink

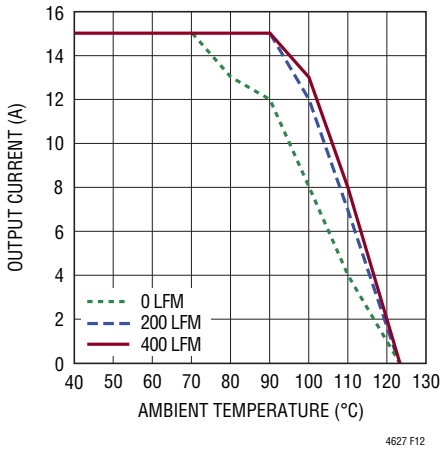


Figure 12. $12V_{IN}$ to $1.2V_{OUT}$ with Heat Sink

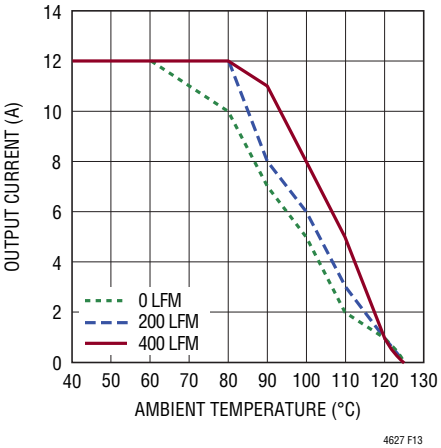


Figure 13. $5V_{IN}$ to $3.3V_{OUT}$ No Heat Sink

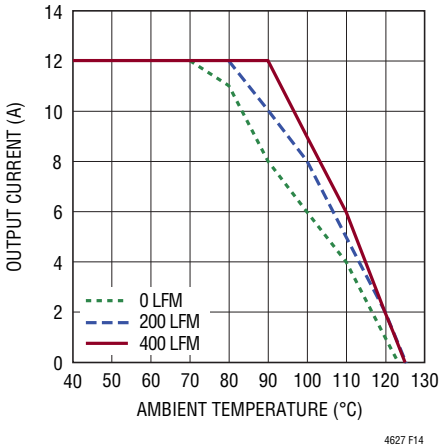


Figure 14. $5V_{IN}$ to $3.3V_{OUT}$ with Heat Sink

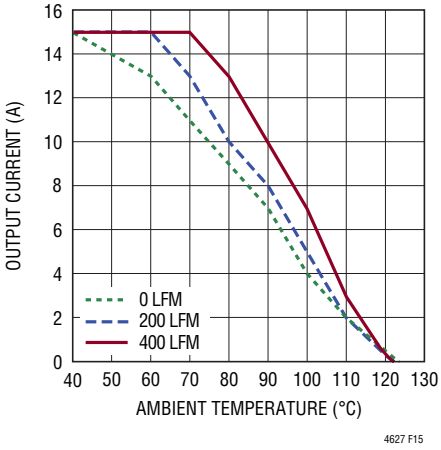


Figure 15. $12V_{IN}$ to $3.3V_{OUT}$ No Heat Sink

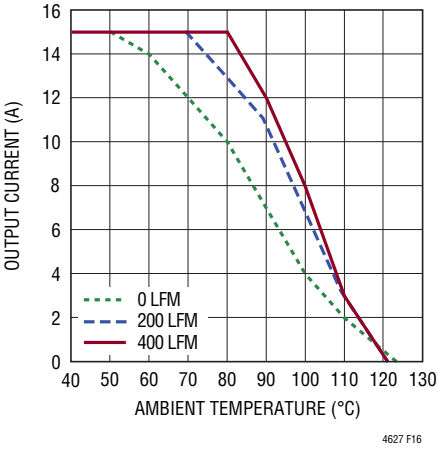


Figure 16. $12V_{IN}$ to $3.3V_{OUT}$ with Heat Sink

APPLICATIONS INFORMATION

Table 2. 1.2V Output

DERATING CURVE	V_{IN}	POWER LOSS CURVE	AIRFLOW (LFM)	HEAT SINK	θ_{JA} (°C/W)*
Figures 9, 11	5V, 12V	Figure 7	0	None	13
Figures 9, 11	5V, 12V	Figure 7	200	None	11
Figures 9, 11	5V, 12V	Figure 7	400	None	8
Figures 10, 12	5V, 12V	Figure 7	0	BGA Heat Sink	12
Figures 10, 12	5V, 12V	Figure 7	200	BGA Heat Sink	8
Figures 10, 12	5V, 12V	Figure 7	400	BGA Heat Sink	7

Table 3. 3.3V Output

DERATING CURVE	V_{IN}	POWER LOSS CURVE	AIRFLOW (LFM)	HEAT SINK	θ_{JA} (°C/W)*
Figures 13, 15	5V, 12V	Figure 8	0	None	13
Figures 13, 15	5V, 12V	Figure 8	200	None	11
Figures 13, 15	5V, 12V	Figure 8	400	None	8
Figures 14, 16	5V, 12V	Figure 8	0	BGA Heat Sink	12
Figures 14, 16	5V, 12V	Figure 8	200	BGA Heat Sink	8
Figures 14, 16	5V, 12V	Figure 8	400	BGA Heat Sink	7

* θ_{JA} derived from laboratory measurements using a 95mm × 76mm PCB with 4 layers. Two outer layers are 2oz copper and two inner layers are 1oz copper. PCB thickness is 1.6mm. BGA heat sink references are listed in Table 4.

APPLICATIONS INFORMATION

Table 4. Output Voltage Response vs Component Matrix (Refer to Figure 18) 0A to 7.5A Load Step

C_{OUT1} AND C_{OUT2} CERAMIC VENDOR	VALUE	PART NUMBER	C_{OUT1} AND C_{OUT2} BULK VENDOR	VALUE	PART NUMBER	C_{IN} BULK VENDOR	VALUE	PART NUMBER
TDK	22µF 6.3V	C3216X7SOJ226M	Sanyo POSCAP	1000µF 2.5V	2R5TPD1000M5	Sanyo	56µF 25V	25SVP56M
Murata	22µF 16V	GRM31CR61C226KE15L	Sanyo POSCAP	470µF 2.5V	2R5TPD470M5			
TDK	100µF 6.3V	C4532X5ROJ107MZ	Sanyo POSCAP	470µF 6.3V	6TPD470M			
Murata	100µF 6.3V	GRM32ER60J107M	Sanyo POSCAP					

V_{OUT} (V)	C_{IN} (CERAMIC)	C_{IN} (BULK)**	C_{OUT1} (CERAMIC) AND C_{OUT2} (CER AND BULK)	C_{FF} (pF)	C_{COMP} (pF)	V_{IN} (V)	DROOP (mV)	PEAK TO PEAK DEVIATION (mV)	RECOVERY TIME(µs)	LOAD STEP (A/µs)	R_{FB} (kΩ)	FREQ. (kHz)
1	22µF × 3	56µF	100µF × 2, 1000µF	68	150	5,12	50	100	30	7.5	90.9	400
1	22µF × 3	56µF	100µF × 2, 470µF × 2	82	150	5,12	50	100	20	7.5	90.9	400
1	22µF × 3	56µF	100µF × 4	82	33	5,12	52	108	18	7.5	90.9	400
1.2	22µF × 3	56µF	100µF × 2, 1000µF	82	150	5,12	40	80	20	7.5	60.4	400
1.2	22µF × 3	56µF	100µF, 470µF	82	150	5,12	60	120	20	7.5	60.4	400
1.2	22µF × 3	56µF	100µF × 2, 470µF × 2	82	150	5,12	40	80	25	7.5	60.4	400
1.2	22µF × 3	56µF	100µF × 4	82	33	5,12	50	114	20	7.5	60.4	400
1.5	22µF × 3	56µF	100µF × 2, 1000µF	82	150	5,12	60	120	23	7.5	40.2	400
1.5	22µF × 3	56µF	100µF, 470µF	82	47	5,12	67	130	20	7.5	40.2	400
1.5	22µF × 3	56µF	100µF × 2, 470µF × 2	82	150	5,12	60	120	25	7.5	40.2	400
1.5	22µF × 3	56µF	100µF × 3	82	33	5,12	65	130	20	7.5	40.2	400
1.8	22µF × 3	56µF	100µF × 2, 1000µF	68	150	5,12	64	130	25	7.5	30.1	400
1.8	22µF × 3	56µF	100µF, 470µF	82	150	5,12	76	135	22	7.5	30.1	400
1.8	22µF × 3	56µF	100µF × 2	82	none	5,12	66	132	20	7.5	30.1	400
2.5	22µF × 3	56µF	100µF × 2	82	none	5,12	88	164	30	7.5	19.1	500
2.5	22µF × 3	56µF	100µF, 470µF	82	150	5,12	100	200	25	7.5	19.1	500
3.3	22µF × 3	56µF	100µF × 2	82	none	5,12	100	200	30	7.5	13.3	600
3.3	22µF × 3	56µF	100µF, 470µF	82	150	5,12	100	200	30	7.5	13.3	600
5	22µF × 3	56µF	100µF × 2	68	none	12	125	250	20	7.5	8.25	700
5	22µF × 3	56µF	470µF	47	150	12	125	250	25	7.5	8.25	700

** Bulk capacitance is optional if V_{IN} has very low input impedance.

HEAT SINK MANUFACTURER	PART NUMBER	WEBSITE
AAVID Thermalloy	375424B00034G	www.aavidthermalloy.com
Cool Innovations	4-050503P to 4-050508P	www.coolinnovations.com

APPLICATIONS INFORMATION

Safety Considerations

The LTM4627 modules do not provide isolation from V_{IN} to V_{OUT}. There is no internal fuse. If required, a slow blow fuse with a rating twice the maximum input current needs to be provided to protect each unit from catastrophic failure. The device does support overvoltage protection and overcurrent protection.

Layout Checklist/Example

The high integration of the LTM4627 makes the PCB board layout very simple and easy. However, to optimize its electrical and thermal performance, some layout considerations are still necessary.

- Use large PCB copper areas for high current paths, including V_{IN}, GND and V_{OUT}. It helps to minimize the PCB conduction loss and thermal stress.
- Place high frequency ceramic input and output capacitors next to the V_{IN}, GND and V_{OUT} pins to minimize high frequency noise.
- Place a dedicated power ground layer underneath the unit.
- To minimize the via conduction loss and reduce module thermal stress, use multiple vias for interconnection between top layer and other power layers.
- Do not put vias directly on the pad, unless they are capped or plated over.
- Place test points on signal pins for testing.
- Use a separated SGND ground copper area for components connected to signal pins. Connect the SGND to GND underneath the unit.
- For parallel modules, tie the COMP and V_{FB} pins together. Use an internal layer to closely connect these pins together.

Figure 17 gives a good example of the recommended layout. LGA and BGA PCB layouts are identical with the exception of circle pads for BGA (see Package Description).

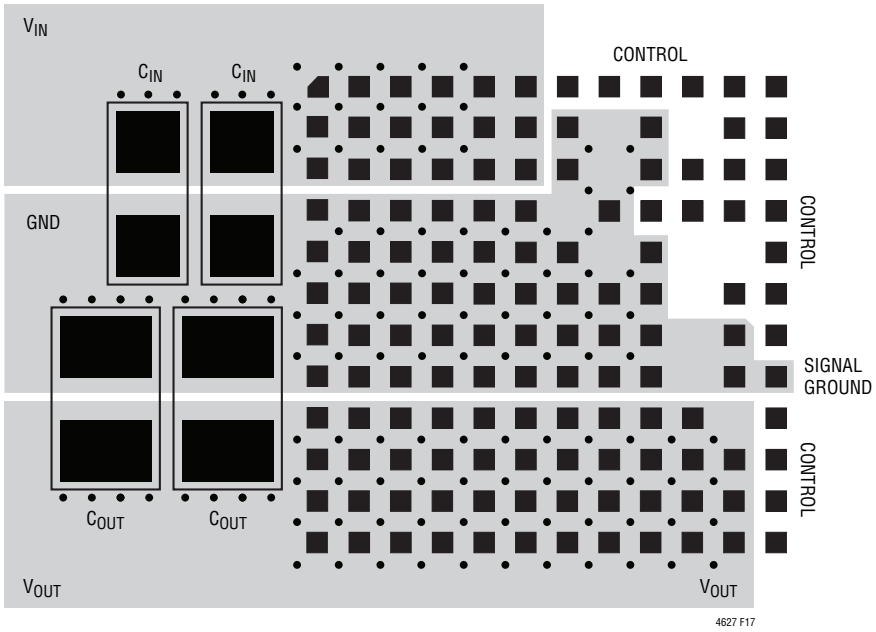


Figure 17. Recommended PCB Layout (LGA Shown, for BGA Use Circle Pads)

TYPICAL APPLICATIONS

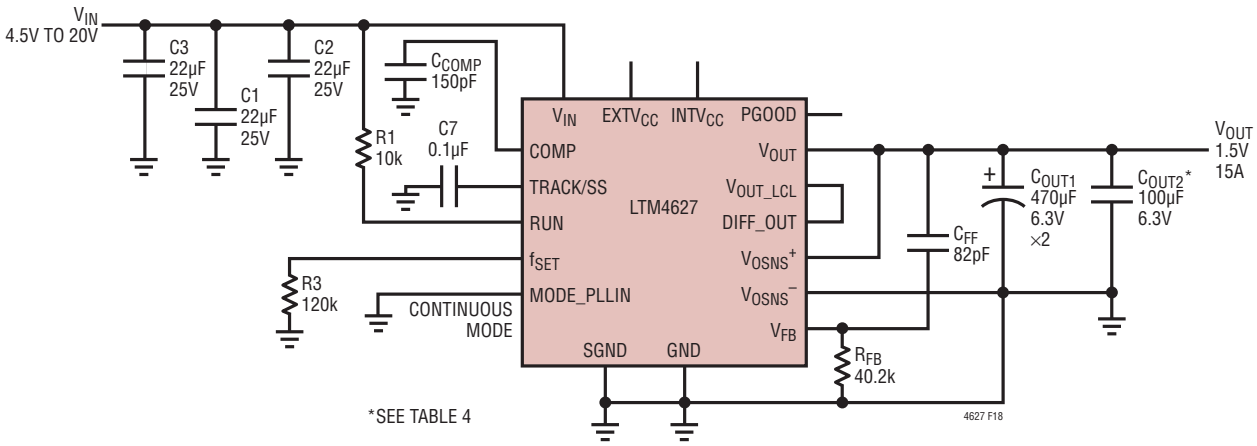


Figure 18. 4.5V to 20V_{IN}, 1.5V at 15A Design

TYPICAL APPLICATIONS

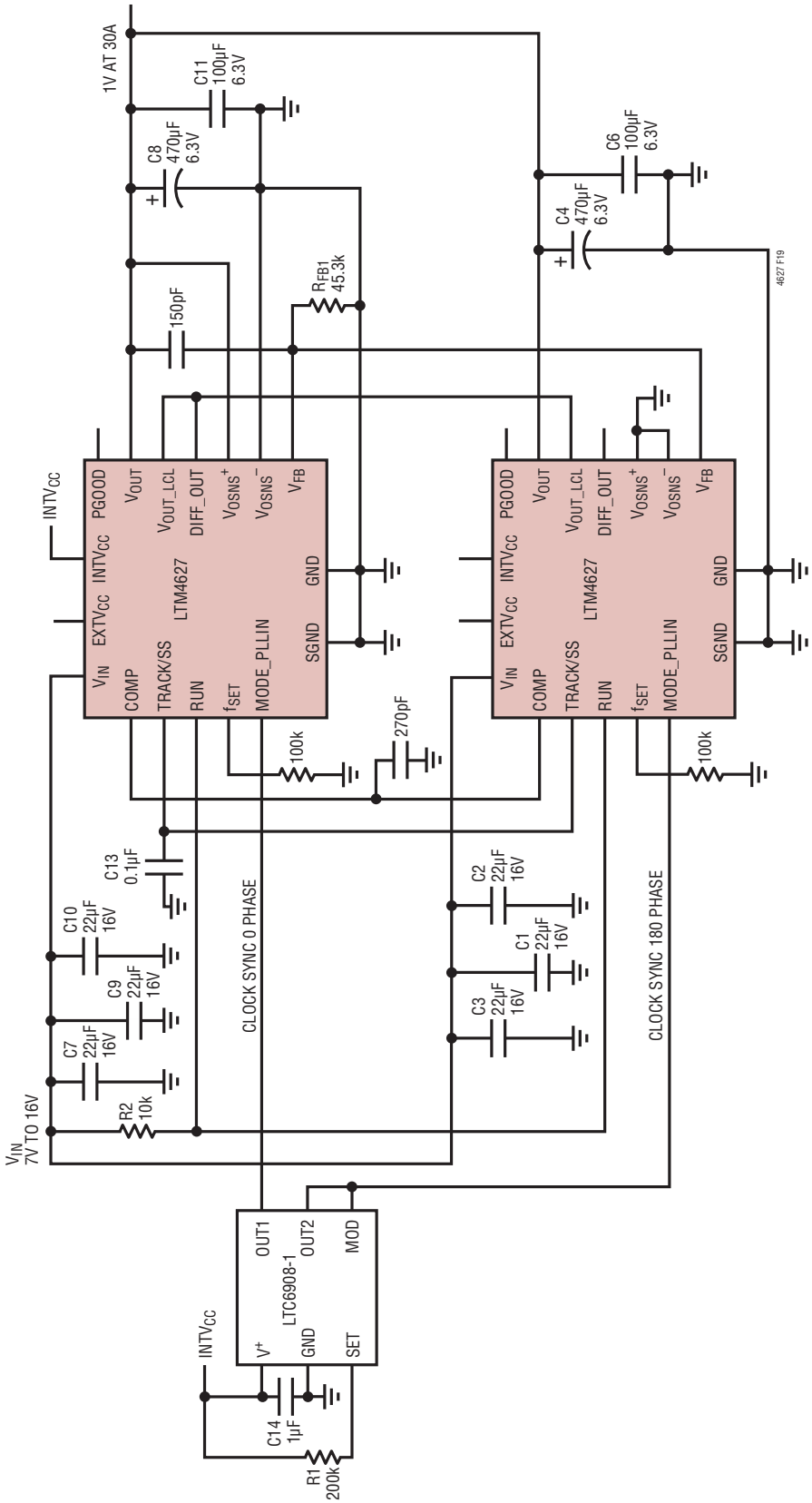


Figure 19. 1V at 30A, Two Parallel Outputs with 2-Phase Operation

TYPICAL APPLICATIONS

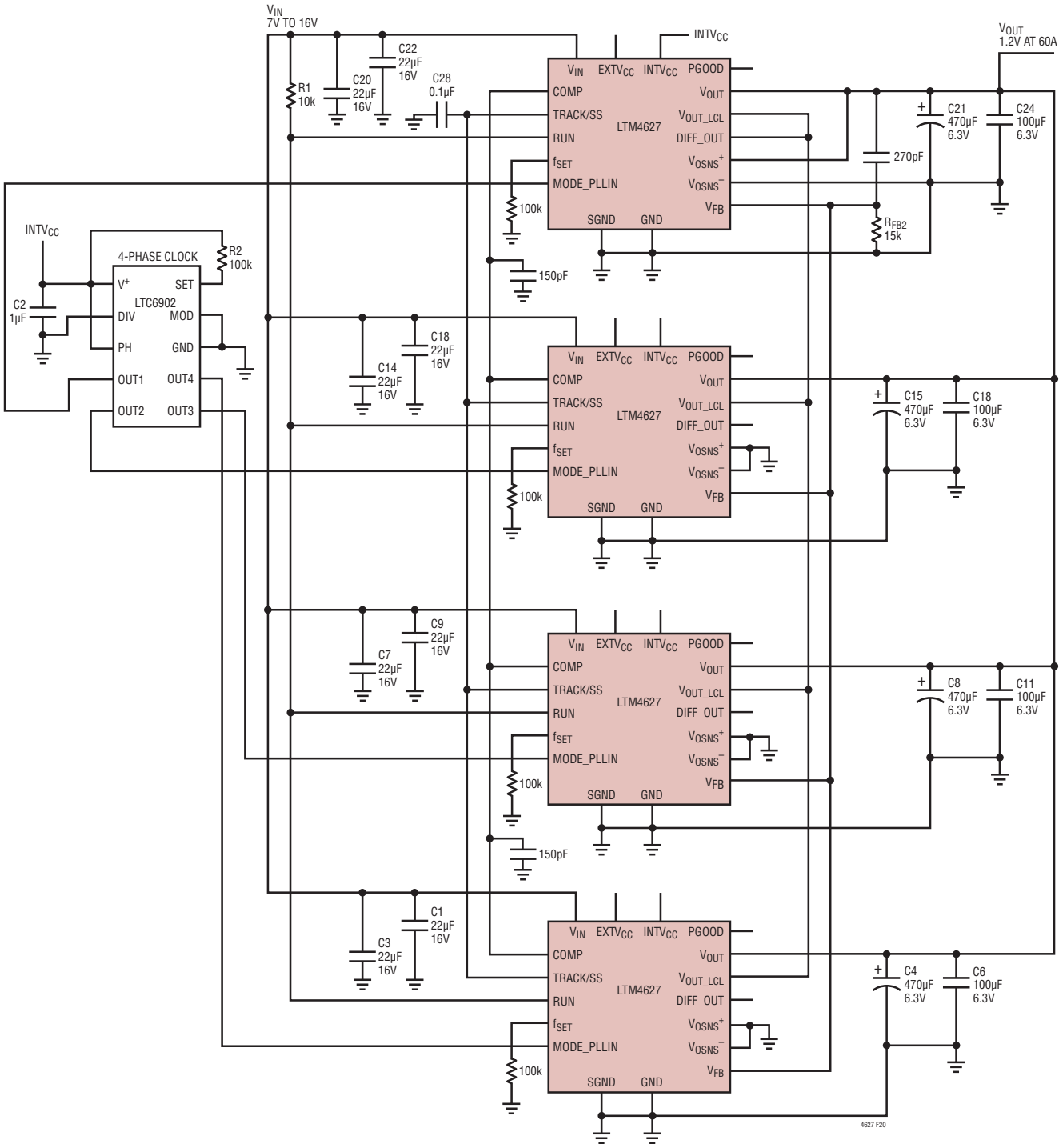


Figure 20. 1.2V, 60A, Current Sharing with 4-Phase Operation

PACKAGE DESCRIPTION

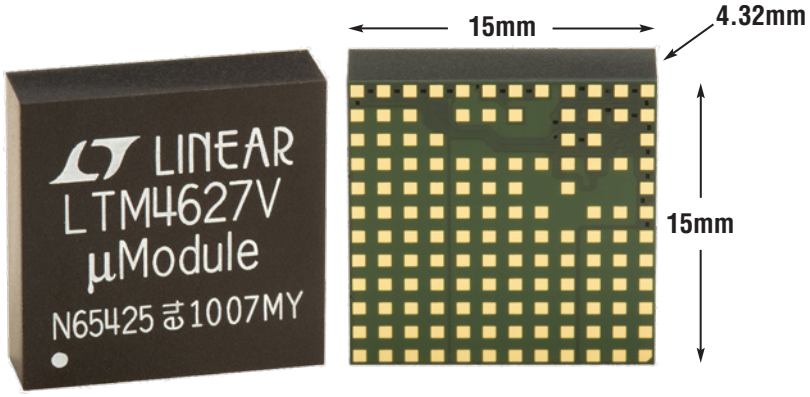
Pin Assignment Table
(Arranged by Pin Number)

PIN NAME	PIN NAME	PIN NAME	PIN NAME	PIN NAME	PIN NAME
A1 V_{IN}	B1 V_{IN}	C1 V_{IN}	D1 GND	E1 GND	F1 GND
A2 V_{IN}	B2 V_{IN}	C2 V_{IN}	D2 GND	E2 GND	F2 GND
A3 V_{IN}	B3 V_{IN}	C3 V_{IN}	D3 GND	E3 GND	F3 GND
A4 V_{IN}	B4 V_{IN}	C4 V_{IN}	D4 GND	E4 GND	F4 GND
A5 V_{IN}	B5 V_{IN}	C5 V_{IN}	D5 GND	E5 GND	F5 GND
A6 V_{IN}	B6 V_{IN}	C6 V_{IN}	D6 GND	E6 GND	F6 GND
A7 $INTV_{CC}$	B7 GND	C7 GND	D7 -	E7 GND	F7 GND
A8 MODE_PLLIN	B8 -	C8 -	D8 GND	E8 -	F8 GND
A9 TRACK/SS	B9 GND	C9 GND	D9 $INTV_{CC}$	E9 GND	F9 GND
A10 RUN	B10 -	C10 MTP3	D10 MTP6	E10 -	F10 -
A11 COMP	B11 MTP2	C11 MTP4	D11 MTP7	E11 -	F11 PGOOD
A12 MTP1	B12 f_{SET}	C12 MTP5	D12 MTP8	E12 $EXTV_{CC}$	F12 V_{FB}

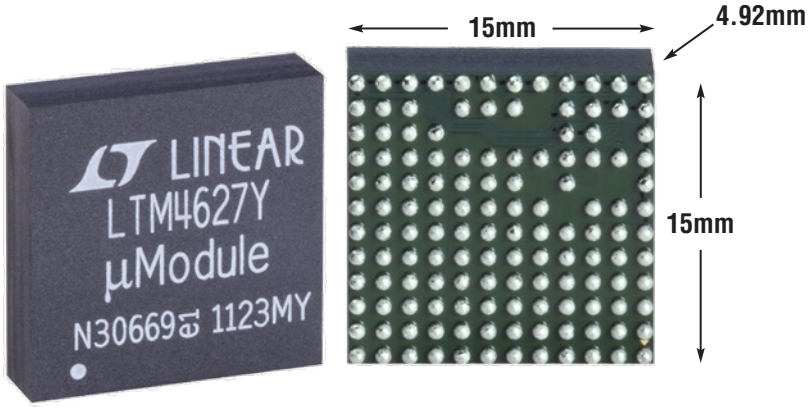
PIN NAME	PIN NAME	PIN NAME	PIN NAME	PIN NAME	PIN NAME
G1 GND	H1 GND	J1 V_{OUT}	K1 V_{OUT}	L1 V_{OUT}	M1 V_{OUT}
G2 GND	H2 GND	J2 V_{OUT}	K2 V_{OUT}	L2 V_{OUT}	M2 V_{OUT}
G3 GND	H3 GND	J3 V_{OUT}	K3 V_{OUT}	L3 V_{OUT}	M3 V_{OUT}
G4 GND	H4 GND	J4 V_{OUT}	K4 V_{OUT}	L4 V_{OUT}	M4 V_{OUT}
G5 GND	H5 GND	J5 V_{OUT}	K5 V_{OUT}	L5 V_{OUT}	M5 V_{OUT}
G6 GND	H6 GND	J6 V_{OUT}	K6 V_{OUT}	L6 V_{OUT}	M6 V_{OUT}
G7 GND	H7 GND	J7 V_{OUT}	K7 V_{OUT}	L7 V_{OUT}	M7 V_{OUT}
G8 GND	H8 GND	J8 V_{OUT}	K8 V_{OUT}	L8 V_{OUT}	M8 V_{OUT}
G9 GND	H9 GND	J9 V_{OUT}	K9 V_{OUT}	L9 V_{OUT}	M9 V_{OUT}
G10 -	H10 -	J10 V_{OUT}	K10 V_{OUT}	L10 V_{OUT}	M10 V_{OUT}
G11 SGND	H11 SGND	J11 -	K11 V_{OUT}	L11 V_{OUT}	M11 V_{OUT}
G12 PGOOD	H12 SGND	J12 V_{OSNS}^{+}	K12 DIFF_OUT	L12 V_{OUT_LCL}	M12 V_{OSNS}^{-}

PACKAGE PHOTOS

LGA



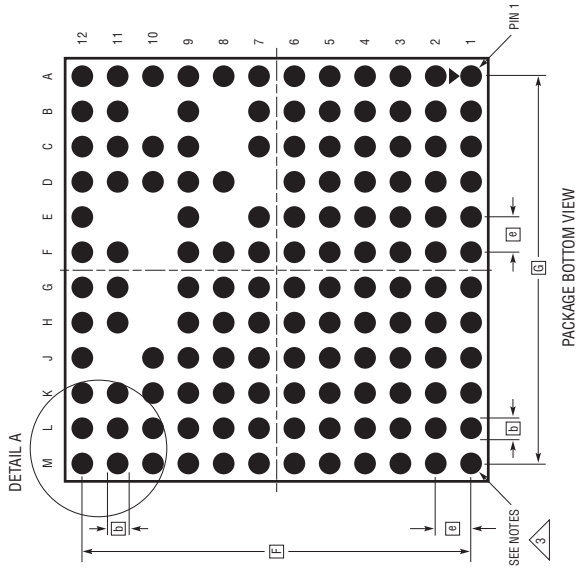
BGA

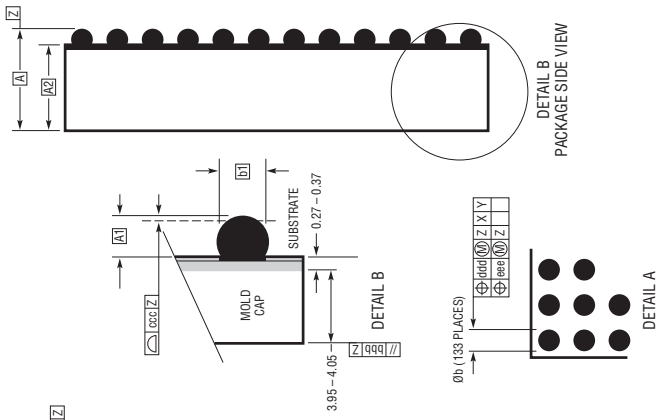


PACKAGE DESCRIPTION

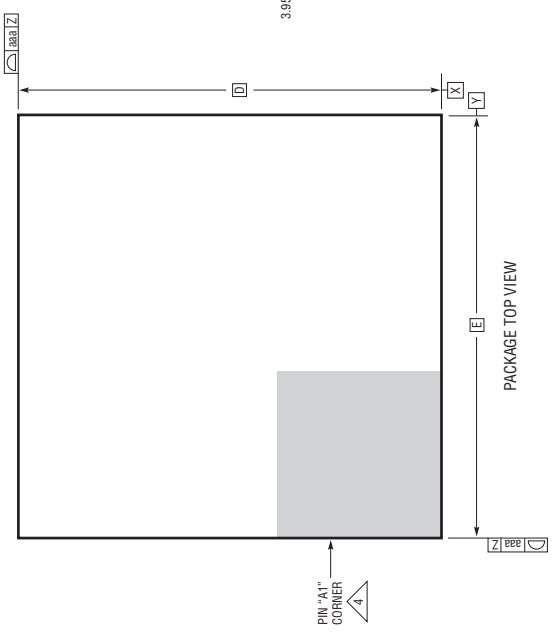
Please refer to http://www.linear.com/designtools/packaging/ for the most recent package drawings.

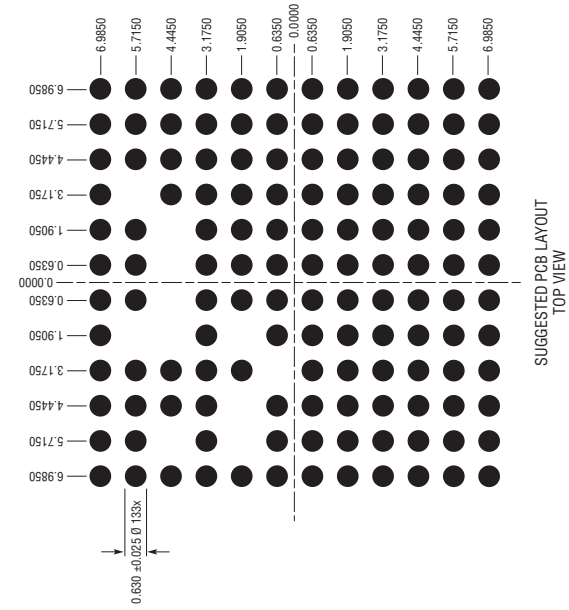
BGA Package
133-Lead (15mm × 15mm × 4.92mm)
(Reference LTC DWG # 05-08-1897 Rev Ø)





DIMENSIONS				
SYMBOL	MIN	NOM	MAX	NOTES
A	4.72	4.92	5.12	
A1	0.50	0.60	0.70	
A2	4.22	4.32	4.42	
b	0.60	0.75	0.90	
b1	0.60	0.63	0.66	
D		15.0		
E		15.0		
e		1.27		
F		13.97		
G		13.97		
aaa			0.15	
bbb			0.10	
ccc			0.20	
ddd			0.30	
eee			0.15	
TOTAL NUMBER OF BALLS: 133				

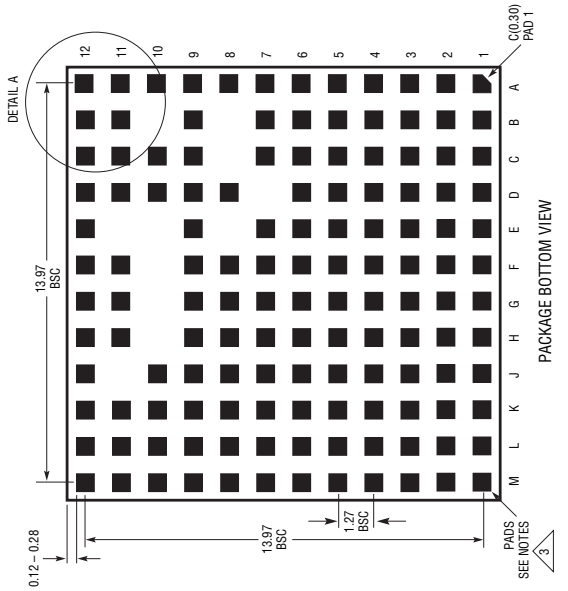


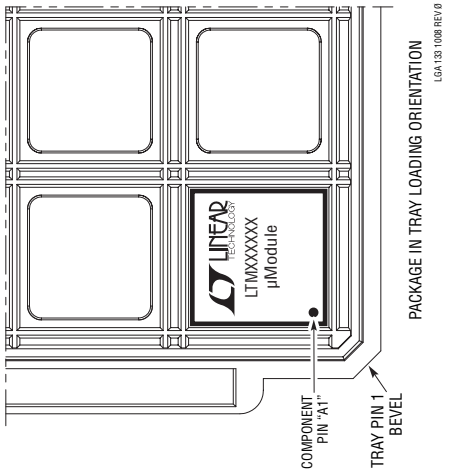


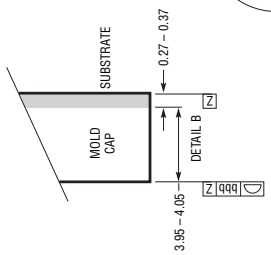
PACKAGE DESCRIPTION

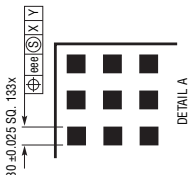
Please refer to http://www.linear.com/designtools/packaging/ for the most recent package drawings.

LGA Package
133-Lead (15mm × 15mm × 4.32mm)
(Reference LTC DWG # 05-08-1777 Rev Ø)



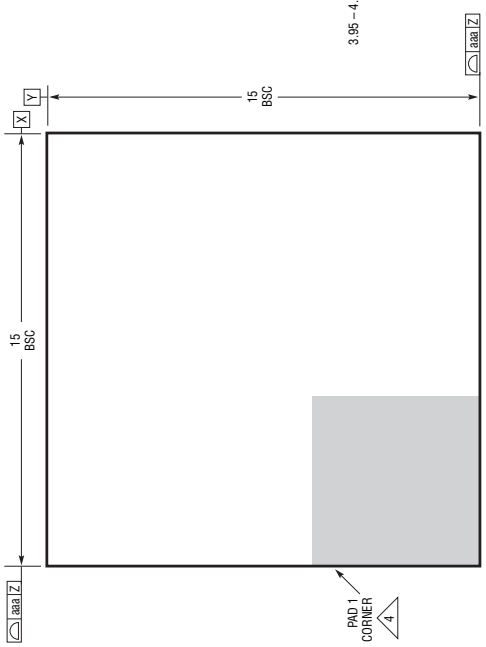


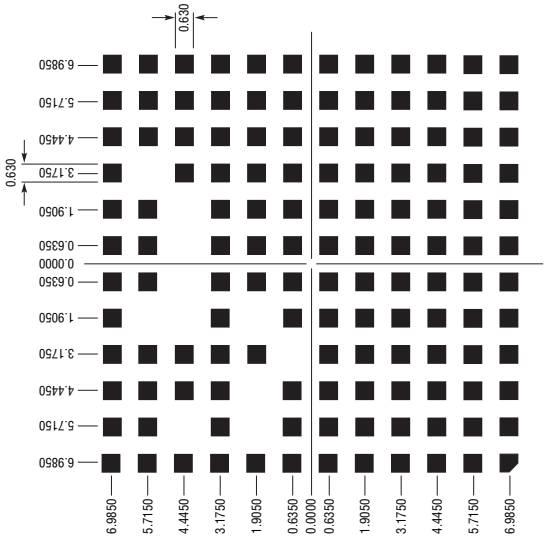




NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M-1994
2. ALL DIMENSIONS ARE IN MILLIMETERS
3. LAND DESIGNATION PER JESD MO-222, SPP-010
4. DETAILS OF PAD #1 IDENTIFIER ARE OPTIONAL, BUT MUST BE LOCATED WITHIN THE ZONE INDICATED. THE PAD #1 IDENTIFIER MAY BE EITHER A MOLD OR MARKED FEATURE
5. PRIMARY DATUM -Z- IS SEATING PLANE
6. THE TOTAL NUMBER OF PADS: 133

SYMBOL	TOLERANCE
aaa	0.15
bbb	0.10
eee	0.05





REVISION HISTORY

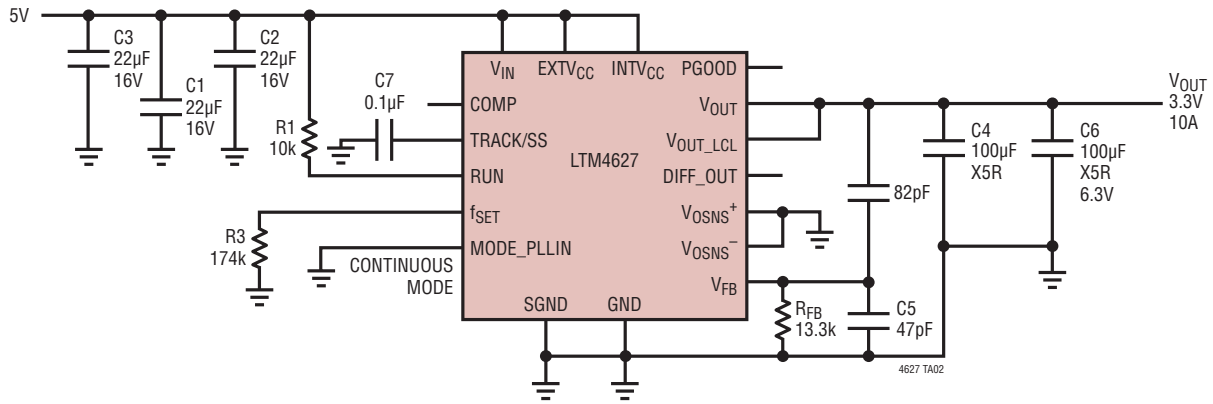
REV	DATE	DESCRIPTION	PAGE NUMBER
A	2/11	Updated the Electrical Characteristics section.	3, 4
		Updated graph G13.	6
		Updated the Inductor value in the Block Diagram and in the Power Module Description section.	9, 10
		Updated the PLL, Frequency Adjustment and Synchronization section.	13
		Updated Figure 3.	14
B	10/11	BGA Package added. Changes reflected throughout the data sheet.	1-32
C	02/14	Add SnPb BGA package option	1, 2

LINEAR TECHNOLOGY

Information furnished by Linear Technology Corporation is believed to be accurate and reliable. However, no responsibility is assumed for its use. Linear Technology Corporation makes no representation that the interconnection of its circuits as described herein will not infringe on existing patent rights.

TYPICAL APPLICATION

3.3V at 10A Design



RELATED PARTS

PART NUMBER	DESCRIPTION	COMMENTS
LTM4628	Dual 8A, 26V, DC/DC Step-Down µModule Regulator	$0.6V \le V_{OUT} \le 5V$, $4.5V \le V_{IN} \le 26.5V$, Remote Sense Amplifier, Internal Temperature Sensing Output, 15mm × 15mm × 4.32mm LGA
LTM4611	$1.5V_{IN(MIN)}$, 15A DC/DC Step-Down µModule Regulator	$0.8V \le V_{OUT} \le 5V$, $1.5V \le V_{IN} \le 5.5V$, PLL Input, Remote Sense Amplifier, V_{OUT} Tracking, 15mm × 15mm × 4.32mm LGA
LTM4618	6A DC/DC Step-Down µModule Regulator	$0.8V \le V_{OUT} \le 5V$, $4.5V \le V_{IN} \le 26.5V$, PLL Input, V_{OUT} Tracking, 9mm × 15mm × 4.32mm LGA
LTM4613	8A EN55022 Class B DC/DC Step-Down µModule Regulator	$3.3V \le V_{OUT} \le 15V$, $5V \le V_{IN} \le 36V$, PLL Input, V_{OUT} Tracking and Margining, 15mm × 15mm × 4.32mm LGA
LTM4601AHV	28V, 12A DC/DC Step-Down µModule Regulator	$0.6V \le V_{OUT} \le 5V$, $4.5V \le V_{IN} \le 28V$, PLL Input, Remote Sense Amplifier, V_{OUT} Tracking and Margining, 15mm × 15mm × 2.82mm LGA or 15mm × 15mm × 3.42mm BGA
LTM4601A	20V, 12A DC/DC Step-Down µModule Regulator	$0.6V \le V_{OUT} \le 5V$, $4.5V \le V_{IN} \le 20V$, PLL Input, Remote Sense Amplifier, V_{OUT} Tracking and Margining, 15mm × 15mm × 2.82mm LGA or 15mm × 15mm × 3.42mm BGA
LTM8027	60V, 4A DC/DC Step-Down µModule Regulator	$4.5V \le V_{OUT} \le 60V$, $2.5V \le V_{IN} \le 24V$, CLK Input, 15mm × 15mm × 4.32mm LGA
LTC6908-1	50kHz to 10MHz Dual Output Oscillator	Single Supply $2.5V \le V_{IN} \le 5.5V$, 90° or 180° Phase Shift Between Outputs, Optional Spread Spectrum Frequency Modulation, 2mm × 3mm DFN

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