THE DATASHEET OF

LTC6655CHLS8-2.5#PBF

www.win-source.net 0086-755-83957316

0.25ppm Noise, Low Drift Precision References

FEATURES

- **Low Noise:**
  - **0.25ppm$_{P-P}$ (0.1Hz to 10Hz) 625nV$_{P-P}$ for the LTC6655-2.5**
  - **0.21ppm$_{RMS}$ (10Hz to 10kHz) for the LTC6655LN-2.5 C_{NR} = 100µF**
- **Low Drift: 2ppm/°C Max**
- **High Accuracy: ±0.025% Max**
- **No Humidity Sensitivity (LS8 Package)**
- **Thermal Hysteresis (LS8): 30ppm (–40°C to 85°C)**
- **Long-Term Drift (LS8): 20ppm/$\sqrt{kHr}$**
- 100% Tested at –40°C, 25°C and 125°C
- Load Regulation: <10ppm/mA
- Sinks and Sources Current: ±5mA
- Low Dropout: 500mV
- Maximum Supply Voltage: 13.2V
- Low Power Shutdown: <20µA Max
- Available Output Voltages: 1.25V, 2.048V, 2.5V, 3V, 3.3V, 4.096V, 5V
- Available in an 8-Lead MSOP and High Stability Hermetic 5mm × 5mm LS8 Packages

APPLICATIONS

- Instrumentation and Test Equipment
- High Resolution Data Acquisition Systems
- Weigh Scales
- Precision Battery Monitors
- Precision Regulators
- Medical Equipment

DESCRIPTION

The LTC®6655 is a complete family of precision bandgap voltage references, offering exceptional noise and drift performance. This low noise and drift is ideally suited for the high resolution measurements required by instrumentation and test equipment. In addition, the LTC6655 is fully specified over the temperature range of –40°C to 125°C, ensuring its suitability for demanding automotive and industrial applications. Advanced curvature compensation allows this bandgap reference to achieve a drift of less than 2ppm/°C with a predictable temperature characteristic and an output voltage accurate to ±0.025%, reducing or eliminating the need for calibration.

The LTC6655LN Low Noise comes with a noise reduction pin that enables reduction of wideband noise with the addition of a single capacitor.

The LTC6655 can be powered from as little as 500mV above the output voltage to as much as 13.2V. Superior load regulation with source and sink capability, coupled with exceptional line rejection, ensures consistent performance over a wide range of operating conditions. A shutdown mode is provided for low power applications.

The LTC6655 references are offered in an 8-lead MSOP package and an 8-lead LS8 package. The LS8 is a 5mm × 5mm surface mount hermetic package that provides outstanding stability.

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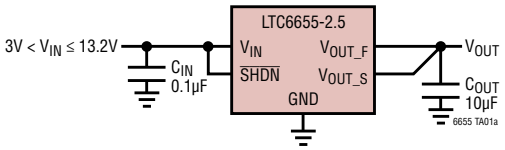
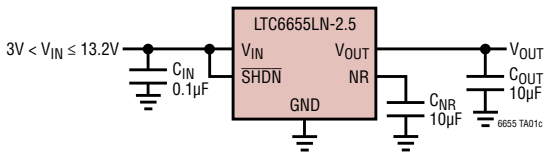
TYPICAL APPLICATION

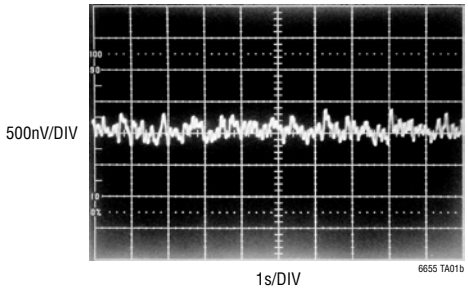
Basic Connection



Basic Connection with Noise Reduction



Low Frequency 0.1Hz to 10Hz Noise (LTC6655-2.5)



ABSOLUTE MAXIMUM RATINGS (Note 1)

Input Voltage
- V_{IN} to GND ..... –0.3V to 13.2V
- $\overline{SHDN}$ to GND ..... –0.3V to (V_{IN} + 0.3V)

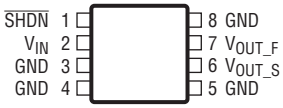
Output Voltage:
- V_{OUT_F} ..... –0.3V to (V_{IN} + 0.3V)
- V_{OUT_S} ..... –0.3V to 6V
- NR ..... –0.3V to 6V
- Output Short-Circuit Duration ..... Indefinite

Operating Temperature Range (Note 2).. –40°C to 125°C
Storage Temperature Range (Note 2)..... –65°C to 150°C
Lead Temperature Range (Soldering, 10 sec)
(Note 3)..... 300°C

PIN CONFIGURATION

LTC6655

TOP VIEW

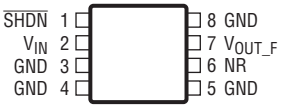


MS8 PACKAGE
8-LEAD PLASTIC MSOP

T_{JMAX} = 150°C, θ_{JA} = 300°C/W
STAR ALL GND CONNECTIONS AT PIN 4

LTC6655LN

TOP VIEW

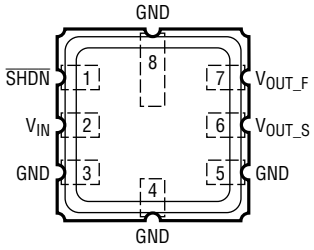


MS8 PACKAGE
8-LEAD PLASTIC MSOP

T_{JMAX} = 150°C, θ_{JA} = 300°C/W
STAR ALL GND CONNECTIONS AT PIN 4

LTC6655

TOP VIEW



LS8 PACKAGE
8-PIN LEADLESS CHIP CARRIER (5mm × 5mm)

T_{JMAX} = 150°C, θ_{JA} = 120°C/W
STAR ALL GND CONNECTIONS AT PIN 4

ORDER INFORMATION

LEAD FREE FINISH	TAPE AND REEL	PART MARKING*	PACKAGE DESCRIPTION	SPECIFIED TEMPERATURE RANGE
LTC6655BHMS8-1.25#PBF	LTC6655BHMS8-1.25#TRPBF	LTFDG	8-Lead Plastic MSOP	–40°C to 125°C
LTC6655CHMS8-1.25#PBF	LTC6655CHMS8-1.25#TRPBF	LTFDG	8-Lead Plastic MSOP	–40°C to 125°C
LTC6655BHMS8-2.048#PBF	LTC6655BHMS8-2.048#TRPBF	LTFDH	8-Lead Plastic MSOP	–40°C to 125°C
LTC6655CHMS8-2.048#PBF	LTC6655CHMS8-2.048#TRPBF	LTFDH	8-Lead Plastic MSOP	–40°C to 125°C
LTC6655BHMS8-2.5#PBF	LTC6655BHMS8-2.5#TRPBF	LTFCY	8-Lead Plastic MSOP	–40°C to 125°C
LTC6655CHMS8-2.5#PBF	LTC6655CHMS8-2.5#TRPBF	LTFCY	8-Lead Plastic MSOP	–40°C to 125°C
LTC6655BHMS8-3#PBF	LTC6655BHMS8-3#TRPBF	LTFDJ	8-Lead Plastic MSOP	–40°C to 125°C
LTC6655CHMS8-3#PBF	LTC6655CHMS8-3#TRPBF	LTFDJ	8-Lead Plastic MSOP	–40°C to 125°C
LTC6655BHMS8-3.3#PBF	LTC6655BHMS8-3.3#TRPBF	LTFDK	8-Lead Plastic MSOP	–40°C to 125°C
LTC6655CHMS8-3.3#PBF	LTC6655CHMS8-3.3#TRPBF	LTFDK	8-Lead Plastic MSOP	–40°C to 125°C
LTC6655BHMS8-4.096#PBF	LTC6655BHMS8-4.096#TRPBF	LTFDM	8-Lead Plastic MSOP	–40°C to 125°C
LTC6655CHMS8-4.096#PBF	LTC6655CHMS8-4.096#TRPBF	LTFDM	8-Lead Plastic MSOP	–40°C to 125°C
LTC6655BHMS8-5#PBF	LTC6655BHMS8-5#TRPBF	LTFDN	8-Lead Plastic MSOP	–40°C to 125°C
LTC6655CHMS8-5#PBF	LTC6655CHMS8-5#TRPBF	LTFDN	8-Lead Plastic MSOP	–40°C to 125°C
LTC6655LNBHMS8-2.5#PBF	LTC6655LNBHMS8-2.5#TRPBF	LTHFK	8-Lead Plastic MSOP	–40°C to 125°C
LTC6655LNCHMS8-2.5#PBF	LTC6655LNCHMS8-2.5#TRPBF	LTHFK	8-Lead Plastic MSOP	–40°C to 125°C
LTC6655BHLS8-2.5 #PBF†	N/A	665525	8-Lead Ceramic LCC (5mm × 5mm)	–40°C to 125°C
LTC6655CHLS8-2.5 #PBF†	N/A	665525	8-Lead Ceramic LCC (5mm × 5mm)	–40°C to 125°C
LTC6655BHLS8-4.096#PBF†	N/A	554096	8-Lead Ceramic LCC (5mm × 5mm)	–40°C to 125°C
LTC6655CHLS8-4.096#PBF†	N/A	554096	8-Lead Ceramic LCC (5mm × 5mm)	–40°C to 125°C
LTC6655BHLS8-5 #PBF†	N/A	66555	8-Lead Ceramic LCC (5mm × 5mm)	–40°C to 125°C
LTC6655CHLS8-5 #PBF†	N/A	66555	8-Lead Ceramic LCC (5mm × 5mm)	–40°C to 125°C

Contact the factory for parts specified with wider operating temperature ranges. *The temperature grade is identified by a label on the shipping container.

†This product is only offered in trays.

Tape and reel specifications. Some packages are available in 500 unit reels through designated sales channels with #TRMPBF suffix.

AVAILABLE OPTIONS

OUTPUT VOLTAGE	INITIAL ACCURACY	TEMPERATURE COEFFICIENT	PART NUMBER†
1.250	0.025% 0.05%	2ppm/°C 5ppm/°C	LTC6655BHMS8-1.25 LTC6655CHMS8-1.25
2.048	0.025% 0.05%	2ppm/°C 5ppm/°C	LTC6655BHMS8-2.048 LTC6655CHMS8-2.048
2.500	0.025% 0.05%	2ppm/°C 5ppm/°C	LTC6655BHMS8-2.5 LTC6655CHMS8-2.5
	0.025% 0.05%	2ppm/°C 5ppm/°C	LTC6655BHLS8-2.5 LTC6655CHLS8-2.5
	0.025% 0.05%	2ppm/°C 5ppm/°C	LTC6655LNBHMS8-2.5 LTC6655LNCHMS8-2.5
3.000	0.025% 0.05%	2ppm/°C 5ppm/°C	LTC6655BHMS8-3.0 LTC6655CHMS8-3.0
3.300	0.025% 0.05%	2ppm/°C 5ppm/°C	LTC6655BHMS8-3.3 LTC6655CHMS8-3.3
4.096	0.025% 0.05%	2ppm/°C 5ppm/°C	LTC6655BHMS8-4.096 LTC6655CHMS8-4.096
	0.025% 0.05%	2ppm/°C 5ppm/°C	LTC6655BHLS8-4.096 LTC6655CHLS8-4.096
5.000	0.025% 0.05%	2ppm/°C 5ppm/°C	LTC6655BHMS8-5 LTC6655CHMS8-5
	0.025% 0.05%	2ppm/°C 5ppm/°C	LTC6655BHLS8-5 LTC6655CHLS8-5

†See Order Information section for complete part number listing.

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. V_{IN} = V_{OUT} + 0.5V, V_{OUT_S} connected to V_{OUT_F}, unless otherwise noted.

PARAMETER	CONDITIONS			MIN	TYP	MAX	UNITS
Output Voltage	LTC6655B LTC6655C			–0.025 –0.05		0.025 0.05	% %
Output Voltage Temperature Coefficient (Note 4)	LTC6655B LTC6655C		● ●		1 2.5	2 5	ppm/°C ppm/°C
Line Regulation	V_{OUT} + 0.5V ≤ V_{IN} ≤ 13.2V, $\overline{SHDN}$ = 2V		 ●		5	25 40	ppm/V ppm/V
Load Regulation (Note 5)	I_{SOURCE} = 5mA	LTC6655MS8	 ●		3	 15	ppm/mA ppm/mA
		LTC6655LS8	 ●		3	 15	ppm/mA ppm/mA
		LTC6655LNMS8	 ●		6	 20	ppm/mA ppm/mA
	I_{SINK} = 5mA	LTC6655MS8	 ●		10	 30	ppm/mA ppm/mA
		LTC6655LS8	 ●		20	 45	ppm/mA ppm/mA
		LTC6655LNMS8	 ●		14	 35	ppm/mA ppm/mA
Operating Voltage (Note 6)	LTC6655-1.25, LTC6655-2.048, LTC6655-2.5 I_{SOURCE} = 5mA, V_{OUT} Error ≤ 0.1%		 ●	 3		 13.2	 V
	LTC6655-3, LTC6655-3.3, LTC6655-4.096, LTC6655-5 I_{SOURCE} = ±5mA, V_{OUT} Error ≤ 0.1% I_{OUT} = 0mA, V_{OUT} Error ≤ 0.1%		 ● ●	 V_{OUT} + 0.5 V_{OUT} + 0.2		 13.2 13.2	 V V
Output Short-Circuit Current	Short V_{OUT} to GND Short V_{OUT} to V_{IN}				20 20		mA mA
Shutdown Pin ($\overline{SHDN}$)	Logic High Input Voltage Logic High Input Current, $\overline{SHDN}$ = 2V		● ●	2.0		 12	V µA
	Logic Low Input Voltage Logic Low Input Current, $\overline{SHDN}$ = 0.8V		● ●			0.8 15	V µA
Supply Current	No Load		 ●		5	7 7.5	mA mA
Shutdown Current	$\overline{SHDN}$ Tied to GND		●			20	µA

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. V_{IN} = V_{OUT} + 0.5V, V_{OUT_S} connected to V_{OUT_F}, unless otherwise noted.

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Output Voltage Noise (Note 7)	LTC6655 0.1Hz ≤ f ≤ 10Hz 10Hz ≤ f ≤ 1kHz			 0.25 0.67		 ppm_{P-P} ppm_{RMS}
	LTC6655LN 0.1Hz ≤ f ≤ 10Hz, C_{NR} = 100µF 10Hz ≤ f ≤ 1kHz, C_{NR} = 100µF			 0.12 0.21		 ppm_{P-P} ppm_{RMS}
Turn-On Time	0.1% Settling, C_{OUT} = 2.7µF			400		µs
Long-Term Drift of Output Voltage (Note 8)	LTC6655MS8 LTC6655LS8			60 20		$ppm/\sqrt{kHr}$ $ppm/\sqrt{kHr}$
Hysteresis (Note 9)	LTC6655MS8 ΔT = 0°C to 70°C ΔT = –40°C to 85°C ΔT = –40°C to 125°C			 20 30 60		 ppm ppm ppm
	LTC6655LS8 ΔT = 0°C to 70°C ΔT = –40°C to 85°C ΔT = –40°C to 125°C			 5 30 80		 ppm ppm ppm

Note 1: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

Note 2: Precision may be affected if the parts are stored outside of the specified temperature range. Large temperature changes may cause changes in device performance due to thermal hysteresis. For best performance, extreme temperatures should be avoided whenever possible.

Note 3: The stated temperature is typical for soldering of the leads during manual rework. For detailed IR reflow recommendations, refer to the Applications Information section.

Note 4: Temperature coefficient is measured by dividing the maximum change in output voltage by the specified temperature range.

Note 5: Load regulation is measured on a pulse basis from no load to the specified load current. Load current does not include the 2mA sense current. Output changes due to die temperature change must be taken into account separately.

Note 6: Excludes load regulation errors. Minimum supply for the LTC6655-1.25, LTC6655-2.048 and LTC6655-2.5 is set by internal circuitry supply requirements, regardless of load condition. Minimum supply for the LTC6655-3, LTC6655-3.3, LTC6655-4.096 and LTC6655-5 is specified by load current.

Note 7: Peak-to-peak noise is measured with a 2-pole highpass filter at 0.1Hz and 3-pole lowpass filter at 10Hz. The unit is enclosed in a still-air environment to eliminate thermocouple effects on the leads, and the test time is 10 seconds. Due to the statistical nature of noise, repeating noise measurements will yield larger and smaller peak values in a given measurement interval. By repeating the measurement for 1000 intervals, each 10 seconds long, it is shown that there are time intervals during which the noise is higher than in a typical single interval, as predicted by statistical theory. In general, typical values are considered to be those for which at least 50% of the units may be expected to perform similarly or better. For the 1000 interval test, a typical unit will exhibit noise that is less than the typical value listed in the Electrical Characteristics table in more than 50% of its measurement intervals. See Application Note 124 for noise testing details. RMS noise is measured with a spectrum analyzer in a shielded environment.

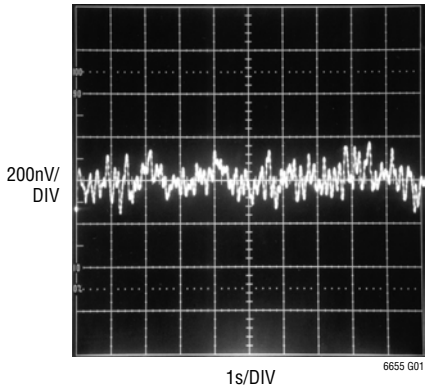
Note 8: Long-term stability typically has a logarithmic characteristic and therefore, changes after 1000 hours tend to be much smaller than before that time. Total drift in the second thousand hours is normally less than one-third that of the first thousand hours with a continuing trend toward reduced drift with time. Long-term stability is also affected by differential stresses between the IC and the board material created during board assembly.

Note 9: Hysteresis in output voltage is created by mechanical stress that differs depending on whether the IC was previously at a higher or lower temperature. Output voltage is always measured at 25°C, but the IC is cycled to the hot or cold temperature limit before successive measurements. Hysteresis is roughly proportional to the square of the temperature change. For instruments that are stored at well controlled temperatures (within 20 or 30 degrees of operational temperature), hysteresis is usually not a significant error source. Typical hysteresis is the worst case of 25°C to cold to 25°C or 25°C to hot to 25°C, preconditioned by one thermal cycle.

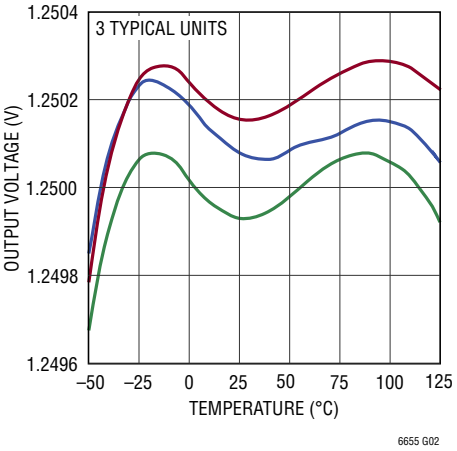
TYPICAL PERFORMANCE CHARACTERISTICS

Characteristic curves are similar for most voltage options of the LTC6655. Curves from the LTC6655-1.25, LTC6655-2.5 and the LTC6655-5 represent the range of performance across the entire family of references. Characteristic curves for other output voltages fall between these curves and can be estimated based on their voltage output.

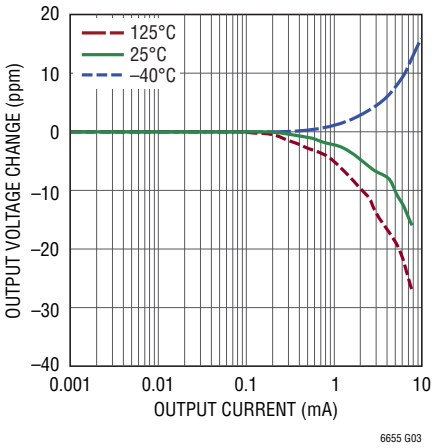
1.25V Low Frequency 0.1Hz to 10Hz Noise



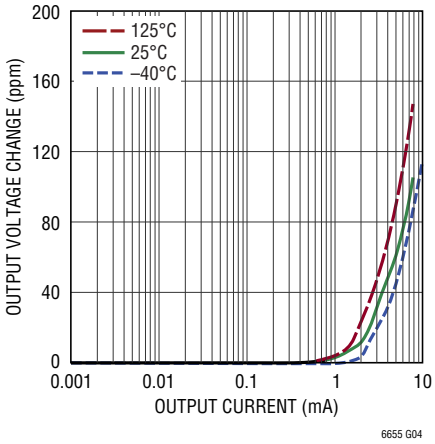
1.25V Output Voltage Temperature Drift



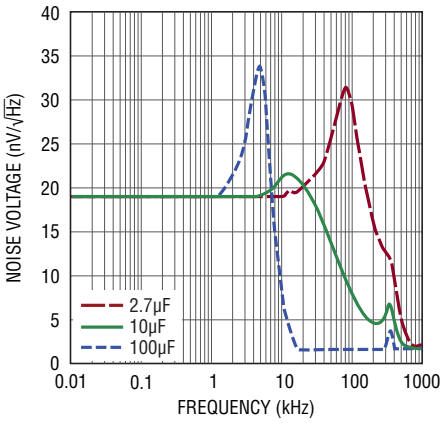
1.25V Load Regulation (Sourcing)



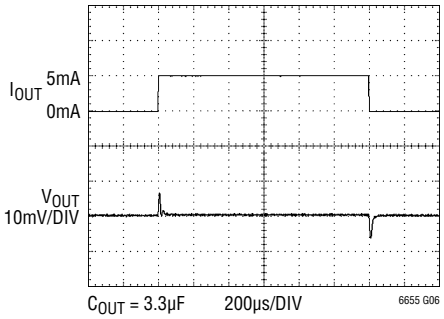
1.25V Load Regulation (Sinking)



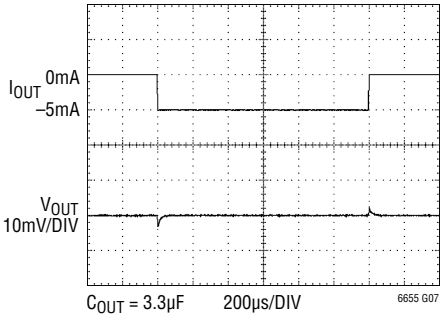
1.25V Output Voltage Noise Spectrum



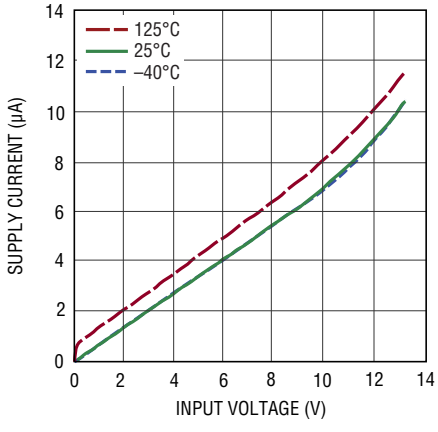
1.25V Sinking Current with a 3.3µF Output Capacitor



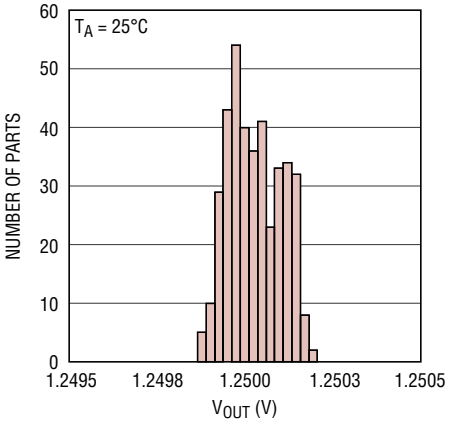
1.25V Sourcing Current with a 3.3µF Output Capacitor



1.25V Shutdown Supply Current vs Input Voltage



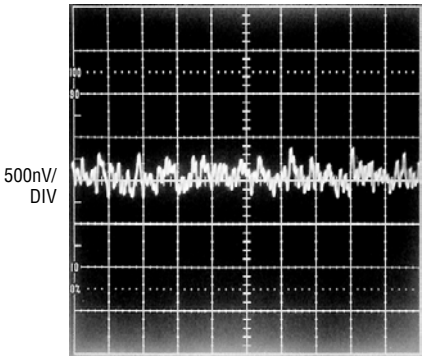
1.25V V_{OUT} Distribution



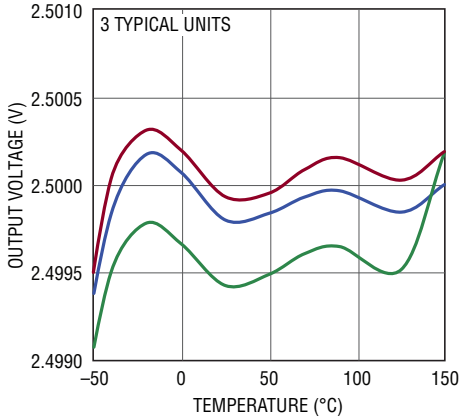
TYPICAL PERFORMANCE CHARACTERISTICS

Characteristic curves are similar for most voltage options of the LTC6655. Curves from the LTC6655-1.25, LTC6655-2.5 and the LTC6655-5 represent the range of performance across the entire family of references. Characteristic curves for other output voltages fall between these curves and can be estimated based on their voltage output.

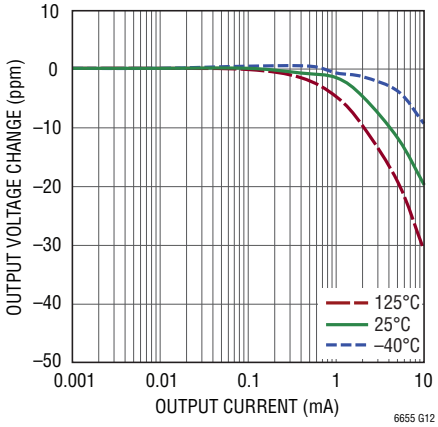
2.5V Low Frequency 0.1Hz to 10Hz Noise



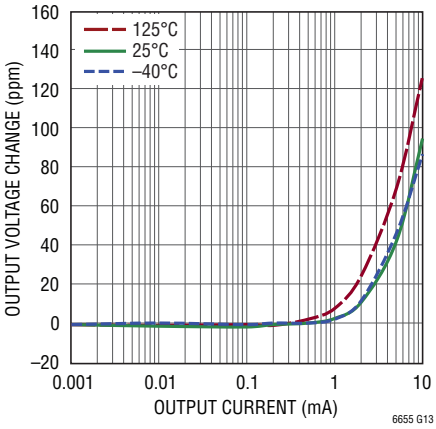
2.5V Output Voltage Temperature Drift



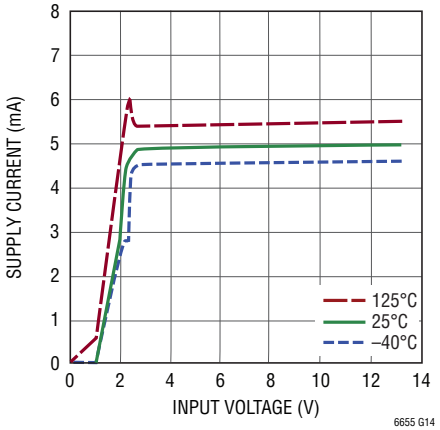
2.5V Load Regulation (Sourcing)



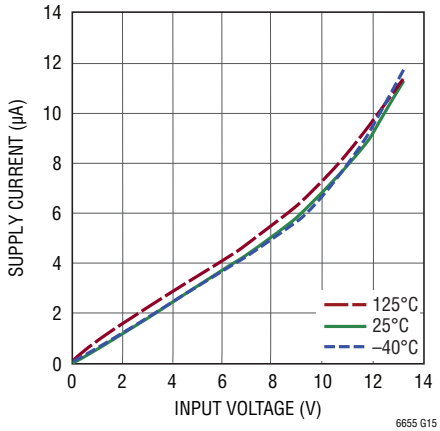
2.5V Load Regulation (Sinking)



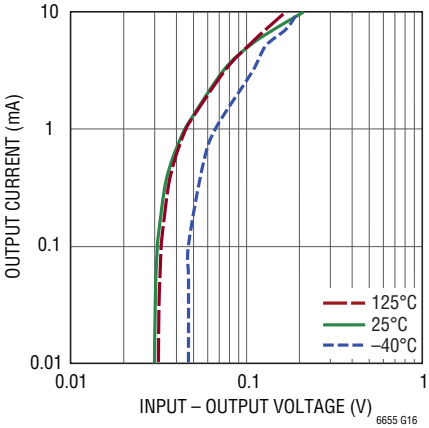
2.5V Supply Current vs Input Voltage



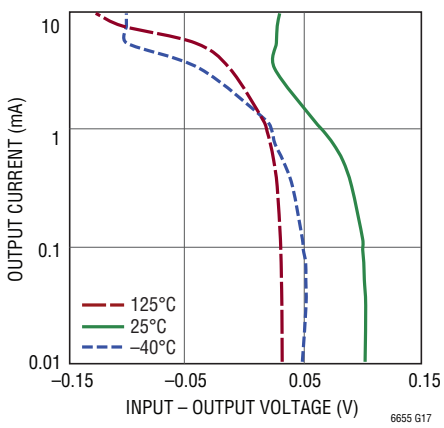
2.5V Shutdown Supply Current vs Input Voltage



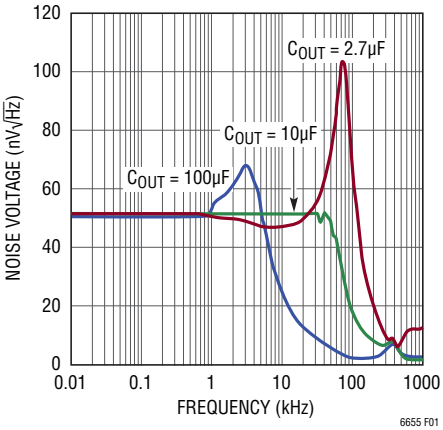
2.5V Minimum $V_{IN} – V_{OUT}$ Differential (Sourcing)



2.5V Minimum $V_{IN} – V_{OUT}$ Differential (Sinking)



2.5V Output Voltage Noise Spectrum



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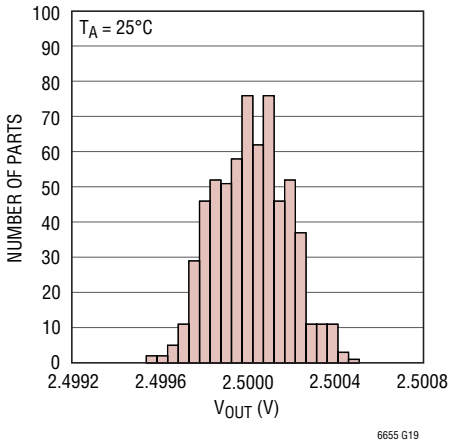
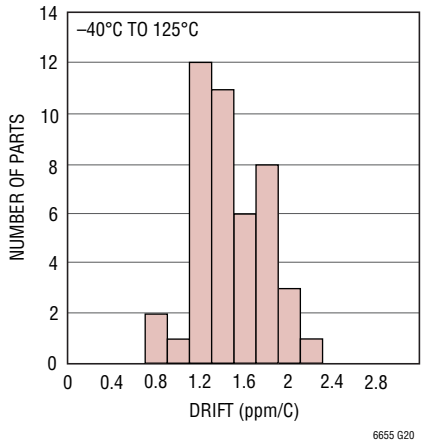
TYPICAL PERFORMANCE CHARACTERISTICS

Characteristic curves are similar for most voltage options of the LTC6655. Curves from the LTC6655-1.25, LTC6655-2.5 and the LTC6655-5 represent the range of performance across the entire family of references. Characteristic curves for other output voltages fall between these curves and can be estimated based on their voltage output.

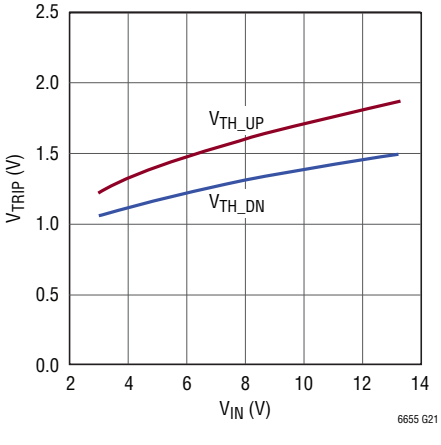
2.5V V_{OUT} Distribution



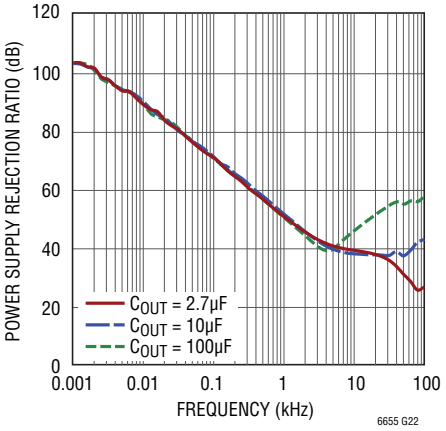
2.5V Temperature Drift Distribution



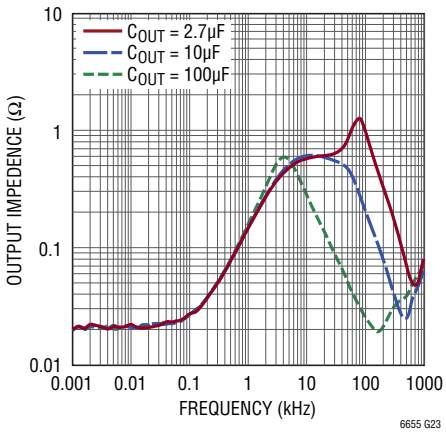
2.5V $\overline{SHDN}$ Input Voltage Thresholds vs V_{IN}



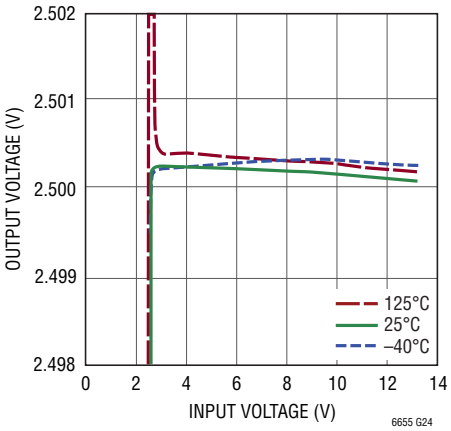
2.5V Power Supply Rejection Ratio vs Frequency



2.5V Output Impedance vs Frequency



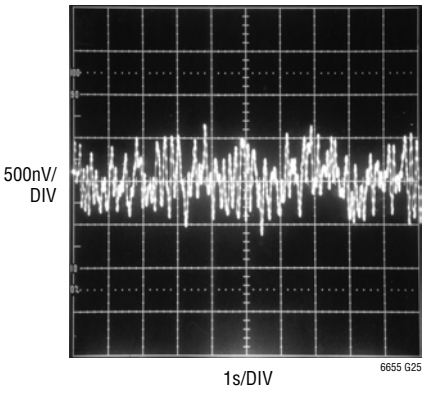
2.5V Line Regulation



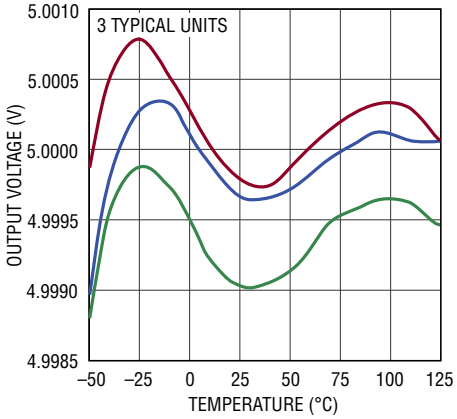
TYPICAL PERFORMANCE CHARACTERISTICS

Characteristic curves are similar for most voltage options of the LTC6655. Curves from the LTC6655-1.25, LTC6655-2.5 and the LTC6655-5 represent the range of performance across the entire family of references. Characteristic curves for other output voltages fall between these curves and can be estimated based on their voltage output.

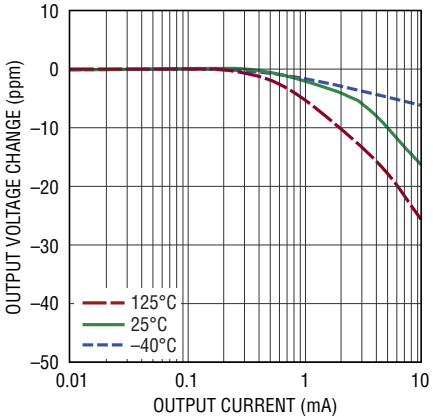
5V Low Frequency 0.1Hz to 10Hz Noise



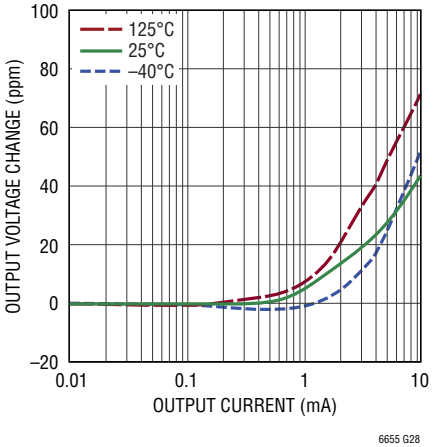
5V Output Voltage Temperature Drift



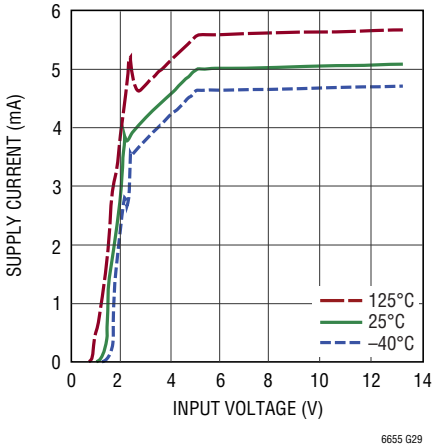
5V Load Regulation (Sourcing)



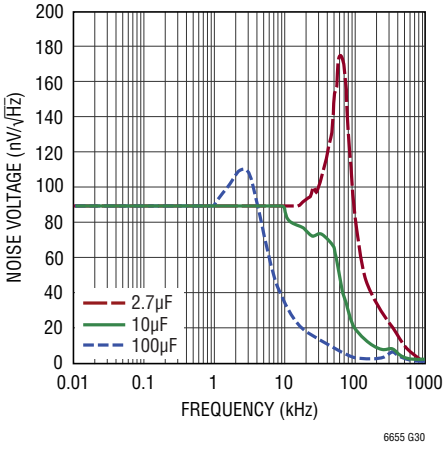
5V Load Regulation (Sinking)



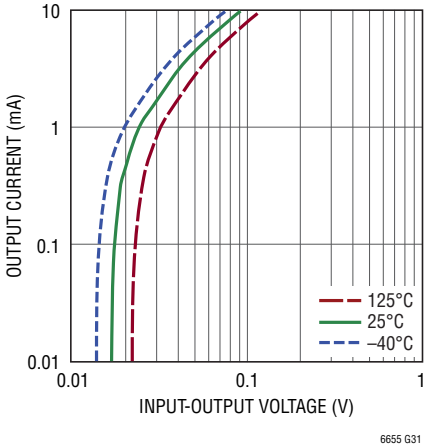
5V Supply Current vs Input Voltage



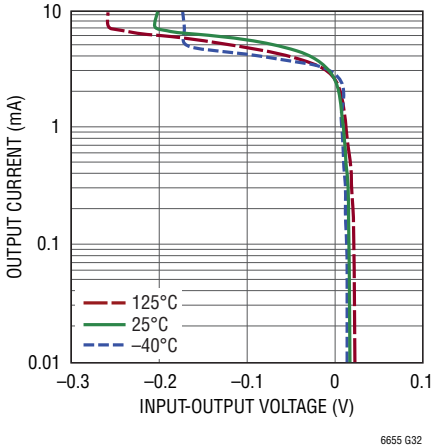
5V Output Voltage Noise Spectrum



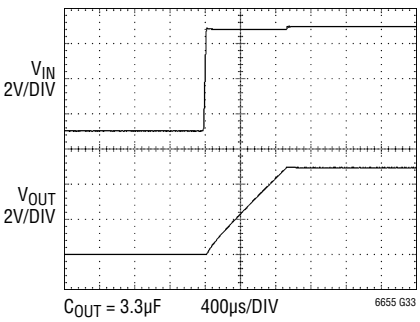
5V Minimum V_{IN}-V_{OUT} Differential (Sourcing)



5V Minimum V_{IN}-V_{OUT} Differential (Sinking)



5V Start-Up Response with a 3.3µF Output Capacitor

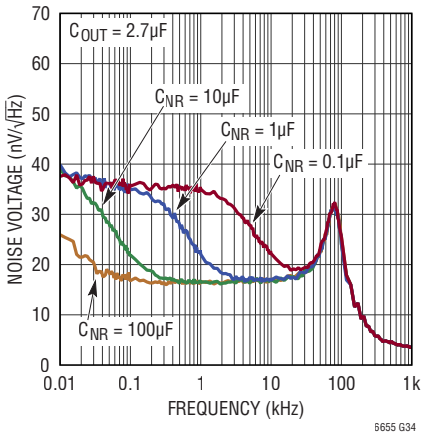


Rev. G

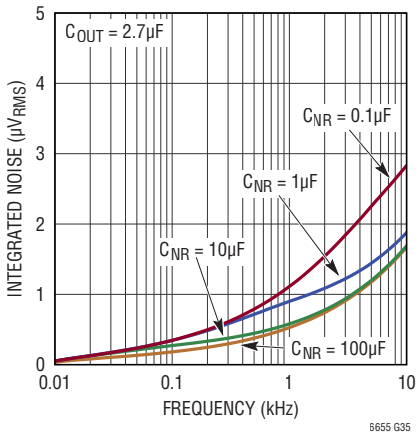
TYPICAL PERFORMANCE CHARACTERISTICS

Characteristic curves shown below are the LTC6655NL option.

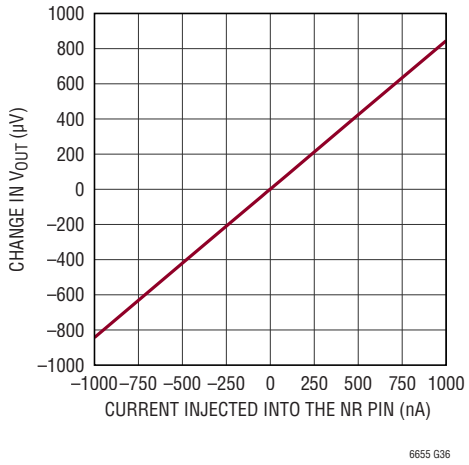
LTC6655LN-2.5 Output Voltage Noise Spectrum



LTC6655LN-2.5 Output Integrated Noise



LTC6655LN-2.5 Effect of NR Pin Leakage on V_{OUT}



PIN FUNCTIONS

$\overline{SHDN}$ (Pin 1): Shutdown Input. This active low input powers down the device to <20µA. If left open, an internal pull-up resistor puts the part in normal operation. It is recommended to tie this pin high externally for best performance during normal operation.

V_{IN} (Pin 2): Power Supply. Bypass V_{IN} with a 0.1µF, or larger, capacitor to GND.

GND (Pin 4): Device Ground. This pin is the main ground and must be connected to a noise-free ground plane.

V_{OUT_S} (Pin 6 – LTC6655): V_{OUT} Sense Pin. Connect this pin at the load and route with a wide metal trace to minimize load regulation errors. This pin sinks 2mA. Output error is R_{TRACE} • 2mA, regardless of load current. For load currents <100µA, tie directly to V_{OUT_F} pin.

NR (Pin 6 – LTC6655LN): Noise Reduction Pin. To band limit noise, connect a capacitor between this pin and ground. See Applications Information section.

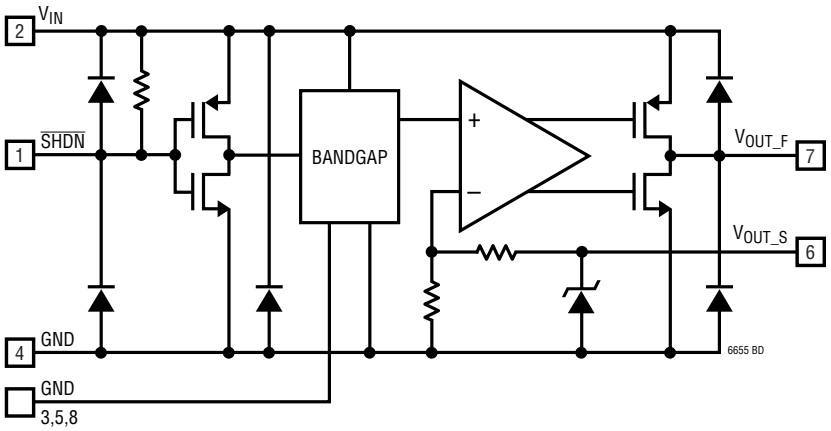
V_{OUT_F} (Pin 7 – LTC6655): V_{OUT} Force Pin. This pin sources and sinks current to the load. An output capacitor of 2.7µF to 100µF is required.

V_{OUT_F} (Pin 7 – LTC6655LN): V_{OUT} Pin. This pin sources and sinks current to the load. An output capacitor of 2.7µF to 100µF is required.

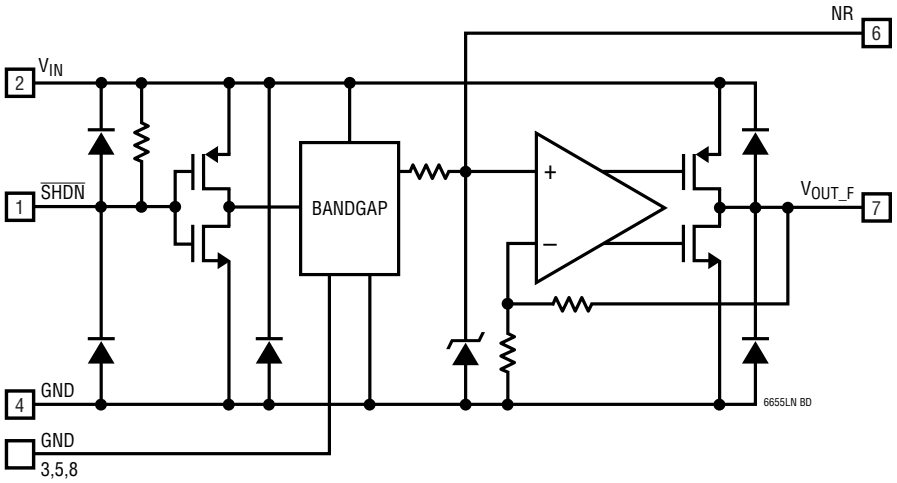
GND (Pins 3, 5, 8): Internal Function. Ground these pins.

BLOCK DIAGRAM

LTC6655



LTC6655LN



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APPLICATIONS INFORMATION

Bypass and Load Capacitors

The LTC6655 voltage references require a 0.1µF or larger input capacitor located close to the part to improve power supply rejection. An output capacitor with a value between 2.7µF and 100µF is also required.

The output capacitor has a direct effect on the stability, turn-on time and settling behavior. Choose a capacitor with low ESR to insure stability. Resistance in series with the output capacitor (ESR) introduces a zero in the output buffer transfer function and could cause instability. The 2.7µF to 100µF range includes several types of capacitors that are readily available as through-hole and surface mount components. It is recommended to keep ESR less than or equal to 0.1Ω. Capacitance and ESR are both frequency dependent. At higher frequencies capacitance drops and ESR increases. To insure stable operation the output capacitor should have the required values at 100kHz.

In order to achieve the best performance, caution should be used when choosing a capacitor. X7R ceramic capacitors are small, come in appropriate values and are relatively stable over a wide temperature range. However, for a low noise application X7R capacitors may not be suitable since they may exhibit a piezoelectric effect. The mechanical vibrations cause a charge displacement in the ceramic dielectric and the resulting perturbation can look like noise. If X7R capacitors are necessary, a thorough bench evaluation should be completed to verify proper performance.

For very low noise applications where every nanovolt counts, film capacitors should be considered for their low noise and lack of piezoelectric effects. Film capacitors such as polyester, polystyrene, polycarbonate, and polypropylene have good temperature stability. Additional care must be taken as polystyrene and polypropylene have an upper temperature limit of 85°C to 105°C. Above these temperatures, the working voltages need to be derated according to manufacturer's specifications. Another type of film capacitor is polyphenylene sulfide (PPS). These devices work over a wide temperature range, are stable, and have large capacitance values beyond 1µF. In general, film capacitors are found in surface mount and leaded packages. Table 1 is a partial list of capacitor companies and some of their available products.

In voltage reference applications, film capacitor lifetime is affected by temperature and applied voltage. When polyester capacitors are operated beyond their rated temperatures (some capacitors are not rated for operation above 85°C) they need to be derated. Voltage derating is usually accomplished as a ratio of applied voltage to rated voltage limit. Contact specific film capacitor manufacturers to determine exact lifetime and derating information.

The lifetime of X7R capacitors is long, especially for reference applications. Capacitor lifetime is degraded by operating near or exceeding the rated voltage, at high temperature, with AC ripple or some combination of these. Most reference applications have AC ripple only during transient events.

Table 1. Film Capacitor Companies

COMPANY	DIELECTRIC	AVAILABLE CAPACITANCE	TEMPERATURE RANGE	TYPE
Cornell Dublier	Polyester	0.5µF to 10µF	–55°C to 125°C	DME
Dearborn Electronics	Polyester	0.1µF to 12µF	–55°C to 125°C	218P, 430P, 431P, 442P, and 410P
Tecate	Polyester	0.01µF to 18µF	–40°C to 105°C	901, 914, and 914D
Wima	Polyester	10µF to 22µF	–55°C to 100°C	MKS 4, MKS 2-XL
Vishay	Polyester	1000pF to 15µF	–55°C to 125°C	MKT1820
Vishay	Polycarbonate	0.01µF to 10µF	–55°C to 100°C	MKC1862, 632P
Dearborn Electronics	Polyphenylene Sulfide (PPS)	0.01µF to 15µF	–55°C to 125°C	820P, 832P, 842P, 860P, and 880P
Wima	Polyphenylene Sulfide (PPS)	0.01µF to 6.8µF	–55°C to 140°C	SMD-PPS

APPLICATIONS INFORMATION

The choice of output capacitor also affects the bandwidth of the reference circuitry and resultant noise peaking. As shown in Figure 1, the bandwidth is inversely proportional to the value of the output capacitor.

Noise peaking is related to the phase margin of the output buffer. Higher peaking generally indicates lower phase margin. Other factors affecting noise peaking are temperature, input voltage, and output load current.

Start-Up and Load Transient Response

Results for the transient response plots (Figures 3 to 8) were produced with the test circuit shown in Figure 2 unless otherwise indicated.

The turn-on time is slew limited and determined by the short-circuit current, the output capacitor, and output voltage as shown in the equation:

$$t_{ON} = V_{OUT} \bullet \frac{C_{OUT}}{I_{SC}}$$

For example, the LTC6655-2.5V, with a 3.3µF output capacitor and a typical short-circuit current of 20mA, the start-up time would be approximately:

$$2.5V \bullet \frac{3.3 \bullet 10^{-6}F}{0.02A} = 412\mu s$$

The resulting turn-on time is shown in Figure 3. Here the output capacitor is 3.3µF and the input capacitor is 0.1µF.

Figure 4 shows the output response to a 500mV step on V_{IN}. The output response to a current step sourcing and sinking is shown in Figures 5 and 6, respectively.

Figure 7 shows the output response as the current goes from sourcing to sinking.

Shutdown Mode

The LTC6655 family of references can be shut down by tying the $\overline{SHDN}$ pin to ground. There is an internal pull-up resistor tied to this pin. If left unconnected this pin rises to V_{IN} and the part is enabled. Due to the low internal pull-up current, it is recommended that the $\overline{SHDN}$ pin be pulled high externally for normal operation to prevent accidental

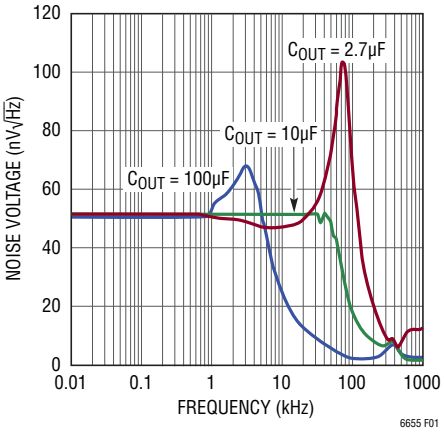

Figure 1. Output Voltage Noise Spectrum

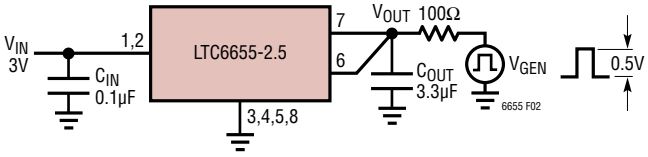

Figure 2. Transient Load Test Circuit

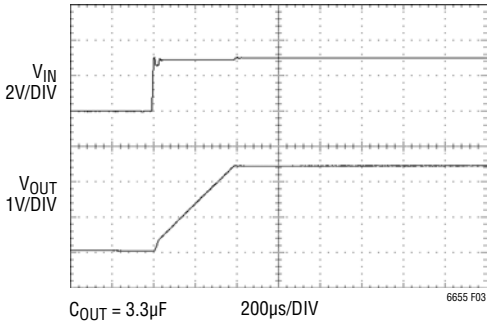

Figure 3. Start-Up Response

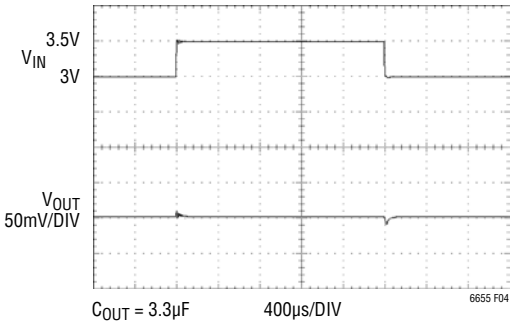

Figure 4. Output Response with a 500mV Step On V_{IN}

APPLICATIONS INFORMATION

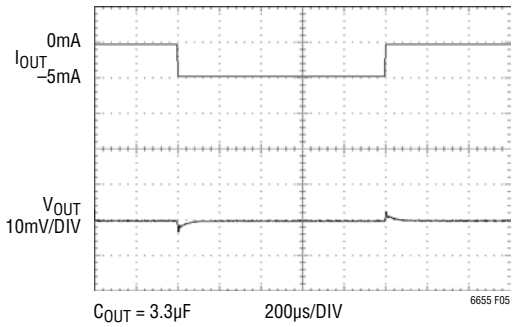

Figure 5. Output Response with a 5mA Load Step Sourcing

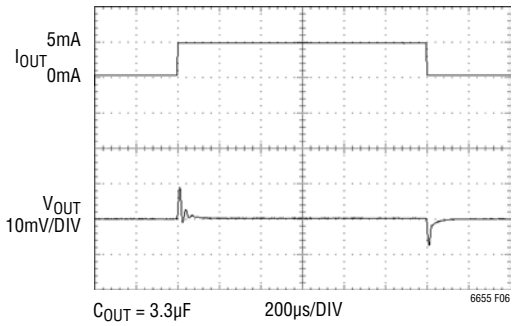

Figure 6. Output Response with 5mA Load Step Sinking

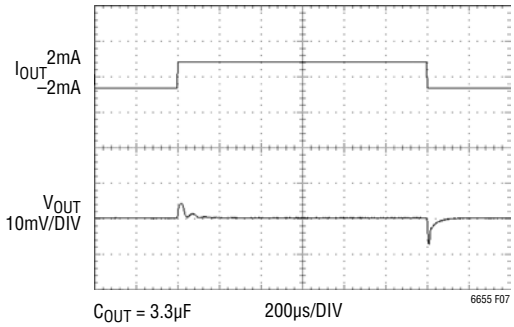

Figure 7. Output Response Showing a Sinking to Sourcing Transition

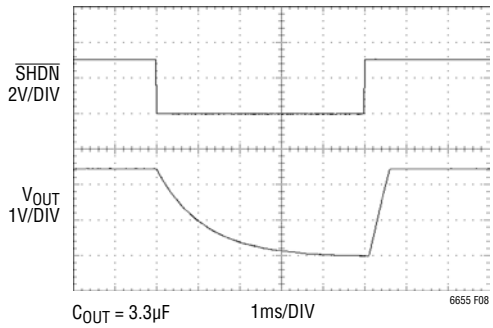

Figure 8. Shutdown Response with 5mA Source Load

shutdown due to system noise or leakage currents. The turn-on/turn-off response due to shutdown is shown in Figure 8.

To control shutdown from a low voltage source, a MOSFET can be used as a pull-down device as shown in Figure 9. Note that an external resistor is unnecessary. A MOSFET with a low drain-to-source leakage over the operating temperature range should be chosen to avoid inadvertently pulling down the $\overline{SHDN}$ pin. A resistor may be added from $\overline{SHDN}$ to V_{IN} to overcome excessive MOSFET leakage.

The $\overline{SHDN}$ thresholds have some dependency on V_{IN} and temperature as shown in the Typical Performance Characteristics section. Avoid leaving $\overline{SHDN}$ at a voltage between the thresholds as this will cause an increase in supply current due to shoot-through current.

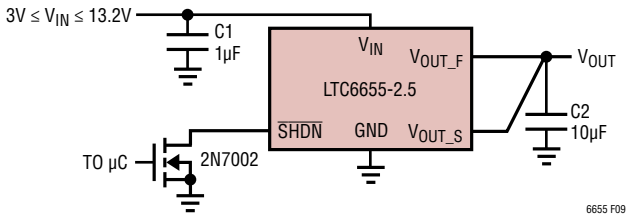

Figure 9. Open-Drain Shutdown Circuit

Long-Term Drift

Long-term drift cannot be extrapolated from accelerated high temperature testing. This erroneous technique gives drift numbers that are wildly optimistic. The only way long-term drift can be determined is to measure it over the time interval of interest.

The LTC6655 long-term drift data was collected on 80 parts that were soldered into printed circuit boards similar to a *real world* application. The boards were then placed into a constant temperature oven with a T_A = 35°C, their outputs were scanned regularly and measured with an 8.5 digit DVM. Typical long-term drift is illustrated in Figure 10a. The hermetic LS8 package provides additional stability as shown in Figure 10b.

APPLICATIONS INFORMATION

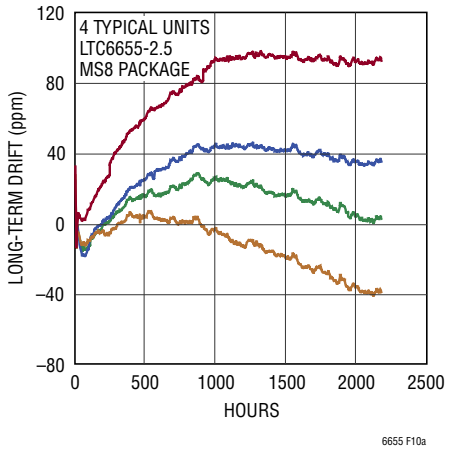

Figure 10a. Long-Term Drift MS8

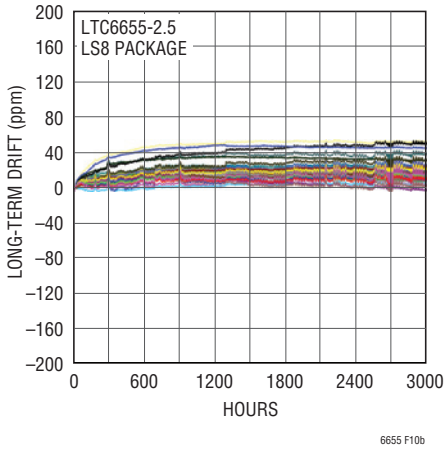

Figure 10b. Long-Term Drift LS8

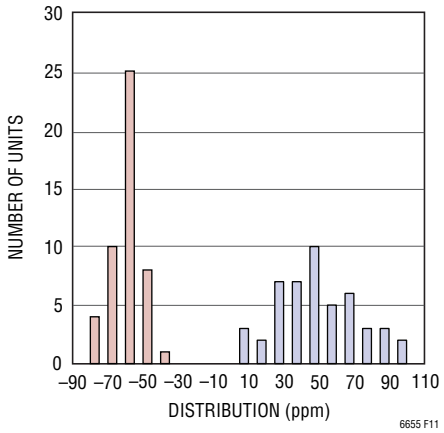

Figure 11. Hysteresis Plot –40°C to 125°C

Hysteresis

Thermal hysteresis is a measure of change of output voltage as a result of temperature cycling. Figure 11 illustrates the typical hysteresis based on data taken from the LTC6655-2.5. A proprietary design technique minimizes thermal hysteresis.

Humidity Sensitivity

Plastic mould compounds absorb water. With changes in relative humidity, plastic packaging materials change the amount of pressure they apply to the die inside, which can cause slight changes in the output of a voltage reference, usually on the order of 100ppm. The LS8 package is hermetic, so it is not affected by humidity, and is therefore more stable in environments where humidity may be a concern. However, PC board material may absorb water and apply mechanical stress to the LTC6655LS8. Proper board materials and layout are essential.

For best stability, the PC board layout is critical. Change in temperature and position of the PC board, as well as aging, can alter the mechanical stress applied to components soldered to the board. FR4 and similar materials also absorb water, causing the board to swell. Even conformal coating or potting of the board does not always eliminate this effect, though it may delay the symptoms by reducing the rate of absorption.

Power and ground planes should be omitted under the voltage reference IC for best stability. Figure 12a shows a tab cut through the PC board on three sides of an LTC6655, which significantly reduces stress on the IC, as described in Application Note 82. For even better performance, Figure 12b shows slots cut through the PC board on all four sides. The slots should be as long as possible, and the corners just large enough to accommodate routing of traces. It has been shown that for PC boards designed in this way, humidity sensitivity can be reduced to less than 35ppm for a change in relative humidity of approximately 60%. Mounting the reference near the center of the board, with slots on four sides, can further reduce the sensitivity to less than 10ppm.

An additional advantage of slotting the PC board is that the LTC6655 is thermally isolated from surrounding circuitry. This can help reduce thermocouple effects and improve accuracy.

APPLICATIONS INFORMATION

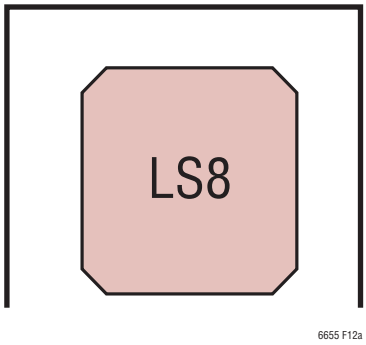

Figure 12a. 3-Sided PCB Tab Cutout

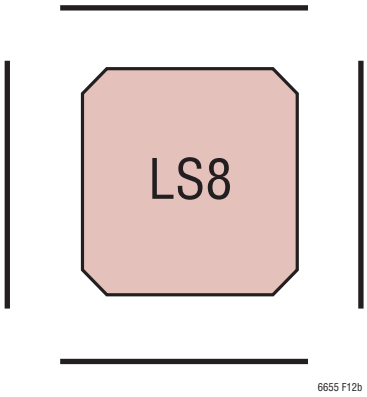

Figure 12b. 4-Sided PCB Cutout

Power Dissipation

Power dissipation for the LTC6655 depends on V_{IN} and load current. Figure 13 illustrates the power consumption versus V_{IN} under a no-load and 5mA load condition at room temperature for the LTC6655-2.5. Other voltage options display similar behavior.

The MSOP8 package has a thermal resistance (θ_{JA}) equal to 300°C/W. Under the maximum loaded condition, the increase in die temperature is over 35°C. If operated at these conditions with an ambient temperature of 125°C, the absolute maximum junction temperature rating of the device would be exceeded. Although the maximum junction temperature is 150°C, for best performance it is recommended to not exceed a junction temperature of 125°C. The plot in Figure 14 shows the recommended maximum ambient temperature limits for differing V_{IN} and load conditions using a maximum junction temperature of 125°C.

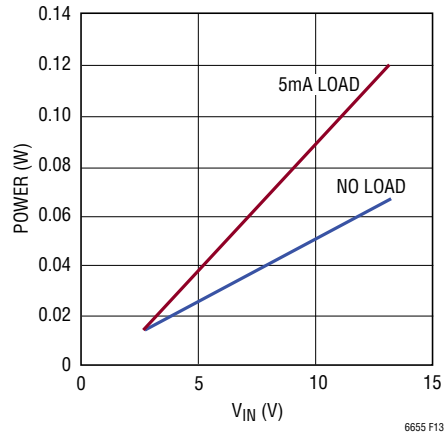

Figure 13. LTC6655-2.5 Power Consumption

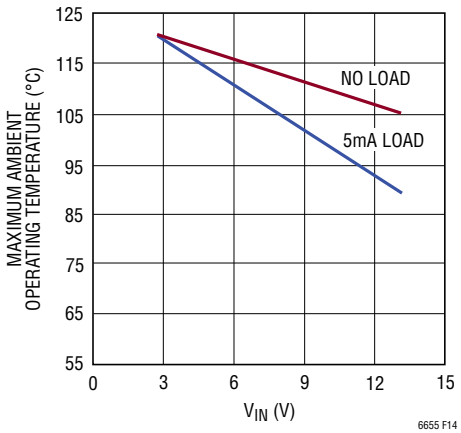

Figure 14. LTC6655-2.5 Maximum Ambient Operating Temperature

PC Board Layout

The LTC6655 reference is a precision device that is factory trimmed to an initial accuracy of ±0.025%, as shown in the Typical Performance Characteristics section. The mechanical stress caused by soldering parts to a printed circuit board may cause the output voltage to shift and the temperature coefficient to change.

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To reduce the effects of stress-related shifts, mount the reference near the short edge of a printed circuit board or in a corner. In addition, slots can be cut into the board on two sides of the device to reduce mechanical stress. A thicker and smaller board is stiffer and less prone to bend. Finally, use stress relief, such as flexible standoffs, when mounting the board.

Additional precautions include making sure the solder joints are clean and the board is flux free to avoid leakage paths. Sample PCB layouts are shown in Figures 15a and 15b.

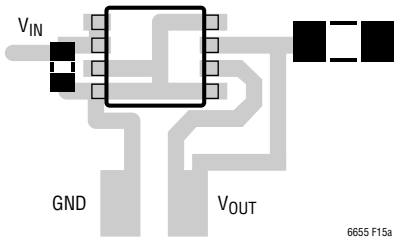

Figure 15a. Sample LTC6655 PCB Layout

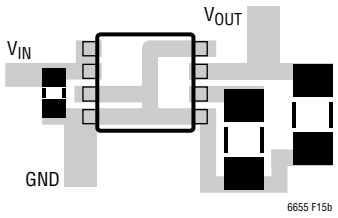

Figure 15b. Sample LTC6655LN PCB Layout

Load Regulation

To take advantage of the V_{OUT} Kelvin force/sense pins, the V_{OUT_S} pin should be connected separately from the V_{OUT_F} pin as shown in Figure 16.

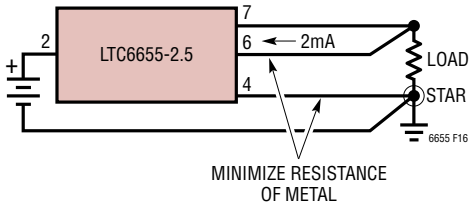

Figure 16. Kelvin Connection for Good Load Regulation

The V_{OUT_S} pin sinks 2mA, which is unusual for a Kelvin connection. However, this is required to achieve the exceptional low noise performance. The I • R drop on the V_{OUT_S} line directly affects load regulation. The V_{OUT_S} trace should be as short and wide as practical to minimize series resistance The V_{OUT_S} trace adds error as R_{TRACE} • 2mA, so a 0.1Ω trace adds 200µV error. The V_{OUT_F} pin is not as important as the V_{OUT_S} pin in this regard. An I • R drop on the V_{OUT_F} pin increases the minimum supply voltage when sourcing current, but does not directly affect load regulation. For light loading of the output (maximum output current <100µA), V_{OUT_S} should be tied to V_{OUT_F} by the shortest possible path to reduce errors caused by resistance in the sense trace.

Careful attention to grounding is also important, especially when sourcing current. The return load current can produce an I • R drop causing poor load regulation. Use a "star" ground connection and minimize the ground to load metal resistance. Although there are several pins that are required to be connected to ground, Pin 4 is the actual ground for return current.

Optimal Noise Performance

The LTC6655 offers extraordinarily low noise for a bandgap reference—only 0.25ppm in 0.1Hz to 10Hz. As a result, system noise performance may be dominated by system design and physical layout.

Some care is required to achieve the best possible noise performance. The use of dissimilar metals in component leads and PC board traces creates thermocouples. Variations in thermal resistance, caused by uneven air flow, create differential lead temperatures, thereby causing thermoelectric voltage noise at the output of the reference. Minimizing the number of thermocouples, as well as limiting airflow, can substantially reduce these errors. Additional information can be found in Analog Devices Application Note 82. Position the input and load capacitors close to the part. Although the LTC6655 has a DC PSRR of over 100dB, the power supply should be as stable as possible to guarantee optimal performance. A plot of the 0.1Hz to 10Hz low frequency noise is shown in the Typical Performance Characteristics section. Noise

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performance can be further improved by wiring several LTC6655s in parallel as shown in the Typical Applications section. With this technique the noise is reduced by $\sqrt{N}$, where N is the number of LTC6655s in parallel.

Noise Specification

Noise in any frequency band is a random function based on physical properties such as thermal noise, shot noise, and flicker noise. The most precise way to specify a random error such as noise is in terms of its statistics, for example as an RMS value. This allows for relatively simple maximum error estimation, generally involving assumptions about noise bandwidth and crest factor. Unlike wideband noise, low frequency noise, typically specified in a 0.1Hz to 10Hz band, has traditionally been specified in terms of expected error, illustrated as peak-to-peak error. Low frequency noise is generally measured with an oscilloscope over a 10 second time frame. This is a pragmatic approach, given that it can be difficult to measure noise accurately at low frequencies, and that it can also be difficult to agree on the statistical characteristics of the noise, since flicker noise dominates the spectral density. While practical, a random sampling of 10 second intervals is an inadequate method for representation of low frequency noise, especially for systems where this noise is a dominant limit of system performance. Given the random nature of noise, the output voltage may be observed over many time intervals, each giving different results. Noise specifications that were determined using this method are prone to subjectivity, and will tend toward a mean statistical value, rather than the maximum noise that is likely to be produced by the device in question.

Because the majority of voltage reference data sheets express low frequency noise as a typical number, and as it tends to be illustrated with a repeatable plot near the mean of a distribution of peak-to-peak values, the LTC6655 data sheet provides a similarly defined typical specification in order to allow a reasonable direct comparison against similar products. Data produced with this method generally suggests that in a series of 10 second output voltage measurements, at least half the observations should have a peak-to-peak value that is below this number. For example, the LTC6655-2.5 measures less than $0.25ppm_{P-P}$ in at least 50% of the 10 second observations.

As mentioned above, the statistical distribution of noise is such that if observed for long periods of time, the peak error in output voltage due to noise may be much larger than that observed in a smaller interval. The likely maximum error due to noise is often estimated using the RMS value, multiplied by an estimated crest factor, assumed to be in the range of 6 to 8.4. This maximum possible value will only be observed if the output voltage is measured for very long periods of time. Therefore, in addition to the common method, a more thorough approach to measuring noise has been used for the LTC6655 (described in detail in Analog Devices's AN124) that allows more information to be obtained from the result. In particular, this method characterizes the noise over a significantly greater length of time, resulting in a more complete description of low frequency noise. The peak-to-peak voltage is measured for 10 second intervals over hundreds of intervals. In addition, an electronic peak-detect circuit stores an objective value for each interval. The results are then summarized in terms of the fraction of measurement intervals for which observed noise is below a specified level. For example, the LTC6655-2.5 measures less than $0.27ppm_{P-P}$ in 80% of the measurement intervals, and less than $0.295ppm_{P-P}$ in 95% of observation intervals. This statistical variation in noise is illustrated in Table 2 and Figure 18. The test circuit is shown in Figure 17.

Table 2.

	Low Frequency Noise (ppm_{P-P})
50%	0.246
60%	0.252
70%	0.260
80%	0.268
90%	0.292

This method of testing low frequency noise is superior to more common methods. The results yield a comprehensive statistical description, rather than a single observation. In addition, the direct measurement of output voltage over time gives an actual representation of peak noise, rather than an estimate based on statistical assumptions such as crest factor. Additional information can be derived from a measurement of low frequency noise spectral density, as shown in Figure 19.

APPLICATIONS INFORMATION

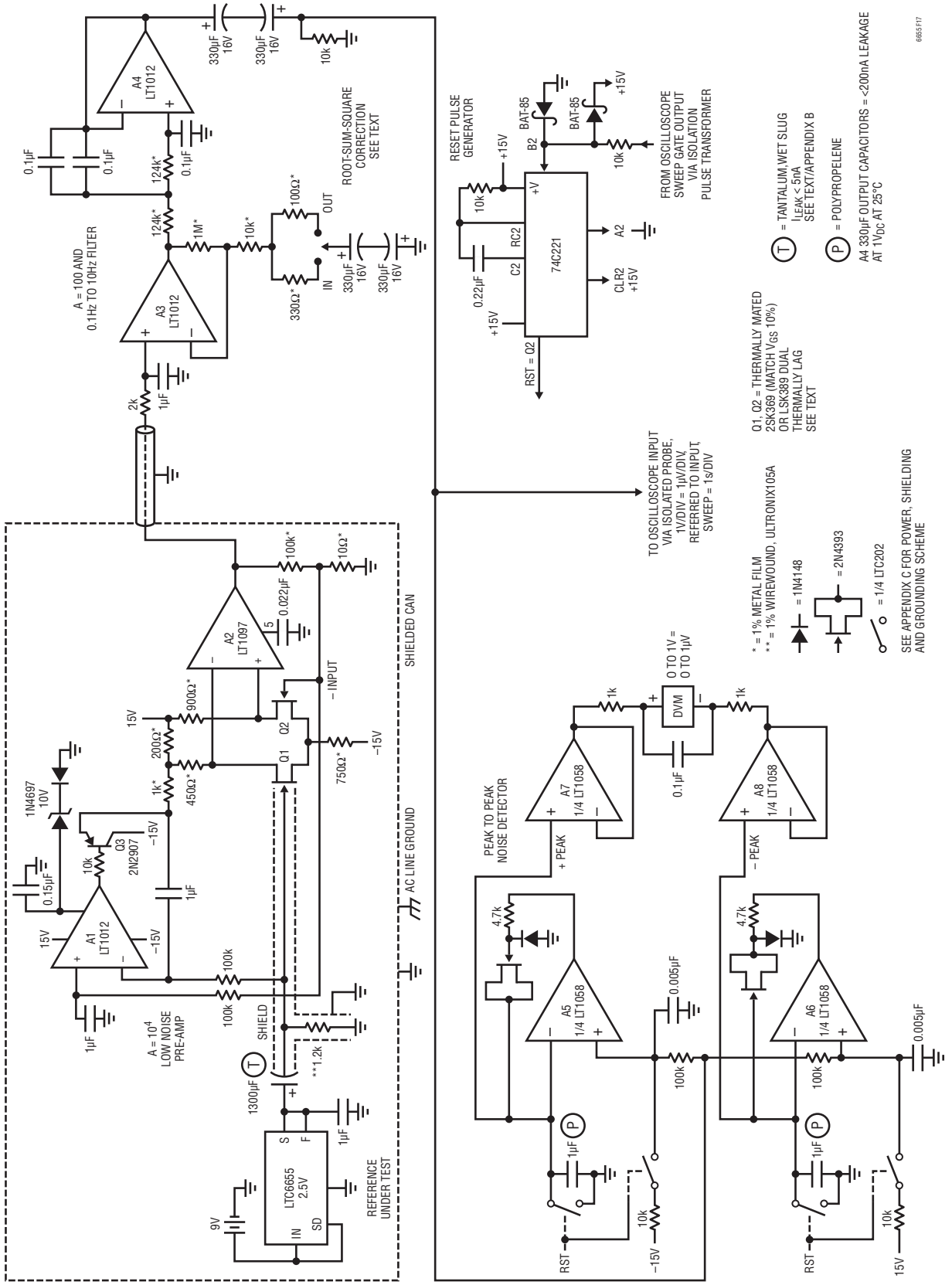

Figure 17. Detailed Noise Test Circuitry. See Application Note 124

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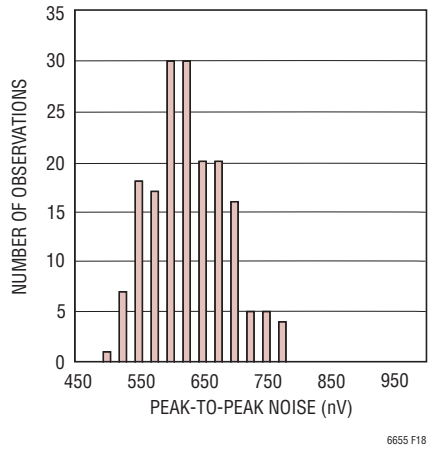

Figure 18. LTC6655-2.5 Low Frequency Noise Histogram

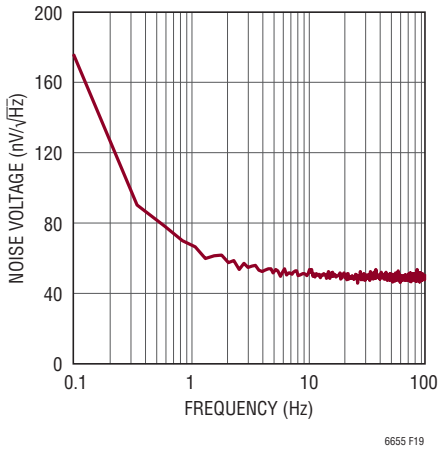

Figure 19. LTC6655-2.5 Low Frequency Noise Spectrum

It should be noted from Figure 19 that the LTC6655 has not only a low wideband noise, but an exceptionally low flicker noise corner of 1Hz! This substantially reduces low frequency noise, as well as long-term variation in peak noise.

Noise Reduction and the NR Pin

The LTC6655LN provides access to an internal circuit node preceding the output buffer so that dynamic performance is not affected. This facilitates the use of a low pass filter (LPF) to reduce wide band noise.

The Block Diagram section illustrates the LTC6655LN architectural differences. The Low Noise version trades out the Kelvin sense pin for the NR pin. Figure 20 shows the typical application circuit with a capacitor on the NR pin. When a capacitor is placed between NR and ground, a LPF is formed.

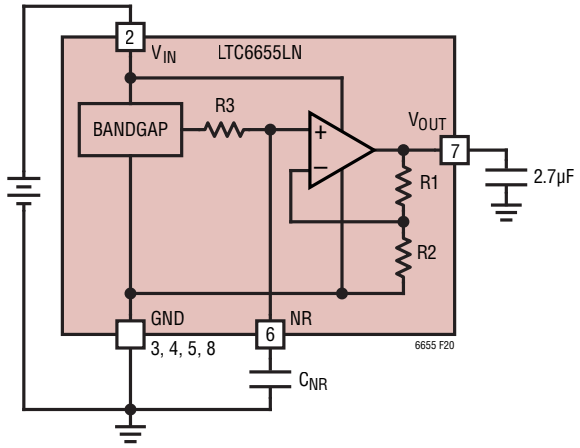

Figure 20. The LTC6655LN Typical Application Circuit

The LPF reduces the wide band noise from the bandgap circuit before it reaches the output buffer. This is very different from placing a LPF after the reference. A LPF following the buffer would cause poor load regulation and slow down the response affecting dynamic performance. With the LPF internally placed before the low noise buffer, the buffer response is not impeded by the LPF. Placing anything between the output buffer and the converter will likely add noise or cause an error such as a load regulation error, or a dynamic response error.

The value of resistor R3 is slightly different depending on the voltage option. Tables 3 and 4 below list the resistance values of R3 for the three available voltage options along with the 3dB cutoff frequencies for four decades of capacitor values.

Table 3. Resistance Value of R3 for the Three Voltage Options

	2.500	4.096	5.000	V
R3 ±15%	5305	4233	3969	Hz

Table 4. The 3dB Cutoff Frequencies for Different Values of C_{NR}

CNR	2.500	4.096	5.000	V
0.1µF	5305	4233	3969	Hz
1µF	531	423	397	Hz
10µF	53	423	397	Hz
100µF	5.3	4.2	4.0	Hz

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Internally the NR pin connects to a sensitive node. Any leakage to this pin can cause excessive shift and drift. Leakage of 10nA will cause a shift of 9µV in V_{OUT}. It is recommended to use high quality, low leakage capacitors. A guard ring may also be employed to control leakage. The nominal pin voltage of NR is 1.000V or 1.024V.

The LTC6655LN-2.5 output noise for three conditions is shown in Figure 21. Without a capacitor on the NR pin the wideband noise extends past 10kHz at 50nV/√Hz. When a 1µF or 100µF capacitor is included, the wideband noise is reduced to 16nV/√Hz. The noise corner frequency produced by the LPF decreases as the capacitor increases.

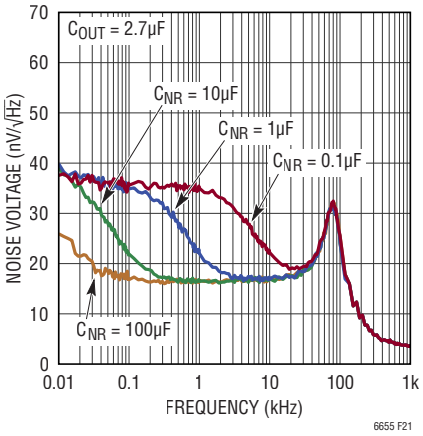


Figure 21. The LTC6655LN-2.5 Output Voltage Noise Spectrum Using the C_{NR} Capacitor

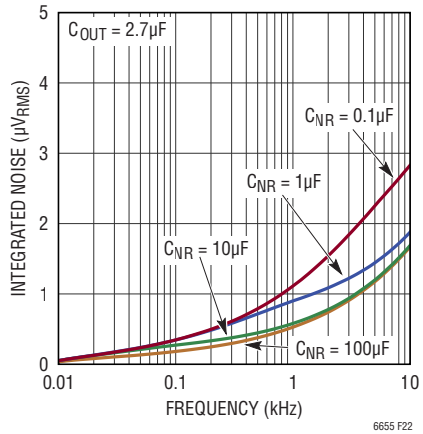


Figure 22. Total Integrated Noise of the LTC6655LN-2.5 Using the C_{NR} Capacitor

A plot of the total integrated noise for the same three conditions is shown in Figure 22. A large value of C_{NR} can have a large impact on the total integrated noise.

Start-Up with C_{NR}

The C_{NR} capacitor will require time to charge. The LTC6655 has an initial accuracy of 0.025%. A single RC time constant circuit will require approximately 8.3τ to reach 0.025% settling. For example, assume R3 = 300Ω and C_{NR} = 10µF; the time constant is R • C = 300Ω • 10µF = 3ms. For 0.025% settling multiply 8.3 • 3ms to get 24.9ms. This is the time required for the signal at the NR pin to settle to 0.025% of its final value. The output buffer will follow the NR pin signal with some delay depending on the capacitive loading on the V_{OUT} pin.

Example start-up measurements are shown in Figures 23a, 23b, and 23c. Figure 23a shows the difference between using no capacitor and a 1µF capacitor on the NR pin. Figures 23b and 23c show the start-up with C_{NR} = 10µF and 100µF, respectively.

IR Reflow Shift

The mechanical stress of soldering a part to a board can cause the output voltage to shift. Moreover, the heat of an IR reflow or convection soldering oven can also cause the output voltage to shift. The materials that make up a semiconductor device and its package have different rates of expansion and contraction. After a part undergoes the extreme heat of a lead-free IR reflow profile, like the one shown in Figure 24, the output voltage shifts. After the device expands, due to the heat, and then contracts, the stresses on the die have changed position. This shift is similar, but more extreme than thermal hysteresis.

Experimental results of IR reflow shift are shown below in Figure 25. These results show only shift due to reflow and not mechanical stress.

APPLICATIONS INFORMATION

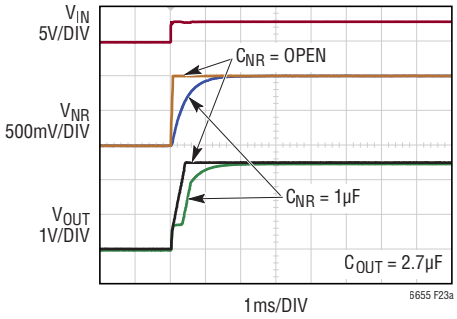


Figure 23a. C_{NR} = Open and 10µF

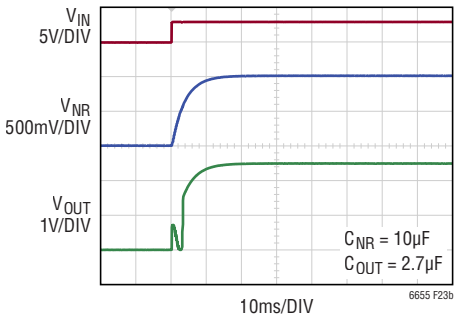


Figure 23b. C_{NR} = 10µF

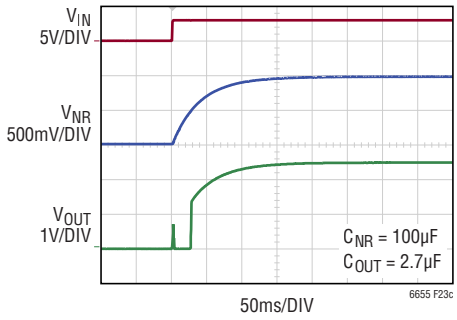


Figure 23c. C_{NR} = 100µF

Figure 23. The LTC6655LN-2.5 Start-Up Response with a) No C_{NR} Capacitor and C_{NR} = 1µF, b) C_{NR} = 10µF, and c) C_{NR} = 100µF

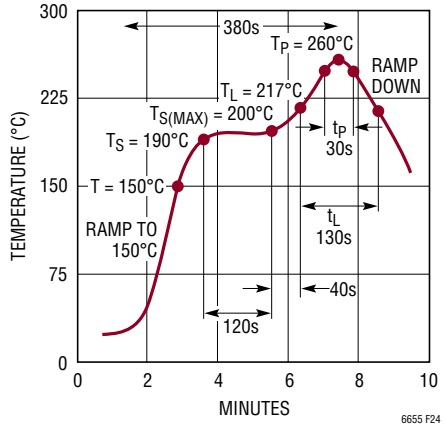


Figure 24. Lead-Free Reflow Profile

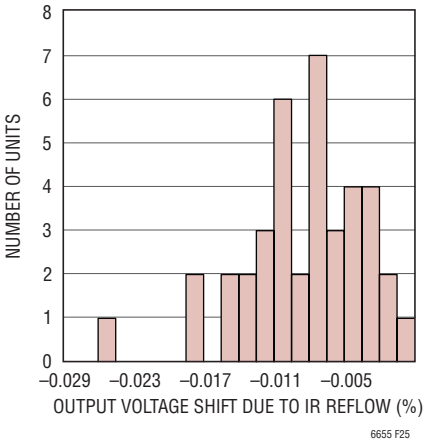
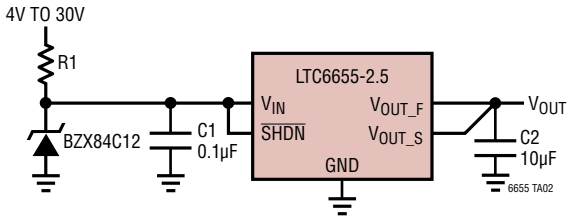


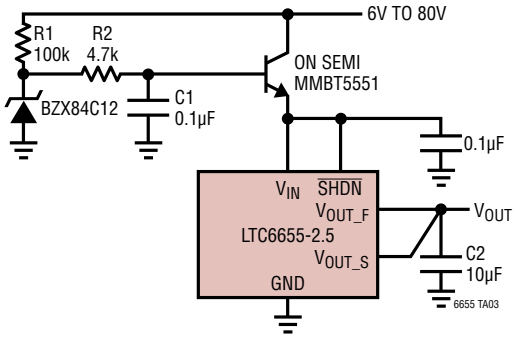
Figure 25. Output Voltage Shift Due to IR Reflow

TYPICAL APPLICATIONS

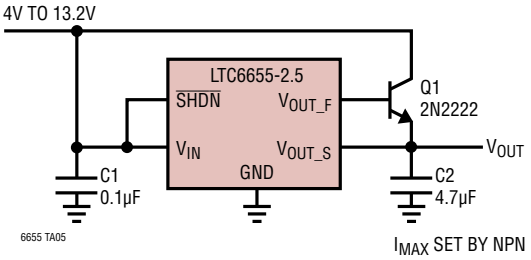
Extended Supply Range Reference



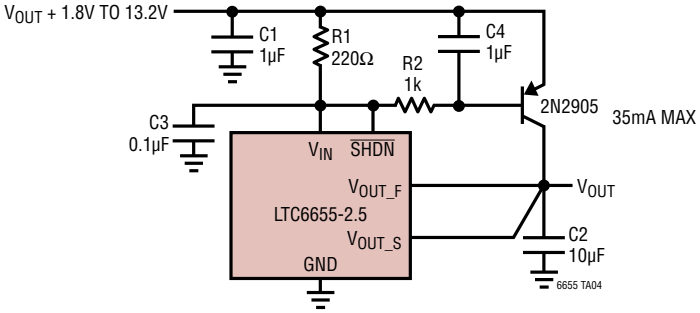
Extended Supply Range Reference



Boosted Output Current

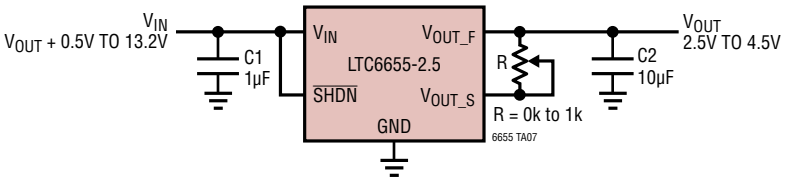


Boosted Output Current



TYPICAL APPLICATIONS

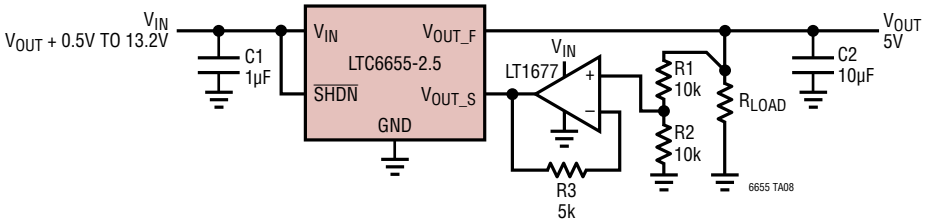
Output Voltage Boost



V_{OUT} = VOLTAGE OPTION + 0.002 • R
THIS EXAMPLE USES 2.5V AS THE VOLTAGE OPTION

FOR R USE A POTENTIOMETER THAT CAN HANDLE 2mA, IS LOW NOISE AND HAS A LOW TEMPERATURE COEFFICIENT

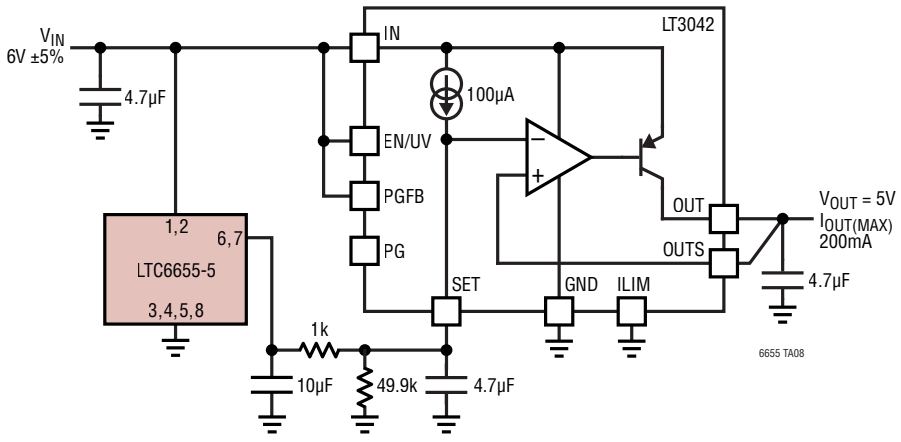
Low Noise Precision Voltage Boost Circuit



V_{OUT} = VOLTAGE OPTION • (1 + R1/R2)
THIS EXAMPLE USES 2.5V AS THE VOLTAGE OPTION

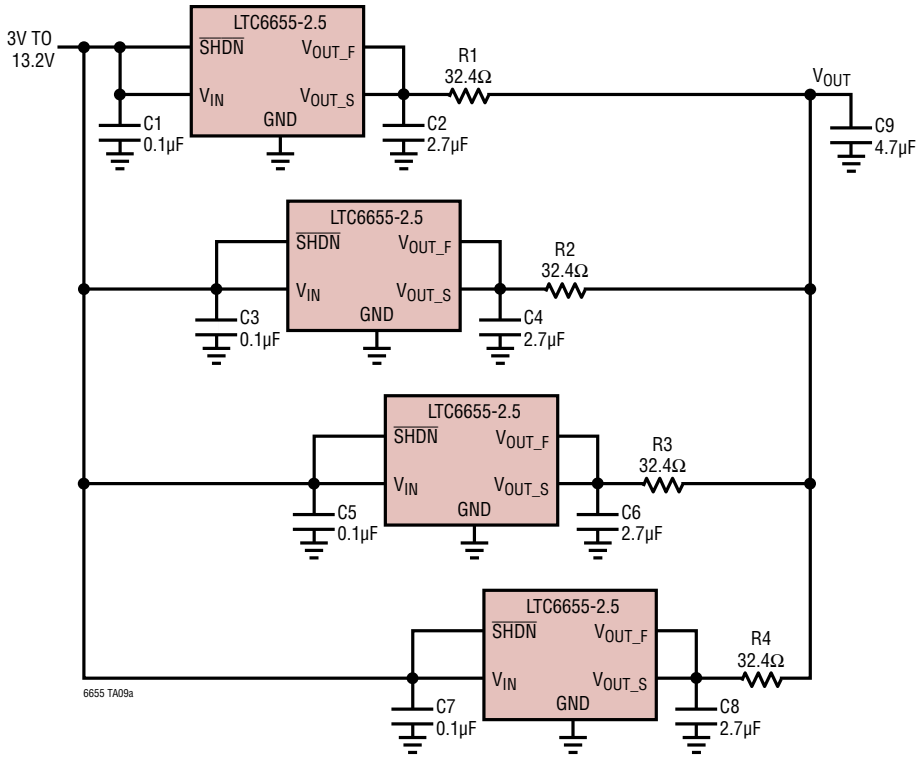
FOR R1, R2 AND R3 USE LT5400-1. WITH A PRECISION ARRAY THE MATCHING AND LOW TC WILL HELP PRESERVE LOW DRIFT. R3 = R1||R2 R3 IS MADE WITH TWO PRALLEL 10k RESISTORS, AVAILABLE IN THE LT5400-1

Ultralow 1/f Noise Reference Buffer

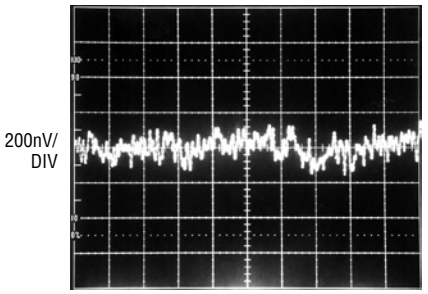


TYPICAL APPLICATIONS

Low Noise Statistical Averaging Reference
$e'_N = e_N/\sqrt{N}$; Where N is the Number of LTC6655s in Parallel



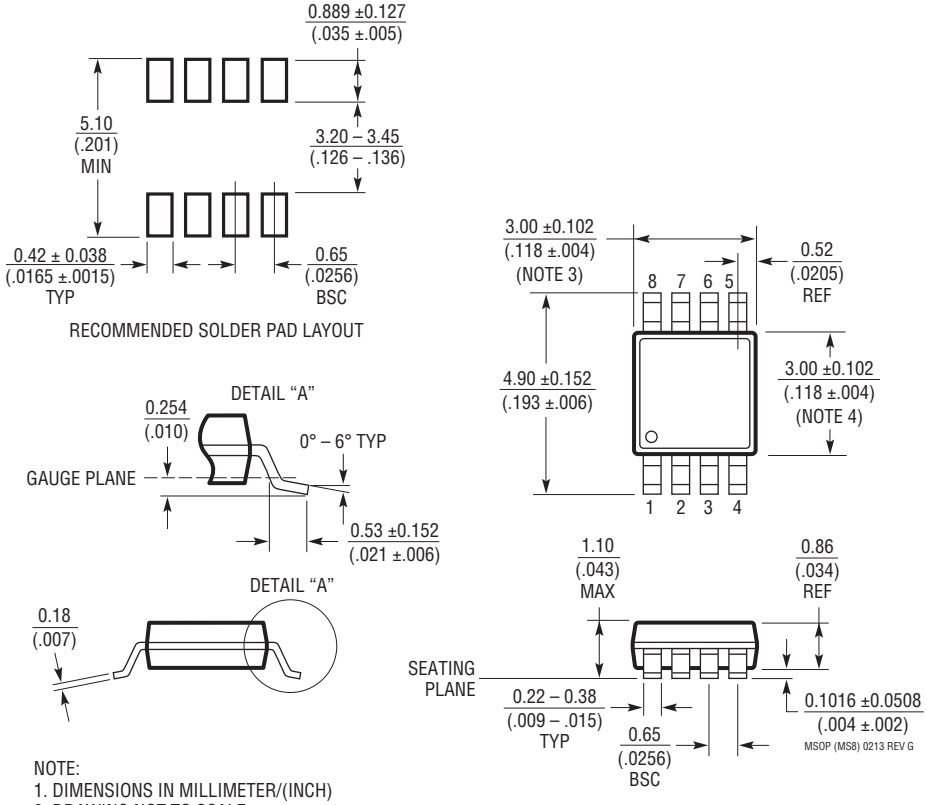
Low Frequency Noise (0.1Hz to 10Hz)
with Four LTC6655-2.5 in Parallel



$320nV_{P-P}$
0.1Hz to 10Hz

PACKAGE DESCRIPTION

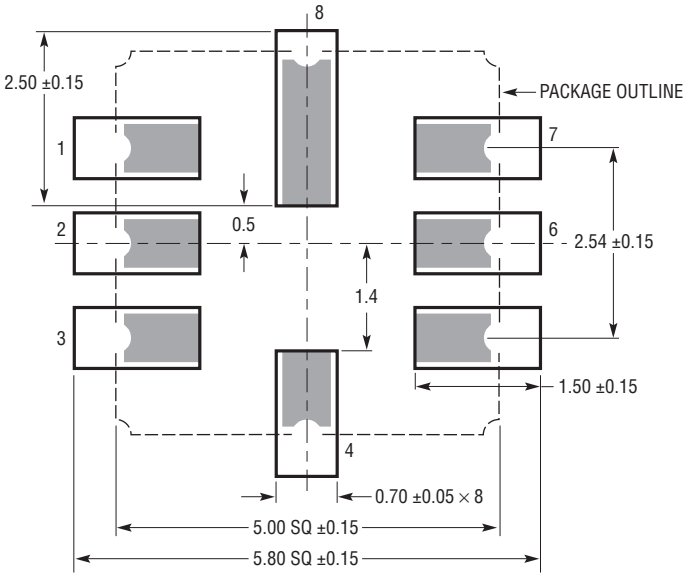
MS8 Package
8-Lead Plastic MSOP
(Reference LTC DWG # 05-08-1660 Rev G)



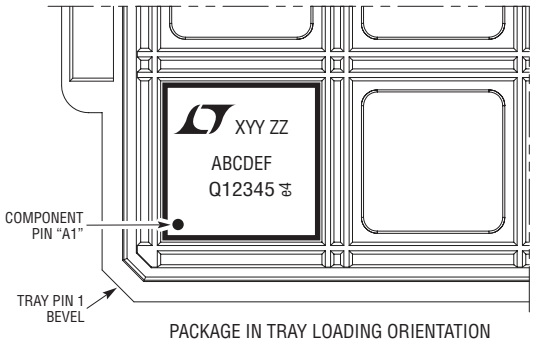
NOTE:
1. DIMENSIONS IN MILLIMETER/(INCH)
2. DRAWING NOT TO SCALE
3. DIMENSION DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS.
   MOLD FLASH, PROTRUSIONS OR GATE BURRS SHALL NOT EXCEED 0.152mm (.006") PER SIDE
4. DIMENSION DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSIONS.
   INTERLEAD FLASH OR PROTRUSIONS SHALL NOT EXCEED 0.152mm (.006") PER SIDE
5. LEAD COPLANARITY (BOTTOM OF LEADS AFTER FORMING) SHALL BE 0.102mm (.004") MAX

PACKAGE DESCRIPTION

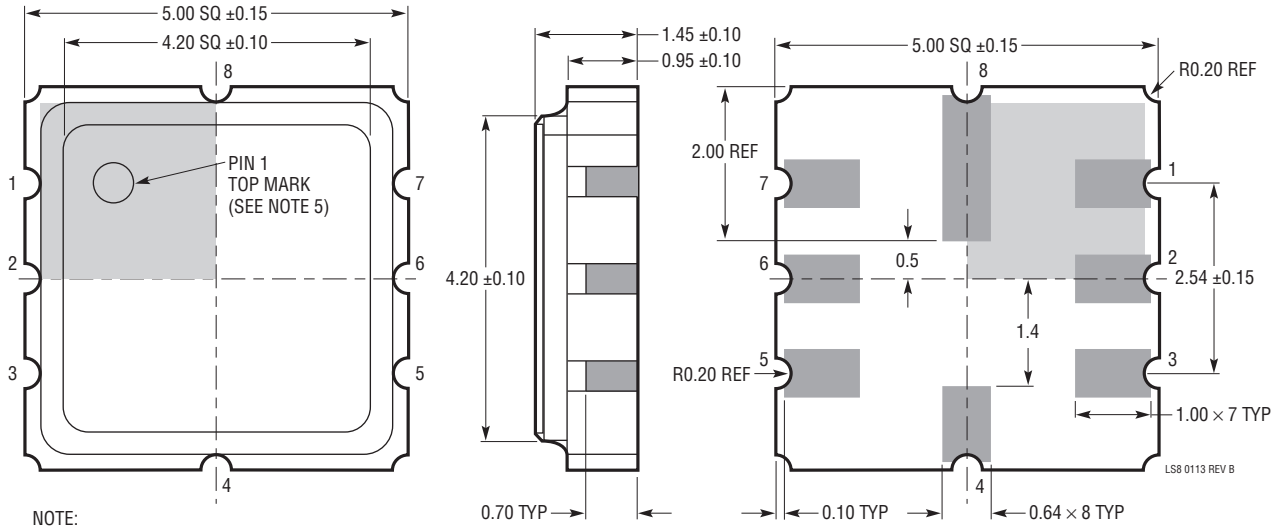
LS8 Package
8-Pin Leadless Chip Carrier (5mm × 5mm)
(Reference LTC DWG # 05-08-1852 Rev B)



APPLY SOLDER MASK TO AREAS THAT ARE NOT SOLDERED



PACKAGE IN TRAY LOADING ORIENTATION



NOTE:
1. ALL DIMENSIONS ARE IN MILLIMETERS
2. DRAWING NOT TO SCALE
3. DIMENSIONS PACKAGE DO NOT INCLUDE PLATING BURRS
   PLATING BURRS, IF PRESENT, SHALL NOT EXCEED 0.30mm ON ANY SIDE
4. PLATING—ELECTO NICKEL MIN 1.25UM, ELECTRO GOLD MIN 0.30UM
5. SHADED AREA IS ONLY A REFERENCE FOR PIN 1 LOCATION ON THE
   TOP AND BOTTOM OF PACKAGE

REVISION HISTORY

REV	DATE	DESCRIPTION	PAGE NUMBER
A	02/10	Voltage Options Added (1.250, 2.048, 3.000, 3.300, 4.096, 5.000), Reflected Throughout the Data Sheet	1 to 22
B	12/12	Addition of 5mm x 5mm hermetic LS8 package	1, 2, 3, 12, 22
		Update to Electrical Characteristics to include LS8 package	3, 4
		Addition of long-term drift and hysteresis plots for LS8 package	13
		Addition of Humidity Sensitivity information	13
		Addition of Related Parts	22
C	06/13	T_{JMAX} changed from 125°C to 150°C	2
		Addition of 5V Option in the LS8 package	3, 4
		Addition of PC board layout guidance	14, 15
D	01/14	Addition of 4.096V option in the LS8 package	3, 4
		Changed Line Regulation Condition to $\overline{SHDN}$ = 2V	4
		Updated PC board layout guidance	14
		Corrected Polarity of 9V battery in Figure 17	18
		Updated captions for Figures 10, 12, 18	14, 15, 19
		Updated note for circuit “Low Noise Precision Voltage Boost Circuit”	21
E	9/14	Corrected LS8-4.096 part marking	3
F	08/17	Trademark information updated.	1
		Web links updated.	3, 23, 24
		Addition of Ultralow 1/f Noise Reference Buffer schematic.	21
G	02/19	Addition of LTC6655LN Specifications and Features.	1 to 6, 11, 12, 18, 22, 23

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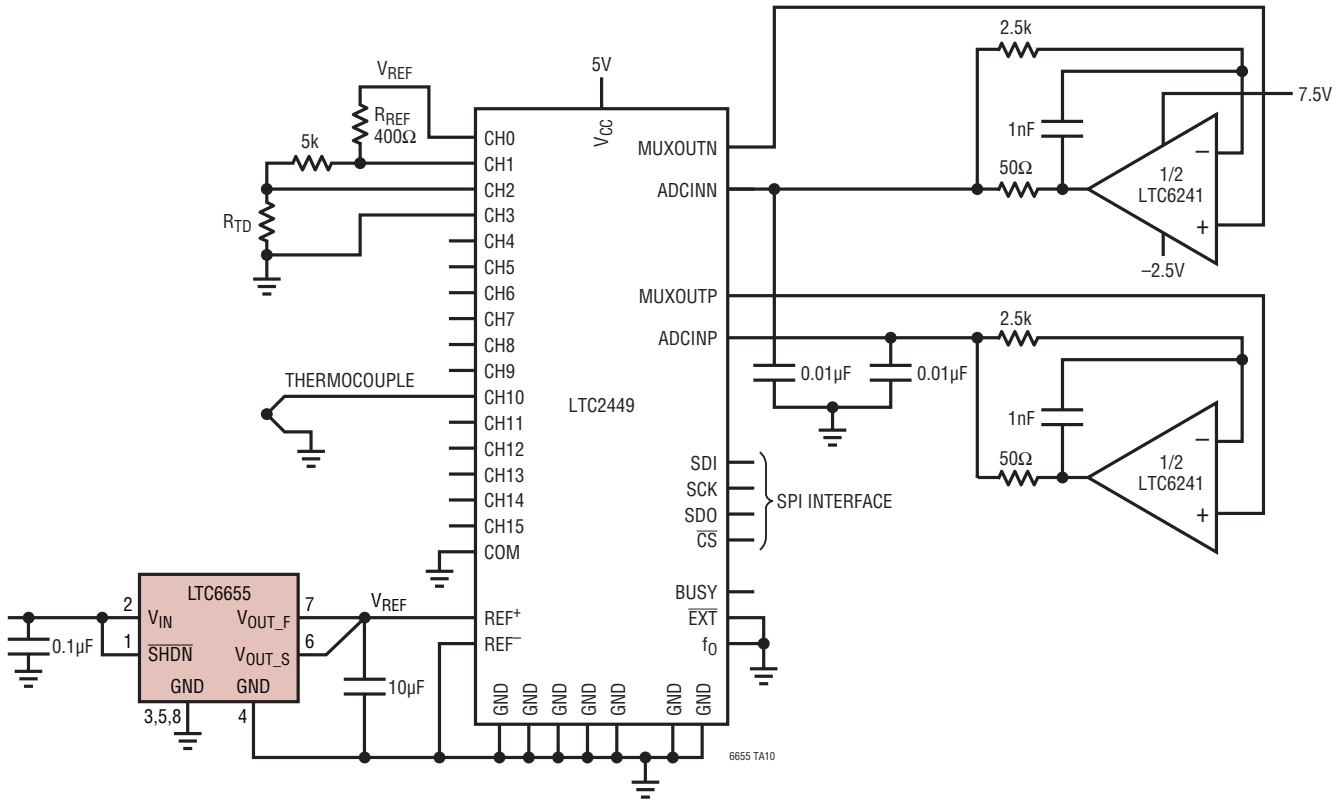
TYPICAL APPLICATION

Low Noise Precision 24-Bit Analog-to-Digital Converter Application



RELATED PARTS

PART NUMBER	DESCRIPTION	COMMENTS
LT®1236	Precision Low Drift Low Noise Reference	0.05% Max, 5ppm/°C Max, 1ppm (Peak-to-Peak) Noise
LT1236LS8	Precision Low Noise, Low Profile Hermetic Voltage Reference	0.05% Max, 5ppm/°C Max, 0.3µV_{P-P} Noise, 5mm × 5mm Hermetic Package
LT1460	Micropower Series References	0.075% Max, 10ppm/°C Max, 20mA Output Current
LT1461	Micropower Series Low Dropout	0.04% Max, 3ppm/°C Max, 50mA Output Current
LT1790	Micropower Precision Series References	0.05% Max, 10ppm/°C Max, 60mA Supply, SOT23 Package
LT6650	Micropower Reference with Buffer Amplifier	0.5% Max, 5.6µA Supply, SOT23 Package
LTC6652	Precision Low Drift Low Noise Reference	0.05% Max, 5ppm/°C Max, –40°C to 125°C, MSOP8
LT6660	Tiny Micropower Series Reference	0.2% Max, 20ppm/°C Max, 20mA Output Current, 2mm × 2mm DFN
LTC6652LS8	High Precision, Buffered Voltage Reference Family in 5mm × 5mm Hermetic QFN Package	0.05% Max Initial Error, 5ppm/°C Max Drift, Shutdown Current <2µA, –40°C to 125°C Operation
LT6654LS8	Precision, Low Noise, High Output Drive Voltage Reference Family in 5mm × 5mm Hermetic QFN Package	1.6ppm Peak-to-Peak Noise (0.1Hz to 10Hz, Sink/Source ±10mA, 5ppm/°C Max Drift, –40°C to 125°C Operation

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