



**THE DATASHEET OF  
LTC6652AHMS8-1.25#TRPBF**



# Precision Low Drift Low Noise Buffered Reference

## FEATURES

- **Low Drift:**
  - A-Grade 5ppm/°C Max**
  - B-Grade 10ppm/°C Max (MSOP8)**
  - B-Grade 8ppm/°C Max (LS8)**
- **High Accuracy:**
  - A-Grade ±0.05% Max**
  - B-Grade ±0.1% Max**
- **Low Noise: 2.1ppm<sub>p-p</sub> (0.1Hz to 10Hz)**
- **100% Tested at -40°C, 25°C and 125°C**
- Sinks and Sources Current: ±5mA
- Low Power Shutdown: <2μA Maximum
- Thermal Hysteresis (LS8): 45ppm (-40°C to 125°C)
- Long-Term Drift (LS8): 20ppm/√kHr
- Low Dropout: 300mV
- Available Output Voltage Options: 1.25V, 2.048V, 2.5V, 3V, 3.3V, 4.096V, 5V
- 8-Lead MSOP and 5mm × 5mm Surface Mount Hermetic Packages

## APPLICATIONS

- Automotive Control and Monitoring
- High Temperature Industrial
- High Resolution Data Acquisition Systems
- Instrumentation and Process Control
- Precision Regulators
- Medical Equipment

## DESCRIPTION

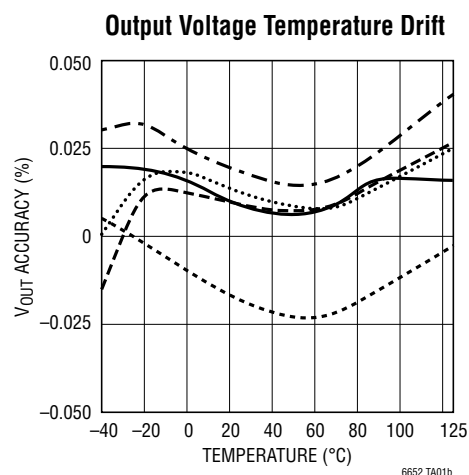
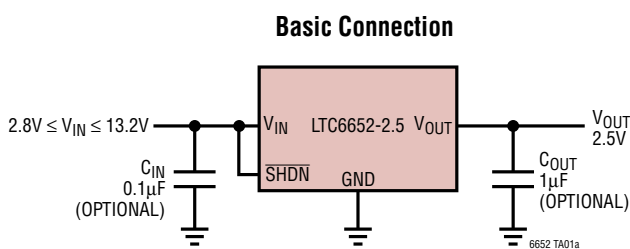
The **LTC®6652** family of precision, low drift, low noise references is fully specified over the temperature range of -40°C to 125°C. High order curvature compensation allows these references to achieve a low drift of less than 5ppm/°C with a predictable temperature characteristic and an output voltage accuracy of ±0.05%. The performance over temperature should appeal to automotive, high performance industrial and other high temperature applications.

The LTC6652 voltage references can be powered from supply voltages up to 13.2V. They boast low noise, excellent load regulation, source and sink capability and exceptional line rejection, making them a superior choice for demanding precision applications. A shutdown mode allows power consumption to be reduced when the reference is not needed. The optional output capacitor can be left off when space constraints are critical.

The LTC6652 references are offered in an 8-lead MSOP package and an 8-lead LS8 package. The LS8 is a 5mm × 5mm surface mount hermetic package that provides outstanding stability.

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## TYPICAL APPLICATION



# LTC6652

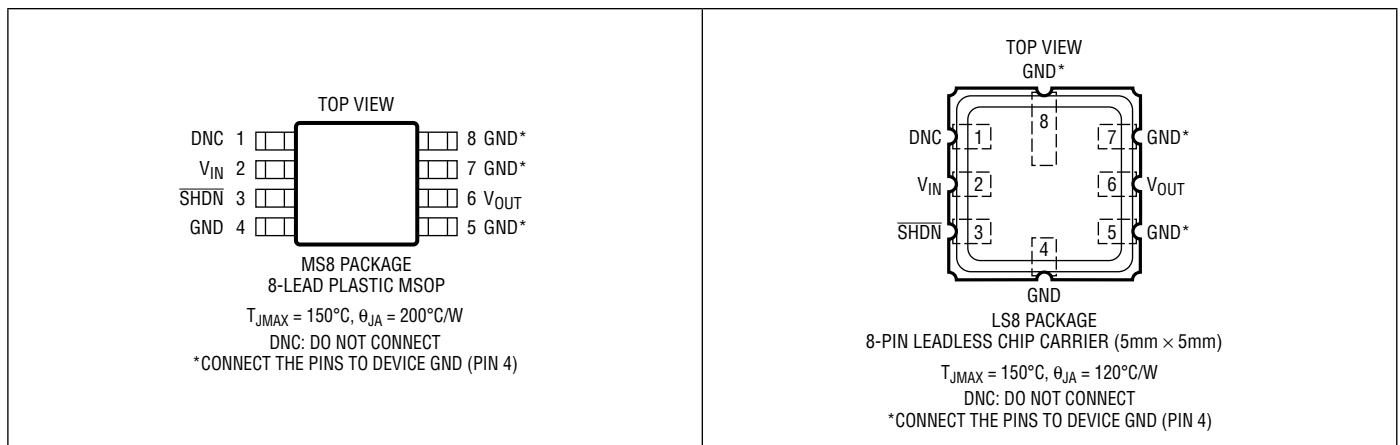
## ABSOLUTE MAXIMUM RATINGS

(Note 1)

Input Voltage  
 $V_{IN}$  to GND ..... -0.3V to 13.2V  
 SHDN to GND ..... -0.3V to ( $V_{IN} + 0.3V$ )  
 Output Voltage  
 $V_{OUT}$ ..... -0.3V to ( $V_{IN} + 0.3V$ )  
 Output Short-Circuit Duration..... Indefinite

Operating Temperature Range ..... -40°C to 125°C  
 Storage Temperature Range (Note 2) ..... -65°C to 150°C  
 Lead Temperature Range (Soldering, 10 sec)  
 (Note 9)..... 300°C

## PIN CONFIGURATION



## ORDER INFORMATION

LEAD FREE FINISH	TAPE AND REEL	PART MARKING*	PACKAGE DESCRIPTION	SPECIFIED TEMPERATURE RANGE
LTC6652AHMS8-1.25#PBF	LTC6652AHMS8-1.25#TRPBF	LTCVH	8-Lead Plastic MSOP	-40°C to 125°C
LTC6652BHMS8-1.25#PBF	LTC6652BHMS8-1.25#TRPBF	LTCVH	8-Lead Plastic MSOP	-40°C to 125°C
LTC6652AHMS8-2.048#PBF	LTC6652AHMS8-2.048#TRPBF	LTCVJ	8-Lead Plastic MSOP	-40°C to 125°C
LTC6652BHMS8-2.048#PBF	LTC6652BHMS8-2.048#TRPBF	LTCVJ	8-Lead Plastic MSOP	-40°C to 125°C
LTC6652AHMS8-2.5#PBF	LTC6652AHMS8-2.5#TRPBF	LTCQV	8-Lead Plastic MSOP	-40°C to 125°C
LTC6652BHMS8-2.5#PBF	LTC6652BHMS8-2.5#TRPBF	LTCQV	8-Lead Plastic MSOP	-40°C to 125°C
LTC6652AHMS8-3#PBF	LTC6652AHMS8-3#TRPBF	LTCVK	8-Lead Plastic MSOP	-40°C to 125°C
LTC6652BHMS8-3#PBF	LTC6652BHMS8-3#TRPBF	LTCVK	8-Lead Plastic MSOP	-40°C to 125°C
LTC6652AHMS8-3.3#PBF	LTC6652AHMS8-3.3#TRPBF	LTCVM	8-Lead Plastic MSOP	-40°C to 125°C
LTC6652BHMS8-3.3#PBF	LTC6652BHMS8-3.3#TRPBF	LTCVM	8-Lead Plastic MSOP	-40°C to 125°C
LTC6652AHMS8-4.096#PBF	LTC6652AHMS8-4.096#TRPBF	LTCVN	8-Lead Plastic MSOP	-40°C to 125°C
LTC6652BHMS8-4.096#PBF	LTC6652BHMS8-4.096#TRPBF	LTCVN	8-Lead Plastic MSOP	-40°C to 125°C
LTC6652AHMS8-5#PBF	LTC6652AHMS8-5#TRPBF	LTCVP	8-Lead Plastic MSOP	-40°C to 125°C
LTC6652BHMS8-5#PBF	LTC6652BHMS8-5#TRPBF	LTCVP	8-Lead Plastic MSOP	-40°C to 125°C

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## ORDER INFORMATION

LEAD FREE FINISH	PART MARKING*	PACKAGE DESCRIPTION	SPECIFIED TEMPERATURE RANGE
LTC6652AHLS8-2.5#PBF†	665225	8-Lead Ceramic LCC 5mm × 5mm	–40°C to 125°C
LTC6652BHLS8-2.5#PBF†	665225	8-Lead Ceramic LCC 5mm × 5mm	–40°C to 125°C
LTC6652AHLS8-4.096#PBF†	524096	8-Lead Ceramic LCC 5mm × 5mm	–40°C to 125°C
LTC6652BHLS8-4.096#PBF†	524096	8-Lead Ceramic LCC 5mm × 5mm	–40°C to 125°C
LTC6652AHLS8-5#PBF†	66525	8-Lead Ceramic LCC 5mm × 5mm	–40°C to 125°C
LTC6652BHLS8-5#PBF†	66525	8-Lead Ceramic LCC 5mm × 5mm	–40°C to 125°C

Consult LTC Marketing for parts specified with wider operating temperature ranges. \*The temperature grade is identified by a label on the shipping container.

For more information on lead free part marking, go to: <http://www.linear.com/leadfree/>

For more information on tape and reel specifications, go to: <http://www.linear.com/tapeandree/>

†This product is only offered in trays. For more information go to: <http://www.linear.com/packaging/>

## AVAILABLE OPTIONS

OUTPUT VOLTAGE	INITIAL ACCURACY	TEMPERATURE COEFFICIENT	PART NUMBER**
1.250	0.05% 0.1%	5ppm/°C 10ppm/°C	LTC6652AHMS8-1.25 LTC6652BHMS8-1.25
2.048	0.05% 0.1%	5ppm/°C 10ppm/°C	LTC6652AHMS8-2.048 LTC6652BHMS8-2.048
2.500	0.05% 0.1% 0.05% 0.1%	5ppm/°C 10ppm/°C 5ppm/°C 8ppm/°C	LTC6652AHMS8-2.5 LTC6652BHMS8-2.5 LTC6652AHLS8-2.5 LTC6652BHLS8-2.5
3.000	0.05% 0.1%	5ppm/°C 10ppm/°C	LTC6652AHMS8-3 LTC6652BHMS8-3
3.300	0.05% 0.1%	5ppm/°C 10ppm/°C	LTC6652AHMS8-3.3 LTC6652BHMS8-3.3
4.096	0.05% 0.1% 0.05% 0.1%	5ppm/°C 10ppm/°C 5ppm/°C 8ppm/°C	LTC6652AHMS8-4.096 LTC6652BHMS8-4.096 LTC6652AHLS8-4.096 LTC6652BHLS8-4.096
5.000	0.05% 0.1% 0.05% 0.1%	5ppm/°C 10ppm/°C 5ppm/°C 8ppm/°C	LTC6652AHMS8-5 LTC6652BHMS8-5 LTC6652AHLS8-5 LTC6652BHLS8-5

\*\*See Order Information section for complete part number listing.

## ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at  $T_A = 25^\circ\text{C}$ ,  $V_{IN} = V_{OUT} + 0.5\text{V}$ , unless otherwise noted.

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Output Voltage	LTC6652A	–0.05		0.05	%
	LTC6652B	–0.1		0.1	%
Output Voltage Temperature Coefficient (Note 3)	LTC6652A	●	2	5	ppm/°C
	LTC6652BMS8	●	4	10	ppm/°C
	LTC6652BLS8	●	4	8	ppm/°C
Line Regulation	$V_{OUT} + 0.5\text{V} \leq V_{IN} \leq 13.2\text{V}$ , $\text{SHDN} = V_{IN}$	●	2	50 80	ppm/V ppm/V

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## ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at  $T_A = 25^\circ\text{C}$ ,  $V_{IN} = V_{OUT} + 0.5\text{V}$ , unless otherwise noted.

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Load Regulation (Note 4)	$I_{SOURCE} = 5\text{mA}$ , LTC6652-1.25, LTC6652-2.048, LTC6652-2.5, LTC6652-3, LTC6652-3.3, LTC6652-4.096, LTC6652-5	●	20	75 200	ppm/mA ppm/mA
	$I_{SINK} = 1\text{mA}$ , LTC6652-1.25, LTC6652-2.048	●	80	250 600	ppm/mA ppm/mA
	$I_{SINK} = 5\text{mA}$ , LTC6652-2.5, LTC6652-3, LTC6652-3.3, LTC6652-4.096, LTC6652-5	●	50	150 450	ppm/mA ppm/mA
Minimum Operating Voltage (Note 5)	$I_{SOURCE} = 5\text{mA}$ , $V_{OUT}$ Error $\leq 0.1\%$ LTC6652-1.25, LTC6652-2.048 LTC6652-2.5, LTC6652-3, LTC6652-3.3, LTC6652-4.096, LTC6652-5	● ●	2.7 $V_{OUT} + 0.3\text{V}$		V V
Output Short-Circuit Current	Short $V_{OUT}$ to GND		16		mA
	Short $V_{OUT}$ to $V_{IN}$		16		mA
Shutdown Pin ( $\overline{\text{SHDN}}$ )	Logic High Input Voltage	●	2		V
	Logic High Input Current	●	0.1	1	$\mu\text{A}$
	Logic Low Input Voltage	●		0.8	V
	Logic Low Input Current	●	0.1	1	$\mu\text{A}$
Supply Current	No Load	●	350		$\mu\text{A}$
		●		560	$\mu\text{A}$
Shutdown Current	$\overline{\text{SHDN}}$ Tied to GND	●	0.1	2	$\mu\text{A}$
Output Voltage Noise (Note 6)	0.1Hz $\leq f \leq 10\text{Hz}$ LTC6652-1.25 LTC6652-2.048, LTC6652-2.5, LTC6652-3 LTC6652-3.3 LTC6652-4.096 LTC6652-5 10Hz $\leq f \leq 1\text{kHz}$		2.4		ppm <sub>p-p</sub>
			2.1		ppm <sub>p-p</sub>
			2.2		ppm <sub>p-p</sub>
			2.3		ppm <sub>p-p</sub>
			2.8		ppm <sub>p-p</sub>
			3		ppm <sub>RMS</sub>
Turn-On Time	0.1% Settling, $C_{LOAD} = 0$		100		$\mu\text{s}$
Long-Term Drift of Output Voltage (Note 7)	LTC6652MS8		60		ppm/ $\sqrt{\text{kHr}}$
	LTC6652LS8		20		ppm/ $\sqrt{\text{kHr}}$
Hysteresis (Note 8)	$\Delta T = -40^\circ\text{C}$ to $125^\circ\text{C}$ , LTC6652MS8		80		ppm
	$\Delta T = -40^\circ\text{C}$ to $85^\circ\text{C}$ , LTC6652MS8		75		ppm
	$\Delta T = 0^\circ\text{C}$ to $70^\circ\text{C}$ , LTC6652MS8		45		ppm
	$\Delta T = -40^\circ\text{C}$ to $125^\circ\text{C}$ , LTC6652LS8		45		ppm
	$\Delta T = -40^\circ\text{C}$ to $85^\circ\text{C}$ , LTC6652LS8		25		ppm
	$\Delta T = 0^\circ\text{C}$ to $70^\circ\text{C}$ , LTC6652LS8		10		ppm

**Note 1:** Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

**Note 2:** If the parts are stored outside of the specified temperature range, the output may shift due to hysteresis.

**Note 3:** Temperature coefficient is measured by dividing the maximum change in output voltage by the specified temperature range.

**Note 4:** Load regulation is measured on a pulse basis from no load to the specified load current. Output changes due to die temperature change must be taken into account separately.

**Note 5:** Excludes load regulation errors.

**Note 6:** Peak-to-peak noise is measured with a 3-pole highpass at 0.1Hz and 4-pole lowpass filter at 10Hz. The unit is enclosed in a still-air environment to eliminate thermocouple effects on the leads. The test time is 10 seconds. RMS noise is measured on a spectrum analyzer in a shielded environment where the intrinsic noise of the instrument is removed to determine the actual noise of the device.

**Note 7:** Long-term stability typically has a logarithmic characteristic and therefore, changes after 1000 hours tend to be much smaller than before that time. Total drift in the second thousand hours is normally less than one third that of the first thousand hours with a continuing trend toward reduced drift with time. Long-term stability will also be affected by differential stresses between the IC and the board material created during board assembly.

**Note 8:** Hysteresis in output voltage is created by package stress that differs depending on whether the IC was previously at a higher or lower temperature. Output voltage is always measured at  $25^\circ\text{C}$ , but the IC is cycled to the hot or cold temperature limit before successive measurements. Hysteresis is roughly proportional to the square of the temperature change. For instruments that are stored at well controlled temperatures (within 20 or 30 degrees of operational temperature) it's usually not a dominant error source. Typical hysteresis is the worst-case of  $25^\circ\text{C}$  to cold to  $25^\circ\text{C}$  or  $25^\circ\text{C}$  to hot to  $25^\circ\text{C}$ , preconditioned by one thermal cycle.

**Note 9:** The stated temperature is typical for soldering of the leads during manual rework. For detailed IR reflow recommendations, refer to the Applications section.

**TYPICAL PERFORMANCE CHARACTERISTICS** Characteristic curves are similar for most LTC6652s. Curves from the LTC6652-1.25, LTC6652-2.5 and the LTC6652-5 represent the extremes and typical of the voltage options. Characteristic curves for other output voltages fall between these curves and can be estimated based on their output.

**1.25V Output Voltage Temperature Drift**



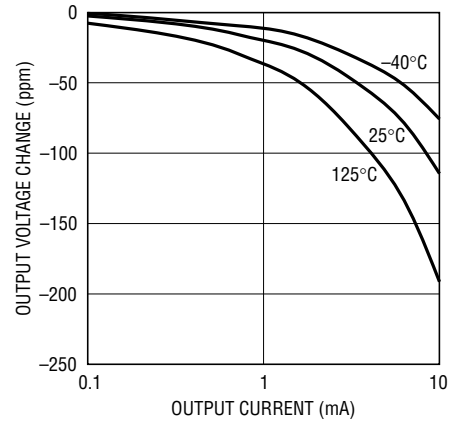
6652 G17

**1.25V Line Regulation**



6652 G18

**1.25V Load Regulation (Sourcing)**



6652 G19

**1.25V Load Regulation (Sinking)**



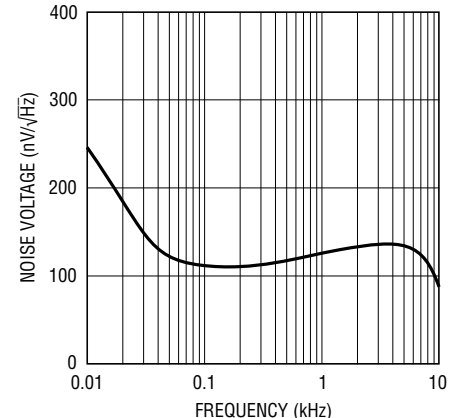
6652 G20

**1.25V Low Frequency 0.1Hz to 10Hz Transient Noise**



6652 G21

**1.25V Output Voltage Noise Spectrum**



6652 G22

**1.25 Sinking Current Without Output Capacitor**



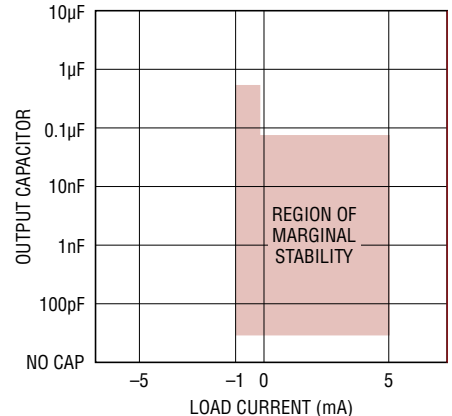
6652 G23

**1.25 Sinking Current with Output Capacitor**



6652 G24

**1.25V Stability with Output Capacitance**



6652 G16

## TYPICAL PERFORMANCE CHARACTERISTICS

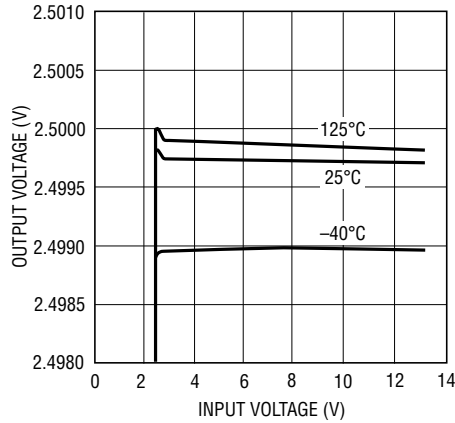
Characteristic curves are similar for most LTC6652s. Curves from the LTC6652-1.25, LTC6652-2.5 and the LTC6652-5 represent the extremes and typical of the voltage options. Characteristic curves for other output voltages fall between these curves and can be estimated based on their output.

**2.5V Output Voltage Temperature Drift**



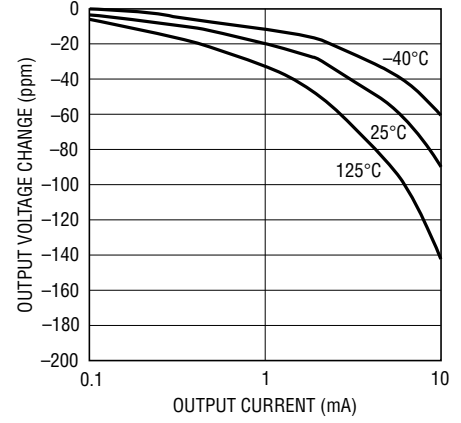
6652 G01

**2.5V Line Regulation**



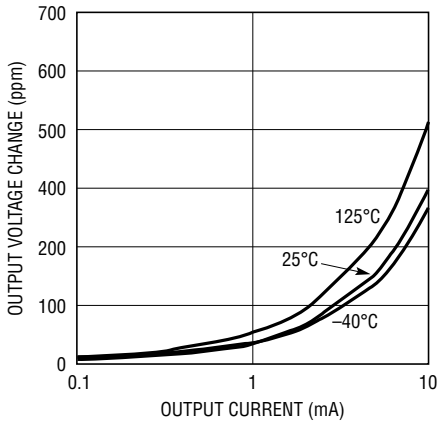
6652 G02

**2.5V Load Regulation (Sourcing)**



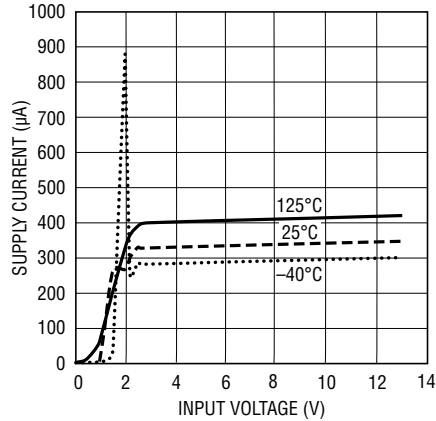
6652 G03

**2.5V Load Regulation (Sinking)**



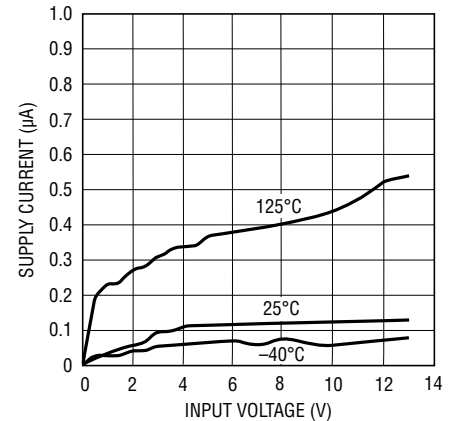
6652 G04

**2.5V Supply Current vs Input Voltage**



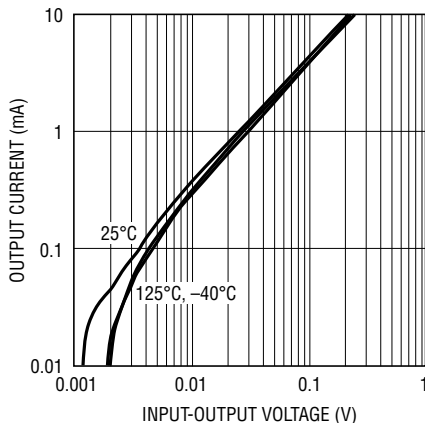
6652 G05

**2.5V Shutdown Current vs Input Voltage**



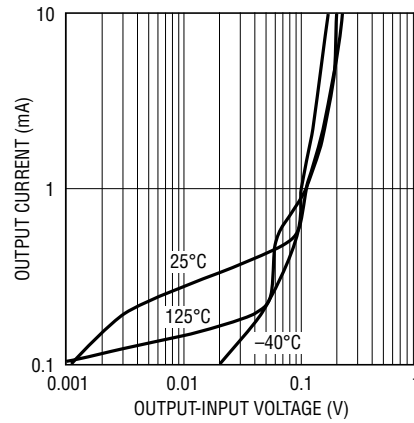
6652 G06

**2.5V Minimum  $V_{IN}-V_{OUT}$  Differential (Sourcing)**



6652 G09

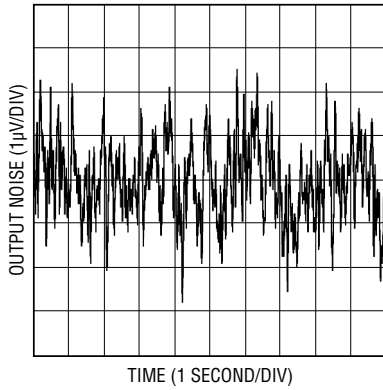
**2.5V Minimum  $V_{OUT}-V_{IN}$  Differential (Sinking)**



6652 G10

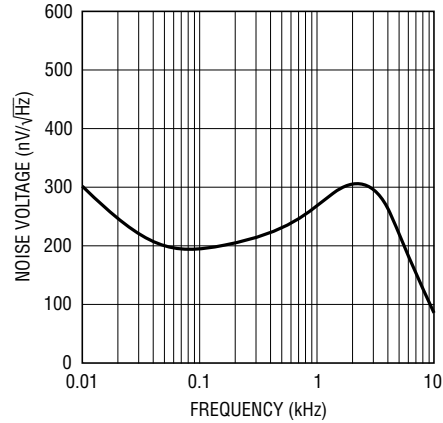
**TYPICAL PERFORMANCE CHARACTERISTICS** Characteristic curves are similar for most LTC6652s. Curves from the LTC6652-1.25, LTC6652-2.5 and the LTC6652-5 represent the extremes and typical of the voltage options. Characteristic curves for other output voltages fall between these curves and can be estimated based on their output.

**2.5V Low Frequency 0.1Hz to 10Hz Transient Noise**



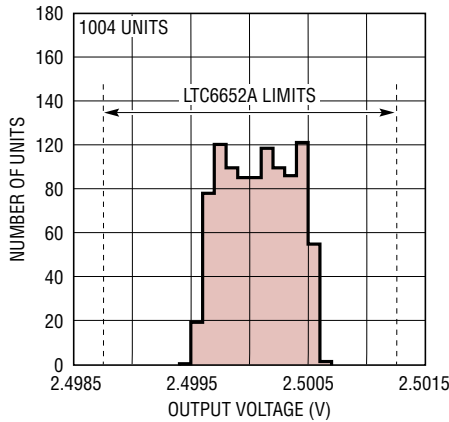
6652 G11

**2.5V Output Voltage Noise Spectrum**



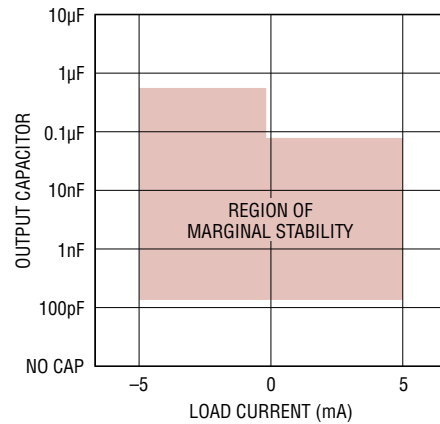
6652 G12

**Typical  $V_{OUT}$  Distribution for LTC6652-2.5**



6652 G15

**Stability with Output Capacitance (LTC6652-2.5, LTC6652-3, LTC6652-3.3, LTC6652-4.096, LTC6652-5)**



6652 G14

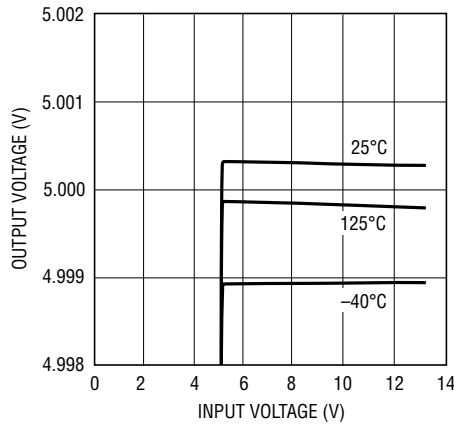
## TYPICAL PERFORMANCE CHARACTERISTICS

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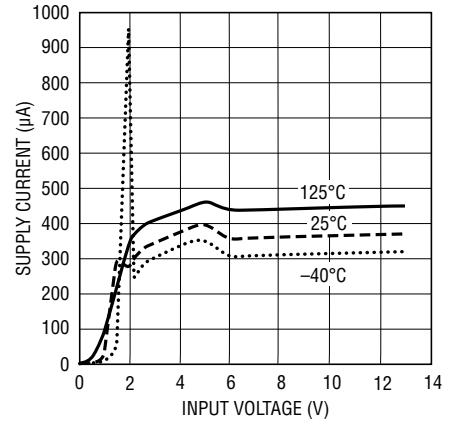
**5V Output Voltage Temperature Drift**



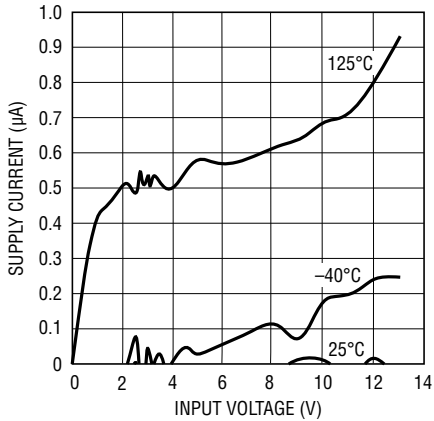
**5V Line Regulation**



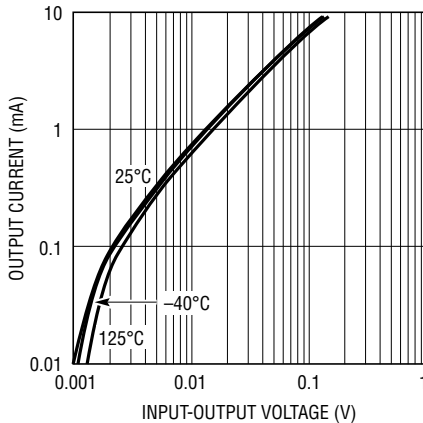
**5V Supply Current vs Input Voltage**



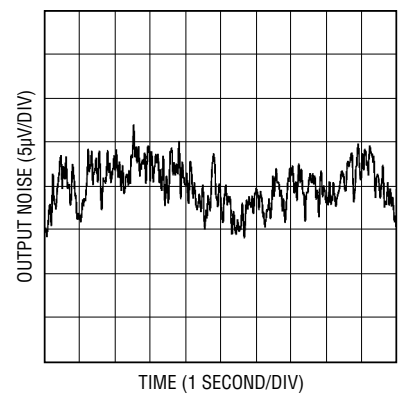
**5V Shutdown Current vs Input Voltage**



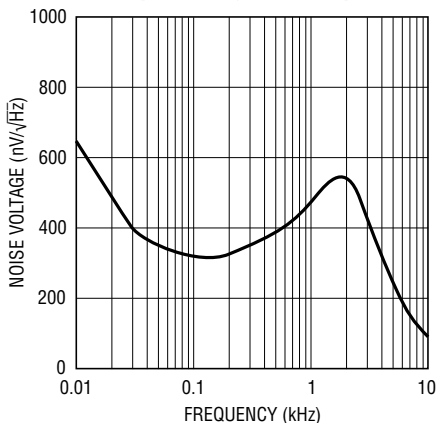
**5V Minimum  $V_{IN}$  to  $V_{OUT}$  Differential (Sourcing)**



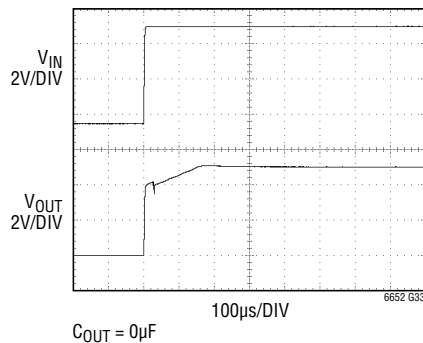
**5V Low Frequency 0.1Hz to 10Hz Transient Noise**



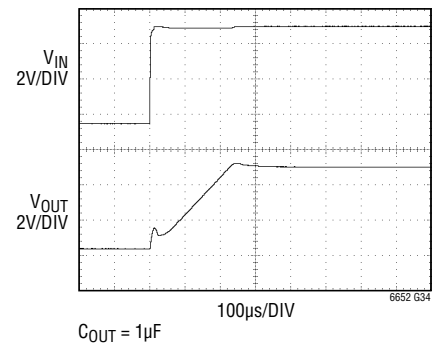
**5V Output Voltage Noise Spectrum**



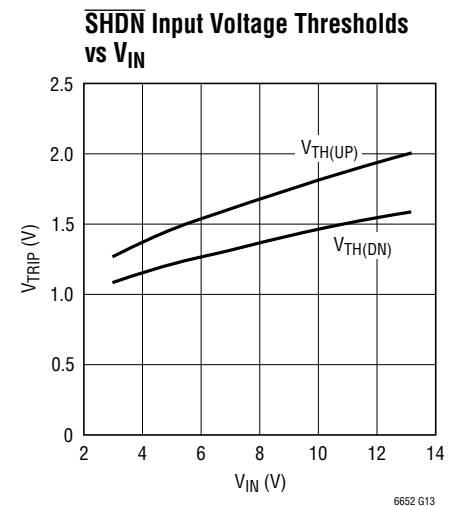
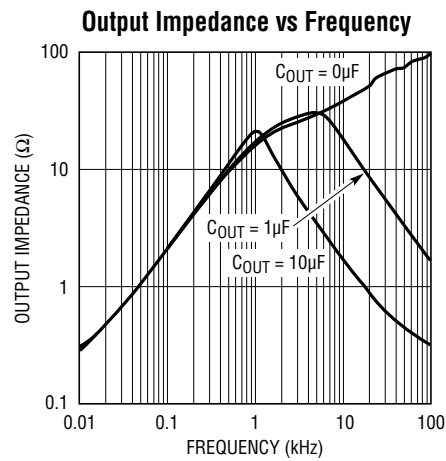
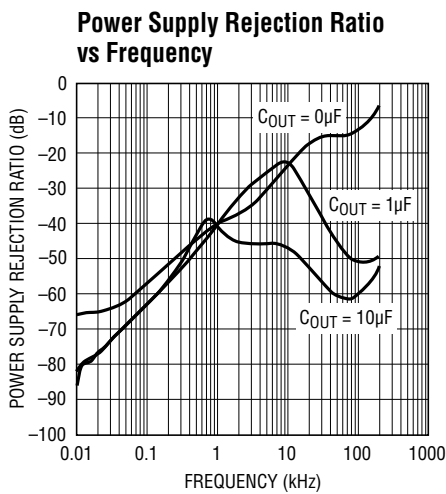
**5V Start-Up Response Without Output Capacitor**



**5V Start-Up Response with Output Capacitor**



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## PIN FUNCTIONS

**DNC (Pin 1):** Do Not Connect.

**$V_{IN}$  (Pin 2):** Power Supply. The minimum supply input is  $V_{OUT} + 300\text{mV}$  or  $2.7\text{V}$ ; whichever is higher. The maximum supply is  $13.2\text{V}$ . Bypassing  $V_{IN}$  with a  $0.1\mu\text{F}$  capacitor to GND will improve PSRR.

**$\overline{SHDN}$  (Pin 3):** Shutdown Input. This active low input powers down the device to  $<2\mu\text{A}$ . For normal operation tie this pin to  $V_{IN}$ .

**GND (Pin 4):** Device Ground.

**$V_{OUT}$  (Pin 6):** Output Voltage. An output capacitor is not required. For some applications, a capacitor between  $0.1\mu\text{F}$  to  $10\mu\text{F}$  can be beneficial. See the graphs in the Typical Performance Characteristics section for further details.

**GND (Pins 5,7,8):** Internal Function. Ground these pins.

## BLOCK DIAGRAM



## APPLICATIONS INFORMATION

### Bypass and Load Capacitors

The LTC6652 voltage references do not require an input capacitor, but a 0.1  $\mu\text{F}$  capacitor located close to the part improves power supply rejection.

The LTC6652 voltage references are stable with or without a capacitive load. For applications where an output capacitor is beneficial, a value of 0.1  $\mu\text{F}$  to 10  $\mu\text{F}$  is recommended depending on load conditions. The Typical Performance Characteristics section includes a plot illustrating a region of marginal stability. Either no or low value capacitors for any load current are acceptable. For loads that sink current or light loads that source current, a 0.1  $\mu\text{F}$  to 10  $\mu\text{F}$  capacitor has stable operation. For heavier loads that source current a 0.5  $\mu\text{F}$  to 10  $\mu\text{F}$  capacitor range is recommended.

The transient response for a 0.5V step on  $V_{\text{IN}}$  with and without an output capacitor is shown in Figures 2 and 3, respectively.

The LTC6652 references with an output of 2.5V and above are guaranteed to source and sink 5mA. The 1.25V and 2.048V versions are guaranteed to source 5mA and sink 1mA. The test circuit for transient load step response is shown in Figure 1. Figures 4 and 5 show a 5mA source and sink load step response without a load capacitor, respectively.

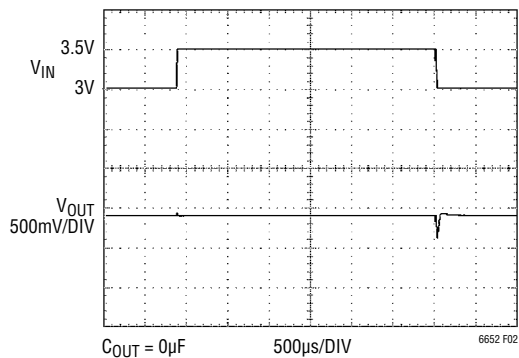
### Start-Up

The start-up characteristic of the LTC6652 is shown in Figures 8 and 9. Note that the turn-on time is affected by the value of the output capacitor.

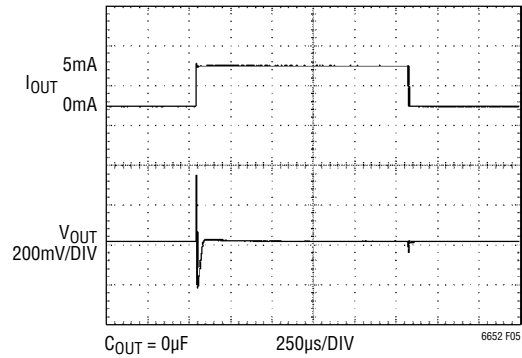


Figure 1. Transient Load Test Circuit

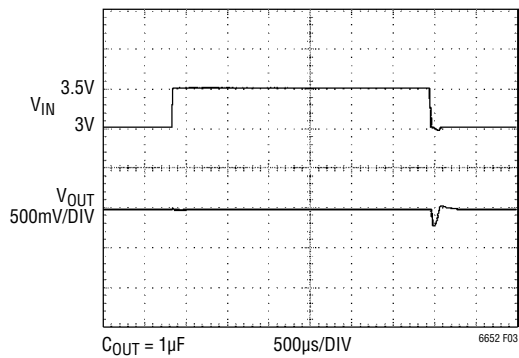
# APPLICATIONS INFORMATION



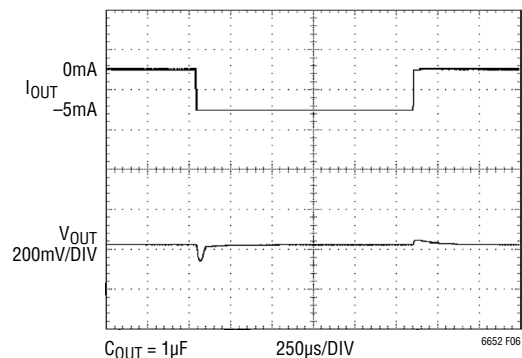
**Figure 2. Transient Response Without Output Capacitor**



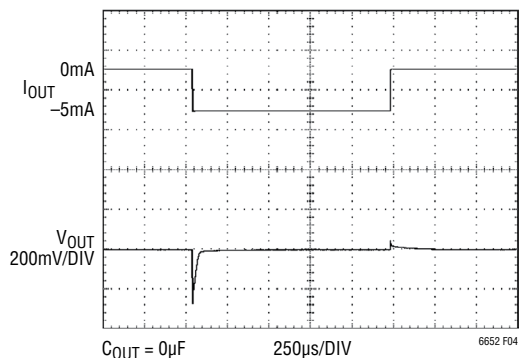
**Figure 5. LTC6652-2.5 Sinking Current Without Output Capacitor**



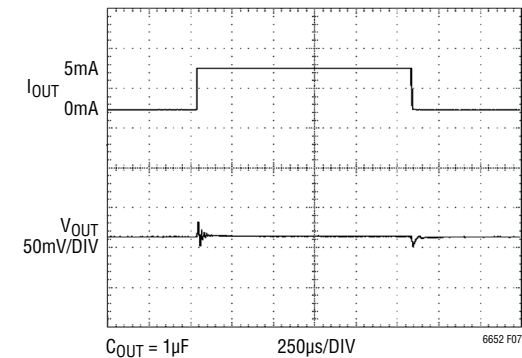
**Figure 3. Transient Response with 1µF Output Capacitor**



**Figure 6. LTC6652-2.5 Sourcing Current with Output Capacitor**



**Figure 4. LTC6652-2.5 Sourcing Current Without Output Capacitor**



**Figure 7. LTC6652-2.5 Sinking Current with Output Capacitor**

## APPLICATIONS INFORMATION



**Figure 8. Start-Up Response without Output Capacitor**

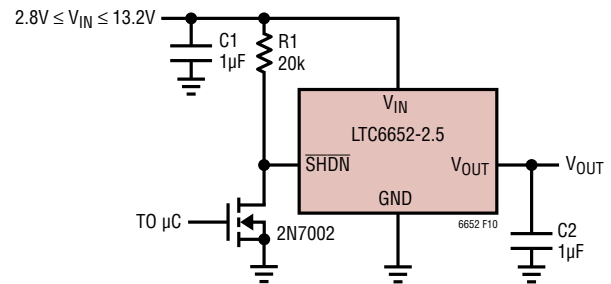


**Figure 9. Start-Up Response with 1µF Output Capacitor**

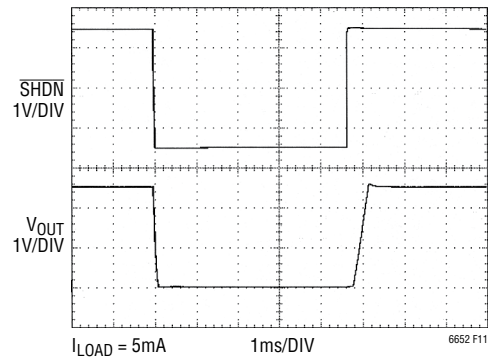
In Figure 8, ripple momentarily appears just after the leading edge of powering on. This brief one time event is caused by calibration circuitry during initialization. When an output capacitor is used, the ripple is virtually undetectable as shown in Figure 9.

### Shutdown Mode

Shutdown mode is enabled by tying  $\overline{\text{SHDN}}$  low which places the part in a low power state (i.e.,  $<2\mu\text{A}$ ). In shutdown mode, the output pin takes the value  $20\text{k} \cdot (\text{rated output voltage})$ . For example, an LTC6652-2.5 will have



**Figure 10. Open-Drain Shutdown Circuit**



**Figure 11. Shutdown Response with 5mA Load**

an output impedance of  $20\text{k} \cdot 2.5 = 50\text{k}\Omega$ . For normal operation,  $\overline{\text{SHDN}}$  should be greater than or equal to 2.0V. For use with a microcontroller, use a pull-up resistor to  $V_{\text{IN}}$  and an open-drain output driver as shown in Figure 10. The LTC6652's response into and out of shutdown mode is shown in Figure 11.

The trip thresholds on  $\overline{\text{SHDN}}$  have some dependence on the voltage applied to  $V_{\text{IN}}$  as shown in the Typical Performance Characteristics section. Be careful to avoid leaving  $\overline{\text{SHDN}}$  at a voltage between the thresholds as this will likely cause an increase in supply current due to shoot-through current.

## APPLICATIONS INFORMATION

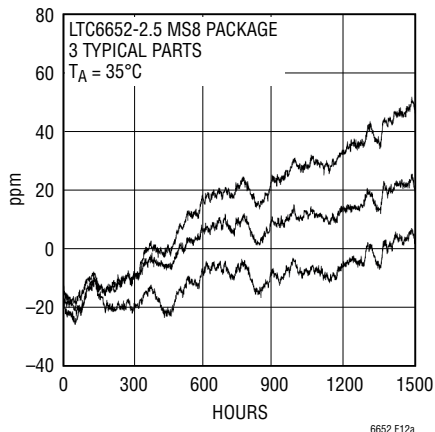


Figure 12a. MS8 Long-Term Drift

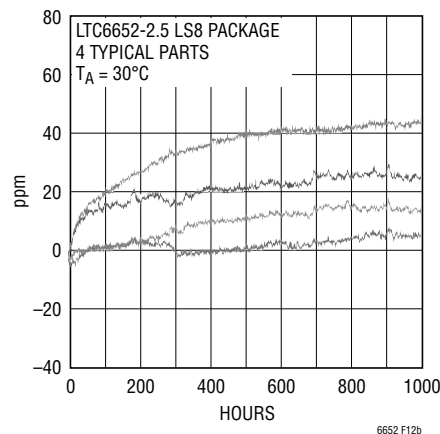


Figure 12b. LS8 Long-Term Drift



Figure 13a. MS8 Hysteresis Plot  
-40°C to 125°C



Figure 13b. LS8 Hysteresis Plot  
-40°C to 125°C

### Long-Term Drift

**Long-term drift cannot be extrapolated from accelerated high temperature testing. This erroneous technique gives drift numbers that are wildly optimistic. The only way long-term drift can be determined is to measure it over the time interval of interest.** The LTC6652 long-term drift data was collected on more than 100 parts that were soldered into PC boards similar to a “real world” application. The boards were then placed into a constant temperature oven with  $T_A = 35^\circ\text{C}$ , their outputs were scanned regularly and measured with an 8.5 digit DVM. Long-term drift is shown below in Figure 12.

### Hysteresis

The hysteresis data shown in Figure 13 represents the worst-case data collected on parts from  $-40^\circ\text{C}$  to  $125^\circ\text{C}$ . The output is capable of dissipating relatively high power, i.e., for the LTC6652-2.5,  $P_D = 10.7\text{V} \cdot 5.5\text{mA} = 58.85\text{mW}$ . The thermal resistance of the MS8 package is  $200^\circ\text{C/W}$  and this dissipation causes a  $11.8^\circ\text{C}$  internal rise. This could increase the junction temperature above  $125^\circ\text{C}$  and may cause the output to shift due to thermal hysteresis.

## APPLICATIONS INFORMATION

### PC Board Layout

The mechanical stress of soldering a surface mount voltage reference to a PC board can cause the output voltage to shift and temperature coefficient to change. These two changes are not correlated. For example, the voltage may shift, but the temperature coefficient may not.

To reduce the effects of stress-related shifts, mount the reference near the short edge of the PC board or in a corner. In addition, slots can be cut into the board on two sides of the device.

The capacitors should be mounted close to the package. The GND and  $V_{OUT}$  traces should be as short as possible to minimize  $I \cdot R$  drops. Excessive trace resistance directly impacts load regulation.

### IR Reflow Shift

The different expansion and contraction rates of the materials that make up the lead-free LTC6652 package cause the output voltage to shift after undergoing IR reflow. Lead-free reflow profiles reach over  $250^{\circ}\text{C}$ , considerably more than their leaded counterparts. The lead-free IR reflow profile used to experimentally measure output voltage shift in the LTC6652-2.5 is shown in Figure 14. Similar results can be

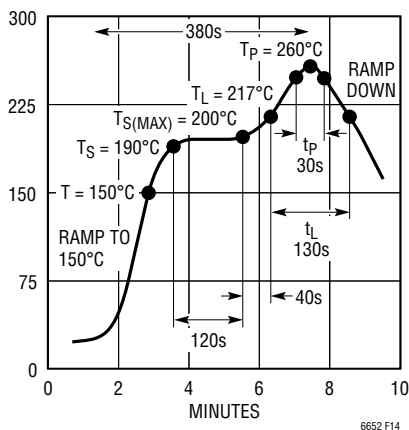


Figure 14. Lead-Free Reflow Profile

expected using a convection reflow oven. In our experiment, the serialized parts were run through the reflow process twice. The results indicate that the standard deviation of the output voltage increases with a slight positive mean shift of 0.003% as shown in Figure 15. While there can be up to 0.016% of output voltage shift, the overall drift of the LTC6652 after IR reflow does not vary significantly.

### Power Dissipation

Power dissipation in the LTC6652 is dependent on  $V_{IN}$ , load current, and package. The LTC6652 package has a thermal resistance, or  $\theta_{JA}$ , of  $200^{\circ}\text{C}/\text{W}$ . A curve that illustrates allowed power dissipation vs temperature for this package is shown in Figure 16.

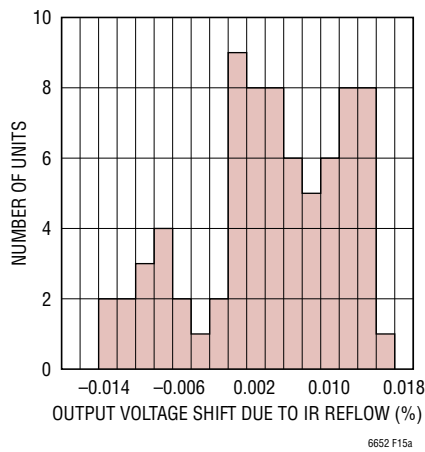
The power dissipation of the LTC6652-2.5V as a function of input voltage is shown in Figure 17. The top curve shows power dissipation with a 5mA load and the bottom curve shows power dissipation with no load.

When operated within its specified limits of  $V_{IN} = 13.2\text{V}$  and sourcing 5mA, the LTC6652-2.5 consumes just under 60mW at room temperature. At  $125^{\circ}\text{C}$  the quiescent current will be slightly higher and the power consumption increases to just over 60mW. The power-derating curve in Figure 16 shows the LTC6652-2.5 can safely dissipate 125mW at  $125^{\circ}\text{C}$  about half the maximum power consumption of the package.

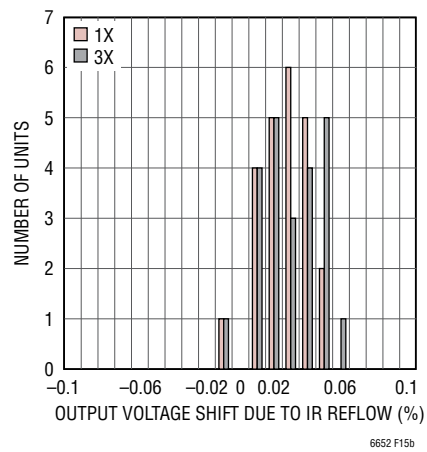
### Humidity Sensitivity

Plastic mould compounds absorb water. With changes in relative humidity, plastic packaging materials change the amount of pressure they apply to the die inside, which can cause slight changes in the output of a voltage reference, usually on the order of 100ppm. The LS8 package is hermetic, so it is not affected by humidity, and is therefore more stable in environments where humidity may be a concern.

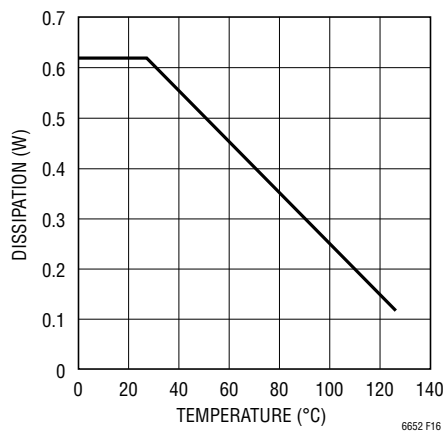
# APPLICATIONS INFORMATION



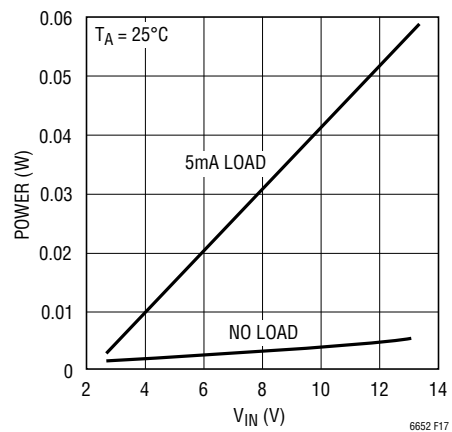
**Figure 15a. MS8 Output Voltage Shift Due to IR Reflow**



**Figure 15b. LS8 Output Voltage Shift Due to IR Reflow**



**Figure 16. Maximum Recommended Dissipation for LTC6652**



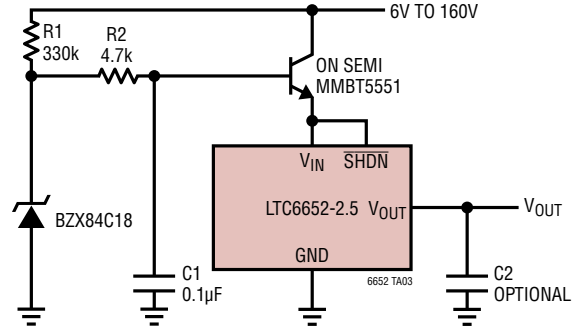
**Figure 17. Typical Power Dissipation of the LTC6652**

## TYPICAL APPLICATIONS

### Extended Supply Range Reference



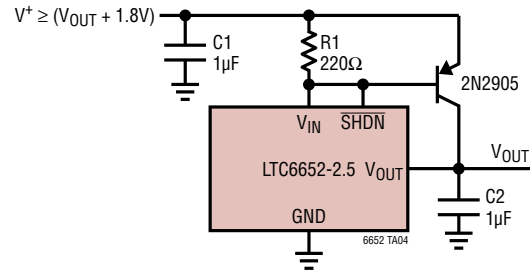
### Extended Supply Range Reference



### Negative Rail Circuit



### Boosted Output Current



## PACKAGE DESCRIPTION

Please refer to <http://www.linear.com/product/LTC6652#packaging> for the most recent package drawings.

### MS8 Package 8-Lead Plastic MSOP

(Reference LTC DWG # 05-08-1660 Rev G)



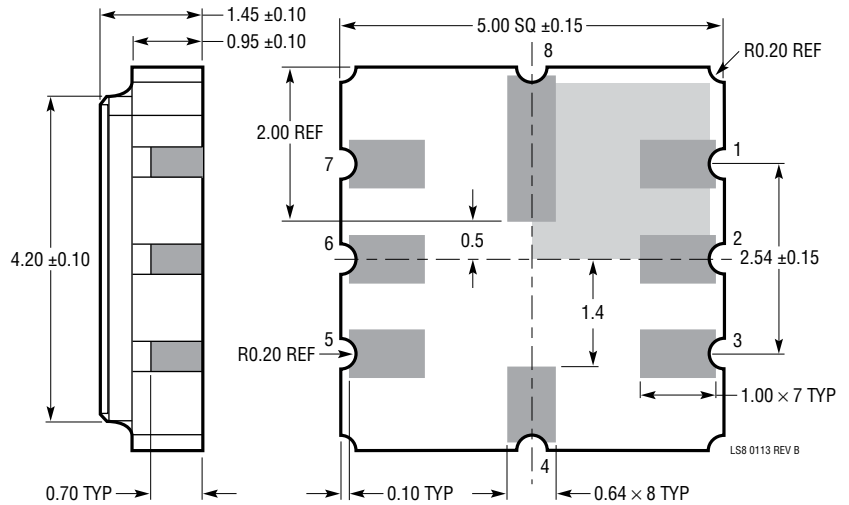
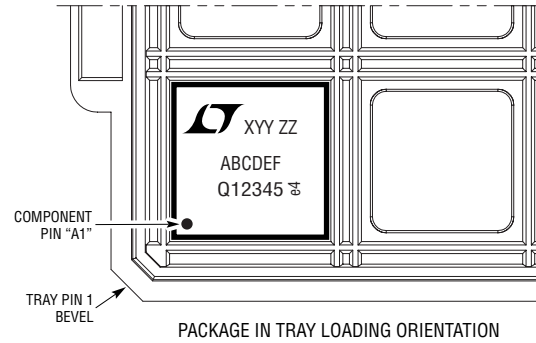
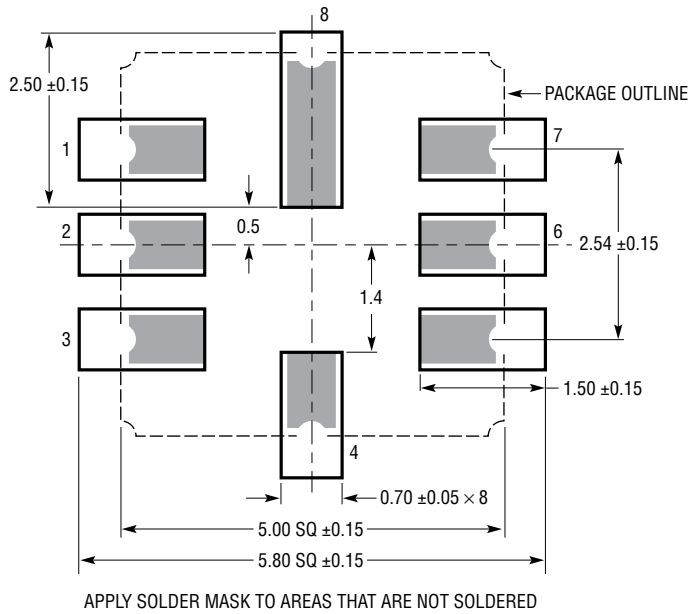
#### NOTE:

1. DIMENSIONS IN MILLIMETER/(INCH)
2. DRAWING NOT TO SCALE
3. DIMENSION DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS.  
MOLD FLASH, PROTRUSIONS OR GATE BURRS SHALL NOT EXCEED  $0.152\text{mm}$  ( $.006''$ ) PER SIDE
4. DIMENSION DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSIONS.  
INTERLEAD FLASH OR PROTRUSIONS SHALL NOT EXCEED  $0.152\text{mm}$  ( $.006''$ ) PER SIDE
5. LEAD COPLANARITY (BOTTOM OF LEADS AFTER FORMING) SHALL BE  $0.102\text{mm}$  ( $.004''$ ) MAX

## PACKAGE DESCRIPTION

Please refer to <http://www.linear.com/product/LTC6652#packaging> for the most recent package drawings.

### LS8 Package 8-Pin Leadless Chip Carrier (5mm × 5mm) (Reference LTC DWG # 05-08-1852 Rev B)



- NOTE:
1. ALL DIMENSIONS ARE IN MILLIMETERS
  2. DRAWING NOT TO SCALE
  3. DIMENSIONS PACKAGE DO NOT INCLUDE PLATING BURRS  
PLATING BURRS, IF PRESENT, SHALL NOT EXCEED 0.30mm ON ANY SIDE
  4. PLATING—ELECTO NICKEL MIN 1.25UM, ELECTRO GOLD MIN 0.30UM
  5. SHADED AREA IS ONLY A REFERENCE FOR PIN 1 LOCATION ON THE TOP AND BOTTOM OF PACKAGE


**REVISION HISTORY** (Revision history begins at Rev C)

REV	DATE	DESCRIPTION	PAGE NUMBER
C	11/09	Change to Typical Performance Characteristics. Change to Typical Application.	6 14
D	8/12	Addition of 5mm × 5mm Hermetic LS8 Package. Update to Electrical Characteristics to Include LS8 Package. Addition of Long Term Drift, Hysteresis, IR Drift Plots for LS8 Package. Addition of Humidity Sensitivity Information.	1, 2, 3, 12, 18 4 13, 15 14
E	1/13	Correction to pin labeling of LS8 Package	2
F	7/15	Order Information updated to include 4.096V and 5V options in LS8 package. MS8 and LS8 package descriptions updated.	3 17, 18
G	10/15	Correction to the Electrical Characteristics Table: Output Voltage Temperature Coefficient for LTC6652BMS8 specification applies over the full operating temperature range.	3



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