THE DATASHEET OF

LTC6601CUF-2#TRPBF

www.win-source.net 0086-755-83957316

Low Power, Low Distortion, 5MHz to 27MHz, Pin Configurable Filter/ADC Driver

FEATURES

- **Pin Configurable Gain and Filter Response Up to 27MHz**
- **Low Power: 16mA at 3V**
- **Low Distortion ($2V_{P-P}$)**
  - **1MHz: –96dBc 2nd, –112dBc 3rd**
  - **10MHz: –65dBc 2nd, –78dBc 3rd**
- **Few External Components Required**
- **Resistors Trimmed to 0.5% Accuracy Typical**
- **Capacitors Trimmed to 0.5% Accuracy Typical**
- Adjustable Output Common Mode Voltage
- Rail-to-Rail Output Swing
- Power Configurability and Low Power Shutdown
- Tiny 0.75mm 20-Lead (4mm × 4mm) QFN Package

APPLICATIONS

- Differential A/D Converter Driver
- Antialiasing/Reconstruction Filter
- Single-Ended to Differential Conversion/Amplification
- Low Voltage, Low Noise, Differential Signal Processing
- Common Mode Voltage Translation
- Portable Instrumentation

DESCRIPTION

The LTC®6601-2 is a low power, low distortion, very easy-to-use fully differential 2nd order active broadband RC filter and driver. On-chip resistors, capacitors, and amplifier bandwidth are trimmed to provide consistent and repeatable filter characteristics.

The filter characteristics are pin-strap configurable. Cutoff frequencies range from 5MHz to 27MHz. Gain is pin-strap programmable between –17dB and +17dB.

A three-state BIAS pin is provided to adjust amplifier power consumption. Select between low power (50% power reduction), high performance and standby modes with the BIAS pin.

The LTC6601 family comes in two options which trade off distortion and noise. The LTC6601-2 offers the lowest distortion at high frequencies. The LTC6601-1 is configured for lowest noise. Both are available in pin-compatible packages.

The LTC6601-2 is available in a compact 4mm × 4mm 20-pin leadless QFN package.

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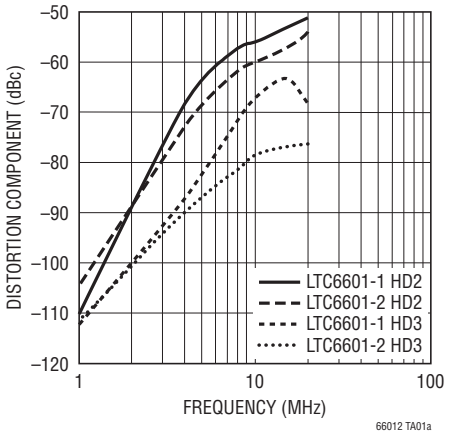
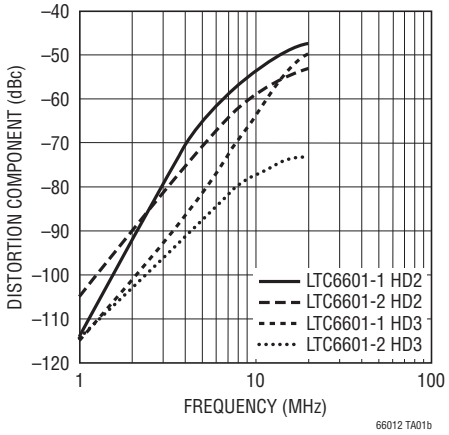
TYPICAL APPLICATION

Distortion Comparison Between LTC6601-1 and LTC6602-2

15MHz Filter, Single-Ended Input, Low Power Mode



25MHz Filter, Single-Ended Input, Low Power Mode

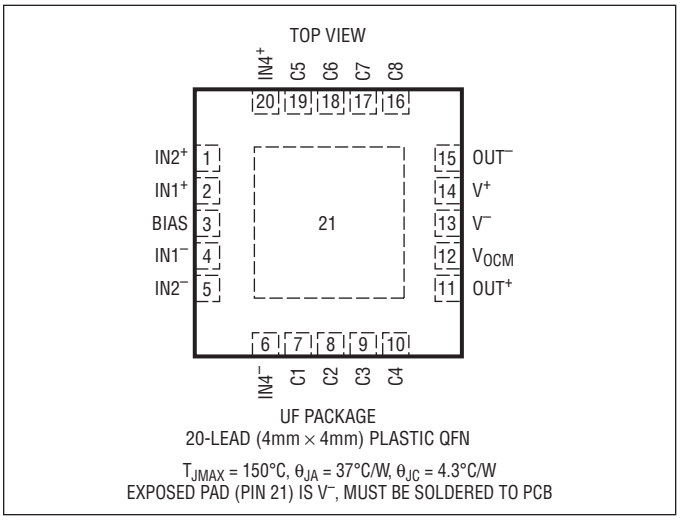


ABSOLUTE MAXIMUM RATINGS

(Note 1)

Total Supply Voltage (V^+ to V^-) 5.5V
Input Voltage (Any Pin) (Note 2)..V^+ + 0.3V to V^- –0.3V
Input Current (V_{OCM}, BIAS).....±10mA
Input Current (Pins 1, 5) (Note 2).....±20mA
Input Current (Pins 2, 4) (Note 2).....±30mA
Input Current (Pins 6, 20) (Note 2).....±15mA
Input Current (Pins 7, 8, 9, 10, 16, 17, 18, 19)
(Note 2).....±10mA
Output Short-Circuit Duration (Note 3) ..... Indefinite
Operating Temperature Range (Note 4)....–40°C to 85°C
Specified Temperature Range (Note 5) ....–40°C to 85°C
Junction Temperature ..... 150°C
Storage Temperature Range.....–65°C to 150°C

PIN CONFIGURATION



UF PACKAGE
20-LEAD (4mm × 4mm) PLASTIC QFN

T_{JMAX} = 150°C, θ_{JA} = 37°C/W, θ_{JC} = 4.3°C/W
EXPOSED PAD (PIN 21) IS V^-, MUST BE SOLDERED TO PCB

ORDER INFORMATION

LEAD FREE FINISH	TAPE AND REEL	PART MARKING*	PACKAGE DESCRIPTION	TEMPERATURE RANGE
LTC6601CUF-2#PBF	LTC6601CUF-2#TRPBF	66012	20-Lead (4mm × 4mm) Plastic QFN	0°C to 70°C
LTC6601IUF-2#PBF	LTC6601IUF-2#TRPBF	66012	20-Lead (4mm × 4mm) Plastic QFN	–40°C to 85°C

Consult LTC Marketing for parts specified with wider operating temperature ranges. *The temperature grade is identified by a label on the shipping container.

For more information on lead free part marking, go to: http://www.linear.com/leadfree/
For more information on tape and reel specifications, go to: http://www.linear.com/tapeandreel/

DC ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. V^+ = 3V, V^- = 0V, V_{INCM} = V_{OCM} = mid-supply, BIAS tied to V^+ or floating, I_{LOAD} = 0, R_{BAL} = 100k. The filter is configured for a gain of 1 unless otherwise noted. V_S is defined as (V^+ – V^-). V_{OUTCM} is defined as (V_{OUT}^+ + V_{OUT}^-)/2. V_{INCM} is defined as (V_{INP} + V_{INM})/2. $V_{OUTDIFF}$ is defined as (V_{OUT}^+ – V_{OUT}^-). V_{INDIFF} is defined as (V_{INP} – V_{INM}). See Figure 1.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
V_{OSDIFF} (Note 6)	Amplifier Differential Offset Voltage (Input Referred)	V_S = 2.7V to 5.25V, BIAS = Floating BIAS = V^+	● ●		±0.25 ±0.25	±2 ±1.25	mV mV
$\Delta V_{OSDIFF}/\Delta T$ (Note 6)	Ampifier Differential Offset Voltage Drift (Input Referred)	V_S = 2.7V to 5.25V			1		µV/°C
R_{IN} (Note 14)	Input Resistance, BIAS = V^+ Single Ended Input Resistance, Pin 2 or Pin 4 Differential Input Resistance	 V_S = 3V V_S = 3V			 133 200		 Ω Ω

DC ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. V^+ = 3V, V^- = 0V, V_{INCM} = V_{OCM} = mid-supply, BIAS tied to V^+ or floating, I_{LOAD} = 0, R_{BAL} = 100k. The filter is configured for a gain of 1 unless otherwise noted. V_S is defined as ($V^+ – V^-$). V_{OUTCM} is defined as ($V_{OUT}^+ + V_{OUT}^-$)/2. V_{INCM} is defined as ($V_{INP} + V_{INM}$)/2. $V_{OUTDIFF}$ is defined as ($V_{OUT}^+ – V_{OUT}^-$). V_{INDIFF} is defined as ($V_{INP} – V_{INM}$). See Figure 1.

SYMBOL	PARAMETER	CONDITIONS			MIN	TYP	MAX	UNITS
ΔR_{IN} (Note 14)	Input Resistance Match, BIAS = V^+ Single Ended Input Resistance, Pin 2 or Pin 4	V_S = 3V		●		±0.25		Ω
I_B (Note 7)	Internal Amplifier Input Bias	V_S = 2.7V to 5V	BIAS = Floating BIAS = V^+	● ●	–25 –50	–12.5 –25	0 0	µA µA
I_{OS} (Note 7)	Internal Amplifier Input Offset	V_S = 2.7V to 5V	BIAS = Floating BIAS = V^+	● ●		±1 ±1	±5 ±10	µA µA
V_{INCM} (Note 8)	Input Signal Common Mode Range ($V_{INP} + V_{INM}$)/2 BIAS = V^+, V_{OCM} = 2.5V BIAS = V^+, V_{OCM} = 1.5V	 V_S = 5V V_S = 3V		 ● ●	 0 0	 	 4.7 1.7	 V V
	BIAS Pin Floating, V_{OCM} = 2.5V BIAS Pin Floating, V_{OCM} = 1.5V	V_S = 5V V_S = 3V		● ●	0 0		4.8 1.8	V V
CMRRI (Notes 9, 14)	Input Common Mode Rejection Ratio (Amplifier Input Referred) $\Delta V_{INCM}/\Delta V_{OSDIFF}$ ΔV_{INCM} = 2.5V	 V_S = 5V		 	 	 74	 	 dB
CMRRO (Notes 9, 14)	Output Common Mode Rejection Ratio (Amplifier Input Referred) $\Delta V_{OCM}/\Delta V_{OSDIFF}$ ΔV_{OCM} = 1V	 V_S = 5V		 	 	 70	 	 dB
PSRR (Note 10)	Power Supply Rejection Ratio (Amplifier Input Referred) $\Delta V_S/\Delta V_{OSDIFF}$ BIAS Pin Floating BIAS = V^+	 V_S = 2.7V to 5V V_S = 2.7V to 5V		 ● ●	 58 58	 94 81	 	 dB dB
PSRRCM (Note 10)	Common Mode Power Supply Rejection Ratio ($\Delta V_S/\Delta V_{OSCM}$)	V_S = 2.7V to 5V		●	40	51		dB
g_{cm}	Common Mode Gain ($\Delta V_{OUTCM}/\Delta V_{OCM}$) ΔV_{OCM} = 2V	V_S = 5V				1		V/V
	Common Mode Gain Error = 100 • (g_{cm} – 1) ΔV_{OCM} = 2V	V_S = 5V		●		±0.3	±1.0	%
BAL	Output Balance ($\Delta V_{OUTCM}/\Delta V_{OUTDIFF}$) Single-Ended Input Differential Input	$\Delta V_{OUTDIFF}$ = 2V V_S = 5V V_S = 5V		 ● ●	 	 –58 –62	 –40 –40	 dB dB
V_{OSCM}	Common Mode Offset Voltage ($V_{OUTCM} – V_{OCM}$)	V_S = 2.7V to 5V V_S = 2.7V to 5V	BIAS = Floating BIAS = V^+	● ●		±15 ±15	±30 ±30	mV mV
$\Delta V_{OSCM}/\Delta T$	Common Mode Offset Voltage Drift ($V_{OUTCM} – V_{OCM}$)	V_S = 2.7V to 5V V_S = 2.7V to 5V	BIAS = Floating BIAS = V^+	● ●		20 20		µV/°C µV/°C
V_{OUTCMR} (Note 8)	Output Signal Common Mode Range (Voltage Range for the V_{OCM} Pin)	V_S = 3V V_S = 5V V_S = 3V V_S = 5V	BIAS Pin Floating BIAS Pin Floating BIAS = V^+ BIAS = V^+	● ● ● ●	1.1 1.1 1.1 1.1	 	1.8 4 1.7 4	V V V V
R_{INVOCM}	Input Resistance, V_{OCM} Pin	V_S = 3V		●	5	7	9	kΩ
V_{MID}	Voltage at the V_{OCM} PIn	V_S = 3V		●	1.475	1.5	1.525	V

DC ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. V^+ = 3V, V^- = 0V, V_{INCM} = V_{OCM} = mid-supply, BIAS tied to V^+ or floating, I_{LOAD} = 0, R_{BAL} = 100k. The filter is configured for a gain of 1 unless otherwise noted. V_S is defined as ($V^+ - V^-$). V_{OUTCM} is defined as ($V_{OUT}^+ + V_{OUT}^-$)/2. V_{INCM} is defined as ($V_{INP} + V_{INM}$)/2. $V_{OUTDIFF}$ is defined as ($V_{OUT}^+ - V_{OUT}^-$). V_{INDIFF} is defined as ($V_{INP} - V_{INM}$). See Figure 1.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
V_{OUT}	Output Voltage, High, Either Output Pin (Note 11)	V_S = 3V, I_L = 0mA, BIAS Pin Floating	●		240	450	mV
		V_S = 3V, I_L = –5mA, BIAS Pin Floating	●		290	525	mV
		V_S = 3V, I_L = –20mA, BIAS Pin Floating	●		470	850	mV
		V_S = 5V, I_L = 0mA, BIAS Pin Floating	●		370	675	mV
		V_S = 5V, I_L = –5mA, BIAS Pin Floating	●		430	775	mV
		V_S = 5V, I_L = –20mA, BIAS Pin Floating	●		650	1100	mV
		V_S = 3V, I_L = 0mA BIAS = V^+	●		245	450	mV
		V_S = 3V, I_L = –5mA BIAS = V^+	●		285	525	mV
		V_S = 3V, I_L = –20mA BIAS = V^+	●		415	750	mV
		V_S = 5V, I_L = 0mA BIAS = V^+	●		350	625	mV
		V_S = 5V, I_L = –5mA BIAS = V^+	●		390	700	mV
		V_S = 5V, I_L = –20mA BIAS = V^+	●		550	1000	mV
	Output Voltage, Low, Either Output Pin (Note 11)	V_S = 3V, I_L = 0mA, BIAS Pin Floating	●		110	200	mV
		V_S = 3V, I_L = 5mA, BIAS Pin Floating	●		120	225	mV
		V_S = 3V, I_L = 20mA, BIAS Pin Floating	●		170	300	mV
		V_S = 5V, I_L = 0mA, BIAS Pin Floating	●		150	270	mV
		V_S = 5V, I_L = 5mA, BIAS Pin Floating	●		170	300	mV
		V_S = 5V, I_L = 20mA, BIAS Pin Floating	●		225	400	mV
		V_S = 3V, I_L = 0mA BIAS = V^+	●		120	225	mV
		V_S = 3V, I_L = 5mA BIAS = V^+	●		135	250	mV
		V_S = 3V, I_L = 20mA BIAS = V^+	●		195	350	mV
		V_S = 5V, I_L = 0mA BIAS = V^+	●		175	325	mV
		V_S = 5V, I_L = 5mA BIAS = V^+	●		200	360	mV
		V_S = 5V, I_L = 20mA BIAS = V^+	●		270	475	mV
I_{SC}	Output Short-Circuit Current, Either Output Pin (Note 12)	V_S = 3V	●	±45	±65		mA
		V_S = 5V	●	±60	±90		mA
V_S	Supply Voltage Range		●	2.7		5.25	V
I_S	Supply Current, BIAS Pin Floating	V_S = 2.7V	●		15.8	23	mA
		V_S = 3V	●		16	23.5	mA
		V_S = 5V	●		16.7	24.5	mA
	Supply Current, BIAS Pin Tied to V^+	V_S = 2.7V	●		32	41	mA
		V_S = 3V	●		32.2	41.5	mA
		V_S = 5V	●		33	43	mA
$I_{\overline{SHDN}}$	Supply Current, BIAS Pin Tied to V^-	V_S = 2.7V	●		0.4	1	mA
		V_S = 3V	●		0.45	1.1	mA
		V_S = 5V	●		0.65	1.8	mA
V_{BIASSD}	BIAS Input Pin Range for Shutdown	V_S = 2.7V to 5V	●	V^-		V^- + 0.4	V
V_{BIASLP} (Note 13)	BIAS Input for Low Power Operation	V_S = 2.7V to 5V	●	V^- + 1.0		V^- + 1.5	V
V_{BIASHP}	BIAS Input for High Performance Operation	V_S = 2.7V to 5V	●	V^- + 2.3		V^+	V
R_{BIAS}	BIAS Input Resistance	V_S = 2.7V to 5V	●	100	150	200	kΩ
V_{BIAS}	BIAS Float Voltage	V_S = 2.7V to 5V	●	V^- + 1.05	V^- + 1.15	V^- + 1.25	V
t_{ON}	Turn-On Time	V_S = 3V, $V_{\overline{SHDN}}$ = 0.25V to 3V			400		ns
t_{OFF}	Turn-Off Time	V_S = 3V, $V_{\overline{SHDN}}$ = 3V to 0.25V			400		ns

AC ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. V^+ = 3V, V^- = 0V, V_{INCM} = V_{OCM} = mid-supply, V_{BIAS} is tied to V^+ or floating, unless otherwise noted. (See Figure 2 for the AC test configuration.) V_S is defined as ($V^+ – V^-$). V_{OUTCM} is defined as ($V_{OUT}^+ + V_{OUT}^-$)/2. V_{ICM} is defined as ($V_{INP} + V_{INM}$)/2. $V_{OUTDIFF}$ is defined as ($V_{OUT}^+ – V_{OUT}^-$). V_{INDIFF} is defined as ($V_{INP} – V_{INM}$).

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
GAIN	Filter Gain, See Figure 2, BIAS Pin Floating (Remaining AC Measurements Relative to 1MHz)	ΔV_{IN} = ±0.25V, f_{TEST} = DC (Note 14) V_{IN} = 600mV$_{P-P}$, f_{TEST} = 1MHz V_{IN} = 600mV$_{P-P}$, f_{TEST} = 2MHz V_{IN} = 600mV$_{P-P}$, f_{TEST} = 5MHz V_{IN} = 600mV$_{P-P}$, f_{TEST} = 10MHz V_{IN} = 600mV$_{P-P}$, f_{TEST} = 14.45MHz V_{IN} = 600mV$_{P-P}$, f_{TEST} = 20MHz V_{IN} = 600mV$_{P-P}$, f_{TEST} = 50MHz	● ● ● ● ● ● ● ●	–0.25 –0.08 –0.01 –0.54 –3.00 –7.55 –23.55	±0.05 0 0.02 0.11 –0.34 –2.50 –6.55 –21.55	0.25 0.12 0.23 –0.14 –2.00 –5.55 –19.55	dB dB dB dB dB dB dB dB
PHASE	Filter Phase, See Figure 2, BIAS Pin Floating	ΔV_{IN} = ±0.25V, f_{TEST} = DC V_{IN} = 600mV$_{P-P}$, f_{TEST} = 1MHz V_{IN} = 600mV$_{P-P}$, f_{TEST} = 2MHz V_{IN} = 600mV$_{P-P}$, f_{TEST} = 5MHz V_{IN} = 600mV$_{P-P}$, f_{TEST} = 10MHz V_{IN} = 600mV$_{P-P}$, f_{TEST} = 14.45MHz V_{IN} = 600mV$_{P-P}$, f_{TEST} = 20MHz V_{IN} = 600mV$_{P-P}$, f_{TEST} = 50MHz	● ● ● ● ● ● ● ●	 –6.0 –12.5 –31.8 –70.1 –103.5 –130.7	0 –5.5 –11.3 –29.3 –65.2 –97.5 –125.1 –173.6	 –4.8 –10.1 –26.8 –60.1 –91.5 –120.7	Deg Deg Deg Deg Deg Deg Deg Deg
NOISE	Output Noise, See Figure 2, BIAS Pin Floating	BW = 100MHz BW = 20MHz			154 135		μV_{RMS} μV_{RMS}
SNR	BIAS Pin Floating	BW = 100MHz BW = 20MHz			73 74		dB dB
Distortion	V_{IN} = 2V$_{P-P}$, 10MHz, BIAS Pin Floating	HD2, Single-Ended Input HD3, Single-Ended Input HD2, Differential Input HD3, Differential Input			–60 –79 –65 –77		dBc dBc dBc dBc
f_O TC	Cutoff Frequency Temperature Coefficient				–120		ppm/°C
GAIN	Filter Gain, See Figure 2, BIAS Pin Tied to V^+, AC Gain Measurements Relative to 1MHz	ΔV_{IN} = ±0.25V, f_{TEST} = DC (Note 14) V_{IN} = 600mV$_{P-P}$, f_{TEST} = 1MHz V_{IN} = 600mV$_{P-P}$, f_{TEST} = 2MHz V_{IN} = 600mV$_{P-P}$, f_{TEST} = 5MHz V_{IN} = 600mV$_{P-P}$, f_{TEST} = 10MHz V_{IN} = 600mV$_{P-P}$, f_{TEST} = 14.45MHz V_{IN} = 600mV$_{P-P}$, f_{TEST} = 20MHz V_{IN} = 600mV$_{P-P}$, f_{TEST} = 50MHz	● ● ● ● ● ● ● ●	–0.25 –0.08 –0.01 –0.54 –2.75 –7.14 –23.70	±0.05 0 0.02 0.11 –0.34 –2.35 –6.24 –21.70	0.25 0.12 0.23 –0.14 –1.95 –5.34 –19.70	dB dB dB dB dB dB dB dB
PHASE	Filter Phase, See Figure 2, BIAS Pin Tied to V^+	ΔV_{IN} = ±0.25V, f_{TEST} = DC V_{IN} = 600mV$_{P-P}$, f_{TEST} = 1MHz V_{IN} = 600mV$_{P-P}$, f_{TEST} = 2MHz V_{IN} = 600mV$_{P-P}$, f_{TEST} = 5MHz V_{IN} = 600mV$_{P-P}$, f_{TEST} = 10MHz V_{IN} = 600mV$_{P-P}$, f_{TEST} = 14.45MHz V_{IN} = 600mV$_{P-P}$, f_{TEST} = 20MHz V_{IN} = 600mV$_{P-P}$, f_{TEST} = 50MHz	● ● ● ● ● ● ● ●	 –6.0 –12.2 –31.2 –68.8 –101.5 –128.4	0 –5.4 –11 –28.7 –63.8 –95.5 –123.4 –169.3	 –4.8 –9.8 –26.2 –58.8 –89.5 –118.4	Deg Deg Deg Deg Deg Deg Deg Deg
NOISE	Wide Band Output Noise, 14.45MHz Cutoff, BIAS Pin Tied to V^+	BW = 100MHz BW = 20MHz			108 97		μV_{RMS} μV_{RMS}
SNR	BIAS Pin Tied to V^+	BW = 100MHz BW = 20MHz			76 77		dB dB
DISTORTION	V_{IN} = 2V$_{P-P}$, 10MHz, BIAS Pin Tied to V^+	HD2, Single-Ended Input HD3, Single-Ended Input HD2, Differential Input HD3, Differential Input			–67.5 –90 –70 –90		dBc dBc dBc dBc
f_O TC	Cutoff Frequency Temperature Coefficient				–120		ppm/°C

ELECTRICAL CHARACTERISTICS

Note 1: Stresses beyond those listed under the Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

Note 2: All pins are protected by steering diodes to either supply. If any pin is driven beyond the part's supply voltage, the excess input current (current in excess of what it takes to drive that pin to the supply rail) should be limited to less than 10mA.

Note 3: A heat sink may be required to keep the junction temperature below the Absolute Maximum Rating when the output is shorted indefinitely. Long-term application of output currents in excess of the Absolute Maximum Ratings may impair the life of the device.

Note 4: The LTC6601C/LTC6601I are guaranteed functional over the operating temperature range –40°C to 85°C.

Note 5: The LTC6601C is guaranteed to meet specified performance from 0°C to 70°C. The LTC6601C is designed, characterized, and expected to meet specified performance from –40°C to 85°C but is not tested or QA sampled at these temperatures. The LTC6601I is guaranteed to meet specified performance from –40°C to 85°C.

Note 6: Output referred voltage offset is a function of the low frequency gain of the LTC6601. To determine output referred voltage offset, or output voltage offset drift, multiply this specification by the noise gain (1 + GAIN). See Applications Information for more details.

Note 7: Input bias current is defined as the average of the currents flowing into the noninverting and inverting inputs of the internal amplifier and is calculated from measurements made at the pins of the IC. Input offset current is defined as the difference of the currents flowing into the noninverting and inverting inputs of the internal amplifier and is calculated from measurements made at the pins of the IC.

Note 8: Input common mode range is tested using the test circuit of Figure 1 by measuring the differential DC gain with V_{ICM} = mid-supply, and with V_{ICM} at the input common mode range limits listed in the Electrical Characteristics table, verifying the differential gain has not deviated from the mid-supply common mode input case by more than 1%, and the common mode offset (V_{OCMOS}) has not deviated from the mid-supply common mode offset by more than ±20mV.

The voltage range for the output common mode range is tested using the test circuit of Figure 1 by measuring the differential DC gain with V_{OCM} = mid-supply, and again with a voltage set on the V_{OCM} pin at the Electrical Characteristics table limits, checking the differential gain has not deviated from the mid-supply common mode input case by more than 1%, and that the common mode offset (V_{OCMOS}) has not deviated by more than ±20mV from the mid-supply case.

Note 9: Input CMRR is defined as the ratio of the change in the input common mode voltage at the amplifier input to the change in differential input referred voltage offset. Output CMRR is defined as the ratio of the change in the voltage at the V_{OCM} pin to the change in differential input referred voltage offset.

Note 10: Power supply rejection (PSRR) is defined as the ratio of the change in supply voltage to the change in differential input referred voltage offset. Common mode power supply rejection (PSRRCM) is defined as the ratio of the change in supply voltage to the change in the common mode offset, V_{OUTCM}/V_{OCM}.

Note 11: Output swings are measured as differences between the output and the respective power supply rail.

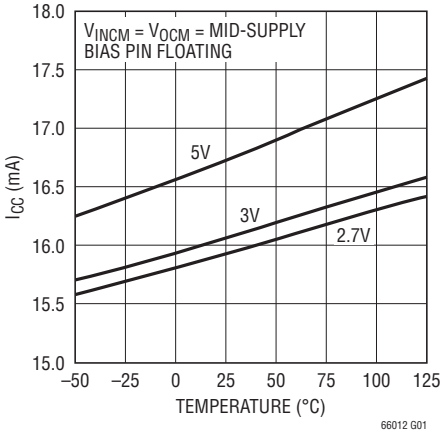
Note 12: Extended operation with the output shorted may cause junction temperatures to exceed the 150°C limit and is not recommended.

Note 13: Floating the BIAS pin will reliably place the part into the half-power mode. The pin does not have to be driven. Care should be taken, however, to prevent external leakage currents in or out of this pin from pulling the pin into an undesired state.

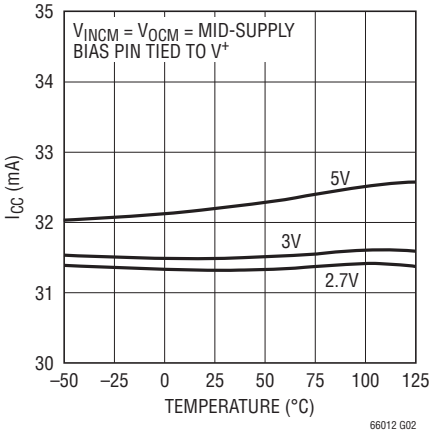
Note 14: The variable contact resistance of the high speed test equipment limits the accuracy of this test. These parameters only show a typical value, or conservative minimum and maximum value.

TYPICAL PERFORMANCE CHARACTERISTICS

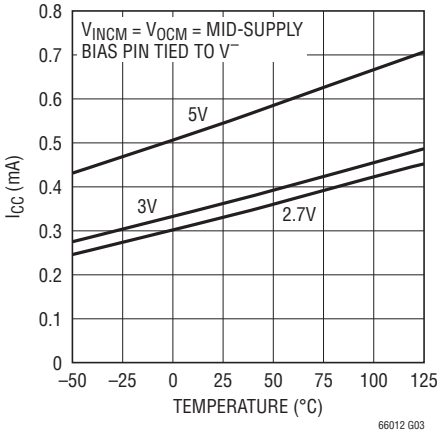
Low Power Supply Current vs Temperature and Supply Voltage



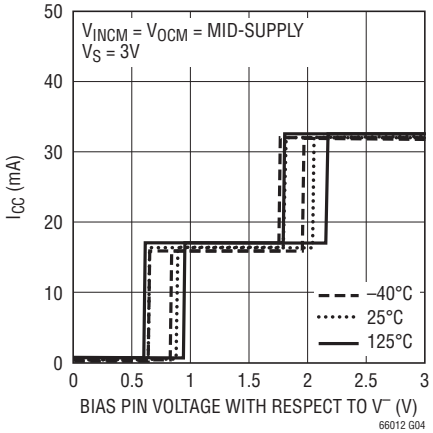
High Performance Supply Current vs Temperature and Supply Voltage



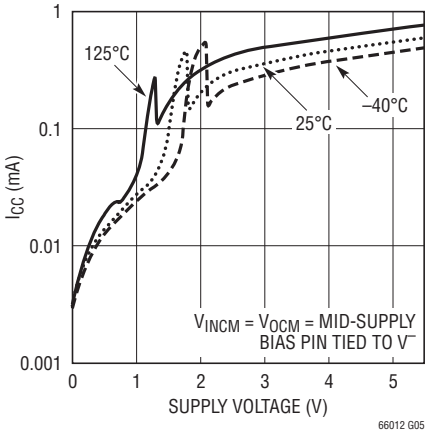
Shutdown Supply Current vs Temperature and Supply Voltage



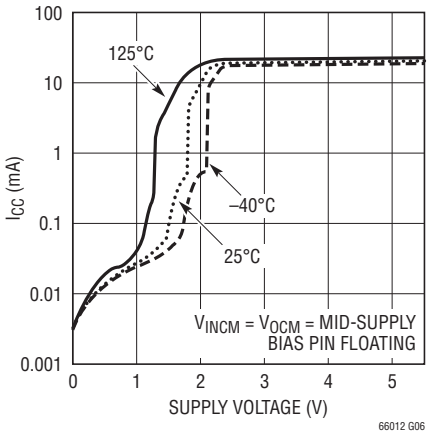
Supply Current vs Bias Pin Voltage and Temperature



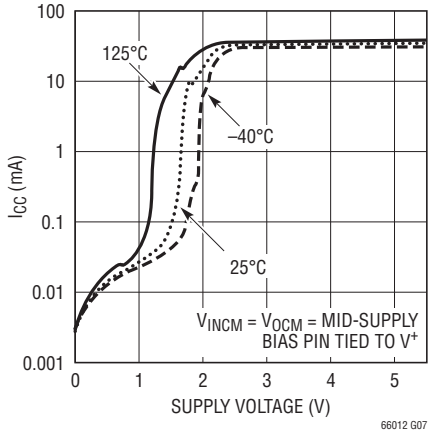
Shutdown Supply Current vs Supply Voltage and Temperature



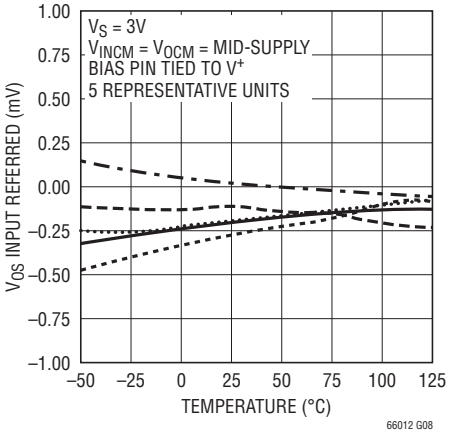
Low Power Mode Supply Current vs Supply Voltage and Temperature



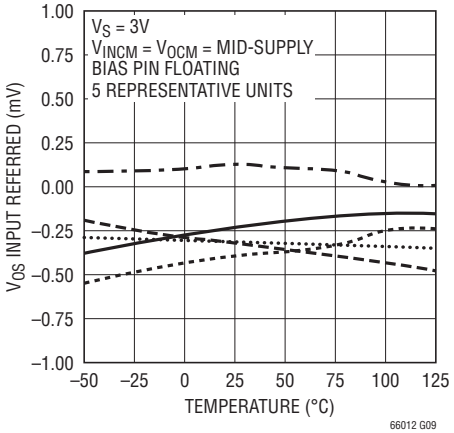
High Performance Supply Current vs Supply Voltage and Temperature



High Performance Mode Differential V_{OS} vs Temperature

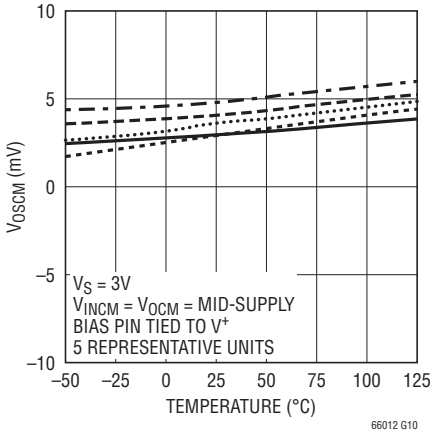


Low Power Mode Differential V_{OS} vs Temperature

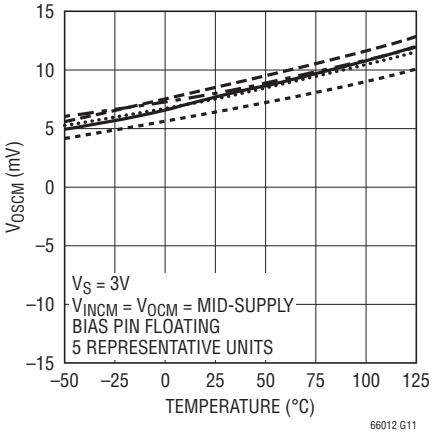


TYPICAL PERFORMANCE CHARACTERISTICS

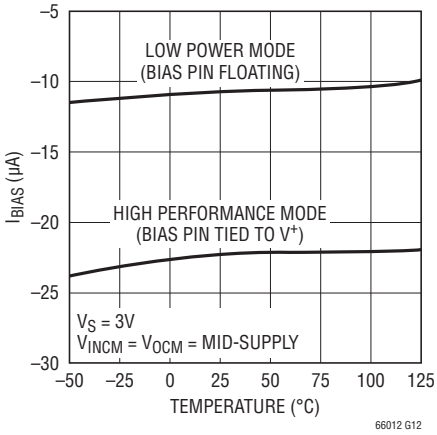
High Performance Common Mode V_{OS} vs Temperature



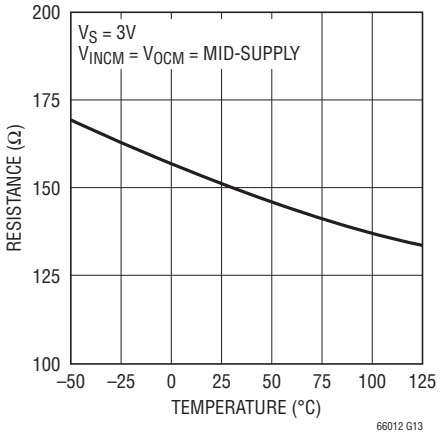
Low Power Common Mode V_{OS} vs Temperature



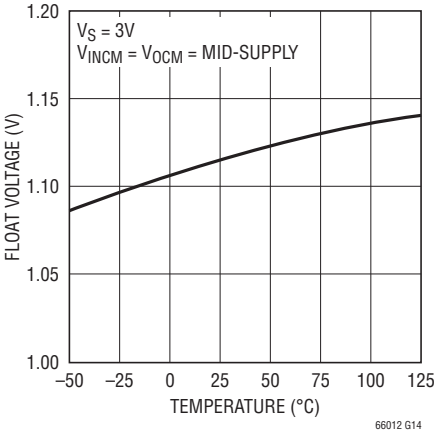
Internal Amplifier Input Bias Current vs Temperature



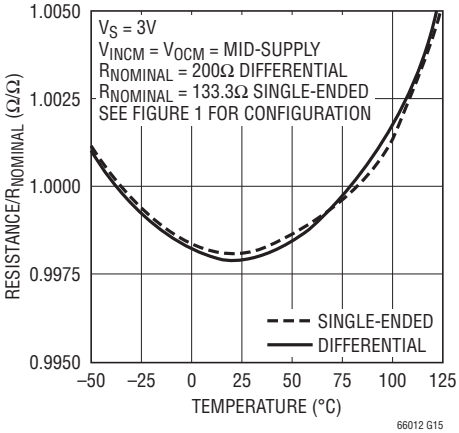
BIAS Pin Input Resistance vs Temperature



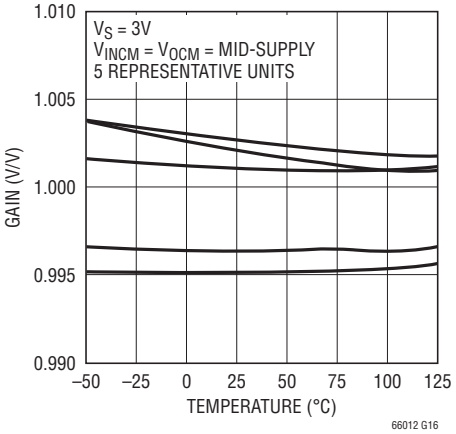
BIAS Pin Float Voltage vs Temperature



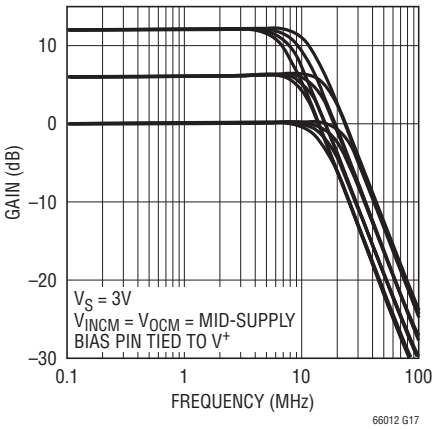
Filter Input Resistance vs Temperature



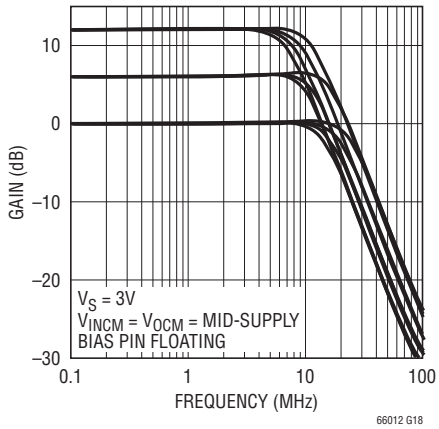
Low Frequency Gain vs Temperature



High Performance Mode Frequency Response of 12 Possible Filter Configurations

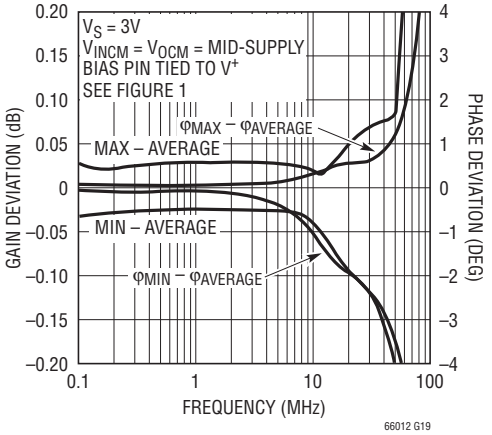


Low Power Mode Frequency Response of 12 Possible Filter Configurations

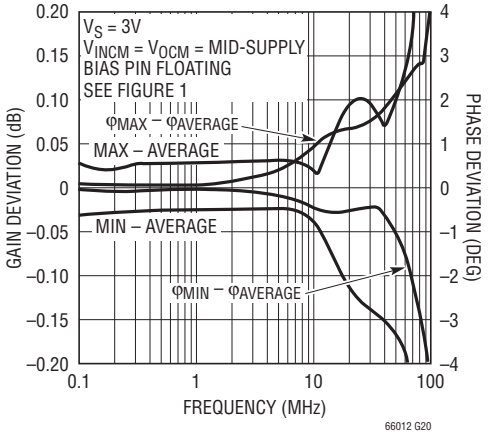


TYPICAL PERFORMANCE CHARACTERISTICS

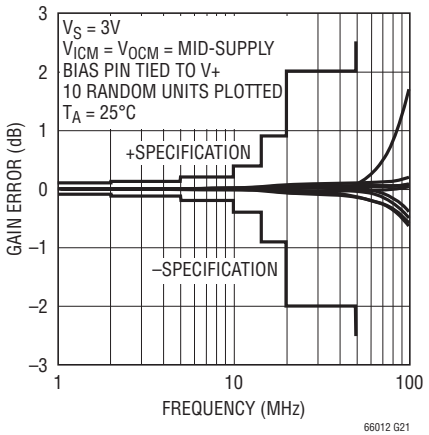
High Performance Mode Gain and Phase Repeatability of 10 Random Units



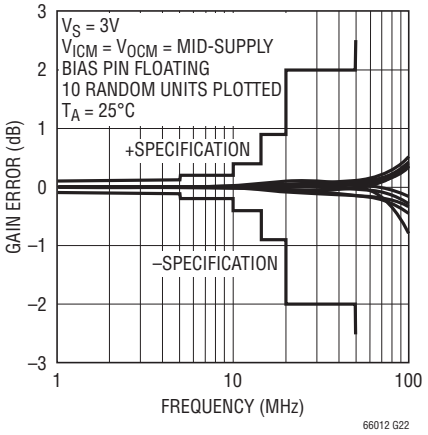
Low Power Mode Gain and Phase Repeatability of 10 Random Units



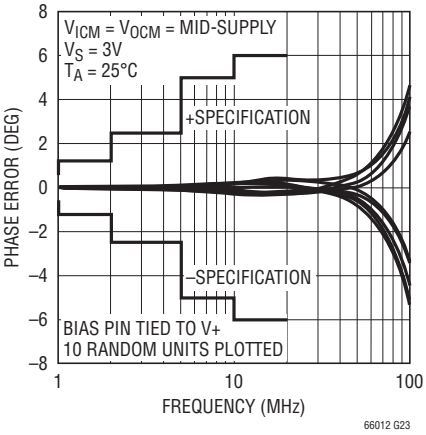
High Performance Mode Gain Error of 10 Random Units Normalized to 1MHz



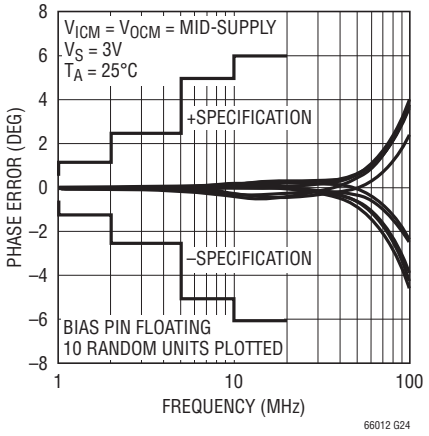
Low Power Mode Gain Error of 10 Random Units Normalized to 1MHz



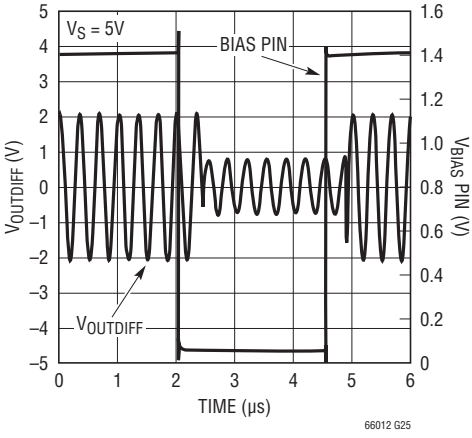
High Performance Mode Phase Error of 10 Random Units



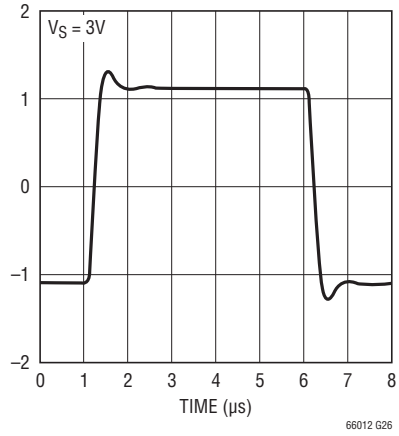
Low Power Mode Phase Error of 10 Random Units



Turn On and Turn Off Transient Response

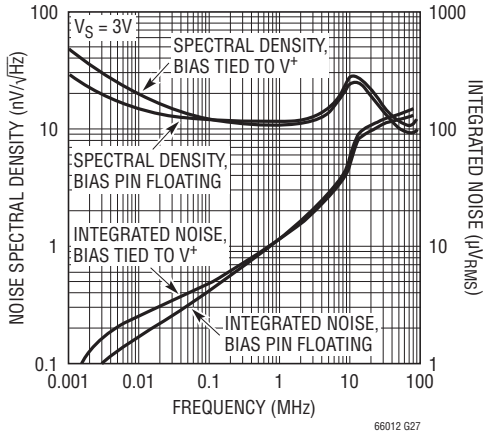


Pulse Response

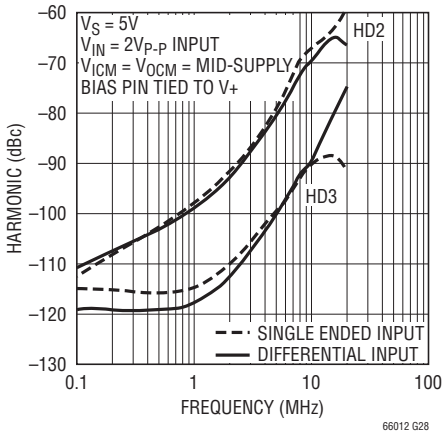


TYPICAL PERFORMANCE CHARACTERISTICS

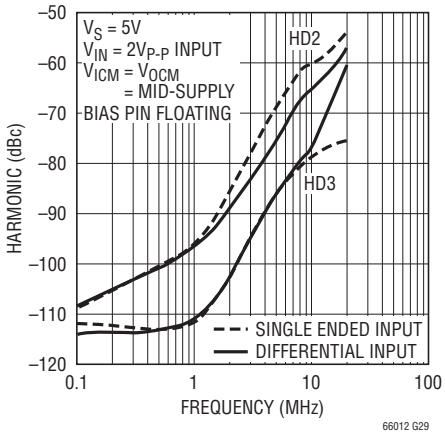
Differential Output Noise



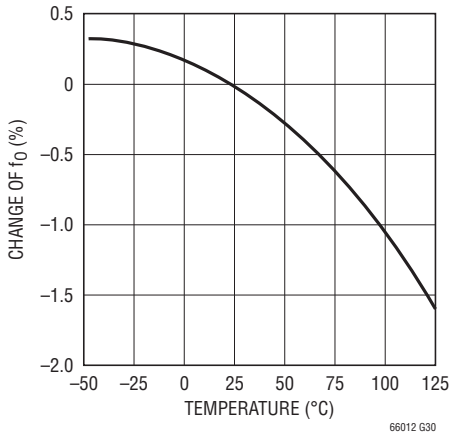
Distortion vs Frequency



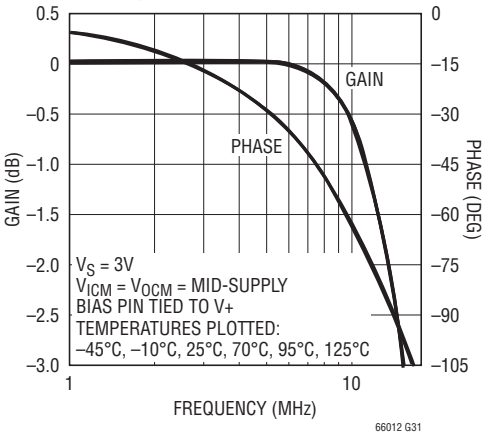
Distortion vs Frequency



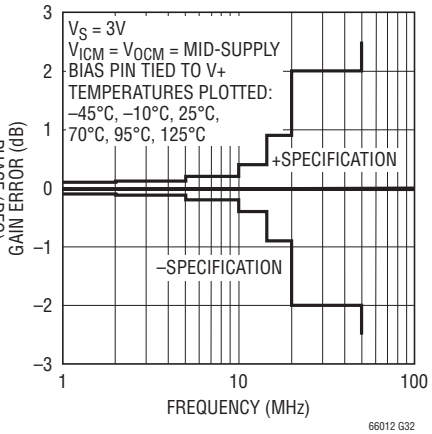
% Change of f_0 vs Temperature



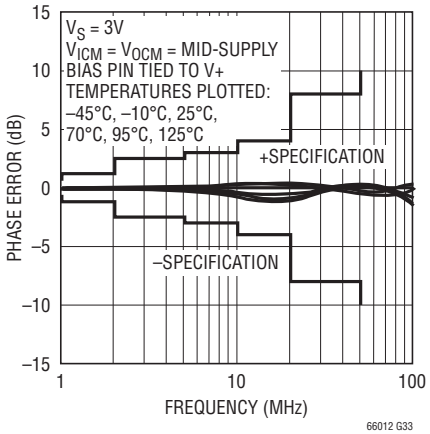
Passband Gain and Phase vs Temperature



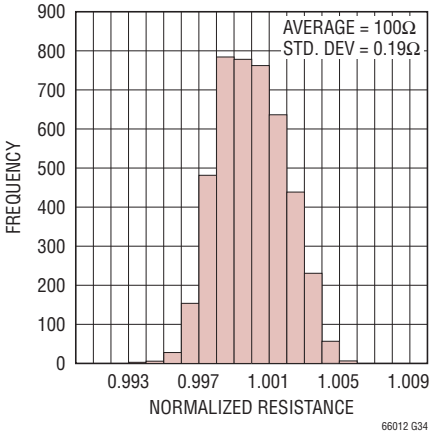
Gain Error Relative to 1MHz vs Temperature



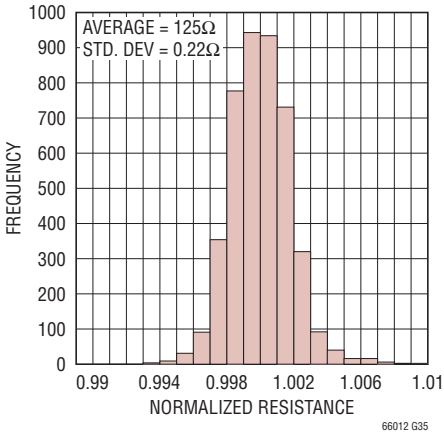
Phase Error vs Temperature



Normalized 100Ω Resistor Trim

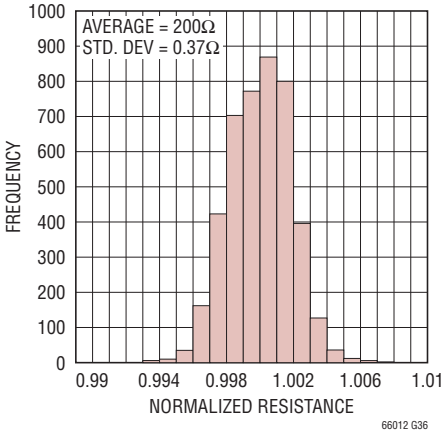


Normalized 125Ω Resistor Trim

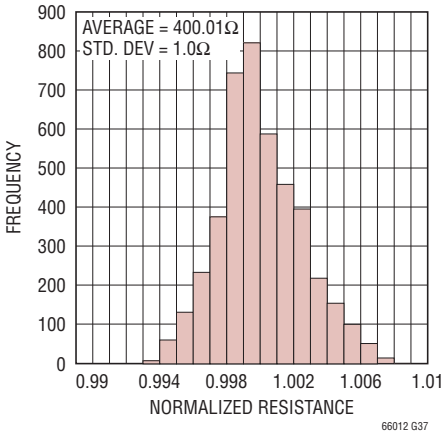


TYPICAL PERFORMANCE CHARACTERISTICS

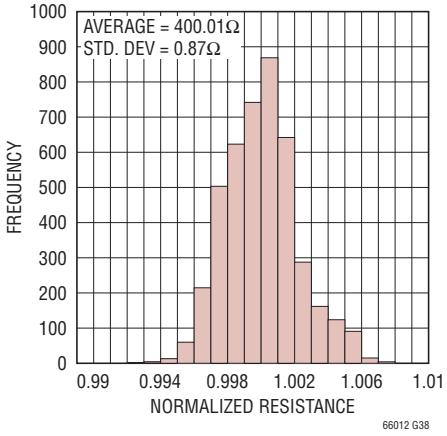
Normalized 200Ω Resistor Trim



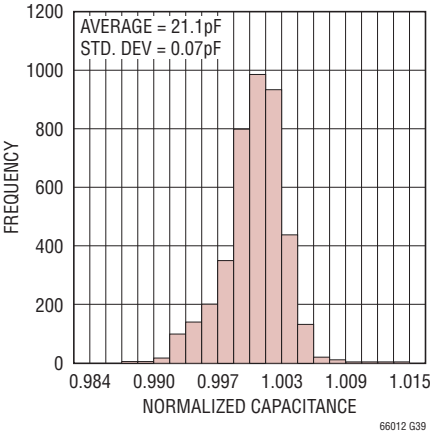
Normalized Input 400Ω Resistor Trim



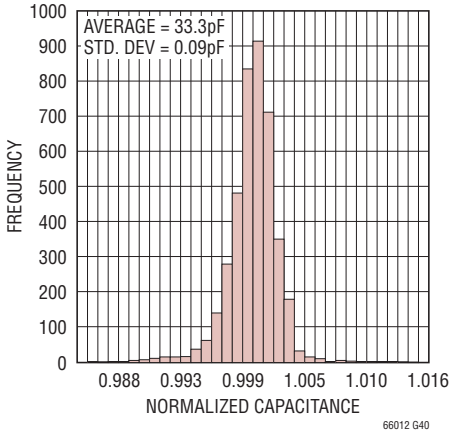
Normalized Feedback 400Ω Resistor Trim



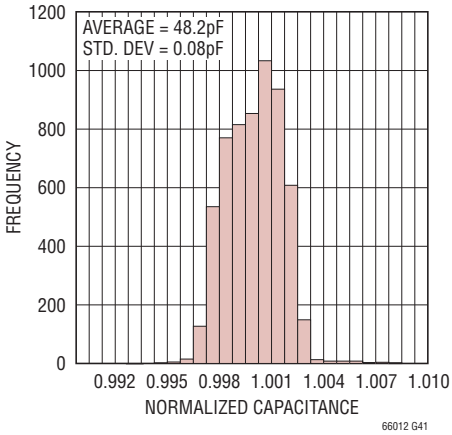
Normalized 21.1pF Capacitor Trim



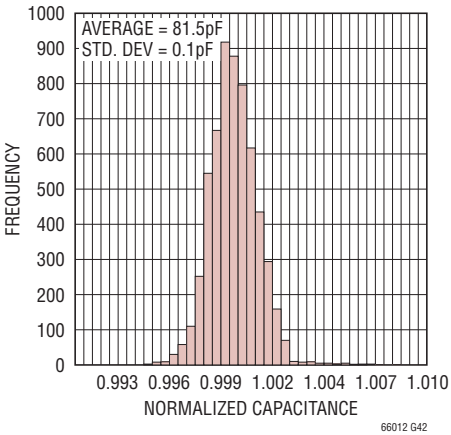
Normalized 33.3pF Capacitor Trim



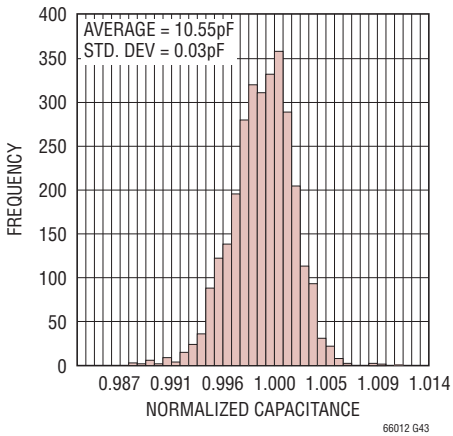
Normalized 48.2pF Capacitor Trim



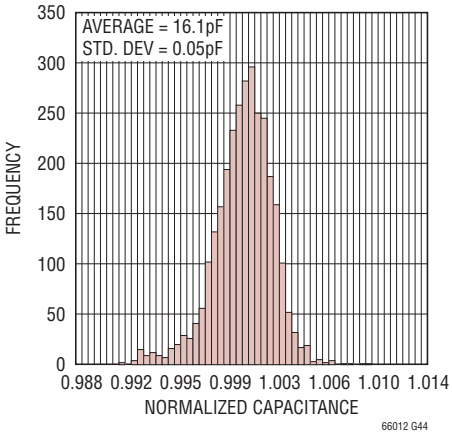
Normalized 81.5pF Capacitor Trim



Normalized 10.55pF Capacitor Trim



Normalized 16.1pF Capacitor Trim



PIN FUNCTIONS (Refer to the Block Diagram)

IN1+, IN2+, IN4+ (Pins 2, 1, 20): Input to a trimmed 100Ω, 200Ω, 400Ω resistor which feeds a noninverting summing node. Can accept an input signal, be floated or tied to OUT–. For best performance, stray capacitance should be kept as low as possible by keeping printed circuit connections as short and direct as possible. If necessary, strip back the surrounding ground plane away from these pins.

BIAS (Pin 3): Input to a three-state comparator whose three states allow the user to tailor amplifier power. The pin impedance appears as a 150k resistor whose default open-circuit potential is 1.15V with respect to the V– power supply. If BIAS is driven to within 0.4V of the V– supply, the amplifier is placed into a low power shutdown, consuming typically 450µA. When BIAS is floated, the amplifier operates in its low power active state. Forcing the pin 2.3V above V– places the part into the high performance active state. See Applications Information for more detail.

IN1–, IN2–, IN4– (Pins 4, 5, 6): Input to a trimmed 100Ω, 200Ω, 400Ω resistor which feeds an inverting summing node. Can accept an input signal, be floated or tied to OUT+. For best performance, it is highly recommended that stray capacitance be kept to as low as possible by keeping printed circuit connections as short and direct as possible, and if necessary, stripping back nearby surrounding ground plane away from these pins.

C1, C2 (Pins 7, 8): Input to a trimmed 16.1pF, 33.3pF capacitor which feeds a noninverting summing node. Typically, either float or tie to OUT–. If either of these pins is tied to a low impedance source other than OUT–, a resistance of at least 25Ω should be placed in series. For best performance, it is highly recommended that stray capacitance be kept to as low as possible by keeping printed circuit connections as short and direct as possible, and if necessary, stripping back nearby surrounding ground plane away from these pins.

C3, C4 (Pins 9, 10): Input to a trimmed 10.55pF, 21.1pF capacitor which feeds the amplifier inverting summing node. Typically, either float or tie to OUT+. For best performance, it is highly recommended that stray capacitance be kept to as low as possible by keeping printed circuit connections as short and direct as possible, and if necessary, stripping back nearby surrounding ground plane away from these pins.

OUT+, OUT– (Pins 11, 15): Output Pins. Besides driving the internal feedback network, each pin can drive an additional 50Ω to ground with typical short-circuit current limiting of ±65mA. Capacitive loading of these pins should be minimized by resistively decoupling the outputs from the load with at least 25Ω.

V_{OCM} (Pin 12): Output Common Mode Reference Voltage. The voltage on V_{OCM} sets the output common mode voltage level (which is defined as the average of the voltages on the OUT+ and OUT– pins). The V_{OCM} pin is the midpoint of an internal resistive voltage divider between the supplies, developing a (default) mid-supply voltage potential to maximize output signal swing. The V_{OCM} pin can be overdriven by an external voltage reference capable of driving the input impedance presented by the V_{OCM} pin. The V_{OCM} pin has an input resistance of approximately 7k to a mid-supply potential. It should be bypassed with a high quality ceramic bypass capacitor (for instance of X7R dielectric) of at least 0.01µF, (unless using symmetrical split supplies, then connect directly to a low impedance, low noise ground plane) to minimize common mode noise from being converted to differential noise by impedance mismatches both externally and internally to the IC.

PIN FUNCTIONS (Refer to the Block Diagram)

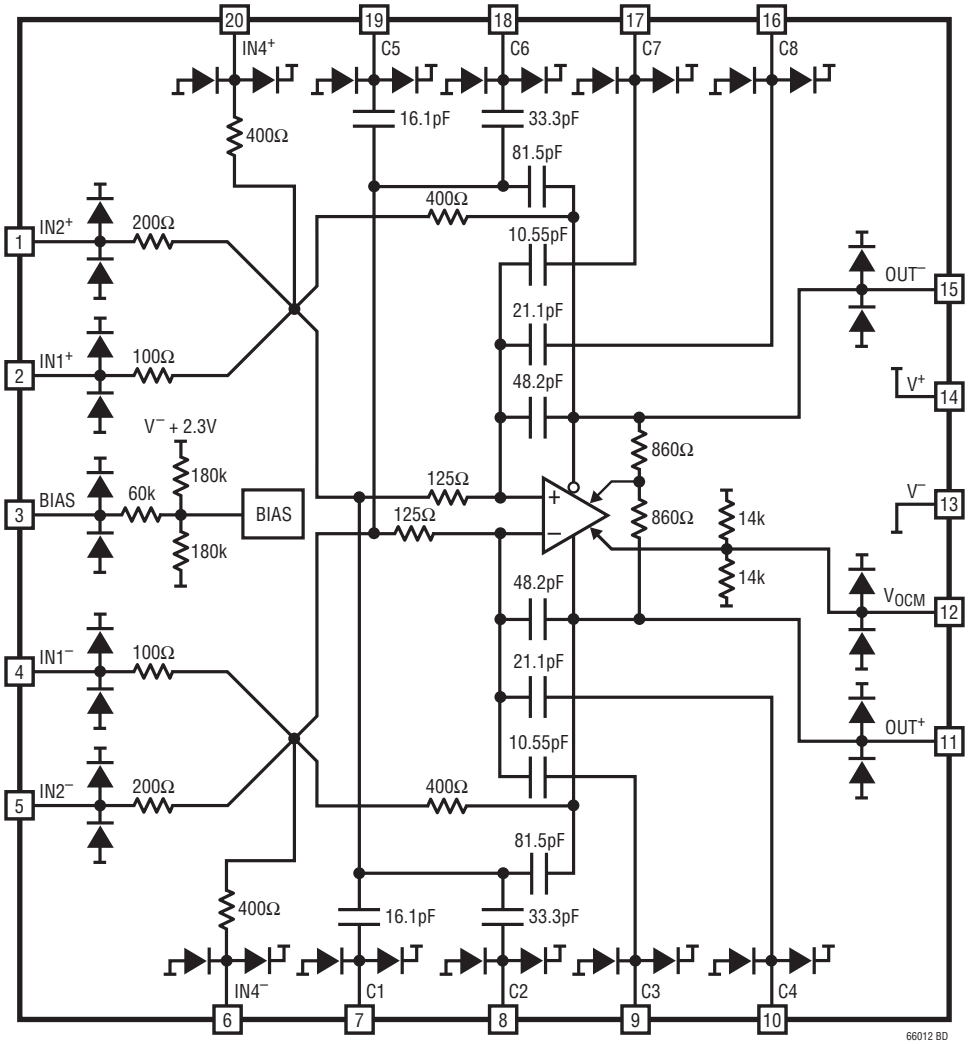
V^+, V^- (Pins 14, 13): Power Supply Pins. It is critical that close attention be paid to supply bypassing. For single supply applications (Pin 13 grounded), it is recommended that a high quality 0.1µF surface mount ceramic bypass capacitor (X7R dielectric for instance) be placed between Pins 14 and 13, with direct short connections. Pin 13 should be tied directly to a low impedance ground plane with minimal routing. For dual (split) power supplies, it is recommended that at least two additional high quality 0.1µF ceramic capacitors are used to bypass V^+ to ground and V^- to ground, again with minimal routing. For driving large loads (< 200Ω), additional bypass capacitance may be added for optimal performance. Keep in mind that small geometry (e.g., 0603) surface mount ceramic capacitors have a much lower ESL than do leaded capacitors, and perform best in high speed applications.

C7, C8 (Pins 17, 16): Input to a trimmed 10.55pF, 21.1pF capacitor which feeds the amplifier noninverting summing node. Typically, either float or tie to OUT^-. For best performance, stray capacitance should be kept as low as possible by keeping printed circuit connections as short and direct as possible.If necessary, strip back the surrounding ground plane away from these pins.

C5, C6 (Pins 19, 18): Input to a trimmed 16.1pF, 33.3pF capacitor which feeds an inverting summing node. Typically, either float or tie to OUT^+. If either of these pins are tied to a low impedance source other than OUT^+, a resistance of at least 25Ω should be placed in series. For best performance, it is highly recommended that stray capacitance be kept to as low as possible by keeping printed circuit connections as short and direct as possible, and if necessary, stripping back nearby surrounding reference plane away from these pins.

Exposed Pad (Pin 21): Always tie the underlying Exposed Pad to V^- (Pin 13). If split supplies are used, **do not tie the pad to ground. Tie it to V^-.**

BLOCK DIAGRAM



TEST CIRCUITS

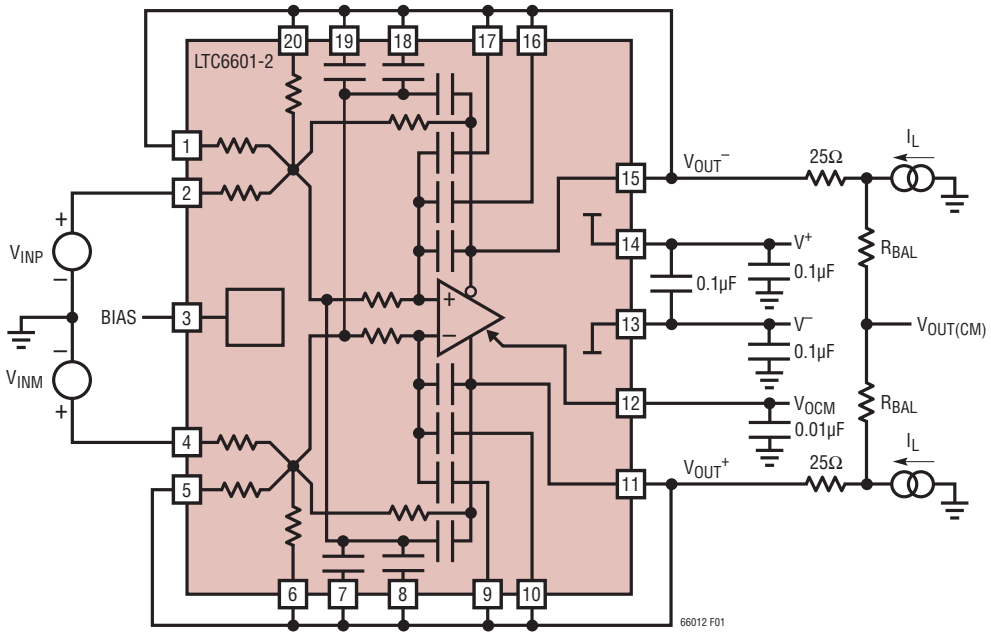


Figure 1. DC Test Circuit

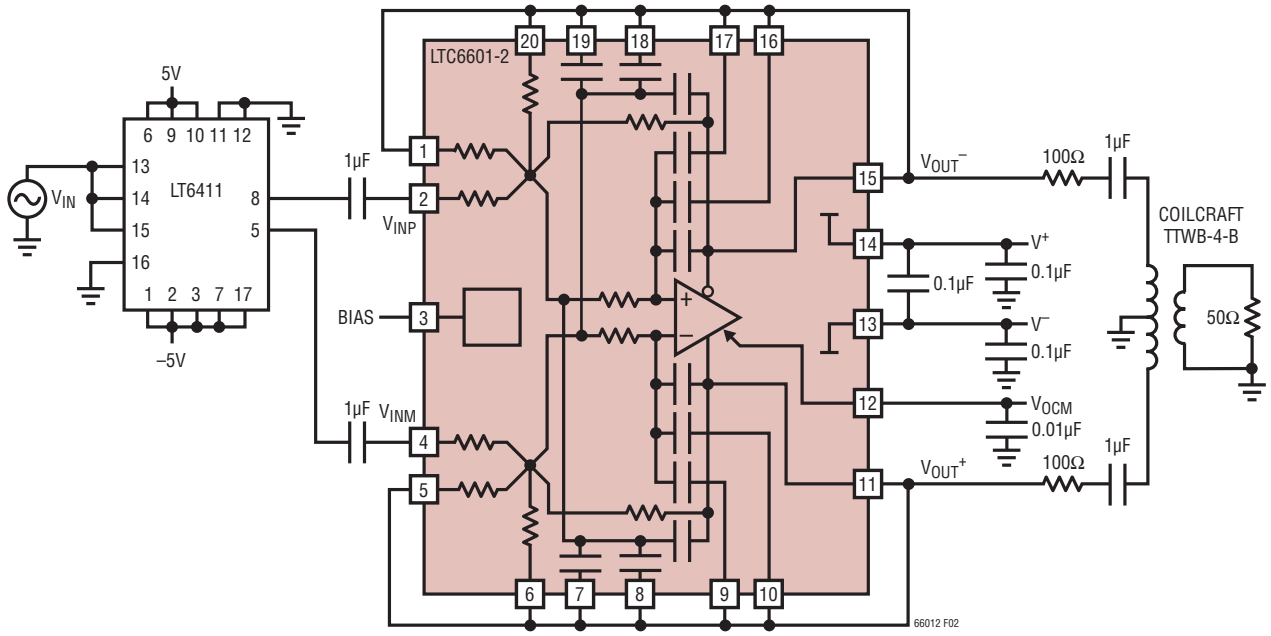


Figure 2. AC Test Circuit (Frequency Response Testing)

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FUNCTIONAL DESCRIPTION

The LTC6601 is designed to make the implementation of high frequency fully-differential filtering functions very easy. A very low noise amplifier is surrounded by 8 precision matched resistors and 12 precision matched capacitors so that a myriad of filter transfer functions limited only by possible combinations and imagination can be configured by hard wiring pins. The amplifier itself is a wide band, low noise and low distortion fully-differential amplifier with accurate output phase balancing. It is optimized for driving low voltage, single-supply, differential input, analog-to-digital converters (ADCs). The LTC6601's outputs are capable of swinging rail-to-rail on supplies as low as 2.7V, which makes the amplifier ideal for converting ground referenced, single-ended signals into V_{OCM} referenced differential signals. Unlike traditional op amps which have a single output, the LTC6601 has two outputs to process signals differentially. This allows for two times the signal swing in low voltage systems when compared to single-ended output amplifiers. The balanced differential nature of the amplifier and matched surrounding components provide even-order harmonic distortion cancellation, and less susceptibility to common mode noise (like power supply noise). The LTC6601 can be used as a single-ended input to differential output amplifier, or as a differential input to differential output amplifier.

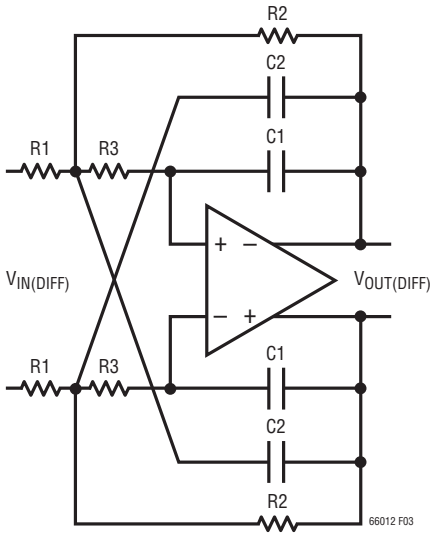
Figure 3 shows the basic filter architecture. The Laplace transfer function from V_{INDIFF} to $V_{OUTDIFF}$ is given by the following generalized equation for a 2nd order lowpass filter:

$$\frac{V_{OUTDIFF}}{V_{INDIFF}} = \frac{Gain}{1+\frac{s}{2\pi f_0 \bullet Q}+\frac{s^2}{(2\pi f_0)^2}}$$

Both Gain and Q of the filter are based on component ratios, which match and track extremely well over temperature. The corner frequency of the filter is a function of an RC product. This RC product is trimmed to ±1% (typical) and is not expected to drift by more than ±1% from nominal over the entire temperature range –40°C to 85°C. As a result, fully differential filters with tight magnitude, phase tolerance and repeatability are achieved.

Although Figure 3 implies a differential input, the LTC6601 easily accepts single-ended inputs to either input, and will faithfully replicate the signal at the output in differential form.

The LTC6601's output common mode voltage, defined as the average of the two output voltages, is independent of the input common mode voltage, and is adjusted by applying a voltage on the V_{OCM} pin. If the pin is left open, there is an internal resistive voltage divider, which develops a



$$f_0 = \frac{1}{2\pi\sqrt{R2 \bullet R3 \bullet C1 \bullet C2}}$$

$$Q = \sqrt{\frac{C2}{C1}\frac{R3}{R2}} \bullet \frac{1}{1+\left(1+|GAIN|\right) \bullet \frac{R3}{R2}-\frac{C2}{C1}}$$

$$GAIN = \frac{R2}{R1}$$

$$f_{3dB} = \frac{f_0 \bullet \sqrt{\left(6089 \bullet \sqrt{\left(3568 \bullet Q^4 - 1788 \bullet Q^2 + 447\right)+1.287 \bullet 10^5 \bullet \left(2 \bullet Q^2 - 1\right)}\right)}}{507.6 \bullet Q}$$

$$Q = \frac{0.2236 \bullet f_0 \bullet \sqrt{\left(2.109 \bullet 10^5 \bullet \sqrt{\left(9.891 \bullet 10^{12} \bullet {f_{3dB}}^4 - 5.486 \bullet 10^9 \bullet {f_0}^4\right)+120 \bullet \left(5.526 \bullet 10^9 \bullet {f_{3dB}}^2 + 3.082 \bullet 10^6 \bullet {f_0}^2\right)}\right)}}{\sqrt{\left(16 \bullet {f_0}^2 \bullet \left(8.29 \bullet 10^9 \bullet {f_{3dB}}^2 + 4.127 \bullet 10^9 \bullet {f_0}^2\right) - 6.638 \bullet 10^{10} \bullet {f_{3dB}}^4\right)}}$$

Figure 3. Basic Filter Topology and Equations

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potential halfway between the V^+ and V^- pins. Whenever this pin is not hard tied to a low impedance ground plane, a high quality ceramic capacitor should be used to bypass the V_{OCM} pin to a low impedance ground plane (see Layout Considerations). The LTC6601's internal common mode feedback path forces accurate output phase balancing to reduce even order harmonics, and centers each individual output about the potential set by the V_{OCM} pin.

$$V_{OUTCM} = V_{OCM} = \frac{V_{OUT}^{+} + V_{OUT}^{-}}{2}$$

The outputs (OUT^+ and OUT^-) of the LTC6601 are capable of swinging rail-to-rail. They can source or sink up to approximately 75mA of current. Load capacitances should be decoupled with at least 25Ω of series resistance from each output.

The LTC6601 Electrical Characteristics table specifies an input referred offset. This specification actually lumps voltage offsets due to offset bias currents (I_{OS}), and amplifier voltage offset into one specification. To refer this specification to the output, you simply multiply the specification by the noise gain the LTC6601 is configured in:

$$V_{OSODIFF} = 1 + Gain$$

where Gain is the closed loop gain in the particular filter application:

$$Gain = \frac{R2}{R1}$$

COMPONENT INPUT PIN PROTECTION

All of the LTC6601 pins with the exception of V^+ and V^- are protected with steering diodes to either power supply. In the event that a pin is driven beyond the supply rails, the excess current should be limited to under 10mA to prevent damage to the IC.

BIAS Pin

The LTC6601 has a BIAS pin (Pin 3) whose function is to tailor both performance and power of the LTC6601. The pin has a Thevenin equivalent impedance of approximately 150kΩ to a voltage source whose potential is 1.15V above the V^- supply. This pin has fixed logic levels relative to V^- (see the Electrical Characteristics table), and can be driven by an external source keeping in mind its equivalent input impedance and equivalent input voltage. If the BIAS pin is floated, care should be taken to control external leakage currents to this pin to under 1µA to prevent putting the LTC6601 an undesired state.

If BIAS is tied to the positive supply, the LTC6601 differential filter will be in a fully active state configured for highest performance (lowest noise and lowest distortion). If the BIAS pin is floated or left unconnected, the LTC6601 filter will be in a fully active state, with amplifier currents reduced and performance scaled back to preserve power consumption. If the BIAS pin is tied to the most negative supply (V^-), the LTC6601 will be placed into a low power shutdown mode with amplifier outputs disabled. In this state, the LTC6601 draws approximately 450µA.

In low power shutdown, all internal biasing current sources are shut off, and the output pins, OUT^+ and OUT^-, will each appear as open collectors with a non-linear capacitor in parallel and steering diodes to either supply. The turn-on and turn-off time constant between states are on the order of 0.4µs. Using this function to wire-OR outputs together is not recommended.

General Design and Usage

As levels of integration have increased and correspondingly, system supply voltages decreased, there has been a need for ADCs to process signals differentially in order to maintain good signal-to-noise ratios. These ADCs are typically supplied from a single supply voltage which can be as low as 3V (2.7V min), and will have an optimal common mode input range near mid-supply. The LTC6601 makes interfacing to these ADCs easy, by providing anti-alias filtering, single-ended to differential conversion and common mode level shifting (translation). Figure 3 shows a general application of this. The low frequency gain to $V_{OUTDIFF}$ from V_{IN} is simply:

$$V_{OUTDIFF} = V_{OUT}^{+} - V_{OUT}^{-} \approx \frac{R2}{R1} \bullet V_{INDIFF}$$

The differential output voltage ($V_{OUT}^+ - V_{OUT}^-$) is completely independent of input and output common mode voltages, or the voltage at the common mode pin. This makes the

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LTC6601 ideally suited for pre-amplification, level shifting and conversion of single-ended signals to differential output signals for driving differential input ADCs.

INPUT IMPEDANCE

Calculating the low frequency input impedance of the LTC6601 depends on how the inputs are driven (whether they are driven from a single-ended or a differential source).

Figure 4 shows a simplified low frequency equivalent circuit of the LTC6601. For balanced input sources ($V_{INP} = -V_{INM}$), the low frequency input impedance is given by the equation:

$$R_{INP} = R_{INM} = R1$$

The differential input impedance is simply:

$$R_{INDIFF} = 2 \bullet R1$$

For single-ended inputs ($V_{INM} = 0$), the input impedance actually increases over the balanced differential case due to the fact the summing node (at the junction of R1, R2 and R3) moves in phase with V_{INP} to bootstrap the input impedance. Referring to Figure 4 with $V_{INM} = 0$, the input impedance looking into either input is:

$$R_{INP} = R_{INM} \frac{R1}{\left(1 - \frac{1}{2} \bullet \left(\frac{R2}{R1+R2}\right)\right)}$$

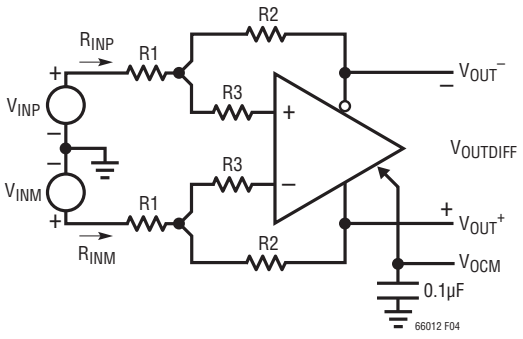

Figure 4. Input Impedance

Input and Output Common Mode Voltage Range

The input common mode voltage is defined as the average of the two inputs:

$$V_{INCM} = \frac{V_{INP} + V_{INM}}{2}$$

The lower limit of the input common mode range is dictated by the ESD protection diodes at the input. While it is possible for the inputs to swing below V^-, the diodes will conduct if the inputs are taken a diode drop below V^-. The upper limit of the input common mode range varies as a function of the filter configuration (GAIN), V_{OCM} potential, and whether or not the inputs are single-ended or differential. While it is possible to exceed the upper limit of the common mode range, doing so will degrade filter linearity. Referring to Figure 4, for linear operation, the summing junction where R1, R2 and R3 merge together should be prevented from swinging to within 1.4V of the V^+ power supply.

For the general case, the upper input common mode voltage limit should be constrained to:

$$V_{OCM} \bullet \frac{R1}{R1+R2} + V_{INCM} \bullet \frac{R2}{R1+R2} \leq V^+ - 1.4V$$

Or equivalently:

$$V_{INCM} \leq \left(1 + \frac{R1}{R2}\right)\left(V^+ - 1.4V\right) - \frac{R1}{R2} \bullet V_{OCM}$$

The specifications for input common mode range (V_{INCMR}) are based on these constraints with R1 = R2 = 100Ω, and V_{OCM} = mid-supply. Substituting the numbers for a single 3V power supply, (V^+ = 3V, V^- = 0V) with V_{OCM} =1.5V, and R1 = R2 = 100Ω, into the above equation, the input common mode range (V_{INCMR}) is between the two limits:

$$0V \leq V_{INCM} \leq 1.7V$$

which is as is specified for a 3V supply.

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Likewise, substituting the numbers for a single 5V power supply, (V^+ = 5V, V^- = 0V) with V_{OCM} = 2.5V, and R1 = R2 = 100Ω, into the above equation, the input common mode range (V_{INCMR}) is between the two limits:

$0V \le V_{INCM} \le 4.7V$

The output common mode voltage is defined as the average of the two outputs:

$$V_{OUTCM} = V_{OCM} = \frac{V_{OUT}^{+} + V_{OUT}^{-}}{2}$$

The V_{OCM} pin sets this average by an internal common mode feedback loop which internally forces $V_{OUT}+ = -V_{OUT}-$. The output common mode range extends from 1.1 V above V^- to 1V below V^+. The V_{OCM} pin sits in the middle of a voltage divider which sets the default mid-supply open circuit potential.

In single supply applications, where the LTC6601 is used to interface to an ADC, the optimal common mode input to the ADC is often determined by the ADC's reference. If the ADC makes a reference available for setting the input common mode voltage, it can be directly tied to the V_{OCM} pin, but must be capable of driving the input impedance of the V_{OCM} pin (R_{VOCM}). This impedance can be assumed to be connected to a mid-supply potential. If an external reference drives the V_{OCM} pin, it should still be bypassed with a high quality 0.01µF or higher capacitor to a low impedance ground plane to filter any thermal noise and to prevent common mode signals on this pin from being inadvertently converted to differential signals.

Noise Considerations

When comparing the LTC6601 noise to other amplifiers, be sure to compare similar specifications. Competing devices often specify noise referred to the inputs of the amplifier. The input referred voltage noise of the LTC6601-2 is 4.7nV/√Hz.

In addition to the noise generated by the amplifier, the surrounding feedback resistors also contribute noise. A noise model is shown in Figure 5. The output spot noise generated by both the amplifier and the feedback components is governed by the equation:

$$e_{no} = \sqrt{\left(e_{ni} \bullet \left(1+\frac{R2}{R1}\right)\right)^2 + 2 \bullet \left(I_n^2 \bullet \left(R2^2 + R3^2 \bullet \left(1+\frac{R2}{R1}\right)^2\right)\right) + 2 \bullet \left(e_{nR1} \bullet \left(\frac{R2}{R1}\right)\right)^2 + 2\left(e_{nR3} \bullet \left(1+\frac{R2}{R1}\right)\right)^2 + 2 \bullet e_{nR2}^2}$$

Substituting the equation for Johnson noise of a resistor (e_{nR} = 4kTR), and simplifying:

$$e_{no} = \sqrt{\left(e_{ni} \bullet \left(1+\frac{R2}{R1}\right)\right)^2 + 2 \bullet \left(I_n^2 \bullet \left(R2^2 + R3^2 \bullet \left(1+\frac{R2}{R1}\right)^2\right)\right) + 8 \bullet k \bullet T\left(R2\left(1+\frac{R2}{R1}\right) + R3\left(1+\frac{R2}{R1}\right)^2\right)}$$

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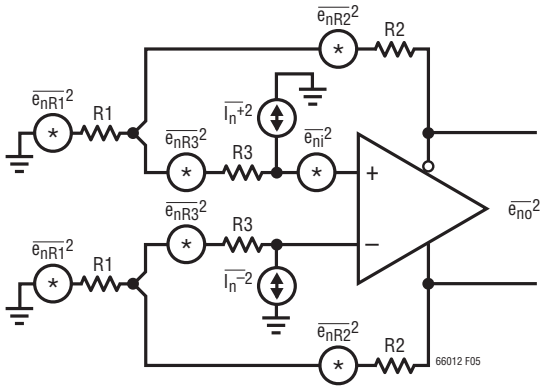

Figure 5. Differential Noise Model of the LTC6601

Table 1 lists the amplifier input referred noise for the LTC6601-2. Tables 2 to10 list the noise referred to the input pins of the IC for common configurations of the LTC6601-2. To determine the spot noise at the output, simply multiply the noise by the Gain = R2/R1. To estimate the integrated noise at the output, multiply the noise by the gain, and the square root of the noise bandwidth. The noise bandwidth depends on the filter configuration. For Figure 2, the noise bandwidth is 100MHz, or approximately 7 times the filter bandwidth. Improvements in SNR can be made by adding an additional RC filter at the output to band limit wide band noise before feeding ADCs. See the section "Interfacing the LTC6601 to ADC Converters" for more detail.

Table 1. Amplifier (Input Referred) Noise Characteristics for the LTC6601-2

BIAS PIN PULLED TO V^+		BIAS PIN FLOATING	
e_{ni} nV/√Hz	i_n pA/√Hz	e_{ni} nV/√Hz	i_n pA/√Hz
4.7	3	5.2	2.1

LAYOUT CONSIDERATIONS

Because the LTC6601 is a very high speed amplifier, it is sensitive to both stray capacitance and stray inductance. It is critical that close attention be paid to supply bypassing. For single supply applications, it is recommended that a high quality 0.1µF surface mount ceramic bypass capacitor be placed between Pins 14 and 13 with direct short connections. Pin 13 and the Exposed Pad, Pin 21, should be tied directly to a low impedance ground plane with minimal routing. For dual (split) power supplies, it is recommended that an additional high quality, 0.1µF ceramic capacitor be used to bypass pin V^+ to ground and $V^–$ to ground, again with minimal routing. For driving large differential loads (<200Ω), additional bypass capacitance may be needed between V^+ and $V^–$ for optimal performance. Note that small geometry (e.g., 0603) surface mount ceramic capacitors have a much higher self resonant frequency than capacitors with leads, and perform best in high speed applications.

The V_{OCM} pin should be bypassed to ground with a high quality ceramic capacitor whose value exceeds 0.01µF, with direct, short connections. In split supply applications, the V_{OCM} pin can be either bypassed to ground or directly hardwired to ground. Be careful not to violate the output common mode range specifications for the V_{OCM} pin.

Stray parasitic capacitances to unused component pins that set up the filter's characteristics, should be kept to an absolute minimum. This prevents deviations from the ideal frequency response. An ideal layout technique would be to remove the solder pads for the unused component pins, and strip away the ground plane underneath these pins to lower capacitance to an absolute minimum. Floating unused component pins which set up the filter characteristics will not reduce the reliability of the LTC6601.

At the output, always keep in mind the differential nature of the LTC6601, and that it is critical that the load impedances seen by both outputs (stray or intended), should be as balanced and symmetric as possible. This will help preserve the natural balance of the LTC6601, which minimizes the generation of even order harmonics and preserves the rejection of common mode signals and noise.

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INTERFACING THE LTC6601 TO ADC CONVERTERS

The LTC6601's rail-to-rail differential output and adjustable output common mode voltage make the LTC6601 ideal for interfacing to low voltage, single supply, differential input ADCs. The sampling process of ADCs creates a sampling transient that is caused by the switching-in of the ADC sampling capacitor. The switching-in of this sampling capacitor momentarily "shorts" the output of the amplifier as charge is transferred between amplifier and sampling capacitor. The amplifier must recover and settle from this load transient before this acquisition period has ended, for a valid representation of the input signal. The LTC6601 will settle much more quickly from these periodic load impulses than it does from a 2V input step, but it is a good idea to add an RC network after the outputs of the LTC6601 to decouple the sampling transient of the ADC (See Figure 6). The capacitance of the decoupling network serves to provide the bulk of the charge during the sampling process, while the two resistors of the filter network are used to dampen and attenuate any transient induced by the ADC. The ADC's sampling bandwidth will often be much greater than that of the LTC6601, so having this discrete RC filter will give the additional benefit of band limiting broadband output noise.

The selection of the RC time constant is trial and error for a given ADC, but the following guidelines are recommended. Choose an RC pole frequency greater than the cutoff frequency of the LTC6601. 80MHz RC filters are good for filtering broadband noise. Lower frequency RC filters improve SNR at the expense of settling time. The resistors in the decoupling network should be at least 25Ω. Too much resistance in the decoupling network leaves insufficient settling time and will create a voltage divider between the dynamic input impedance of the ADC and the decoupling resistors. Using insufficient resistance might prevent proper dampening of the load transient caused by the sampling process, and prolong the time required for settling. In 16-bit applications, this will typically require a minimum of 11 RC time constants. It is recommended that the capacitor is chosen with low dielectric absorption (such as a C0G multilayer ceramic capacitor).

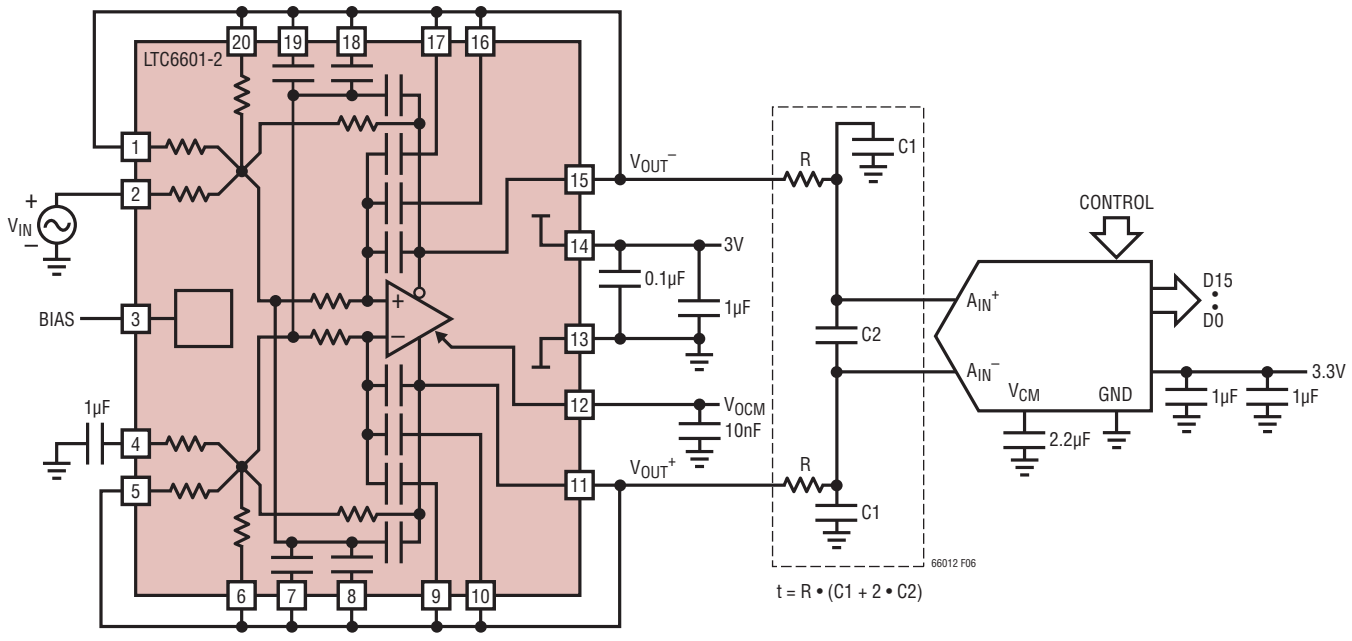

Figure 6. Interfacing the LTC6601 to A/D Converters

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A GALLERY OF BASIC FILTER TOPOLOGIES

Tables 2 through 10 list (sorted by Gain) a hundred possible filter topologies that can be easily implemented with the LTC6601. The tables also list the LTC6601-2 approximate midband (1MHz) spot noise e_{in} referred to the input resistor, R1 (with the BIAS pin pulled to V^+). The gains for these topologies range from 1V/V to 7V/V. The Qs listed are within the range of 0.54 and 1.72. The f_0s listed are in the range of 6.96MHz and 22.71MHz, and the –3dB frequencies listed range from 5.5MHz to 27.5MHz. For all filters listed, R3 = 125Ω. Figures 7 to 10 show how to pin-strap each filter configuration.

Table 2. Gain of 7 Filter Configurations

GAIN									
V/V	dB	f_0 (MHz)	f_{-3dB} (MHz)	Q	R1 (Ω)	R2 (Ω)	C1 (pF)	C2 (pF)	e_{in} (nV/√Hz)
7.0	16.902	10.38	7.43	0.539	57.14	400.00	48.2	97.6	6.1
7.0	16.902	9.57	10.36	0.771	57.14	400.00	48.2	114.8	6.1
7.0	16.902	8.96	12.10	1.175	57.14	400.00	48.2	130.9	6.1
7.0	16.902	8.12	7.49	0.656	57.14	400.00	58.75	130.9	6.1

Table 3. Gain of 6 Filter Configurations

GAIN									
V/V	dB	f_0 (MHz)	f_{-3dB} (MHz)	Q	R1 (Ω)	R2 (Ω)	C1 (pF)	C_2 (pF)	e_{in} (nV/√Hz)
6.0	15.563	10.38	10.03	0.684	66.67	400.00	48.2	97.6	6.2
6.0	15.563	9.57	12.52	1.071	66.67	400.00	48.2	114.8	6.2
6.0	15.563	8.67	7.67	0.634	66.67	400.00	58.75	114.8	6.2
6.0	15.563	8.12	9.59	0.870	66.67	400.00	58.75	130.9	6.2
6.0	15.563	7.47	6.07	0.592	66.67	400.00	69.3	130.9	6.2

Table 4. Gain of 5 Filter Configurations

GAIN									
V/V	dB	f_0 (MHz)	f_{-3dB} (MHz)	Q	R1 (Ω)	R2 (Ω)	C1 (pF)	C2 (pF)	e_{in} nV/√Hz
5.0	13.979	11.36	9.67	0.614	80.00	400.00	48.2	81.5	6.5
5.0	13.979	10.38	12.78	0.936	80.00	400.00	48.2	97.6	6.5
5.0	13.979	9.40	7.67	0.594	80.00	400.00	58.75	97.6	6.5
5.0	13.979	8.67	10.07	0.849	80.00	400.00	58.75	114.8	6.5
5.0	13.979	8.12	11.25	1.290	80.00	400.00	58.75	130.9	6.5
5.0	13.979	7.98	6.46	0.591	80.00	400.00	69.3	114.8	6.5
5.0	13.979	7.47	8.16	0.779	80.00	400.00	69.3	130.9	6.5
5.0	13.979	6.96	5.50	0.579	80.00	400.00	79.85	130.9	6.5

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Table 5. Gain of 4 Filter Configurations

GAIN									
V/V	dB	f_0 (MHz)	f_{-3dB} MHz	Q	R1 (Ω)	R2 (Ω)	C1 (pF)	C2 (pF)	e_{in} nV/√Hz
4.0	12.041	11.36	13.05	0.834	100.00	400.00	48.2	81.5	6.8
4.0	12.041	10.38	14.80	1.480	100.00	400.00	48.2	97.6	6.8
4.0	12.041	9.40	10.47	0.799	100.00	400.00	58.75	97.6	6.8
4.0	12.041	8.67	12.00	1.284	100.00	400.00	58.75	114.8	6.8
4.0	12.041	8.65	6.76	0.575	100.00	400.00	69.3	97.6	6.8
4.0	12.041	7.98	8.84	0.794	100.00	400.00	69.3	114.8	6.8
4.0	12.041	7.43	6.09	0.596	100.00	400.00	79.85	114.8	6.8
4.0	12.041	7.47	10.00	1.141	100.00	400.00	69.3	130.9	6.8
4.0	12.041	6.96	7.57	0.775	100.00	400.00	79.85	130.9	6.8

Table 6. Gain of 3 Filter Configurations

GAIN									
V/V	dB	f_0 (MHz)	f_{-3dB} (MHz)	Q	R1 (Ω)	R2 (Ω)	C1 (pF)	C2 (pF)	e_{in} (nV/√Hz)
3.0	9.542	16.06	12.36	0.568	66.67	200.00	48.2	81.5	7.1
3.0	9.542	14.68	15.74	0.763	66.67	200.00	48.2	97.6	7.1
3.0	9.542	13.53	17.83	1.091	66.67	200.00	48.2	114.8	7.1
3.0	9.542	13.29	9.88	0.554	66.67	200.00	58.75	97.6	7.1
3.0	9.542	12.26	12.39	0.715	66.67	200.00	58.75	114.8	7.1
3.0	9.542	11.36	15.77	1.300	133.33	400.00	48.2	81.5	7.4
3.0	9.542	11.48	14.07	0.928	66.67	200.00	58.75	130.9	7.1
3.0	9.542	11.29	8.34	0.552	66.67	200.00	69.3	114.8	7.1
3.0	9.542	10.29	11.04	0.763	133.33	400.00	58.75	81.5	7.4
3.0	9.542	10.57	10.06	0.674	66.67	200.00	69.3	130.9	7.1
3.0	9.542	9.40	12.85	1.224	133.33	400.00	58.75	97.6	7.4
3.0	9.542	8.65	9.54	0.788	133.33	400.00	69.3	97.6	7.4
3.0	9.542	8.06	6.69	0.601	133.33	400.00	79.85	97.6	7.4
3.0	9.542	7.98	10.88	1.212	133.33	400.00	69.3	114.8	7.4
3.0	9.542	7.43	8.48	0.825	133.33	400.00	79.85	114.8	7.4
3.0	9.542	6.96	9.40	1.172	133.33	400.00	79.85	130.9	7.4
3.0	9.542	9.85	7.13	0.544	66.67	200.00	79.85	130.9	7.1

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Table 7. Gain of 2 Filter Configurations

GAIN									
V/V	dB	f_0 (MHz)	f_{-3dB} (MHz)	Q	R1 (Ω)	R2 (Ω)	C1 (pF)	C2 (pF)	e_{in} (nV/√Hz)
2.0	6.021	16.06	18.95	0.868	100.00	200.00	48.2	81.5	8.1
2.0	6.021	14.55	12.69	0.626	100.00	200.00	58.75	81.5	8.1
2.0	6.021	14.68	20.46	1.323	100.00	200.00	48.2	97.6	8.1
2.0	6.021	13.29	15.34	0.840	100.00	200.00	58.75	97.6	8.1
2.0	6.021	12.24	10.96	0.640	100.00	200.00	69.3	97.6	8.1
2.0	6.021	12.26	16.66	1.200	100.00	200.00	58.75	114.8	8.1
2.0	6.021	11.29	12.98	0.835	100.00	200.00	69.3	114.8	8.1
2.0	6.021	10.29	13.97	1.197	200.00	400.00	58.75	81.5	8.5
2.0	6.021	10.51	9.76	0.660	100.00	200.00	79.85	114.8	8.1
2.0	6.021	10.57	13.97	1.102	100.00	200.00	69.3	130.9	8.1
2.0	6.021	9.47	10.52	0.796	200.00	400.00	69.3	81.5	8.5
2.0	6.021	9.85	11.17	0.819	100.00	200.00	79.85	130.9	8.1
2.0	6.021	8.82	7.55	0.616	200.00	400.00	79.85	81.5	8.5
2.0	6.021	8.65	11.91	1.254	200.00	400.00	69.3	97.6	8.5
2.0	6.021	8.06	9.48	0.864	200.00	400.00	79.85	97.6	8.5
2.0	6.021	7.43	10.40	1.341	200.00	400.00	79.85	114.8	8.5

Table 8. Gain of 1.667 Filter Configurations

GAIN									
V/V	dB	f_0 (MHz)	f_{-3dB} MHz	Q	R1 (Ω)	R2 (Ω)	C1 (pF)	C2 (pF)	e_{in} nV/√Hz
1.667	4.437	19.67	19.35	0.696	80.00	133.33	48.2	81.5	8.5
1.667	4.437	17.97	22.12	0.934	80.00	133.33	48.2	97.6	8.5
1.667	4.437	16.57	23.16	1.336	80.00	133.33	48.2	114.8	8.5
1.667	4.437	16.28	15.60	0.679	80.00	133.33	58.75	97.6	8.5
1.667	4.437	15.01	17.80	0.875	80.00	133.33	58.75	114.8	8.5
1.667	4.437	14.33	18.58	1.046	80.00	133.33	58.75	126	8.5
1.667	4.437	13.82	13.19	0.676	80.00	133.33	69.3	114.8	8.5
1.667	4.437	12.94	14.77	0.826	80.00	133.33	69.3	130.9	8.5
1.667	4.437	12.06	11.32	0.666	80.00	133.33	79.85	130.9	8.5

APPLICATIONS INFORMATION

Table 9. Gain of 1.333 Filter Configurations

GAIN									
V/V	dB	f_0 (MHz)	f_{-3dB} MHz	Q	R1 (Ω)	R2 (Ω)	C1 (pF)	C2 (pF)	e_{in} nV/√Hz
1.333	2.499	19.67	22.73	0.841	100.00	133.33	48.2	81.5	9.4
1.333	2.499	17.82	15.77	0.633	100.00	133.33	58.75	81.5	9.4
1.333	2.499	17.97	24.34	1.185	100.00	133.33	48.2	97.6	9.4
1.333	2.499	16.28	18.44	0.818	100.00	133.33	58.75	97.6	9.4
1.333	2.499	14.99	13.58	0.646	100.00	133.33	69.3	97.6	9.4
1.333	2.499	15.01	19.82	1.097	100.00	133.33	58.75	114.8	9.4
1.333	2.499	14.06	20.12	1.506	100.00	133.33	58.75	130.9	9.4
1.333	2.499	13.82	15.61	0.814	100.00	133.33	69.3	114.8	9.4
1.333	2.499	12.88	12.03	0.663	100.00	133.33	79.85	114.8	9.4
1.333	2.499	12.94	16.64	1.025	100.00	133.33	69.3	130.9	9.4
1.333	2.499	12.06	13.45	0.801	100.00	133.33	79.85	130.9	9.4

Table 10. Gain of 1 Filter Configurations

GAIN									
V/V	dB	f_0 (MHz)	f_{-3dB} MHz	Q	R1 (Ω)	R2 (Ω)	C1 (pF)	C2 (pF)	e_{in} nV/√Hz
1.0	0.0	22.71	25.40	0.804	100.0	100.0	48.2	81.5	10.7
1.0	0.0	20.75	27.23	1.079	100.0	100.0	48.2	97.6	10.7
1.0	0.0	20.57	17.86	0.623	100.0	100.0	58.75	81.5	10.7
1.0	0.0	19.14	27.50	1.543	100.0	100.0	48.2	114.8	10.7
1.0	0.0	18.80	20.62	0.784	100.0	100.0	58.75	97.6	10.7
1.0	0.0	17.31	15.35	0.634	100.0	100.0	69.3	97.6	10.7
1.0	0.0	17.33	22.15	1.011	100.0	100.0	58.75	114.8	10.7
1.0	0.0	16.23	22.58	1.312	100.0	100.0	58.75	130.9	10.7
1.0	0.0	15.96	17.45	0.781	100.0	100.0	69.3	114.8	10.7
1.0	0.0	14.55	19.09	1.079	200.0	200.0	58.75	81.5	11
1.0	0.0	14.87	13.57	0.650	100.0	100.0	79.85	114.8	10.7
1.0	0.0	14.95	18.59	0.954	100.0	100.0	69.3	130.9	10.7
1.0	0.0	13.39	14.90	0.798	200.0	200.0	69.3	81.5	11
1.0	0.0	13.92	15.04	0.769	100.0	100.0	79.85	130.9	10.7
1.0	0.0	12.48	11.38	0.650	200.0	200.0	79.85	81.5	11
1.0	0.0	12.24	16.25	1.115	200.0	200.0	69.3	97.6	11
1.0	0.0	11.40	13.27	0.850	200.0	200.0	79.85	97.6	11
1.0	0.0	11.29	16.47	1.715	200.0	200.0	69.3	114.8	11
1.0	0.0	10.51	14.17	1.167	200.0	200.0	79.85	114.8	11
1.0	0.0	9.47	13.26	1.350	400.0	400.0	69.3	81.5	11.8
1.0	0.0	8.82	10.86	0.935	400.0	400.0	79.85	81.5	11.8
1.0	0.0	8.06	11.57	1.535	400.0	400.0	79.85	97.6	11.8

APPLICATIONS INFORMATION

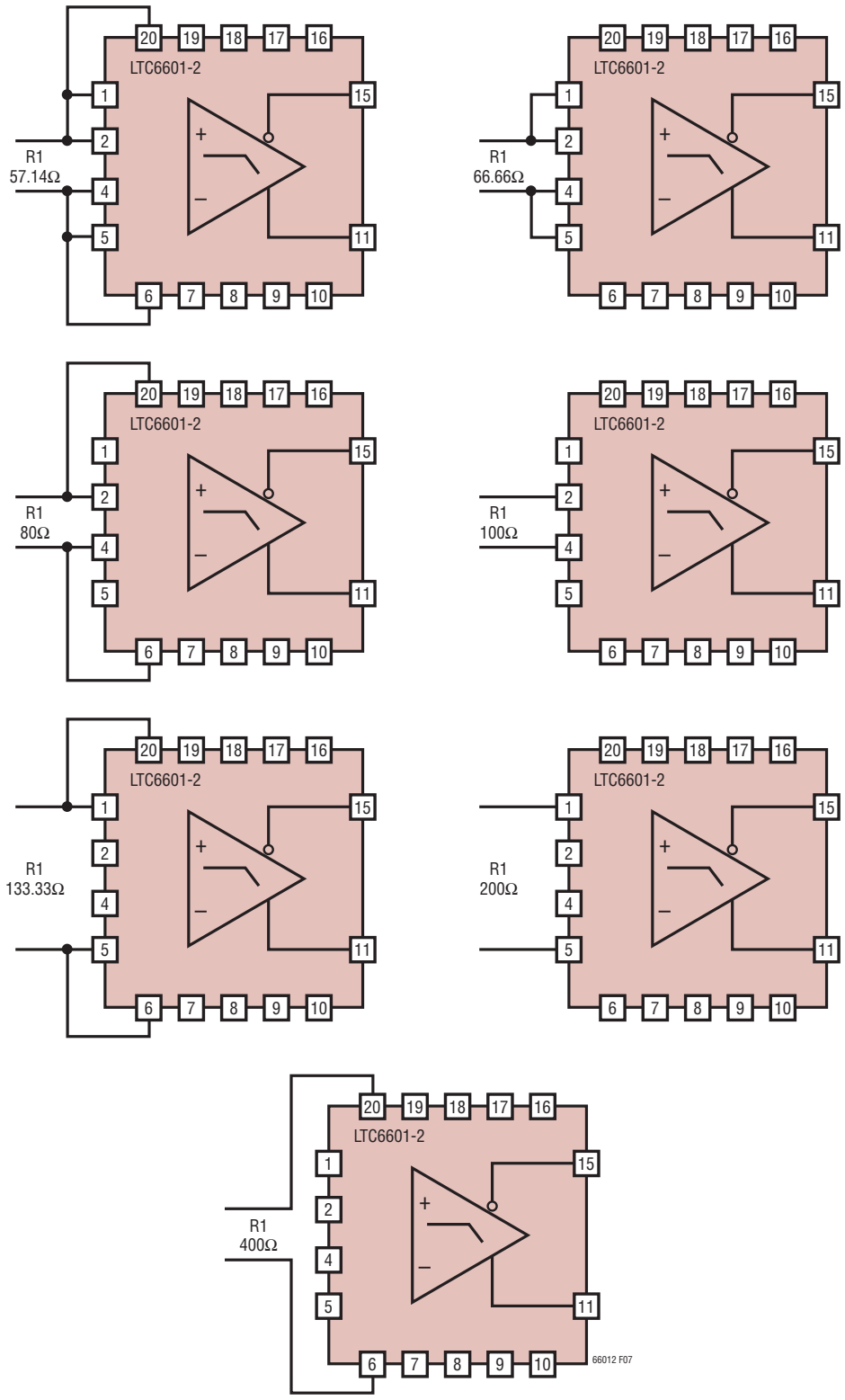


Figure 7. Pin-Strap Hookup for a Particular R1

APPLICATIONS INFORMATION

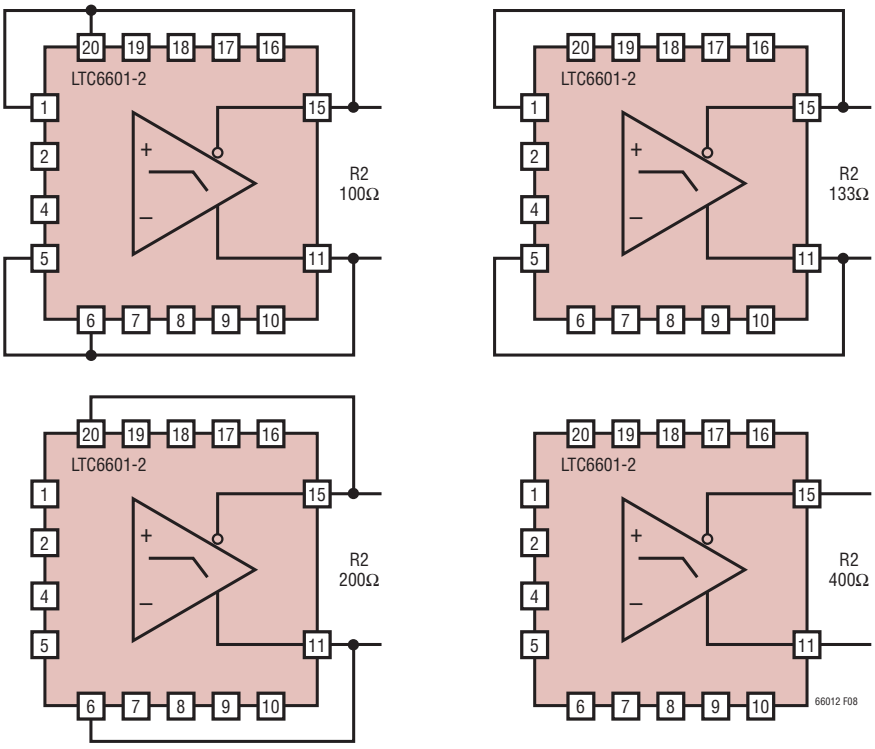


Figure 8. Pin-Strap Hookup for a Particular R2

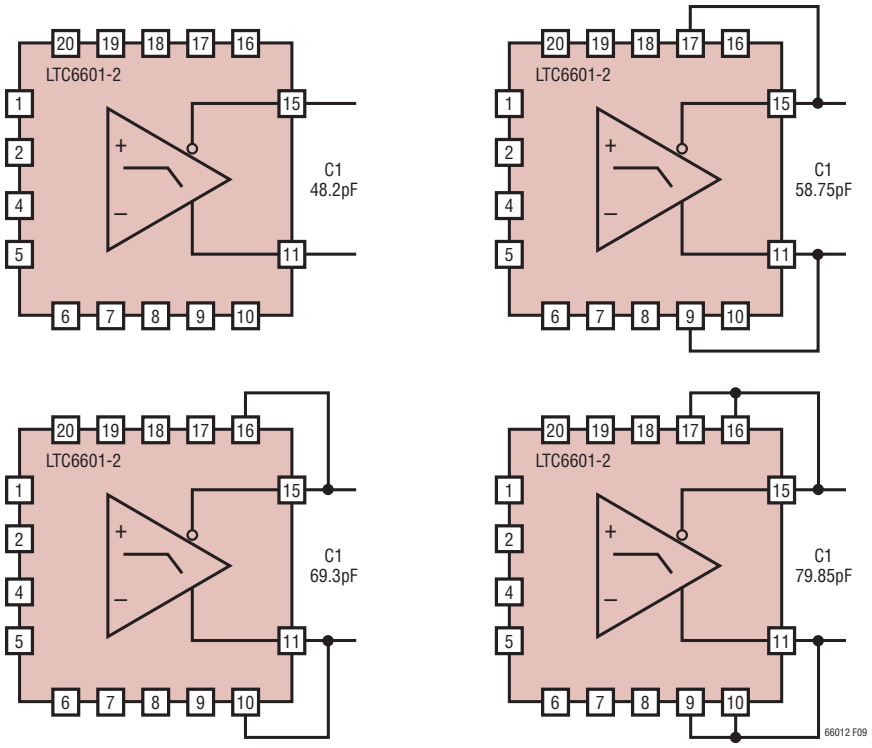


Figure 9. Pin-Strap Hookup for a Particular C1

APPLICATIONS INFORMATION

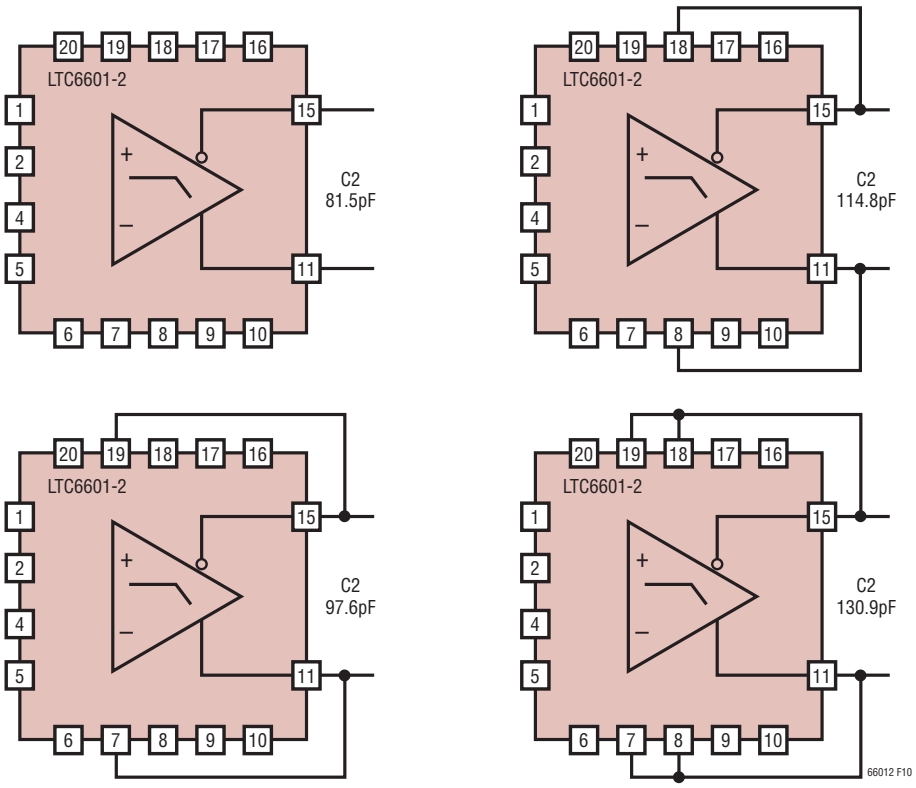


Figure 10. Pin-Strap Hookup for a Particular C2

APPLICATIONS INFORMATION

Example Filter Configurations of Basic 2nd Order Filters

Figure 11 shows some simplified component hookups of a selection of filters taken from Tables 7, 9 and 10. For simplicity, V_{OCM} pin bypass and power supply bypass are not shown.

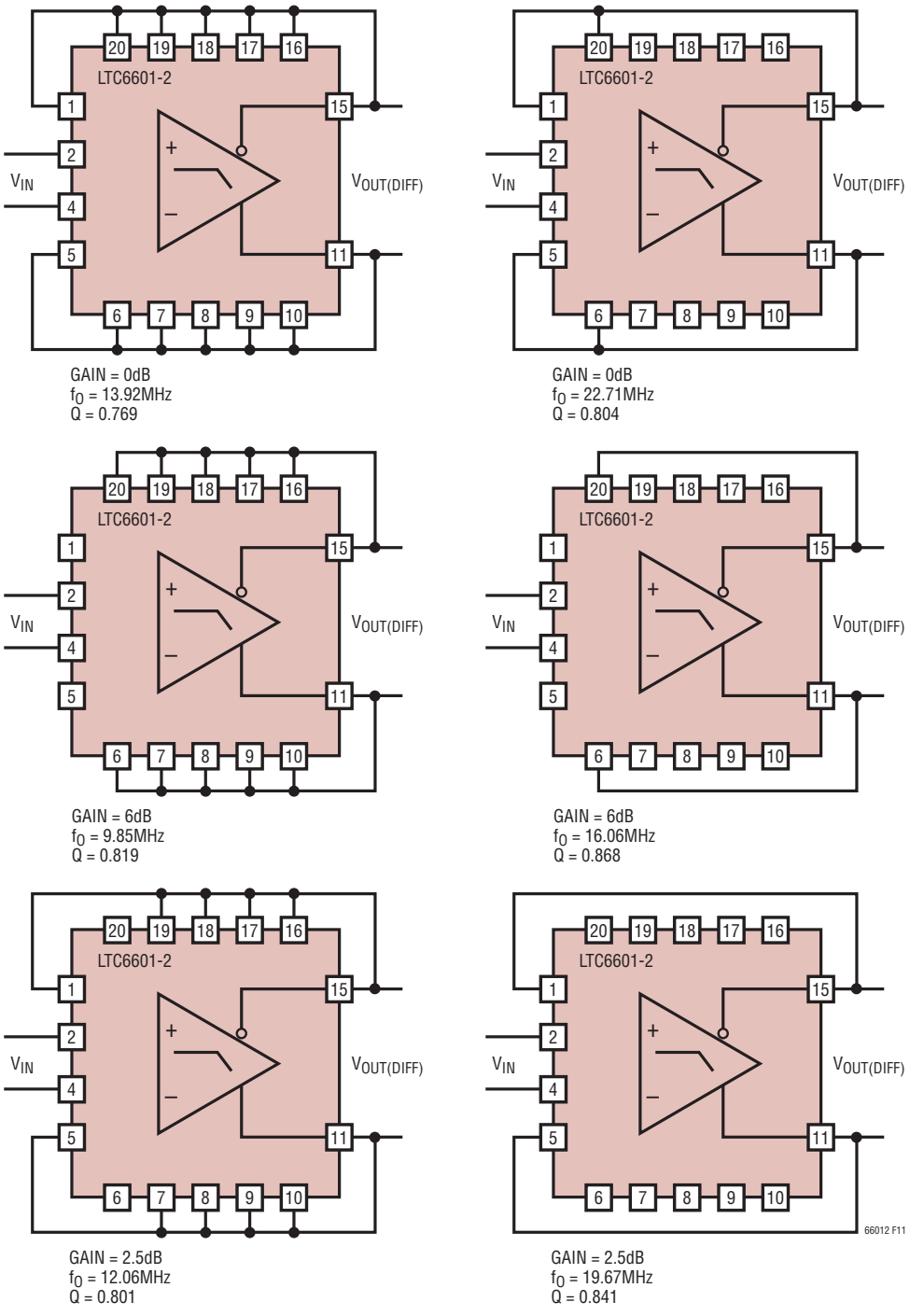


Figure 11. Basic 2nd Order Filter Configurations

APPLICATIONS INFORMATION

Figure 12 shows some simplified component hookups of a selection of filters taken from Tables 4, 5, and 6. For simplicity, V_{OCM} pin bypass and power supply bypass are not shown.

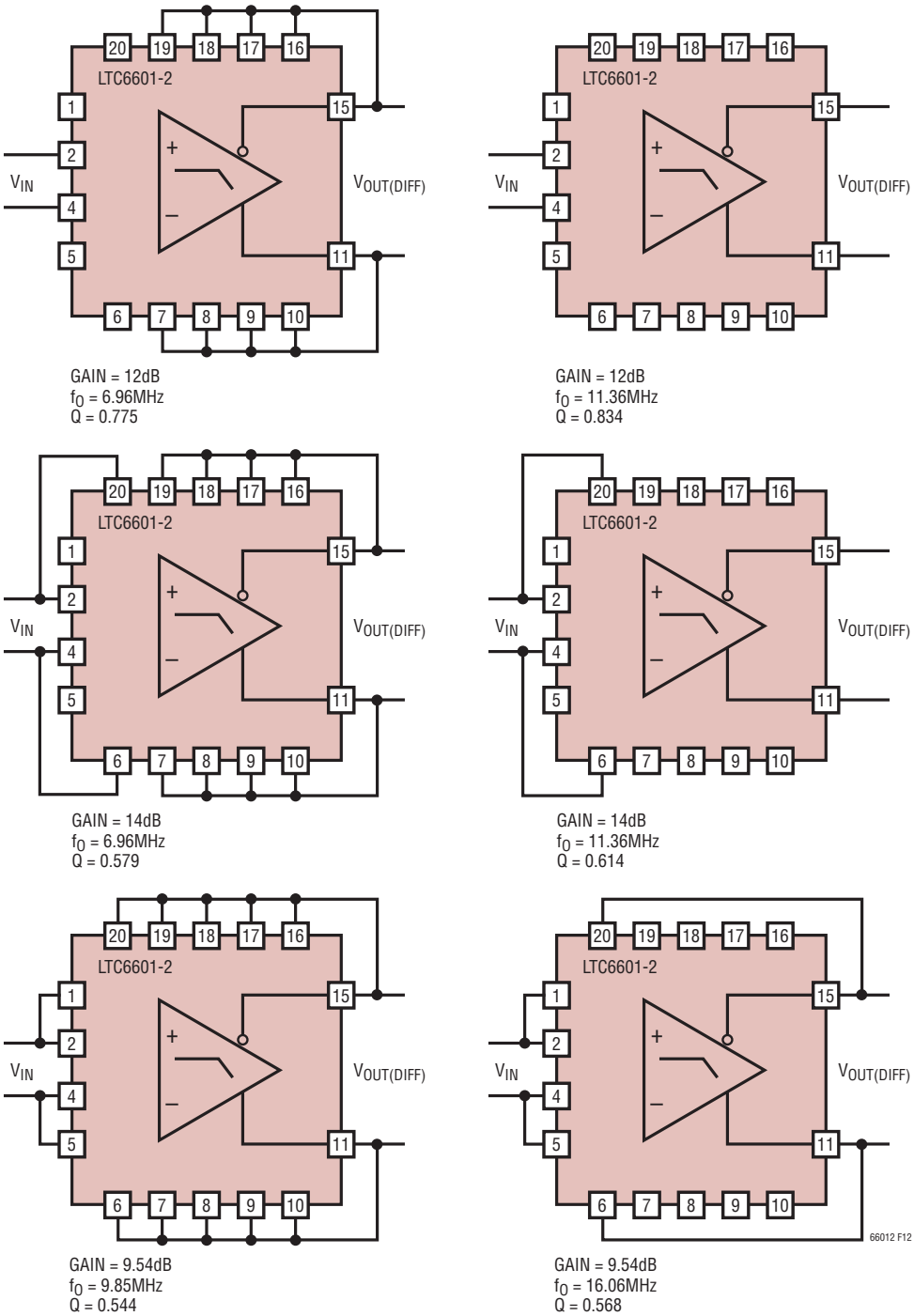


Figure 12. Basic 2nd Order Filter Configurations

APPLICATIONS INFORMATION

COMPLEX FILTER CONFIGURATIONS

A Modified 2nd Order Lowpass Filter Topology

The basic filter topology of Figure 3 can be modified as shown in Figure 13. The Figure 13 circuit includes an impedance path between the two summing nodes (the circuit nodes common to resistors R1, R2 and R3). A resistor and/or a capacitor connection between the summing nodes provide even more flexibility, and enhance the filter design options (the f_O and Q equations shown in Figure 13 reduce to equations of Figure 3 if C3 is zero and R4 is infinite).

The modified second order filter topology provides for setting the Q value (with R4) without changing the f_O value and increasing the passband gain to greater than one without changing the Q value (in the Q equation of Figure 13 the value of Q does not change if the value of the [1 + GAIN + 2(R2/R4)] denominator factor does not change). Using R4 to set the Q value allows the option to design the –3dB frequency (f_{3dB}). If the Q value varies and the f_O value is constant then the f_{3dB} frequency varies in a second order lowpass function (refer to the f_{3dB} equation of Figure 13).

Figures 14 to 17 show additional circuits highlighting the use of R4 or C3 in the modified second order cicuit to set the f_{3dB} frequency to 13MHz, 19MHz, 22.7MHz and 24.6MHz respectively.

The design procedure for a specified f_{3dB} frequency is as follows:

1 Using the chosen C1, C2 and C3 values calculate the f_O value.

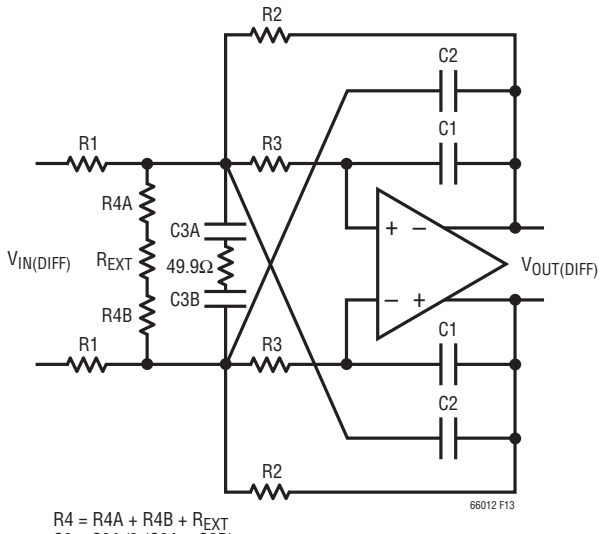
2. Using f_O of step 1 and the specified f_{3dB} calculate the Q value.

3. Calculate the R4 value using the Q value of step 3.

4. Calculate the required external resistor R_{EXT} value for the R4 value in step 3. Example, in Figure 14 the Q value for f_{3dB} = 5MHz is 0.54, the required R4 resistor is 350Ω, the R4A and R4B resistors are the internal 100Ω and the R_{EXT} resistor is 150Ω [R_{EXT} = R4 – (R4A + R4B)].

Note: The modified second order filter topology requires the use of at least two of the three input resistor pairs (two of the three 400Ω, 200Ω and 100Ω pairs).

APPLICATIONS INFORMATION



R4 = R4A + R4B + R_{EXT}
C3 = C3A/2 (C3A = C3B)

$$f_{3dB} = \frac{f_0 \bullet \sqrt{\left(6089 \bullet \sqrt{\left(3568 \bullet Q^4 - 1788 \bullet Q^2 + 447\right) + 1.287 \bullet 10^5 \bullet \left(2 \bullet Q^2 - 1\right)}\right)}}{507.6 \bullet Q}$$

$$Q = \frac{0.2236 \bullet f_0 \bullet \sqrt{\left(2.109 \bullet 10^5 \bullet \sqrt{\left(9.891 \bullet 10^{12} \bullet {f_{3dB}}^4 - 5.486 \bullet 10^9 \bullet {f_0}^4\right) + 120 \bullet \left(5.526 \bullet 10^9 \bullet {f_{3dB}}^2 + 3.082 \bullet 10^6 \bullet {f_0}^2\right)}\right)}}{\sqrt{\left(16 \bullet {f_0}^2 \bullet \left(8.29 \bullet 10^9 \bullet {f_{3dB}}^2 + 4.127 \bullet 10^9 \bullet {f_0}^2\right) - 6.638 \bullet 10^{10} \bullet {f_{3dB}}^4\right)}}$$

$$R4 = \frac{1.25 \bullet 10^4 \bullet C1 \bullet Q \bullet R2}{559 \bullet C1 \bullet \sqrt{R2} \bullet \sqrt{\left(\frac{C2 + 2 \bullet C3}{C1}\right)} - 50 \bullet Q \bullet \left(C1 \bullet \left(125 \bullet GAIN + R2 + 125\right) - C2 \bullet R2\right)}$$

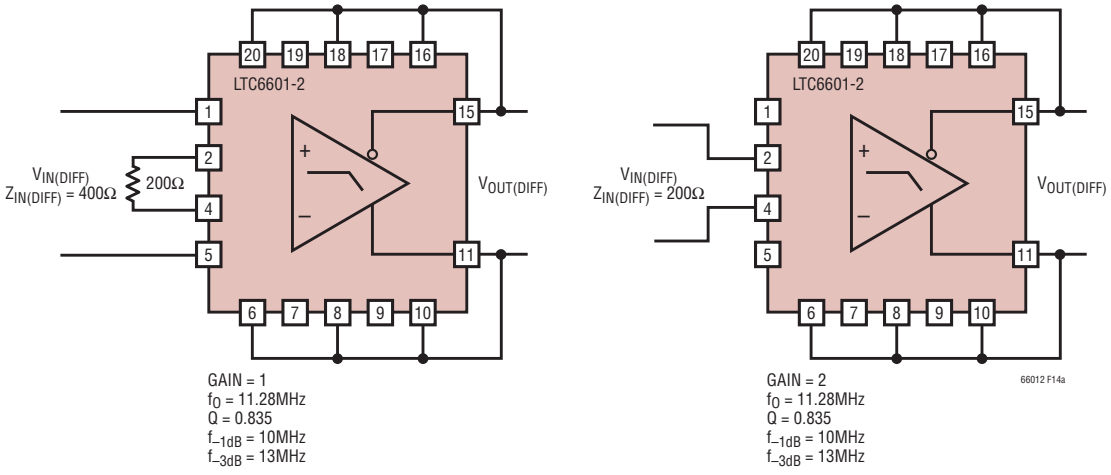
$$\frac{V_{OUT(DIFF)}}{V_{IN(DIFF)}} = -\frac{\frac{GAIN}{R2 \bullet R3 \bullet C1 \bullet (C2 + 2 \bullet C3)}}{S^2 + \frac{R1 \bullet \left(R2 \bullet \left(2 \bullet R3 + R4\right) + R3 \bullet R4\right) + R2 \bullet R3 \bullet R4}{R1 \bullet R2 \bullet R3 \bullet R4 \bullet (C2 + 2 \bullet C3)} \bullet S + \frac{1}{R2 \bullet R3 \bullet C1 \bullet (C2 + 2 \bullet C3)}}$$

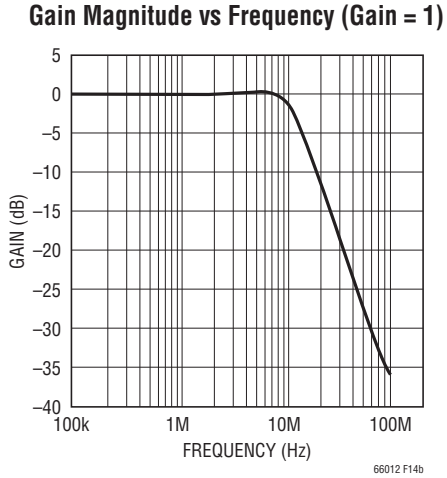
$$GAIN = -\frac{V_{OUT(DIFF)}}{V_{IN(DIFF)}} = -\frac{R2}{R1}$$

$$f_0 = \frac{1}{2 \bullet \pi \bullet \sqrt{R2 \bullet R3 \bullet C1 \bullet (C2 + 2 \bullet C3)}} \qquad Q = \frac{\sqrt{\left(\frac{R3}{R2}\right)} \bullet \sqrt{\left(\frac{C2}{C1} + 2 \bullet \frac{C3}{C1}\right)}}{1 + \left(1 + |GAIN| + 2 \bullet \frac{R2}{R4}\right) \bullet \frac{R3}{R2} - \frac{C2}{C1}}$$

Figure 13. Modified Filter Topology and Equations

APPLICATIONS INFORMATION





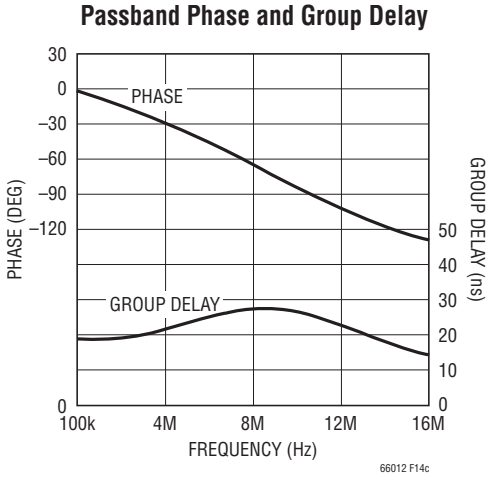
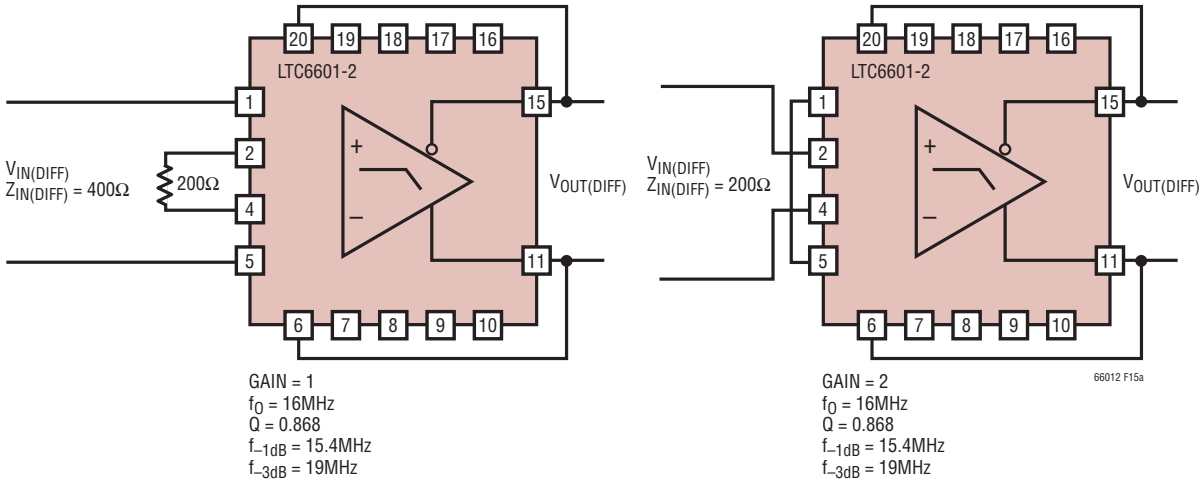
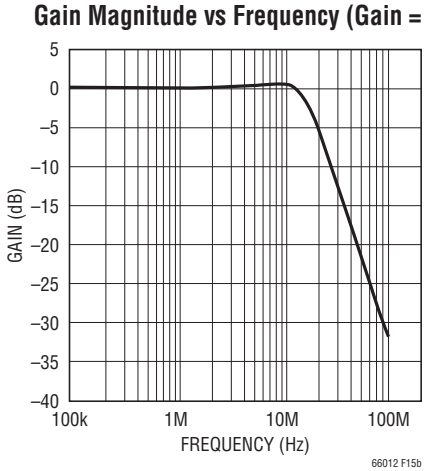


Figure 14. Modified Filter Configuration Using a Resistor Between Summing Nodes (f_{-3dB} = 13MHz)

APPLICATIONS INFORMATION





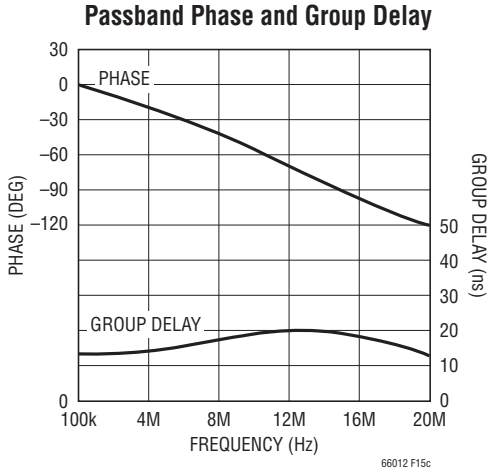
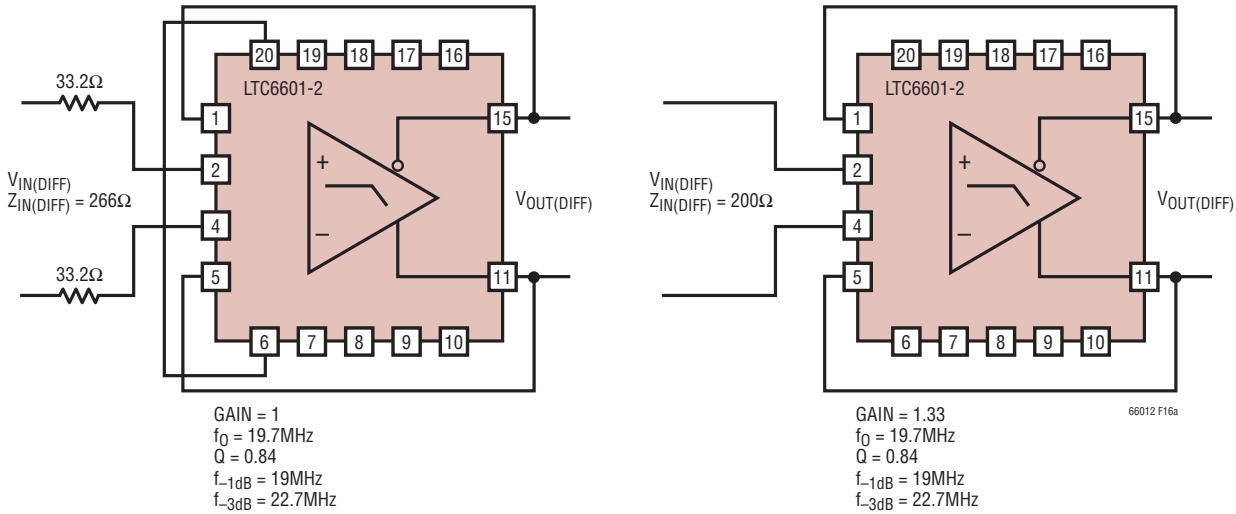
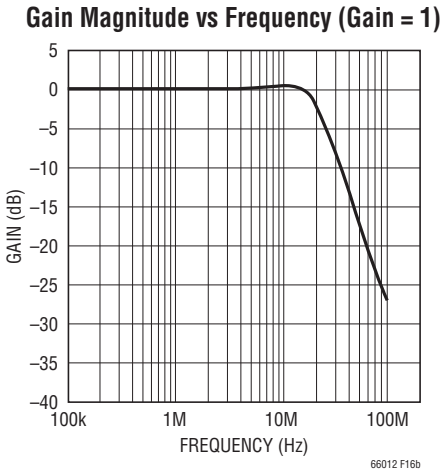


Figure 15. Modified Filter Configuration Using a Resistor Between Summing Nodes (f_{-3dB} = 19MHz)

APPLICATIONS INFORMATION





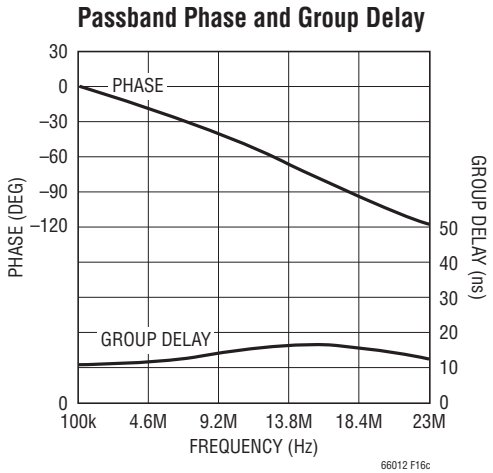
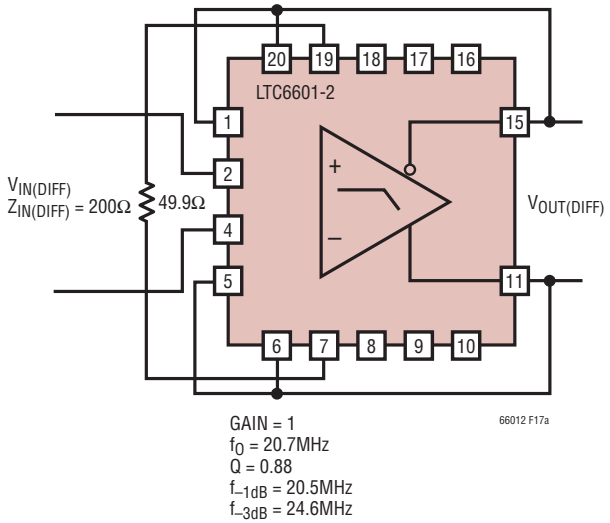
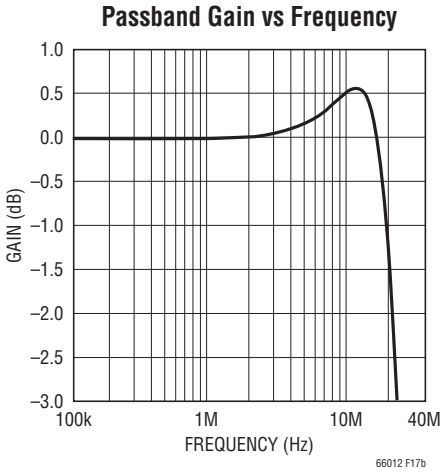


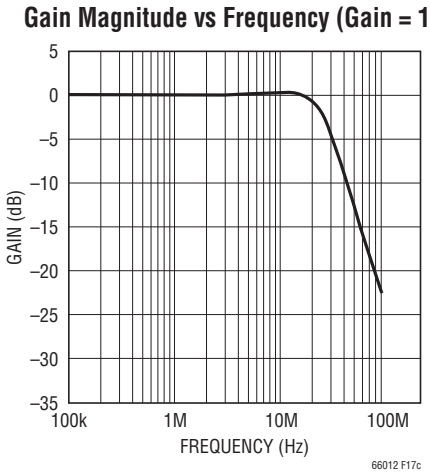
Figure 16. Modified Filter Configuration Using a Resistor Between Summing Nodes (f_{-3dB} = 22.7MHz)

APPLICATIONS INFORMATION



GAIN = 1
f_O = 20.7MHz
Q = 0.88
$f_{–1dB}$ = 20.5MHz
$f_{–3dB}$ = 24.6MHz





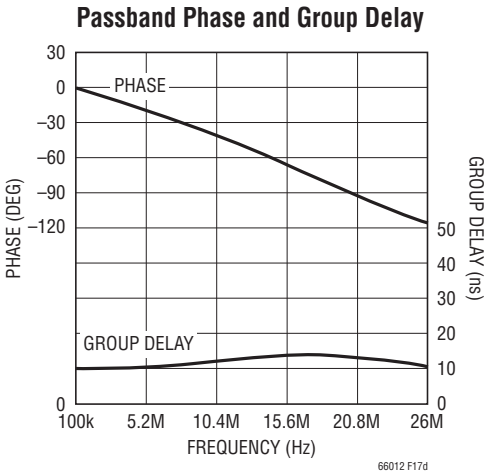


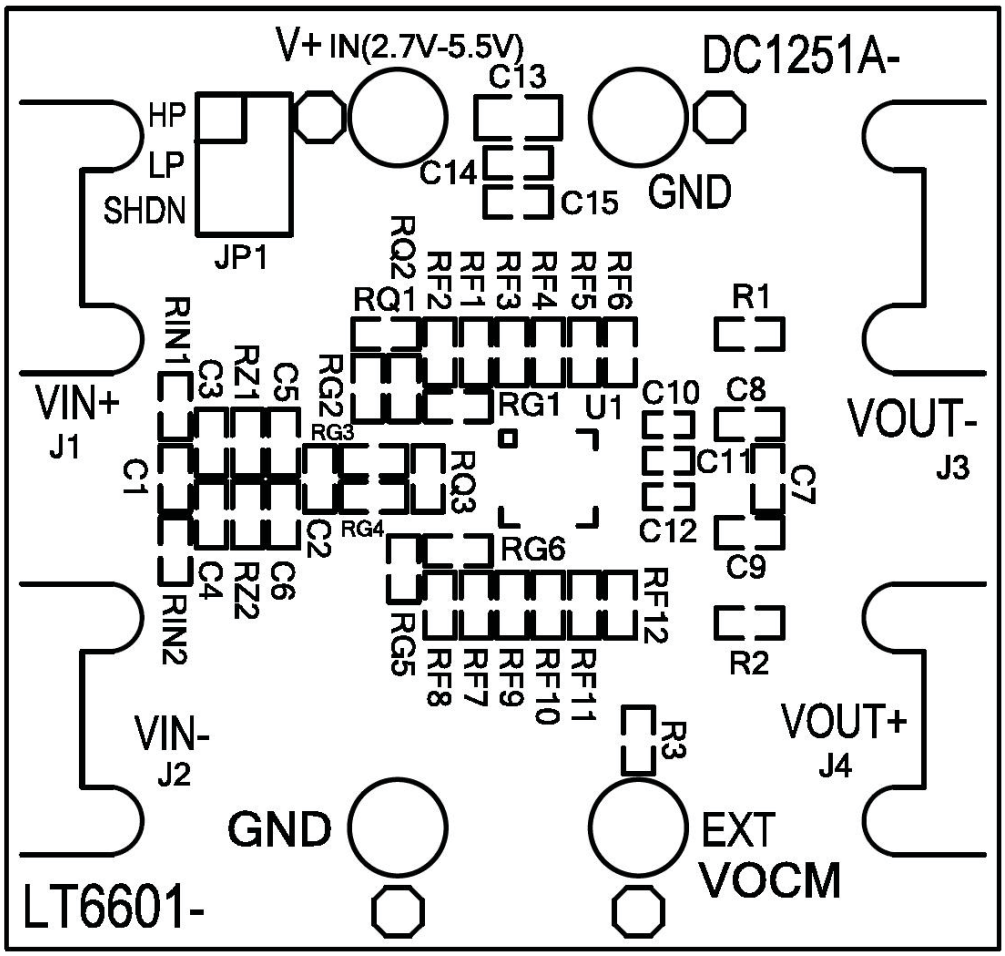
Figure 17. Modified Filter Configuration Using a Capacitor Between Summing Nodes ($f_{–3dB}$ = 24.6MHz)

APPLICATIONS INFORMATION

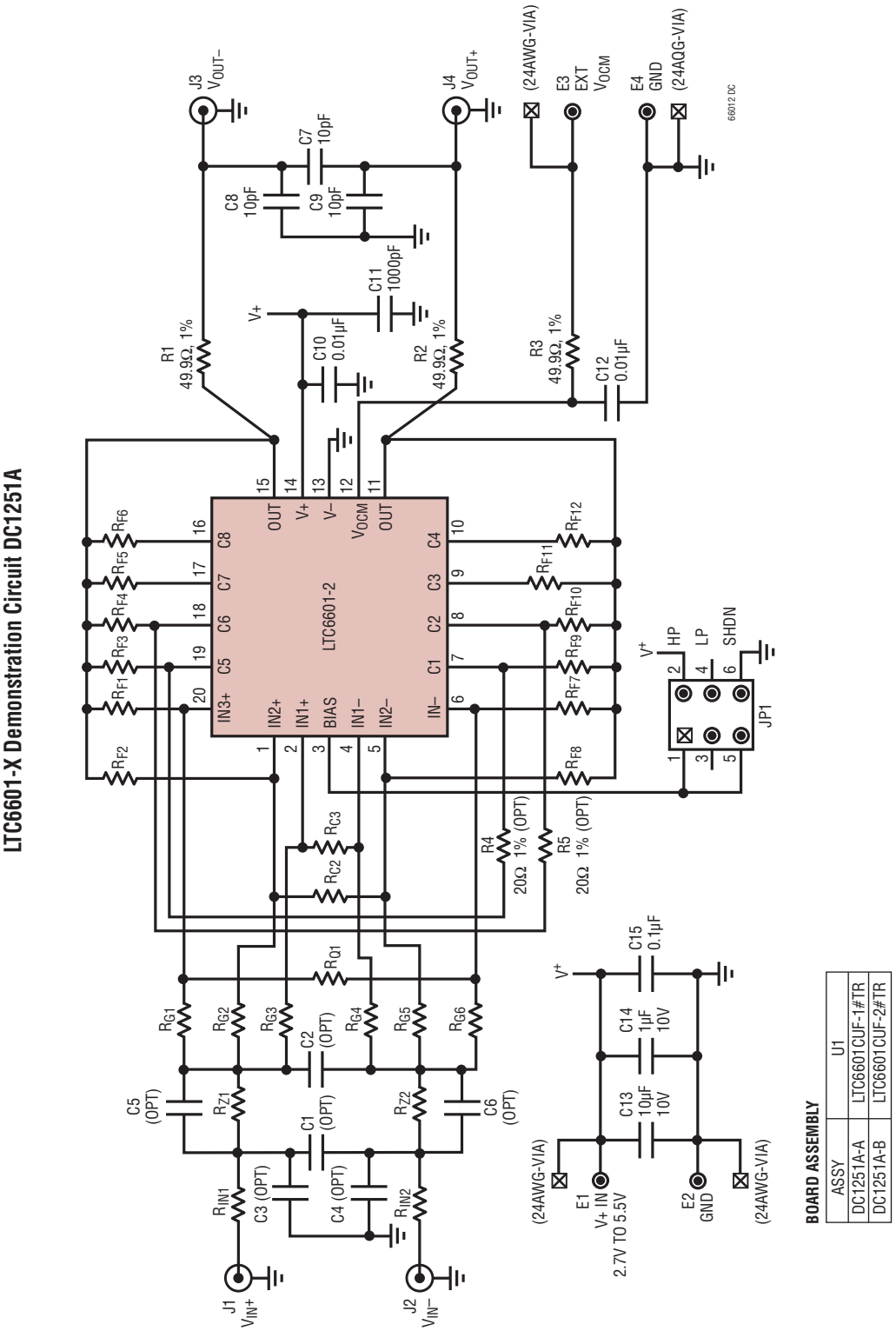
DC1251A Demonstration Board

The DC1251A demonstration circuit contains an LTC6601-2 (DC1251A-B). On a DC1251A the LTC6601 programming pins can be connected through 0603 resistor jumpers. In addition, optional surface mount capacitors and inductors at the LTC6601 input and/or output can be installed for additional filtering (a lowpass filter up to a 5th order can be implemented with a DC1251A demonstration circuit). The DC1251A has SMA connectors for the differential input and output of the LTC6601. An on board 106MHz lowpass RC filters the LTC6601 output.

DC1251A Top Silk Screen



APPLICATIONS INFORMATION

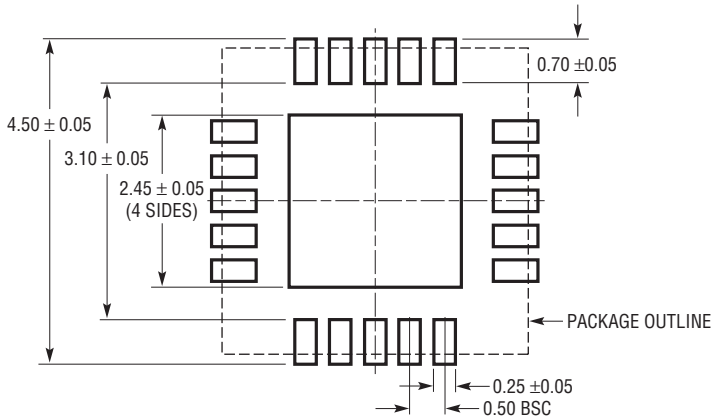


BOARD ASSEMBLY

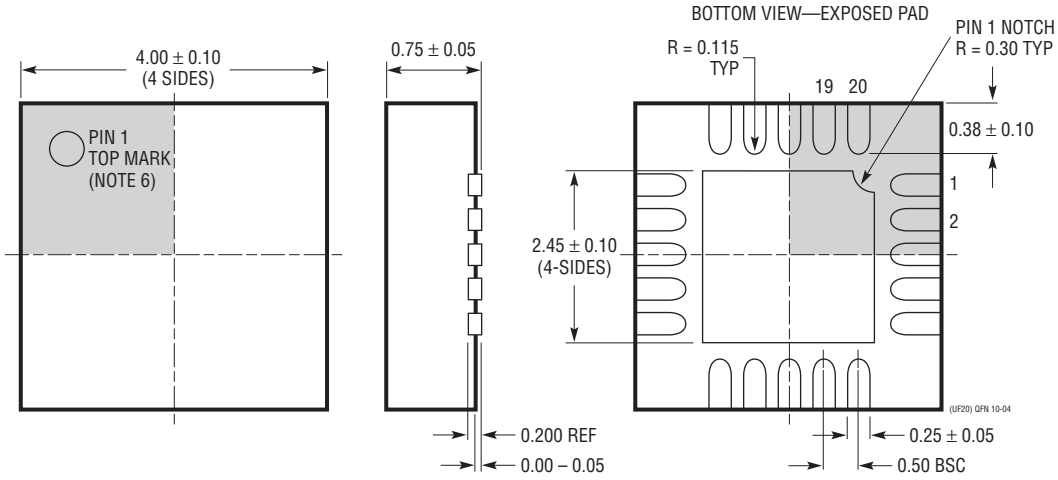
ASSY	U1
DC1251A-A	LTC6601CUF-1#TR
DC1251A-B	LTC6601CUF-2#TR

PACKAGE DESCRIPTION

UF Package
20-Lead Plastic QFN (4mm × 4mm)
(Reference LTC DWG # 05-08-1710)



RECOMMENDED SOLDER PAD PITCH AND DIMENSIONS

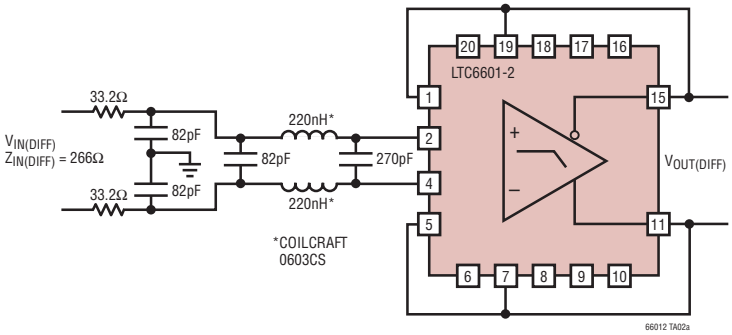


NOTE:
1. DRAWING IS PROPOSED TO BE MADE A JEDEC PACKAGE OUTLINE MO-220 VARIATION (WGGD-1)—TO BE APPROVED
2. DRAWING NOT TO SCALE
3. ALL DIMENSIONS ARE IN MILLIMETERS
4. DIMENSIONS OF EXPOSED PAD ON BOTTOM OF PACKAGE DO NOT INCLUDE MOLD FLASH. MOLD FLASH, IF PRESENT, SHALL NOT EXCEED 0.15mm ON ANY SIDE
5. EXPOSED PAD SHALL BE SOLDER PLATED
6. SHADED AREA IS ONLY A REFERENCE FOR PIN 1 LOCATION ON THE TOP AND BOTTOM OF PACKAGE

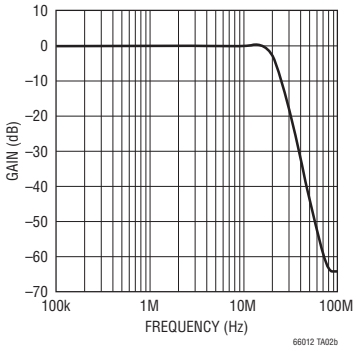
Information furnished by Linear Technology Corporation is believed to be accurate and reliable. However, no responsibility is assumed for its use. Linear Technology Corporation makes no representation that the interconnection of its circuits as described herein will not infringe on existing patent rights.

TYPICAL APPLICATION

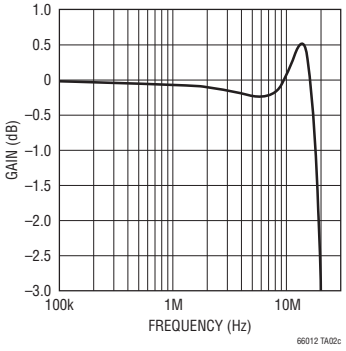
5th Order, 20MHz, Lowpass Filter



Gain Magnitude vs Frequency



Passband Gain vs Frequency



RELATED PARTS

PART NUMBER	DESCRIPTION	COMMENTS
LT®1568	Very Low Noise, High Frequency, Active RC, Filter Building Block	Up to 10MHz Filters, SNR = 92dB, THD = –84dBc at 2MHz
LT1993-2/LT1993-4/ LT1993-10	800MHz/900MHz/700MHz Low Distortion, Low Noise Differential Amplifier/ADC Driver	A_V = 2V/V / A_V = 4V/V / A_V = 10V/V, NF = 12.3dB/14.5dB/12.7dB, OIP3 = 38dBm/40dBm/40dBm at 70MHz
LT1994	Low Noise, Low Distortion Fully differential Input/Output Amplifier/Driver	Low Distortion, $2V_{P-P}$, 1MHz: –94dBc, 13mA, Low Noise: $3nV/\sqrt{Hz}$
LT6402-6/LT6402-12/ LT6402-20	300MHz Low Distortion, Low Noise Differential Amplifier/ ADC Driver	A_V = 6dB/A_V = 12dB/A_V = 20dB, NF = 18.6dB/15dB/12.4dB, OIP3 = 49dBm/43dBm/51dBm at 20MHz
LTC6404-1	Fully Differential Amplifier, GBW = 500MHz	Very Low Distortion, ($2V_{P-P}$, 10MHz): –91dBc
LTC6404-2	Fully Differential Amplifier, GBW = 900MHz	Very Low Distortion, ($2V_{P-P}$, 10MHz): –96dBc
LTC6404-4	Fully Differential Amplifier, GBW = 1700MHz	Very Low Distortion, ($2V_{P-P}$, 10MHz): –101dBc
LT6600-2.5/LT6600-5/ LT6600-10/LT6600-20	Very Low Noise, Fully Differential Amplifier and Filter	2.5MHz/5MHz/10MHz/20MHz Integrated Filter, 3V Supply, SO-8 Package
LTC6601-1	Low Noise, Pin-Configurable Filter	5MHz to 27MHz Bandwidth, Second Order Differential Filter
LTC6602	Dual, Matched Bandpass Filter	Programmable Gain and Bandwidth for RFID Applications (40kHz to 1MHz)
LTC6603	Dual, Matched Lowpass Filter	Programmable Gain and Bandwidth (25kHz to 2.5MHz)
LT6604-X	Dual, Matched Lowpass Filter	2.5MHz, 5MHz, 10MHz and 15MHz
LTC6605-X	Dual, Matched Lowpass Filter	7MHz, 10MHz and 14MHz

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