



**THE DATASHEET OF  
LTC4280CUFD#PBF**



## FEATURES

- Allows Safe Insertion into Live Backplane
- 8-Bit ADC Monitors Current and Voltage
- I<sup>2</sup>C/SMBus Interface
- Wide Operating Voltage Range: 2.9V to 15V
- Adjustable Overcurrent Filter Time
- High Side Drive for External N-Channel MOSFET
- No External Gate Capacitor Required
- Input Overvoltage/Undervoltage Protection
- Optional Latchoff or Auto-Retry After Faults
- Alerts Host After Faults
- Inrush Current Limit with Foldback
- Available in 24-Pin 4mm × 5mm QFN Package

## APPLICATIONS

- Live Board Insertion
- Electronic Circuit Breakers
- Computers, Servers
- Platform Management

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## DESCRIPTION

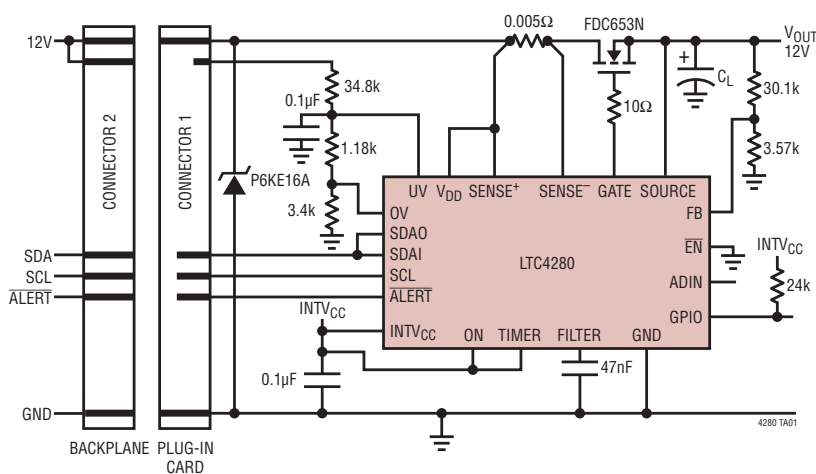
The LTC<sup>®</sup>4280 Hot Swap<sup>™</sup> controller allows a board to be safely inserted and removed from a live backplane. Using an external N-channel pass transistor, board supply voltage and inrush current are ramped up at an adjustable rate. An I<sup>2</sup>C interface and onboard ADC allow for monitoring of load current, voltage and fault status.

The device features adjustable analog foldback current limit and a FILTER pin which configures the time spent in overcurrent before declaring a fault. An I<sup>2</sup>C interface may configure the part to latch off or automatically restart after the LTC4280 detects a current limit fault.

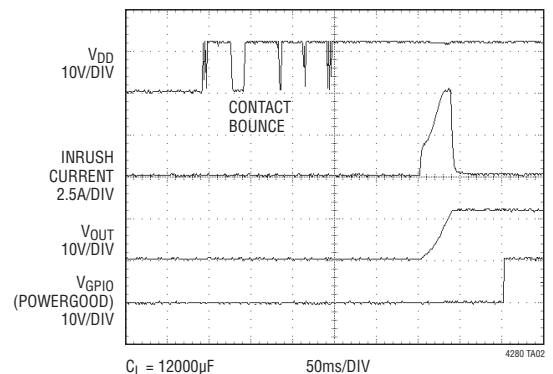
The controller has additional features to interrupt the host when a fault has occurred, notify when output power is good, detect insertion of a load card, and power-up either automatically upon insertion or wait for an I<sup>2</sup>C command to turn on.

## TYPICAL APPLICATION

12V Application with 5A Circuit Breaker



Start-Up Waveform



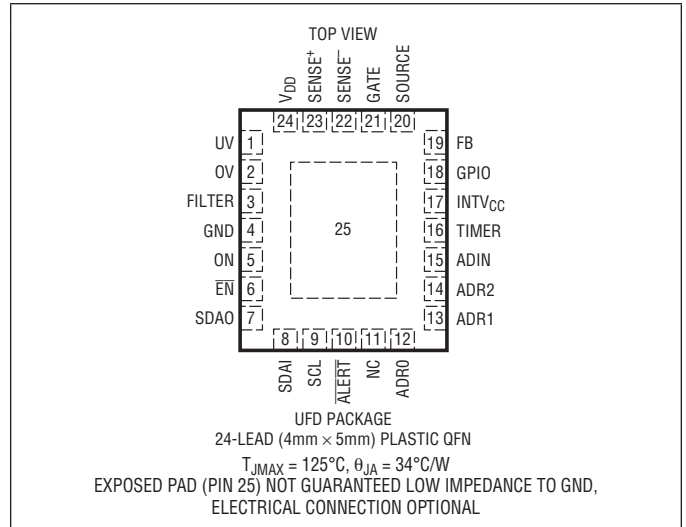
# LTC4280

## ABSOLUTE MAXIMUM RATINGS

(Notes 1, 2)

Supply Voltage ( $V_{DD}$ )	-0.3V to 24V
Supply Voltage ( $INTV_{CC}$ )	-0.3V to 6.5V
Input Voltages	
GATE-SOURCE (Note 3)	-0.3V to 5V
SENSE <sup>+</sup> , SENSE <sup>-</sup>	$V_{DD} - 0.3V$ to $V_{DD} + 0.3V$
SOURCE	-5V to 24V
$\overline{EN}$ , FB, ON, OV, UV	-0.3V to 12V
ADR0, ADR1, ADR2, TIMER, ADIN, FILTER	-0.3V to $INTV_{CC} + 0.3V$
ALERT SCL, SDA, SDAI, SDAO	-0.3V to 6.5V
Output Voltages	
GATE, GPIO	-0.3V to 24V
Operating Temperature Range	
LTC4280C	0°C to 70°C
LTC4280I	-40°C to 85°C
Storage Temperature Range	
SSOP	-65°C to 150°C
QFN	-65°C to 125°C
Lead Temperature (Soldering, 10 sec)	
SSOP	300°C

## PIN CONFIGURATION



## ORDER INFORMATION

LEAD FREE FINISH	TAPE AND REEL	PART MARKING*	PACKAGE DESCRIPTION	TEMPERATURE RANGE
LTC4280CUFD#PBF	LTC4280CUFD#TRPBF	4280	24-Lead (4mm × 5mm) Plastic QFN	0°C to 70°C
LTC4280IUFD#PBF	LTC4280IUFD#TRPBF	4280	24-Lead (4mm × 5mm) Plastic QFN	-40°C to 85°C
LEAD BASED FINISH	TAPE AND REEL	PART MARKING*	PACKAGE DESCRIPTION	TEMPERATURE RANGE
LTC4280CUFD	LTC4280CUFD#TR	4280	24-Lead (4mm × 5mm) Plastic QFN	0°C to 70°C
LTC4280IUFD	LTC4280IUFD#TR	4280	24-Lead (4mm × 5mm) Plastic QFN	-40°C to 85°C

Consult LTC Marketing for parts specified with wider operating temperature ranges. \*The temperature grade is identified by a label on the shipping container.

For more information on lead free part marking, go to: <http://www.linear.com/leadfree/>

For more information on tape and reel specifications, go to: <http://www.linear.com/tapeandreeel/>

## ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at  $T_A = 25^\circ\text{C}$ .  $V_{DD} = 12\text{V}$  unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
<b>Supplies</b>							
$V_{DD}$	Input Supply Range		●	2.9		15	V
$V_{OV(VDD)}$	Input Supply Overvoltage Threshold		●	15	15.6	16.5	V
$I_{DD}$	Input Supply Current		●		3	5	mA
$V_{DD(UVL)}$	Input Supply Undervoltage Lockout	$V_{DD}$ Rising	●	2.75	2.84	2.89	V
$V_{DD(HYST)}$	Input Supply Undervoltage Lockout Hysteresis		●	75	100	125	mV
$INTV_{CC}$	Internal Regulator Voltage	$V_{DD} \geq 3.3\text{V}$	●	2.9	3.1	3.4	V
$INTV_{CC(UVL)}$	$INTV_{CC}$ Undervoltage Lockout	$INTV_{CC}$ Rising	●	2.55	2.64	2.79	V
$INTV_{CC(HYST)}$	$INTV_{CC}$ Undervoltage Lockout Hysteresis		●	20	55	75	mV
<b>Current Limit and Circuit Breaker</b>							
$\Delta V_{SENSE(TH)}$	Circuit Breaker Threshold ( $V_{DD} - V_{SENSE}$ )		●	22.5	25	27.5	mV
$\Delta V_{SENSE}$	Current Limit Voltage ( $V_{DD} - V_{SENSE}$ )	$V_{FB} = 1.3\text{V}$ $V_{FB} = 0\text{V}$	● ●	22.5 7	26 10	29.5 13.5	mV mV
$I_{SENSE(IN)}$	SENSE +/- Input Current	$V_{SENSE} = 12\text{V}$	●	10	20	35	$\mu\text{A}$
<b>Gate Drive</b>							
$\Delta V_{GATE}$	External N-Channel Gate Drive ( $V_{GATE} - V_{SOURCE}$ ) (Note 3)	$V_{DD} = 2.9\text{V}$ to $15\text{V}$	●	4.7	5.9	6.5	V
$I_{GATE(UP)}$	External N-Channel Gate Pull-Up Current	Gate On, $V_{GATE} = 0\text{V}$	●	-15	-20	-30	$\mu\text{A}$
$I_{GATE(DN)SLOW}$	External N-Channel Gate Pulldown Current	Gate Off, $V_{GATE} = 15\text{V}$	●	0.8	1	1.6	mA
$I_{GATE(DN)FAST}$	Pulldown Current From GATE to SOURCE During OC/UVLO	$V_{DD} - SENSE = 100\text{mV}$ , $V_{GS} = 4\text{V}$	●	300	450	700	mA
$t_{PHL(SENSE)}$	( $V_{DD} - SENSE$ ) High to GATE Low	$V_{DD} - SENSE = 100\text{mV}$ , $C_{GS} = 10\text{nF}$	●		0.5	1	$\mu\text{s}$
$V_{GS(PowerBAD)}$	Gate-Source Voltage for Power Bad Fault	$V_{SOURCE} = 2.9\text{V} - 15\text{V}$	●	3.8	4.3	4.7	V
<b>Comparator Inputs</b>							
$V_{ON(TH)}$	ON Pin Threshold Voltage	$V_{ON}$ Rising	●	1.210	1.235	1.26	V
$\Delta V_{ON(HYST)}$	ON Pin Hysteresis		●	60	128	180	mV
$I_{ON(IN)}$	ON Pin Input Current	$V_{ON} = 1.2\text{V}$	●		0	$\pm 1$	$\mu\text{A}$
$V_{\overline{EN}(TH)}$	$\overline{EN}$ Input Threshold	$V_{\overline{EN}} = \text{Rising}$	●	1.215	1.235	1.255	V
$\Delta V_{\overline{EN}(HYST)}$	$\overline{EN}$ Hysteresis		●	50	128	200	mV
$I_{\overline{EN}}$	$\overline{EN}$ Pin Input Current	$\overline{EN} = 3.5\text{V}$	●		0	$\pm 1$	$\mu\text{A}$
$V_{OV(TH)}$	OV Pin Threshold Voltage	$V_{OV}$ Rising	●	1.215	1.235	1.255	V
$\Delta V_{OV(HYST)}$	OV Pin Hysteresis		●	10	30	40	mV
$I_{OV(IN)}$	OV Pin Input Current	$V_{OV} = 1.8\text{V}$	●		0	$\pm 1$	$\mu\text{A}$
$V_{UV(TH)}$	UV Pin Threshold Voltage	$V_{UV}$ Rising	●	1.215	1.235	1.255	V
$\Delta V_{UV(HYST)}$	UV Pin Hysteresis		●	60	80	100	mV
$I_{UV(IN)}$	UV Pin Input Current	$V_{UV} = 1.8\text{V}$	●		0	$\pm 1$	$\mu\text{A}$
$V_{UV(RTH)}$	UV Pin Reset Threshold Voltage	$V_{UV}$ Falling	●	0.33	0.4	0.47	V
$\Delta V_{UV(RHYST)}$	UV Pin Reset Threshold Hysteresis		●	60	125	210	mV
$V_{FB}$	Foldback Pin Power Good Threshold	FB Rising	●	1.215	1.235	1.255	V
$\Delta V_{FB(HYST)}$	FB Pin Power Good Hysteresis		●	3	8	15	mV
$I_{FB}$	Foldback Pin Input Current	FB = 1.8V	●		0	$\pm 1$	$\mu\text{A}$
$V_{GPIO(TH)}$	GPIO Pin Input Threshold	$V_{GPIO}$ Rising	●	0.8	1	1.2	V

## ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at  $T_A = 25^\circ\text{C}$ .  $V_{DD} = 12\text{V}$  unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS	
<b>Other Pin Functions</b>							
$V_{GPIO(OL)}$	GPIO Pin Output Low Voltage	$I_{GPIO} = 5\text{mA}$	●	0.25	0.5	V	
$I_{GPIO(OH)}$	GPIO Pin Input Leakage Current	$V_{GPIO} = 15\text{V}$	●	0	$\pm 1$	$\mu\text{A}$	
$I_{SOURCE}$	SOURCE Pin Input Current	SOURCE = 15V	●	40	80	120	$\mu\text{A}$
$t_P(\text{GATE})$	Input (ON, OV, UV, $\overline{\text{EN}}$ ) to GATE Off Propagation Delay		●	3	5	$\mu\text{s}$	
$t_D(\text{GATE})$	Turn-On Delay	ON UV, OV, $\overline{\text{EN}}$ Overcurrent Auto-Retry	● ● ●	1 50 2.5	2 100 5	$\mu\text{s}$ ms s	
$V_{TIMERL(TH)}$	Timer Low Threshold		●	0.17	0.2	0.23	V
$V_{TIMERH(TH)}$	Timer High Threshold		●	1.2	1.235	1.26	V
$I_{TIMER(UP)}$	TIMER Pin Pull-Up Current		●	-80	-100	-120	$\mu\text{A}$
$I_{TIMER(DOWN)}$	TIMER Pin Pulldown Current for OC Auto-Retry		●	1.4	2	2.6	$\mu\text{A}$
$I_{TIMER(UP/DOWN)}$	TIMER Current Up/Down Ratio		●	40	50	60	
$V_{FILTER(TH)}$	FILTER High Threshold		●	1.2	1.235	1.27	V
$I_{FILTER}$	FILTER Timer Current	During OC FILTER = 0.5V	●	-7.5	-10	-12.5	$\mu\text{A}$
		After OC FILTER = 0.5V	●	1	2	3.5	$\mu\text{A}$
		During Startup FILTER = 0.5V	●	.03	0.6	1.2	mA
<b>ADC</b>							
RES	Resolution (No Missing Codes)		●	8		Bits	
INL	Integral Nonlinearity	$V_{DD} - \text{SENSE}$ (Note 5) SOURCE ADIN	● ● ●	-2 -1.25 -1.25	0.5 0.2 0.2	2 1.25 1.25	LSB LSB LSB
$V_{OS}$	Offset Error (Note 4)	$V_{DD} - \text{SENSE}$ SOURCE ADIN	● ● ●			$\pm 2.0$ $\pm 1.0$ $\pm 1.0$	LSB LSB LSB
TUE	Total Unadjusted Error	$V_{DD} - \text{SENSE}$ SOURCE ADIN	● ● ●			$\pm 5.5$ $\pm 5.0$ $\pm 5.0$	LSB LSB LSB
FSE	Full-Scale Error	$V_{DD} - \text{SENSE}$ SOURCE ADIN	● ● ●			$\pm 5.5$ $\pm 5.0$ $\pm 5.0$	LSB LSB LSB
$V_{FS}$	Full-Scale Voltage ( $255 \cdot V_{LSB}$ )	$V_{DD} - \text{SENSE}$ SOURCE ADIN	● ● ●	37.625 15.14 1.205	38.45 15.44 1.23	39.275 15.74 1.255	mV V V
$R_{ADIN}$	ADIN Pin Sampling Resistance	$V_{ADIN} = 1.28\text{V}$	●	1	2		$\text{M}\Omega$
$I_{ADIN}$	ADIN Pin Input Current	$V_{ADIN} = 1.28\text{V}$	●		0	$\pm 0.1$	$\mu\text{A}$
	Conversion Rate				10		Hz

## ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at  $T_A = 25^\circ\text{C}$ .  $V_{DD} = 12\text{V}$  unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS	
<b>I<sup>2</sup>C Interface</b>							
$V_{ADR(H)}$	ADR0, ADR1, ADR2 Input High Voltage		●	$INTV_{CC} - 0.8$	$INTV_{CC} - 0.4$	$INTV_{CC} - 0.2$	V
$I_{ADR(IN,Z)}$	ADR0, ADR1, ADR2 Hi-Z Input Current	ADR0, ADR1, ADR2 = 0.8V ADR0, ADR1, ADR2 = $INTV_{CC} - 0.8\text{V}$	●	3	-3		$\mu\text{A}$ $\mu\text{A}$
$V_{ADR(L)}$	ADR0, ADR1, ADR2 Input Low Voltage		●	0.2	0.4	0.8	V
$I_{ADR(IN)}$	ADR0, ADR1, ADR2 Input Current	ADR0, ADR1, ADR2 = 0V, $INTV_{CC}$	●	-80		80	$\mu\text{A}$
$I_{\overline{ALERT}}$	$\overline{ALERT}$ Input Current	$\overline{ALERT} = 6.5\text{V}$	●			$\pm 1$	$\mu\text{A}$
$V_{\overline{ALERT}(OL)}$	$\overline{ALERT}$ Output Low Voltage	$I_{\overline{ALERT}} = 3\text{mA}$	●		0.2	0.4	V
$V_{SDA,SCL(TH)}$	SDA, SCL Input Threshold		●	1.3	1.7	1.9	V
$I_{SDA,SCL(OH)}$	SDA, SCL Input Current	SCL, SDA = 6.5V	●			$\pm 1$	$\mu\text{A}$
$V_{SDA(OL)}$	SDA Output Low Voltage	$I_{SDA} = 3\text{mA}$	●		0.2	0.4	V
<b>I<sup>2</sup>C Interface Timing</b>							
$f_{SCL(MAX)}$	SCL Clock Frequency	Operates with $f_{SCL} \leq f_{SCL(MAX)}$	●	400	1000		kHz
$t_{BUF(MIN)}$	Bus Free Time Between Stop/Start Condition		●		0.12	1.3	$\mu\text{s}$
$t_{HD,STA(MIN)}$	Hold Time After (Repeated) Start Condition		●		30	600	ns
$t_{SU,STA(MIN)}$	Repeated Start Condition Set-Up Time		●		30	600	ns
$t_{SU,STO(MIN)}$	Stop Condition Set-Up Time		●		140	600	ns
$t_{HD,DAT(MIN)}$	Data Hold Time (Input)		●		30	100	ns
$t_{HD,DATO}$	Data Hold Time (Output)		●	300	500	900	ns
$t_{SU,DAT(MIN)}$	Data Set-Up Time		●		30	600	ns
$t_{SP}$	Suppressed Spike Pulse Width		●	50	110	250	ns
$C_X$	SCL, SDA Input Capacitance	SDAI Tied to SDAO (Note 6)	●			10	pF

**Note 1:** Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

**Note 2:** All currents into pins are positive; all voltages are referenced to GND unless otherwise specified.

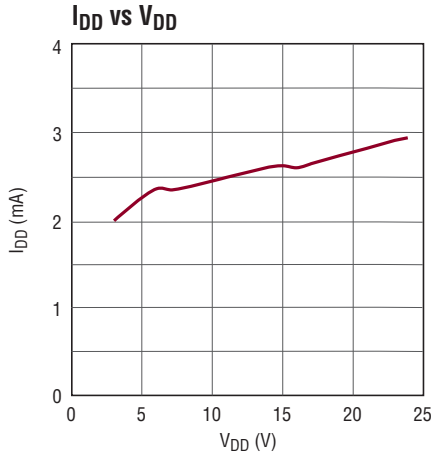
**Note 3:** An internal clamp limits the GATE pin to a minimum of 5V above SOURCE. Driving this pin to voltages beyond the clamp may damage the device.

**Note 4:** Offset error is the offset voltage measured from 1LSB when the output code flickers between 0000 0000 and 0000 0001.

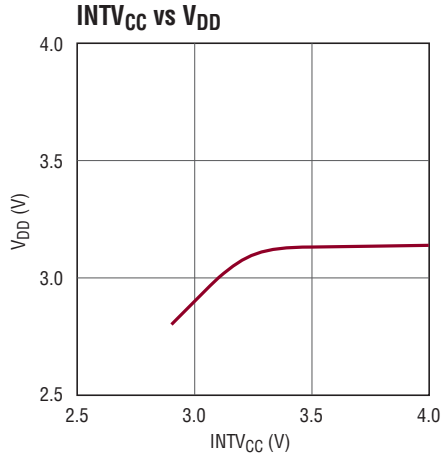
**Note 5:** Integral nonlinearity is defined as the deviation of a code from a precise analog input voltage. Maximum specifications are limited by the LSB step size and the single shot measurement. Typical specifications are measured from the 1/4, 1/2 and 3/4 areas of the quantization band.

**Note 6:** Guaranteed by design and not subject to test.

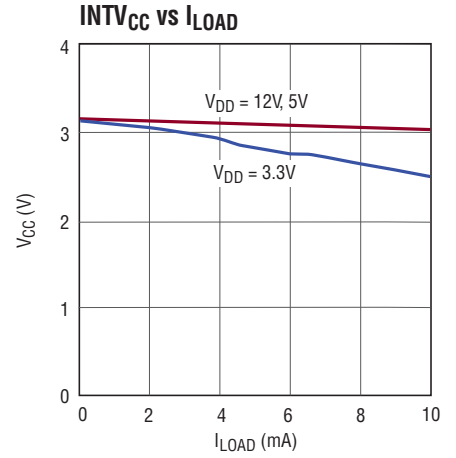
## TYPICAL PERFORMANCE CHARACTERISTICS $T_A = 25^\circ\text{C}$ , $V_{DD} = 12\text{V}$ unless otherwise noted



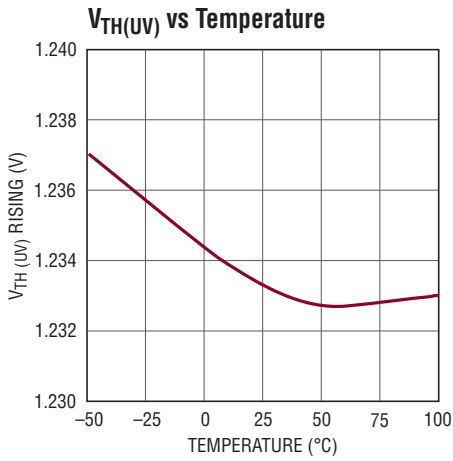
4280 G01



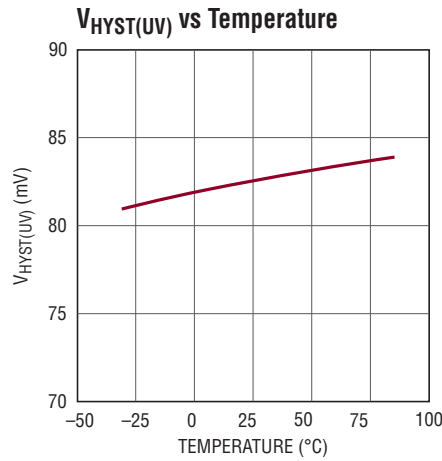
4280 G02



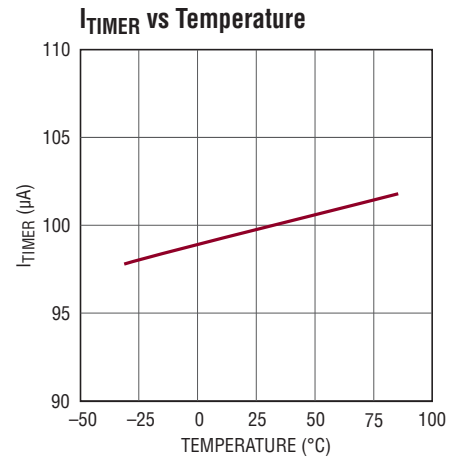
4280 G03



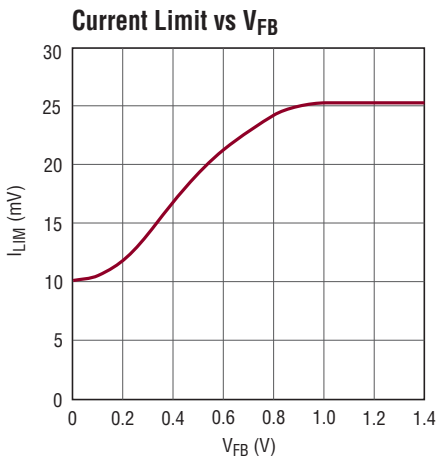
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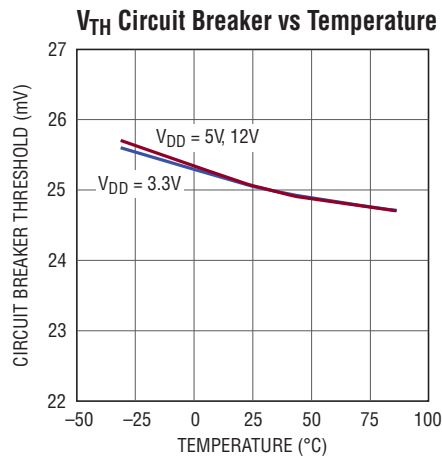
4280 G05



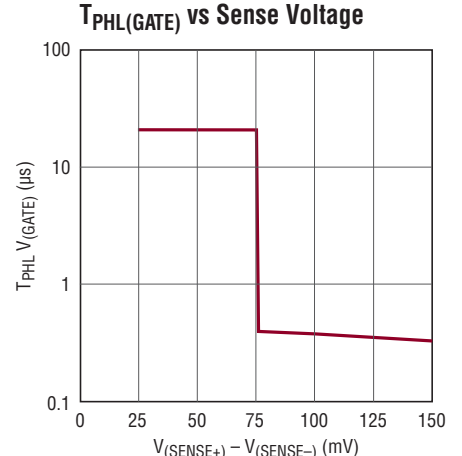
4280 G06



4280 G07

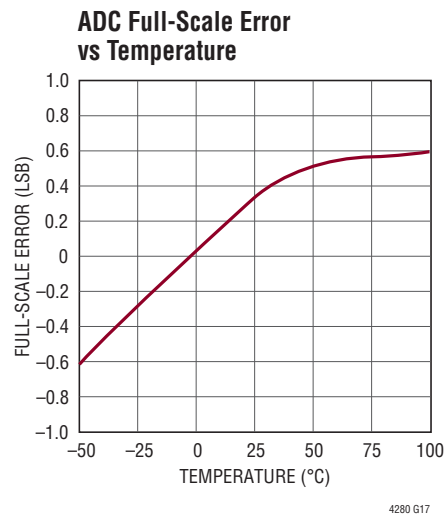
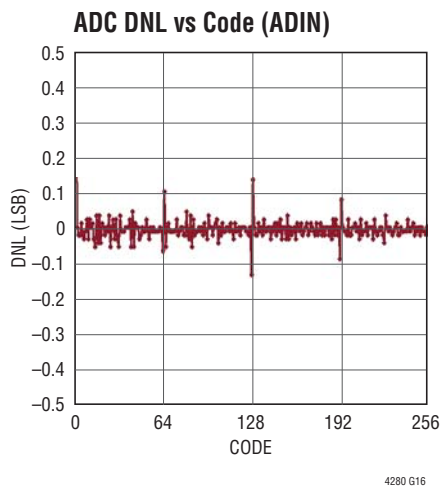
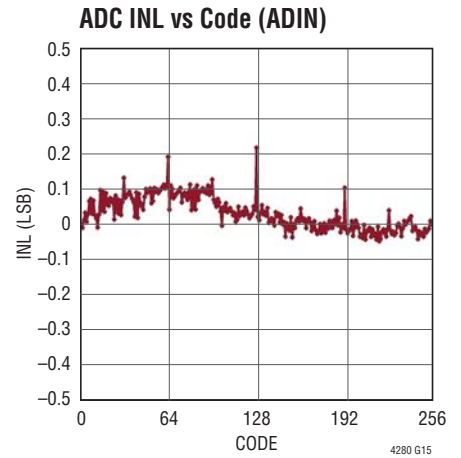
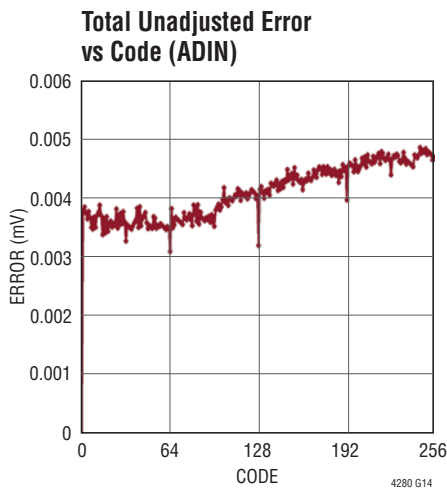
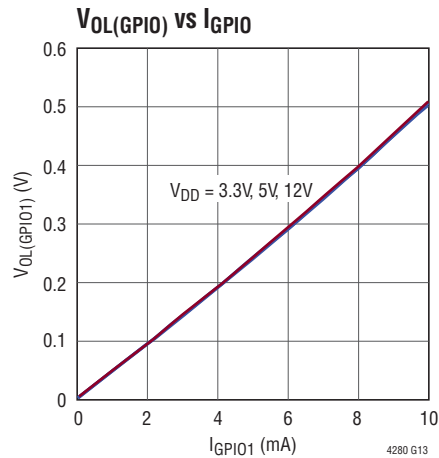
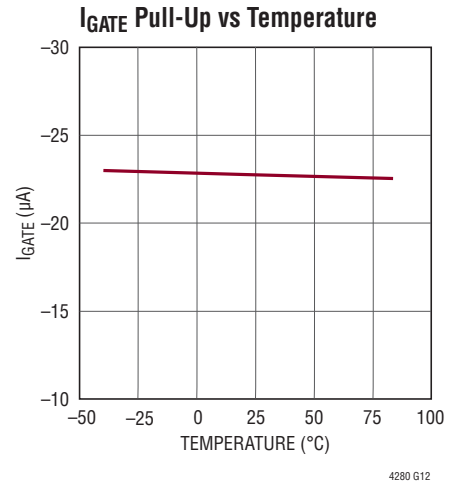
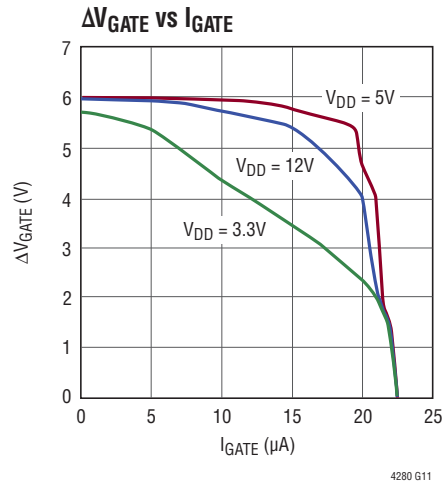
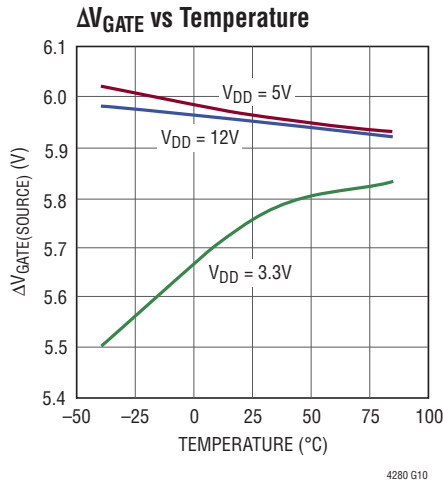


4280 G08



4280 G09

**TYPICAL PERFORMANCE CHARACTERISTICS**  $T_A = 25^\circ\text{C}$ ,  $V_{DD} = 12\text{V}$  unless otherwise noted



## PIN FUNCTIONS

**ADIN:** ADC Input. A voltage between 0V and 1.235V applied to this pin is measured by the onboard ADC. Tie to ground if unused.

**ADRO, ADR1, ADR2:** Serial Bus Address Inputs. Tying these pins to ground, to the INTV<sub>CC</sub> pin or open configures one of 27 possible addresses. See Table 1 in Applications Information.

**ALERT:** Fault Alert Output. Open-drain logic output that is pulled to ground when a fault occurs to alert the host controller. A fault alert is enabled by the  $\overline{\text{ALERT}}$  register. See Applications Information. Tie to ground if unused.

**EN:** Enable Input. Ground this pin to indicate a board is present and enable the N-channel MOSFET to turn on. When this pin is high, the MOSFET is not allowed to turn on. An internal 10 $\mu$ A current source pulls up this pin. Transitions on this pin are recorded in the Fault register. A high-to-low transition activates the logic to read the state of the ON pin and clear Faults. See Applications Information.

**EXPOSED PAD (Pin 25):** Exposed pad may be left open or connected to device ground.

**FB:** Foldback Current Limit and Power Good Input. A resistive divider from the output is tied to this pin. When the voltage at this pin drops below 1.235V, power is not considered good. The power bad condition may result in the GPIO pin pulling low or going high impedance depending on the configuration of control register bits A6 and A7. Also a power bad fault is logged in this condition if the LTC4280 has finished the start-up cycle and the GATE pin is high. See Applications Information. The current limit folds back from a 26mV sense voltage to 10mV as the FB pin voltage falls from 0.6V to 0V.

**FILTER:** Fault Filter Input. Connect a capacitor between this pin and ground to set a 123ms/ $\mu$ F delay for overcurrent fault filtering after startup.

**GATE:** Gate Drive for External N-Channel MOSFET. An internal 20 $\mu$ A current source charges the gate of the MOSFET. Often no compensation capacitor is required on the GATE pin, but a resistor and capacitor network from this pin to ground may be used to set the turn-on output voltage slew rate. See Applications Information. During turn-off there is a 1mA pulldown current. During a short-circuit or undervoltage lockout ( $V_{DD}$  or INTV<sub>CC</sub>), a 450mA pulldown current source between GATE and SOURCE is activated.

**GND:** Device Ground.

**GPIO:** General Purpose Input/Output. Open-drain logic output or logic input. Defaults to an output set to pull low to indicate power is not good. Configure according to Table 2 and 3.

**INTV<sub>CC</sub>:** Low Voltage Supply Decoupling Output. Connect a 0.1 $\mu$ F capacitor from this pin to ground.

**ON:** On Control Input. A rising edge turns on the external N-channel MOSFET and a falling edge turns it off. This pin also configures the state of the FET On bit in the control register (and hence the external MOSFET) at power up. For example, if the ON pin is tied high, then the FET On bit (A3 in Table 2) goes high 100ms after power-up. Likewise if the ON pin is tied low then the part remains off after power-up until the FET On bit is set high using the I<sup>2</sup>C bus. A high-to-low transition on this pin clears the fault register.

**OV:** Overvoltage Comparator Input. Connect this pin to an external resistive divider from  $V_{DD}$ . If the voltage at this pin rises above 1.235V, an overvoltage fault is detected and the GATE turns off. Tie to GND if unused.

## PIN FUNCTIONS

**SCL:** Serial Bus Clock Input. Data at the SDA pin is shifted in or out on rising edges of SCL. This is a high impedance pin that is generally driven by an open-collector output from a master controller. An external pull-up resistor or current source is required.

**SDAO:** Serial Bus Data Output. Open-drain output for sending data back to the master controller or acknowledging a write operation. Normally tied to SDAI to form the SDA line. An external pull-up resistor or current source is required.

**SDAI:** Serial Bus Data Input. A high impedance input for shifting in address, command or data bits. Normally tied to SDAO to form the SDA line.

**SENSE<sup>+</sup>:** Positive Current Sense Input. Connect this pin to the input of the current sense resistor. Must be connected to the same trace as  $V_{DD}$ .

**SENSE<sup>-</sup>:** Negative Current Sense Input. Connect this pin to the output of the current sense resistor. This pin provides sense voltage feedback and monitoring for the current limit, circuit breaker and ADC.

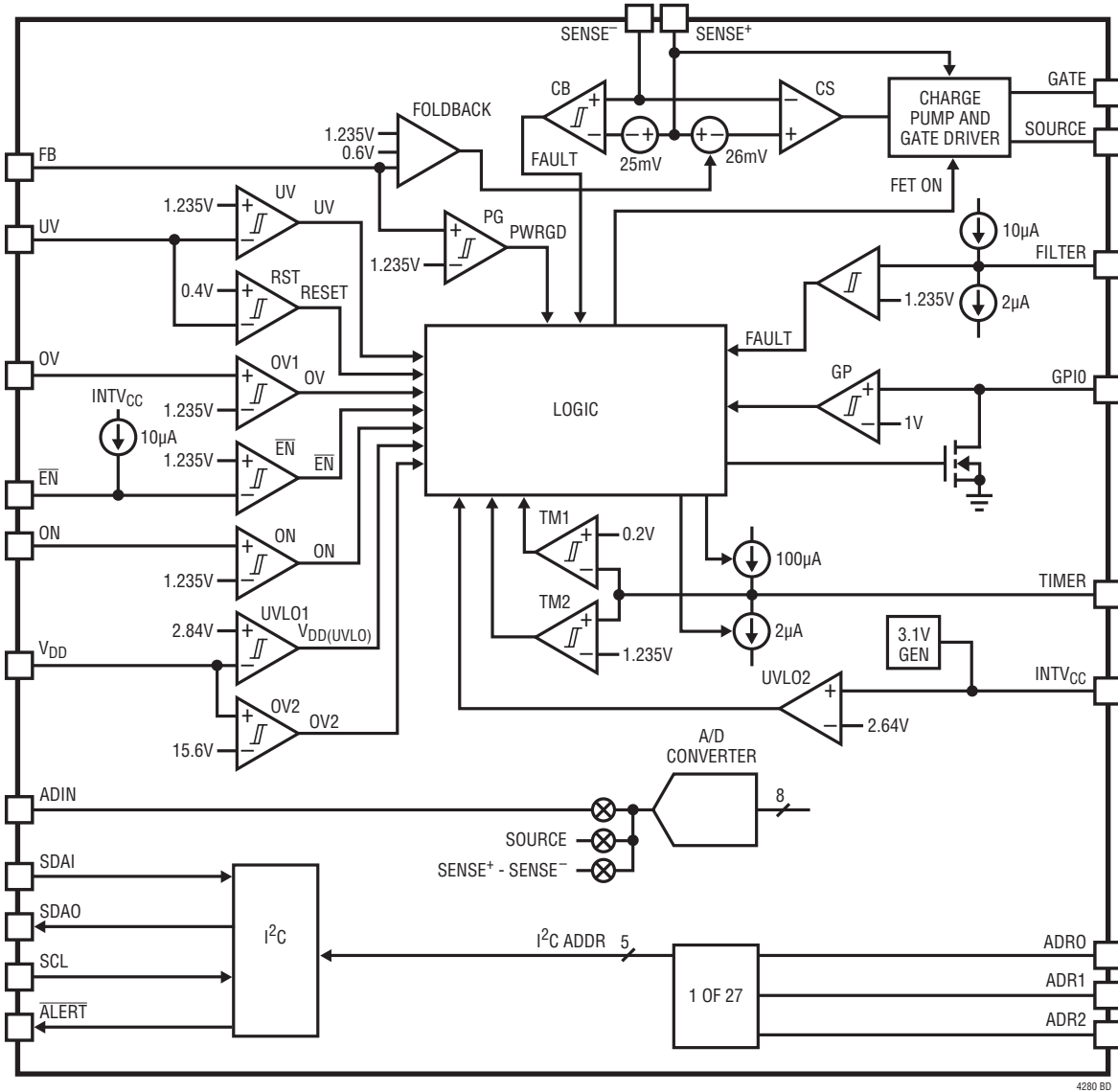
**SOURCE:** N-Channel MOSFET Source and ADC Input. Connect this pin to the source of the external N-channel MOSFET switch for gate drive return. This pin also serves as the ADC input to monitor output voltage. The pin provides a return for the gate pulldown circuit.

**TIMER:** Start-Up Timer Input. Connect a capacitor between this pin and ground to set a 12.3ms/ $\mu$ F duration for start-up, after which an overcurrent fault is logged if the inrush is still current limited. The duration of the off time is 600ms/ $\mu$ F when overcurrent auto-retry is enabled, resulting in a 1:50 duty cycle. An internal timer provides a 100ms start-up time and 5 seconds auto-retry time if this pin is tied to INTV<sub>CC</sub>.

**UV:** Undervoltage Comparator Input. Connect this pin to an external resistive divider from  $V_{DD}$ . If the voltage at this pin falls below 1.155V, an undervoltage fault is detected and the GATE turns off. Pulling this pin below 0.4V resets all faults and allows the GATE to turn back on. Tie to INTV<sub>CC</sub> if unused.

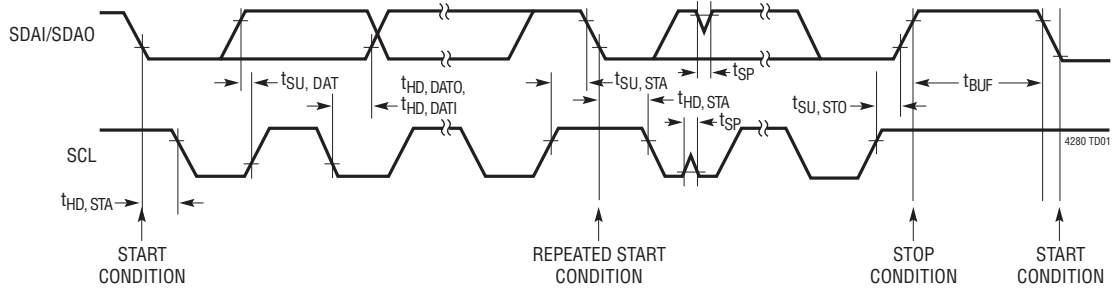
**V<sub>DD</sub>:** Supply Voltage Input. This pin has an undervoltage lockout threshold of 2.84V and overvoltage lockout threshold of 15.6V.

FUNCTIONAL DIAGRAM



4280 BD

# TIMING DIAGRAM



## OPERATION

The LTC4280 is designed to turn a board's supply voltage on and off in a controlled manner, allowing the board to be safely inserted or removed from a live backplane. During normal operation, the charge pump and gate driver turn on an external N-channel MOSFET's gate to pass power to the load. The gate driver uses a charge pump that derives its power from the  $V_{DD}$  pin. Also included in the gate driver is an internal 6.5V gate-to-source clamp. During start-up the inrush current is tightly controlled by using current limit foldback and output  $dV/dt$  limiting.

The current sense (CS) amplifier monitors the load current using the difference between the  $SENSE^+$  and  $SENSE^-$  pin voltages. The CS amplifier limits the current in the load by pulling back on the gate-to-source voltage in an active control loop when the sense voltage exceeds the commanded value. The CS amplifier requires  $20\mu A$  input bias current from both the  $SENSE^+$  and the  $SENSE^-$  pins.

A short-circuit on the output to ground results in excessive power dissipation during active current limiting. To limit this power, the CS amplifier regulates the voltage between the  $SENSE^+$  and  $SENSE^-$  pins at 26mV with foldback to 10mV.

If an overcurrent condition persists, the internal circuit breaker (CB) registers a fault when either the sense voltage exceeds 25mV or the current sense amplifier is in regulation for more than the time limit set by the capacitor on the FILTER pin. This indicates to the logic that it is time to turn off the GATE to prevent overheating. At this point the start-up TIMER pin voltage ramps down using the  $2\mu A$  current source until the voltage drops below 0.2V (comparator TM1) which tells the logic that the pass transistor has cooled and it is safe to turn it on again if overcurrent auto-retry is enabled. If the TIMER pin is tied to  $INTV_{CC}$ , the cool-down time defaults to 5 seconds on an internal system timer in the logic.

The output voltage is monitored using the FB pin and the Power Good (PG) comparator to determine if the power is available for the load. The power good condition can be signaled by the GPIO pin using an open-drain pulldown transistor. The GPIO pin may also be configured to signal power bad, or as a general purpose input (GP comparator), or a general purpose open drain output.

The Functional Diagram shows the monitoring blocks of the LTC4280. The group of comparators on the left side includes the undervoltage (UV), overvoltage (OV), reset (RST), enable ( $\overline{EN}$ ) and signal on (ON) comparators. These comparators determine if the external conditions are valid prior to turning on the GATE. But first the two undervoltage lockout circuits, UVLO1 and UVLO2, validate the input supply and the internally generated 3.1V supply,  $INTV_{CC}$ . UVLO2 also generates the power-up initialization to the logic circuits as  $INTV_{CC}$  crosses this rising threshold. If the fixed internal overvoltage comparator, OV2, detects that  $V_{DD}$  is greater than 15.6V, the part immediately generates an overvoltage fault and turns the GATE off.

Included in the LTC4280 is an 8-bit A/D converter. The converter has a 3-input multiplexer to select between the ADIN pin, the SOURCE pin and the  $SENSE^+ - SENSE^-$  voltage.

An  $I^2C$  interface is provided to read the A/D registers. It also allows the host to poll the device and determine if faults have occurred. If the  $\overline{ALERT}$  line is configured as an interrupt, the host is enabled to respond to faults in real time. The typical SDA line is divided into an SDAI (input) and SDAO (output). This simplifies applications using an optoisolator driven directly from the SDAO output. An application which uses optoisolation is shown on the back cover. The  $I^2C$  device address is decoded using the ADR0, ADR1 and ADR2 pins. These inputs have three states each that decode into a total of 27 device addresses.



## APPLICATIONS INFORMATION

When the MOSFET is turning on, the inrush current follows the foldback profile as shown in Figure 2. Meanwhile the FILTER pin is held low with 0.6mA to prevent the FILTER pin from generating an overcurrent fault during start-up. The TIMER pin integrates at 100 $\mu$ A during start-up and once it reaches its threshold of 1.235V, the part checks to see if it is in current limit, which indicates that it has started up into a short-circuit condition. If this is the case, the overcurrent fault bit, D2 in Table 5, is set and the part turns off. If the part is not in current limit, the FILTER pin is released to enable circuit breaker and current limit based overcurrent faults. Alternately an internal 100ms start-up timer may be selected by tying the TIMER pin to INTV<sub>CC</sub>.

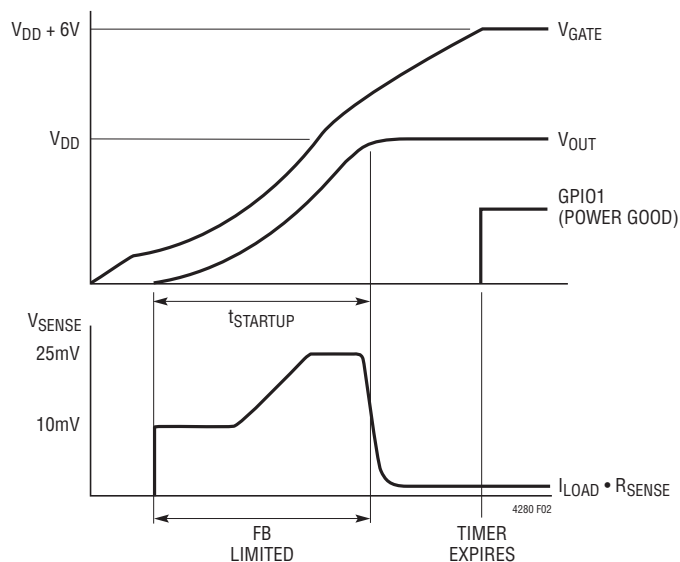


Figure 2. Power-Up Waveforms

As the SOURCE voltage rises, the FB pin follows as set by R7 and R8. Once FB crosses its 1.235V threshold, and the start-up timer has expired, the GPIO pin, in its default configuration, ceases to pull low and indicates that power is now good.

If R6 and C1 are employed for a constant current during start-up, which produces a constant dV/dt at the output,

a 20 $\mu$ A pull-up current from the gate pin slews the gate upwards and the part is not in current limit. The start-up TIMER may expire in this condition and an OC fault is not generated even though start-up has not completed. Either the sense voltage increases to the 25mV CB threshold or the current limit as set by the FB pin which generates an OC fault when the FILTER pin reaches its 1.235V threshold, or the FB pin voltage crosses its 1.235V power good threshold and the GPIO pin signals power good.

### GATE Pin Voltage

A curve of gate-to-source drive vs V<sub>DD</sub> is shown in the Typical Performance Characteristics. At minimum input supply voltage of 2.9V, the minimum gate-to-source drive voltage is 4.7V. The gate-to-source voltage is clamped below 6.5V to protect the gates of logic level N-channel MOSFETs.

### Turn-Off Sequence

The GATE is turned off by a variety of conditions. A normal turn-off is initiated by the ON pin going low or a serial bus turn-off command. Additionally, several fault conditions turn off the GATE. These include an input overvoltage (OV pin), input undervoltage (UV pin), overcurrent circuit breaker (SENSE<sup>-</sup> pin), or EN transitioning high. Writing a logic one into the UV, OV or OC fault bits (D0-D2 in Table 5) also latches off the GATE if their auto-retry bits are set to false.

Normally the MOSFET is turned off with a 1mA current pulling down the GATE pin to ground. With the MOSFET turned off, the SOURCE and FB voltages drop as C<sub>L</sub> discharges. When the FB voltage crosses below its threshold, GPIO pulls low to indicate that the output power is no longer good.

If the V<sub>DD</sub> pin falls below 2.74V for greater than 2 $\mu$ s or INTV<sub>CC</sub> drops below 2.60V for greater than 1 $\mu$ s, a fast shut down of the MOSFET is initiated. The GATE pin is pulled down with a 450mA current to the SOURCE pin.

## APPLICATIONS INFORMATION

### Overcurrent Fault

The LTC4280 features an adjustable current limit that protects against short-circuits or excessive load current until an overcurrent fault is generated. An overcurrent fault can occur in two different manners. First, at the end of start-up when the TIMER pin reaches its 1.235V threshold or the internal 100ms start-up timer expires, if the part is in current limit an overcurrent fault is generated. Second, after start-up the FILTER pin ramps up with 10 $\mu$ A if the sense voltage exceeds the 25mV circuit breaker threshold or the current limit circuit regulates the sense voltage. When the FILTER pin passes its 1.235V threshold the overcurrent present bit C2 is set and an overcurrent fault is generated. In both cases the external MOSFET is turned off and the overcurrent fault bit is set.

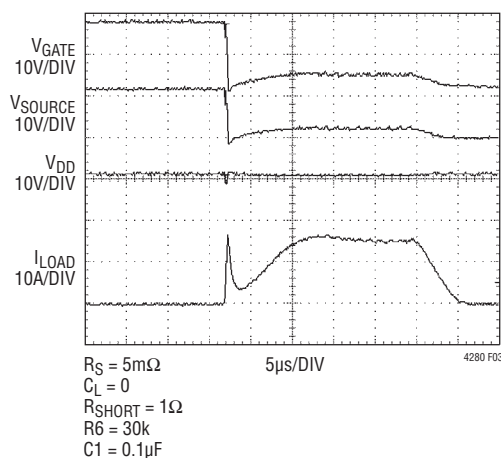


Figure 3. Short-Circuit Waveforms

After the MOSFET is turned off, the TIMER and FILTER capacitors begins discharging with 2 $\mu$ A pulldown currents. When the TIMER pin reaches its 0.2V threshold the MOSFET is allowed to turn on again if the overcurrent fault has been cleared. However, if the overcurrent auto-retry bit, A2 has been set then the MOSFET turns on again automatically without resetting the overcurrent fault. Use a minimum value of 10nF for  $C_T$ . If the TIMER pin is bypassed by tying

it to INTV<sub>CC</sub>, the part is allowed to turn on again after an internal 5 second timer has expired, in the same manner as the TIMER pin passing its 0.2V threshold.

### Overvoltage Fault

An overvoltage fault occurs when either the OV pin rises above its 1.235V threshold, or the V<sub>DD</sub> pin rises above its 15.6V threshold, for more than 2 $\mu$ s. This shuts off the GATE with a 1mA current to ground and sets the overvoltage present bit C0 and the overvoltage fault bit D0. If the pin subsequently falls back below the threshold for 100ms, the GATE is allowed to turn on again unless overvoltage auto-retry has been disabled by clearing bit A0.

### Undervoltage Fault

An undervoltage fault occurs when the UV pin falls below its 1.235V threshold for more than 2 $\mu$ s. This turns off the GATE with a 1mA current to ground and sets undervoltage present bit C1 and undervoltage fault bit D1. If the UV pin subsequently rises above the threshold for 100ms, the GATE is turned on again unless undervoltage auto-retry has been disabled by clearing bit A1. When power is applied to the device, if UV is below its 1.235V threshold after INTV<sub>CC</sub> crosses its 2.64V undervoltage lockout threshold, an undervoltage fault is logged in the fault register.

### Board Present Change of State

Whenever the  $\overline{\text{EN}}$  pin toggles, bit D4 is set to indicate a change of state. When the  $\overline{\text{EN}}$  pin goes high, indicating board removal, the GATE turns off immediately (with a 1mA current to ground) and clears the board present bit, C4. If the  $\overline{\text{EN}}$  pin is pulled low, indicating a board insertion, all fault bits except D4 are cleared and enable bit, C4, is set. If the  $\overline{\text{EN}}$  pin remains low for 100ms the state of the ON pin is captured in 'FET On' control bit A3. This turns the switch on if the ON pin is tied high. There is an internal 10 $\mu$ A pull-up current source on the  $\overline{\text{EN}}$  pin.

## APPLICATIONS INFORMATION

If the system shuts down due to a fault, it may be desirable to restart the system simply by removing and reinserting a load card. In cases where the LTC4280 and the switch reside on a backplane or midplane and the load resides on a plug-in card, the  $\overline{\text{EN}}$  pin detects when the plug-in card is removed. Figure 4 shows an example where the  $\overline{\text{EN}}$  pin is used to detect insertion. Once the plug-in card is reinserted the fault register is cleared (except for D4). After 100ms the state of the ON pin is latched into bit A3 of the control register. At this point the system starts up again.

If a connection sense on the plug-in card is driving the  $\overline{\text{EN}}$  pin, insertion or removal of the card may cause the pin voltage to bounce. This results in clearing the fault register when the card is removed. The pin may be debounced using a filter capacitor,  $C_{\text{EN}}$ , on the  $\overline{\text{EN}}$  pin as shown in Figure 4. The filter time is given by:

$$t_{\text{FILTER}} = C_{\text{EN}} \cdot 123 \text{ [ms/}\mu\text{F]}$$

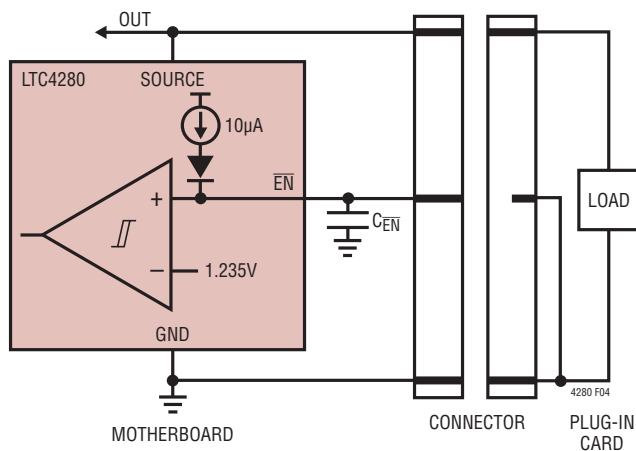


Figure 4. Plug-In Card Insertion/Removal

### FET Short Fault

A FET short fault is reported if the data converter measures a current sense voltage greater than or equal to 1.6mV while the GATE is turned off. This condition sets FET short present bit, C5, and FET short fault bit D5.

### Power Bad Fault

A power bad fault is reported if the FB pin voltage drops below its 1.235V threshold for more than 2µs when the GATE is high. This pulls the GPIO pin low immediately when configured as power-good, and sets power-bad present bit, C3, and power bad fault bit D3. A circuit prevents power-bad faults if the gate-to-source voltage is low, eliminating false power-bad faults during power-up or power-down. If the FB pin voltage subsequently rises back above the threshold, the GPIO pin returns to a high impedance state and bit C3 is reset.

### Fault Alerts

When any of the fault bits in FAULT register D are set, an optional bus alert is generated if the appropriate bit in the  $\overline{\text{ALERT}}$  register B has been set. This allows only selected faults to generate alerts. At power-up the default state is to not alert on faults. If an alert is enabled, the corresponding fault causes the  $\overline{\text{ALERT}}$  pin to pull low. After the bus master controller broadcasts the Alert Response Address, the LTC4280 responds with its address on the SDA line and releases  $\overline{\text{ALERT}}$  as shown in Table 6. If there is a collision between two LTC4215s responding with their addresses simultaneously, then the device with the lower address wins arbitration and responds first. The  $\overline{\text{ALERT}}$  line is also released if the device is addressed by the bus master.

Once the  $\overline{\text{ALERT}}$  signal has been released for one fault, it is not pulled low again until the FAULT register indicates a different fault has occurred or the original fault is cleared and it occurs again. Note that this means repeated or continuing faults do not generate alerts until the associated FAULT register bit has been cleared.

### Resetting Faults

Faults are reset with any of the following conditions. First, a serial bus command writing zeros to the FAULT register D clears the associated faults. Second, the entire FAULT register is cleared when the switch is turned off by the ON

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pin or bit A3 going from high to low, if the UV pin is brought below its 0.4V reset threshold for 2 $\mu$ s, or if INTV<sub>CC</sub> falls below its 2.64V undervoltage lockout threshold. Finally, when  $\overline{\text{EN}}$  is brought from high to low, only FAULT bits D0-D3 are cleared, and bit D4, that indicates a  $\overline{\text{EN}}$  change of state, is set. Note that faults that are still present, as indicated in STATUS Register C, cannot be cleared.

The FAULT register is not cleared when auto-retrying. When auto-retry is disabled the existence of a D0, D1 or D2 fault keeps the switch off. As soon as the fault is cleared, the switch turns on. If auto-retry is enabled, then a high value in C0, C1 or C2 holds the switch off and the fault register is ignored. Subsequently, when bits C0, C1 and C2 are cleared by removal of the fault condition, the switch is allowed to turn on again.

The LTC4280 will set bit D2 and turn off in the event of an overcurrent fault, preventing it from remaining in an overcurrent condition. If configured to auto-retry, the LTC4280 will continually attempt to restart after cool-down cycles until it succeeds in starting up without generating an overcurrent fault.

### Data Converter

The LTC4280 incorporates an 8-bit  $\Delta\Sigma$  A/D converter that continuously monitors three different voltages. The  $\Delta\Sigma$  architecture inherently averages signal noise during the measurement period. The SOURCE pin has a 1/12.5 resistive divider to monitor a full-scale voltage of 15.4V with 60mV resolution. The ADIN pin is monitored with a 1.235V full-scale and 4.82mV resolution, and the voltage between the V<sub>DD</sub> and SENSE pins is monitored with a 38.6mV full-scale and 151 $\mu$ V resolution.

Results from each conversion are stored in registers E (Sense), F (Source) and G (ADIN), as seen in Tables 6-8, and are updated 10 times per second. Setting CONTROL register bit A5 invokes a test mode that halts the data converter so that registers E, F, and G may be written to and read from for software testing.

### Configuring the GPIO Pin

Table 2 describes the possible states of the GPIO pin using the control register bits A6 and A7. At power-up, the default state is for the GPIO pin to go high impedance when power is good (FB pin greater than 1.235V). Other applications for the GPIO pin are to pull down when power is good, a general purpose output and a general purpose input.

### Current Limit Stability

For many applications the LTC4280 current limit will be stable without additional components. However there are certain conditions where additional components may be needed to improve stability. The dominant pole of the current limit circuit is set by the capacitance and resistance at the gate of the external MOSFET, and larger gate capacitance makes the current limit loop more stable. Usually a total of 8nF gate to source capacitance is sufficient for stability and is typically provided by inherent MOSFET C<sub>GS</sub>, however the stability of the loop is degraded by increasing R<sub>SENSE</sub> or by reducing the size of the resistor on a gate RC network if one is used, which may require additional gate to source capacitance. Board level short-circuit testing is highly recommended as board layout can also affect transient performance, for stability testing the worst case condition for current limit stability occurs when the output is shorted to ground after a normal startup.

There are two possible parasitic oscillations when the MOSFET operates as a source follower when ramping at power-up or during current limiting. The first type of oscillation occurs at high frequencies, typically above 1MHz. This high frequency oscillation is easily damped with R5 as shown in Figure 1. In some applications, one may find that R5 helps in short-circuit transient recovery as well. However, too large of an R5 value will slow down the turn-off time. The recommended R5 range is between 5 $\Omega$  and 500 $\Omega$ .

The second type of source follower oscillation occurs at frequencies between 200kHz and 800kHz due to the load capacitance being between 0.2 $\mu$ F and 9 $\mu$ F, the presence

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of R5 resistance, the absence of a drain bypass capacitor, a combination of bus wiring inductance and bus supply output impedance. To prevent this second type of oscillation avoid load capacitance below 10 $\mu$ F, alternately connect an external capacitor from the MOSFET gate to ground with a value greater than 1.5 $\mu$ F.

### Supply Transients

The LTC4280 is designed to ride through supply transients caused by load steps. If there is a shorted load and the parasitic inductance back to the supply is greater than 0.5 $\mu$ H, there is a chance that the supply collapses before the active current limit circuit brings down the GATE pin. If this occurs, the undervoltage monitors pull the GATE pin low. The undervoltage lockout circuit has a 2 $\mu$ s filter time after V<sub>DD</sub> drops below 2.74V. The UV pin reacts in 2 $\mu$ s to shut the GATE off, but it is recommended to add a filter capacitor C<sub>F</sub> to prevent unwanted shutdown caused by a transient. Eventually either the UV pin or undervoltage lockout responds to bring the current under control before the supply completely collapses.

### Supply Transient Protection

The LTC4280 is safe from damage with supply voltages up to 24V. However, spikes above 24V may damage the part. During a short-circuit condition, large changes in current flowing through power supply traces may cause inductive voltage spikes which exceed 24V. To minimize such spikes, the power trace inductance should be minimized by using wider traces or heavier trace plating. Also, a snubber circuit dampens inductive voltage spikes. Build a snubber by using a 100 $\Omega$  resistor in series with a 0.1 $\mu$ F capacitor between V<sub>DD</sub> and GND. A surge suppressor, Z1 in Figure 1, at the input can also prevent damage from voltage surges.

### Design Example

As a design example, take the following specifications: V<sub>IN</sub> = 12V, I<sub>MAX</sub> = 5A, I<sub>INRUSH</sub> = 1A, 5ms FILTER time, C<sub>L</sub> = 330 $\mu$ F, V<sub>UV(ON)</sub> = 10.75V, V<sub>OV(OFF)</sub> = 14.0V, V<sub>PWRGD(UP)</sub> = 11.6V, and I<sup>2</sup>C ADDRESS = 1010011. This completed design is shown in Figure 1.

Selection of the sense resistor, R<sub>S</sub>, is set by the overcurrent threshold of 25mV:

$$R_S = \frac{25\text{mV}}{I_{\text{MAX}}} = 0.005\Omega$$

The MOSFET is sized to handle the power dissipation during inrush when output capacitor C<sub>OUT</sub> is being charged. A method to determine power dissipation during inrush is based on the principle that:

$$\text{Energy in CL} = \text{Energy in Q1}$$

This uses:

$$\text{Energy in } C_L = \frac{1}{2}CV^2 = \frac{1}{2}(0.33\text{mF})(12)^2$$

or 0.024 joules. Calculate the time it takes to charge up C<sub>OUT</sub>:

$$t_{\text{STARTUP}} = C_L \cdot \frac{V_{\text{DD}}}{I_{\text{INRUSH}}} = 0.33\text{mF} \cdot \frac{12\text{V}}{1\text{A}} = 4\text{ms}$$

The power dissipated in the MOSFET:

$$P_{\text{DISS}} = \frac{\text{Energy in } C_L}{t_{\text{STARTUP}}} = 6\text{W}$$

The SOA (safe operating area) curves of candidate MOSFETs must be evaluated to ensure that the heat capacity of the package tolerates 6W for 4ms. The SOA curves of the Fairchild FDC653N provide for 2A at 12V (24W) for 10ms, satisfying this requirement. Since the FDC653N has less than 8 $\mu$ F of gate capacitance and we are using a GATE RC network, the short-circuit stability of the current limit should be checked and improved by adding a capacitor from GATE to SOURCE if needed.

The inrush current is set to 1A using C1:

$$C1 = C_L \cdot \frac{I_{\text{GATE}}}{I_{\text{INRUSH}}}$$

$$C1 = 0.33\text{mF} \cdot \frac{20\mu\text{A}}{1\text{A}} \text{ or } C1 = 6.8\text{nF}$$

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For a start-up time of 4ms with a 2x safety margin we choose:

$$C_{\text{TIMER}} = 2 \cdot \frac{t_{\text{STARTUP}}}{12.3\text{ms}/\mu\text{F}}$$

$$C_{\text{TIMER}} = \frac{8\text{ms}}{12.3\text{ms}/\mu\text{F}} \approx 0.68\mu\text{F}$$

For an overcurrent fault filter time of 5ms we choose:

$$C_F = t_{\text{FILTER}}/123\text{ms}/\mu\text{F} \approx 47\text{nF}$$

The UV and OV resistor string values can be solved in the following method. First pick R3 based on  $I_{\text{STRING}}$  being  $1.235\text{V}/R3$  at the edge of the OV rising threshold, where  $I_{\text{STRING}} > 40\mu\text{A}$ . Then solve the following equations:

$$R2 = \frac{V_{\text{OV(OFF)}}}{V_{\text{UV(ON)}}} \cdot R3 \cdot \frac{UV_{\text{TH(RISING)}}}{OV_{\text{TH(FALLING)}}} - R3$$

$$R1 = \frac{V_{\text{UV(ON)}} \cdot (R3 + R2)}{UV_{\text{TH(RISING)}}} - R3 - R2$$

In our case we choose R3 to be 3.4k $\Omega$  to give a resistor string current below 100 $\mu\text{A}$ . Then solving the equations results in R2 = 1.16k $\Omega$  and R1 = 34.6k $\Omega$ .

The FB divider is solved by picking R8 and solving for R7, choosing 3.57k $\Omega$  for R8 we get:

$$R7 = \frac{V_{\text{PWRGD(UP)}} \cdot R8}{FB_{\text{TH(RISING)}}} - R8$$

resulting in R7 = 30k $\Omega$ .

A 0.1 $\mu\text{F}$  capacitor, C<sub>F</sub>, is placed on the UV pin to prevent supply glitches from turning off the GATE via UV or OV.

The address is set with the help of Table 1, which indicates binary address 1010011 corresponds to address 19. Address 19 is set by setting ADR2 high, ADR1 open and ADR0 high.

Next the value of R5 and R6 are chosen to be the default values 10 $\Omega$  and 15k as discussed previously.

In addition a 0.1 $\mu\text{F}$  ceramic bypass capacitor is placed on the INTV<sub>CC</sub> pin.

### Layout Considerations

To achieve accurate current sensing, a Kelvin connection is required. The minimum trace width for 1oz copper foil is 0.02" per amp to make sure the trace stays at a reasonable temperature. Using 0.03" per amp or wider is recommended. Note that 1oz copper exhibits a sheet resistance of about 530 $\mu\Omega/\square$ . Small resistances add up quickly in high current applications. To improve noise immunity, put the resistive dividers to the UV, OV and FB pins close to the device and keep traces to V<sub>DD</sub> and GND short. It is also important to put the bypass capacitor for the INTV<sub>CC</sub> pin, C3, as close as possible between INTV<sub>CC</sub> and GND. A 0.1 $\mu\text{F}$  capacitor from the UV pin (and OV pin through resistor R2) to GND also helps reject supply noise. Figure 4 shows a layout that addresses these issues. Note that a surge suppressor, Z1, is placed between supply and ground using wide traces.

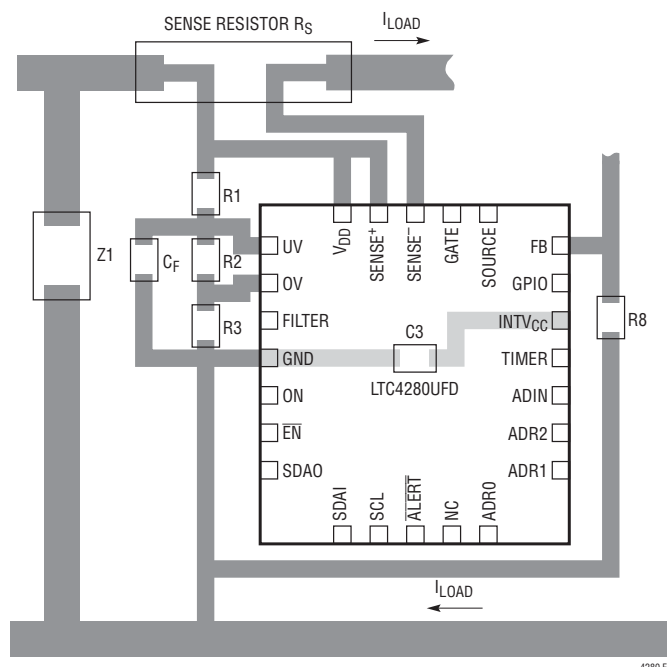


Figure 5. Recommended Layout

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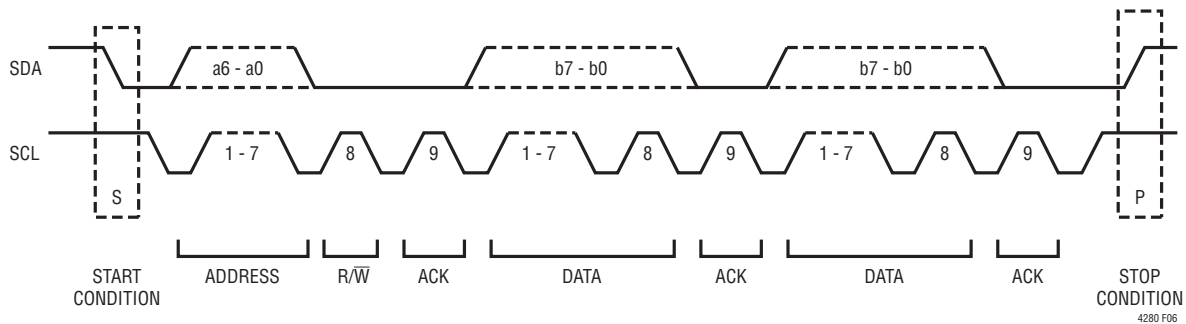


Figure 6. Data Transfer Over I<sup>2</sup>C or SMBus

### Digital Interface

The LTC4280 communicates with a bus master using a 2-wire interface compatible with I<sup>2</sup>C Bus and SMBus, an I<sup>2</sup>C extension for low power devices.

The LTC4280 is a read-write slave device and supports SMBus bus Read Byte, Write Byte, Read Word and Write Word commands. The second word in a Read Word command is identical to the first word. The second word in a Write Word command is ignored. Data formats for these commands are shown in Figures 6 to 11.

### START and STOP Conditions

When the bus is idle, both SCL and SDA are high. A bus master signals the beginning of a transmission with a start condition by transitioning SDA from high to low while SCL is high, as shown in Figure 6. When the master has finished communicating with the slave, it issues a STOP condition by transitioning SDA from low to high while SCL is high. The bus is then free for another transmission.

### I<sup>2</sup>C Device Addressing

Twenty-seven distinct bus addresses are available using three 3-state address pins, ADR0-ADR2. Table 1 shows the correspondence between pin states and addresses. Note that address bits B7 and B6 are internally configured to 10. In addition, the LTC4280 responds to two special addresses. Address (1011 111) is a mass write address that writes to all LTC4280s, regardless of their individual address settings. Mass write can be disabled by setting register A4 to zero. Address (0001 100) is the SMBus Alert Response Address. If the LTC4280 is pulling low on the  $\overline{\text{ALERT}}$  pin, it acknowledges this address by broadcasting its address and releasing the  $\overline{\text{ALERT}}$  pin.

### Acknowledge

The acknowledge signal is used in handshaking between transmitter and receiver to indicate that the last byte of data was received. The transmitter always releases the SDA line during the acknowledge clock pulse. When the slave is the receiver, it pulls down the SDA line so that it

## APPLICATIONS INFORMATION

remains LOW during this pulse to acknowledge receipt of the data. If the slave fails to acknowledge by leaving SDA high, then the master may abort the transmission by generating a STOP condition. When the master is receiving data from the slave, the master pulls down the SDA line during the clock pulse to indicate receipt of the data. After the last byte has been received the master leaves the SDA line HIGH (not acknowledge) and issues a stop condition to terminate the transmission.

### Write Protocol

The master begins communication with a START condition followed by the seven bit slave address and the  $R/\bar{W}$  bit set to zero, as shown in Figure 7. The addressed LTC4280 acknowledges this and then the master sends a command byte which indicates which internal register the master wishes to write. The LTC4280 acknowledges this and then latches the lower three bits of the command byte into its internal Register Address pointer. The master then delivers the data byte and the LTC4280 acknowledges once more and latches the data into its control register. The transmission is ended when the master sends a STOP condition. If the master continues sending a second data byte, as in a Write Word command, the second data byte is acknowledged by the LTC4280 but ignored, as shown in Figure 8.

### Read Protocol

The master begins a read operation with a START condition followed by the seven bit slave address and the  $R/\bar{W}$  bit

set to zero, as shown in Figure 9. The addressed LTC4280 acknowledges this and then the master sends a command byte which indicates which internal register the master wishes to read. The LTC4280 acknowledges this and then latches the lower three bits of the command byte into its internal Register Address pointer. The master then sends a repeated START condition followed by the same seven bit address with the  $R/\bar{W}$  bit now set to one. The LTC4280 acknowledges and send the contents of the requested register. The transmission is ended when the master sends a STOP condition. If the master acknowledges the transmitted data byte, as in a Read Word command, Figure 10, the LTC4280 repeats the requested register as the second data byte.

### Alert Response Protocol

When any of the fault bits in FAULT register D are set, an optional bus alert is generated if the appropriate bit in the ALERT register B is also set. If an alert is enabled, the corresponding fault causes the  $\overline{\text{ALERT}}$  pin to pull low. After the bus master controller broadcasts the Alert Response Address, the LTC4280 responds with its address on the SDA line and then release  $\overline{\text{ALERT}}$  as shown in Figure 11. The  $\overline{\text{ALERT}}$  line is also released if the device is addressed by the bus master. The  $\overline{\text{ALERT}}$  signal is not pulled low again until the FAULT register indicates a different fault has occurred or the original fault is cleared and it occurs again. Note that this means repeated or continuing faults do not generate alerts until the associated FAULT register bit has been cleared.

## APPLICATIONS INFORMATION

S	ADDRESS	$\bar{W}$	A	COMMAND	A	DATA	A	P
	1 0 a4:a0	0	0	X X X X X b2:b0	0	b7:b0	0	

- FROM MASTER TO SLAVE
- FROM SLAVE TO MASTER

A: ACKNOWLEDGE (LOW)  
 $\bar{A}$ : NOT ACKNOWLEDGE (HIGH)  
 R: READ BIT (HIGH)  
 $\bar{W}$ : WRITE BIT (LOW)  
 S: START CONDITION  
 P: STOP CONDITION

4280 F07

Figure 7. LTC4280 Serial Bus SDA Write Byte Protocol

S	ADDRESS	$\bar{W}$	A	COMMAND	A	DATA	A	DATA	A	P
	1 0 a4:a0	0	0	X X X X X b2:b0	0	b7:b0	0	X X X X X X X X	0	

4280 F08

Figure 8. LTC4280 Serial Bus SDA Write Word Protocol

S	ADDRESS	$\bar{W}$	A	COMMAND	A	S	ADDRESS	R	A	DATA	$\bar{A}$	P
	1 0 a4:a0	0	0	X X X X X b2:b0	0		1 0 a4:a0	1	0	b7:b0	1	

4280 F09

Figure 9. LTC4280 Serial Bus SDA Read Byte Protocol

S	ADDRESS	$\bar{W}$	A	COMMAND	A	S	ADDRESS	R	A	DATA	A	DATA	$\bar{A}$	P
	1 0 a4:a0	0	0	X X X X X b2:b0	0		1 0 a4:a0	1	0	b7:b0	0	b7:b0	1	

4280 F10

Figure 10. LTC4280 Serial Bus SDA Read Word Protocol

S	ALERT RESPONSE ADDRESS	R	A	DEVICE ADDRESS	$\bar{A}$	P
	0 0 0 1 1 0 0	1	0	1 0 a4:a0	0	1

4280 F11

Figure 11. LTC4280 Serial Bus SDA Alert Response Protocol

## APPLICATIONS INFORMATION

Table 1. LTC4280 Device Addressing (UH24 Package)

DESCRIPTION	DEVICE ADDRESS	DEVICE ADDRESS								LTC4280UH ADDRESS PINS		
		7	6	5	4	3	2	1	0	ADR2	ADR1	ADR0
Mass Write	BE	1	0	1	1	1	1	1	0	X	X	X
Alert Response	19	0	0	0	1	1	0	0	1	X	X	X
0	80	1	0	0	0	0	0	0	X	L	NC	L
1	82	1	0	0	0	0	0	1	X	L	H	NC
2	84	1	0	0	0	0	1	0	X	L	NC	NC
3	86	1	0	0	0	0	1	1	X	L	NC	H
4	88	1	0	0	0	1	0	0	X	L	L	L
5	8A	1	0	0	0	1	0	1	X	L	H	H
6	8C	1	0	0	0	1	1	0	X	L	L	NC
7	8E	1	0	0	0	1	1	1	X	L	L	H
8	90	1	0	0	1	0	0	0	X	NC	NC	L
9	92	1	0	0	1	0	0	1	X	NC	H	NC
10	94	1	0	0	1	0	1	0	X	NC	NC	NC
11	96	1	0	0	1	0	1	1	X	NC	NC	H
12	98	1	0	0	1	1	0	0	X	NC	L	L
13	9A	1	0	0	1	1	0	1	X	NC	H	H
14	9C	1	0	0	1	1	1	0	X	NC	L	NC
15	9E	1	0	0	1	1	1	1	X	NC	L	H
16	A0	1	0	1	0	0	0	0	X	H	NC	L
17	A2	1	0	1	0	0	0	1	X	H	H	NC
18	A4	1	0	1	0	0	1	0	X	H	NC	NC
19	A6	1	0	1	0	0	1	1	X	H	NC	H
20	A8	1	0	1	0	1	0	0	X	H	L	L
21	AA	1	0	1	0	1	0	1	X	H	H	H
22	AC	1	0	1	0	1	1	0	X	H	L	NC
23	AE	1	0	1	0	1	1	1	X	H	L	H
24	B0	1	0	1	1	0	0	0	X	L	H	L
25	B2	1	0	1	1	0	0	1	X	NC	H	L
26	B4	1	0	1	1	0	1	0	X	H	H	L

## APPLICATIONS INFORMATION

**Table 2. CONTROL Register A (00h)—Read/Write**

BIT	NAME	OPERATION			
		FUNCTION	A6	A7	GPIO PIN
A7:6	GPIO Configure	Power Good (Default)	0	0	GPIO = $\overline{C3}$
		Power Good	0	1	GPIO = C3
		General Purpose Output	1	0	GPIO = B6
		General Purpose Input	1	1	C6 = GPIO
A5	Test Mode Enable	Enables Test Mode to Disable the ADC; 1 = ADC Disable, 0 = ADC Enable (Default)			
A4	Mass Write Enable	Allows Mass Write Addressing; 1 = Mass Write Enabled (Default), 0 = Mass Write Disabled			
A3	FET On Control	On Control Bit Latches the State of the ON Pin at the End of the Debounce Delay; 1 = FET On, 0 = FET Off			
A2	Overcurrent Auto-Retry	Overcurrent Auto-Retry Bit; 1 = Auto-Retry After Overcurrent, 0 = Latch Off After Overcurrent			
A1	Undervoltage Auto-Retry	Undervoltage Auto-Retry; 1 = Auto-Retry After Undervoltage (Default), 0 = Latch Off After Undervoltage			
A0	Overvoltage Auto-Retry	Overvoltage Auto-Retry; 1 = Auto-Retry After Overvoltage (Default), 0 = Latch Off After Overvoltage			

**Table 3. ALERT Register B (01h)—Read/Write**

BIT	NAME	OPERATION
B7	Reserved	Not Used
B6	GPIO Output	Output Data Bit to GPIO Pin when Configured as Output. Defaults to 0
B5	FET Short Alert	Enables Alert for FET Short Condition; 1 = Enable Alert, 0 = Disable Alert (Default)
B4	EN State Change Alert	Enables Alert when EN Changes State; 1 = Enable Alert, 0 Disable Alert (Default)
B3	Power Bad Alert	Enables Alert when Output Power is Bad; 1 = Enable Alert, 0 Disable Alert (Default)
B2	Overcurrent Alert	Enables Alert for Overcurrent Condition; 1 = Enable Alert, 0 Disable Alert (Default)
B1	Undervoltage Alert	Enables Alert for Undervoltage Condition; 1 = Enable Alert, 0 Disable Alert (Default)
B0	Overvoltage Alert	Enables Alert for Overvoltage Condition; 1 = Enable Alert, 0 Disable Alert (Default)

## APPLICATIONS INFORMATION

**Table 4. STATUS Register C (02h)—Read**

BIT	NAME	OPERATION
C7	FET On	1 = FET On, 0 = FET Off
C6	GPIO Input	State of the GPIO Pin; 1 = GPIO High, 0 = GPIO Low
C5	FET Short Present	Indicates Potential FET Short if Current Sense Voltage Exceeds 1mV While FET is Off; 1 = FET is Shorted, 0 = FET is Not Shorted
C4	EN	Indicates if the LTC4280 is enabled when EN is low; 1 = EN Pin Low, 0 = EN Pin High
C3	Power Bad	Indicates Power is Bad when FB is low; 1 = FB Low, 0 = FB High
C2	Overcurrent	Indicates Overcurrent Condition During Cool Down Cycle; 1 = Overcurrent, 0 = Not Overcurrent
C1	Undervoltage	Indicates Input Undervoltage when UV is Low; 1 = UV Low, 0 = UV High
C0	Overvoltage	Indicates $V_{DD}$ or OV Input Overvoltage when OV is High; 1 = OV High, 0 = OV Low

**Table 5. FAULT Register D (03h)—Read/Write**

BIT	NAME	OPERATION
D7:6	Reserved	
D5	FET Short Fault Occurred	Indicates Potential FET Short was Detected when Measured Current Sense Voltage Exceeded 1mV while FET was Off; 1 = FET is Shorted, 0 = FET is Good
D4	EN Changed State	Indicates That the LTC4280 was Enabled or Disabled when EN Changed State; 1 = EN Changed State, 0 = EN Unchanged
D3	Power Bad Fault Occurred	Indicates Power was Bad when FB when Low; 1 = FB was Low, 0 = FB was High
D2	Overcurrent Fault Occurred	Indicates Overcurrent Fault Occurred; 1 = Overcurrent Fault Occurred, 0 = Not Overcurrent Faults
D1	Undervoltage Fault Occurred	Indicates Input Undervoltage Fault Occurred when UV went Low; 1 = UV was Low, 0 = UV was High
D0	Overvoltage Fault Occurred	Indicates Input Overvoltage Fault Occurred when OV went High; 1 = OV was High, 0 = OV was Low

**Table 6. SENSE Register E (04h)—Read/Write**

BIT	NAME	OPERATION
E7:0	SENSE Voltage Measurement	Sense Voltage Data. 8-Bit Data with 151 $\mu$ V LSB and 38.45mV Full Scale.

**Table 7. SOURCE Register F (05h)—Read/Write**

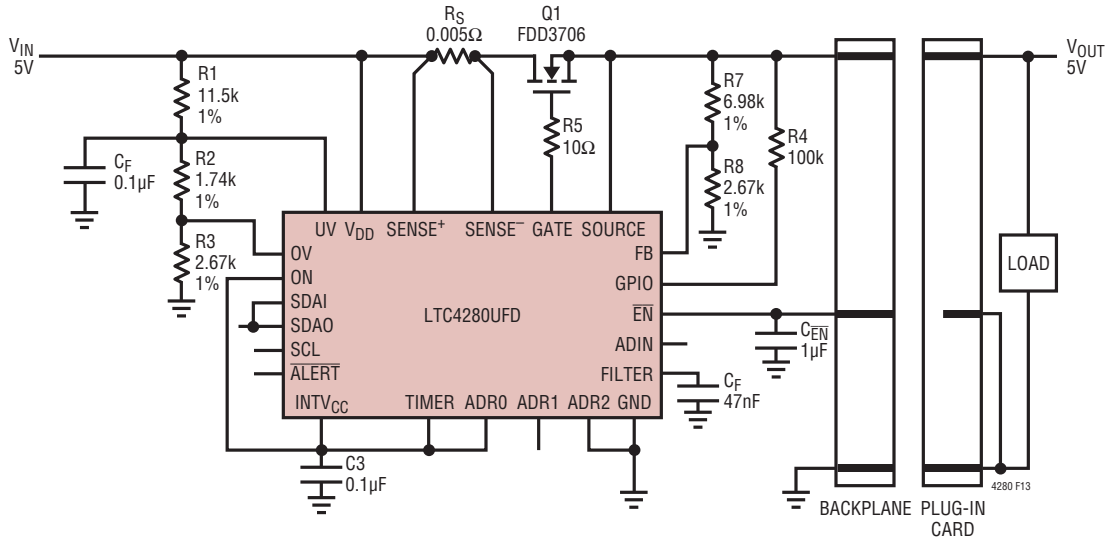
BIT	NAME	OPERATION
F7:0	SOURCE Voltage Measurement	Source Voltage Data. 8-Bit Data with 60.5mV LSB and 15.44V Full Scale.

**Table 8. ADIN Register G (06h)—Read/Write**

BIT	NAME	OPERATION
G7:0	ADIN Voltage Measurement	ADIN Voltage Data. 8-Bit Data with 4.82mV LSB and 1.23V Full Scale.

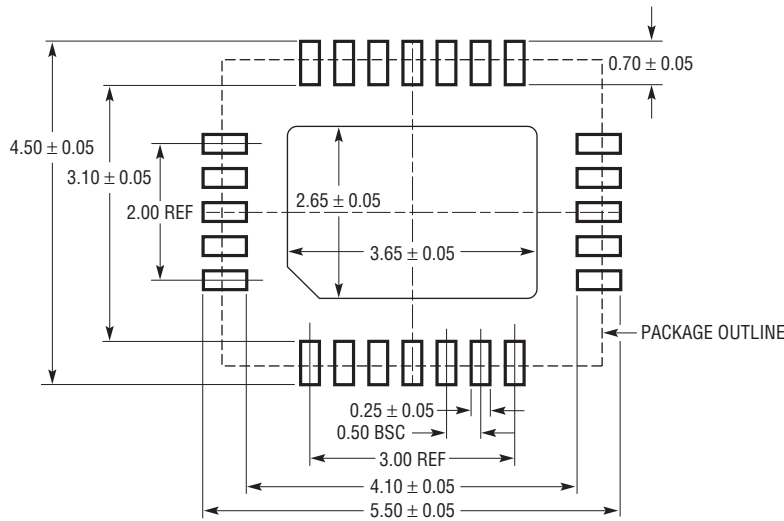
## TYPICAL APPLICATIONS

5V Backplane Resident Application with Insertion Activated Turn-On and a 5A Circuit Breaker

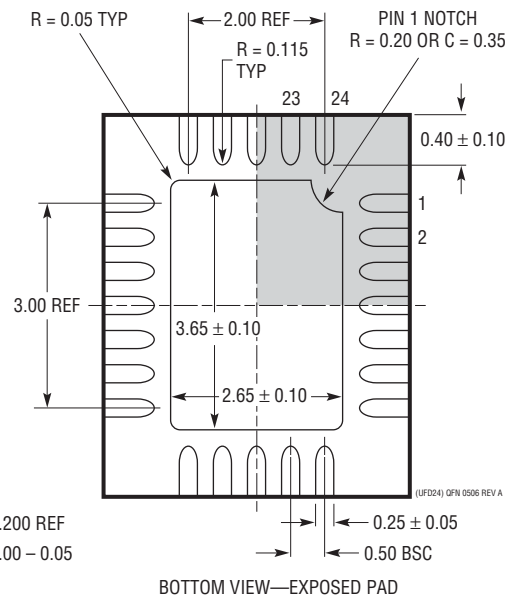
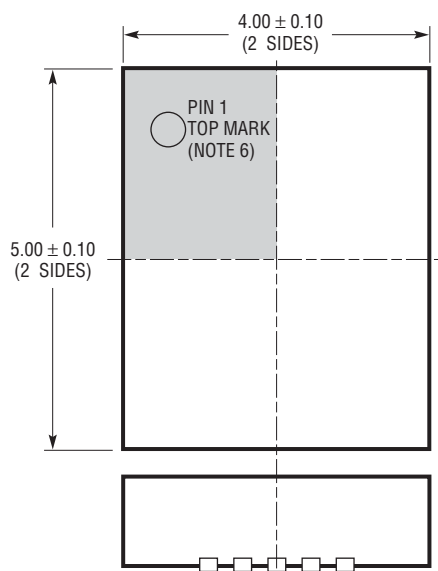


# PACKAGE DESCRIPTION

**UFD Package**  
**24-Lead Plastic QFN (4mm × 5mm)**  
 (Reference LTC DWG # 05-08-1696 Rev A)



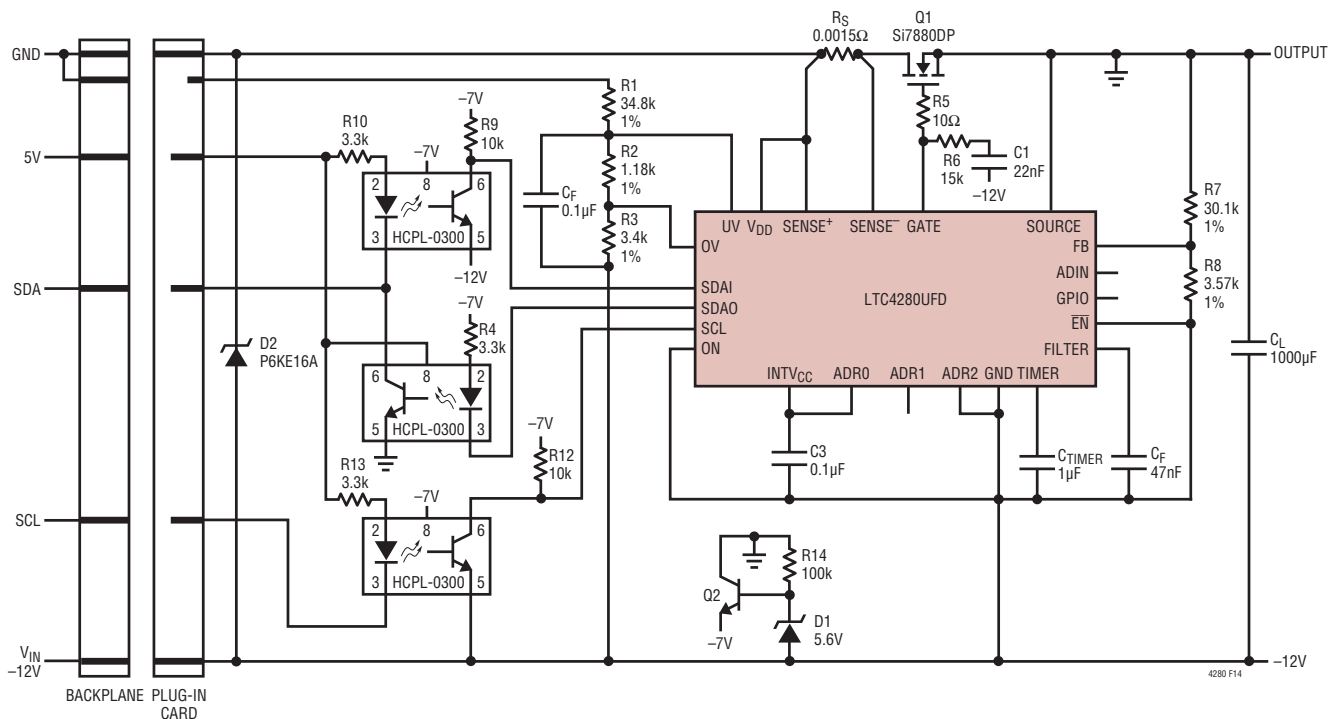
RECOMMENDED SOLDER PAD PITCH AND DIMENSIONS  
 APPLY SOLDER MASK TO AREAS THAT ARE NOT SOLDERED



- NOTE:
1. DRAWING PROPOSED TO BE MADE A JEDEC PACKAGE OUTLINE MO-220 VARIATION (WXXX-X).
  2. DRAWING NOT TO SCALE
  3. ALL DIMENSIONS ARE IN MILLIMETERS
  4. DIMENSIONS OF EXPOSED PAD ON BOTTOM OF PACKAGE DO NOT INCLUDE MOLD FLASH. MOLD FLASH, IF PRESENT, SHALL NOT EXCEED 0.15mm ON ANY SIDE
  5. EXPOSED PAD SHALL BE SOLDER PLATED
  6. SHADED AREA IS ONLY A REFERENCE FOR PIN 1 LOCATION ON THE TOP AND BOTTOM OF PACKAGE

## TYPICAL APPLICATION

### -12V Card Resident Application with Optically Isolated I<sup>2</sup>C and a 16.6A Circuit Breaker



## RELATED PARTS

PART NUMBER	DESCRIPTION	COMMENTS
LTC4151	High Voltage Current and Voltage Monitor with ADC and I <sup>2</sup> C	7V to 80V Single Voltage/Current Monitor with 12-Bit ADC
LTC4210	Single Channel, Hot Swap Controller	Operates from 2.7V to 16.5V, Active Current Limiting, SOT23-6
LTC4211	Single Channel, Hot Swap Controller	Operates from 2.5V to 16.5V, Multifunction Current Control, MSOP-8 or MSOP-10
LTC4212	Single Channel, Hot Swap Controller	Operates from 2.5V to 16.5V, Power-Up Timeout, MSOP-10
LTC4215	Single Channel, Hot Swap Controller with I <sup>2</sup> C Monitoring	Operates from 2.9V to 15V, 8-Bit ADC Monitors Current and Voltage
LTC4216	Single Channel, Hot Swap Controller	Operates from 0V to 6V, MSOP-10 or 12-Lead (4mm × 3mm) DFN
LTC4222	Dual Hot Swap Controller with ADC and I <sup>2</sup> C	2.9V to 29V Dual Controller with 10-Bit ADC, di/dt Controlled Soft-Start
LTC4245	Multiple Supply CompactPCI or PCI Express Hot Swap Controller with I <sup>2</sup> C	Internal 8-Bit ADC, di/dt Controlled Soft-Start
LTC4260	Positive High Voltage Hot Swap Controller with ADC and I <sup>2</sup> C	8-Bit ADC Monitoring Current and Voltages, Supplies from 8.5V to 80V
LTC4261	Negative High Voltage Hot Swap Controller with ADC and I <sup>2</sup> C	10-Bit ADC Monitoring Current and Voltages, Supplies from -12V to -100V

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